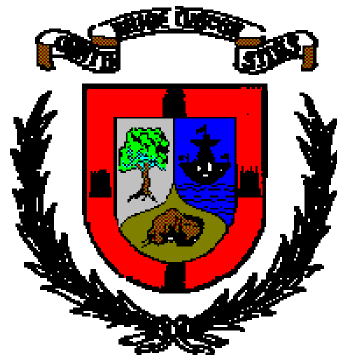
UNIVERSIDAD DE CANTABRIA

Departamento de Ingeniería de Comunicaciones



TESIS DOCTORAL

Cryogenic Technology in the Microwave Engineering: Application to MIC and MMIC Very Low Noise Amplifier Design

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Chapter IV

Cryogenic Temperature Effects on Microwave Devices

Cryogenic temperatures produce behavior changes in the materials that make up the microwave devices used in circuits and systems. These changes modify the circuit performance under such conditions, which can be advantageous if the circuit has been designed taking into account those changes.

In order to be able to design a circuit aimed for cryogenic operation with confidence on its final performance, this chapter gives a short introduction to the effects produced by low temperatures on the microwave devices; mainly transistors processed using indium-phosphide (InP) technology[1]. This technology has been selected for this study because is the best technology for very low noise and very low power consumption applications today. Variations on DC, RF and noise performance are shown through suitable measurements and, where possible, these results are related with different indium contents or compared with other technologies such as mHEMT (metamorphic structures formed by inclusion of indium within gallium-arsenide HEMT structures). The chapter concludes with a brief characterization of passive components such as capacitors and resistors with temperature, showing how very low temperatures ruin the performance of some of these components making them totally unadvisable for cryogenic designs.

[1] The data related with InP devices presented in this chapter were obtained during a four months stay in 2007 at the Department of Microtechnology and Nanosciencie (MC2) of the Chalmers University of Technology, Gothenburg, Sweden, within a collaboration project under the MC2ACCESS FP6 EU-financed programme.

4.1. Transistor Structure

Low noise transistors used in the applications dealt in this document need to have high channel mobility μ and peak velocity v_{peak} while maintaining a low DC power consumption. This is achieved through the use of narrow bandgap HEMTs; in particular, InP-based HEMTs are the best option [4.1], [4.2]. The main drawback of this technology is its high cost, related with a lack of maturity. On the other hand, the performance of the mature and less expensive GaAs-based (GaAs, gallium-arsenide) mHEMT technology is reducing differences with the InP-based technology [4.3], [4.4]. These reasons, together with the fact that InP-based HEMTs and GaAs-based mHEMTs are used in Chapters V and VI respectively, make this chapter to be focused on these technologies.

To create an n-type HEMT, the large bandgap material is doped with donor atoms. Due to the lower conduction band energy of the channel, electrons originating from the donors will transfer into the channel. This will create a two-dimensional electron gas (2DEG). Since the electrons are separated from the donor atoms, the ionized impurity scattering mechanism will decrease significantly compared to a bulk doped semiconductor transistor, e.g. a metal-semiconductor FET (MESFET). This is especially essential at cryogenic temperatures where ionized impurity scattering is the dominating scattering mechanism. As a consequence, μ and v_{peak} will be exceptionally high in HEMTs [4.5].

The electron mobility, μ, is the velocity per unit electric field and at low fields is described by (4.1), where e is the electric charge, τ is the average scattering time and m_e^* is the electron effective mass.

$$\mu = \frac{e\tau}{m_e^*} \tag{4.1}$$

The principal scattering mechanisms controlling the scattering time are phonon scattering and ionized impurity scattering. Phonons are an expression of the thermally stimulated lattice vibrations and hence are strongly dependent on temperature. When temperature is lowered the phonon scattering is reduced and therefore the average scattering time increases. This is the main reason of increased electron mobility at cryogenic temperatures for the same material.

On the other hand, the addition of indium content to the device channel ($In_XGa_{1-X}As$) reduces the electron effective mass improving the low field mobility accordingly [4.5]. Unfortunately, the indium content can not be increased indefinitely because this will induce strain due to lattice mismatch, which will produce the material to relax. At

the same time, the increment of indium content increases the separation between the Γ- and L- valleys in the conduction band [4.6], which is beneficial for v_{peak}. Devices on InP substrate enable higher indium contents than on GaAs substrate without material relaxation and hence both higher μ and v_{peak} are achieved with InP transistors. Moreover, for InP-based devices, v_{peak} is reached at lower electric fields providing lower DC power consumption. For all these reasons, InP-based transistors are preferable for microwave-millimeterwave cryogenic applications.

Figure 4.1 shows the epitaxial structure and a picture of the InP HEMT devices analyzed in this document. More information about the device structure and fabrication can be found in the following references [4.5], [4.7].

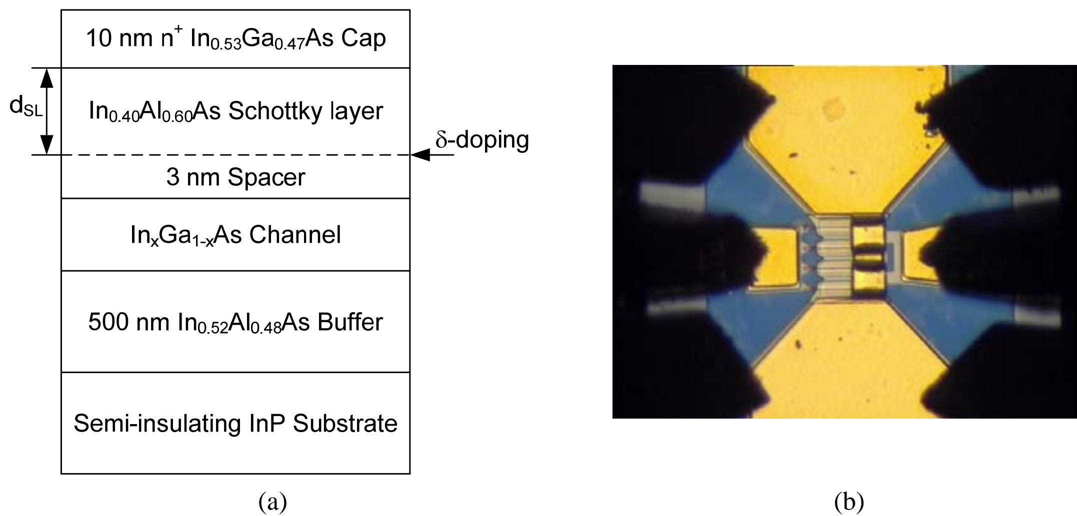


Fig. 4.1. Chalmers InP HEMT; (a) epitaxial structure: indium content in the channel is varied for obtaining different transistor performances; (b) photograph of a 4x50 μm device during measurement.

Different indium contents following the structure in Fig. 4.1 have been investigated. An indium content of 53% (x = 0.53) in the channel is the optimum value to avoid strain in the material since its lattice constant matches perfectly the InP lattice constant. These devices are called lattice-matched (LM) HEMTs. In this case, the Schottky layer is slightly modified to increase its indium content to 52% ($In_{0.52}Al_{0.48}As$), and the thickness of the Schottky layer is d_{SL} = 200 Å. The other InP devices analyzed are the so-called composite-channel (CC) HEMTs and they have an 80% (x = 0.80) indium content in the channel. The composite channel is formed by an alternation of InAs and GaAs layers between two lattice-matched InGaAs layers. This is required when using high percentage indium content to achieve a high electron confinement in the channel and to avoid the material relaxation. As a result of this high indium content, the energy band-gap is smaller in the channel of these devices. The thickness of CC-HEMT Schottky layer is d_{SL} = 120 Å. Finally, these devices are compared with the

commercial mHEMT technology from OMMIC[2], specifically with the D01MH process. This process follows an epitaxial structure similar to the one presented in Fig. 4.1 but with 40% (x = 0.40) indium content and a graded buffer (metamorphic) used to ensure a good transition between the GaAs substrate and the active layer, which is not lattice matched due to the high indium content [4.8]. All the structures considered in this chapter have the same gate-length, L_g = 130 nm, total gate-width, W = 200 μm (4x50 μm) and different δ-doping. A summary of the transistors characteristics is presented in Table 4.1.

Name	Substrate	% In content	L_g (nm)	W (μm)	Foundry
LM-HEMT	InP	53	130	200	Chalmers
CC-HEMT	InP	80	130	200	Chalmers
mHEMT	GaAs	40	130	200	OMMIC

Table 4.1. Characteristics of the transistors analyzed in this chapter.

4.2. Measurement Equipment and Setup

In order to obtain device measurements at room and cryogenic temperatures there is need of a cryo-probe station. At the moment of these measurements a home-made probe station was available at MC2 [4.9] which enables on-wafer device measurements up to 40 GHz and cooled down to 30 K.

For DC measurements, the semiconductor parameter analyzer model 4156B[3] from Hewlett-Packard was used. The bias signals were fed to the devices through the bias-Ts available in the E8364A network analyzer. Better results (less noisy) were found using the network analyzer internal bias-Ts than external bias-Ts. Moreover, it was checked that the internal bias-Ts of the 8510C network analyzer give worse results since they present higher leaks compared with model E8364A and hence small signals, like gate leakage currents, are hidden. All the measurement equipment was controlled by the GPIB bus using suitable programs running in a computer. This setup is described in Fig. 4.2 and it is shown in Fig. 4.3.

[2] OMMIC, 94453, Limeil-Brévannes Cedex, France. www.ommic.com

[3] Updated versions available from Agilent Technologies. www.agilent.com

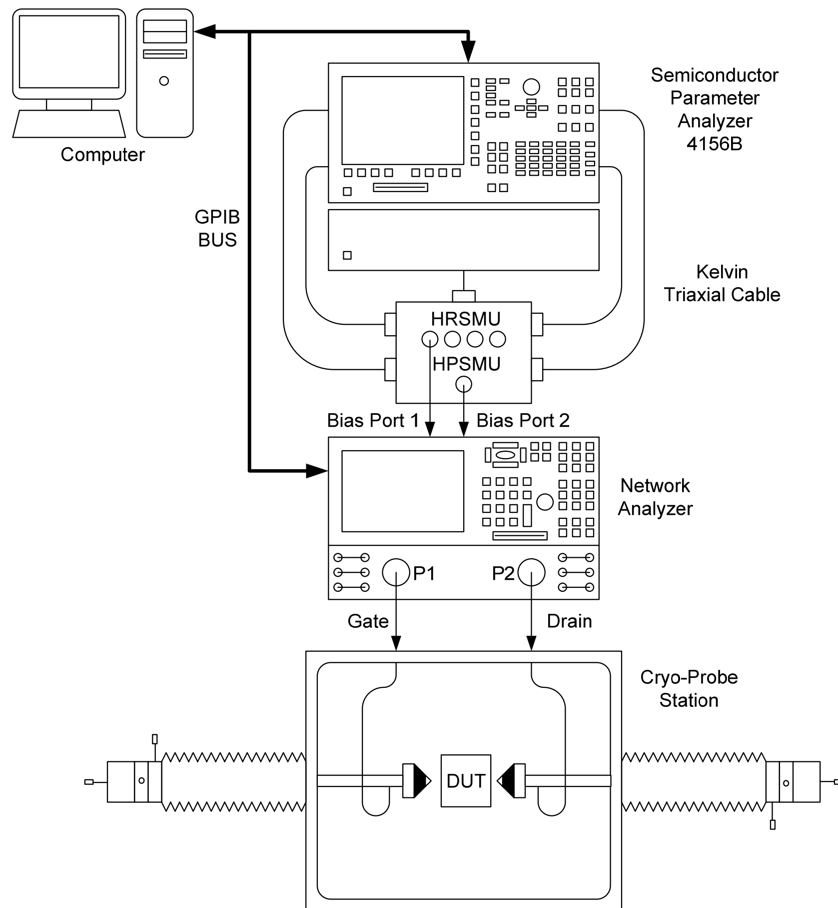


Fig. 4.2. Setup for the measurement of DC and RF device performance at MC2.

For RF measurements the same setup was used, but in this case the network analyzer measured the device S-parameters while the semiconductor parameter analyzer was used for providing the bias signals. The calibration process was carried out applying the LRM (Line-Reflect-Match) technique with the CS-5 calibration substrate from Picoprobe.

The devices were soldered to a small copper sheet screwed on to the cryostat cold-head using H20E[4] epoxy, and a temperature sensor was attached using Indalloy290[5] close to the devices location. In order to estimate the temperature gradient between the copper sheet and the transistor surface a preliminary test was carried out: a small dummy InP piece was pasted to the copper sheet and the temperature sensor was attached on its surface. It was found that, for a device thickness ≤100 μm, the temperature gradient was negligible, and therefore the temperature measured on the copper sheet can be considered as a real measurement of the transistor temperature.

[4] Epoxy Technology, Inc., 01821-3972, Billerica, MA, USA.

[5] Indium Corporation of America, Utica, NY 13502. USA.

(a) (b)

Fig. 4.3. Pictures of the measurement setup; (a) general view of the setup; (b) detailed view through the Dewar window of some transistors together with the calibration substrate.

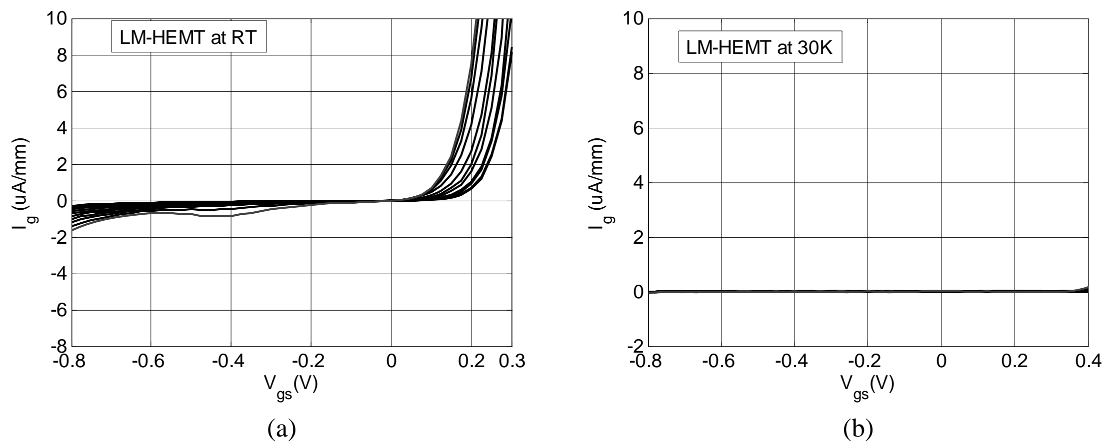
4.3. DC Measurement Results at Room and Cryogenic Temperatures

4.3.1. Gate-leakage current (I_g vs. V_{gs})

Gate-leakage current is produced by electrons crossing the Schottky barrier from the gate to the channel, originating the so-called shot noise [4.5] given by (4.2). At frequencies below 10 GHz the gate-leakage current of InP HEMTs can contribute significantly to the noise temperature [4.10], [4.11], and therefore this current should be minimized.

$$i_s^2 = 2e\left|I_g\right| \tag{4.2}$$

Results of the gate-leakage current for the different devices at room and cryogenic temperatures are shown in Fig. 4.4.



(a) (b)

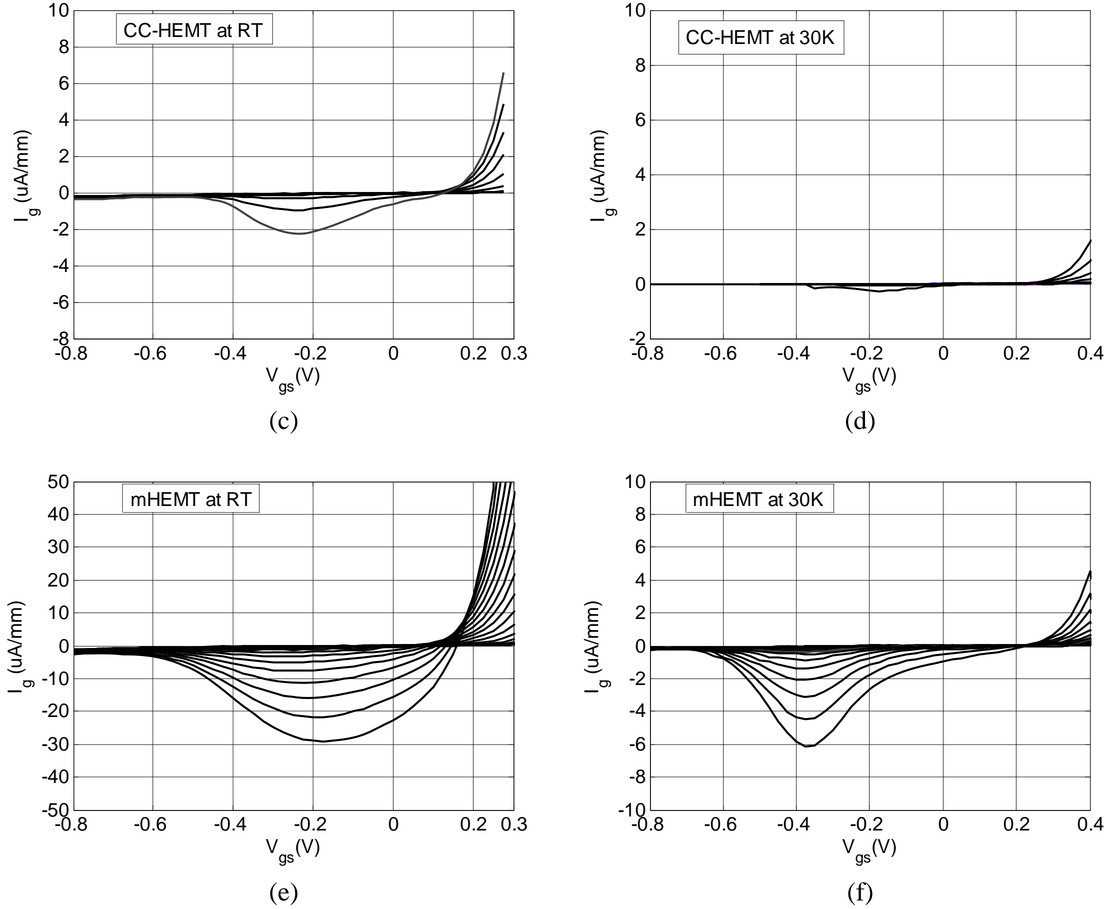


Fig. 4.4. Gate-leakage current versus gate-source voltage (I_g vs. V_{gs}) for the different transistors; (a) LM-HEMT (53% indium content) at RT; (b) LM-HEMT (53% indium content) at 30 K; (c) CC-HEMT (80% indium content) at RT; (d) CC-HEMT (80% indium content) at 30 K; (e) mHEMT at room temperature; (f) mHEMT at 30 K. Curves are for V_{ds} from 0 – 1 V with 0.1 V steps, except in mHEMTs where V_{ds} ranges from 0 – 2 V with 0.1 V steps.

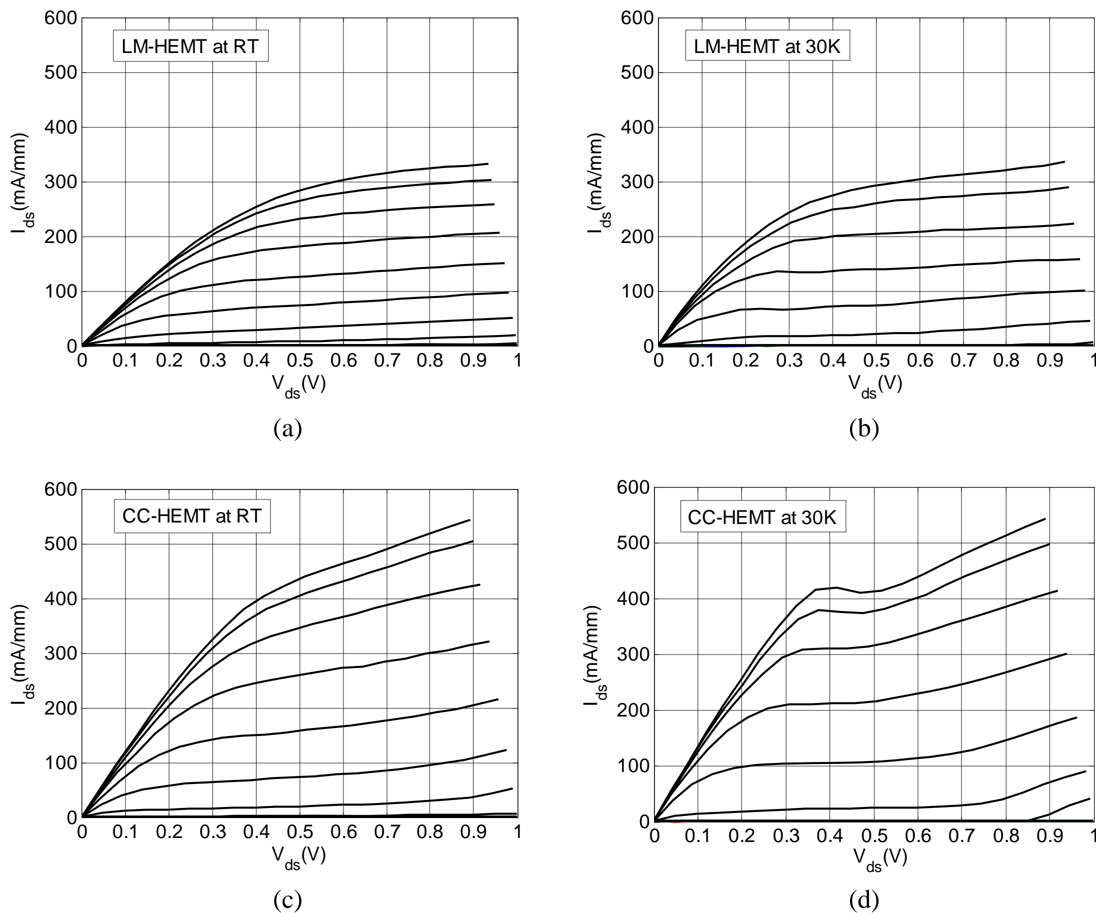
From Fig. 4.4 the impact ionization effect is clearly appreciated for high values of V_{ds}. The gate current is the result of two combined mechanism: first, the standard gate-leakage current associated to electron tunneling from the Schottky gate towards the channel, which increases monotonously at more negative gate voltages and more positive drain voltages; and second, the current related to impact ionization in the InGaAs channel. This last mechanism is produced when the electric field between gate and drain rises. Therefore electrons can gain enough energy to pull out valence electrons and create electron-hole pairs. The extra hole current adds to the tunneling current which increases the gate current. This effect is continued up to certain V_{gs} value where the high ionization rate can not be maintained and the number of holes starts to decrease, reducing the total gate current. Finally, for even more negative values of V_{gs}, only tunneling current exists [4.12]. The impact ionization shape is less noticeable for lower indium concentration rates due to the larger energy band-gap of these structures. Furthermore, for the mHEMT device the V_{ds} need to be increased up to 2 V to make this effect clearly noticeable; if V_{ds} is raised only up to 1 V, like in the InP structures, then

the plots of the mHEMT gate current are very similar to Figs. 4.4a and 4.4b with even less noticeable impact ionization shape. The magnitude of the impact ionization is also dependent on the channel thickness, the thinner the channel the smaller the effect [4.13].

At cryogenic temperature a great reduction of the impact ionization occurs, which is around ten times or more lower for InP devices and around five times lower for mHEMT devices. The reason for this variation may be the reduction of the ionization process due to the increase of the band-gap energy upon cooling, and also the loss of holes as a consequence of trapping mechanisms [4.12].

4.3.2. Output DC characteristic (I_{ds} *vs.* V_{ds})

The transistors output DC characteristics for both temperatures are presented in Fig. 4.5.



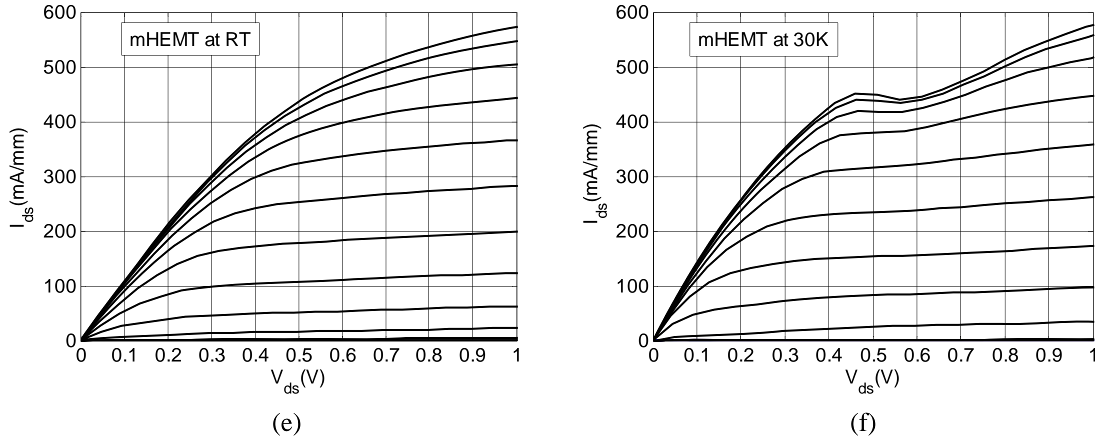


Fig. 4.5. Drain-source current versus drain-source voltage (I_{ds} vs. V_{ds}) for the different transistors; (a) LM-HEMT (53% indium content) at RT; (b) LM-HEMT (53% indium content) at 30 K; (c) CC-HEMT (80% indium content) at RT; (d) CC-HEMT (80% indium content) at 30 K; (e) mHEMT at room temperature; (f) mHEMT at 30 K. Curves are for V_{gs} from -0.8 – 0.3 V with 0.1 V steps.

From Fig. 4.5 two different effects could be analyzed. First one is the increase of I_{ds} at low V_{ds} upon cooling while there is a reduction of I_{ds} for higher values of V_{ds}. This effect is explained if it is considered that the drain current is limited by the saturation velocity v_{sat} [4.5]. Electrons velocity is increased when the temperature is lowered but only for low values of electric field (V_{ds}); this is due to improved electron confinement in the channel. On the other hand, this velocity tends to remain constant at high values of V_{ds} with temperature, i.e. the electrons reach v_{sat} [4.12]. The reduction of drain current for higher values of drain current could be related with the following effect.

The most important effect of low temperatures in transistors from Fig. 4.5 is the so-called *kink-effect*. Kink-effect consists of a sudden increase of the drain current at a certain value of the drain-source voltage and it leads to an increase of the output conductance g_{ds} (see Fig. 4.6), as well as the compression of the transconductance g_m and the lack of linearity. Some publications relate kink-effect to impact ionization [4.14], [4.15] while others claim it is due to trapping and detrapping mechanisms produced by deep levels in the Al containing layers [4.16], [4.17]. In the case of the analyzed devices, the kink-effect increases when cooling while the impact ionization decreases as shown in Fig. 4.4, therefore trapping mechanisms are more likely the reason of this behavior.

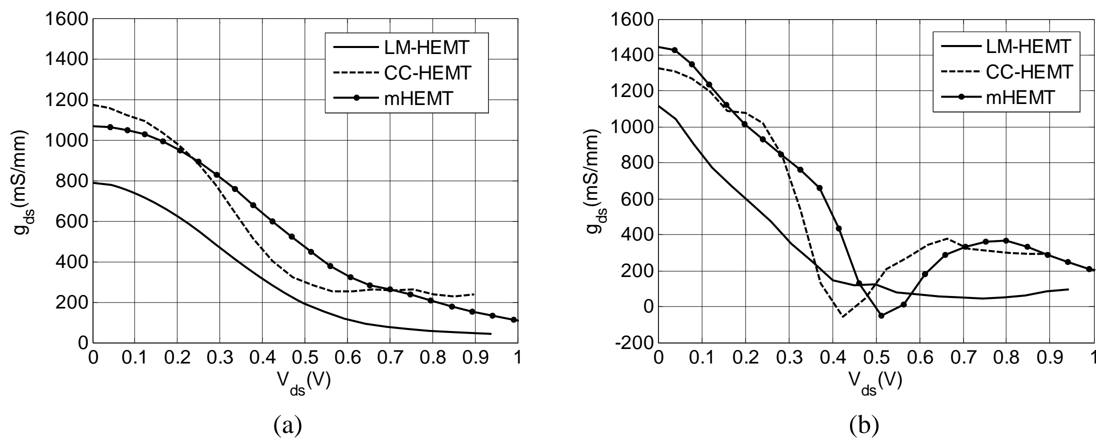


Fig. 4.6. Output conductance vs. drain-source voltage at (a) RT and (b) 30 K. V_{gs} = 0.2 V.

From Fig. 4.6, where kink-effect is better appreciated, it is seen that the composite-channel HEMT slightly shows this effect even at RT, whereas it appears in the mHEMT device only when it is cooled and it is not present in the LM-HEMT. Other analyzed LM-HEMT structures showed kink-effect under cryogenic temperatures and therefore not only the materials but also the fabrication process could be related with this effect.

In order to find out if traps are the reason of the kink-effect the best is to take a pulsed measurement of the device output characteristic. The pulsed technique uses pulsed DC signals to emulate high frequency behavior. Since the traps are not fast enough to respond to microwave frequencies the I_{ds} vs. V_{ds} curves should not show the kink-effect.

Since pulsed measurements could not be taken during the test campaign another way to get an idea of the high frequency output conductance has been explored. From S-parameters measurements the g_{ds} value can be modeled for many different bias points and then plotted versus V_{ds} comparing the results with the values extracted from DC measurements. This test is presented in Fig. 4.7 for the CC-HEMT for different values of V_{gs}.

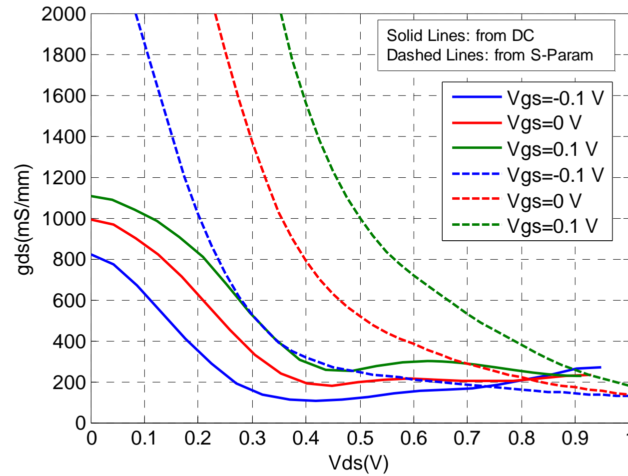


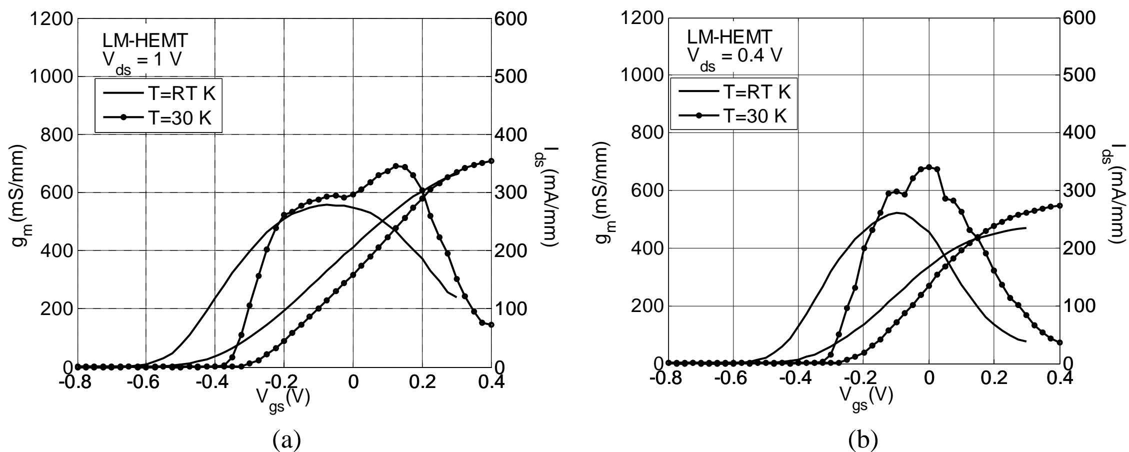
Fig. 4.7. RT output conductance vs. V_{ds} of the CC-HEMT from DC measurements (solid lines) and S-parameters modeling (dashed lines) for different values of V_{gs} = -0.1 V (blue), 0 V (red), and 0.1 V (green).

From Fig. 4.7 it is clear that the output conductance extracted from high frequency data does not present the positive slope region, therefore the I_{ds} is not affected by kink-effect. This test also seems to relate the kink-effect with trapping mechanisms.

Although kink-effect is present in DC output curves and this is an undesirable characteristic for transistors, this effect occurs at bias points without interest from the low noise point of view. A typical bias point for low noise operation at cryogenic temperatures is V_{ds} = 0.6 V and I_{ds} = 50-75 mA/mm. The analyzed kink-effect seems to occur above 300 mA/mm, which is an order of magnitude higher.

4.3.3. Transconductance (g_m vs. V_{gs} and I_{ds} vs. V_{gs})

Probably, the main transistor performance variation when it is cooled, together with the noise reduction, is the transconductance increase, as shown in Fig. 4.8, which leads to a gain improvement. This is mainly due to enhanced electron mobility at cryogenic temperatures produced by the reduction of scattering mechanisms as explained in Section 4.1.



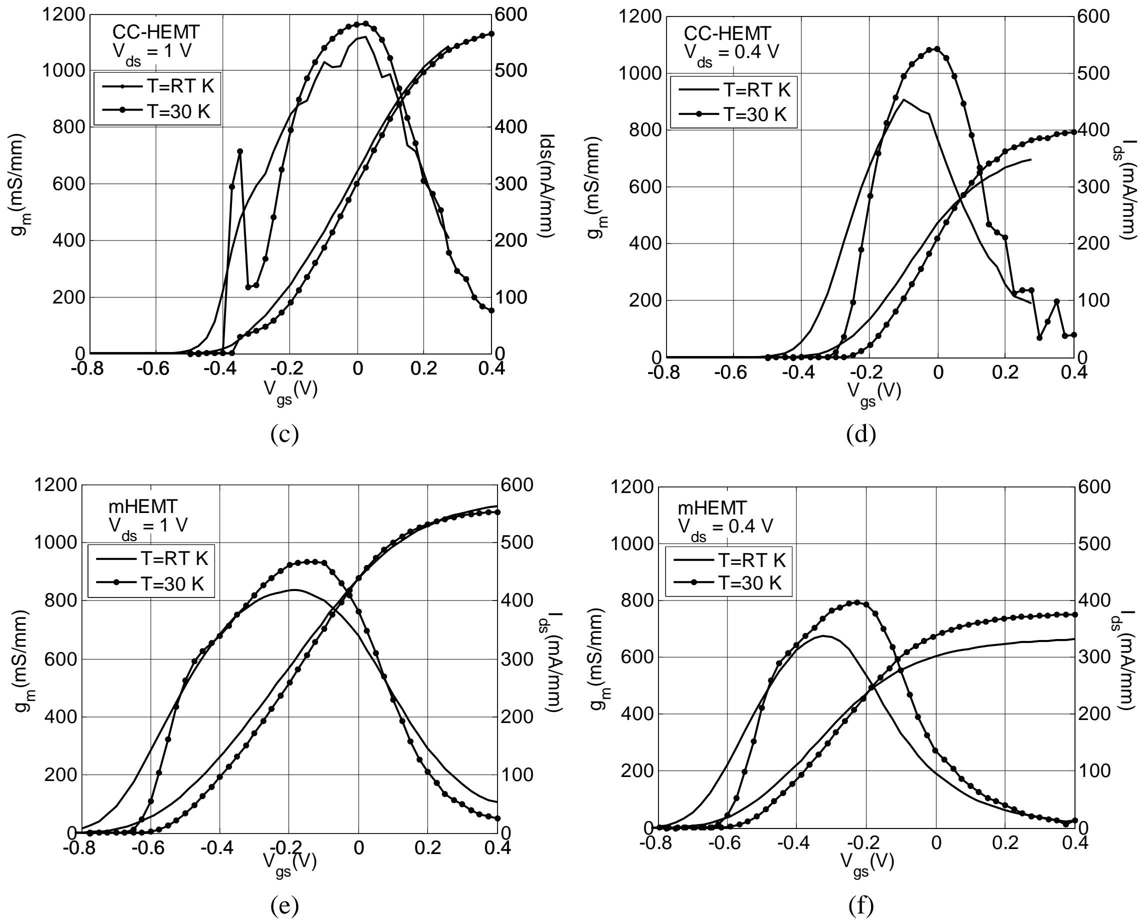


Fig. 4.8. Transconductance (g_m) and drain-source current (I_{ds}) vs. gate-source voltage at room and cryogenic temperature; (a) LM-HEMT for V_{ds} = 1 V; (b) LM-HEMT for V_{ds} = 0.4 V; (c) CC-HEMT for V_{ds} = 1 V; (d) CC-HEMT for V_{ds} = 0.4 V; (e) mHEMT for V_{ds} = 1 V; (f) mHEMT for V_{ds} = 0.4 V.

Cryogenic temperatures produce improved electron confinement, low field mobility and therefore increased electron peak velocity v_{peak}. At high bias the mobility is limited by the electron saturation velocity and hence the transconductance improvement is not as important as for low V_{ds} values. This is clearly shown in Fig. 4.8 where the same curves are compared for two different values of V_{ds} showing greater improvement of g_m upon cooling for lower values of drain-source voltage. Some non-monotonous points in these plots are probably due to oscillation problems during the measurements.

The increase of indium concentration in the devices produce the same effects [4.18] as lowering the temperature, as well as the decrease of carrier effective mass. Therefore the transconductance increases with indium concentration. However some works [4.19] have reported maximum indium content (around 70 %) to achieve the best performance beyond which there is observed degradation.

Finally, one well known effect of low temperatures in the transistor DC curves is the shift of the threshold voltage, which can be positive or negative. In the analyzed structures the threshold voltage is shifted toward positive values. Threshold voltage is

the gate-source bias at which the transistor starts to drain current and its shift at cryogenic temperatures is clearly appreciated in all plots from Fig. 4.8. This shift may occur due the reduction of carriers as a consequence of existing traps, and the shift of Fermi levels.

4.4. RF Measurement Results at Room and Cryogenic Temperatures

The high frequency performance in HEMTs is highly dependent on the transit-time. This time defines the cut-off frequency f_T (4.3), which is the frequency that produces unity current gain. The cut-off frequency also defines the maximum oscillation frequency f_{max} (4.4), which gives the frequency to obtain unity power gain. Therefore f_T and f_{max} gives an idea of the maximum operating frequency for a given device and thus an idea of the high frequency performance. In a simple approach, the higher these frequencies, the better the performance.

$$f_T = \frac{1}{2\pi\tau_T} \approx \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} \tag{4.3}$$

$$f_{\max} \approx \frac{f_T}{\sqrt{g_{ds}\left(R_i + R_g + R_s\right) + g_m R_g \dfrac{C_{gd}}{C_{gs}}}} \tag{4.4}$$

Where τ_T is the total transit time and the other parameters are from the transistor small signal model according with Fig. 4.9.

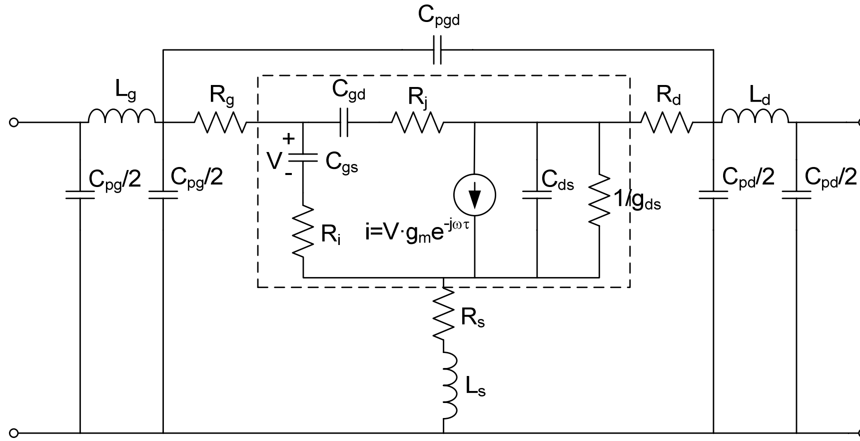


Fig. 4.9. HEMT small signal model

Intrinsic parameters in the small signal model are surrounded by the dashed line in Fig. 4.9 while the remaining parameters represent unwanted effects produced by pads and terminal accesses. From (4.3) and (4.4) it is clear that low capacitances and parasitic resistances are the key elements to obtain a transistor with superior high frequency performance. Figure 4.10 shows the S-parameter measurement results of the considered devices at room temperature and for similar bias points. Figure 4.11 presents the

measured S-parameters at cryogenic temperatures for the same devices but for the cooled LM-HEMT whose S-parameters could not be measured.

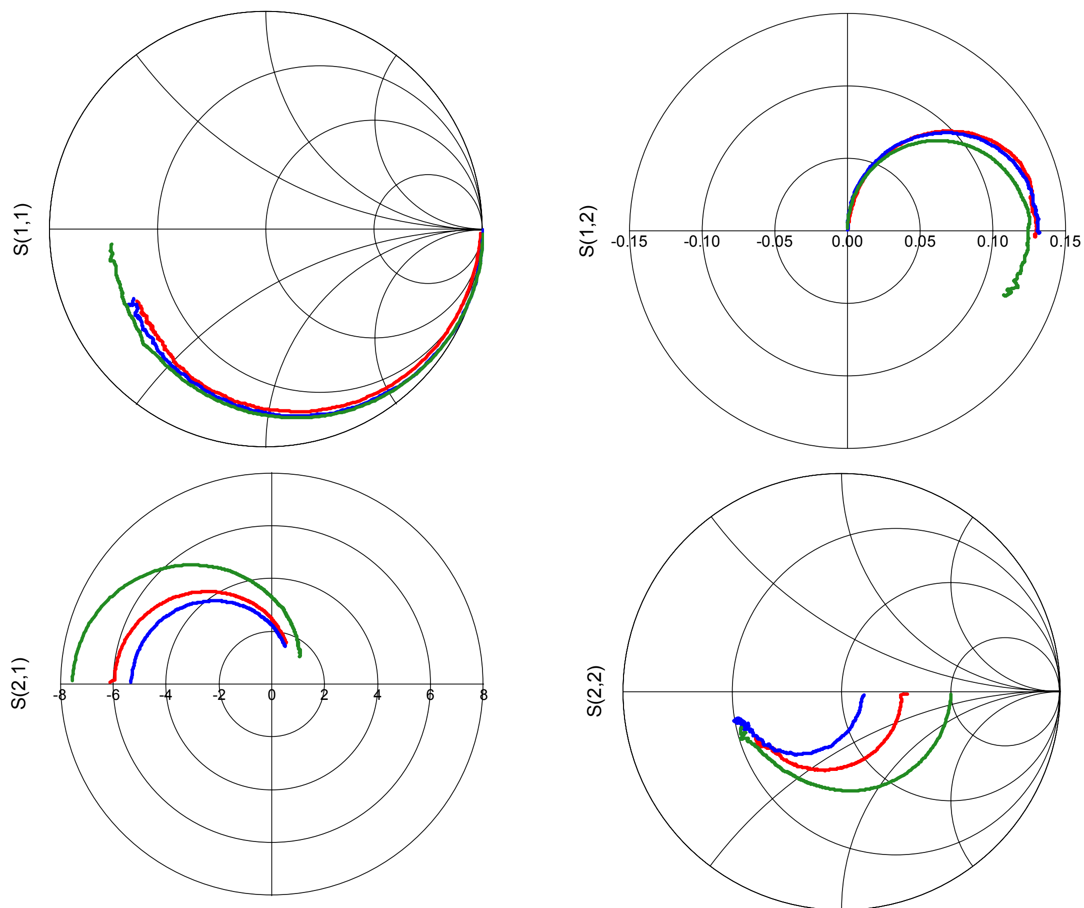


Fig. 4.10. S-parameter results from 0.05 – 40 GHz at RT for the LM-HEMT (red), CC-HEMT (blue) and mHEMT (green). Bias points are V_{ds} = 0.6 V, V_{gs} = -0.25 V and I_{ds} = 11 mA for the LM-HEMT; V_{ds} = 0.6 V, V_{gs} = -0.25 V and I_{ds} = 10.7 mA for the CC-HEMT; and V_{ds} = 0.7 V, V_{gs} = -0.5 V and I_{ds} = 11.1 mA for the mHEMT.

From Fig. 4.10, parameter S_{11} is quite similar for all devices; in the case of the mHEMT device a greater C_{gs} is responsible of the extended frequency dependence. Differences in R_{ds} and C_{ds} could explain the results of parameter S_{22}. The higher S_{21} of the LM-HEMT compared with the CC-HEMT at low frequency could be explained through the high value of R_{ds} in the first device, even when its g_m is lower.

The small signal model intrinsic parameters of these devices both at room and cryogenic temperatures are presented in Table 4.2. For the extraction of the small signal parameters an application developed in Chalmers following [4.20], [4.21] was used. This software is based in the cold-FET technique which needs at least three different S-parameters measurements to obtain the model: one with V_{ds} = 0 V and $V_{gs} << V_{pinch\text{-}off}$ from where the parasitic capacitances are extracted, one with V_{ds} = 0 V and $V_{gs} >> V_{pinch\text{-}off}$ (high gate current) from where the parasitic inductances and resistances are extracted, and one last measurement with the desired bias point to extract the intrinsic

parameters. Generally, the desired bias points for these applications are around the transconductance peak value.

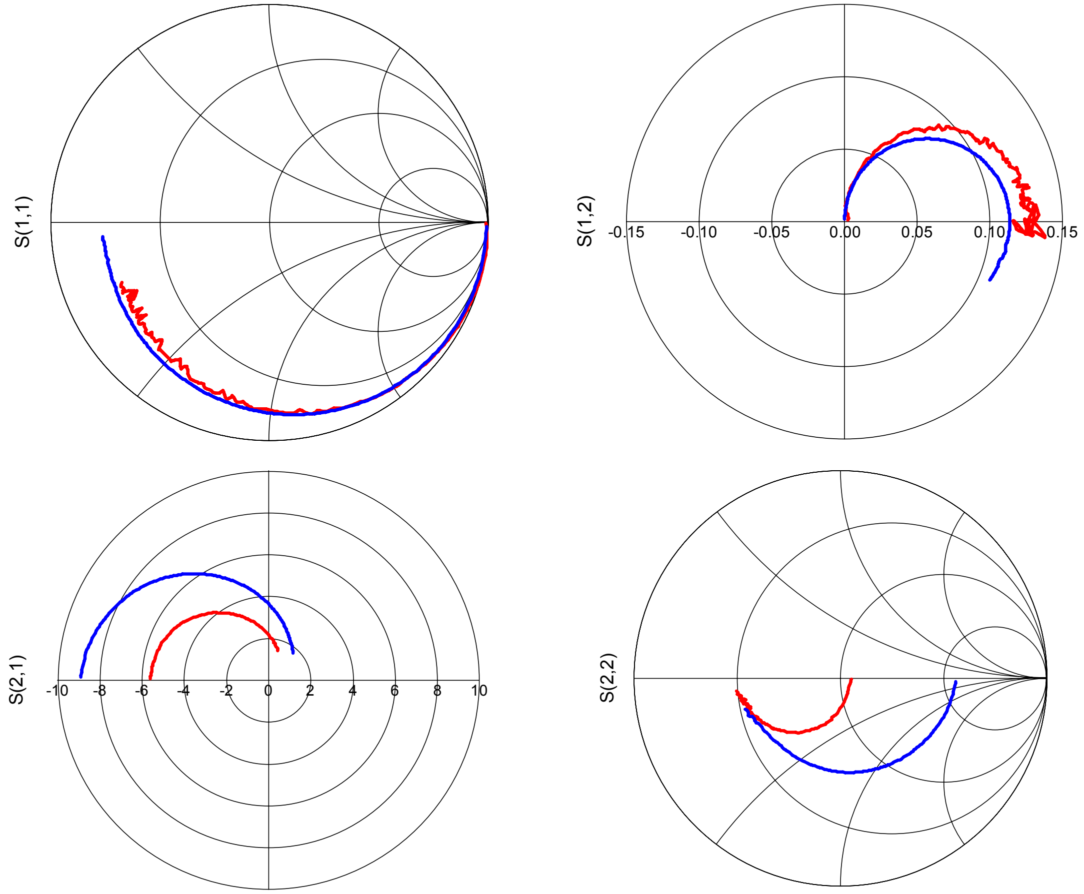


Fig. 4.11. S-parameter results from 0.05 – 40 GHz at 30 K for the CC-HEMT (red) and mHEMT (blue). Bias points are V_{ds} = 0.6 V, V_{gs} = -0.2 V and I_{ds} = 6 mA for the CC-HEMT; and V_{ds} = 0.7 V, V_{gs} = -0.45 V and I_{ds} = 7 mA for the mHEMT.

	LM-HEMT (RT)	CC-HEMT (RT)	mHEMT (RT)	CC-HEMT (30 K)	mHEMT (30 K)
C_{gs} (fF)	100.3	89.5	133.4	96.4	133.8
R_i (Ω)	5	2.7	4.2	4.1	3.4
C_{gd} (fF)	31.4	35.8	34.7	38.1	32.7
R_j (Ω)	14.6	7	0	13.2	4.2
C_{ds} (fF)	63.2	57.2	60	38.9	48.5
R_{ds} (Ω)	73	55.2	131.6	46.1	125
g_m (mS)	117.4	105.9	112	127.6	121.8
τ (psec)	0.09	0.35	0	0.26	0

Table 4.2. Small signal model intrinsic parameters of the analyzed transistors at room and cryogenic temperatures.

From the data in Table 4.2, the cooling process mainly produces a reduction of output resistance R_{ds} and an improvement of the transconductance, which is much more noticeable in the InP-based devices.

Finally, the models extracted for the CC-HEMT at room and cryogenic temperatures are compared in Fig. 4.12. The bias points selected for both temperatures are those indicated in Figs. 4.10 and 4.11 which are suitable for low noise applications, i.e. these bias points give a noise figure close to the minimum at each temperature. In the following section an easy calculation to get an estimation of the best bias point for noise from DC measurements is shown.

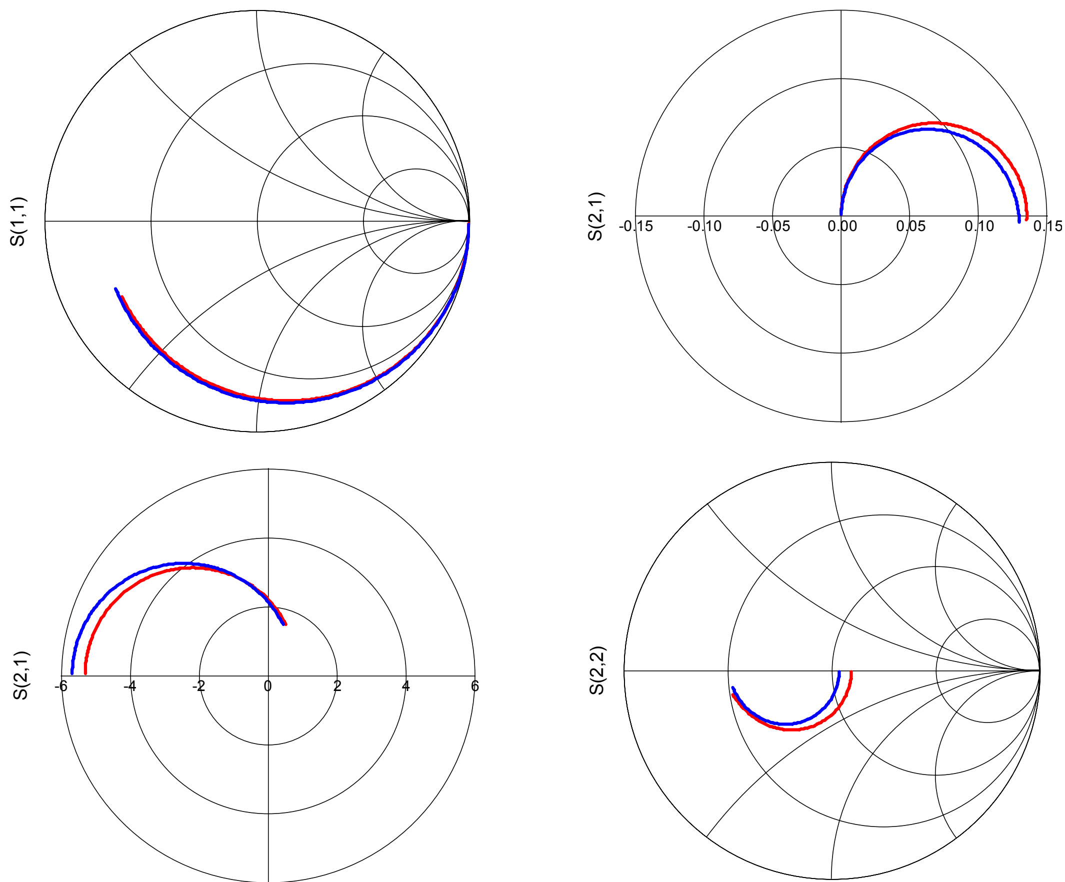


Fig. 4.12. Modeled S-parameters of the CC-HEMT at room (red) and cryogenic (blue) temperatures for suitable bias points for low noise at each temperature.

In Fig. 4.12 the similarity of the S-parameters at both temperatures for low noise bias points is demonstrated; therefore, in absence of a cryogenic model, room temperature parameters could be used for designing at cryogenic temperature as a first approximation without much error. Obviously, a good noise model is still needed for a cryogenic design.

4.5. Noise Performance at Room and Cryogenic Temperatures

Random behavior of carriers within the transistors generates different kinds of noise. Thermal noise is originated by the thermal agitation of the charge carriers inside the conductors without the need of any applied voltage. Therefore this noise is directly proportional to the temperature and theoretically it would be eliminated for $T = 0$ K.

Microwave engineering tries to take advantage of this property to reduce the receiver noise in applications where the received signal is of the same order of, and even lower, the receiver noise. In some applications like radio astronomy or deep space communications cryogenics is fundamental to enable signals reception.

In order to design cryogenic LNAs a transistor noise model is required at cryogenic temperatures. The most complete noise model is based in the so-called *noise parameters* extracted from multiple transistor noise measurements for different source impedances [4.22]. The accurate determination of the four noise parameters is difficult and many techniques have been proposed in the literature [4.23]-[4.27]. If the noise parameters are not available or they can not be measured, then they can be modeled using the small signal model parameters and two additional temperatures T_g and T_d [4.28]. These temperatures are assigned to the resistive elements in the small signal model: T_d is the equivalent temperature of the output resistance R_{ds} while T_g is the equivalent temperature of the remaining resistive elements in the small signal model. Noise parameters can be calculated following this noise model (4.5)-(4.8).

$$X_{opt} = \frac{1}{\omega C_{gs}} \tag{4.5}$$

$$R_{opt} \cong \frac{f_T}{f}\sqrt{\frac{R_{gs}T_g}{g_{ds}T_d}} \tag{4.6}$$

$$T_{\min} \cong 2\frac{f}{f_T}\sqrt{g_{ds}T_d R_{gs}T_g} \tag{4.7}$$

$$g_n = \left(\frac{f}{f_T}\right)^2 \frac{g_{ds}T_d}{T_0} \tag{4.8}$$

Where R_{gs} is the sum of R_g, R_s and R_i. In practice, it has been found that T_g can be set to ambient temperature T_{amb} and therefore only one temperature needs to be calculated to obtain the noise parameters. In order to calculate T_d there is a simple procedure consisting of assembling the transistor in the first stage of a well known and suitable LNA and to take a noise measurement. The noise result can be fitted by the optimization of this parameter and thus the value of T_d is obtained. In absence of a suitable LNA the drain temperature T_d can be estimated using (4.9) for InP-based devices [4.10].

$$T_d(K) = 300 + 6T_{amb} \tag{4.9}$$

The noise model is completed for the desired bias point but, is it possible to make an estimation a priori of the suitable bias point for low noise. Equation (4.7) gives the minimum noise temperature, which only can be achieved if the transistor is perfectly

matched to its optimum noise impedance. This equation can be further simplified obtaining (4.10) [4.29]. Hence, from DC measurements, the minimum of the function presented in (4.10) can be calculated providing the optimum bias point to minimize T_{min}.

$$f(V_{ds}, V_{gs}) \cong \frac{\sqrt{I_{ds}}}{g_m} \tag{4.10}$$

Equation (4.10) is plotted in Fig. 4.13 for the CC-HEMT at cryogenic temperature. The minimum in Fig. 4.13 is V_{gs} ~ -0.2 V and V_{ds} ~ 0.6 – 0.8 V which meets the bias settings given in Fig. 4.11.

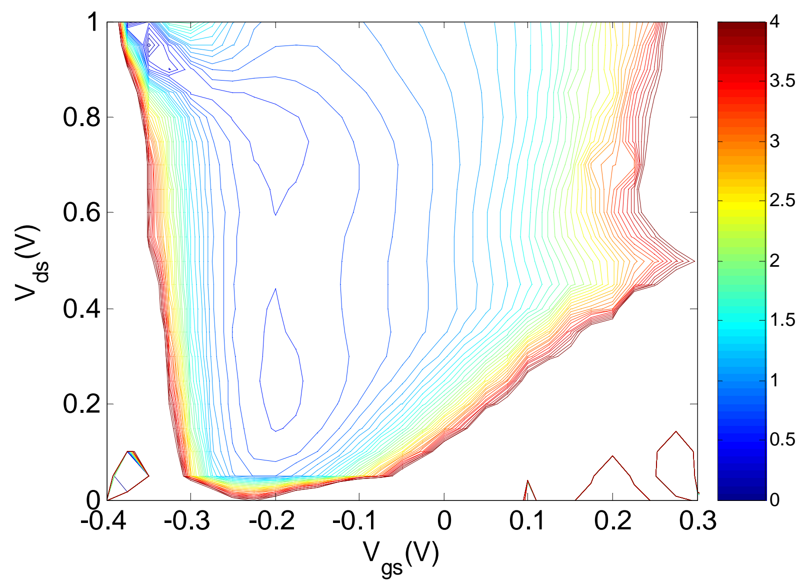


Fig. 4.13. Noise function (4.10) for the CC-HEMT at 30 K. Minimum noise optimum bias is V_{gs} ~ -0.2 V and V_{ds} ~ 0.6 – 0.8 V.

In order to demonstrate that the bias point suggested by (4.10) and Fig. 4.13 provides the minimum noise, a CC-HEMT from the same run as the transistor analyzed here was mounted in the first stage of a well known broadband LNA [3.31]. The results of the noise measurements for different bias points indicated in Table 4.3 are presented in Fig. 4.14.

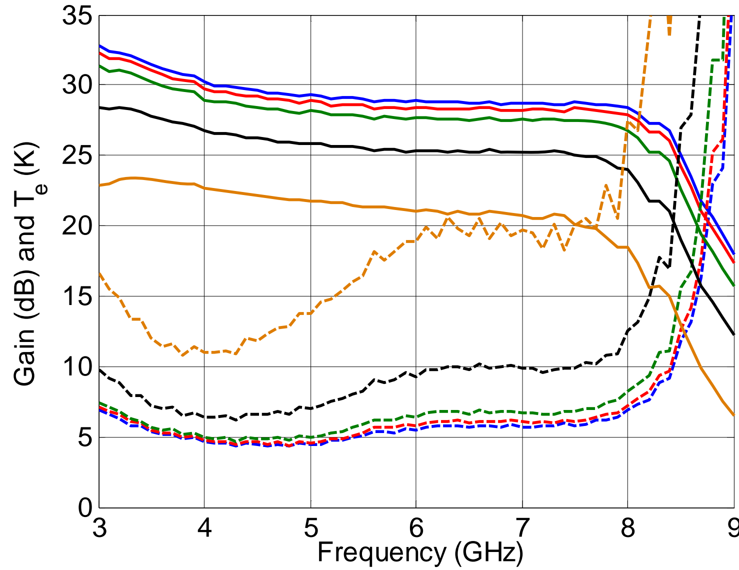


Fig. 4.14. LNA gain (solid lines) and noise (dashed lines) measurement for different bias points (BP) with a CC-HEMT in the first stage: BP1 (blue), BP2 (red), BP3 (green), BP4 (black), and BP5 (yellow). Ambient temperature T_{amb} = 10 K.

Bias	BP1	BP2	BP3	BP4	BP5
V_d (V)	0.8	0.6	0.4	0.2	0.1
I_d (mA)	5	4	3	1.5	0.8
V_g (V)	-0.16	-0.15	-0.15	-0.16	-0.16

Table 4.3. Bias points for the amplifier measured with the CC-HEMT in the first stage.

The bias point that produces minimum noise in Fig. 4.14 is very similar to the bias calculated from (4.10), hence the suitability of this equation to estimate low noise bias points is demonstrated.

To finish this section, the noise of the LM-HEMT and the CC-HEMT at room and cryogenic temperatures are compared in Fig. 4.15 through the use of the broadband LNA. The noise of the LM-HEMT is lower than of the CC-HEMT which is an unexpected result due to the improved performance of the later. This result could be related with a specific problem in the measured device, and thus further investigation would be needed in order to know the source of the extra noise.

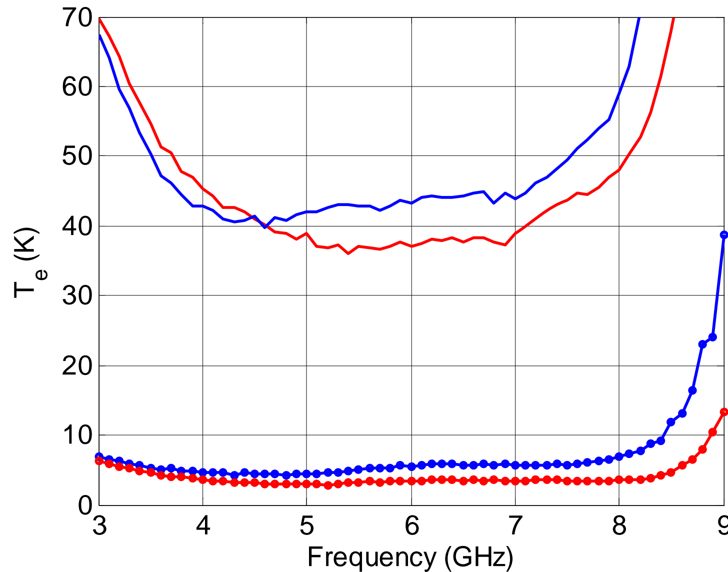


Fig. 4.15. LNA noise results with the LM-HEMT (red) and CC-HEMT (blue) in the first stage at room temperature (solid) and T_{amb} = 10 K (dots).

Figure 4.15 clearly shows the noise improvement upon cooling. This improvement is around one order of magnitude from room temperature to 10 K for InP-based and well-behaved transistors.

4.6. Low Temperature Effects on Microwave Passive Components

Passive components are very important in the LNA design, especially in the hybrid technology where different choices are available and a wrong selection may ruin the circuit performance. At microwaves and millimeterwaves frequencies only capacitors and resistors are used since inductors are made using planar technologies or bonding wires.

Some components used for long time in the DICOM for RT designs are analyzed in this section in order to find the suitable ones to be used under a cryogenic environment. The measurements are carried out using the precision LCR meter model E4980A from Agilent Technologies. This equipment enables the evaluation of LCR components (inductors, capacitors and resistors), materials and semiconductor devices in the 20 Hz to 2 MHz frequency range. For the measurement the DUT is attached to a dedicated test-fixture, which is designed with four connectors, and placed in the Dewar. The four connections are needed in order to make the system calibration. These connectors are routed in pairs to the DUT terminals. The calibration process is performed with the test-fixture left open, i.e. without the DUT installed, then the DUT is placed in the fixture and the measurement is taken. A computer program samples the parameters values and the temperature and these results are stored for data processing.

4.6.1. Capacitor 100 pF (ATC 118CL101M100TT)

This capacitor is usually used as the first element in the bias networks for monolithic chips at RT, i.e. the filtering component closest to the chip. It is a single layer capacitor with a high dielectric constant $\varepsilon_r = 16000$. This high value of dielectric constant enables high capacitances with very small sizes, which facilitates to mount several units close to the chip location. Figure 4.16 shows the capacitance value variation with temperature.

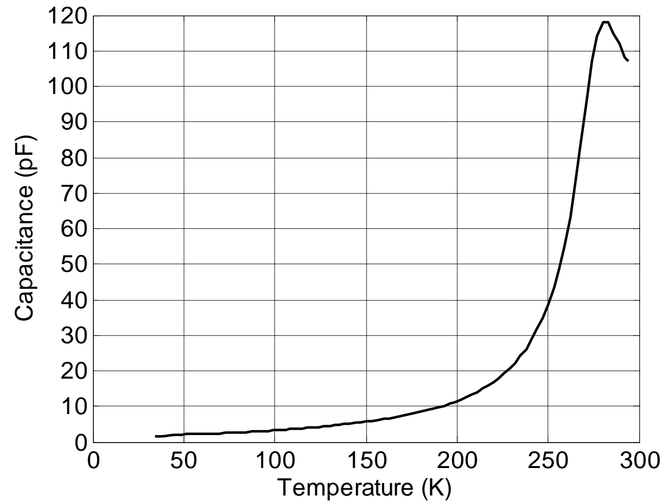
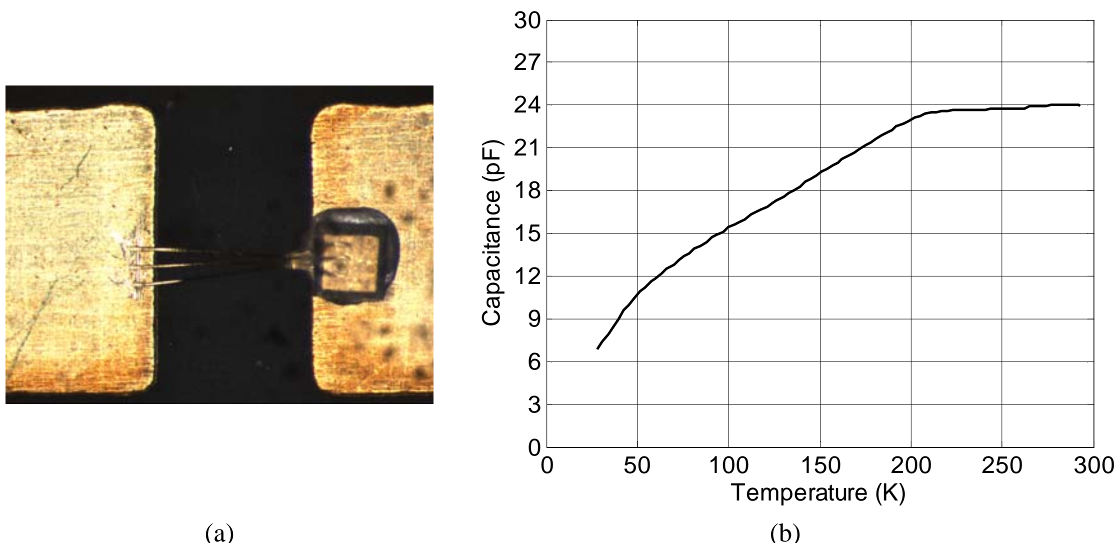


Fig. 4.16. Capacitance vs. temperature for the capacitor ATC 118CL101M100TT at 1 KHz.

The capacitance variation when the device is cooled is unacceptable for cryogenic applications. This high variation is produced by the high dielectric constant and hence such kind of components should be avoided.

4.6.2. Capacitor 22 pF (ATC 118DF220K100TX)

This capacitor comes from the same manufacturer and series than the previous one but it has lower capacitance and a lower dielectric constant $\varepsilon_r = 2000$. A picture of the capacitor mounted with three bonding wires for the measurement is shown in Fig. 4.17 together with the measurement result.



(a) (b)

Fig. 4.17. (a) Capacitor picture and (b) capacitance vs. temperature for the capacitor ATC 118DF220K100TX at 1 KHz.

This capacitor also shows a great dependence on temperature and it is completely useless for cryogenic designs. Therefore, for low temperature applications capacitors with very low dielectric constants should be used, preferably with values of $\varepsilon_r < 100$ [4.30].

4.6.3. Capacitor 22 pF (Siemens B37940K5220J060)

In this case it is a 0805 SMD multi-layer ceramic capacitor. The value of the dielectric constant is not provided by the manufacturer but it is rated as Class I ($\varepsilon_r < 200$). The measurement result for this capacitor is shown in Fig. 4.18.

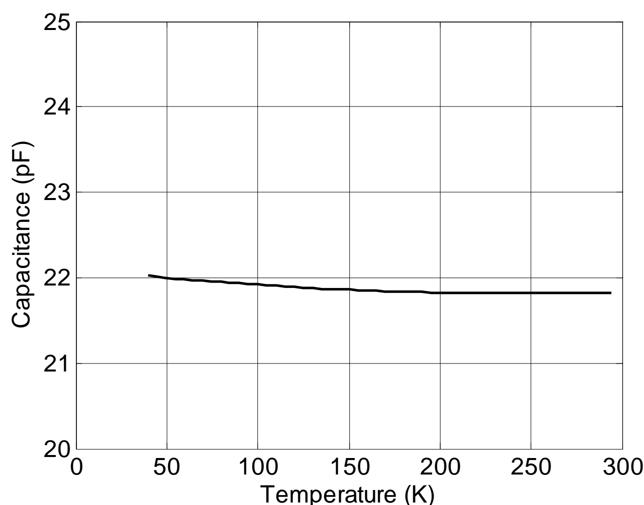
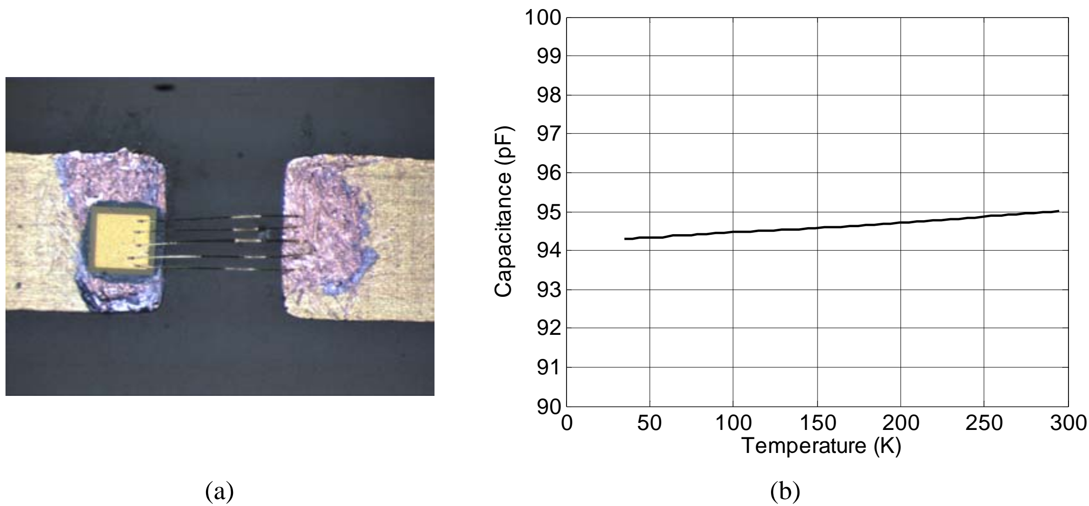


Fig. 4.18. Capacitance vs. temperature for the capacitor B37940K5220J060 at 1 KHz.

Since this capacitor presents a low dielectric constant the capacitance variation with temperature is small and hence this device is suitable for being used in cryogenic designs.

4.6.4. Capacitor 100 pF (Skyworks SC10002430)

This capacitor has been recently purchased by the DICOM to overcome the problems of the capacitor in Section 4.6.1. This MIS (Metal-Insulator-Semiconductor) capacitor has a dielectric composed of thermally-grown silicon dioxide over which a layer of silicon nitride is deposited. This two-layer dielectric produces a very low temperature coefficient of capacitance less than 50 ppm/ºC [4.31]. Figure 4.19 shows a picture of the measured capacitor and the measurement result.



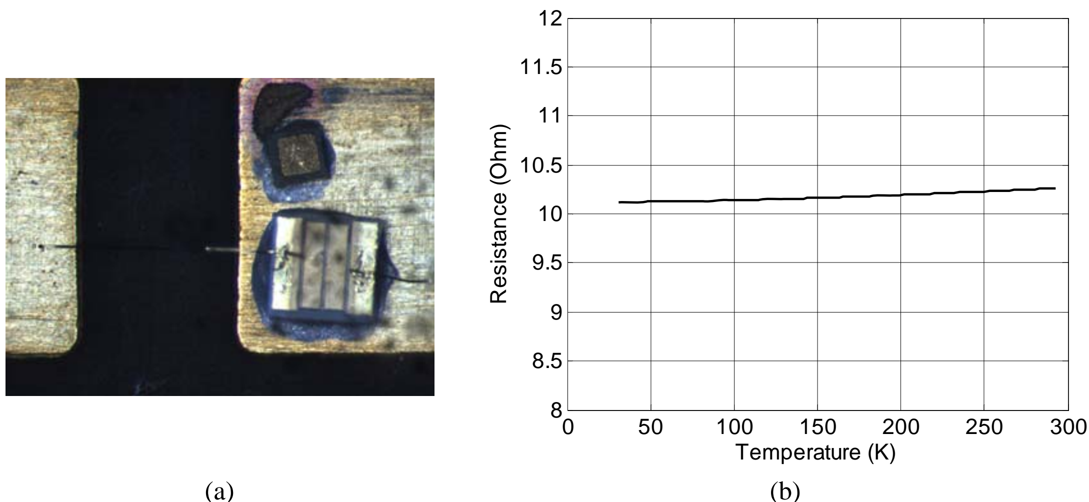
(a) (b)

Fig. 4.19. (a) Capacitor picture and (b) capacitance vs. temperature for the capacitor Skyworks SC10002430 at 1 KHz.

As can be appreciated from Fig. 4.19b this capacitor is very stable with temperature and it can be used for cryogenic designs with confidence.

4.6.5. Resistor 10 Ω (SOTA S0303DA10RFEW)

Finally a thin-film resistor is characterized over the temperature range of interest. The resistance is very stable with temperature according with Fig. 4.20b where its measurement result is plotted; therefore this resistor is suitable for cryogenic designs.



(a) (b)

Fig. 4.20. (a) Resistor picture and (b) Resistance vs. temperature for the resistor SOTA S0303DA10RFEW at 1 KHz.

4.7. Conclusions

This chapter has shown the effect of low temperatures on microwave devices, both active and passive. In the transistors, InP-based and metamorphic structures have been analyzed finding similar trends upon cooling. In general, from the DC results point of view, low temperatures produce a reduction of leakage current, an increase of transconductance, an increase in trapping mechanisms like the kink-effect, and a shift of the threshold voltage towards more positive values.

High frequency measurements have shown the gain improvement and noise reduction (up to an order of magnitude) at cryogenic temperatures. These measurements have also shown the similarity of the S-parameters in all the analyzed transistors and the small variation of them from RT to cryogenic temperature when the transistor is biased at the low noise optimum bias for both temperatures.

Finally, low frequency measurements carried out on passive capacitors and resistors have demonstrated their suitability for cryogenic designs. Capacitors with a dielectric constant $\varepsilon_r > 100 - 150$ have shown a great variation of capacitance with temperature and therefore they should be avoided in these designs. The analyzed resistor has presented good resistance stability in the temperature range.