UNIVERSIDAD DE CANTABRIA

Departamento de Ingeniería de Comunicaciones

TESIS DOCTORAL

Cryogenic Technology in the Microwave Engineering: Application to MIC and MMIC Very Low Noise Amplifier Design

Juan Luis Cano de Diego

Santander, Mayo 2010

Chapter V
Design of Cryogenic MIC Low Noise Amplifiers

Microwave integrated circuits (MIC), also known as hybrid technology circuits, are circuits constructed of individual devices, such as semiconductors and passive components, bonded or soldered to a substrate or printed circuit board (PCB). Hybrid technology has some advantages over the monolithic technology in which all the components (active and passive) are fabricated together in the same chip: discrete passive components have typically higher quality factors; MIC circuits enable post-production tuning to improve its performance; the design process, from initial design to final measurement, is less time consuming than in monolithic technology due to the absence of processing time in the foundry; and finally, the production cost is easily affordable for small quantities. But the main advantage over the monolithic technology that makes MIC technology the best option when extremely low noise amplifiers are required is that the noise of MIC amplifiers is still lower than the best monolithic design, if they are compared under the same conditions. This good performance in terms of noise is due to the small dielectric loss in the hybrid substrate compared with the monolithic substrate which reduces the input matching network resistive loss.

This chapter presents the development and first measurements of a cryogenic MIC low noise amplifier designed[1] in Ka band using InP technology transistors.

[1] The design was carried out during a six months stay at the Centro Astronómico de Yebes, CAY, Guadalajara, Spain, to be the prototype of a LNA demonstrator in the 25 – 35 GHz and to explore its performance for future projects.

5.1. Design Specifications

The cryogenic LNA is designed in the Ka-band which is of great interest for different radio astronomy applications such as VLBI (Very Large Baseline Interferometry), CMB measurements (for example in QUIJOTE project) and deep space communications (DSN, Deep Space Network). In order to design the prototype starting from real specifications, the requirements given in Table 5.1 are used as a guideline. The LNA is fully designed using available HRL[2] devices.

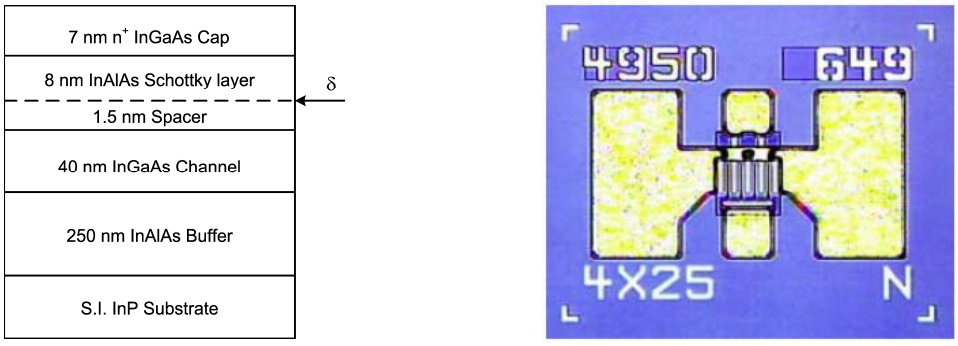
Frequency	25 – 33 GHz
Noise temperature	< 25 K at working temp. (target 15 K)
Gain	30 dB min.
Gain flatness	±1 dB (2 dB peak-to-peak)
Input reflection coefficient	-7 dB (target -14 dB) without isolator
Output reflection coefficient	-7 dB (target -14 dB) without isolator
Characteristic impedance	50 Ω
1 dB compression point	-7 dBm min.
Max. input power	0 dBm

Table 5.1. Design specifications for the cryogenic low noise amplifier.

5.2. Amplifier Electrical Design

5.2.1. Transistor model

The HRL devices are fabricated in InP HEMT technology with gate length of 100 nm. The basic epitaxial structure of these devices follows the sketch of Fig. 5.1 [5.1].



(a) (b)

Fig. 5.1. (a) Epitaxial structure of the HRL devices according with [5.1]; (b) Picture of one transistor with 100 μm gate width, dimensions are 0.350x0.285x0.100 mm³.

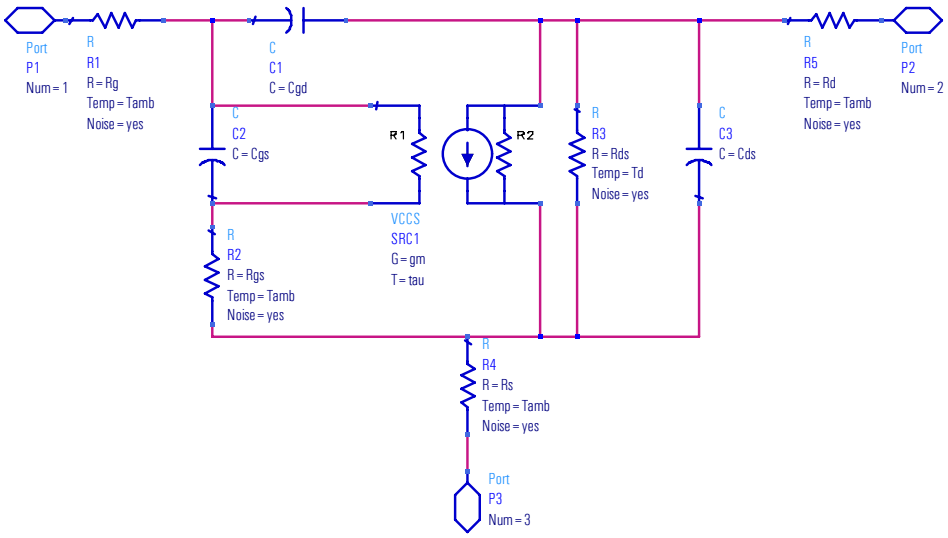
These devices give a transconductance around g_m = 600 mS/mm and an I_{ds} = 200 mA/mm with an optimum drain current for low noise operation of I_{ds} = 100 mA/mm. The transistors available at the CAY have been processed in a subsequent batch to those presented in [5.1] and therefore their characteristics may be different from Fig. 5.1.

[2] HRL Laboratories, LLC (formerly Hughes Research Laboratories), 90265-4797, Malibu, CA, USA.

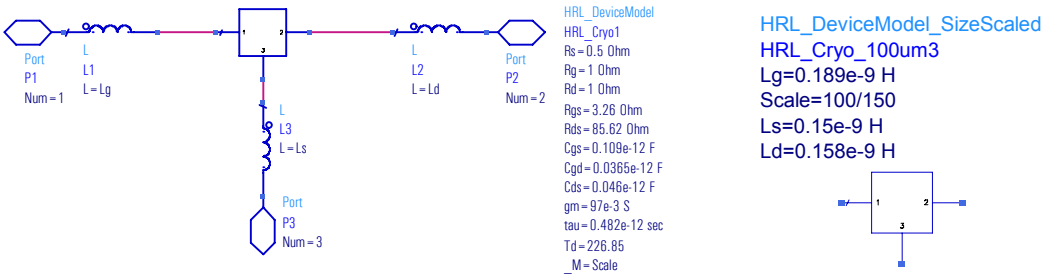
The small signal model of the transistor used for the amplifier design is a scaled version, down to 100 μm (4x25), from a 150 μm (6x25) model available at CAY. The original model was extracted from DC and S-parameter cryogenic measurements taken to a discrete transistor mounted on a microwave substrate. These measurements were not taken in a coplanar probe station and therefore the model includes the bonding wires used in the transistor assembly. It is assumed that these bonding wires represent the minimum wire length that can be achieved in an actual amplifier.

Transistor noise was modeled using the parameters of Pospieszalski's model [5.2], T_g and T_d. It has been found that at cryogenics all the resistive elements in the small signal model can be set to a temperature T_g equal to the ambient temperature except R_{ds} which is set to a temperature T_d. The value of T_d has been previously obtained through the measurement of a known amplifier with the transistor to be modelled as the first stage. From the noise measurement of this amplifier the parameter T_d can be optimized to fit the noise result.

The small signal and noise models used in the amplifier design are shown in Fig. 5.2. All the parameters are scaled to the transistor size except the inductors since they are dominated by the existing bonding wires. The bias point for this model is V_{ds} = 0.7 V and I_{ds} = 4 mA.



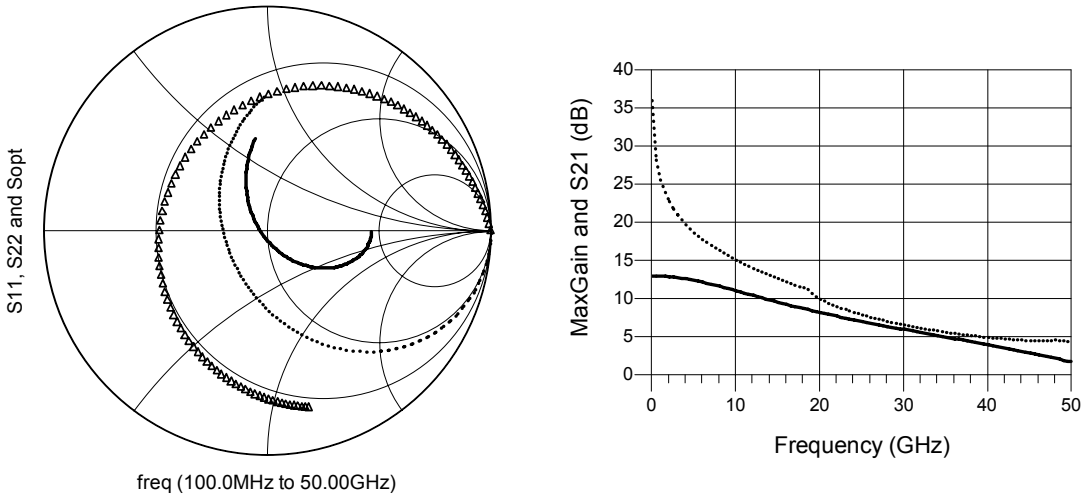
(a)



(b) (c)

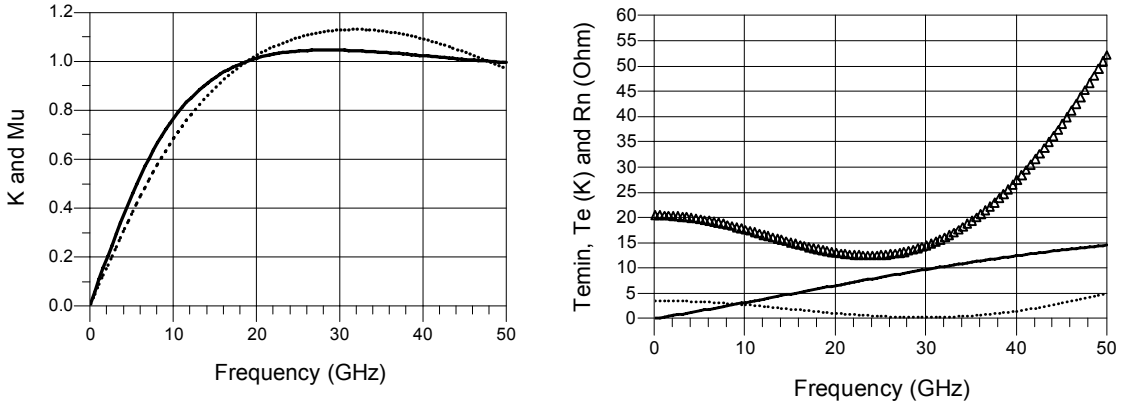
Fig. 5.2. Noise and small signal models for the HRL devices at cryogenics (T = 12.5 K) implemented in ADS[3]; (a) Scalable elements; (b) model with inductors included, T_g = 12.5 K, T_d = 500 K; (c) subcircuit ready to be used in ADS.

The available model is valid for cryogenic temperatures. For room temperature simulations the values of T_g and T_d need to be changed while the small signal parameters remain unchanged. In Fig. 5.3 some parameters of the simulated transistor model are presented. From Fig. 5.3b it is clear that the amplifier gain specified in Table 5.1 can not be achieved with four stages, however the amplifier is designed with four stages in order to not increase the design complexity since it is a prototype.



(a) (b)

[3] Advaced Design System (ADS) is a CAD tool from Agilent Technologies. The amplifier electrical design has been completely carried out in ADS except where noted.



(c) (d)

Fig. 5.3. Small signal and noise properties of the HRL transistor model at T = 12.5 K in the 0.1 to 50 GHz frequency range; (a) S_{11} (dots), S_{22} (solid) and Γ_{opt} (triangles); (b) S_{21} (solid) and maximum gain (dots); (c) Stability factors K (solid) and μ (dots); (d) Effective input noise temperature (triangles), minimum effective input noise temperature (solid), and the noise resistance (dots) which indicates the sensitivity of the noise match .

5.2.2. Substrate definition

For this amplifier the microwave substrate RT/Duroid® 6002[4] has been selected, which has shown its suitability for working at cryogenic temperatures in many designs from CAY and other laboratories. The main characteristic of this substrate to be used at cryogenics is its dielectric constant stability with temperature: ε_r = 2.94 (2.93) at T = 300 K (15 K) [3.31]. The characteristics of the Duroid 6002 substrate are presented in Table 5.2.

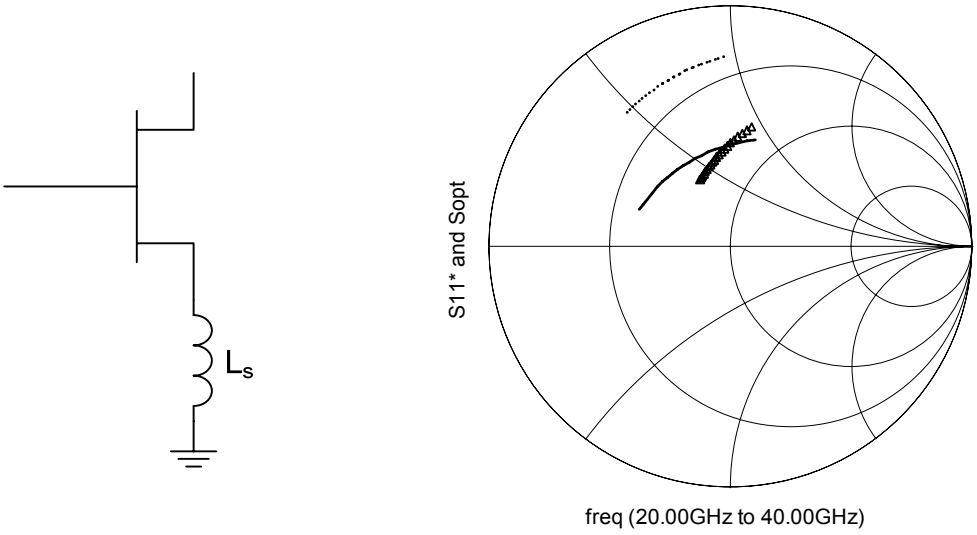
Dielectric constant (ε_r)	2.94
Height (h)	0.127 mm (5 mils)
Gold conductivity (σ)	$4.1 \cdot 10^7$ S/m
Metallization thickness (t)	25.5 μm
Loss tangent (tanδ)	0.0012

Table 5.2. Characteristics of Duroid 6002 substrate.

5.2.3. Inductive source feedback

The design of a low noise amplifier starts with the design of the input matching network. Usually the conjugate of the input reflection coefficient is far from the optimum impedance for noise; hence the designer has to decide between a good input matching and a low noise design. A well-know technique to overcome this problem is to use an inductive feedback in the transistor source [5.3]. This feedback reduces the gain of the amplifier, increases its stability and, if a suitable value for the inductance is selected, produces that $S^*_{11} \approx \Gamma_{opt}$ (see Fig. 5.4), achieving gain and noise matching simultaneously without additional contribution to noise (ideal inductance).

[4] Rogers Corporation, 85226-3415, Chandler, AZ, USA.



(a) (b)

Fig. 5.4. Inductive source feedback; (a) implementation; (b) effect on the Smith chart, Γ_{opt} (solid), S^*_{11} without feedback (dots), S^*_{11} with feedback (triangles).

For the HRL transistor, as the model includes inductive source feedback through the source bonding wires, it has been found that no additional feedback is required. Furthermore, the simulation has demonstrated that reduced inductance would improve the simultaneous matching. In order to reduce the inductance feedback from the model additional wires may be bonded in parallel in each source. The final inductance values obtained through circuit simulation are 0.15 nH for the first and fourth stages and 0.1 nH for the second and third stages.

Physical dimensions of the bonding wires are obtained optimizing their lengths to fit the desired inductances. The bonding wire model used for this optimization is shown in Fig. 5.5. Transistor layout includes two pads for the source then one wire is bonded in each pad in order to maintain the circuit symmetry. Since these two wires are electrically parallel then the total inductance is half of one wire; therefore each wire is optimized to have twice the desired total inductance. Thus, in the first and fourth stages the wires are designed to have 0.3 nH while in the second and third stages they need to have 0.2 nH. On the other hand gate and drain wires are unique and therefore they are optimized to have 0.19 nH in the gate and 0.16 nH in the drain.

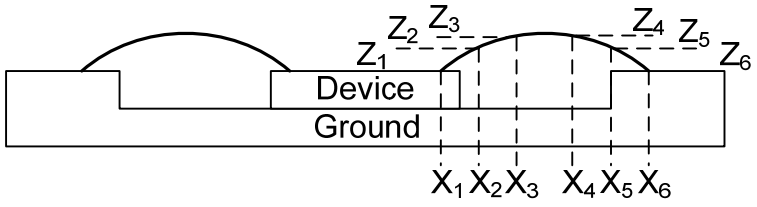
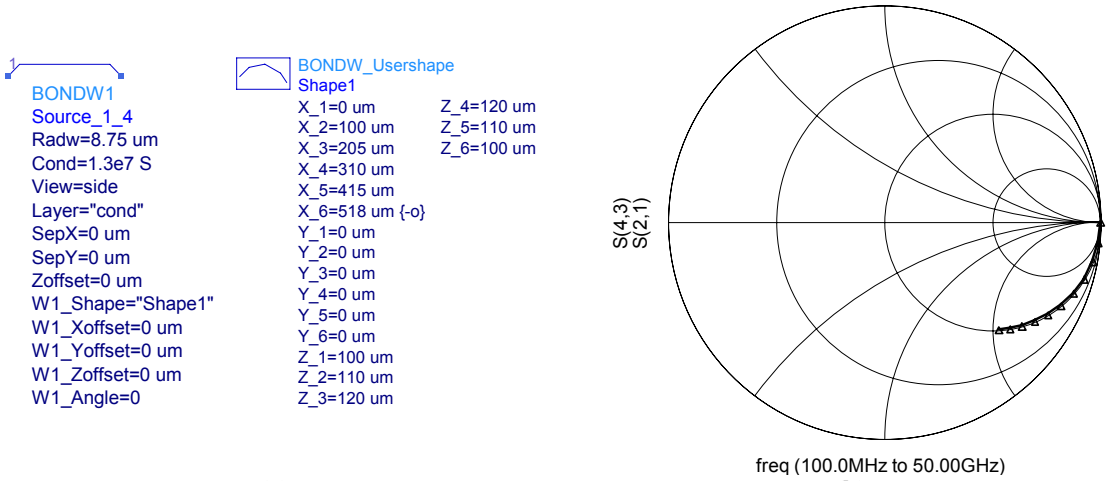


Fig. 5.5. Bonding wire model definition as a five-section wire. The total length and loop are set through the inclusion of six X-Y-Z coordinates in the ADS model. For all coordinates, y = 0.

The Z coordinates are fixed before the optimization and they are set equal for all the bonding wires with the following values: $Z_1 = Z_6 = 100$ μm, $Z_2 = Z_5 = 110$ μm, and $Z_3 = Z_4 = 120$ μm. The coordinate X_6 is optimized to achieve the desired inductance while the other X coordinates are kept more or less equispaced. Figure 5.6 shows the result of this optimization for a source wire with 0.3 nH inductance.



(a) (b)

Fig. 5.6. Optimization of one source bonding wire; (a) ADS model parameters; (b) Comparison of transmission parameters between the model (solid) and an ideal inductance of 0.3 nH (triangles).

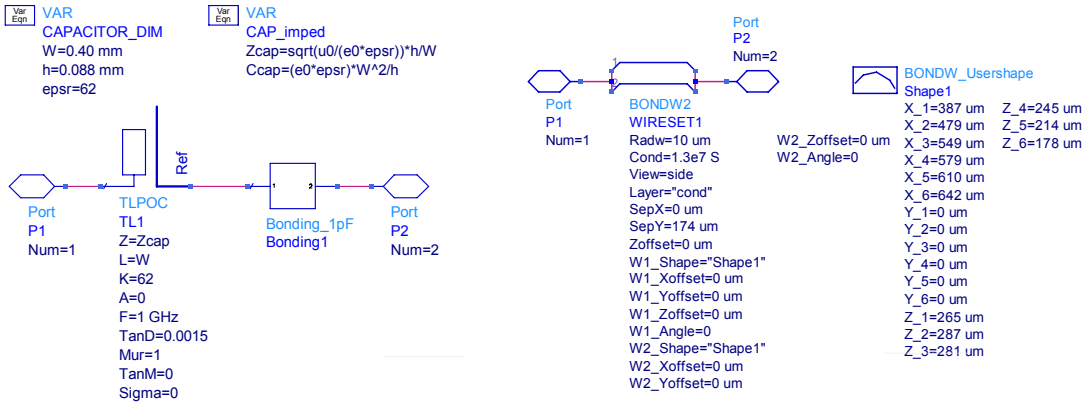
From Fig. 5.6 a wire with 518 μm length is equivalent to a 0.3 nH inductance. In the same way, a wire with 360 μm is equivalent to a 0.2 nH, a wire with 345 μm is used for all gates, and a wire with 300 μm is bonded in each drain.

5.2.4. Matching networks

All the matching networks are made of microstrip elements except the bypass capacitors. At these frequencies the high and low impedance microstrip lines are equivalent to inductors and capacitors.

Among the different elements in the matching networks the capacitive element just before the biasing networks is of special importance. This element has to filter the in-band RF signal to avoid leaks to the biasing network and, at the same time, acts as a tuning element controlling the effect of the resistive elements of the biasing network, which are used for stabilization, in the performance within the frequency band. For this amplifier the capacitive element is made with a radial stub since it is supposed that its model presents fewer uncertainties than the home-made model of an actual capacitor. Moreover, the radial stub enables to achieve intermediate capacitive values just varying the stub radius, thus improving the circuit fine tuning. The dimensions of the radial stubs used in this design are equivalent to capacitances around 5 pF, which represents a good short-circuit in the band.

The bypass capacitors block the DC signals to isolate the biasing of each amplifier stage from each other. The bypass capacitors have a value of 1 pF and they are of the ATC111[5] series. This value is a little bit short to be a good short-circuit in the frequency band but there is a model available in the CAY which has been proven successfully in previous designs and therefore it was decided to use this component. The capacitor model is shown in Fig. 5.7.

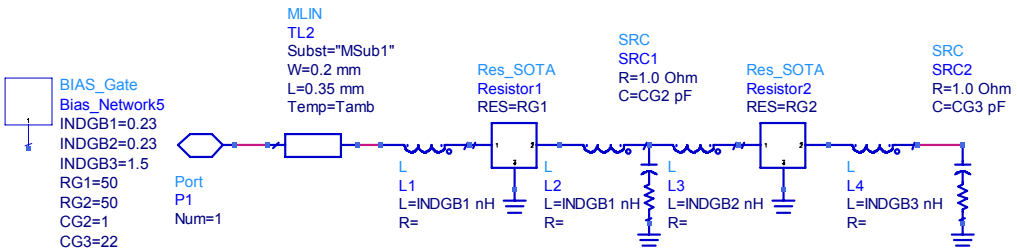


(a) (b)

Fig. 5.7. Definition of the ATC111 1 pF capacitor model in ADS; (a) model as a transmission line; (b) model of the bonding wires used in the assembly.

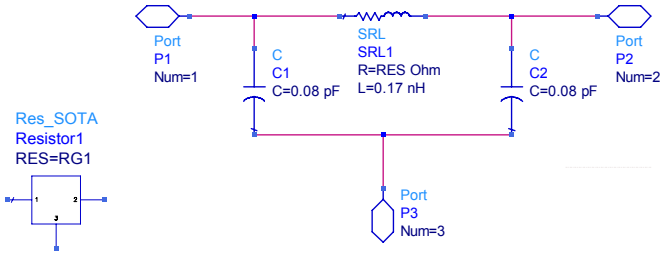
5.2.5. Biasing networks

The purpose of the biasing networks is to provide a path for DC signals to bias the transistors and, at the same time, to stabilize the circuit out-band. These networks are made of series resistors which stabilize the circuit, capacitors to ground to filter the RF signals at different frequencies, and parasitic inductances introduced by the wires bonded in the assembly. The gate biasing network is shown in Fig. 5.8 whereas the drain biasing network is presented in Fig. 5.9.



(a)

[5] American Technical Ceramics Corp., 11746, Huntington Station, NY, USA.



(b)

Fig. 5.8. Gate biasing network implemented in ADS; (a) complete network; (b) model of SOTA resistor.

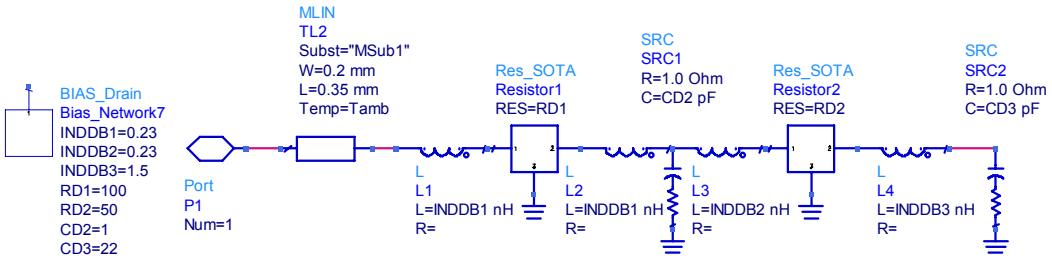


Fig. 5.9. Drain biasing network.

For these networks resistors from the S0302 series from SOTA[6] and capacitors from the ATC111 series for the 1 pF value and from the ATC100A series for the 22 pF value have been selected. Following the components shown in Figs. 5.8 and 5.9 there are other components used as a filter at very low frequencies. These components are a 50 Ω resistor from S0705 series from SOTA and a 680 pF capacitor from the ATC100B series. Finally, as a protection component the LED diode model RL50 from Infineon Technologies[7] is used. This diode is used due to its good performance under cryogenic conditions and not due to its capability to produce light.

5.2.6. Final design and simulation

The electrical scheme is shown in Fig. 5.10 and the layout is presented in Fig. 5.11.

[6] State of the Art, Inc., 16803-1797, State College, PA, USA.

[7] Infineon Technologies AG, 95035, Milpitas, CA, USA.

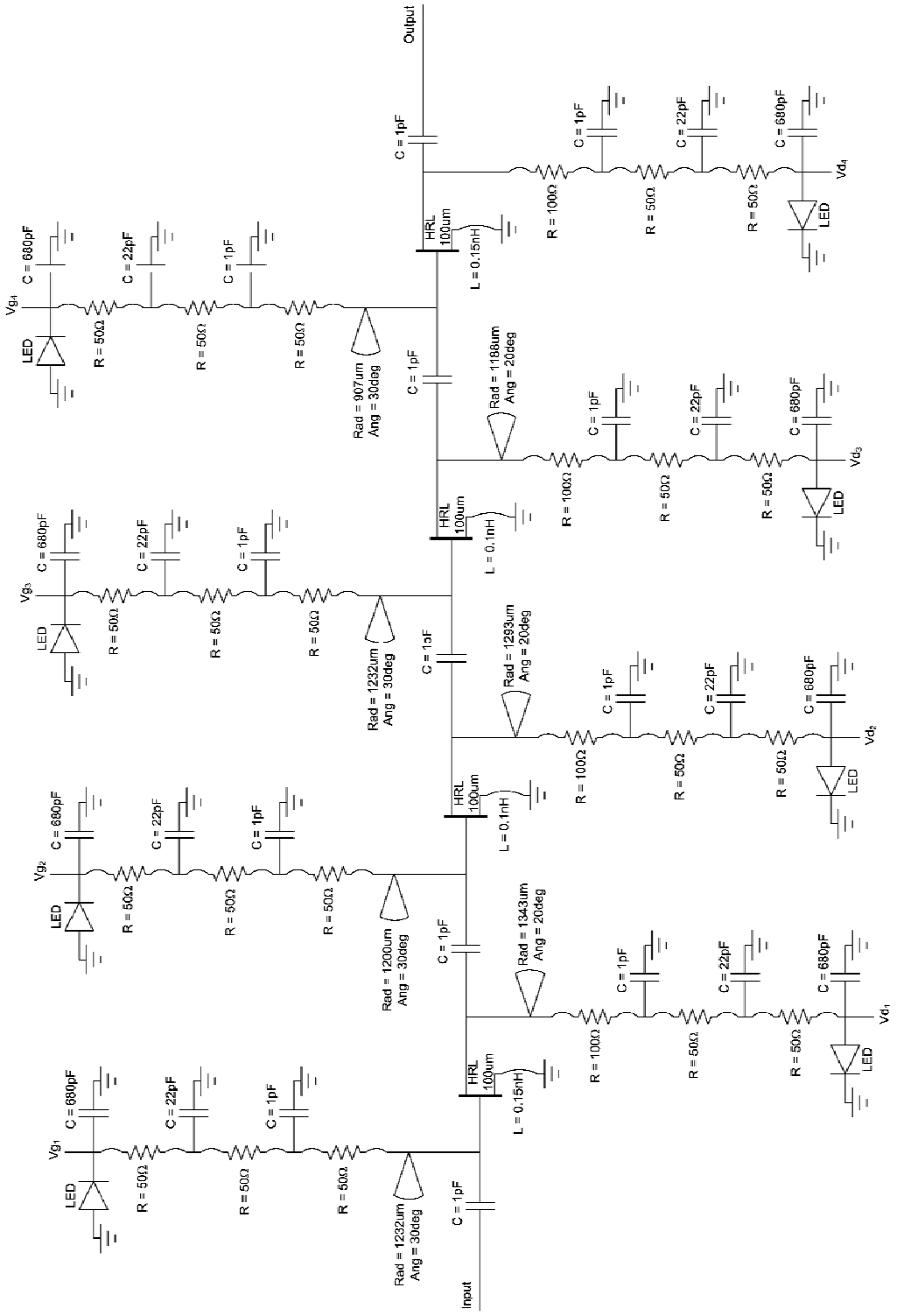


Fig. 5.10. Electrical scheme of the designed amplifier.

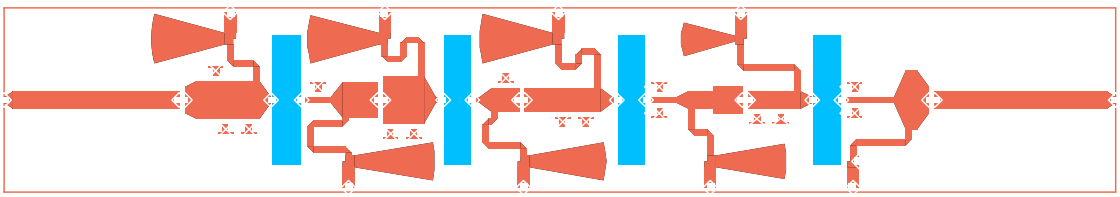


Fig. 5.11. Circuit layout. Dimensions are 18.9x3.15 mm^2.

As can be seen in Fig. 5.11 the circuit is completely fabricated on the same substrate piece. Four *islands* (indicated in blue) are included ready to be cut in order to assembly the transistors over suitable pedestals mechanized in the module. These islands have dimensions of 2.2x0.45 mm^2. Moreover, tiny conductive islands are place close to the microstrip lines. These islands, with dimensions of 0.1x0.25 mm^2, enable performance tuning if necessary just connecting them with the microstrip lines with bonding wires. On the other hand, input and output lines present a narrowing at their ends where the connectors are soldered to. This narrowing, from 0.3 mm to 0.1 mm in 0.15 mm length, improves the electrical performance of the coaxial-microstrip transition.

In Fig. 5.12 the simulation results of the amplifier at T = 12.5 K are presented.

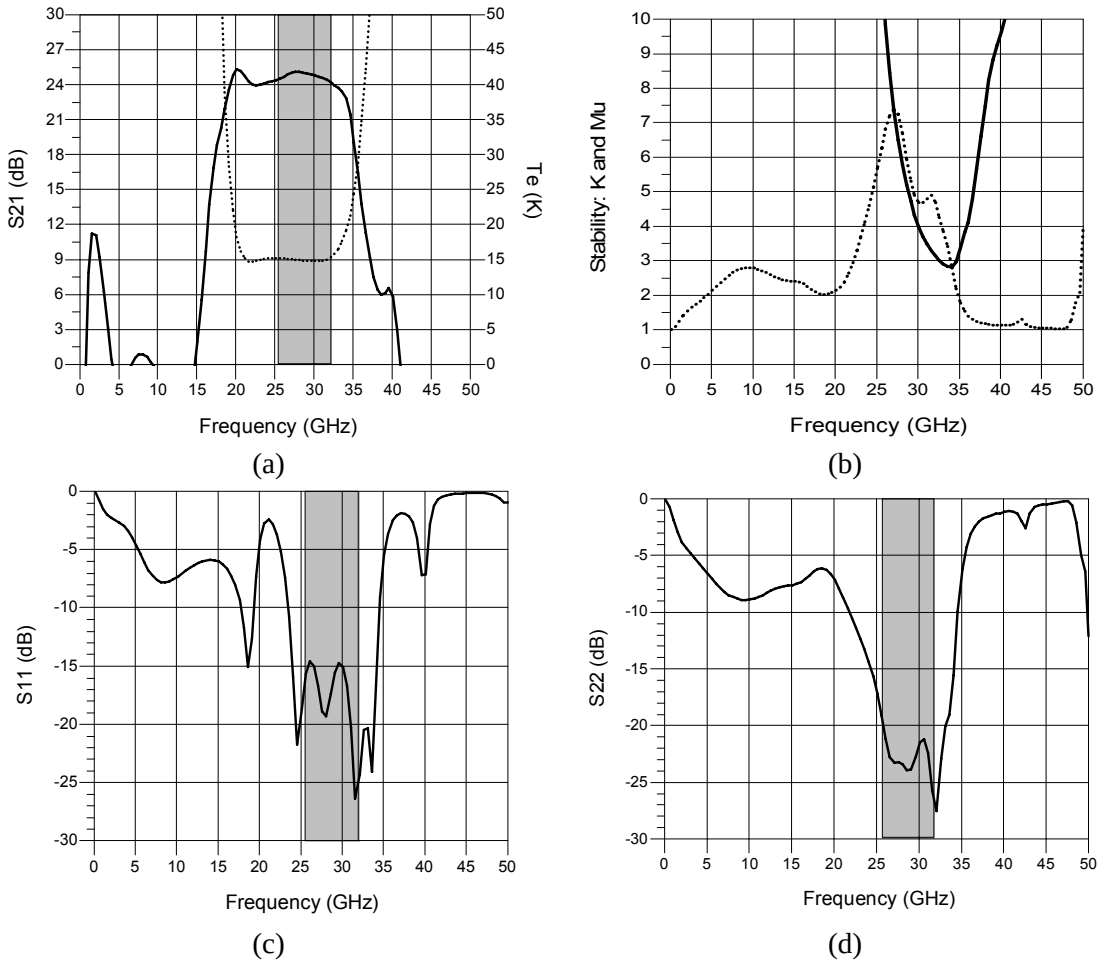


Fig. 5.12. Simulation results of the designed amplifier at T = 12.5 K; (a) Gain (solid) and noise temperature (dots); (b) Stability factors, K (solid) and μ (dots); (c) Input matching; (d) Output matching. The designing bandwidth is plotted in grey.

5.2.7. Design of a coaxial-waveguide transition

Although the amplifier is designed to be used with coaxial connectors (K or 2.92 mm type) the possibility of waveguide ports has been foreseen and therefore a WR28-coaxial transition has been designed. This transition must reuse the existing glass-bead in order to be able to take measurements both in coaxial and waveguide. The transition design has been carried out in HFSS[8].

The WR28 to coaxial transition can be easily made adding a metallic cylinder, just like a *hat*, to the glass bead central conductor entering the waveguide as shown in Fig. 5.13. The transition performance can be optimized varying a few parameters: the cylinder diameter, *D*, the cylinder length, *L*, the gap between the cylinder and the glass bead, *d*, and the distance from the center conductor to the waveguide short-circuit, *H*. The dielectric of the glass-bead is made of Corning 7070 (ε_r = 4, tanδ = 0.0012).

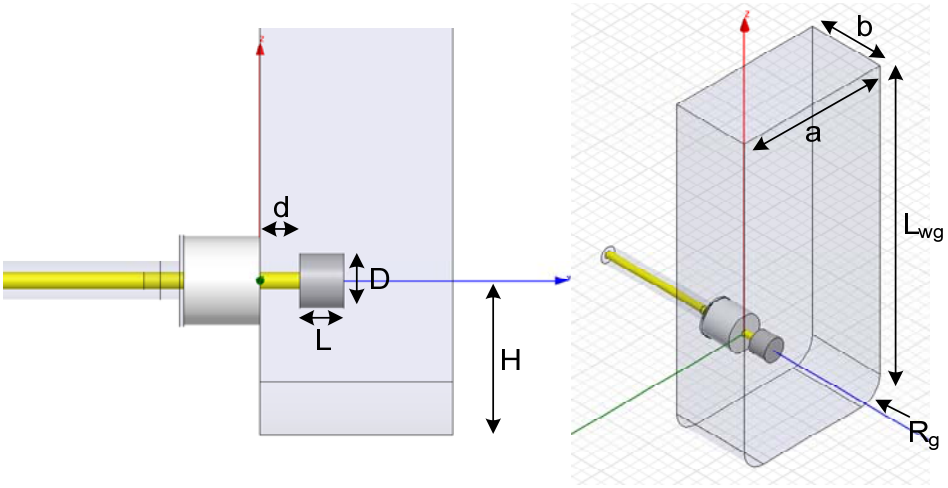


Fig. 5.13. WR28-coaxial transition designed for the amplifier.

The values for the design parameters in the presented transition can be found in Table 5.2.

Parameter	Description	Value
H	Cylinder to short-circuit distance	2.85 mm
D	Cylinder diameter	1 mm
L	Cylinder length	0.81 mm
d	Glass-bead to cylinder gap	0.74 mm
a	WR28 waveguide dimension	7.11 mm
b	WR28 waveguide dimension	3.56 mm
L_{wg}	Waveguide length	15 mm
R_g	Milling tool radius	1 mm

Table 5.2. Parameters of the WR28-coaxial transition

[8] Ansoft, LLC, 15219, Pittsburgh, PA, USA.

Simulation results of this transition are plotted in Fig. 5.14.

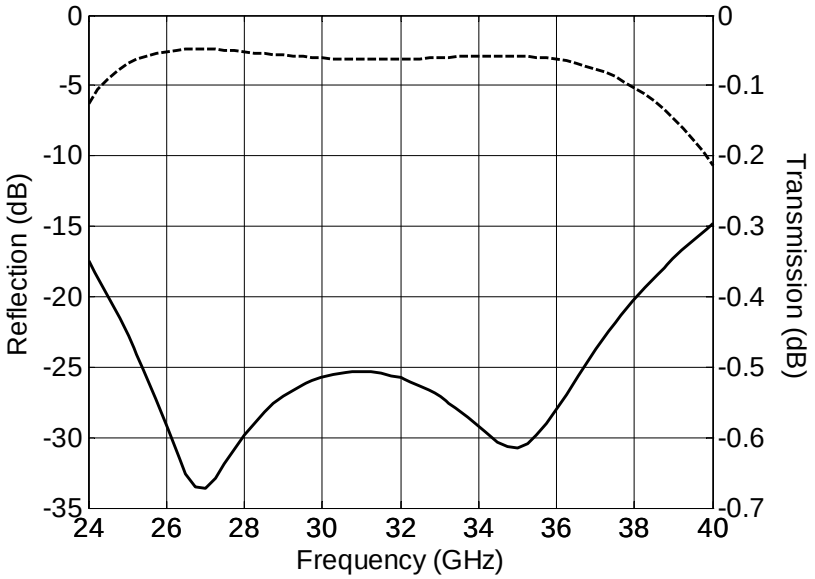


Fig. 5.14. Simulation results of the designed transition: input matching (solid) and transmission (dashed).

The designed transition shows an input matching better than 25 dB in the frequency band of interest with return losses of 0.05 dB. The transition performance is greatly affected by parameter *d* in Fig. 5.13 therefore this parameter should be adjusted in a back-to-back measurement. The expected result from this measurement with a 19 mm long microstrip line connecting both transitions is shown in Fig. 5.15.

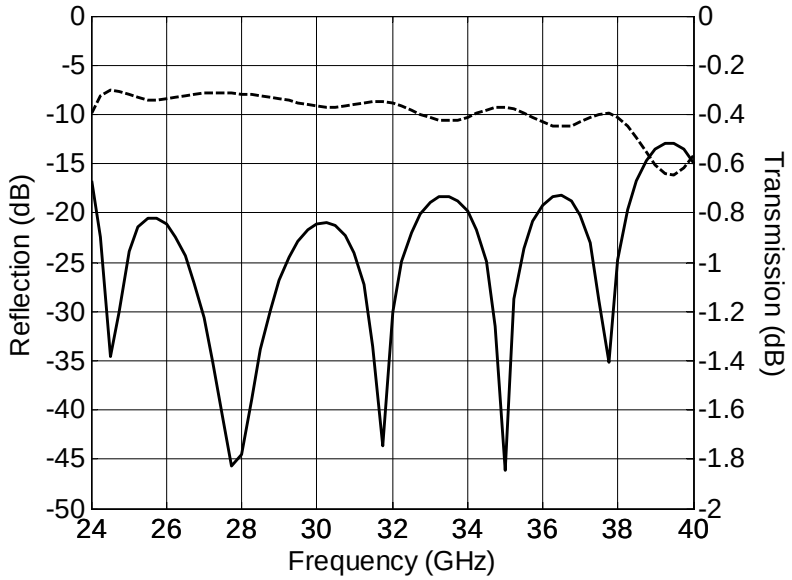


Fig. 5.15. Simulation results of the designed transition in a back-to-back configuration with a 19 mm long microstrip line connecting both transitions. Input matching is shown in solid line while insertion loss is presented in dashed line.

5.3. Amplifier Mechanical Design

The mechanical design is one of the most important steps in the whole amplifier design since both mechanical and electrical aspects need to be considered. The amplifier module is split into two blocks: the body and the cover, which are machined in brass to make the mechanization and gold plating easier. In Fig. 5.16 an artist view of the final module is shown. The mechanical design has been carried out with Autodesk Inventor[9] and its different drawings are included in Annex III.

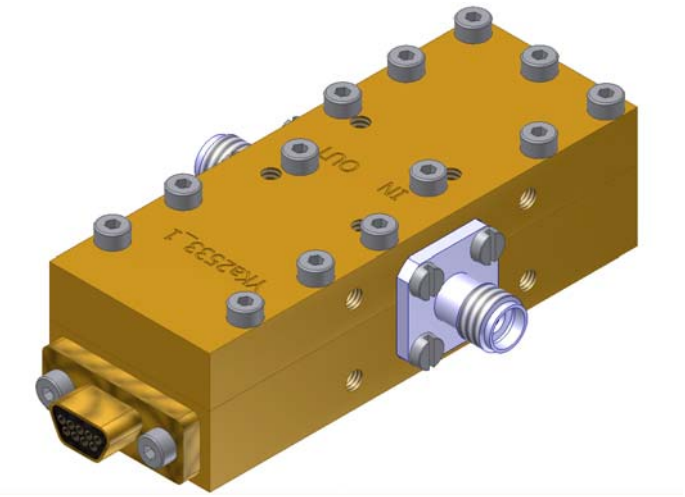


Fig. 5.16. Artist view of the designed amplifier. Dimensions are 60.6x22.7x17.1 mm^3 excluding connectors.

5.3.1. Module design

The module body is divided into three cavities: two of them for the bias circuitry of gates and drains and the center cavity dedicated to the high frequency elements.

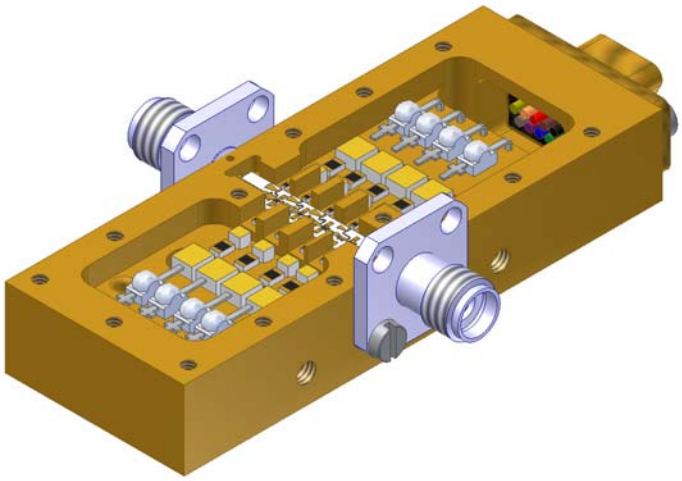


Fig. 5.17. Artist view of the designed amplifier with the cover removed. The three cavities are clearly shown with all the circuit elements mounted.

[9] Autodesk, Inc., 94903, San Rafael, CA, USA.

The body is designed with a 1.5 mm wide and 1.5 mm deep groove machined in the back side to connect both bias cavities in order to enable the distribution of bias cables in the amplifier.

There are four islands mechanized along the central cavity for the transistors assembly. These islands are 2x0.4 mm^2 with 80 μm of height where the devices are soldered and 170 μm of height where the source bonding wires are bonded. Thus, both transistors and wires are at the same height as shown in Fig. 5.5. On the other hand the width of the cavity is kept as minimum in order to avoid the propagation of high order modes in the cavity. In this case the cavity width is 3.2 mm and thus the cut-off frequency of the first mode in the cavity is 46.9 GHz which is well above of the design bandwidth. Due to the dimensions of the islands and the cavity it is needed to use a 0.6 mm diameter bit between the islands and the cavity walls (for the rest of the cavity a 1 mm diameter milling tool is used). The use of such a small bit together with visibility limitations of the bonding machine imposes a constraint in the maximum cavity depth to 1.8 mm. Finally, this limitation has some implications in the selection of the coaxial connectors; connectors with two assembly holes can not be used due to the difficulty to accommodate properly these two holes with good electrical contact, therefore connectors with four holes have been chosen.

A critical dimension in the mechanical design is the height of the central conductor of the coaxial connector from the cavity floor. This dimension determines the performance of the coaxial-microstrip transition. In this case this dimension is set to 0.35 mm which permits enough space to accommodate the substrate including a 20 μm gap for security.

In the lateral sides of the module, as well as the holes for the connectors, holes for mounting the pieces of the waveguide-coaxial transitions are drilled. Likewise, in the cover and body back-side there are suitable holes drilled, which are compatible with the WR28 flange, in order to make waveguide measurements. The waveguide-coaxial transition pieces are designed in such a way that they can be rotated 180 degrees to facilitate the measurement process in different setups.

Finally, the different discrete components are glued to the circuit using electrically conductive silver epoxy H20E[10] and they are bonded with 17 μm diameter gold wire.

[10] Epoxy Technology, Inc., 01821-3972, Billerica, MA, USA.

5.3.2. Gold-plating

The gold-plating of the brass pieces is made with soft gold and its thickness depends on the need of making bonding on the surface. For the cover a gold layer with 4 μm of thickness is enough however, in the body, a thickness of 8 μm is advisable for proper bonding. A later analysis of the gold-plated module with spectroscopic techniques revealed an actual thickness of 4.5 μm for the cover and 8.5 μm for the body.

5.3.3. Connectors

For the coaxial connectors model SK-50-0-51 from Huber+Suhner[11] has been used which are suitable up to 40 GHz. About the DC biasing, it is a 9 pin connector from the MDM series from ITT Cannon[12]. The pin-out of this connector is shown in Fig. 5.18 and Table 5.4. The internal wiring of the amplifier is made using WQL-32 cable from LakeShore which is indicated for cryogenic applications.

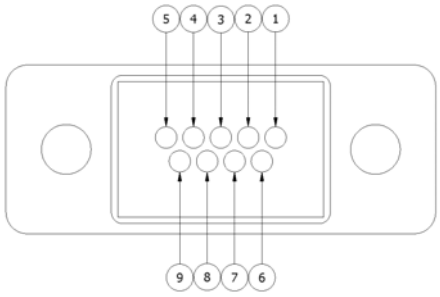


Fig. 5.18. Pin-out of the DC connector. View from the cables side.

Pin	Bias
1	GND
2	Vd1
3	Vg1
4	Vd2
5	Vg2
6	Vd3
7	Vg3
8	Vd4
9	Vg4

Table 5.4. Correspondence between pins and bias signals.

[11] Huber+Suhner AG, 9100, Herisau, Switzerland.

[12] ITT Corporation, 10604, White Plains, NY, USA.

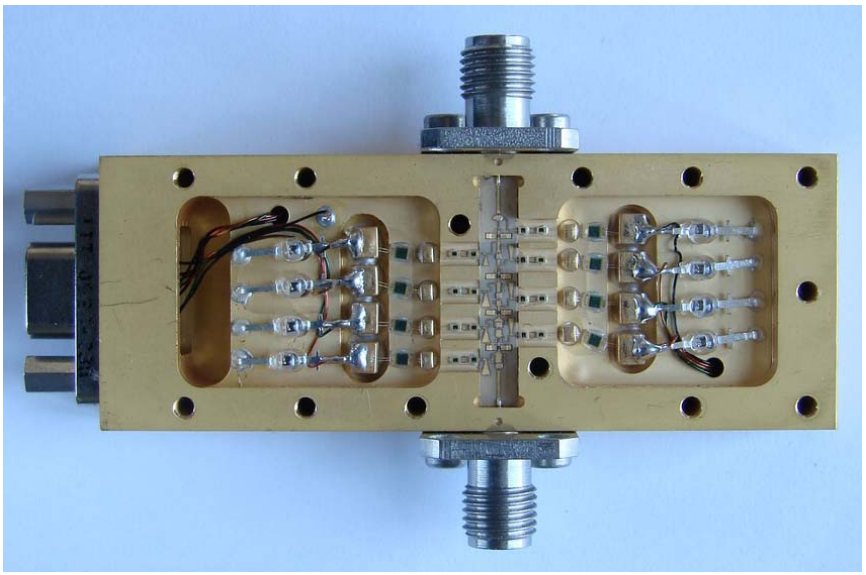


Fig. 5.19. Picture of the finished amplifier.

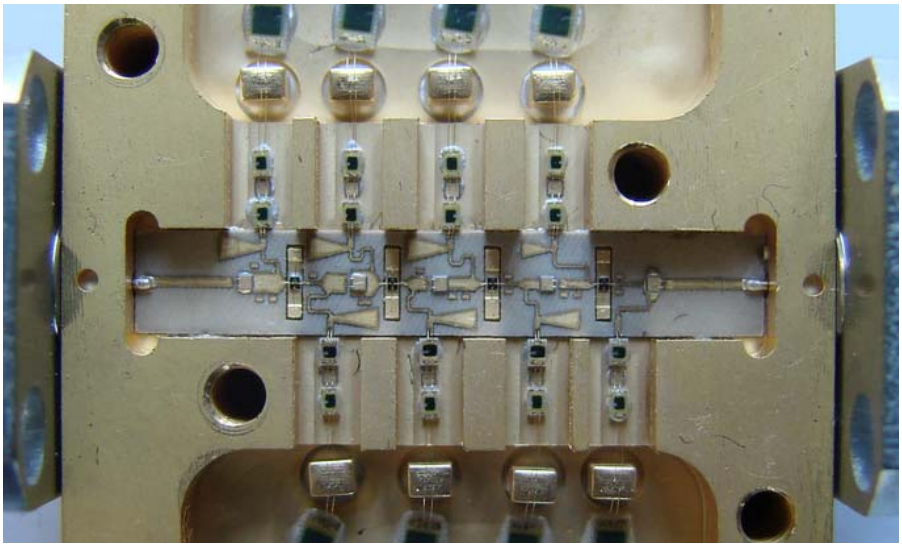


Fig. 5.20. Detailed view of the high frequency cavity.

5.4. Amplifier Characterization

The amplifier characterization has been carried out both at room and cryogenic temperatures. The S-parameter measurement is made using the 8510C network analyzer from Hewlett-Packard whereas for the noise measurement the noise figure meter 8970B from Hewlett-Packard is used. Due to the measurement frequencies it is necessary to use a downconversion stage at the input of the noise figure meter. This downconversion stage is included in the receiver block during the calibration and measurement processes as shown in Fig. 5.21.

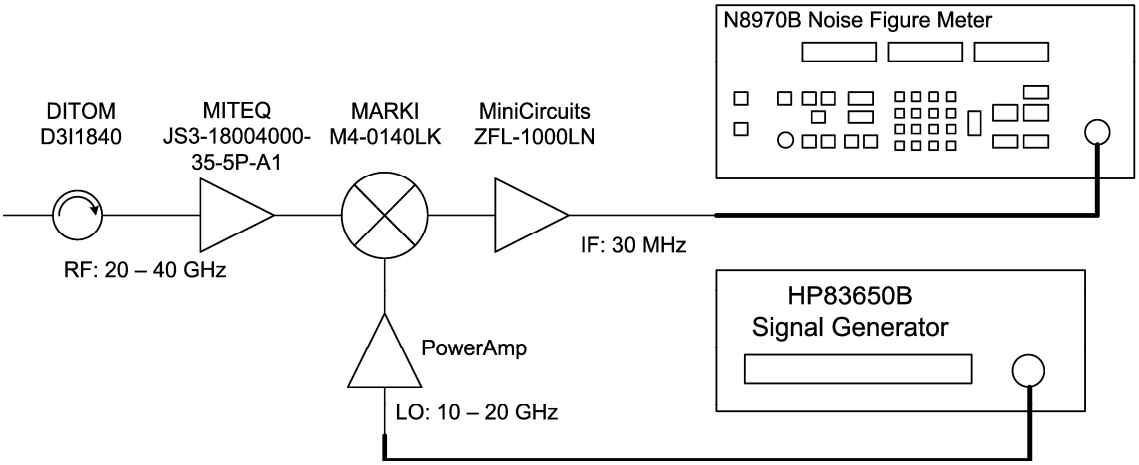
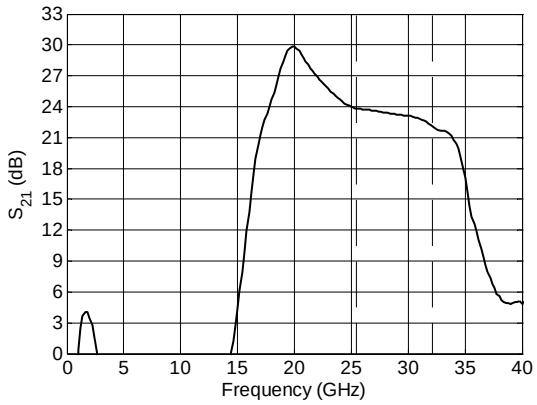


Fig. 5.21. Receiver block diagram for noise measurements both at room and cryogenic temperatures.

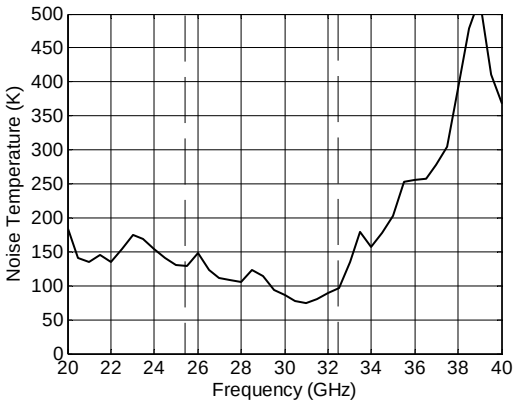
The isolator at the receiver input provides a good return loss over the whole frequency range while its insertion losses should be low in order to reduce its contribution to the total receiver noise. The RF LNA reduces the contribution of the subsequent elements in the receiver to the total noise keeping it between adequate limits. The power amplifier provides adequate power levels to drive the mixer.

5.4.1. Room temperature characterization

At room temperature the measurement results are presented in Fig. 5.22. Noise measurement is taken with noise source NC346KA[13] and a 10 dB attenuator model 4768-10 from Narda[14] at its input. As commented in Chapter III, the use of an attenuator at the noise source input reduces the measurement uncertainty.



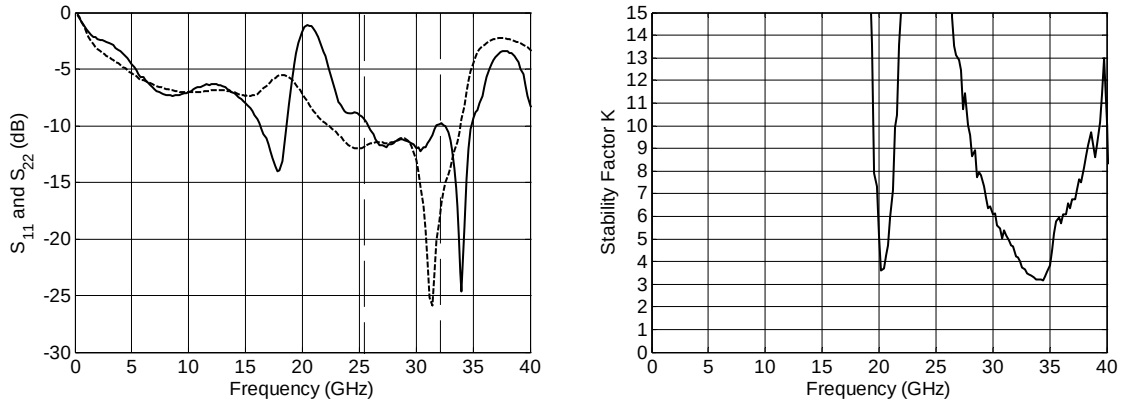
(a)



(b)

[13] NoiseCom, 07054-3702, Persippany, NJ, USA.

[14] Narda Microwave-East, 11788, Hauppauge, NY, USA.



(c) (d)

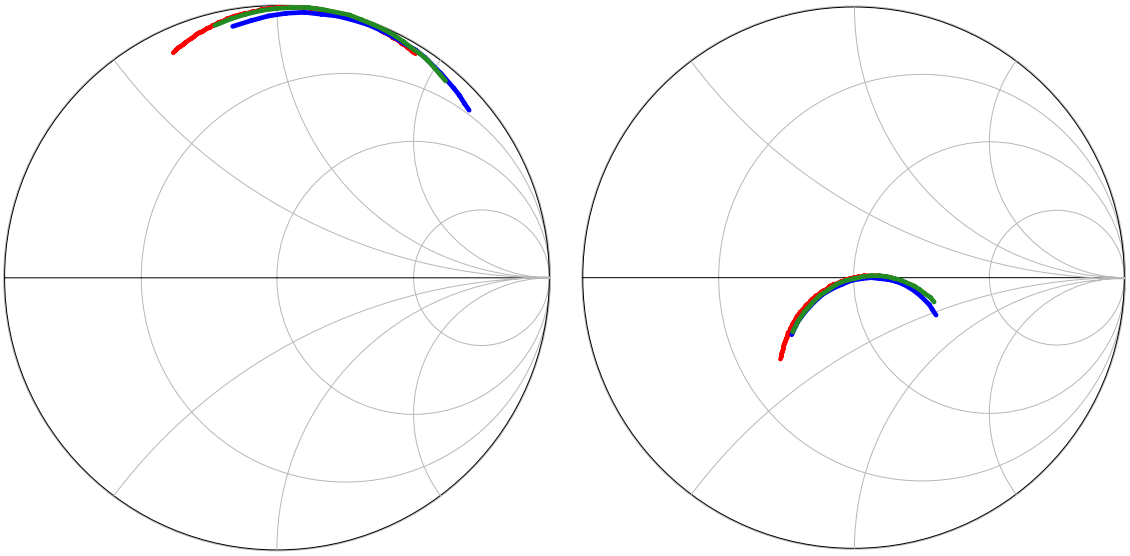
Fig. 5.22. Measurement results of the designed amplifier at room temperature. Bias settings for each stage are V_d = 1.5 V and I_d = 4 mA; (a) gain; (b) noise temperature, the mean value in the bandwidth is 104 K; (c) input matching (solid) and output matching (dashed); (d) stability factor K. Design bandwidth is marked with dashed vertical lines.

To achieve the results showed in Fig. 5.22 some modifications were made to the initial assembly. Mainly, it was detected that the bonding wire model had not worked properly and the inductance needed to be reduced in all stages. To obtain the presented results all the bondings in the transistor sources of all stages were duplicated except in one source of stage two.

Although these results are good for a first prototype some differences from the simulated results can be observed: there is an excess of gain at 20 GHz which coincides with a noticeable reduction in the stability and ports matching should be better.

The improvement of the amplifier performance has been investigated through simulations and it has been determined that, in order to reduce the peak of gain at 20 GHz without modifying other parameters, the radial stubs need to be changed.

Electromagnetic simulations demonstrate that the radial stub model used for the simulation and optimization in ADS underestimates the actual capacitive effect of this stub. The comparison between results of one radial stub simulated with three different tools shows that the radius of the schematic model needs to be increased to obtain similar results than those obtained with the electromagnetic tools. In Fig. 5.23 the results from these simulations are presented: the schematic model is plotted with red line, the radial stub simulated with a 2.5D electromagnetic tool such as Momentum from ADS is shown with blue line, and the same structure simulated with a 3D electromagnetic tool such as HFSS is depicted with green line.

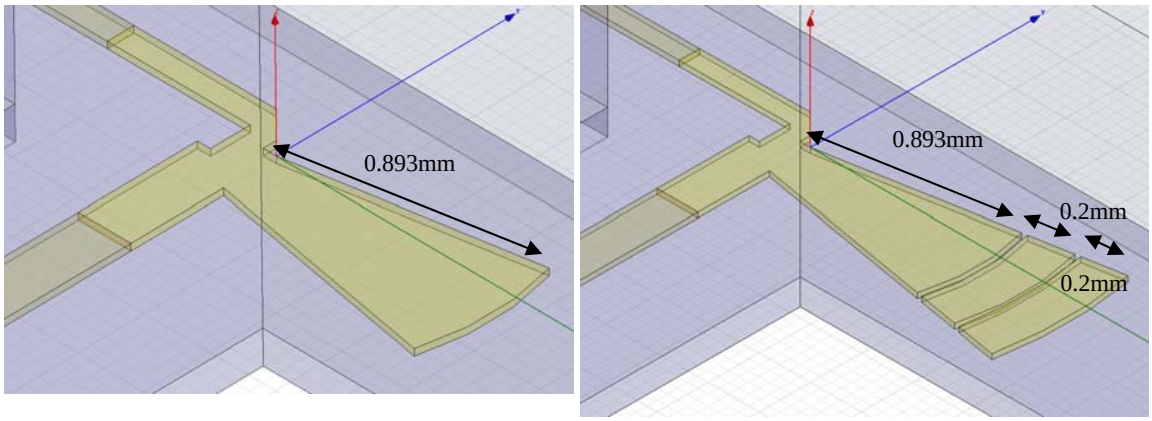


(a) (b)

Fig. 5.23. Simulation of the radial stub in ADS schematic (red), ADS momentum (blue), and HFSS (green); (a) S_{11} and (b) S_{21}. Adding some length to the schematic model, in this case 100 – 150 μm, the red curve approaches the other curves.

From the previous simulation it is clear that the radial stubs implemented in the actual circuit have more capacitance than the needed values extracted from the initial simulation and optimization. Therefore the radius of the stubs in the amplifier has to be reduced in order to adjust the amplifier performance to the simulated response.

To reduce the stub radius two strategies have been considered: to cut the stub to the desired length or to make some concentric cuts in the stub so some islands are left to be used in case that this modification is desired to be withdrawn. These two alternatives have been simulated in HFSS, starting with a stub with a 1343 μm radius this length is reduced to 893 μm using the two strategies. The Fig. 5.24 shows both implementations in the simulation tool and their simulation results. The gap produced by the cutting machine is 25 μm.



(a) (b)

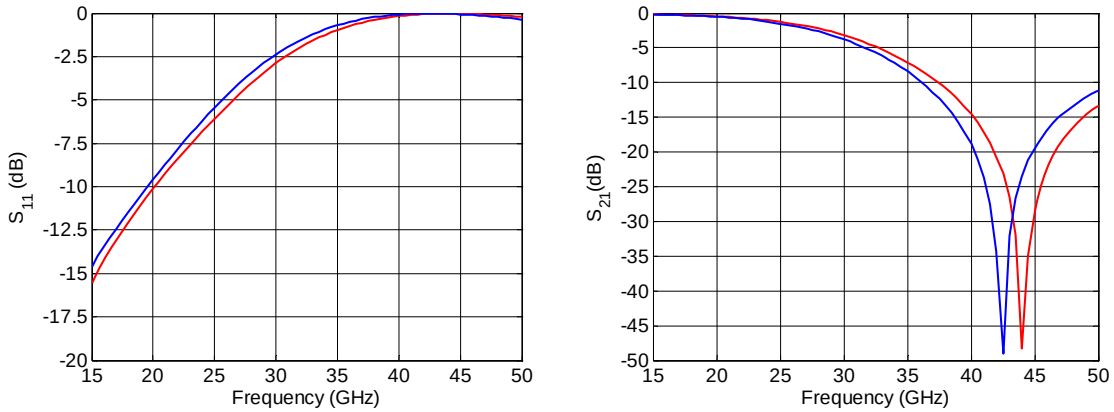


Fig. 5.24. Simulation of the two strategies to reduce the radius of one radial stub from 1343 μm to 893 μm; (a) direct cut (solution A); (b) cut with islands (solution B); (c) S_{11} from solution A (red) and solution B (blue); (d) S_{21} from solution A (red) and solution B (blue).

From Fig. 5.24d the resonant frequency for both solutions is different. In the solution B there is some coupling between the conductive patches and therefore the total capacitance of the structure is greater than in solution A, thus lowering the resonant frequency. Despite of this, the solution B is advised in this thesis if the amplifier performance wants to be improved since this solution can be turned back just adding conductive epoxy or wire bondings. In the case of the amplifier presented in this work, it has been determined through simulation that the most effective modification would be the 200 – 300 μm reduction of the radius in the gate radial stub of the first stage. This modification has not been still implemented by the moment of ending this thesis.

5.4.2. Characterization at cryogenic temperature

The amplifier has been characterized at cryogenic temperature using the cold-attenuator technique and the existing setup at the CAY with the new chip attenuator designed in Section 3.4. The classical setup at the CAY with coaxial attenuators and the heat block is shown in Figs. 5.25 and 5.26. The noise source is the same as in the room temperature measurements without the 10 dB attenuator. Results are presented in Fig. 5.27.

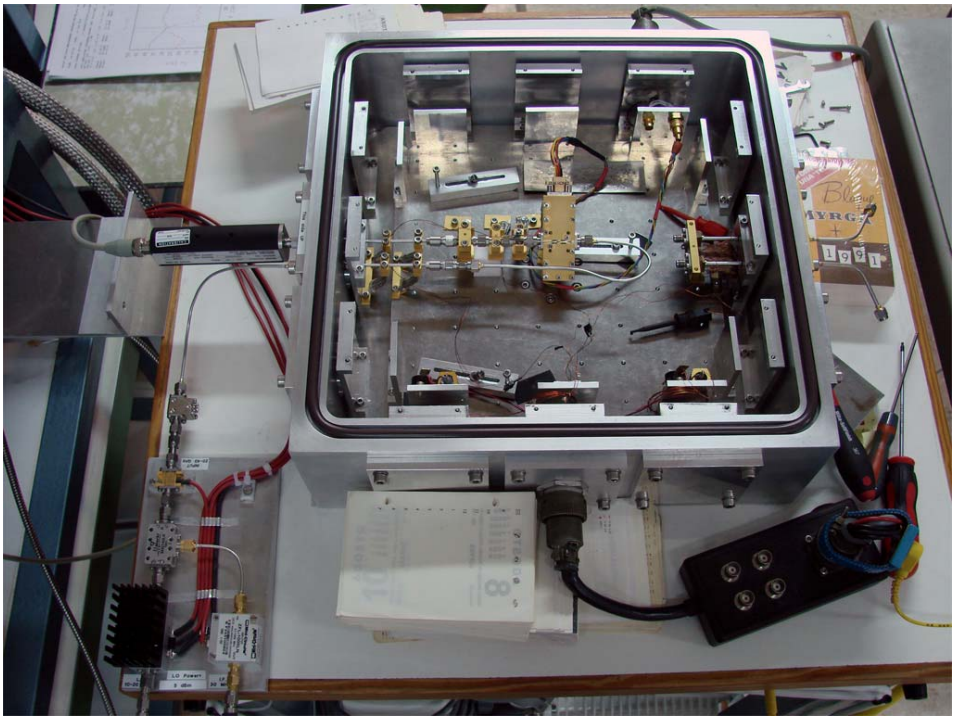


Fig. 5.25. Noise measurement setup. Noise source and downconversion stage can be seen out of the Dewar.

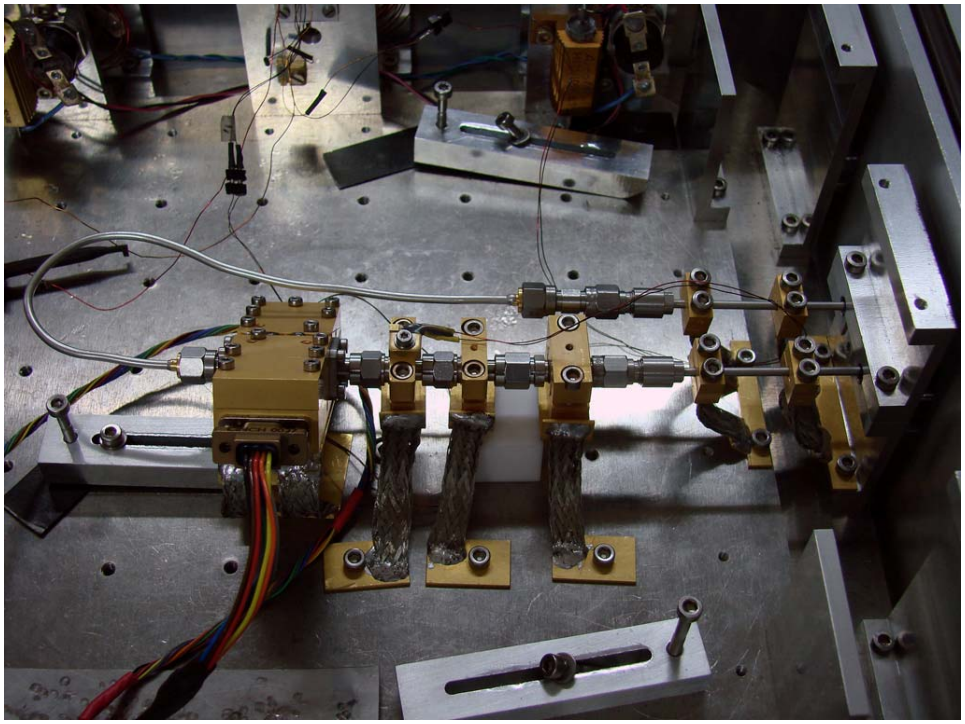


Fig. 5.26. Detailed view of the setup inside of the cryostat. The heat-block and the 10 dB + 6 dB cascaded attenuators are cooled in front of the LNA.

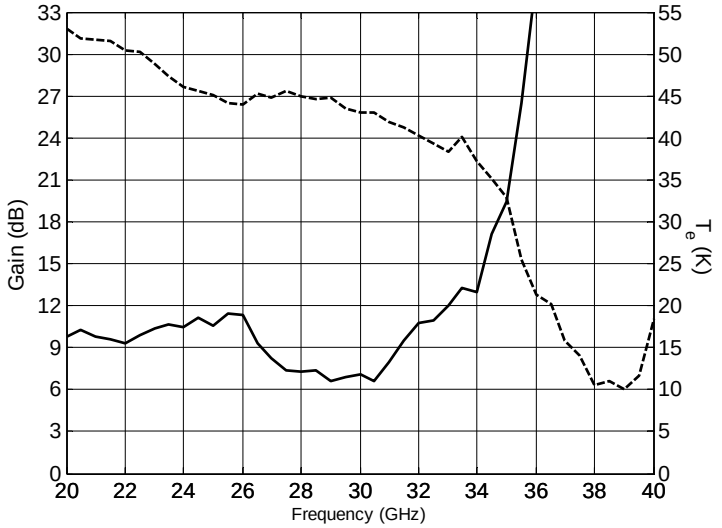


Fig. 5.27. Gain (dashed) and noise (solid) results of the designed LNA at 12.5 K. The mean value of noise in the band is 14.3 K. The bias settings are V_{d1} = 1 V, I_{d1} = 2 mA, V_{d234} = 1.5 V, I_{d234} = 4 mA.

5.5. Conclusions

This chapter has presented the design and characterization processes of one MIC LNA for operating at cryogenic temperatures in the 25 – 33 GHz band. The design is based on home-made cryogenic models of 100 nm InP transistors from HRL. These transistors enable to achieve the noise requirements but not the gain specifications.

At room temperature the amplifier shows a gain around 24 dB with a mean noise temperature of 104 K according with the measurements presented in this document. With the LNA cooled down to 12.5 K, the amplifier presents a gain around 25 dB with an associated noise temperature of 14.3 K in the band. The total DC power consumption at cryogenic temperature is only 20 mW.

Some modifications to improve the LNA performance have been presented and analyzed, although they could not be carried out by the end of this document. However, the results obtained with this prototype are considered to be a good starting point to get a reliable LNA fulfilling the given specifications, while they show a good performance comparable with the best designs found in the literature and presented in Table 5.5.

Reference	Technology	Foundry	Bandwidth (GHz)	Gain (dB)	T_e (K)	DC consumption (mW)
This work	100 nm InP HEMT	HRL	25.5 – 32.5	25.5±1.5	14.3	20
[5.4]	100 nm InP HEMT	TRW	31 – 33	31.5±1.5	20 – 25	2.1 (first stage)
[5.5]	100 nm InP HEMT	HRL	40 – 50	32±4	15	-
[5.6]	100 nm InP HEMT	TRW	30 – 34	30±5	11	8.4
[5.7]	100 nm InP HEMT	HRL	28 – 37	33±1.5	<40@80K	< 33 @ 80K

Table 5.5. Comparison between the results obtained with the designed LNA and other works about cryogenic MIC LNAs found in the literature.