

UNIVERSIDAD DE CANTABRIA

Departamento de Ingeniería de Comunicaciones



TESIS DOCTORAL

Cryogenic Technology in the Microwave Engineering:
Application to MIC and MMIC Very Low Noise
Amplifier Design

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Chapter VI

Design of Cryogenic MMIC Low Noise Amplifiers

Monolithic microwave integrated circuits (MMIC) are circuits in which all the components (passive and active) and interconnections are fabricated at the same time on the same semiconductor substrate. These chips are small in size, usually less than 10 mm², and they work in the microwave frequency range and beyond.

As stated in the introduction of Chapter V, MICs offer the best noise and additionally they can be used even in the W-band [4.29] but generally they are very difficult to assemble and MMICs are usually the preferred solution for frequencies above 30 GHz. MMICs simplify the module mechanical design and reduce the assembly labor, furthermore they are cheaper than MICs for large quantities making complex arrays feasible. Among the advantages of MMICs it can also be added that they are more repeatable and smaller than MICs, and they can achieve wider bandwidths due to their lower parasitic reactances.

This chapter deals with the design and measurement at room and cryogenic temperatures of a MMIC low noise amplifier in Ka band. The MMIC is designed using D01MH process (130 nm gate length mHEMT process) from OMMIC foundry. Although this amplifier is not based in given specifications from any project it is designed to cover the same frequency range as the QUIJOTE project high frequency channel and thus to be an option for the final project assembly.

D01MH mHEMT, 4x15 μm , $T = 15 \text{ K}$, $V_{ds} = 0.9 \text{ V}$, $I_{ds} = 3.7 \text{ mA}$																	
L_g	R_g	C_{pg}	L_d	R_d	C_{pd}	L_s	R_s	C_{gs}	R_i	C_{gd}	R_j	C_{ds}	R_{ds}	g_m	τ	T_d	T_g
(pH)	(Ω)	(fF)	(pH)	(Ω)	(fF)	(pH)	(Ω)	(fF)	(Ω)	(fF)	(Ω)	(fF)	(Ω)	(mS)	(psec)	(K)	(K)
15	0.5	7	14	5.3	3.6	5.5	2.11	49.9	3	11.4	10	16	365	50	0	1250	15

Table 6.1. Parameters of the small signal and noise model at cryogenic temperature.

The most significant parameters of the transistor model are simulated and plotted in Fig. 6.2.

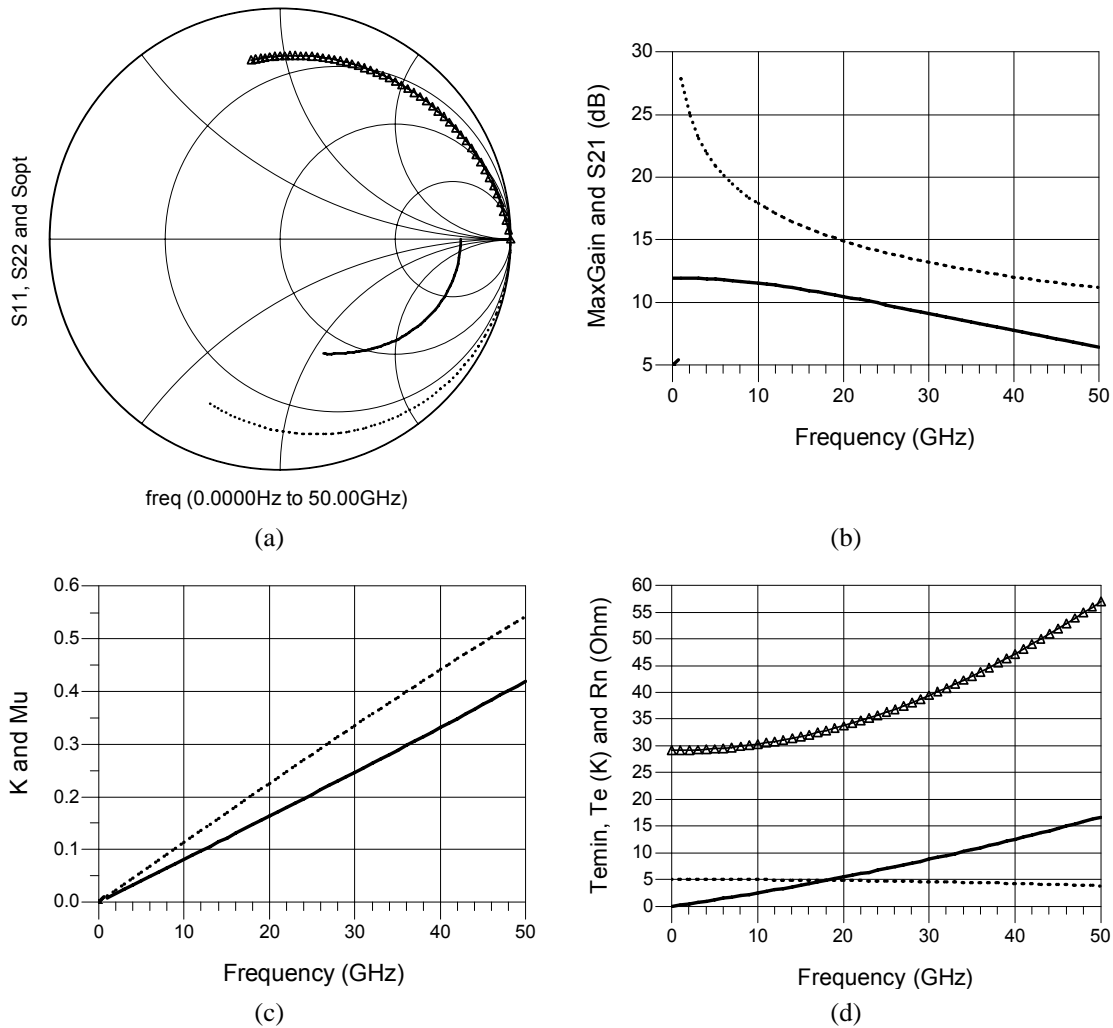


Fig. 6.2. Small signal and noise properties of the OMMIC transistor model at $T = 15 \text{ K}$ in the 0.1 to 50 GHz frequency range; (a) S_{11} (dots), S_{22} (solid) and Γ_{opt} (triangles); (b) S_{21} (solid) and maximum gain (dots); (c) Stability factors K (solid) and μ (dots); (d) Effective input noise temperature (triangles), minimum effective input noise temperature (solid), and the noise resistance (dots) which indicates the sensitivity of the noise match.

6.1.2. Chip design and layout

The amplifier is designed with four stages to achieve around 30 dB of gain. The first two stages are optimized for low noise whereas the other two provide gain level and flatness. The low noise optimization is carried out through the inductive source feedback in the same way as in Section 5.2.3. In this case the inductance is accomplished using microstrip lines connected to the transistor source terminals. Since

the required inductance value is high then only one source is connected to ground through this inductance. In the last two stages the inductance is low and therefore the two transistor sources are connected to ground, thus the inductance is half.

Matching networks are mainly made up of capacitors and microstrip transmission lines which replace inductors due to the high frequency. Resistors are included in the matching networks (not in the first stage to avoid the increase of noise) to provide gain equalization and to improve the amplifier stability. The output network includes a low value resistor in series to achieve a wideband output matching without losing too much gain. Matching networks are implemented using curves instead of bends in order to improve their frequency behaviour.

The in-band filtering networks are included inside the chip; big capacitors of 3.5 pF filter the RF signal to ground and avoid this signal to propagate to the bias networks. The out-of-band filtering networks are placed in the bias networks outside of the chip. Finally, in order to enable individual tuning of each stage, each bias signal is routed separately up to the DC pads. Due to the limitation of eight DC pads, because of the available DC probes, then the drain voltages of the last two stages are biased together. However, all the gate and drain lines inside the chip are designed to have 150 Ω and 36.5 Ω of series resistance respectively, and all the gates pads and drain pads are placed together; hence the chip can be easily biased with only two bias supplies if it is desired: one for all the gates and one for all the drains. The schematic of the complete LNA is presented in Fig. 6.3

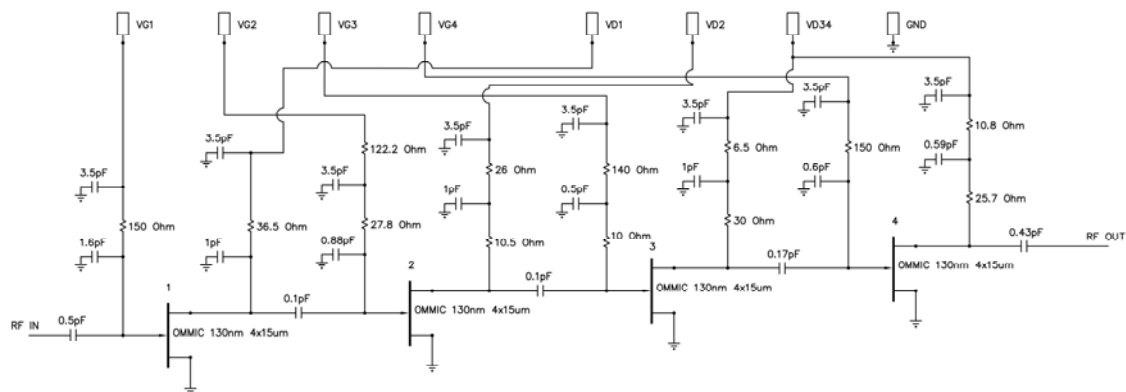


Fig. 6.3. Schematic of the designed MMIC LNA in the Ka band.

Simulation results of the schematic design in ADS are presented in Fig. 6.5 together with layout electromagnetic simulations. For the layout simulation, since the transistors can not be simulated electromagnetically, each layout subnetwork is simulated and optimized separately in ADS Momentum and then all these results are included as individual S-parameters boxes in the ADS schematic simulation replacing

the original subnetworks. The substrate is introduced in the electromagnetic simulator through adequate layers definition following the data provided in Table 6.2.

Type	Name	Boundary	Thickness (μm)	ϵ_r	$\tan \delta$	Conduct. (S/m)
	Free Space	Open				
Substrate	Sin_0		0.15	6.8	0	
Sheet Cond.	IN, TIN		2			$2.3 \cdot 10^7$
Substrate	SiO/Via CO		0.85	5	0	
Sheet Cond.	TE		0.56			$7.4 \cdot 10^6$
Substrate	Sin/Via CG		0.15	6.8	0	
Sheet Cond.	BE		0.65			$2.3 \cdot 10^7$
Substrate	GaAs/Via VH		100	12.9	0.006	
	GND	Closed				Perfect

Table 6.2. Substrate layers definition for ADS Momentum.

The D01MH process enables the use of two metallization layers (IN and TIN) to double the conductor thickness and thus to increase its power handling capability. This feature is included in the present design to reduce the resistive loss in the transmission lines and hence to reduce their contribution to noise. The amplifier is completed with coplanar RF ports designed for 125 μm pitch probes. Finally, a 4x15 μm sample transistor is added in the remaining chip space in order to characterize the wafer run performance in comparison with the data provided by the manufacturer and/or the data available from previous runs. The layout of the designed LNA is shown in Fig. 6.4.

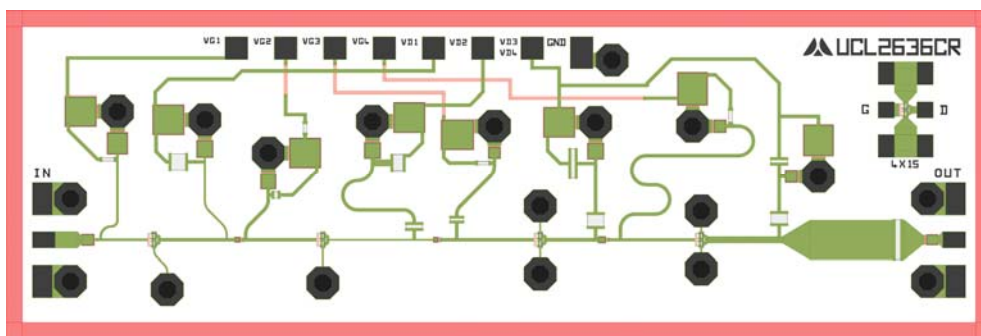


Fig. 6.4. Layout of the MMIC LNA in the Ka band. Dimensions are 3x1 mm².

The electromagnetic and schematic simulation results are compared in Fig. 6.5. This comparison is made at cryogenic temperature, $T = 15$ K, using the same transistor model, given in Table 6.1, for both simulations. The simulation results from schematic and Momentum are quite similar which increases the confidence in the designed chip before sending it to the foundry for processing.

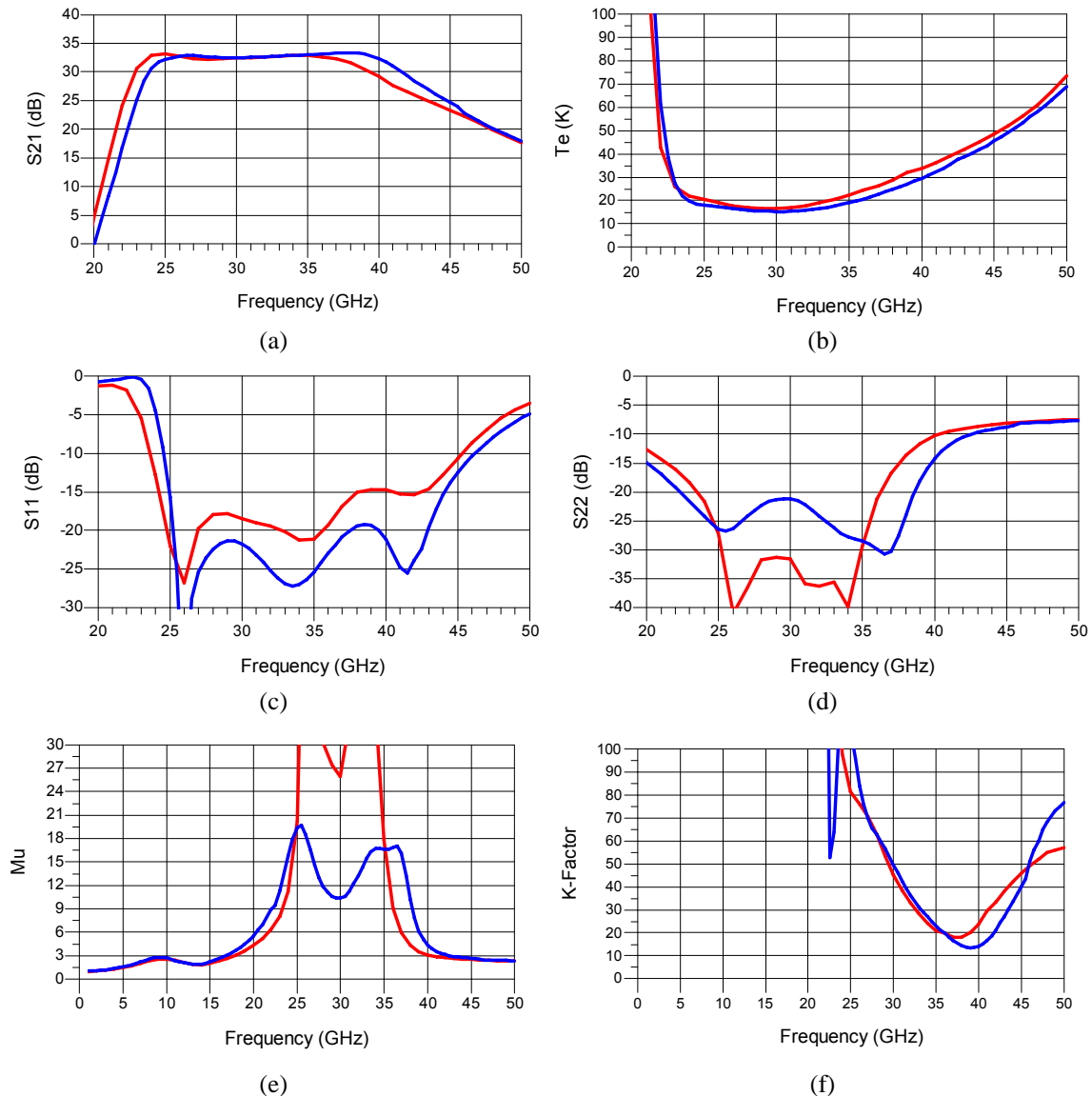


Fig. 6.5. Simulation results of the MMIC Ka-band LNA chip from schematic simulation (blue) and from electromagnetic simulation (Momentum) (red) at $T = 15$ K; (a) gain; (b) noise temperature; (c) input matching; (d) output matching; (e) stability factor μ ; (f) stability factor K .

Finally, a yield analysis of the whole chip has been performed using the technological parameters variation provided by the foundry together with the following constraints in the 26 – 36 GHz band: $S_{21} > 30$ dB, $S_{11} < -10$ dB, $S_{22} < -15$ dB, $T_e < 25$ K and K -factor > 5 (in the 1 – 50 GHz band), resulting in 94 % of yield, which indicates that this is a robust design.

6.1.3. External biasing networks

The biasing networks included within the chip are designed to provide stability and filtering functions in the nominal working frequency range of the amplifier. For frequencies below the designed band these networks need to be placed outside the chip since their dimensions would be too large to be included in the substrate. Therefore

suitable components need to be selected for biasing networks working from very low frequencies (below 1 GHz) up to the microwave range.

Although special care has been taken in order to design a very stable amplifier, even sacrificing noise performance, the amplifier can be easily turned into oscillation if the chip is not conveniently stabilized at low frequency, where its performance is not well predicted by the microwave models and the device gain is very high. For example, the available DC probes can not be used for RT measurements since they are not equipped with big capacitors at the tips and the inductive effect introduced by the needles makes the chip to oscillate. Hence, each chip has to be assembled with a simple bias network before RT characterization, which slows down the test campaign and make the characterization of the full wafer impossible. Figure 6.6 shows one chip during RT tests. The chip is assembled with 100 pF ATC118 capacitors close to the DC pads followed by a 100 nF SMD capacitor each.

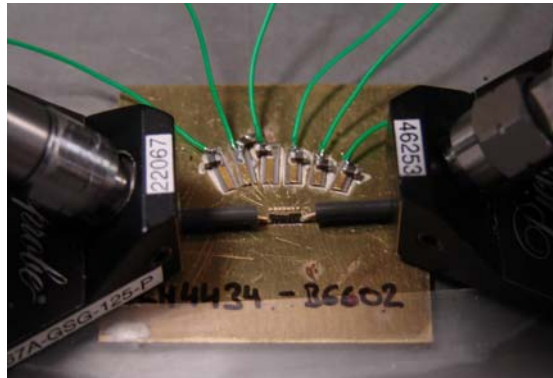


Fig. 6.6. MMIC chip during RT test campaign. External bias networks are required to avoid oscillation.

For the characterization at cryogenic temperature the chip is assembled in a module so it is measured as a complete LNA. Additional care needs to be taken in the bias networks at cryogenic temperature since the amplifier gain is increased and then the stability is reduced. First, the 100 pF transistors must be changed since the ATC118 series is not suitable for low temperatures as it was demonstrated in Chapter IV. Capacitors from Skyworks are used instead. Also series resistors are included in the bias networks to improve stability; specifically 1 K Ω resistors are placed in each gate whereas 10 Ω resistors are put in the drain lines to not increase the power consumption too much. Finally, protection diodes are placed in the gate lines since the transistors are very sensitive to voltage peaks in their gates. The configuration for the bias networks in the module assembly is presented in Fig. 6.7.

enough in the whole band affecting the measurement accuracy and bandwidth, and producing ripples in the noise results. This problem could be fixed adding an isolator before the LNA but it was not available at the moment of the measurements.

- The mixer needs high OL power to keep its conversion loss low. Since the available stage does not include an OL power amplifier then the OL generator is set to its maximum power, which it is not sufficient at some frequencies. This also affects the calibration and measurement processes.

A block diagram of the setup for noise measurement is shown in Fig. 6.8.

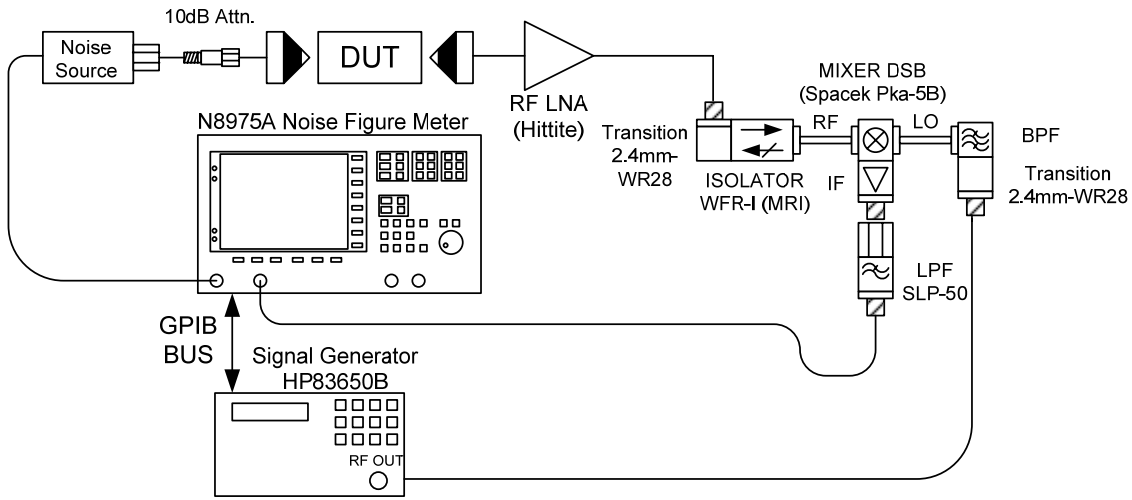


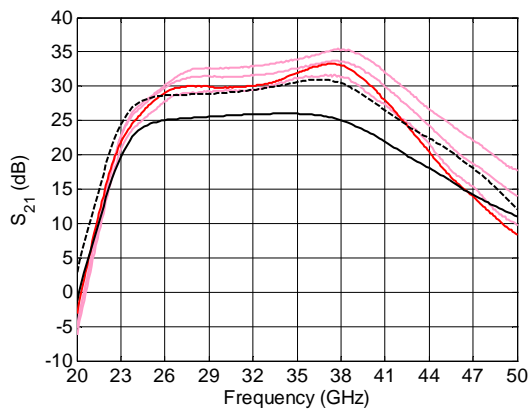
Fig. 6.8. Noise measurement setup in Ka-band at RT in the DICOM laboratory.

Some chips from different batches have been measured and their results are presented in Fig. 6.9 with soft colors. The chip with the best noise result is highlighted in each plot using a dark color. The bias point for each chip is optimized for low noise and therefore is slightly different from the others. In the case of the best noise chip the bias settings are $V_{d1} = 0.9$ V, $V_{d2} = 0.9$ V, $V_{d34} = 1.5$ V, $I_{d1} = 10$ mA, $I_{d2} = 10$ mA, and $I_{d34} = 22$ mA. These measurement results are compared with simulation results at RT. For these simulations a small signal model has been extracted from available S-parameter measurements of sample transistors provided by the foundry. The extracted model follows Fig. 6.1, its parameters are presented in Table 6.3, and the simulation results are presented with black dashed lines in Fig. 6.9.

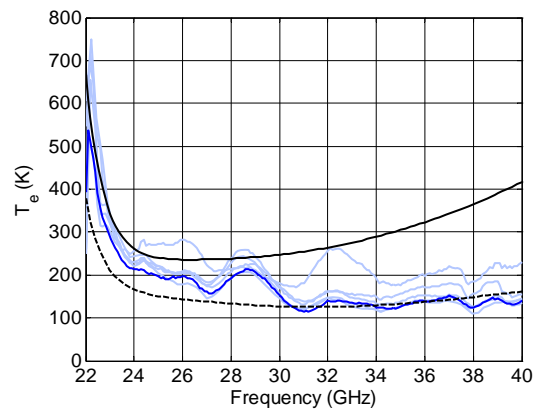
D01MH mHEMT, 4x15 μ m, $T = 300$ K, $V_{ds} = 0.9$ V, $I_{ds} = 9.5$ mA																	
L_g	R_g	C_{pg}	L_d	R_d	C_{pd}	L_s	R_s	C_{gs}	R_i	C_{gd}	R_j	C_{ds}	R_{ds}	g_m	τ	T_d	T_g
(pH)	(Ω)	(fF)	(pH)	(Ω)	(fF)	(pH)	(Ω)	(fF)	(Ω)	(fF)	(Ω)	(fF)	(Ω)	(mS)	(psec)	(K)	(K)
23	0.5	28	26.7	8.9	28	5.13	4	53.1	6.5	11.2	0	16.8	333.3	57	0	2000	300

Table 6.3. Parameters of the small signal and noise model at room temperature.

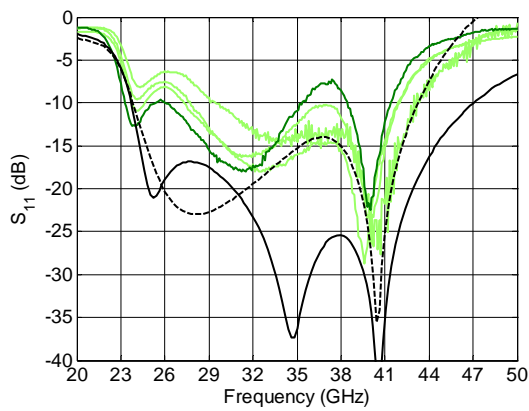
The noise model has not been extracted for the sample transistor at room temperature; hence the drain temperature value given in Table 6.3 is calculated to fit the measured result. Additionally, simulation results obtained with the transistor small signal model from the foundry library are included in the plots with black solid lines. In this last case the bias settings are $V_{ds} = 0.9$ V and $V_{gs} = -0.25$ V ($I_{ds} = 13.8$ mA). The drain current from the library model is significantly greater than the measured value for similar voltages; this may be due to threshold voltage variation between the wafer from where the model was extracted and the measured wafer.



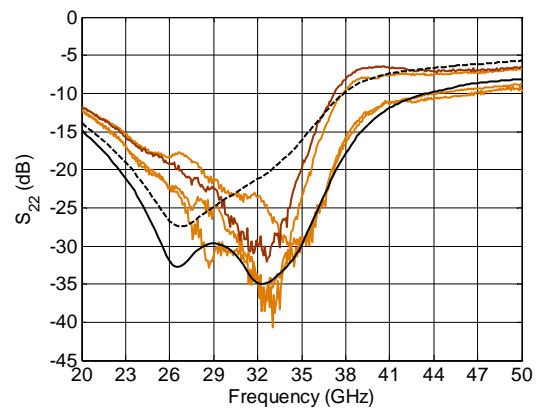
(a)



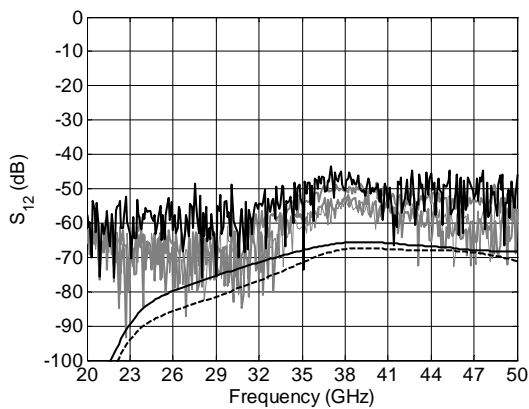
(b)



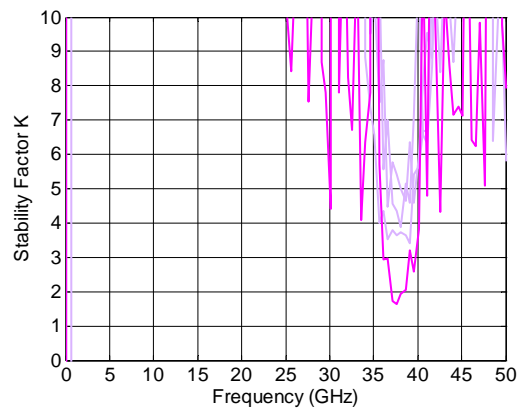
(c)



(d)



(e)



(f)

Fig. 6.9. Measured and simulated results of the designed MMIC LNA chip at RT. Measured results from different chips in colors: the best chip in terms of noise is plotted with dark colors whereas the other chips are plotted with soft colors. Simulation results with the extracted small signal model are plotted with black dashed line. Simulation results with the foundry library small signal model are plotted with black solid lines; (a) gain; (b) noise temperature; (c) input matching; (d) output matching; (e) reverse gain; (f) stability factor K .

From Fig. 6.9, the measured results are quite similar to the simulation with the extracted model which validates this model. Simulated stabilities are much higher than measured; therefore these results are not displayed. The small differences may be attributed to:

- Performance differences between the sample transistor, from where the model was extracted, and the actual transistors in the chips. These transistors belong to different batches and therefore they are affected by processing variations. As an example of this, Figure 6.10 compares the IV curves of the transistor from two different wafers: the sample wafer from where the model was extracted on the left, and the first wafer received from the foundry.

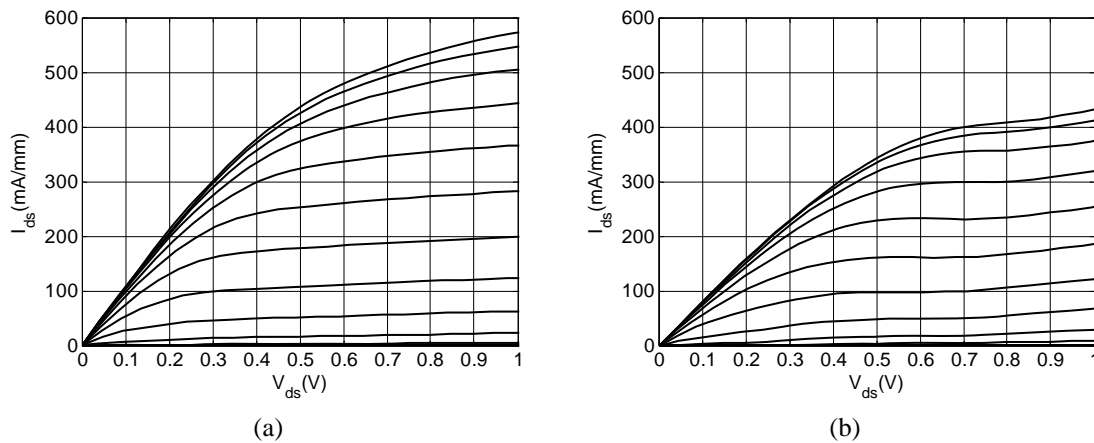


Fig. 6.10. Comparison between transistors from different wafers; (a) IV curves of the sample transistor; (b) IV curves of one transistor from the first wafer received from the foundry.

- Different polarizations between the model and the measured transistors. All the transistors in the simulated LNA have the same bias setting due to the available data to extract the model, whereas the transistors in the measured chips have slightly different bias settings in order to optimize their noise results.

On the other hand, the simulated results obtained with the foundry small signal model are quite different from the measured results. The foundry models predict higher current for this transistor and this could affect the simulated parameters, specially the noise, which would explain the differences shown in Fig. 6.9.

Measured results displayed with dark colors show a gain of $S_{21} = 30.9 \pm 1.9$ dB with a minimum noise temperature of $T_e = 116$ K in the 26 – 36 GHz band. Input

matching presents a worst value of $S_{11} = -8.5$ dB which can be easily improved varying slightly the bias point, and the output matching is better than 15 dB in the whole band. The remaining measured results plotted with soft colors show a good repeatability between chips and batches.

6.3. Amplifier Mechanical Design

For the characterization of the designed MMIC LNA at cryogenic temperatures a suitable module has been machined, since it is not available a cryogenic probe station. An artist view of the designed module is shown in Fig. 6.11 whereas its different drawings are included in Annex IV.

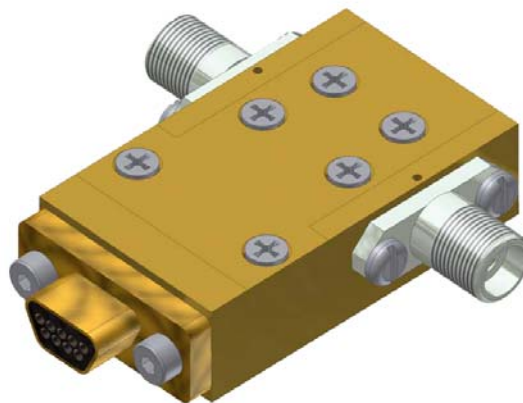


Fig. 6.11. Artist view of the designed amplifier. Dimensions are $34 \times 20 \times 9.5$ mm³ excluding connectors.

Both the module and the cover are machined in aluminum in order to improve the thermal conductivity (regarding to brass) and to reduce the total weight, enabling faster and colder cryogenic tests. Afterwards, these pieces are nickel and gold plated to avoid oxidation and enable wire bonding. A thin layer of gold, around 2.5 μm , is deposited over a 5 – 10 μm layer of nickel.

The module is composed of two cavities: one for the chip and the high frequency access lines, whereas the other houses the biasing networks as shown in Fig. 6.12.

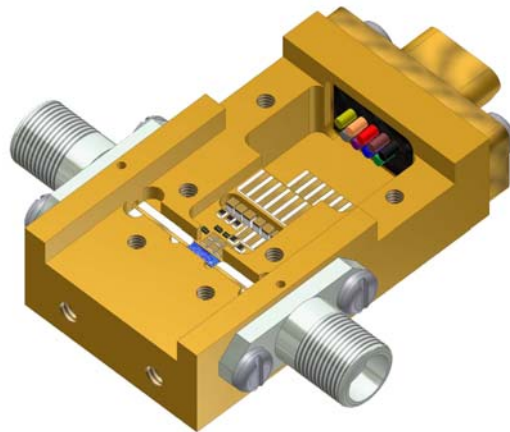


Fig. 6.12. Artist view of the designed amplifier with the cover removed.

The high frequency cavity has a width of 2 mm and thus the cut-off frequency of the first mode in this *waveguide* is 75 GHz, which is well above of the MMIC maximum operating frequency with gain. The depth of this cavity is 1.5 mm which enables to work with 1 mm diameter bits. In order to match the heights of the chip and the access lines a pedestal is machined in the module with a height of only 70 μm .

The transition between the coaxial connectors and the microstrip lines is made using sliding contacts as in Chapter III for the cryogenic attenuator. These components require more distance from the coaxial center axis to the cavity ground than a regular transition; in this case this distance is 370 μm .

Finally, the amplifier is equipped with two coaxial connectors model K103-F from Anritsu¹ for measurements up to 40 GHz, and with a DC connector model MDM-9PH003B from ITT Cannon which follows the pin out of Fig. 6.13 and Table 6.4.

Pin	Bias
1	GND
2	Vd1
3	Vg1
4	Vd2
5	Vg2
6	Vd3
7	Vg3
8	NC
9	NC

Table 6.4. Correspondence between pins and bias signals.

¹ Anritsu Company, 75081, Richardson, TX, USA.

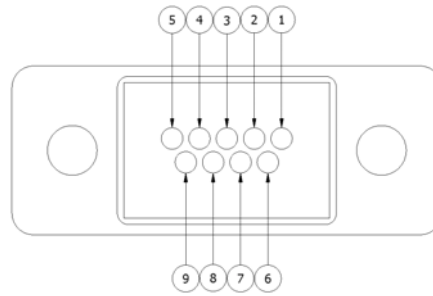


Fig. 6.13. Pin out of the DC connector. View from the cables side.

The amplifier final assembly is shown in Fig. 6.14.

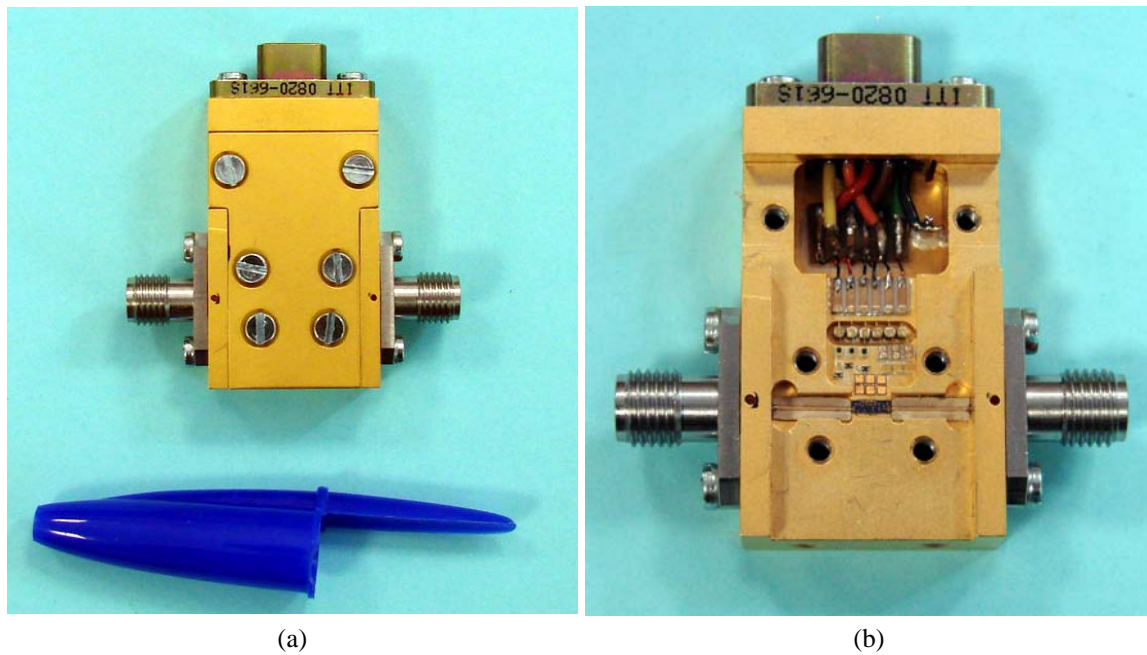


Fig. 6.14. Amplifier assembly; (a) external view, dimensions are $34 \times 20 \times 9.5 \text{ mm}^3$ excluding connectors; (b) internal view with cover removed.

6.4. Amplifier Characterization at Room and Cryogenic Temperatures

The designed amplifier is characterized both at room and cryogenic temperatures. At room temperature the S-parameters measurement is performed with the network analyzer E8364A from Agilent Technologies together with the K-calibration kit model 3652 from Anritsu. The results from this measurement, presented in Fig. 6.15, compare two measured circuits: the final LNA shown in Fig. 6.14 (solid lines) and one LNA prototype (dashed lines) with the same electrical design but mounted in an existing module to test the performance of the bias networks; therefore two different assembled chips are measured and compared.

The noise is measured following the setup shown in Fig. 6.8 for the prototype. In the case of the final amplifier (Fig. 6.14) the Ka-band conversion stage could not be used due to being damaged, hence a Q-band conversion stage was used and, as

consequence, only results for the 30 – 40 GHz band are presented. Once again the 10 dB attenuator is used at room temperature to improve the difference between reflection coefficients in the noise source from one state to the other.

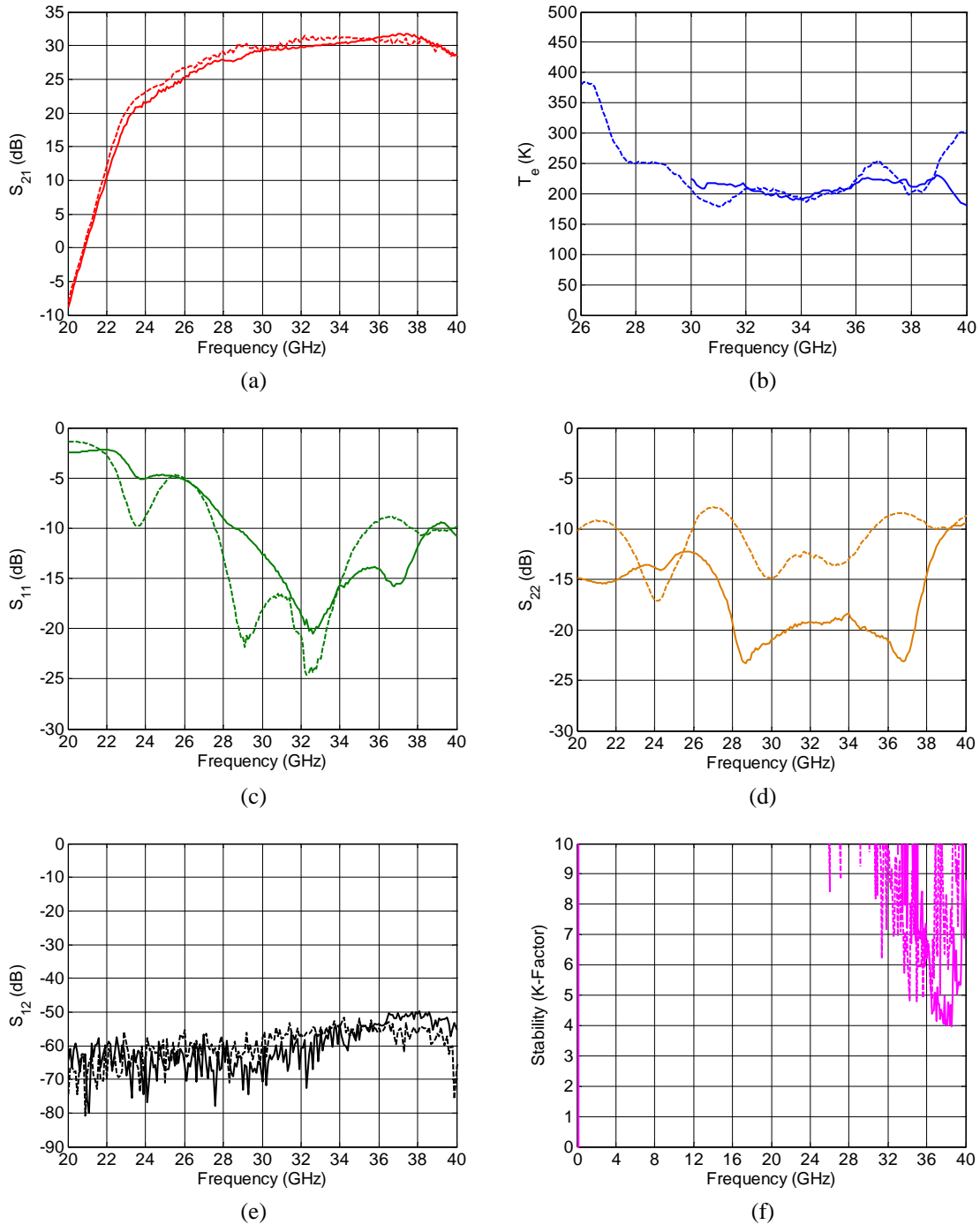
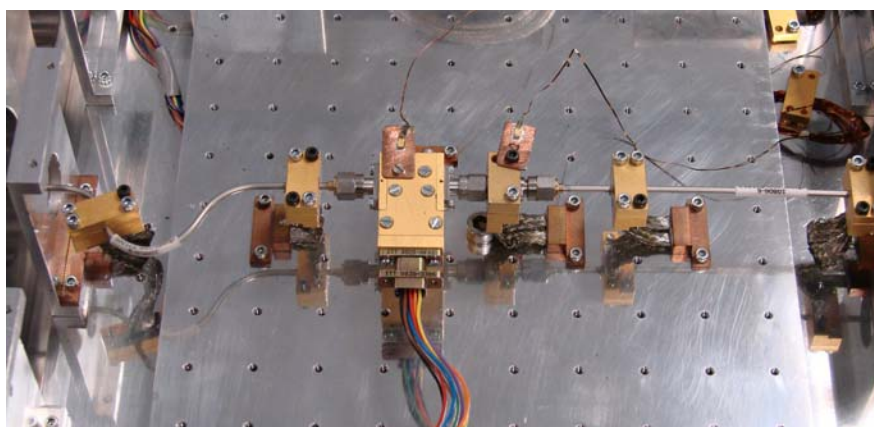


Fig. 6.15. Measured results of the assembled LNAs at room temperature. Solid lines are from the circuit shown in Fig. 6.14 and dashed lines are from a prototype; (a) gain; (b) noise temperature; (c) input matching; (d) output matching; (e) reverse gain; (f) stability factor-K. Bias points are: $V_{d1} = 1.2$ V, $I_{d1} = 7$ mA, $V_{d2} = 1.2$ V, $I_{d2} = 8$ mA, $V_{d34} = 1.2$ V, and $I_{d34} = 17$ mA for the final LNA; and $V_{d1} = 1$ V, $I_{d1} = 7$ mA, $V_{d2} = 1$ V, $I_{d2} = 8$ mA, $V_{d34} = 1.5$ V, and $I_{d34} = 17$ mA for the prototype LNA.

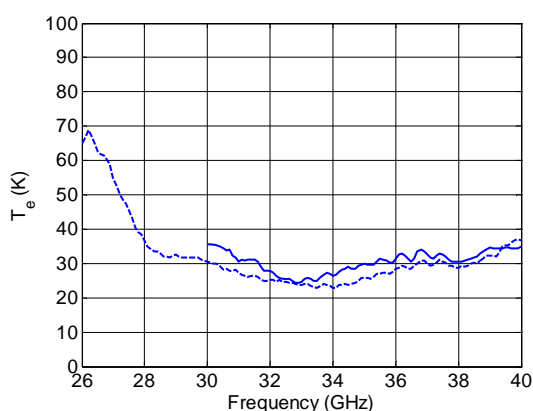
The room temperature results show a clear shift in frequency from the design that was already appreciable from the on-wafer measurements in Fig. 6.9. If the 28 – 40

GHz bandwidth is considered for the final LNA then the circuit presents a gain of 30 ± 2 dB with input and output return losses generally better than 10 dB. The improved return losses and reduced ripples in the noise measurement of the final amplifier regarding the prototype are believed to be due to the use of the sliding contacts in the coaxial connectors. These components were not used in the prototype because their use was not foreseen in the existing module design. It has been found that the sliding contacts have superior matching performance than the direct coaxial to microstrip transition. The noise temperature in the 30 – 40 GHz frequency range has a mean value of 203 K (noise figure of 2.3 dB).

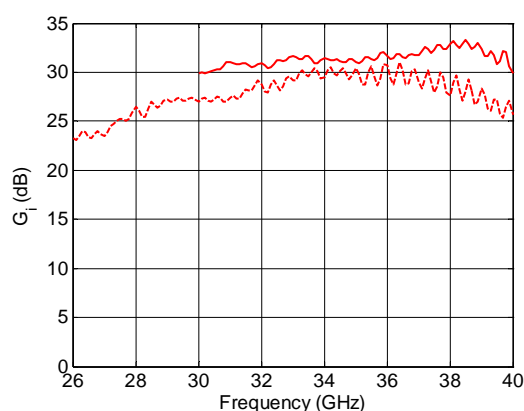
At cryogenic temperature the noise source is connected directly to the cryostat input line, i.e. without the 10 dB attenuator, since the cryogenic setup includes a 20 dB coaxial attenuator in the input line (cold-attenuator technique, see Fig. 6.16). Unfortunately, the noise of the cooled amplifiers could not be measured with the chip attenuator designed in Chapter III due to its unavailability at the moment of the measurements. The final LNA was only measured in the 30 – 40 GHz band. The gain and noise measurement results at 15 K ambient temperature are shown in Fig. 6.16.



(a)



(b)



(c)

Fig. 6.16. Cryogenic measurement of the designed final LNA (solid) on the prototype (dashed); (a) setup in the Dewar; (b) noise temperature; (c) insertion gain. Bias points are: $V_{d1} = 1.2$ V, $I_{d1} = 2$ mA, $V_{d2} = 1.2$ V, $I_{d2} = 3$ mA, $V_{d34} = 1.2$ V, and $I_{d34} = 9$ mA for the final LNA; and $V_{d1} = 0.7$ V, $I_{d1} = 2$ mA, $V_{d2} = 0.8$ V, $I_{d2} = 3$ mA, $V_{d34} = 1.2$ V, and $I_{d34} = 14$ mA for the prototype.

The measured cryogenic results show a minimum noise temperature value of 22 K at 34 GHz with appreciable differences between both circuits which are explained within the performance variability of the chips. This variability is more noticeable in the gain results of Fig. 6.16c where the final LNA has greater gain than the prototype. Both results are for optimum noise bias points.

6.5. Conclusions

This chapter has presented the design and measurement of a MMIC low noise amplifier for the Ka-band. The monolithic circuit has been designed with the D01MH process (0.13 μm mHEMT, GaInAs-InAlAs 40% indium content) from OMMIC foundry. The design is based in a home-made cryogenic transistor model from a sample wafer provided by the foundry.

At room temperature the chip shows a gain of $S_{21} = 30.9 \pm 1.9$ dB with a minimum noise temperature of $T_e = 116$ K in the 26 – 36 GHz band, whereas the assembled amplifier presents a gain of $S_{21} = 30 \pm 2$ dB with a minimum noise temperature of $T_e = 180$ K in the 30 – 40 GHz band. Return losses are generally better than 10 dB in the band of interest.

At cryogenic temperature the designed amplifier shows a gain of $S_{21} = 31.7 \pm 1.7$ dB with a minimum noise temperature of $T_e = 22$ K in the 30 – 40 GHz band. These results are satisfactory for an initial design, i.e. without re-design, and they are comparable with other results found in the literature for full MMIC amplifiers as shown in Table 6.5. Taking into account that this amplifier is designed with GaAs mHEMT technology, which is considerably cheaper than InP HEMT technology, these results demonstrate the suitability of this technology for antenna arrays projects where a large number of circuits are required.

Reference	Technology	Foundry	Bandwidth (GHz)	Gain (dB)	T_e @Cryo (K)	NF @RT (dB)	DC cons. (mW)
This work	0.13 μm mHEMT (In)	OMMIC	28 – 40	30 ± 2		2.3	37.2
			30 – 40	31.7 ± 1.7	22		16.8
[6.1]	0.18 μm pHEMT	OMMIC	26 – 40	> 18		< 3.8	
[6.2]	0.1 μm InP HEMT	NGST	26 – 36	42 ± 2	20		
[6.3]	0.25 μm mHEMT (Sb)	Rockwell	34 – 36	22		2.1	4.5
[6.4]	0.1 μm InP HEMT	NGST	26 – 40	21.9 ± 0.9		1.5	14
				23 ± 1	15.5		6
[6.5]	0.18 μm mHEMT (In)	Raytheon	28 – 33	> 23		< 1.6	15
[6.6]	pHEMT	Avago Tech.	26 – 40	20 ± 2		2.7 – 3	180

Table 6.5. Comparison between the results obtained with the designed LNA and other works about cryogenic full MMIC LNAs found in the literature.

