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Design of Efficient Microwave Power Amplifier Systems

PhD Thesis Dissertation

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Abstract

In the future communication systems, it is of key importance that the transceivers are capable of operating in multiple frequency bands and with complex signals. In this context, the power amplifier is a critical component of the transceiver, since it is responsible for most of the total power consumption in base stations and portable devices. Apart from the power consumption, the design of power amplifier systems must account for multi-band/broadband capabilities, high peak-to-average power ratio signals and the mismatch effect caused by the various operating conditions. Hence, the design of power amplifier topologies that enhance the total system efficiency and reliability is a challenging task.

This PhD dissertation introduces novel power amplifier architectures and solutions for modern communication systems. The contributions of this thesis can be divided in two parts. The first part deals with the study and design of power amplifier systems. It is of major importance that these designs provide linear amplification and operation at multiple frequency bands, which will permit the reduction of the cost and size of the devices. Additionally, the possibility to harvest the dissipated power from the power amplification process is investigated. For the development of the prototypes, lumped-element topologies, transmission line implementation and Substrate Integrated Waveguide (SIW) technology are adopted.

In the second part of the thesis, novel matching networks are introduced and their properties are studied. In particular, resistance compression topologies are proposed to overcome the performance degradation associated with the sensitivity of nonlinear devices to environmental changes. These networks can be adopted in

modern power amplifier architectures, such as envelope tracking and outphasing energy recovery power amplifier topologies, in order to provide improved performance over a wide range of operating conditions.

Resumen

Es primordial que los transceptores de los futuros sistemas de comunicación sean capaces de operar en múltiples bandas de frecuencia y con señales complejas. En este contexto, el amplificador de potencia es un componente crítico del transceptor dado que su consumo energético supone la mayor parte del consumo tanto de las estaciones base como de los dispositivos móviles. Aparte del consumo energético, los nuevos diseños de sistemas de amplificación de potencia deben considerar aspectos como la capacidad de operar en múltiples bandas o en banda ancha, el uso de señales con alta relación de potencia pico a potencia media (PAPR) y el efecto de desadaptación que aparece bajo las diferentes condiciones de funcionamiento. Por lo tanto, el diseño de nuevas topologías para amplificadores de potencia que mejoren la eficiencia total del sistema y la fiabilidad es una tarea compleja.

Esta tesis doctoral presenta nuevas arquitecturas de amplificadores de potencia y soluciones para los sistemas de comunicación modernos. Las contribuciones de esta tesis se pueden dividir en dos partes. La primera parte se centra en el estudio y diseño de sistemas de amplificación de potencia con el fin de proporcionar amplificación lineal y funcionamiento en múltiples bandas de frecuencia, lo que permitirá reducir el coste y tamaño de los dispositivos. Además, se investiga la posibilidad de reutilizar la energía disipada en el proceso de amplificación de potencia. Para el desarrollo de los prototipos, se utilizan topologías hibridas, implementaciones con líneas de transmisión y tecnología de guía de onda integrada en sustrato (SIW).

En la segunda parte de la tesis, se proponen redes de adaptación y se estudian sus propiedades. En particular, se proponen topologías de compresión de resistencia para minimizar el efecto que producen en el rendimiento la sensibilidad de los dispositivos no lineales a los cambios ambientales. Estas redes pueden ser utilizadas en arquitecturas modernas de amplificadores de potencia como pueden ser las topologías envelope tracking y outphasing energy recovery con el fin de proporcionar un rendimiento mejorado bajo múltiples condiciones de funcionamiento.

Acknowledgements

First of all, I would like to sincerely thank my PhD advisors Dr. Apostolos Georgiadis and Dr. Christos Verikoukis for giving me the opportunity to work with such an interesting research topic. I am more than grateful for their invaluable time and help during the last three years. Thank you for being always here to provide ideas, suggestions and comments, and mostly to teach me how to reach my goals!

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Thank you! Gracias! Gràcies! Ευχαριστώ πολύ!

List of Publications

This is a selected list of publications based on this PhD dissertation.

Journal Publications

[J3] *In Preparation* - K. Niotaki, A. Georgiadis, A. Collado and J. Vardakas, "Resistance Compression Networks for Improved Envelope Amplifier Performance".

[J2] *Accepted for Publication* - K. Niotaki, A. Georgiadis, A. Collado and J. Vardakas, "Dual-Band Resistance Compression Networks for Improved Rectifier Performance," *IEEE Trans. Microw. Theory Techn*.

[J1] K. Niotaki, A. Collado, A. Georgiadis and J. Vardakas, "5 Watt GaN HEMT Power Amplifier for LTE," *Radioengineering*, pp. 338 - 344, Apr. 2014.

Conference Publications

[C4] K. Niotaki, A. Collado, A. Georgiadis and J. Vardakas, "A dual-band power amplifier based on composite right/left-handed matching networks," *in Proc. 64th IEEE Electron. Compon. Technol. Conf.*, Orlando, FL, 2014, pp. 796-802.

[C3] K. Niotaki, F. Giuppi, A. Collado, A. Georgiadis and J. Vardakas, "A Broadband Power Amplifier Based on Composite Right/Left-Handed Half-Mode Substrate Integrated Waveguide," *in Proc. Conf. Design Circuits and Integr. Syst.*, Donostia-San Sebastian, 2013, pp. 289 - 293.

[C2] F. Giuppi, K. Niotaki, A. Collado and A. Georgiadis, “Challenges in energy harvesting techniques for autonomous self-powered wireless sensors,” *in Proc. 2013 European Microw. Conf.,* Nuremberg, 2013, pp. 854 - 857.

[C1] K. Niotaki, A. Georgiadis and A. Collado, “Thermal Energy Harvesting for Power Amplifiers,” *in Proc. 2013 IEEE Radio and Wireless Symp*., Austin, TX, 2013, pp. 196 - 198.

Talks/Presentations

[P1] K. Niotaki, A. Georgiadis and A. Collado, “Thermoelectric energy harvesting for power amplifiers,” *European Union COST IC0803 RF/Microwave Communication Subsystems for Emerging Wireless Technol.*, Belfast, May 2012.

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Notation

α	Seebeck coefficient
ΔT	Temperature gradient
$\Delta\varphi$	Phase shift of a single unit cell
Δf	Frequency spacing
η	Drain efficiency
η_c	Carnot efficiency
η_{conv}	Conversion efficiency
η_{PAE}	Power added efficiency
$\eta_{RF\text{-}DC}$	RF-DC conversion efficiency
η_{tot}	Total system efficiency
$\eta_{[f1]}$	Drain efficiency at the low operating frequency (in the case of dual-band circuit)
$\eta_{[f2]}$	Drain efficiency at the high operating frequency (in the case of dual-band circuit)
λ	Thermal conductivity
σ	Electrical conductivity
φ	Phase shift
$ACPR_L$	Lower adjacent channel power ratio
$ACPR_U$	Upper adjacent channel power ratio
$B_n(x)$	Modified Bessel function of order n
$B_0(x)$	Modified Bessel function of order 0
C	Electrical capacitance

C_{th}	Thermal capacitance
C/I	Carrier to intermodulation ratio
$(C/I)_L$	Lower carrier to intermodulation ratio
$(C/I)_U$	Upper carrier to intermodulation ratio
f	Operating frequency
f_L	Operating frequency of the RCN_L topology
f_R	Operating frequency of the RCN_R topology
f_1	Low operating frequency (in the case of dual-band circuit)
f_2	High operating frequency (in the case of dual-band circuit)
i_1	Diode current
G	Gain
I	Current
I_{ds}	DC current at the drain of the transistor
I_{gs}	DC current at the gate of the transistor
I_{PA}	Output current of the envelope amplifier
I_{sc}	Short circuit current
I_{s1}, I_{s2}	Diode saturation current
K	Stability factor
N	Number of unit cells
P_{dc}	Dissipated power
P_{dc_harv}	DC harvested power
P_{diode}	Dissipated power from the diode
P_{ds}	Dissipated power at the drain of the transistor
P_{EA}	Envelope amplifier output power
P_{gs}	Dissipated power at the gate of the transistor
P_{in}	RF input power
$P_{in[f1]}$	Input power at the low operating frequency (in the case of dual-band circuit)
$P_{in[f2]}$	Input power at the high operating frequency (in the case of dual-band circuit)
P_{loss}	Total losses from the envelope amplifier operation
P_{max}	Maximum harvested DC power
P_{opamp}	Dissipated power from the operational amplifier

P_{out}	RF output power at the fundamental frequency
P_{out_L}	Total power in the lower adjacent-channel
P_{out_U}	Total power in the upper adjacent-channel
$P_{out[f1]}$	Output power at the low operating frequency (in the case of dual-band circuit)
$P_{out[f2]}$	Output power at the high operating frequency (in the case of dual-band circuit)
$P_{out[2f1-f2]}$	Output power at the third-order intermodulation products at the frequency ($2f_1$-f_2)
$P_{out[2f2-f1]}$	Output power at the third-order intermodulation products at the frequency ($2f_2$-f_1)
P_{rf}	RF available power
P_{tran}	Dissipated power from the switching transistor
P_{1dB}	1 dB compression point
Q	Heat
R_{A25N}	Thermal resistance of the substrate and the contact
R_{D1}	Thermal resistance of the device (junction-ambient)
R_{D2}	Thermal resistance of the device (junction-substrate)
R_{elec}	Electrical resistance
R_{HS}	Thermal resistance of the heatsink
R_L	Output load of the rectifier
R_{load}	Output load of the resistance compression networks
R_{PA}	Drain/Collector resistance
$R_{TEGPack}$	Total thermal resistance of the TEG package
R_{TEGPCB}	Thermal resistance of the TEG PCB
R_{th}	Thermal resistance
T	Temperature
T_{cold}	Temperature at the cold side of the TEG
T_{hot}	Temperature at the hot side of the TEG
$\overline{T}$	Mean temperature
V	Voltage
V_{dclev}	DC level of the input signal
V_{dc1}	Supply voltage of the switching transistor

V_{dc2}	Supply voltage of the operational amplifier
V_{ds}	Drain voltage
V_{gs}	Gate voltage
V_{in}	Envelope of the transmitted signal
V_L	Output DC voltage
V_{oc}	Open circuit voltage
V_{PA}	Output voltage of the envelope amplifier
V_{pp}	Peak to peak voltage
V_t	Thermal voltage
Y	Admittance
Z	Impedance
Z_{cap}	Capacitor reactance
Z_{in}	Input impedance
Z_{ind}	Inductor reactance
Z_L	Characteristic impedance of the RCN_L topology
Z_R	Characteristic impedance of the RCN_R topology
Z_{th}	Figure of merit of thermoelectric materials
Z_1	Diode input impedance

Abbreviations

ACPR	Adjacent Channel Power Ratio
ADS	Advanced Design System
AWG	Arbitrary Waveform Generator
Bi_2Te_3	Bismuth Telluride
BJT	Bipolar-Junction Transistors
BS	Base Station
BW	BandWidth
CCDF	Complementary Cumulative Distribution Function
CPU	Central Processing Unit
CRLH	Composite Right/Left-Handed
DC	Direct Current
DC-DC	Direct Current to Direct Current
DE	Drain Efficiency
DPS	Dynamic Power Supply
EA	Envelope Amplifier
EER	Envelope Elimination and Restoration
EH	Energy Harvesting
EM	Electromagnetic
ET	Envelope Tracking
E-pHEMT	Enhancement mode Pseudomorphic High Electron Mobility Transistor
FEM	Finite Element Method
FET	Field Effect Transistor

FOM	Figure Of Merit
GaN	Gallium Nitride
GPS	Global Positioning System
GSM	Global System for Mobile communication
HB	Harmonic Balance
HEMT	High Electron Mobility Transistor
HFSS	High Frequency Structural Simulator
HMSIW	Half-Mode Substrate Integrated Waveguide
HSA	Hybrid Switching Amplifier
IMD	InterModulation Distortion
IoE	Internet of Everything
IoT	Internet of Things
ISM	Industrial, Scientific and Medical
LC	Inductor-Capacitor
LE	Lumped-Element
LH	Left-Handed
LSSP	Large Signal S-Parameter
LTE	Long-Term Evolution
LTE-A	LTE-Advanced
MTM	Metamaterial
OFDM	Orthogonal Frequency Division Multiplexing
PA	Power Amplifier
PAE	Power Added Efficiency
PAPR	Peak-to-Average Power Ratio
PCB	Printed Circuit Board
RCN	Resistance Compression Network
RF	Radio Frequency
RH	Right-Handed
SDD	Symbolically Defined Device
SG	Signal Generator
SIW	Substrate Integrated Waveguide
SMD	Surface Mounted Device
SoA	State-Of-the-Art

TEG	ThermoElectric Generator
TGP	ThermoGenerator Package
TL	Transmission Line
UE	User Equipment
UHF	Ultra High Frequency
VHF	Very High Frequency
VSA	Vector Signal Analyzer
Wifi	Wireless Fidelity
WiMAX	Worldwide Interoperability for Microwave Access
WPT	Wireless Power Transfer
2G	Second Generation
2.5G	Second and a half Generation
3G	Third Generation
4G	Fourth Generation

Chapter 1

Introduction

1.1 Motivation and Thesis Objectives

In 1940s (during the World War II), the development of Radar in microwave frequencies introduced the application of microwaves in communication systems [1]. The term microwave signals refers to the alternative current signals that occupy the frequency band of 300 MHz to 300 GHz in the electromagnetic spectrum [1]. Some of the benefits provided by microwave applications are the increased bandwidth and the use of line of the sight propagation with the tradeoff of the increased complexity in the analysis and the design of microwave circuits.

In 1947, John Bardeen, Walter Brattain and William Shockley invented the transistor, which had a significant impact in the evolution of electronics and communication systems [1]-[3]. Transistor has played a key role in the development of critical electronic components, such as power amplifiers (PAs) and oscillators. So far, numerous investigations have been carried out for the evolution of transistors that have already resulted in two main categories: the Bipolar-Junction Transistors (BJTs) and the Field Effect Transistors (FETs) [3], [4]. The best candidate for each application depends on a variety of parameters, including the desired output power level and the operating frequency.

The design of active microwave electronic circuits poses numerous challenges in developing efficient solutions for the current communication systems. Among them stands the design of efficient power amplifier circuits for modern communication standards, multi-band/broadband nonlinear devices and circuits with reduced sensitivity to environmental changes.

In this context, this thesis is focused on investigating novel solutions for the power ampification stage of modern transceivers. In particular, this work can be mainly divided in two parts: i) Chapter 2, 3 and 4 consider different approaches for the design of power amplifier systems and ii) Chapter 5 and 6 investigate resistance compression networks in order to alleviate the problem of impedance changes in power amplifier topologies.

1.1.1 Challenges of Radio Frequency (RF) Power Amplifiers

Nowadays, power amplifiers are critical components for the design of base stations (BSs) and mobile user equipment (UE). According to [5], [6], the power amplification process in a base station consumes up to 65 % of the total power consumption, as it shown in Figure 1.1. Therefore, power amplifiers are key components to reduce the power consumption in base stations, contributing to the total system efficiency and reliability. The same applies for the power amplifier components utilized in mobile user equipment, such as the smartphones, where the main goal is to boost the battery life, and thus increase the limited standby/talk time of the handset.

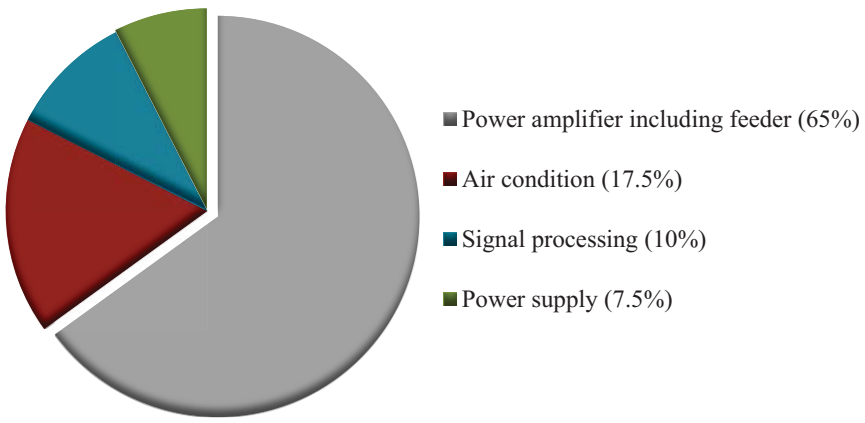

Figure 1.1: Average power consumption distribution in base stations. The data are taken from [5], [6].

Additionally to the efficiency requirements, modern wireless communication standards imply new constraints in the design of the power amplification stage due to the emergence of new signal modulation schemes. In contrast with the second generation cellular systems (2G), modern modulation techniques produce high bandwidth signals that are characterized with a non-constant envelope. In many cases, the signal envelope (i.e. LTE-Advanced) exceeds the peak-to-average power ratio (PAPR) of 10 dB [7], [8]. Figure 1.2 shows how the peak-to-average power ratio of communication standards has evolved from the 2G to 4G systems. In order to efficiently amplify such signals, the power amplifier should operate with a good efficiency over a wide range of input power levels. Additionally to the high efficiency requirements, linearity has also become a primary concern and the power amplifier should operate at its back off power region. Thus, there is an inherent tradeoff between linearity and efficiency in modern communication systems.

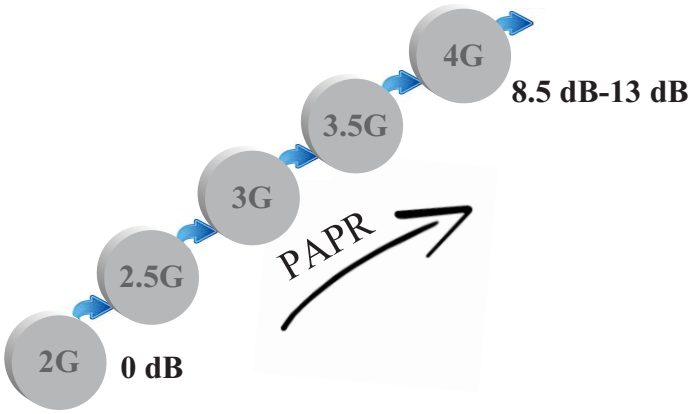

Figure 1.2: The evolution of the peak to average power ratio of wireless communication standards. The data are taken from [8].

Simultaneously, the emergence of new communication standards requires transceivers capable of operating at multiple frequency bands, especially in the case of portable devices where the size of the device is of great importance. To this end, the design of multi-band and broadband PAs is a major challenge that may allow the operation of different standards in the same equipment and thus lead to cost-effective and compact devices. The major challenge that arises from the design of multi-band power amplifiers is the implementation of the impedance matching networks that should meet similar behavior at two frequency bands.

Taking into account the significance of the power amplification process in modern transceivers and the associated design challenges as part of the total system performance, Chapters 2, 3 and 4 deal with the introduction of novel power amplifier systems. In particular, Chapters 2 and 3 are mainly focused on investigating power amplifier topologies for modern communication systems with the design and characterization of various PAs topologies. In Chapter 4, a novel way to exploit the dissipated power from the power amplification process, using a commercial thermoelectric generator and its conversion to useful DC power is proposed.

1.1.2 Resistance Compression Networks

Microwave circuits are usually designed for specific operating conditions, including frequency of operation, input power level and fixed output load. In many cases, the design of multi-band or broadband matching networks is needed for the implementation of multi-band and broadband microwave circuits. The design of such impedance matching networks is a complex task in which the desired tradeoff between the performances at the operating frequencies should be considered.

Although the nonlinear devices are usually optimized for specific operating conditions, their input power level and/or the output load usually vary due to the changes in the surrounding environment. For instance, the design of envelope amplifier circuits for dynamic power supply schemes is a major issue due to the time-varying operating conditions. In this case, the envelope amplifier should be designed to operate for a time-varying load that represents the RF power amplifier (typically in the range of 1 Ω - 100 Ω [8]), as Figure 1.3 shows. Therefore, it is a challenging task to keep the efficiency of the envelope amplifier high for a wide range of output load values.

The same challenge applies for the design of rectifier circuits for outphasing power amplifier architectures (with a power recycling network) and for energy harvesting applications. In outphasing PAs, the isolation resistance of the power combiner circuity can be replaced with a rectifier topology in order to recover the dissipated power (Figure 1.4a). In such a topology, an impedance variation between the ports of the power combiner results in an impedance mismatch and non-perfect isolation between the RF power amplifier outputs [9]. Thus, the design of rectifier

circuits with reduced sensitivity to the surrounding environment conditions is of great concern in order to improve the isolation between the RF PAs and thus the performance of the outphasing energy recovery amplifier.

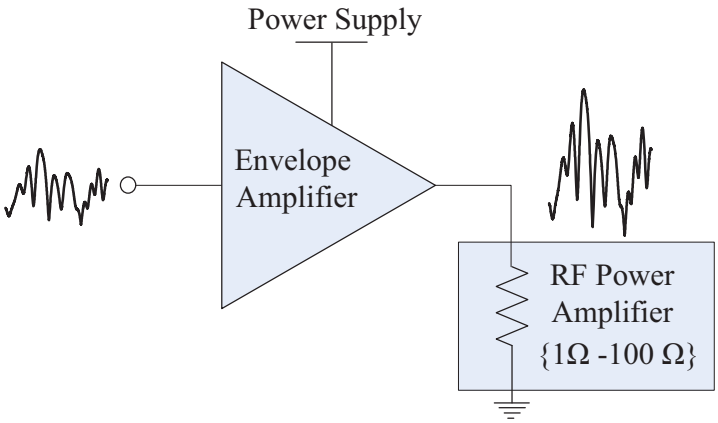

Figure 1.3: Envelope amplifier topology, where the drain/collector of the RF power amplifier is represented as a resistance.

In the same way, the input power of rectifiers for energy harvesting (EH) applications is not constant since the availability of the harvested power level depends on the application scenario. Such an input power variation results in an input impedance change at the input of the diode. Furthermore, the output of the rectifier is usually connected to a time-varying load (such as a DC-DC converter) that also results in an input impedance change at the input of the rectifying device (Figure 1.4b).

The impedance mismatch caused by such environmental changes results in degraded performance. Thus, the design of rectifiers with reduced sensitivity to the surrounding environment conditions is of great importance. An even more challenging task is the design of multi-band microwave circuits with reduced sensitivity to such changes.

In order to alleviate the problem of such impedance changes in microwave circuits, special consideration should be paid in the design of the impedance matching networks. Recently, the concept of resistance compression network (RCN) has been introduced as a novel kind of matching networks that alleviates the sensitivity of microwave circuits to environmental changes [10].

As part of this work, novel impedance matching networks for power amplifier topologies are proposed. Chapter 5 considers novel resistance compression networks

for the design of envelope amplifier circuits, while Chapter 6 proposes dual-band resistance compression topologies that find successful application in rectifier circuits for power recycling networks in outphasing PA systems.

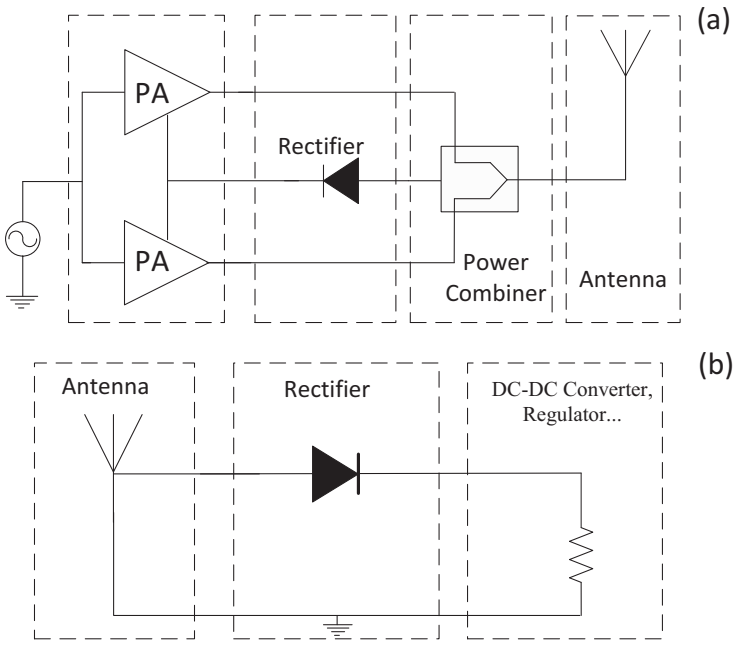

Figure 1.4: Application of rectifiers in a) a simplified topology of an outphasing power amplifier with a power recycling network and b) an architecture for energy harvesting application.

1.2 Thesis Structure

The contribution of this thesis is divided in two parts:

I. The first part mainly deals with the power amplification process which dominates the power consumption in base stations and portable devices. In Chapter 2 and Chapter 3, the design of power amplifier topologies for modern transceivers is proposed, while an approach to exploit their dissipated power and convert it to useful DC power is analyzed in Chapter 4.

II. The second part introduces the design of resistance compression networks for PA architectures, such as envelope tracking topologies and outphasing energy recovery power amplifiers. In particular, the concept of dual-band RCNs is introduced, while the resistance compression properties are applied in the design of i) an envelope amplifier topology

(Chapter 5) and ii) a dual-band rectifier (Chapter 6). Such a dual-band RCN based rectifier can find successful application in RF energy harvesting applications and wireless power transfer scenarios, where the rectifier has to operate with highly time-varying conditions.

The thesis is divided in seven Chapters. A brief description of each Chapter is given at the rest of this Section.

CHAPTER 2

Chapter 2 considers the design of a linear stand-alone power amplifier capable of operating with modern communications signals that are characterized with time-varying envelopes. A GaN HEMT transistor is selected for the design and the implementation of the power amplifier. The linearity of the proposed topology is validated with different input signals. In order to maximize the efficiency of the proposed circuit, the concept of applying the RF power amplifier in an envelope tracking (ET) architecture is also considered. The contributions of Chapter 2 were published in the Radioengineering journal.

- K. Niotaki, A. Collado, A. Georgiadis and J. Vardakas, "5 Watt GaN HEMT Power Amplifier for LTE," *Radioengineering*, pp. 338 - 344, Apr. 2014.

CHAPTER 3

Multi-band and broadband power amplifiers are crucial components to employ different communication standards in the same equipment. Chapter 3 considers the design of a 2.4 GHz/3.35 GHz power amplifier based on the use of Composite Right/Left-Handed (CRLH) unit cells as the impedance matching networks of the topology. In this Chapter, the approach of designing a broadband (from 2.3 GHz to 3.5 GHz) power amplifier based on the same concept is also examined. The current design investigates the implementation of CRLH unit cells in Substrate Integrated Waveguide (SIW) technology. The contributions of Chapter 3 were presented in the 2012 Conference on Design of Circuits and Integrated Systems and in the 2013 IEEE Electronic Components and Technology Conference.

- K. Niotaki, F. Giuppi, A. Collado, A. Georgiadis and J. Vardakas, "A Broadband Power Amplifier Based on Composite Right/Left-Handed Half-Mode Substrate Integrated Waveguide," *in Proc. Conf. Design Circuits and Integr. Syst.*, Donostia-San Sebastian, 2013, pp. 289 - 293.
- K. Niotaki, A. Collado, A. Georgiadis and J. Vardakas, "A dual-band power amplifier based on composite right/left-handed matching networks," *in Proc. 64th IEEE Electron. Compon. Technol. Conf.*, Orlando, FL, 2014, pp. 796-802.

CHAPTER 4

Chapter 4 considers the potential of exploiting the dissipated power from the power amplifier operation. A simplified thermal model that predicts the amount of DC power that can be obtained from a specific thermal harvesting scenario that includes a power amplifier is proposed. A set of experiments are carried out to predict the amount of the harvested DC power from a power amplifier circuit with a dissipated power of 1.37 Watt. The contributions of this Chapter were presented in the 2012 COST IC0803 RF/Microwave Communication Subsystems for Emerging Wireless Technologies workshop, the 2013 IEEE Radio and Wireless Week conference and the 2013 IEEE European Microwave Conference.

- K. Niotaki, A. Georgiadis and A. Collado, "Thermoelectric energy harvesting for power amplifiers," *8th COST IC0803 RF/Microwave Communication Subsystems for Emerging Wireless Technologies Group Meeting and Workshop*, Belfast, May 2012.
- K. Niotaki, A. Georgiadis and A. Collado, "Thermal Energy Harvesting for Power Amplifiers," *in Proc. 2013 IEEE Radio and Wireless Symp*., Austin, TX, 2013, pp. 196 - 198.
- F. Giuppi, K. Niotaki, A. Collado and A. Georgiadis, "Challenges in energy harvesting techniques for autonomous self-powered wireless sensors," *in Proc. 2013 European Microw. Conf.,* Nuremberg, 2013, pp. 854 - 857.

CHAPTER 5

Chapter 5 investigates a method to improve the performance of an envelope amplifier circuit by adding a resistance compression network (RCN) at the switching stage of a hybrid envelope amplifier topology. A novel way to achieve resistance compression is introduced and applied for the design of the envelope amplifier. In order to evaluate the performance of the proposed design, a conventional hybrid envelope amplifier is also designed and fabricated. The considered design exhibits reduced sensitivity to the environmental conditions and improved performance in comparison with a conventional topology without resistance compression network. The contributions of this Chapter will be submitted in a journal.

- K. Niotaki, A. Georgiadis, A. Collado and J. Vardakas, "Resistance Compression Networks for Improved Envelope Amplifier Performance," *(in preparation)*.

CHAPTER 6

In Chapter 6, the concept of dual-band resistance compression networks is introduced and applied to the design of a rectifier circuit with improved performance. The operation principles of these dual-band matching networks are presented in detail. The proposed dual-band RCN can be used as the matching network located between the antenna and the rectifying element of a dual-band rectifier for energy harvesting applications or as part of an outphasing energy recovery power amplifier architecture. A dual-band (915 MHz / 2.45 GHz) rectifier based on RCN is designed and characterized showing improved performance in comparison with a conventional dual-band envelope detector by exhibiting improved RF-DC conversion efficiency and reduced sensitivity versus output load and input power variations. The contributions of this Chapter were submitted in the IEEE Transactions on Microwave Theory and Techniques.

- K. Niotaki, A. Georgiadis, A. Collado and J. Vardakas, "Dual-Band Resistance Compression Networks for Improved Rectifier Performance", *IEEE Trans. Microw. Theory Techn.* (*Accepted for Publication*).

CHAPTER 7

Chapter 7 concludes the dissertation considering some potential research directions for future development.

Chapter 2

A Linear GaN HEMT Power Amplifier

2.1 Introduction

The increasing demand for radio frequency (RF) power amplifiers (PAs) in communication systems has led to enormous research efforts towards the development of reliable and low-cost circuit designs with the best tradeoff between linearity and efficiency. As communication systems evolve to higher data rates the modulation schemes generate complex signals that are characterized by non-constant envelopes with high peak-to-average power ratio (PAPR). Modern modulation schemes in 4G signals, such as Long-Term Evolution (LTE), are characterized with a PAPR that exceeds the value of 10 dB [8]. For instance, the PAPR of a Long-Term Evolution (LTE) signal is in the range of 8.5 dB to 13 dB [8]. Figure 2.1 shows the complex waveform of the envelope of a 5 dBm LTE downlink signal with a bandwidth (BW) of 20 MHz.

The high PAPR signals should be amplified linearly to avoid the signal distortion and thus the power amplifier should operate below the saturation at back off. To improve the efficiency in the back off region, several efficiency enhancement techniques have already been proposed in the literature, including the envelope tracking (ET) technique [7], [11], [12]. The ET topology consists of an RF PA operating at its linear region and a dynamic power supply (DPS) that adjusts the

power supply voltage provided to the amplifier according to the input power level. Several ET systems have been proposed in the literature recently [13]-[18].

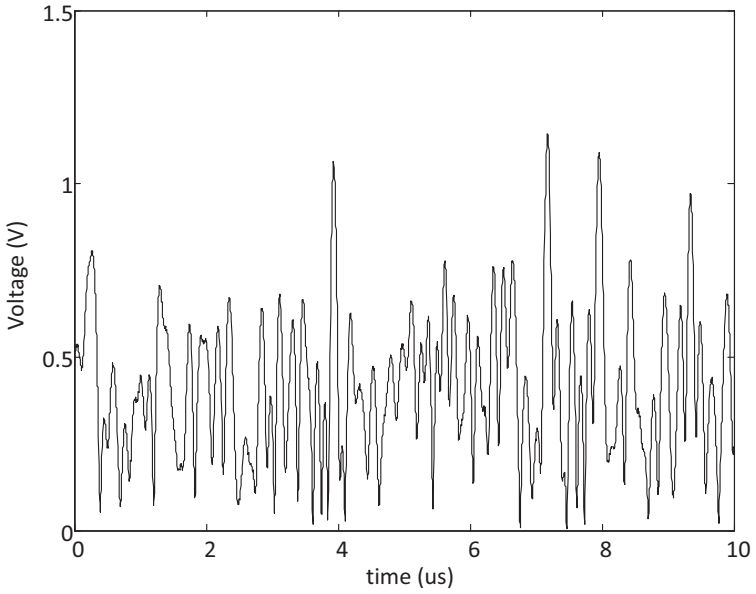

Figure 2.1: Measured waveform of the envelope of a downlink 5 dBm 20 MHz LTE signal in the time domain.

The design of the PA usually starts with the selection of the proper device and the set of specifications. So far, various structures of transistors have been developed. Figure 2.2 shows the main classes of power devices, including the Bipolar-Junction Transistors (BJTs) and the Field Effect Transistors (FETs) transistor technologies. The best candidate for each application depends on a variety of parameters, including the desired output power level and operating frequency. Among the candidates for ET power amplifiers for base stations (BSs) stands the design of gallium nitride (GaN) high electron mobility transistor (HEMT) RF power amplifiers because of the inherent advantages of high breakdown voltage, high efficiency, high power density and large bandwidth [19]-[21].

The specifications for the design of a PA circuit depend on the targeted application and are significantly different for user equipment (UE) or base stations (BSs) [22]. The requirements for UE in terms of output power and linearity are modest in comparison to the BS power amplifiers due to the high power that is involved in the BS operation [22]. The tight requirements for the design of high power PAs usually result in a decreased efficiency and thus, the design of a high power linear RF power amplifier is considered as an even more challenging task.

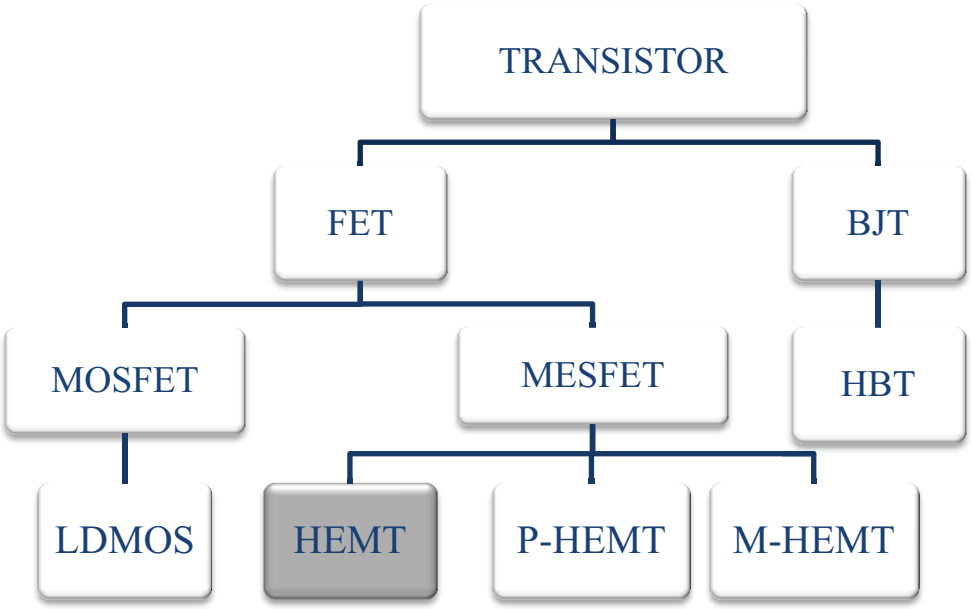

Figure 2.2: Classes of transistors. The data come from [3].

In this Chapter, taking into account the significance of the power amplification stage for modern transceivers, a 5 Watt stand-alone GaN HEMT linear power amplifier that can have successful application in ET systems is proposed. The PA is also manufactured and its performance is evaluated in terms of linearity, output power and efficiency. Various input signals, such as single carrier, two-tone and LTE signals are used for the characterization of the proposed design.

The outline of this Chapter is as follows. Section 2.2 presents the design of the GaN HEMT PA. The device is designed and optimized for optimum tradeoff between linearity and efficiency at 2.4 GHz. In Section 2.3, the fabrication procedure of the RF PA is described in detail. Section 2.3 also includes the experimental characterization of the power amplifier in terms of power gain (G), power added efficiency (η_{PAE}) and drain efficiency (η). Section 2.4 presents additional measurements to evaluate the linearity of the amplifier, such as two-tone intermodulation distortion (IMD) and adjacent channel power ratio (ACPR) measurements. Section 2.5 summarizes the conclusions of the presented work.

2.2 Design of GaN HEMT Power Amplifier

GaN devices are promising candidates for the design of microwave PAs mainly due to the advantages of high power density and high breakdown voltage, as it has already been discussed in the previous Section [23], [24]. A plethora of microwave GaN HEMT PAs has already been presented in the literature demonstrating good performance for a variety of applications [25]-[33].

The design of GaN HEMT power amplifiers operating at the Ultra High Frequency (UHF) and Very High Frequency (VHF) band is a challenging task as the devices are characterized with high gain at these frequencies and thus, special attention should be paid for the stability of the device [26]. A VHF/UHF high power amplifier (20 W), operating in the frequency band of 50 MHz to 550 MHz has been proposed in [25], with a drain efficiency in the range of 63 % to 72 % in the corresponding band. A GaN HEMT PA operating at the 5.8 GHz band has been presented in [27] demonstrating a 33.3 dBm output power at 5.65 GHz. A GaN HEMT device has also been selected for a high power amplifier (310 W) that has shown a power gain of 10 dB over the frequency band of 8.5 GHz - 10 GHz [29].

In this Chapter, a GaN HEMT transistor from Cree (CGH40006P) that operates up to a frequency of 6 GHz is chosen for the design and implementation of the microwave power amplifier [34], [35]. The PA is designed using the harmonic balance (HB) analysis and S-parameter analysis in Agilent Advanced Design System (ADS) software. The schematic of the designed power amplifier is shown in Figure 2.3a. The drain and gate bias networks are implemented as quarter wavelength bias lines with some decoupling capacitances, including chip capacitances and a radial stub with width=0.415 mm, length=19 mm and angle=70^{o}. DC-blocking capacitances are placed in the input (C_1, C_2) and output (C_3) matching networks (Figure 2.3a).

The topology of the power amplifier includes three resistances (R_1, R_2 and R_3) that contribute to the global stabilization of the power amplifier for all the expected operation conditions in terms of bias voltage and input power level. Stability considerations should always be taken into account in the design of nonlinear devices in order to eliminate oscillation problems [36].

The input and output matching networks are designed and optimized to match the power amplifier to 50 Ω. Small-signal S-parameters and Large-signal S-

parameter (LSSP) analysis is also used to impose constraints on the impedance matching of the nonlinear device at the operating frequency band. The matching network parameters are optimized to match the instantaneous output impedance of the transistor at the fundamental frequency (2.4 GHz). The final circuit parameters are shown in Table 2.1.

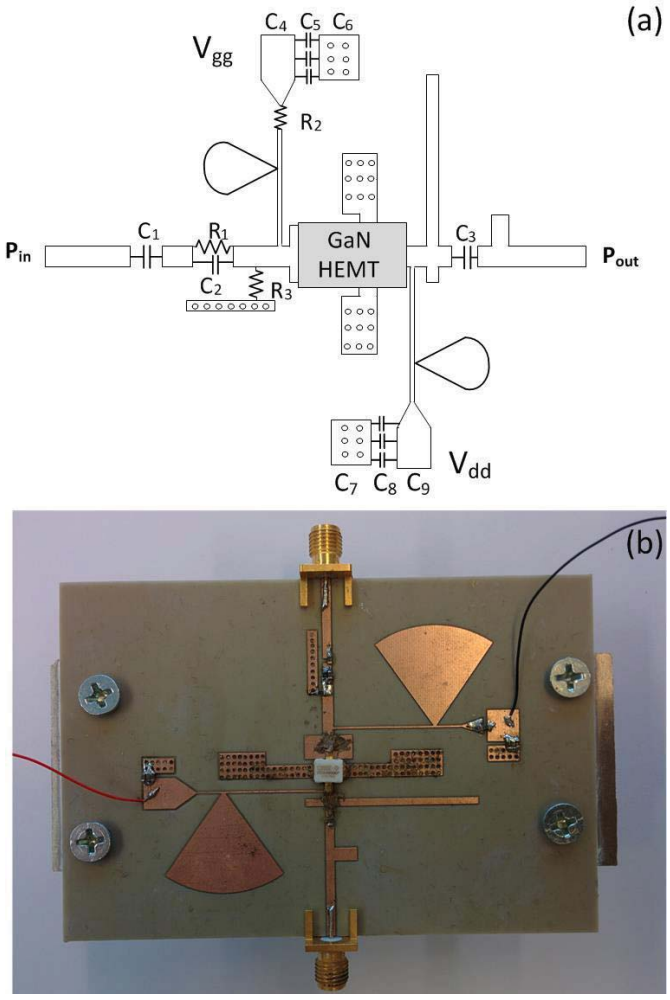

Figure 2.3: GaN HEMT power amplifier: a) Simulated circuit topology and b) fabricated prototype. The fabricated prototype has a total size of 6 cm x 10 cm. The active device is a GaN HEMT transistor from Cree (CGH40006P) [34].

Design specifications for the linearity of the device are taken into account during the design of the power amplifier. The proposed system is excited with a two-tone input signal at f_1 GHz and f_2 GHz, with equal input power levels ($P_{in[f1]}$=$P_{in[f2]}$), where $f_2 > f_1$. The main goal of the optimization process is to minimize the output power of the third order components, at $2f_1$-f_2 GHz ($P_{out[2f1-f2]}$) and at $2f_2$-f_1 GHz ($P_{out[2f2-f1]}$), as Figure 2.4 shows.

In order to do so, a two-tone HB simulation, in combination with two optimization goals, one at each third order intermodulation product, are used aiming at minimizing the power level at these frequency components (Figure 2.4). The IMD sweet spots are also examined to minimize the level of the nonlinear distortion (IMD) [36]-[38]. The IMD sweet spots are particular points of operation that lead to reduced third order intermodulation products and depend on the bias of the device, as well as the input power level [37].

Component	Value	Component	Value
C_1	1 pF	C_4	6.8 nF
C_2	0.5 pF	C_5	22 nF
C_3	3.3 pF	C_6	47 nF
R_1	5 Ω	C_7	6.8 nF
R_2	52 Ω	C_8	22 nF
R_3	390 Ω	C_9	47 nF

Table 2.1: GaN HEMT power amplifier circuit (Figure 2.3a) component values.

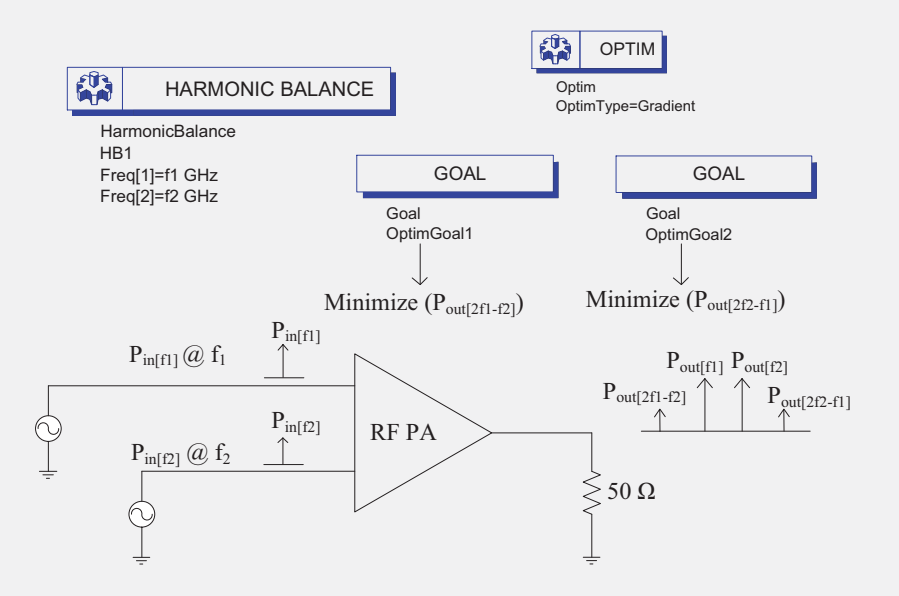

Figure 2.4: Simplified schematic of the optimization process that minimizes the level of the nonlinear distortion for a two-tone input signal, using HB analysis in Agilent ADS software.

High linearity should be met at high output power levels close to 1 dB compression point. The selected operating frequencies are f_1=2.395 GHz and

f_2=2.405 GHz and the input power level is $P_{in[f1]}$=$P_{in[f2]}$=22 dBm. A comparison of the carrier to intermodulation ratio for different values of the gate voltages is shown in Figure 2.5. The optimum carrier to intermodulation ratio is predicted from the nonlinear simulation when the device is biased with a drain voltage (V_{ds}) of 35 V and a gate voltage (V_{gs}) of -3.5 V. The simulation results show a high linearity level for a wide input power range when the device operates in its linear region for the selected bias conditions.

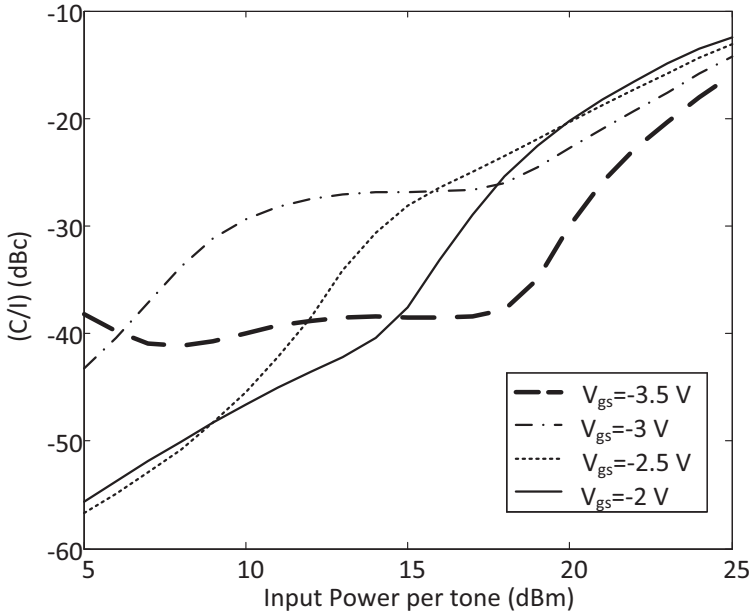

Figure 2.5: Simulated C/I ratio versus input power level per tone for V_{gs}= -3.5 V, V_{gs}= -3 V, V_{gs}= -2.5 V and V_{gs}= -2 V. The selected operating frequencies are f_1=2.395 GHz and f_2=2.405 GHz. The results are obtained when the device is biased with a drain bias of 35 V.

Figure 2.6 shows the simulated output power and the carrier to intermodulation ratio of the power amplifier when excited by a two-tone signal around 2.4 GHz (f_1=2.395 GHz and f_2=2.405 GHz). The x-axis corresponds to the total power of one of the tones, which means the total input power at the amplifier is 3 dB higher. The output power at the operating frequencies ($P_{out[f1]}$ and $P_{out[f2]}$) is shown in the plot, along with the upper and lower carrier to intermodulation ratios (C/I_L and C/I_U). Details about the calculation of the carrier to intermodulation ratio are given in Section 2.3. A reduced IMD is noticed when the PA operates with total input power from 8 dBm (5 dBm each tone) to 23 dBm (20 dBm each tone) for the selected bias conditions.

The potential use of the device as the RF PA of an ET topology is examined by varying the drain voltage of the device. The performance of the device is compared

for different V_{ds} when the power amplifier operates with an input signal at 2.4 GHz and for V_{gs}=-3.5 V. The simulated performance of the power amplifier over a wide range of output power levels is shown in Figure 2.7 and Figure 2.8. The simulation results are obtained when the PA operates at 2.4 GHz and for V_{gs}=-3.5V. Details about the calculation of the power added efficiency are provided at Section 2.3.

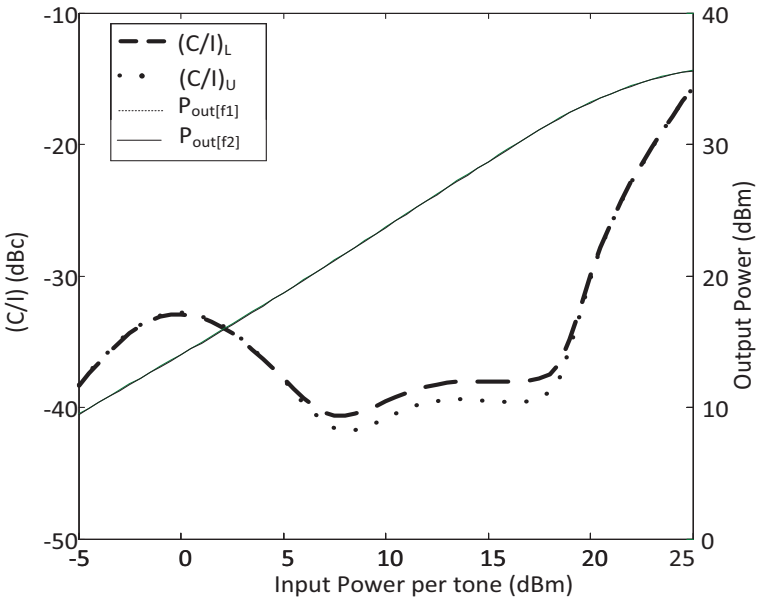

Figure 2.6: Simulated output power and C/I ratio versus input power level of one of the tones. The selected operating frequencies are f_1=2.395 GHz and f_2=2.405 GHz. The results are obtained for V_{ds}= 35 V and V_{gs}= -3.5 V.

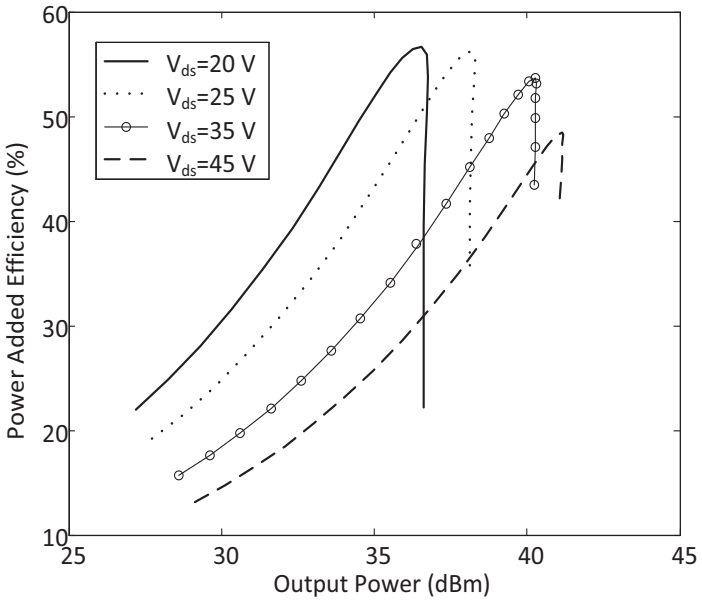

Figure 2.7: Simulated power added efficiency versus output power for V_{ds}= 20 V, V_{ds}=25 V, V_{ds}=35 V and V_{ds}=45 V. The power amplifier operates at 2.4 GHz and the selected gate voltage is -3.5 V.

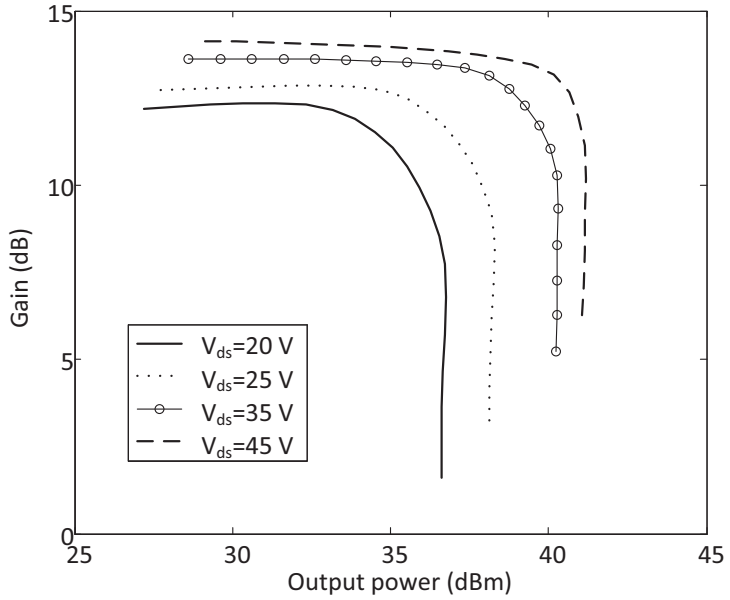

Figure 2.8: Simulated gain of the power amplifier for different drain voltages (V_{ds}= 20 V, V_{ds}=25 V, V_{ds}=35 V and V_{ds}=45 V) and output power levels. The power amplifier operates at 2.4 GHz and the selected gate voltage is -3.5 V.

It can be observed from Figure 2.7 and Figure 2.8 that different efficiency levels are achieved for various drain voltage and input power values. Thus, the proposed device could be potentially used in an ET topology in order to improve the average efficiency of the device when operating with high PAPR input signals and time-varying envelopes, such as LTE.

2.3 Implementation and Characterization of the Power Amplifier

The power amplifier is fabricated in Arlon 25N substrate with dielectric constant of 3.38, loss tangent of 0.0025 and 30 mil thickness using an LPKF Protomat C100/HF circuit board plotter [39]. A brief description of the fabrication process is given in this Section. The first step in the fabrication procedure is machining the surface of the substrate using the available tools (i.e. universal cutter and micro cutter [40]). The second stage of the process includes the drilling of the vias on the board using spiral drills [40]. Figure 2.9 shows the moving plotter milling head during the drilling

phase, where adhesive film is placed at both sides of the substrate material. Finally, the PCB has to be cut along the border lines of the board using a contour router [40] .

Conductive paste is applied at both sides of the board using a squeeze and a vacuum table that assures that the conductive paste is inserted in the vias [40], [41] (Figure 2.10). Then, the adhesive film is carefully removed from both sides of the PCB and the fabricated board is placed into a hot air oven (170 ^{o}C) in order to cure the conductive paste for around 30 minutes. After the removal of the PCB from the oven, the copper is peeled from the board manually, as Figure 2.11 shows. The final layout of the circuit (after the removal of the copper) is shown in Figure 2.12.

Then, the lumped-element (LE) components, such as capacitors and resistances, are soldered on the board. The active device is placed on the board using a conductive epoxy (Circuitworks - CW2400) [42]. In order to cure the paste, the printed circuit board (PCB) is placed in the hot air oven (80 ^{o}C) for a few minutes (around 20 minutes).

Special considerations are taken into account for the heat dissipation of the device. Initially, an aluminum board is placed at the bottom side of the PCB (using screws) in order to help in the heat dissipation during the power amplification process. Thermal paste (Figure 2.13) is also applied in between the aluminum board and the PCB in order to achieve a good contact between them by filling in the air gaps due to the surface imperfections. Figure 2.13 shows the bottom side of the PCB after applying thermal paste on it.

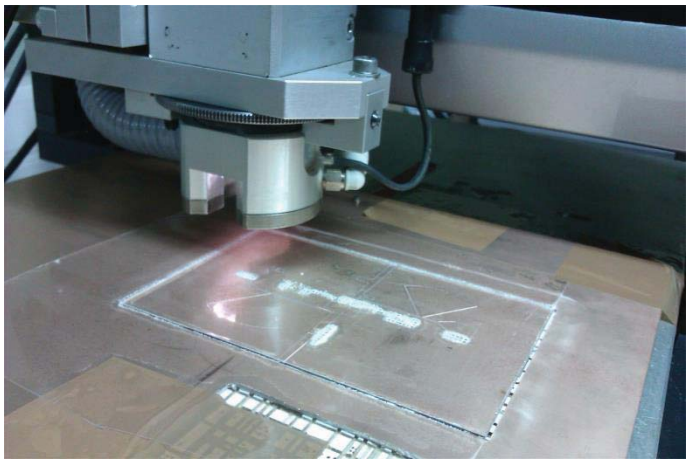

Figure 2.9: Drilling the vias of the power amplifier using an LPKF Protomat C100/HF circuit board plotter [39].

Figure 2.10: Insertion of the conductive paste through the vias of the board [40].

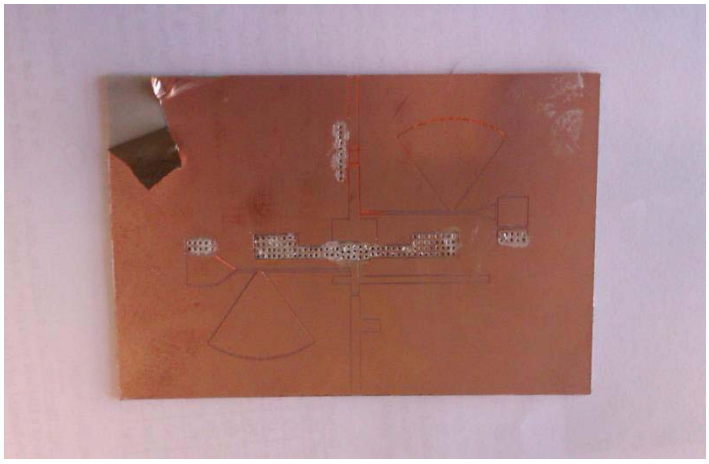

Figure 2.11: Peeling the copper of the board manually (top view of the PCB).

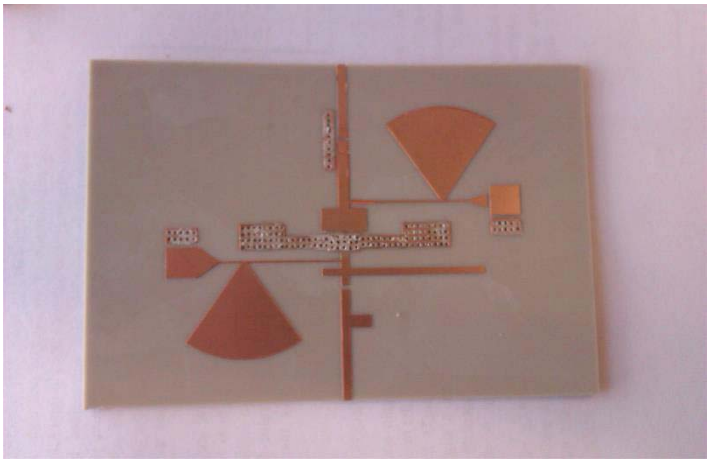

Figure 2.12: Top view of the layout of the board after the peeling phase shown in Figure 2.11.

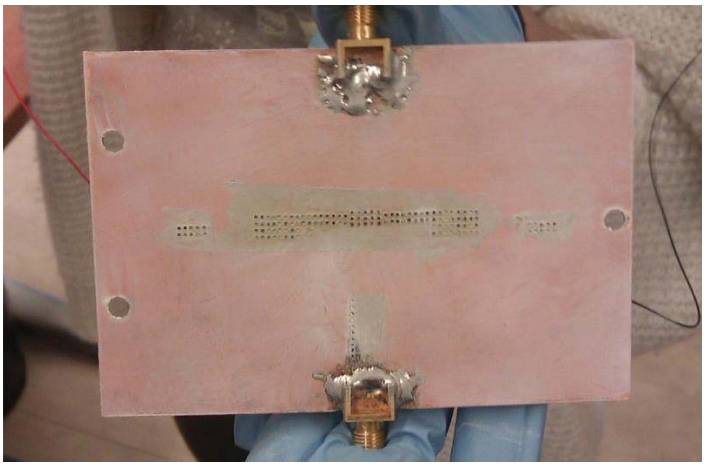

Figure 2.13: View of the bottom side of the board after applying thermal paste on it.

Finally, a heatsink is attached at the bottom side of the aluminum board in order to dissipate the heat efficiently to the environment. In this case, conductive epoxy (Circuitworks - CW2400) [42] is used between the surfaces in order to provide a good contact between them. The PCB is also placed in the hot air oven (80 ^{o}C) for around 20 minutes. The final implemented power amplifier circuit is shown in Figure 2.3b and has a total size of 6 cm x10 cm.

The power amplifier is initially characterized in its small signal regime. Figure 2.14 - Figure 2.17 show a comparison among the simulated and measured small-signal S-parameters performance over the frequency range of 0.5 GHz to 3 GHz. In Figure 2.14, a comparison between the simulated and measured reflection coefficient ($|S_{11}|$) is shown. The measured and simulated small-signal gain ($|S_{21}|$) of the device is also shown in Figure 2.15, where a slight shift to higher frequencies is observed at the frequency band of interest. Figure 2.16 and Figure 2.17 show the $|S_{22}|$ and $|S_{12}|$ parameters showing good agreement between simulation and measurements. The small discrepancies between the simulation and the measurements could be attributed to various factors, as it will be explained at the end of the Section.

The fabricated prototype is also characterized in terms of its output power (P_{out}), power gain (G), power added efficiency (η_{PAE}) and drain efficiency (η) with a single tone input signal using a signal generator (Agilent E8247C) and a spectrum analyzer (Agilent E4448A). The drain efficiency is calculated as the ratio of the output power (P_{out}) and the dissipated power (P_{dc}) [11], as

$$\eta = \frac{P_{out}}{P_{dc}} \tag{2.1}$$

where P_{dc} is the total DC power consumed at the drain (P_d) and at the gate of the device (P_g). The dissipated power at the drain is calculated as the product of the DC current (I_{ds}) at the drain of the transistor and the drain voltage (V_{ds}). In the same way, P_g is given as the product of the DC current (I_{gs}) at the gate of the transistor and the gate voltage (V_{gs}).

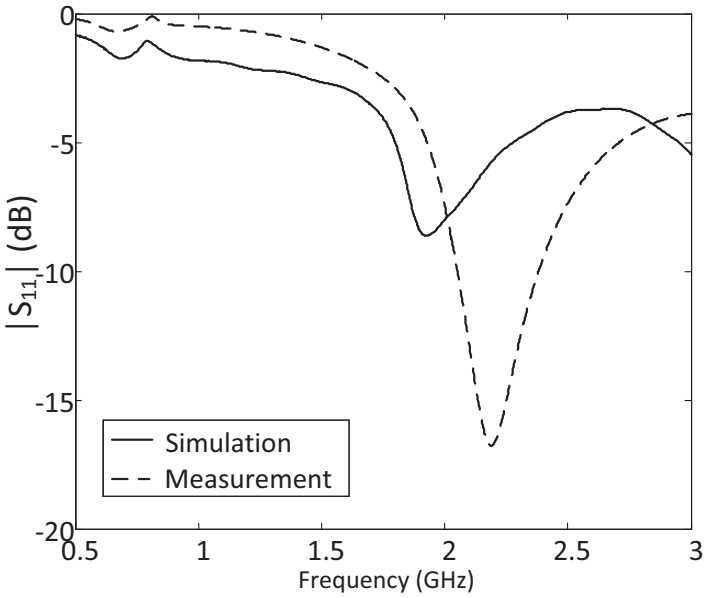

Figure 2.14: Comparison of simulated (solid line) and measured (dashed line) small-signal $|S_{11}|$ over the frequency range of 0.5 GHz to 3 GHz.

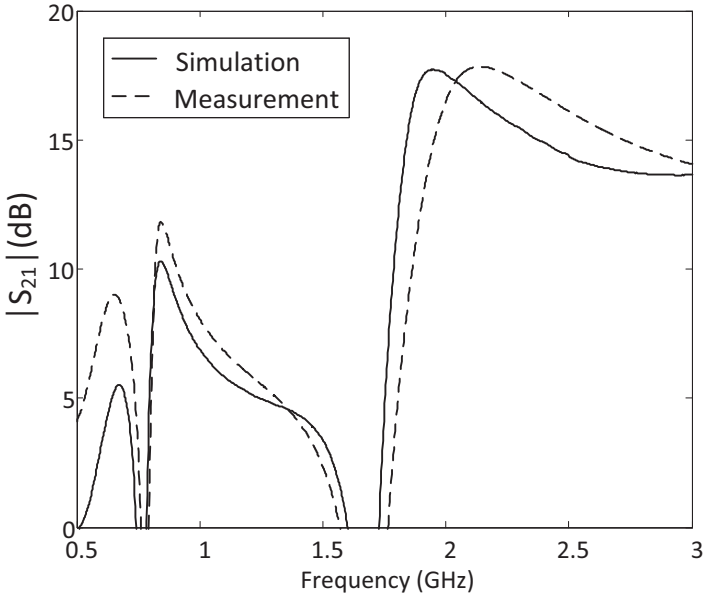

Figure 2.15: Comparison of simulated (solid line) and measured (dashed line) small-signal $|S_{21}|$ over the frequency range of 0.5 GHz to 3 GHz.

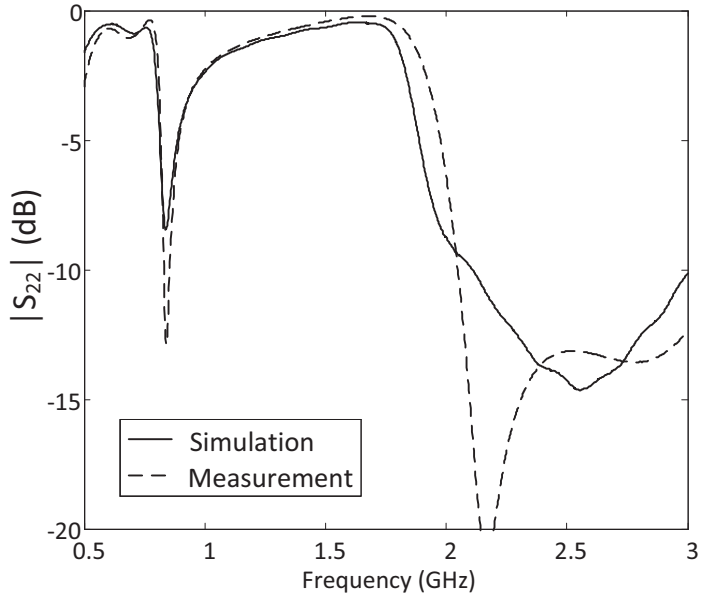

Figure 2.16: Comparison of simulated (solid line) and measured (dashed line) small-signal $|S_{22}|$ over the frequency range of 0.5 GHz to 3 GHz.

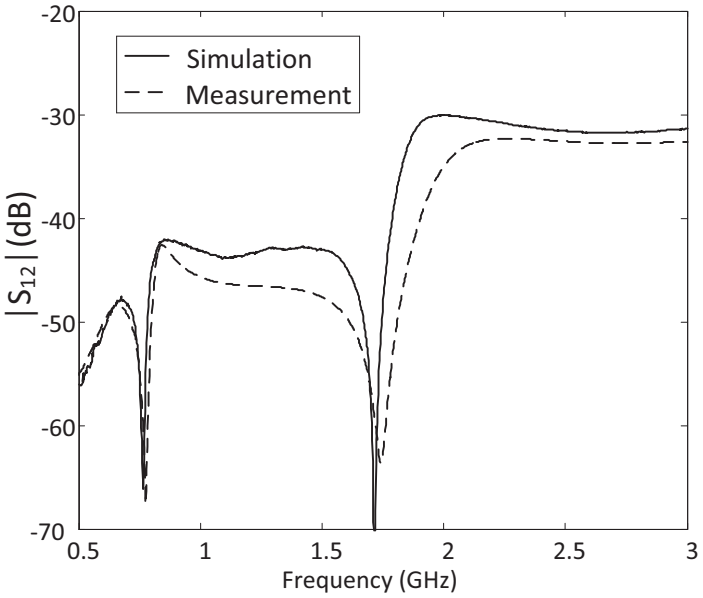

Figure 2.17: Comparison of simulated (solid line) and measured (dashed line) small-signal $|S_{12}|$ over the frequency range of 0.5 GHz to 3 GHz.

The power added efficiency [12] takes into account the RF input power (P_{in}) and is defined as

$$\eta_{PAE} = \frac{P_{out} - P_{in}}{P_{dc}} \tag{2.2}$$

Table 2.2 shows a comparison of the simulated and measured performance of the fabricated PA for an input power of 25 dBm at 2.4 GHz and 2.45 GHz. The device demonstrates a measured gain of 11.7 dB and a drain efficiency of 39 % for an input power of 25 dBm at 2.4 GHz, while a higher gain of 12.7 dB and drain efficiency of 43.3 % is obtained at 2.45 GHz.

Parameter	Simulated Performance		Measured Performance	
	2.4 GHz	2.45 GHz	2.4 GHz	2.45 GHz
P_{out}	38.1 dBm	37.9 dBm	36.7 dBm	37.7 dBm
G	13.1 dB	12.9 dB	11.7 dB	12.7 dB
η	47.2 %	45.4 %	39 %	43.3 %
η_{PAE}	44.9 %	43.1 %	37 %	41 %

Table 2.2: Measured and simulated output power, gain, drain efficiency and power added efficiency of the power amplifier for a fixed input power of 25 dBm at 2.4 GHz and 2.45 GHz. The device is biased with 35 V drain and -3.5 V gate voltage.

Discrepancies between the simulated and measured S-parameters (Figure 2.14-Figure 2.17) and the performance of the power amplifier (Table 2.2) can be attributed to the tolerance in the fabrication process (during the drilling and milling phase) of the prototype. In addition, the tolerances of the surface mounted devices (SMD), such as capacitors and inductors, and the substrate material produce inaccuracies in the simulation results. Finally, the discrepancies between the simulation and the measurements could be due to possible inaccuracies in the nonlinear model of the transistor.

2.4 Linearity Measurements

The performance of the PA in terms of linearity is evaluated with different input signals. Initially, the power amplifier is tested with a single carrier input signal and the 1 dB compression point is defined. A two-tone input signal is used in order to evaluate the linearity of the power amplifier by calculating the carrier to intermodulation (C/I) ratio. The device is also tested in a LTE environment using a LTE input signal.

2.4.1 One and Two-Tone Characterization

Initially, the performance of the PA is evaluated for different input power levels. The measured output power and gain when the input varies from 0 to 27 dBm are shown in Figure 2.18. As the input power increases, the device is driven into saturation. It is observed that the maximum linear P_{out} of the stand-alone power amplifier is 24 dBm and corresponds to an input power of 10 dBm and a gain of 14 dB at 2.4 GHz. The measured value of the 1 dB compression point (P_{1dB}) is observed for P_{in}=22 dBm.

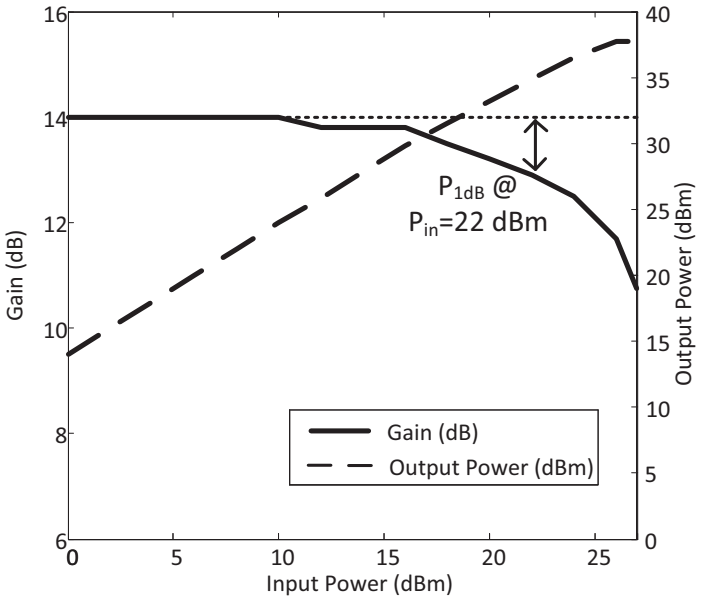

Figure 2.18: Measured output power and gain for a 2.4 GHz input signal as a function of the input power level. The measurements are for V_{ds}=35 V and V_{gs}=-3.5 V.

One of the most widely used nonlinear distortion metrics is the carrier to intermodulation ratio. The C/I is defined as the ratio between the carrier output power (P_{out}) and the intermodulation product output power ($P_{out[2f2-f1]}$ or $P_{out[2f1-f2]}$). Many factors including memory effects contribute to C/I asymmetries at the output power spectrum [36]-[38], [43], [44]. Thus, due to the asymmetry in the upper and lower bands of the intermodulation products, the C/I is defined as lower ($(C/I)_L$) and upper C/I ($(C/I)_U$), where $(C/I)_L$ and $(C/I)_U$ are calculated as

$$\left(C/I\right)_L = \frac{P_{out[f1]}}{P_{out[2f1-f2]}} \tag{2.3}$$

and

$$\left(C/I\right)_U = \frac{P_{out[f2]}}{P_{out[2f2-f1]}} \tag{2.4}$$

The C/I ratio is measured using a two-tone input signal. The two tones have equal amplitude and they are centered around 2.4 GHz. The C/I is calculated for different frequency spacings ($\Delta f=f_2 - f_1$) between the two tones (5 MHz, 10 MHz, 15 MHz, 20 MHz). Each of the tones has a power of $P_{in[f1]}=P_{in[f2]}=22$ dBm. The measurement setup is depicted in Figure 2.19.

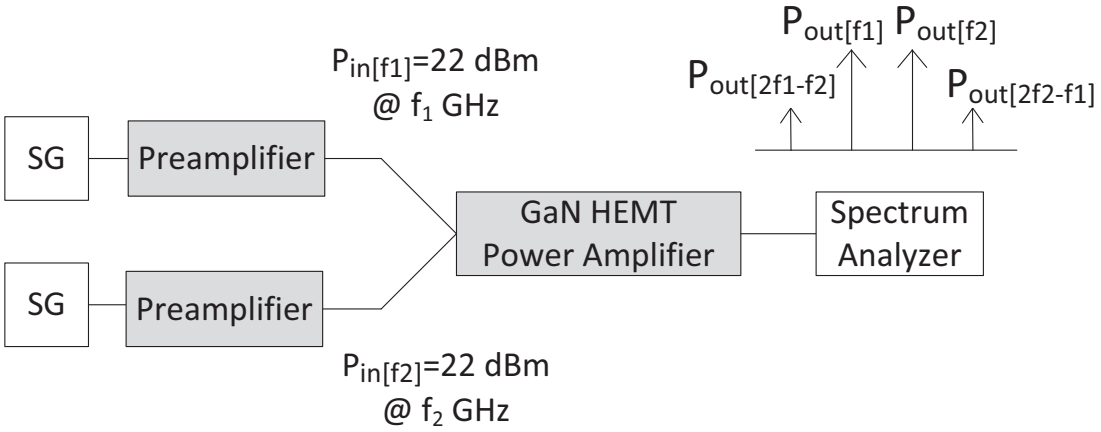

Figure 2.19: Measurement setup for a two-tone characterization of the PA. The device is tested for different frequency spacing at a center frequency of 2.4 GHz.

Two preamplifiers are used as the signal generators (SGs) are not able to give such a high output power. The preamplifiers are adjusted to provide an input signal of 22 dBm to the fabricated PA at the selected frequencies. The output spectrum of the power amplifier when excited with a two-tone 22 dBm input signal at 2.395 GHz and 2.405 GHz (Δf=10 MHz) is shown in Figure 2.20. The PA operates at the compression region and the obtained lower and upper carrier to intermodulation ratios are 24.3 dB and 24.6 dB, respectively.

$(C/I)_L$ and $(C/I)_U$ for different frequency spacing are shown in Table 2.3 demonstrating a good performance even though the device is not operating at its linear region. It is shown that for a spacing of 5 MHz the PA demonstrates a carrier to intermodulation ratio better than 25 dB.

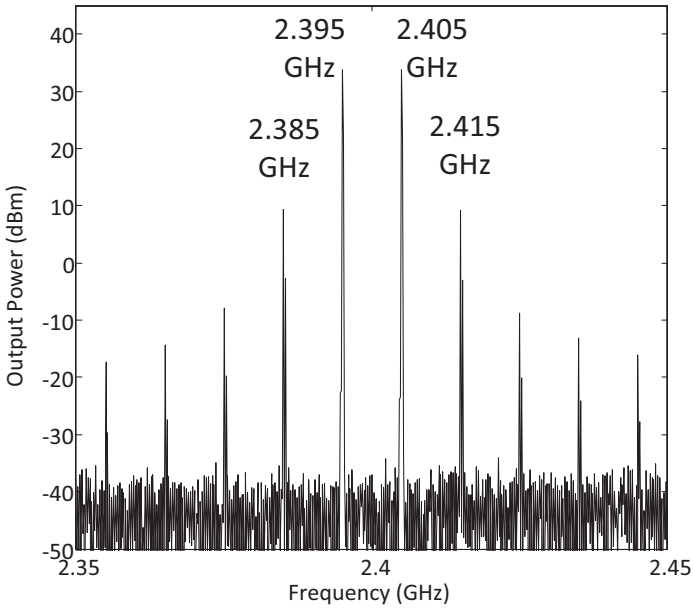

Figure 2.20: Output spectrum when the power amplifier is excited with a two-tone input signal (22 dBm each of them) of a center frequency of 2.4 GHz and spacing of 10 MHz.

Δf (MHz)	$(C/I)_L$ (dB)	$(C/I)_U$ (dB)
5	25.4	32
10	24.3	24.6
15	23.4	25.4
20	24.9	22.3

Table 2.3: Lower and upper carrier to intermodulation ratios for different frequency spacing at 2.4 GHz. The measurements are made for a two-tone input signal of 22 dBm power each.

2.4.2 LTE Environment

In this Section, the linearity of the proposed topology is also tested using a LTE input signal. LTE supports different channel bandwidths ranging from 1.4 MHz to 20 MHz (1.4 MHz, 3 MHz, 5 MHz, 10 MHz, 15 MHz and 20 MHz) to deploy more spectrum flexibility than the previous systems. The wider channel bandwidths of 10 MHz, 15 MHz and 20 MHz target to improve the system performance as users may perceive that they have a wide bandwidth connection while sharing the bandwidth with individual users [7].

The proposed PA is tested with LTE input signals with different BWs (3 MHz, 5 MHz, 10 MHz, 15 MHz and 20 MHz) in order to evaluate the performance of the device under various operating conditions. This is done because the performance of the PA and also its stability properties may vary depending on the signal bandwidths due to the nonlinear device. Additionally, the gain of the PA circuit is not flat over the whole frequency band which will results in different performances depending on the signal bandwidth.

One of the metrics that are used for the protection of the adjacent channel is the ACPR [7]. A LTE signal is used as the input signal of the device for the calculation of the ACPR. The measured complementary cumulative distribution function (CCDF) [45], [46] of the envelope of the LTE input signal for an input power of 5 dBm is measured using the Agilent Vector Signal Analyzer (VSA) software and is shown in Figure 2.21. A maximum PAPR of 9.54 dB is measured for the envelope of the LTE signal and thus the PAPR of the signal is around 12.54 dB [45].

The lower adjacent channel power ratio ($ACPR_L$) is defined as the ratio between the total output power measured in the fundamental zone around the carrier, P_{out}, and the total power in the lower adjacent-channel power (P_{out_L}) as it is shown in (2.5).

$$ACPR_L = \frac{P_{out}}{P_{out\_L}} \tag{2.5}$$

The same applies for the upper ACPR ($ACPR_U$) which is defined as the ratio of the P_{out} and the upper adjacent-channel power (P_{out_U}) according to (2.6).

$$ACPR_U = \frac{P_{out}}{P_{out\_U}} \tag{2.6}$$

The upper and lower adjacent channel power ratio for each LTE input signal is measured according to the channel bandwidth (5 MHz, 10 MHz, 15 MHz and 20 MHz) [7], as it is shown in Table 2.4. For instance, for a 5 MHz LTE input signal, P_{out} is measured in a 4.5 MHz bandwidth in the transmitted frequency channel, while P_{out_L} and P_{out_U} is measured for the same bandwidth (4.5 MHz) at a frequency offset of +5 MHz and -5 MHz, respectively.

Figure 2.22 - Figure 2.25 show the measured output spectrum of the fabricated power amplifier for an input LTE signal with total power of 5 dBm for different BWs (5 MHz, 10 MHz, 15 MHz and 20 MHz). As it can be observed from Figure 2.26, two unequal adjacent channels exist at the measured output spectrum of the PA and therefore different metrics are defined: the lower ACPR and the upper ACPR. A comprehensive explanation about the reasons that cause this asymmetry can be found in [47].

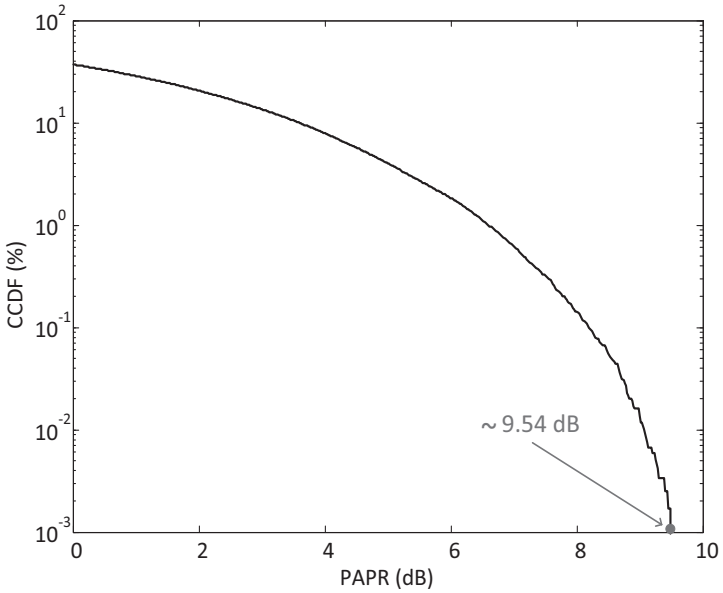

Figure 2.21: Measured complementary cumulative distribution function of the envelope of a downlink LTE 5 dBm signal (BW=10 MHz).

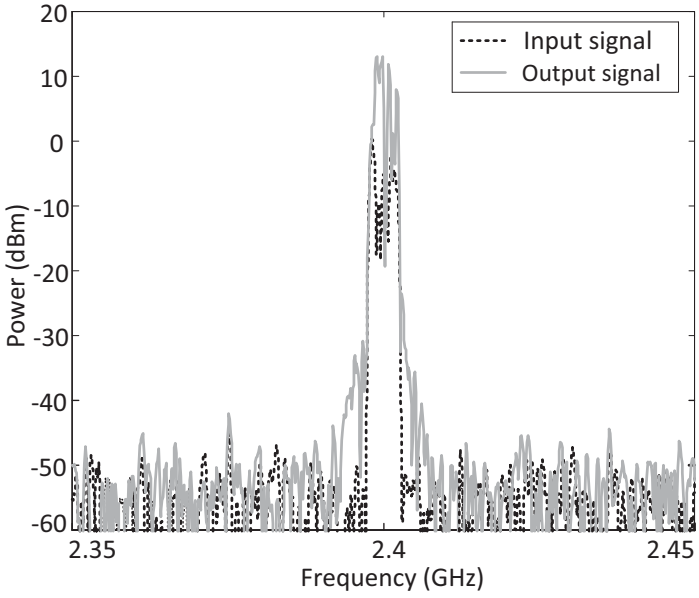

Figure 2.22: Measured output spectrum for a 5 MHz LTE 2.4 GHz input signal (5 dBm).

BW (MHz)	Measured BW (MHz)	Adjacent Channel Center Frequency Offset (MHz)
5	4.5	+5/-5
10	9	+10/-10
15	13.5	+15/-15
20	18	+20/-20

Table 2.4: Measured Bandwidth and adjacent channel center frequency offset for LTE signals with different bandwidths [7].

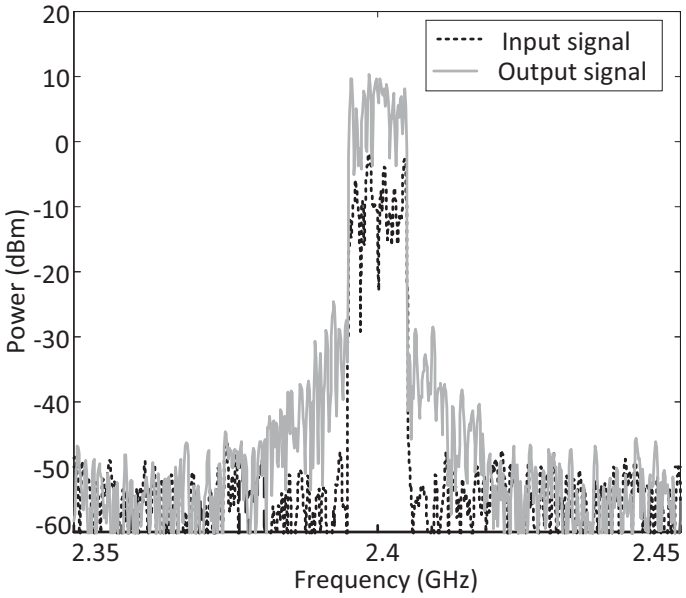

Figure 2.23: Measured output spectrum for a 10 MHz LTE 2.4 GHz input signal (5 dBm).

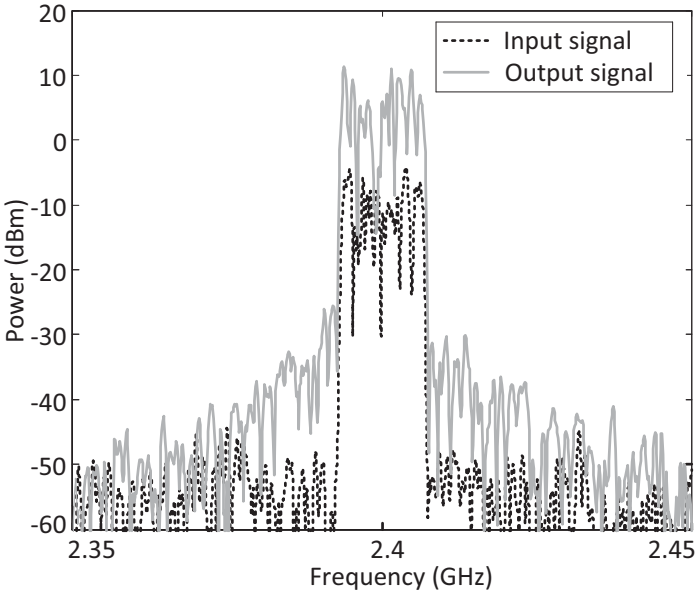

Figure 2.24: Measured output spectrum for a 15 MHz LTE 2.4 GHz input signal (5 dBm).

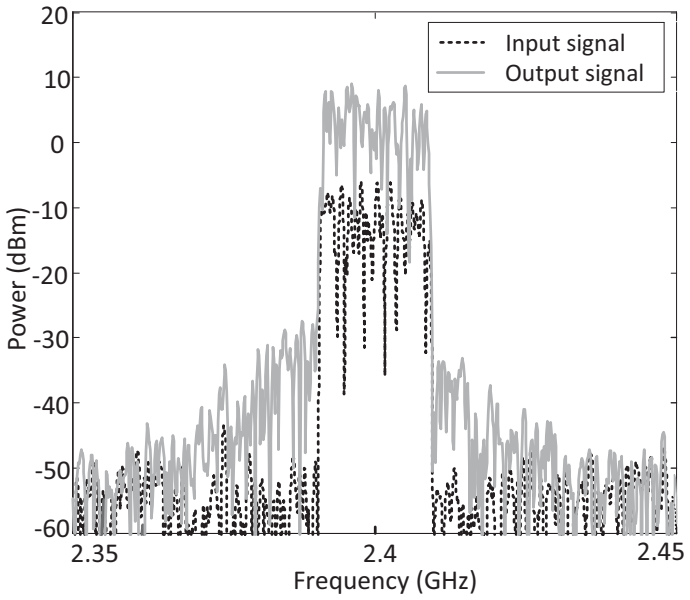

Figure 2.25: Measured output spectrum for a 20 MHz LTE 2.4 GHz input signal (5 dBm).

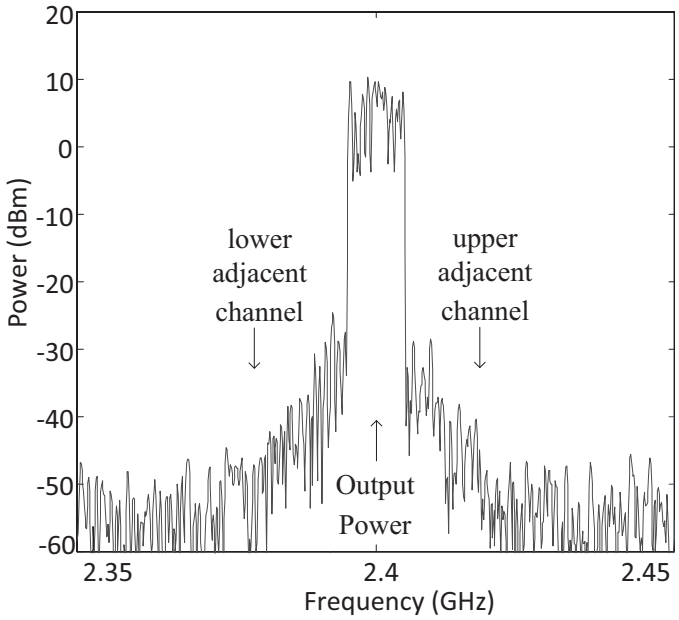

Figure 2.26: Output spectrum of the power amplifier when excited with a 2.4 GHz LTE signal. The input power level is 5 dBm and the bandwidth 10 MHz.

The nonlinear distortion of the output signal is shown in Table 2.5. It can be noted that the $ACPR_L$ and $ACPR_U$ are higher than 40 dB for an input power of 5 dBm. The PA has almost the same ACPR performance regardless of the LTE input signal bandwidth. Measurements with a higher input power level is not possible as the available instrumentation in the laboratory is not able to give a higher output power level.

BW (MHz)	$ACPR_L$ (dB)	$ACPR_U$ (dB)
5	43.2	44.2
10	40.7	43
15	41	43.75
20	40	43.4

Table 2.5: Measured adjacent channel power ratio of the power amplifier for various bandwidths (5 MHz, 10 MHz, 15 MHz and 20 MHz.

The overall performance of the PA is summarized in Table 2.6. The device exhibits a gain of 11.7 dB and a drain efficiency of 39 % for an output power of 36.7 dBm at 2.4 GHz. The carrier to intermodulation ratio is better than 24 dB for a two-tone input signal of 25 dBm of total power and a spacing of 10 MHz. Table 2.7 compares the performance of the power amplifier with previously published GaN HEMT power amplifiers operating around the same frequency band for an input power of 25 dBm, demonstrating that the proposed stand-alone linear GaN HEMT power amplifier shows comparable performance to these PAs, using a simpler topology.

Parameter	Value
V_{ds}, V_{gs}	35 V, -3.5 V
P_{out} @ P_{in}=25 dBm	36.7 dBm
G @ P_{in}=25 dBm	11.7 dB
η @ P_{in}=25 dBm	39 %
C/I @ P_{in}=25 dBm (Δf= 10 MHz)	$(C/I)_L$=24.3 dB $(C/I)_U$=24.8 dB
ACPR for a 5 dBm LTE signal (BW=10 MHz)	$ACPR_L$=40.7 dB $ACPR_U$=43 dB

Table 2.6: Summarized performance of the power amplifier at 2.4 GHz.

	f (GHz)	P_{out} (dBm)	G (dB)	η (%)	η_{PAE} (%)
[19]	2.45	34.68	12.27*	-	42.5
[48]	1. 8	34.4	9.4	-	24.19
[This Thesis]	2.4	36.7	11.7	39	37

Table 2.7: Comparison of GaN HEMT power amplifiers for P_{in}=25 dBm.

*small signal-gain

2.5 Chapter Summary

This Chapter presents the design and implementation of a stand-alone linear power amplifier at 2.4 GHz with high output power. A GaN HEMT transistor is selected for the design and implementation of the PA. The device exhibits a gain of 11.7 dB and a drain efficiency of 39 % for an output power of 36.7 dBm at 2.4 GHz (P_{in}= 25 dBm). The device achieves a carrier to intermodulation ratio as good as 25 dB for a two-tone input signal of 25 dBm of total power when it is not operating at its linear region. The fabricated power amplifier is also tested with LTE input signals with different input signal bandwidths (5 MHz to 20 MHz). The PA despite its simple design achieves high linearity close to 1 dB compression point. This design, taking advantage of the device linearity sweet spots can have successful application in ET systems.

Chapter 3

Design of Dual-Band and Broadband Power Amplifiers

3.1 Introduction

Modern wireless communication systems require transceivers that are capable of operating at multiple frequency bands simultaneously in order to allow for the implementation of multiple standards in the same equipment. In fact, broadband and multi-band operation can substantially reduce the number of circuit components needed in wireless platforms, as well as the cost and the size of the devices [49]. As PAs are critical components in most communication systems, their design can actually benefit from a multi-band or broadband approach. Nonetheless, such devices are difficult to design, as the input and output matching networks need to be optimized for operation in a wider frequency range or in multiple frequency bands.

So far, many efforts have been made to realize impedance matching networks operating in multiple frequency bands, including lumped-element (LE) networks and transmission line (TL) implementations [50]-[52]. A 1.81 GHz/2.65 GHz PA based on multiharmonic load transformation network is described in [52]. In [53], the design and implementation of a dual-band PA with two frequency matching

networks based on the low-pass Chebyshev form impedance transformer design is presented. The design of a dual-band (1.9 GHz/ 3.5 GHz) PA circuit based on π-topology matching network is also discussed in [54].

Among the efforts for dual-band operation stands the implementation of PA circuits based on the newly introduced concept of Metamaterial (MTM) structures [55]-[60]. The term MTM refers to artificial effectively homogeneous electromagnetic structures with unusual properties that are not readily available in nature [56]. The properties of the metamamaterial transmission lines have found successful application to the design of a plethora of devices, from antennas [61]-[64] to microwave sensors [65]. The first topology considered in this Chapter is a dual-band power amplifier inspired from the MTM concept and based on Composite Right/Left-Handed (CRLH) TL unit cells for both the input and output matching networks.

Starting from the realization of multi-band impedance matching networks using CRLH unit cells for the development of multi-band PAs, the implementation of such PA topologies in Substrate Integrated Waveguide (SIW) technology is also considered in this Chapter. In particular, in this Chapter, two power amplifier topologies are proposed, along with the design techniques used for every approach. Initially, the concept of using CRLH unit cells for the design of multi-band PAs is addressed and verified by means of a single-substrate prototype [66]. Then, starting from this result, the development of a broadband power amplifier topology based on SIW technology is also investigated [67].

This Chapter is organized as follows. In Section 3.2 the properties of CRLH unit cells are discussed and applied to the implementation of a dual-band PA operating at ISM band and 3.35 GHz WiMAX band. Initially, two design approaches for the implementation of the matching networks are considered and simulated in Section 3.2.1. Harmonic Balance simulation along with optimization goals are used for the design of the PA, as it is described in Section 3.2.2. Finally, the experimental characterization of the fabricated device is presented in Section 3.2.3, where a dual-band frequency response is demonstrated.

After obtaining the multi-band frequency response of the CRLH unit cells, an additional study related to the implementation of CRLH unit cells in Half-Mode SIW (HMSIW) technology is carried out. In Section 3.3, a broadband PA operating

from 2.3 GHz to 3.5 GHz based on CRLH Half-Mode Substrate Integrated Waveguide technology is presented. Section 3.3.1 describes the preliminary design phase, where the PA is designed and optimized using the equivalent circuit model of the CRLH unit cells.

Then, based on the resulting requirements for the matching networks response, input and output CRLH HMSIW are dimensioned, following an approach that combines full-wave finite element method (FEM)-based simulation with nonlinear HB analysis (Section 3.3.2). Section 3.3.3 presents the experimental results from the single-substrate prototype, demonstrating broadband operation. Finally, Section 3.4 discusses the obtained results.

3.2 A Dual-Band Power Amplifier Based on Metamaterial-Inspired Matching Networks

3.2.1 Design of Dual-Band Matching Networks

The design of a power amplifier circuit implies the design of two matching networks as it is shown in the simplified power amplifier topology of Figure 3.1. The input matching network matches the signal source to the gate of the device, while the output matching network offers an impedance matching from the drain/collector of the transistor to the 50 Ω output load.

The selection of the matching networks depends on the system specifications and the operating frequency or frequencies. A variety of matching network topologies can be applied when operating at a single frequency. The simplest structures for an impedance transformation network are the L-type and π-type networks [1]. Their implementation varies according to the device specifications and the available technology. Implementations with commercial lumped-element topologies or transmission line have been presented in the literature [1].

The design of dual-band matching networks is a more complex task as the same behavior should be met at an arbitrary set of frequencies. Among the efforts for multi-band operation stands the implementation of dual-band power amplifier topologies based on the MTM concept.

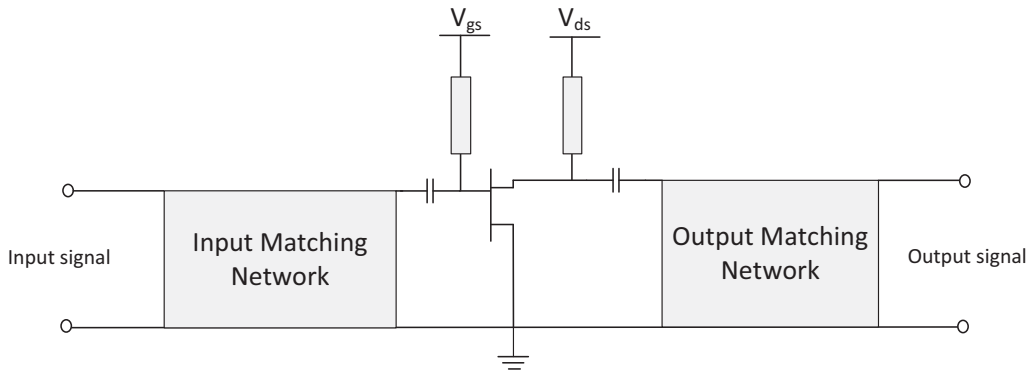

Figure 3.1: Simplified PA circuit topology that consists of the input and output impedance matching networks, two DC blocking capacitors and the bias of the transistor.

In this Chapter, a dual-band PA is proposed based on the CRLH MTM TL unit cells. In particular, a single CRLH TL unit cell is used for both the input and output matching networks. A CRLH MTM TL unit cell is the combination of a right-handed (Figure 3.2a) and a left-handed (Figure 3.2b) TL unit cell, and is shown in Figure 3.2c [1][56]. Additional CRLH TL unit cells (N) can be put in series according to the application scenario and the available technology. The total phase shift (φ) depends on the number of cells along a CRLH TL and is given by:

$$\varphi = N\Delta\varphi \tag{3.1}$$

where N is the number of unit cells and Δφ is the phase shift for each unit cell.

A CRLH TL unit cell shows a left-handed (LH) response at the low operating frequency as C_R and L_R tend to be open and short at f_1 [56]. Likewise, the CRLH TL unit cell shows right-handed (RH) behavior at the high frequency f_2 as C_L and L_L tend to be short and open at f_2. A CRLH transmission line can be implemented with asymmetric or symmetric unit cells. The asymmetric structure of a CRLH TL (Figure 3.2c) has unequal input and output impedance. On the other hand, the symmetric CRLH TL unit cell (Figure 3.2d) is characterized with equal input and output impedance.

A dual-band PA is designed based on the ATF-50189 E-pHEMT transistor from Avago (operating frequency from 400 MHz to 3.9 GHz) [68]. The performance of the power amplifier using one and two unit cells at the input and output matching networks of topology is investigated in simulation. Figure 3.3 shows the simulated $|S_{11}|$ for both topologies (with a single and two unit cells at the

impedance matching networks) showing a similar behavior at the frequencies of interest.

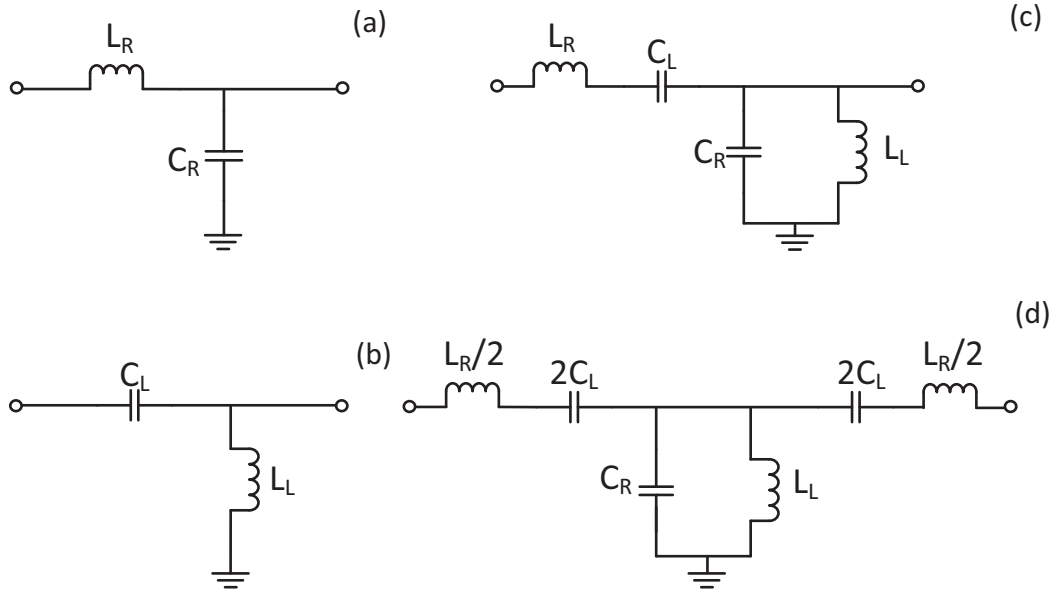

Figure 3.2: Equivalent circuit model of: a) ideal lumped-element RH TL unit cell, b) ideal lumped-element LH TL unit cell, c) ideal asymmetric lumped-element CRLH TL unit cell (T-shaped topology) and d) ideal symmetric lumped-element CRLH TL unit cell (T-shaped topology).

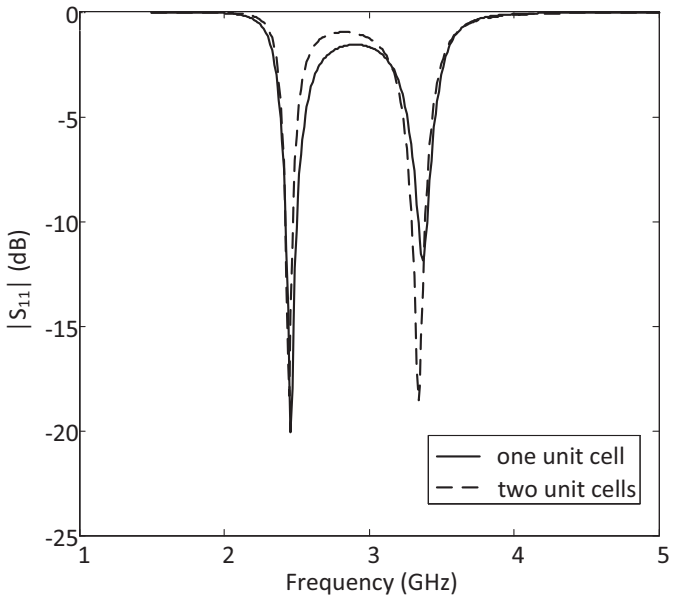

Figure 3.3: Simulated $|S_{11}|$ versus operating frequency for two different impedance matching networks.

In Figure 3.4 and Figure 3.5 the drain efficiency and the gain of the structures is shown, respectively, where a good compromise between the efficiency and the gain is achieved for both topologies. Thus, the simulated results demonstrate that the use of a single cell can lead to a good performance, while additionally it

minimizes the size and number of components used in the PA. As a result the PA with N=1 is selected for the implementation of the input and output impedance networks.

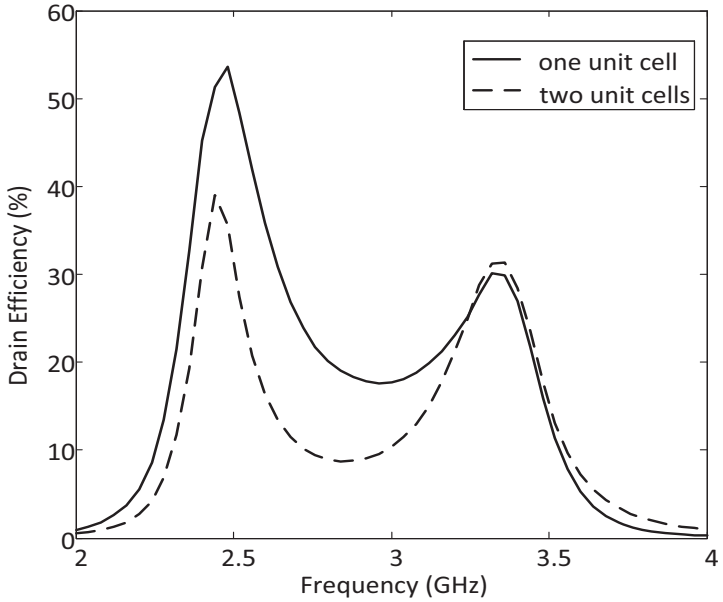

Figure 3.4: Simulated drain efficiency versus operating frequency (P_{in}=19 dBm) for two different impedance matching networks.

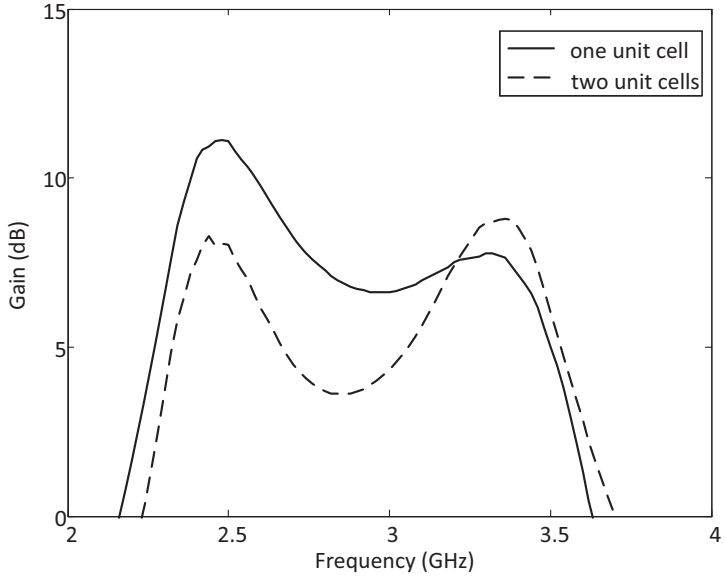

Figure 3.5: Simulated gain versus operating frequency (P_{in}=19 dBm) for two different impedance matching networks.

3.2.2 Design of the Dual-Band Power Amplifier

The design of the PA starts with the selection of the active device and the system specifications. The selected transistor is an enhancement mode pseudomorphic HEMT (E-pHEMT) transistor (ATF-50189) from Avago [68], as it has already been mentioned. Harmonic Balance analysis in combination with nonlinear optimization procedure is used to obtain an efficient and stable operation at the selected frequencies (2.4 GHz and 3.35 GHz). Optimization goals are carefully selected to match the system requirements as far as the output power and the efficiency of the system (Figure 3.6). In particular, the simulation setup includes the following optimization goals for the output power and the drain efficiency of the topology:

$$P_{out[f1]} > P_{min} \text{ and } \eta_{[f1]} > \eta_{min} \text{ at } f_1 = 2.4 \text{ GHz} \quad (3.2)$$

and

$$P_{out[f2]} > P_{min} \text{ and } \eta_{[f2]} > \eta_{min} \text{ at } f_2 = 3.35 \text{ GHz} \quad (3.3)$$

where $P_{out[f1]}$ and $\eta_{[f1]}$ is the output power and the drain efficiency at the low operating frequency ($f_1 = 2.4$ GHz), respectively. $P_{out[f2]}$ and $\eta_{[f2]}$ is the output power and the drain efficiency at the high operating frequency ($f_2 = 3.35$ GHz), respectively.

In Figure 3.6, the simplified schematic of the simulation setup is demonstrated. Two identical circuit schematics are placed in the simulation setup, each of them using a HB analysis at a different operating frequency. Thus, the simulator optimizes the values of the lumped-components, such as inductors and capacitors, to be able to operate simultaneously in the two frequencies. The lumped-element component values are optimized to fulfill these goals when the device operates with an input power level of 19 dBm. Small-signal S-parameters and LSSP analysis is also used to ensure the impedance matching of the circuit at the selected frequencies.

The simulation data from the S-parameter analysis are also used for a stability analysis of the topology. In particular, the design is optimized in order to meet the necessary and sufficient conditions for unconditional stability $B > 0$ and $K > 1$ [4], [69]. The simulation result shows that by placing a series resistance of 22 Ω at the gate of the transistor, the PA exhibits a stable operation for all the expected operating conditions. The final circuit schematic and the component values is shown in Figure 3.7a and Table 3.1, respectively.

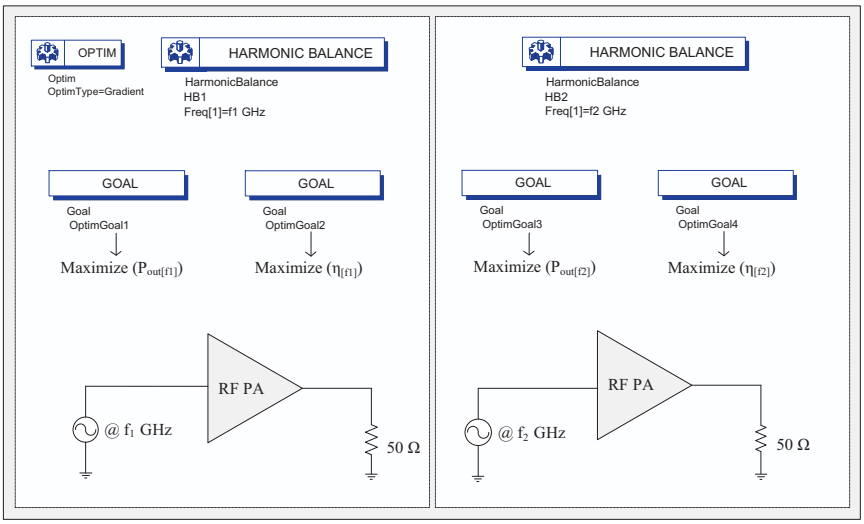

Figure 3.6: Simplified schematic of the optimization process that results in dual-band frequency response, using HB analysis in Agilent ADS software.

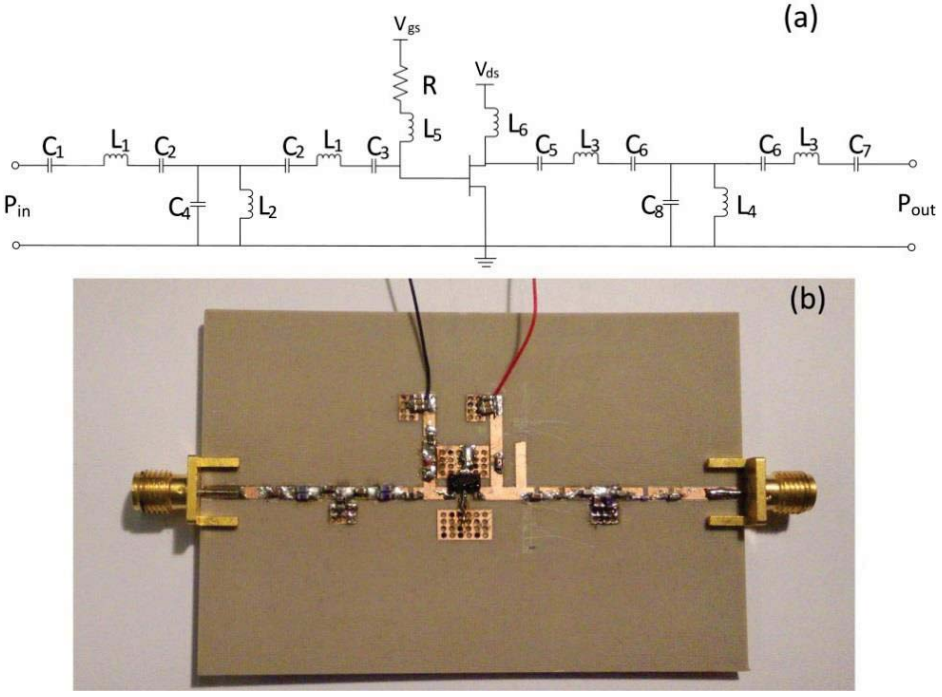

Figure 3.7: Dual-band power amplifier: a) Schematic of the circuit topology and b) fabricated prototype. The fabricated prototype has a total size of 7 cm by 5 cm. The active device is an enhancement mode pseudomorphic HEMT (E-pHEMT) transistor (ATF-50189) from Avago.

Commercial capacitors from Murata and AVX and inductors from Coilcraft are used for both the simulation and the implementation of the current design. The PA is fabricated in Arlon 25N substrate with dielectric constant of 3.38, loss tangent of 0.0025 and thickness of 30 mil utilizing a LPKF Protomat C100/HF circuit board plotter [39]. A photo of the implemented prototype is shown in Figure 3.7b. The fabricated prototype has a total size of 7 cm x 5 cm.

Component	Value	Component	Value	Component	Value
C_1	1.8 pF	C_6	12 pF	L_2	1 nH
C_2	3.9 pF	C_7	10 pF	L_3	1 nH
C_3	0.45 pF	C_8	1 pF	L_4	1.8 nH
C_4	0.25 pF	R	22 Ω	L_5	16 nH
C_5	5.6 pF	L_1	0.9 nH	L_6	100 nH

Table 3.1: Dual-band power amplifier (Figure 3.7a) circuit component values.

3.2.3 Experimental Results

Initially, the S-parameters of the PA are measured using a signal with an input power of 0 dBm. The $|S_{11}|$ and $|S_{22}|$ parameters are shown in Figure 3.8 showing a good impedance matching at the two operating frequencies (2.4 GHz and 3.35 GHz).

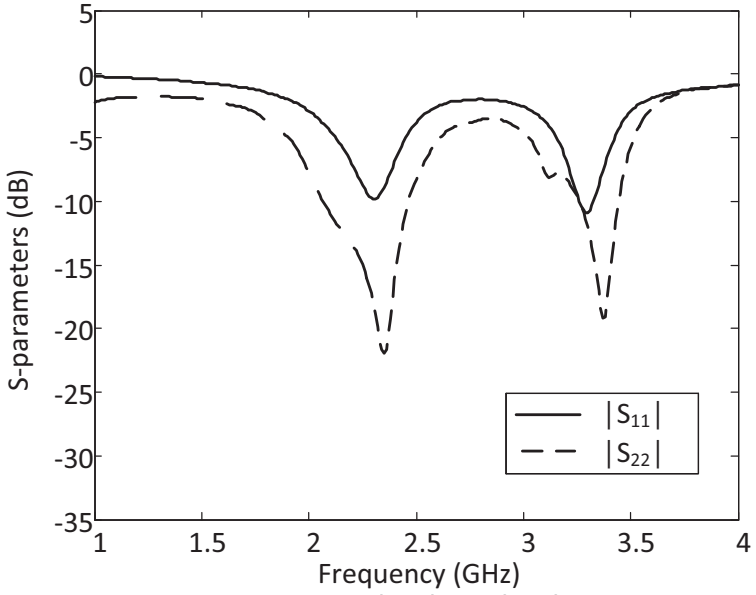

Figure 3.8: Measured small-signal S-parameters ($|S_{11}|$ and $|S_{22}|$) versus operating frequency for an input power of 0 dBm (V_{ds}=4.5 V and V_{gs}=0.54 V).

The $|S_{21}|$ and $|S_{12}|$ parameters are also shown in Figure 3.9, where it can be observed that the circuit exhibits a small-signal gain of 11 dB and 7.8 dB at 2.4 GHz and 3.35 GHz (P_{in}=0 dBm), respectively. The small-signal gain of the circuit is tested for different gate voltages as Figure 3.10 shows. From Figure 3.10, it can be seen that the device reaches a maximum value of gain for V_{gs}=0.54 V and thus, the characterization of the circuit will be carried out for V_{gs}=0.54 V.

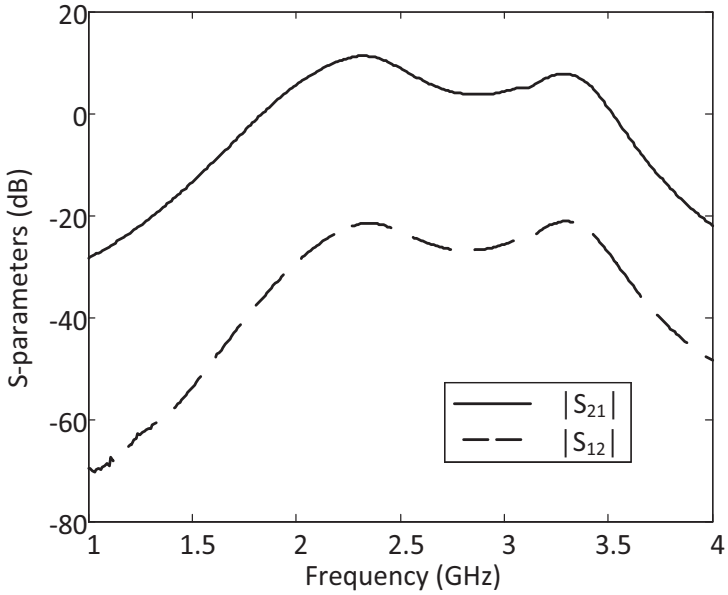

Figure 3.9: Measured small-signal S-parameters ($|S_{21}|$ and $|S_{12}|$) versus operating frequency for an input power of 0 dBm (Vds=4.5 V and Vgs=0.54 V).

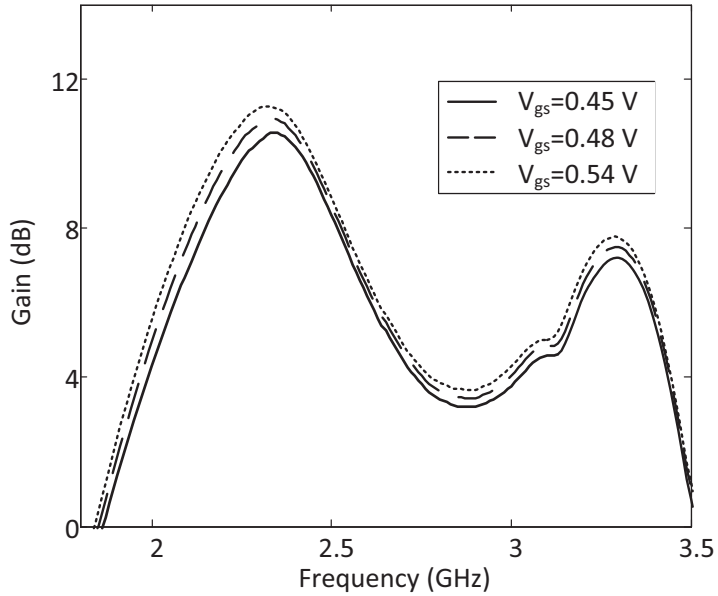

Figure 3.10: Measured $|S_{21}|$ versus operating frequency for different gate voltages (V_{gs}= 0.45V, V_{gs}= 0.48V and V_{gs}= 0. 54V). The measurements are for input power P_{in}=0 dBm and V_{ds}= 4.5 V.

Then, the circuit is characterized for a fixed input power level of 19 dBm versus operating frequency. The measured output power and drain efficiency are

shown in Figure 3.11 and Figure 3.12, respectively. A measured efficiency of 58 % and 38 % is obtained at 2.4 GHz and 3.35 GHz, respectively, as it can be seen from Figure 3.11. Additionally, Figure 3.13 shows the measured gain of the circuit versus frequency.

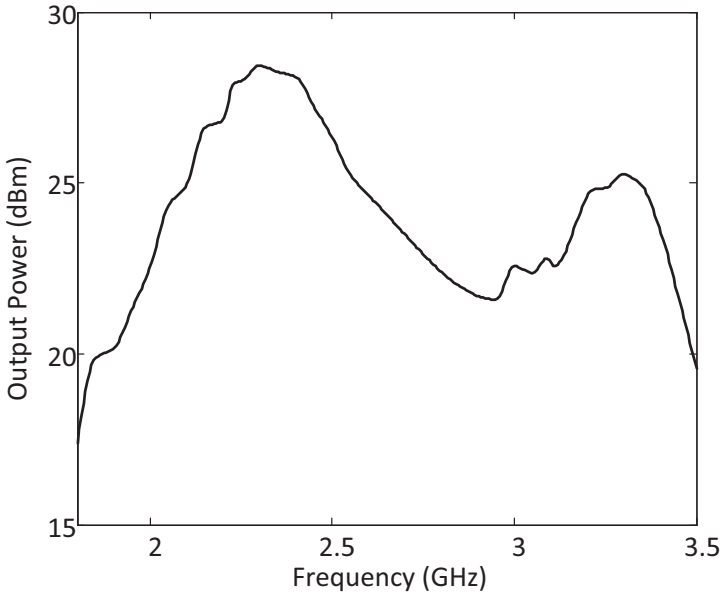

Figure 3.11: Measured output power level versus operating frequency for an input power of 19 dBm. The measurements are for V_{ds}= 4.5 V and V_{gs}=0.54 V.

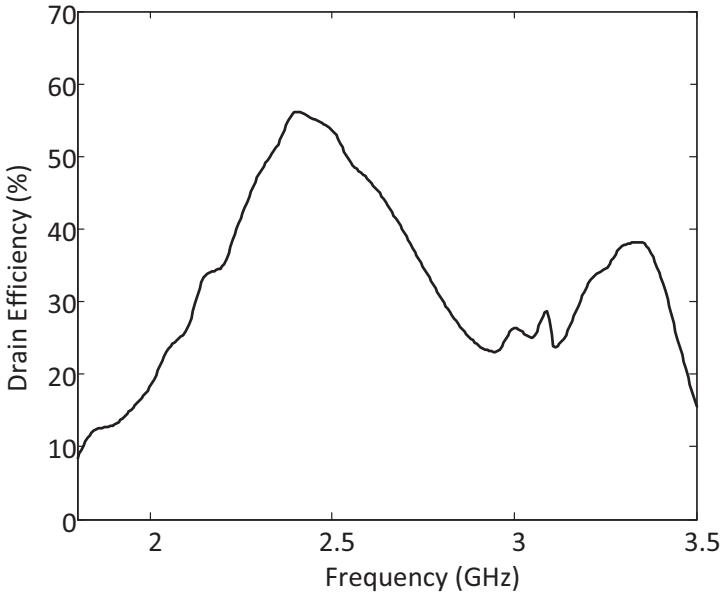

Figure 3.12: Measured drain efficiency versus operating frequency for an input power of 19 dBm (V_{ds}=4.5 V and V_{gs}=0.54 V).

The circuit is also tested versus input power level at the two operating frequencies. Figure 3.14 shows the measured drain efficiency of the device when the input power level varies from 0 to 24 dBm. A maximum drain efficiency of 65

% and 52 % is achieved for an output level of 28.7 dBm and 27.5 dBm at 2.4 GHz and 3.35 GHz, respectively. Finally, Figure 3.15 shows the measured gain of the circuit versus input power.

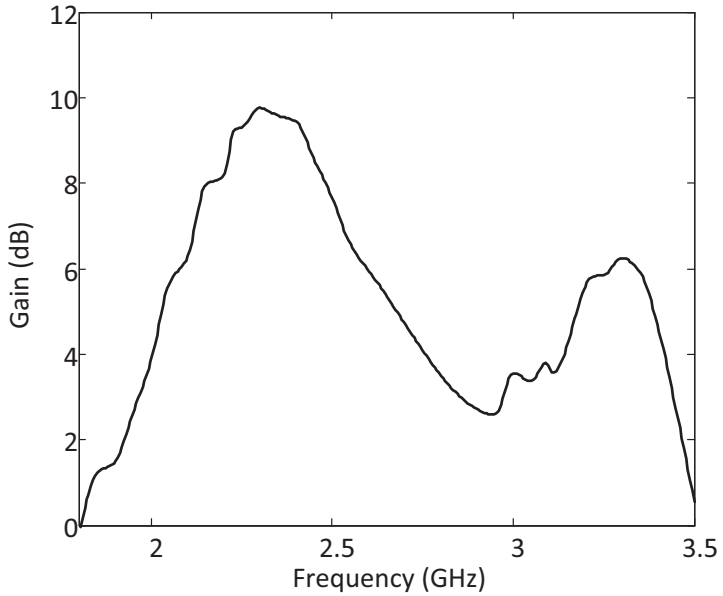

Figure 3.13: Measured gain versus operating frequency for an input power of 19 dBm (V_{ds}=4.5 V and V_{gs}=0.54 V).

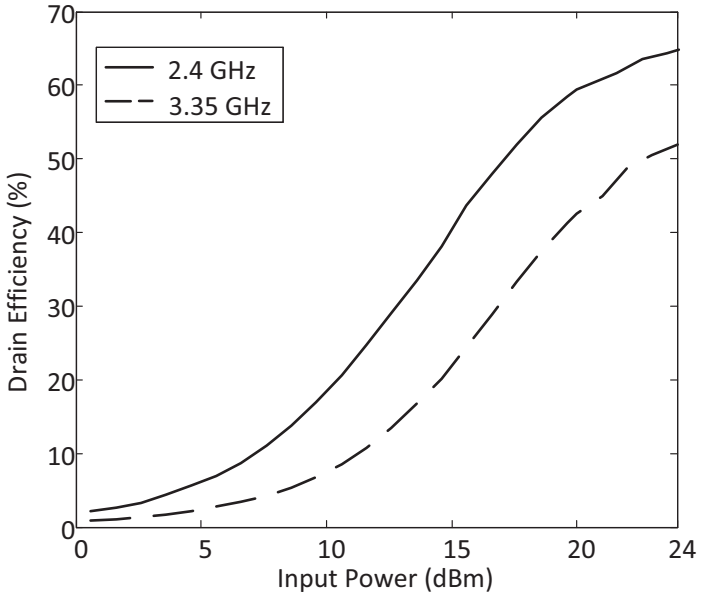

Figure 3.14: Measured drain efficiency versus input power level for the two operating frequencies (2.4 GHz and 3.35 GHz). The measurements are for V_{ds}= 4.5 V and V_{gs}=0.54 V.

As it can be observed from the measured value of the gain, the 1 dB compression point of the PA is observed for P_{in}=18 dBm and P_{in}=20 dBm at 2.4 GHz and 3.35 GHz, respectively. Thus, the PA approaches the P_{1dB} at a higher input power level (P_{in}=20 dBm) at 3.35 GHz, if compared with its operation at 2.4

GHz where the 1 dB compression point is measured for P_{in}=18 dBm. The improved linearity at 3.35 GHz comes in the tradeoff the reduced efficiency and gain, as it is shown in Figure 3.14 and Figure 3.15.

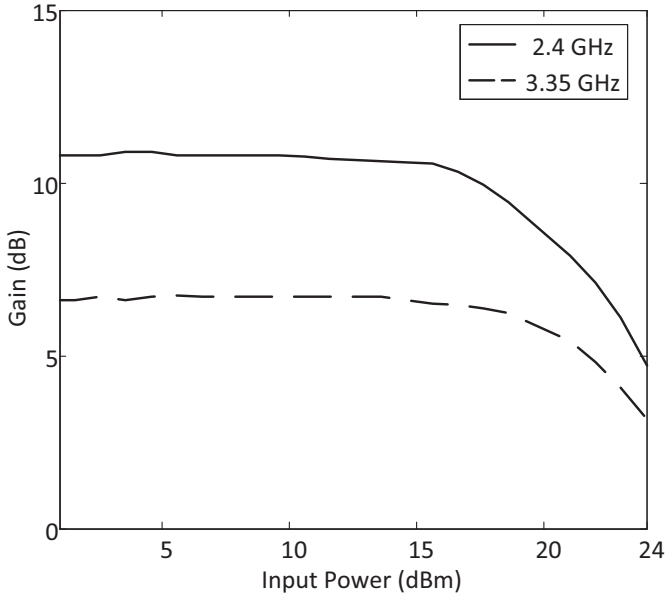

Figure 3.15: Measured gain versus input power level for the two operating frequencies (2.4 GHz and 3.35 GHz). The measurements are for V_{ds}= 4.5 V and V_{gs}=0.54 V.

A comparison of the measured performance of the power amplifier with a selection of the State-of-the-Art (SoA) dual-band power amplifiers in the literature is shown in Table 3.2, where it can be observed that the proposed approach can be successfully applied for the design of efficient dual-band PAs operating at an arbitrary set of frequencies. The proposed design shows a good performance at the two operating frequencies (2.4 GHz and 3.35 GHz) and can reduce the number of components used in wireless platforms.

Ref.	f_1/f_2 (GHz)	Peak Efficiency (%)	P_{out} (dBm)
[70]	2.45/ 3.3	(η) 53/ 46	33/ 32.5
[71]	1.96 /3.5	(η) 59.8/ 55.1	40/ 40
[72]	0.8/1.7	(η_{PAE}) 42.5/ 42.6	22.4/ 22.2
[73]	2.5/3.5	(η_{PAE}) 45/ 34	22/ 20.8
[74]	0.433/0.915	(η_{PAE}) 44/ 44/8	29/ 29.8
[This Thesis]	2.4/3.35	(η) 65/ 52 (P_{in}=24dBm) (η_{PAE}) 50/ 34 (P_{in}= 22dBm)	28.7/ 27.5 29.1/ 27.23

Table 3.2: Comparison of the measured performance of the power amplifier with other reported dual-band power amplifiers in the literature.

3.3 A Broadband Power Amplifier Based on Metamaterial-Inspired Half-Mode SIW Technology

3.3.1 Preliminary Nonlinear Analysis of the Power Amplifier

SIW technology is as a very promising design technique for the realization of compact wireless communication systems. Starting from the obtained results of Section 3.2, this Section investigates the implementation of CRLH unit cells in SIW technology. In particular, a broadband power amplifier is designed based on CRLH unit cells implemented in Half-Mode SIW technology.

The applications of SIW technology are of great interest nowadays, and a variety of passive and active components have already been proposed in the literature [75]-[79]. SIW technology allows for the integration of traditional rectangular waveguides within a single-substrate configuration and combines the low losses and high isolation of a bulky metallic waveguide with a compact shape and reduced fabrication cost [75]. SIW structures can be designed with two rows of conductive cylinders or slots embedded in a dielectric substrate [75], as it is shown in Figure 3.16.

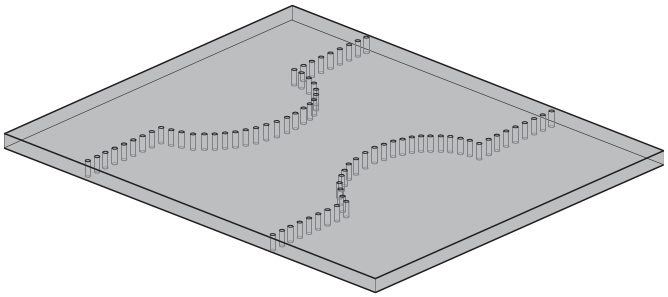

Figure 3.16: SIW topology. It consists of two rows of conductive cylinders or slots embedded in a dielectric substrate.

In order to reduce the size of SIW technology, the Half-Mode SIW topology (Figure 3.17) has been proposed [67], [75]. HMSIW technology shows similar propagation characteristics to conventional SIW, but allows for a dramatic decrease in the area occupied by the circuit [75]. In fact, both the waveguide width and the metallic surface area are reduced by nearly half.

The implementation of CRLH unit cells in SIW technology arises from the equivalence between the structure of the CRLH unit cell and the SIW

characteristics. Figure 3.18 shows the equivalent circuit model of a lumped-element CRLH unit cell (π-shaped topology) [67], [79]. A CRLH transmission line can be modeled by means of a π-shaped equivalent circuit because of the intrinsic shunt inductance, shunt capacitance and series inductance of the structure. The series capacitance of the CRLH unit cell topology can be added to the circuit by etching interdigital meander slots on the top metal surface of the waveguide. Figure 3.19a shows the schematic of a meander slot that acts like a series capacitor and Figure 3.19b – Figure 3.19d show three different implementations.

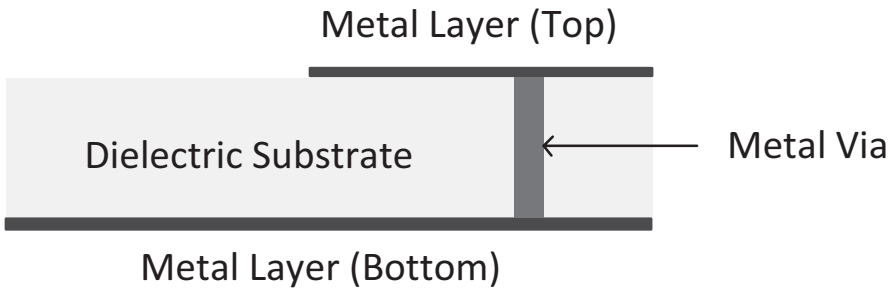

Figure 3.17: Half-Mode SIW topology.

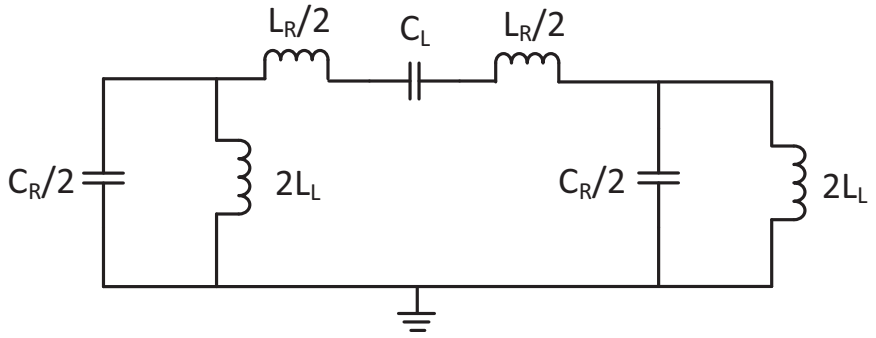

Figure 3.18: Equivalent circuit model of ideal symmetric lumped-element CRLH unit cell (π-shaped topology).

In Figure 3.20a, the schematic of the selected PA topology based on CRLH TL unit cells is shown. In the current design, three unit cells (N=3) are selected for both the input and output matching networks. In this design, the separation between f_1 and f_2 is chosen in such a way to obtain a broadband design. The analysis of the topology of Figure 3.20a is carried out by means of nonlinear HB simulation using Agilent ADS software. In this implementation, wideband operation from f_1=2.3 GHz to f_2=3.5 GHz is addressed. In order to accomplish this specification, the unit cells are designed for improved performance at the boundaries of the frequency band.

Two DC-blocking capacitors are placed in the input and output matching network. Stability considerations have also been taken into account in the design phase in order to eliminate oscillation problems. In particular, the simulation has shown that a resistance should be placed at the gate biasing path in order to make the device unconditionally stable. The values of the circuit components used in the design are listed in Table 3.3.

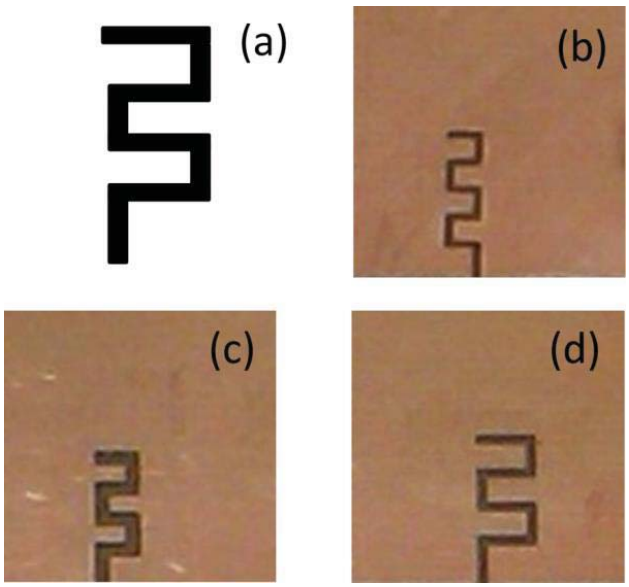

Figure 3.19: a) Schematic of meander slot and b), c), d) implementation of meanders with different dimensions.

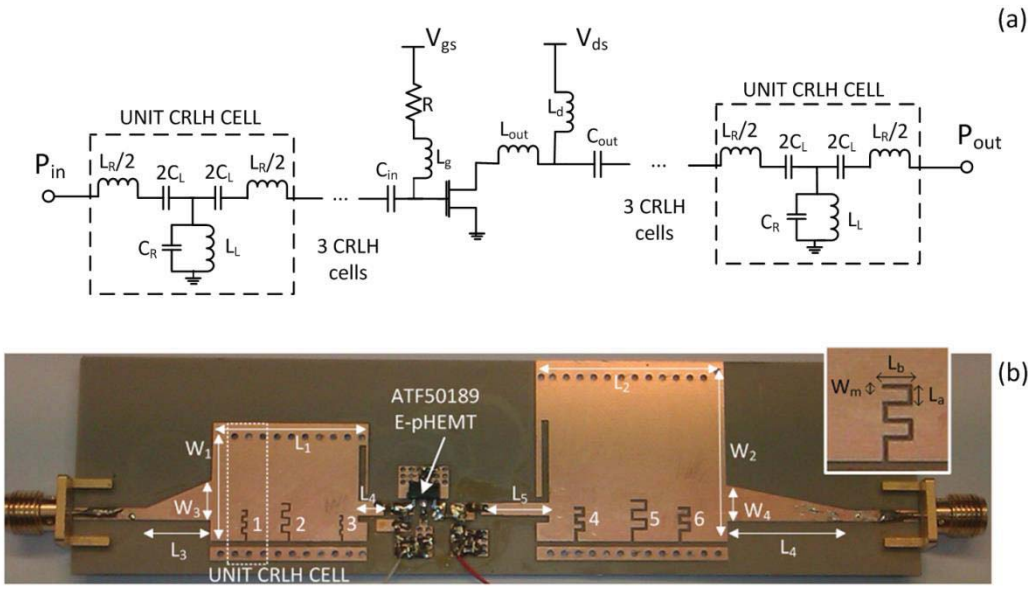

Figure 3.20: Broadband power amplifier: a) Schematic of the simulated PA topology and b) fabricated prototype based on HMSIW CRLH waveguide. The overall size of the prototype is 3 cm by 12 cm.

Component	Value	Component	Value
C_{in}	0.5 pF	L_d	100 nH
C_{out}	0.5 pF	L_{out}	1 nH
R	560 Ω	L_g	100 nH

Table 3.3: Power amplifier (Figure 3.20a) component values.

3.3.2 HMSIW Sections and Power Amplifier Design

As it is described in [67], [79], the unit cell of Figure 3.20a can be implemented by means of a HMSIW waveguide. In particular, the CRLH behavior can be obtained by etching interdigital meander slots on the top metal surface of the waveguide. By comparing Figure 3.20a and Figure 3.20b, one can see how the circuital model of the unit CRLH cell can be implemented in such a waveguide topology.

Figure 3.20b shows the implemented PA based on HMSIW input and output matching networks. The device is fabricated in Arlon 25N substrate with dielectric constant of 3.38, loss tangent of 0.0025 and thickness of 30 mil utilizing the LPKF Protomat C100/HF circuit board plotter [39]. The active device is also the ATF-50189 E-pHEMT device from Avago Technologies with an operating frequency range from 400 MHz to 3.9 GHz [68]. The overall size of the prototype is 3 cm by 12 cm.

The optimization of the lumped-element matching networks results in the information regarding the necessary frequency response for the PA operation. Then, a finite element method-based simulator (Ansys HFSS Version 12) is used to dimension the input and output CRLH HMSIW waveguides, in order to obtain the same frequency response. The optimization process addresses mainly the real and imaginary part of the S-parameters of the HMSIW structures in the selected frequency points of the considered bandwidth.

Figure 3.20b also shows a detail of the meander line capacitor, pointing the relevant geometric parameters. Three different parameters (W_m, L_a, L_b) are optimized in order to match the correct value of the series capacitance of the CRLH cells. Additionally to the optimization of the interdigital capacitors shape, the guide width is used as an additional degree of freedom in this design phase, leading to input and output waveguide sections that feature different widths. This is

due to the fact that the meander slots in each section modify in different ways the characteristics of the structure.

The ground path along the cells length (Figure 3.20b) is placed in order to minimize the eventual radiation losses from the HMSIW guide. Finally, for measurement purposes, input and output 50 Ω microstrip transitions are added to the design and taken into account in the simulation. The final geometric parameters of the design are listed in Table 3.4. After the full-wave analysis of the HMSIW sections, the S-parameters resulting from simulation are imported in the HB simulator, where a final analysis of the complete structure is carried out. The simulated performance for the complete design is shown in Figure 3.21-Figure 3.25.

Component	Value (mm)	Component	Value (mm)
L_1	22	$L_{a,5}$	1.76
L_2	27.4	$L_{a,6}$	1.52
L_3	9	$L_{b,1}$	0.85
L_4	17.7	$L_{b,2}$	1.3
L_5	2	$L_{b,3}$	0.53
L_6	9.7	$L_{b,4}$	1.8
W_1	15.5	$L_{b,5}$	2.4
W_2	24.5	$L_{b,6}$	1.54
W_3	5.8	$W_{m,1}$	0.25
W_4	5.4	$W_{m,2}$	0.25
$L_{a,1}$	1	$W_{m,3}$	0.25
$L_{a,2}$	1.3	$W_{m,4}$	0.44
$L_{a,3}$	0.93	$W_{m,5}$	0.39
$L_{a,4}$	1.5	$W_{m,6}$	0.47

Table 3.4: Geometric dimensions of the input and output matching networks of the broadband PA (Figure 3.20b).

3.3.3 Experimental Results

The implemented prototype is characterized with an input power of 20 dBm provided by an Agilent signal generator (Agilent E8247C). The output power is

then evaluated by means of an Agilent spectrum analyzer (Agilent E4448A), in order to calculate the efficiency and gain characteristics of the PA at the frequencies of interest. The active device is biased with V_{gs}=0.5 V and V_{ds}= 4.2 V.

In Figure 3.21, the simulated and measured gain is plotted versus operating frequency. As it can be seen, the measured gain exceeds 4 dB in the frequency band from 2.3 GHz to 3.5 GHz, with the peak value of 6.9 dB at 2.4 GHz. A second peak of 6.2 dB, which has not been predicted in the simulation, is additionally measured at the other extreme of the band.

The same behavior is observed in Figure 3.22, where a comparison between the simulated and measured power added efficiency is shown. One can see that the power added efficiency shows a peak of 38 % at 2.4 GHz. The simulated and measured evolution of the drain efficiency versus frequency is plotted in Figure 3.23, showing a maximum value of about 49 % at approximately 2.7 GHz.

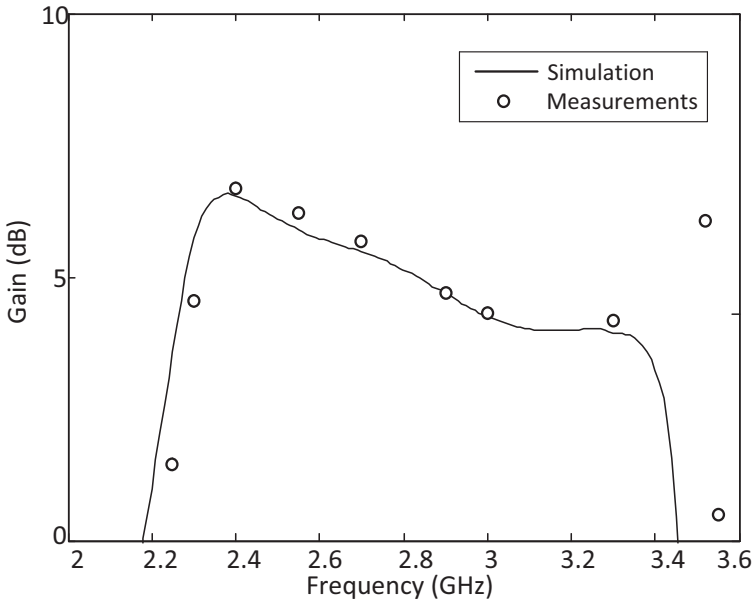

Figure 3.21: Simulated and measured gain versus operating frequency for an input power of 20 dBm. The measurements are for V_{ds}= 4.2 V and V_{gs}=0.5 V.

Figure 3.21-Figure 3.23 show that a second peak is measured at 3.5 GHz, although it has not been predicted during the simulation phase. The discrepancies between the simulated and the measured performance of the power amplifier versus frequency are mainly attributed to inaccuracies in the nonlinear model of the transistor as the higher extreme of the operating frequency band is approached. As

it can be observed from the measurement results, the device presents a slightly wider bandwidth and a small shift to higher frequencies respect to simulations. Additional factors that contribute to the simulation inaccuracy are the i) fabrication tolerance (during the drilling and milling phase), ii) tolerance of the capacitors and inductors and iii) tolerance of the substrate material properties.

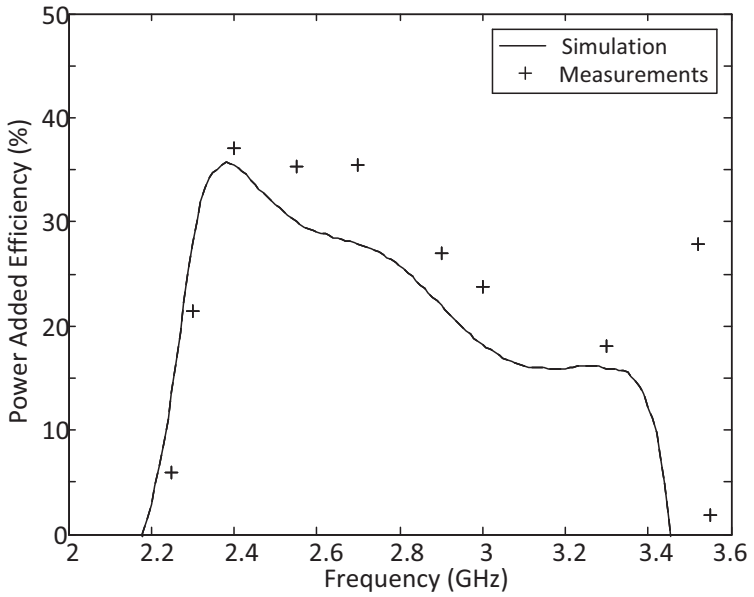

Figure 3.22: Simulated and measured power added efficiency versus operating frequency for an input power of 20 dBm. The measurements are for V_{ds}= 4.2 V and V_{gs}=0.5 V.

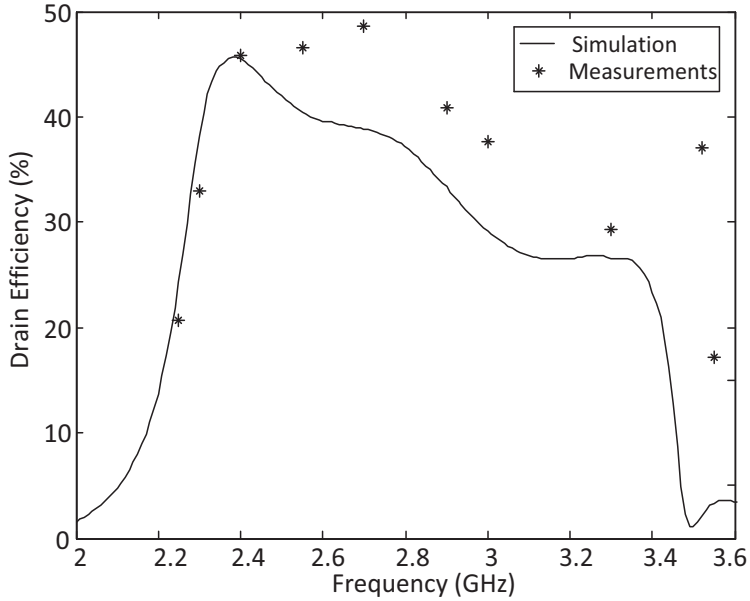

Figure 3.23: Simulated and measured drain efficiency versus operating frequency for an input power of 20 dBm. The measurements are for V_{ds}= 4.2 V and V_{gs}=0.5 V.

Finally, the performance of the implemented PA is tested for different input power levels ranging from 0 to 21 dBm at 2.4 GHz, showing good agreement between measurements and simulation, as it is shown in Figure 3.24 and Figure 3.25. The measurements demonstrate the possibility to employ the concept of broadband and multi-band CRLH TLs for the design of SIW PA topologies.

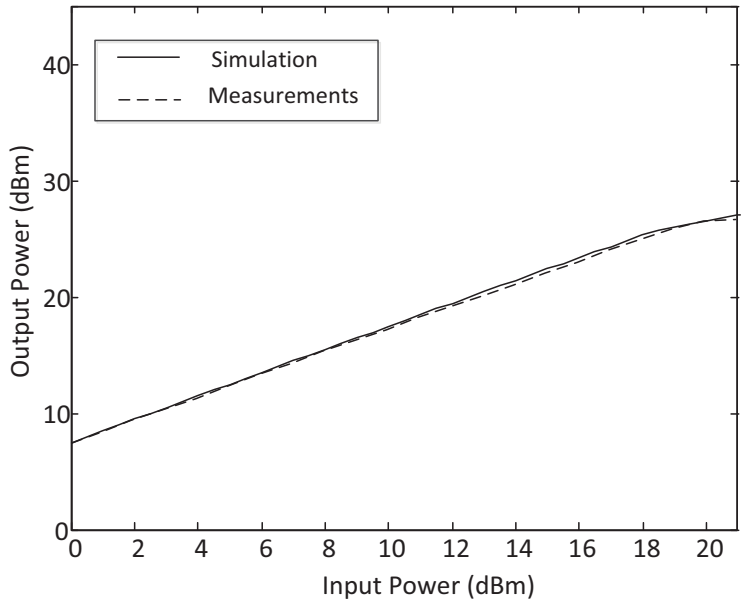

Figure 3.24: Simulated and measured output power versus input power at 2.4 GHz for the broadband PA. The measurements are for V_{ds}= 4.2 V and V_{gs}=0.5 V.

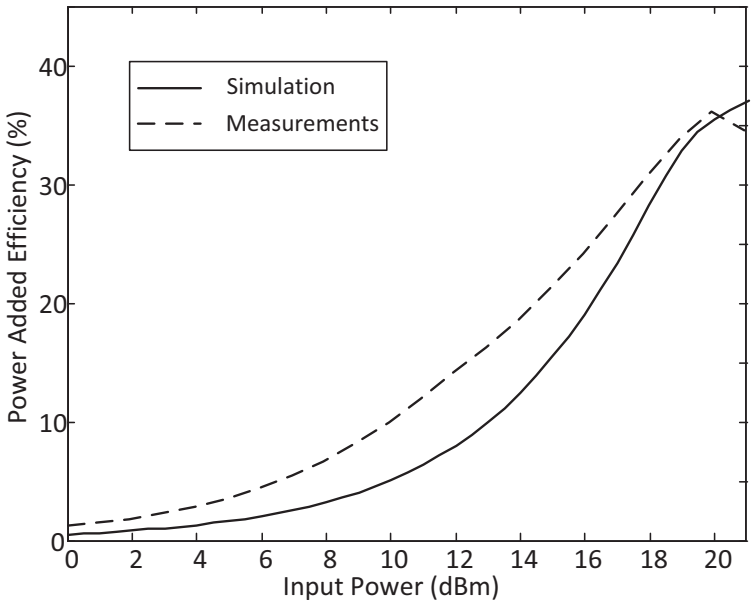

Figure 3.25: Simulated and measured PAE at 2.4 GHz operation for the implemented PA. The measurements are for V_{ds}= 4.2 V and V_{gs}=0.5 V.

3.4 Chapter Summary

This Chapter presents the design and development of i) a dual-band power amplifier operating at 2.4 GHz and 3.35 GHz and ii) a broadband power amplifier based on SIW technology. Both approaches are based on the use of CRLH unit cells for the implementation of the impedance matching networks. Initially, the dual-band PA is designed based on CRLH unit cells and is characterized in terms of measurements. A maximum drain efficiency of 65 % and 52 % is achieved for an output level of 28.7 dBm and 27.5 dBm at 2.4 GHz and 3.35 GHz, respectively and thus, the proposed design can be successfully applied for the design of dual-band PAs operating at an arbitrary set of frequencies.

Starting from this achievement, the design of CRLH unit cells in Half-Mode SIW topology has been investigated for the design of a broadband PA topology. In this design, the impedance matching networks of the device are realized in CRLH Half-Mode SIW waveguide, thus allowing for a more compact implementation, and for a reduction in the number of metal vias needed. The PA is designed following a single-transistor topology, and thanks to the CRLH waveguide sections the number of lumped-elements to be soldered is greatly reduced. Moreover, the use of HMSIW input and output matching networks permits a straightforward integration of the device within the packaging of the complete wireless platform. Using the SIW technology for the design of multi-band or broadband PAs opens a variety of new perspectives, since it combines the advantages of the capability to operate at different standards with compact and easy to fabricate structures.

Chapter 4

Thermal Energy Harvesting from Power Amplifier Operation

4.1 Introduction

Power amplifiers are fundamental components in any transmitter circuit. Unfortunately, power amplification has a poor efficiency that results in a significant amount of wasted power, as it has already been discussed in the previous Chapters. Figure 4.1 shows the calculated dissipated power from the operation of highly efficient PAs, where it can be seen that a lot of power is dissipated in terms of heat in the case of high power PAs [25], [80]-[87]. The possibility to recover DC electrical power from this wasted heat using thermoelectric generators (TEGs) is of great interest, as it can be utilized for providing back up electricity, supply low-power sensors and control circuits forming part or placed near a transmitter circuit.

So far, numerous investigations have been carried out for the energy recovery from the dissipated power of many devices (usually indicated as thermal energy harvesting), such as the thermoelectric power generation from the operation of the Central Processing Unit (CPU) [88]-[90]. In [88], the possibility to implement a heat driven cooling system using a TEG attached to the CPU of a portable

computer has been experimentally demonstrated. The generated electricity has been supplied to a cooling fan which provided sufficient airflow to heatsinks that in turn keep the temperature of the CPU below 85 °C. In [90], the wasted power from the operation of a microprocessor has been considered. Using a commercial TEG, 7 mW of power has been harvested from a Pentium III processor operating at 1 GHz [90].

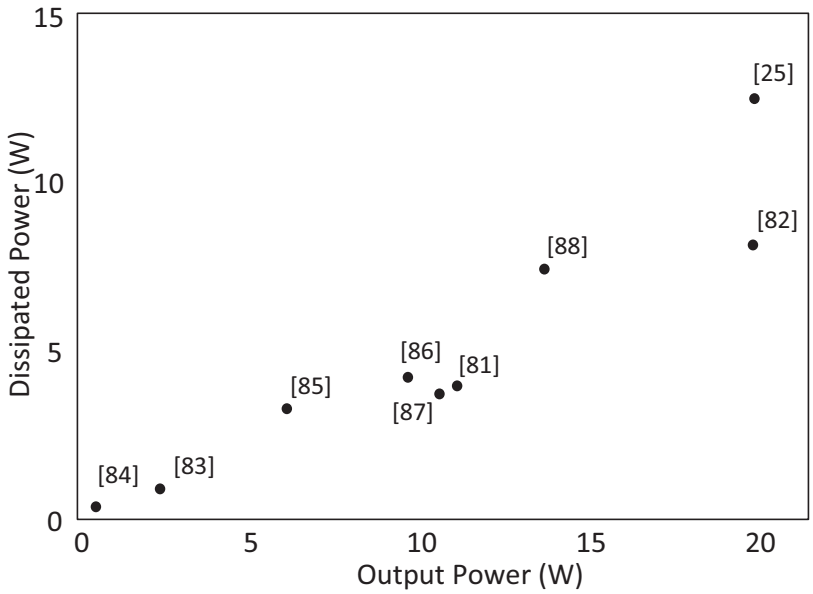

Figure 4.1: Calculated dissipated power from the operation of efficient power amplifiers in the literature [25], [80]-[87].

In this Chapter, the potential to recover electrical DC power from the operation of a power amplifier is examined [91], [92]. A novel approach for exploiting the dissipated power from the power amplification process using commercial thermoelectric generators and its conversion to DC power is introduced, employing both simulated and experimental results. The main idea is that the harvested power could either be used as a part of the power supply of the power amplifier circuit or even supply low-power sensors.

This Chapter is organized as follows. Initially, the operating principles of the TEGs are briefly discussed (Section 4.2). Then, a preliminary thermal model that can be used in circuit simulators to predict the amount of DC power that can be obtained from a thermal energy harvesting scenario is presented in Section 4.3. Section 4.4 and Section 4.5 present a set of experimental results using commercial TEGs in different topologies. At the end of the Chapter (Section 4.6), the obtained results are discussed.

4.2 Thermoelectric Generators

Under full operation conditions the active device of the power amplifier can reach high temperature levels, which are translated into wasted heat. Commercial TEGs can be used to recover electrical power from the generated heat in thermal energy harvesting applications and their operation relies on the Seebeck effect [93], [94]. The Seebeck effect describes the phenomenon where a voltage is generated from the temperature difference across the junctions of dissimilar metals/semiconductors [94] (Figure 4.2).

TEGs are usually packaged inside a thermogenerator package (TGP) that protects them and provide the integration of the system. The TEG package is mounted between the hot (T_{hot}) and the cold source (T_{cold}) and its temperature difference (ΔT) leads to heat flow through the TEG, as Figure 4.3 shows. The temperature difference across the TEG of the system is given by

$$\Delta T = T_{hot} - T_{cold} \tag{4.1}$$

where T_{hot} and T_{cold} is the hot and cold temperature (Figure 4.3), respectively.

The limit of the maximum theoretical efficiency of thermal to electrical energy conversion, defined as Carnot efficiency (η_c), can be calculated by measuring the T_{hot} and T_{cold} of the TEG, as (4.2) indicates.

$$\eta_c = \frac{\Delta T}{T_{hot}} \tag{4.2}$$

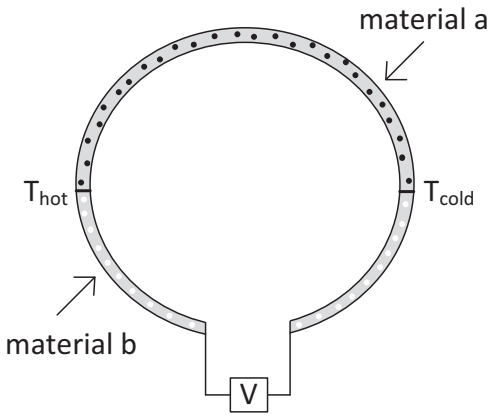

Figure 4.2: A voltage is generated from the temperature difference across the junctions of dissimilar metals/semiconductors (Seebeck effect) [94].

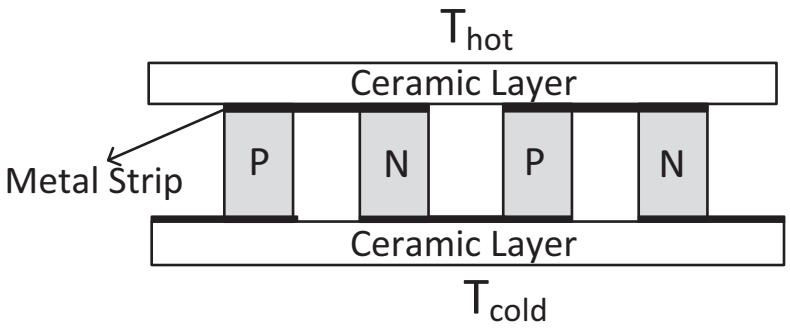

Figure 4.3: Structure of a thermoelectric generator.

The hot and cold side contacts of the TEG are thermally connected in parallel and electrically connected in series, using ceramic layers with low thermal conductivity, as it is shown in Figure 4.3. A pair of N-type and P-type thermoelements (usually called as a thermocouple) is the basic building block for most of the thermoelectric generators and refrigerators [94].

For the evaluation of the TEG, the conversion efficiency (η_{conv}) for the maximum output power is also used and is defined as

$$\eta_{conv} = \eta_c \frac{\sqrt{Z_{th}\overline{T}+1}-1}{\left(\sqrt{Z_{th}\overline{T}+1}+\frac{T_{cold}}{T_{hot}}\right)} \tag{4.3}$$

where $\overline{T}$ is the mean temperature across the thermoelements ($(T_{hot}+T_{cold})/2$) and Z_{th} is the thermoelectric figure of merit [94]. The conversion efficiency is primarily limited by the Carnot efficiency and the figure of merit of the thermoelectric materials, which depends on the Seebeck coefficient α, the electrical conductivity σ, and the thermal conductivity λ, as it shown in (4.4).

$$Z_{th} = \frac{\alpha^2\sigma}{\lambda} \tag{4.4}$$

The figure of merit of a thermoelectric material indicates if the material is suitable for thermoelectric applications and depends on many factors, such as the material properties [94].

4.3 Thermal Model

In this Section, a preliminary thermal model that predicts the harvested DC power from the operation of a power amplifier is considered. A commercial thermogenerator package from Micropelt (TGP-751) is used in the proposed thermal energy harvesting setup. TGP-751 is shown in Figure 4.4 and is integrated with a DC-Booster, power management and heatsink. For the selected commercial TEG, the thermoelectric material is bismuth telluride (Bi_2Te_3), which is mainly used when the cold junction temperature is approximately 300 K and has a figure of merit of 0.0025 K^{-1} [93]-[96]. The properties of the TGP-751 [97] are listed in Table 4.1.

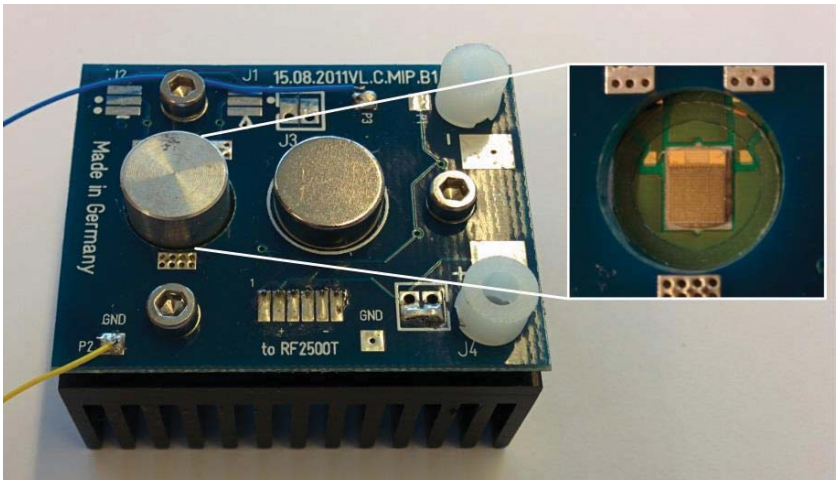

Figure 4.4: Micropelt thermoharvesting module with integrated TGP, DC-Booster, power management and heatsink [97].

Component	Value
R_{elec}	300 Ω
R_{th}	18 K/W
Seebeck Voltage	110 mV/K
TEG inside	MPG-D751
Length	15 mm
Width	10 mm
Weight	2.2 gr

Table 4.1: Properties of the TGP-751 according to manufacturer datasheet [97].

Figure 4.5 shows the schematic of the thermal energy harvesting setup that consists of a power amplifier, a thermoelectric generator package and a heatsink. The power amplifier is represented as a transistor placed on the Arlon 25N (A_{25N}) PCB substrate. The TEG is attached on the bottom side of the PCB, at the area below the transistor, as it can be seen from Figure 4.5.

Using the analogy between the electrical and heat charge [93] that is shown in Table 4.2, a preliminary thermal model is derived to predict the harvested power level from the thermal energy harvesting setup of Figure 4.5. The setup can be expressed in terms of the thermal resistances (R_{th}) in a commercial circuit simulator, as Figure 4.6 illustrates. A temperature gradient (voltage difference) between the top and the bottom sides of the generator results in heat (current) flowing through the TEG, and thus to an open circuit at the TEG output terminals.

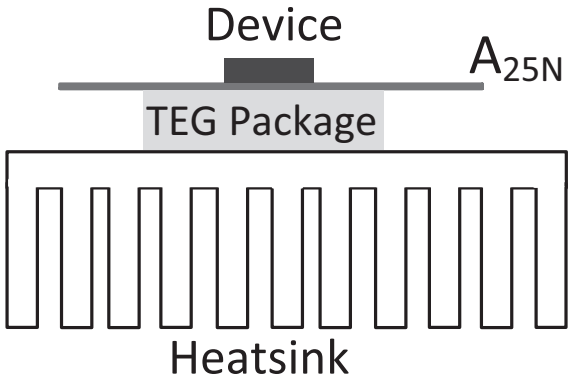

Figure 4.5: Schematic of the thermal harvesting setup, where the TEG is attached on the bottom side of the PCB, at the area below the transistor.

Electrical Quantity	Symbol	Unit	Thermal Quantity	Symbol	Unit
Voltage	V	V	Temperature	T	K
Current	I	A	Heat	Q	W
Electrical Resistance	R_{elec}	Ω	Thermal Resistance	R_{th}	K/W
Electrical Capacitance	C	F	Thermal Capacitance	C_{th}	J/K
Ground	0 V		Absolute zero temperature	0 K	

Table 4.2: Electrical and thermal analogy [95].

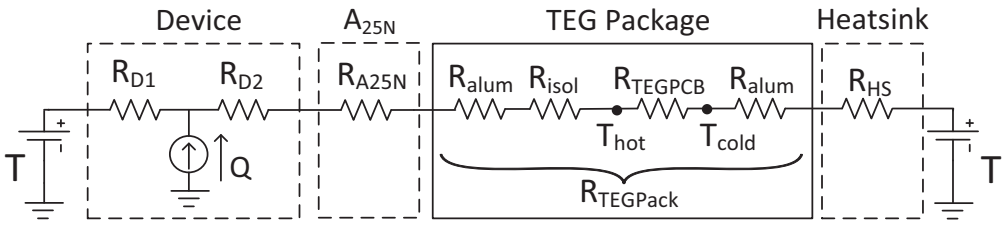

Figure 4.6: Equivalent thermal circuit for the thermal harvesting setup of Figure 4.5. The model consists of the total thermal resistance of the device, the substrate, the TEG package and the heatsink.

The thermal model of Figure 4.6 is simulated using the DC analysis in Agilent ADS. Using the analogy between the thermal and the electrical conduction [93], the simulation has predicted a hot temperature of 318.1 K and a cold temperature of 306.7 K. Thus, a maximum harvested power of 2.1 mW and a Carnot efficiency of 3.58 % are expected. In the next Section, the experimental results of this setup are presented and compared with the simulation.

Thermal capacitances are not included as only steady state conditions are considered. The thermal equivalent circuit consists of the thermal resistance of the device (R_{D1} and R_{D2}), the substrate (R_{A25N}), the TEG package ($R_{TEGPack}$) and the heatsink (R_{HS}). The total thermal resistance of the TEG package ($R_{TEGPack}$) is the series connection of the thermal resistances of the TEG PCB (R_{TEGPCB}), two layers of aluminium (R_{alum}) and the ring isolator (R_{isol}), as Figure 4.6 shows. R_{A25N} takes into account the thermal resistance due to the substrate material and the thermal resistance due to the contact between the PA board and the TEG. The selected values of the thermal resistances are based on the manufacturer datasheets [97] and are listed in Table 4.3.

Quantity	Symbol	Value (K/W)
R_{th} of the device (junction-ambient)	R_{D1}	125
R_{th} of the device (junction-substrate)	R_{D2}	29
R_{th} of the substrate and the contact	R_{A25N}	10
Total R_{th} of the TEG package	$R_{TEGPack}$	18
R_{th} of the TEG PCB	R_{TEGPCB}	12.5
R_{th} of the heatsink	R_{HS}	5.8

Table 4.3: Thermal resistances values for the thermal model of Figure 4.6. The values of the thermal resistances are based on the manufacturer datasheets [97].

4.4 Experimental Results

In this Section, a set of experimental results for the power generation from a thermal energy harvesting setup is presented. Initially, a 1 Watt PA prototype is designed based on the ATF-50189 E-pHEMT from Avago [68] in order to be used as the heat generating mechanism. The circuit schematic and component values are shown in Figure 4.7 and Table 4.4, respectively.

The prototype is fabricated on Arlon 25N substrate with height of 30 mil, relative permittivity of 3.38 and loss tangent of 0.0025 using an LPKF Protomat C100/HF circuit board plotter [39]. The PA has a measured gain of 10 dB and power added efficiency of 34 % when operating with a 2.45 GHz 19 dBm input signal. The device drain bias is 4.5 V, the gate bias is 0.54 V and the drain current is 465 mA, corresponding to a dissipated power of 1.37 W. Due to the fact that the prototype is intended to be used in a thermoelectric energy harvesting system, its efficiency is not optimized to be maximum.

After designing and characterizing the power amplifier, a preliminary experiment is carried out in order to evaluate the thermal behavior of the circuit and find out the area with maximum temperature on the PCB.

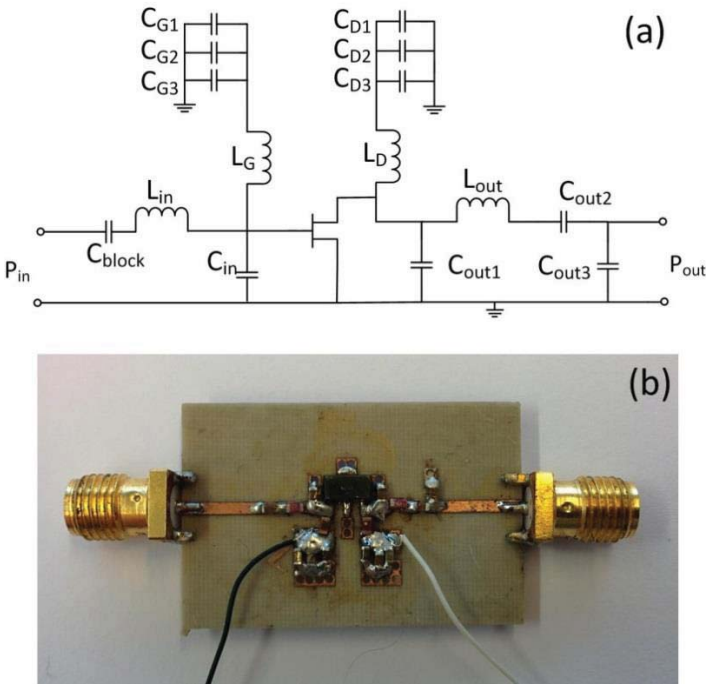

Figure 4.7: a) Simulated power amplifier circuit schematic and b) fabricated prototype. The fabricated prototype has a total size of 3.2 cm by 2.1 cm.

Component	Value	Component	Value
C_{block}	4.7 pF	C_{D2}	1 nF
L_{in}	3 nH	C_{D3}	4.7 uF
C_{in}	1.8 pF	L_D	680 nH
L_G	4.7 nF	L_{out}	3.3 nH
C_{G1}	1 uF	C_{out1}	0.5 pF
C_{G2}	1 nF	C_{out2}	0.5 pF
C_{G3}	4.7 uF	C_{out3}	0.5 pF
C_{D1}	1 uF		

Table 4.4: Power amplifier circuit (Figure 4.7a) component values.

The thermal behavior of the PA is evaluated by measuring the temperature along the ground plane of the PCB at 72 different points, as Figure 4.8a shows. The measurements are taken with a digital multimeter from TENMA and a temperature probe. The temperature probe is in contact with the corresponding measuring point on the board and each measurement is taken after allowing sufficient time for the probe reading to stabilize. The temperature varies depending on the measurement point and the maximum achievable temperature value is obtained for the points close to the area where the transistor is located.

The measured temperature distribution of the PCB is shown in Figure 4.8b, where a maximum temperature of 355.4 K (82.4 ^{o}C) is measured for an ambient temperature of 298.7 K (25.7 ^{o}C). Based on these values a Carnot efficiency of 15.95 % is estimated. Once a TEG module is brought to contact with the PA circuit board, its thermal resistance leads to a new thermal equilibrium where a reduced temperature gradient is present between the hot and cold sides of the TEG. The new thermal equilibrium as well as the underestimation of the contact thermal resistance in the model (included in R_{A25N}) result in a reduced Carnot efficiency.

Starting from these measurements, an experiment for the electrical power generation from the power amplifier operation is carried out. The TEG is placed in contact with the metal ground of the PA circuit board at the area that presented maximum temperature (Figure 4.8b), as it is shown in Figure 4.5. The photos of the experimental setup are shown in Figure 4.9 and Figure 4.10.

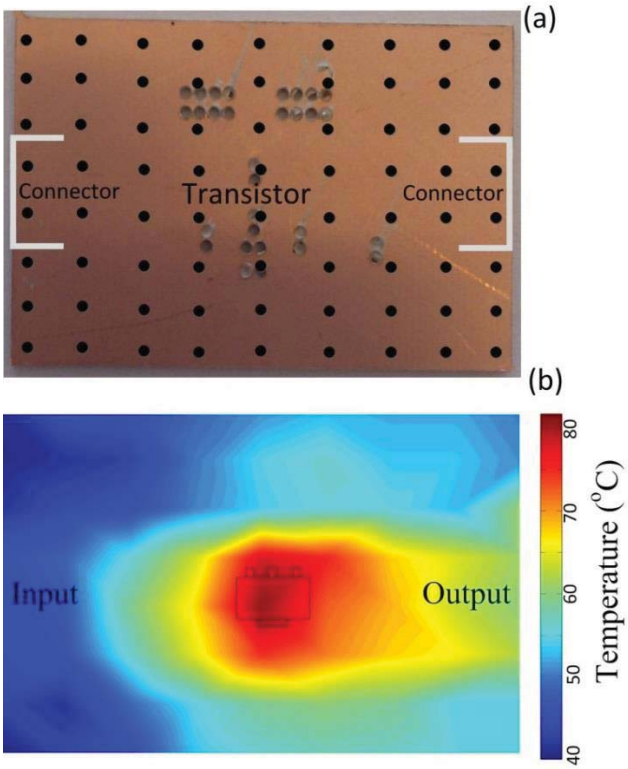

Figure 4.8: Temperature distribution measurement: a) selected measurement points on the metal ground of the power amplifier board and b) measured temperature distribution.

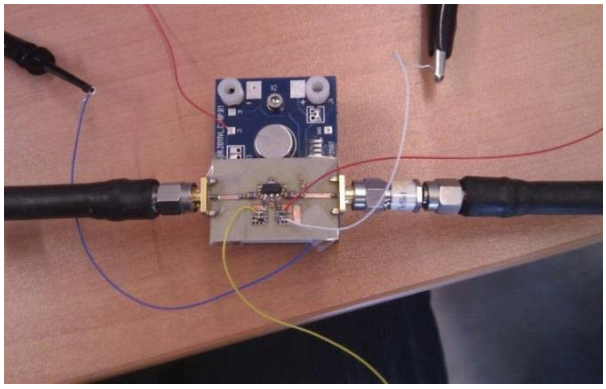

Figure 4.9: Experimental setup for scavenging the wasted power from a power amplifier operation. The TEG is attached on the bottom side of the PA, at the area below the transistor.

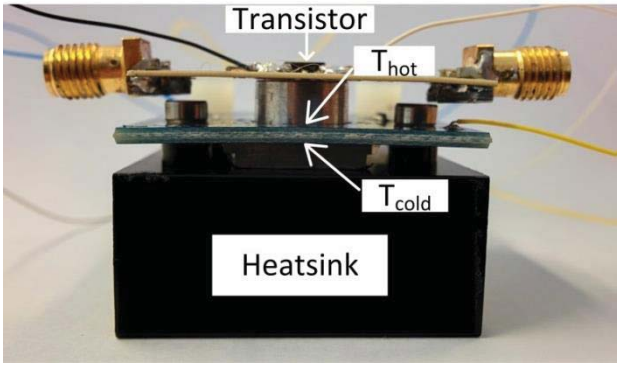

Figure 4.10: Side view of the energy harvesting setup of Figure 4.9 [97].

The value of the electrical resistance of the TEG (R_{elec}=300 Ω) is used as provided by the manufacturer [97] in order to calculate the maximum harvested power according to (4.5). The maximum harvested DC power (P_{max}) can be expressed in terms of the TEG open circuit voltage (V_{oc}) and short circuit current (I_{sc}) as

$$P_{max} = \frac{V_{oc} I_{sc}}{4} \tag{4.5}$$

where the open circuit voltage and short circuit current are given by (4.6) and (4.7), respectively,

$$V_{oc} = \alpha \Delta T \tag{4.6}$$

$$I_{sc} = \frac{V_{oc}}{R_{elec}} \tag{4.7}$$

where α is the Seebeck coefficient that depends on the properties of the materials and R_{elec} is the electrical resistance of the TEG [94].

Figure 4.11 shows the evolution of the measured V_{oc} and I_{sc}, where it is shown that the output terminals of the TEG reach a steady state after approximately 4 minutes of operation, with maximum values of V_{oc}=1.31 V and I_{sc}=3.1 mA respectively. Consequently a maximum available harvested output power (P_{max}) of 1.015 mW is measured, which is lower than the one predicted in simulations of 2.1 mW due to the differences in the simulated and measured $T_{hot.}$

The measured and simulated Carnot efficiency and conversion efficiency versus the temperature gradient at the TEG are shown in Figure 4.12. More accurate theoretical conversion efficiency can be calculated by taking into account the dimensions of the TEG [94]. The measured temperature at the hot and cold sides of the TEG (T_{hot}=313.1 K and T_{cold}=305.9 K) predict a Carnot efficiency of 2.3 %, while the simulated thermal model predicted a 3.58 % Carnot efficiency due mainly to a higher simulated T_{hot}. Table 4.5 summarizes the performance of the

measuring setup. The difference between the simulated and measured Carnot efficiency is mainly attributed to the underestimation of the value of the thermal contact resistance (included in R_{A25N}) that in the experiment is higher due to the existing air gaps between the PA board and the TEG.

A fluid with large thermal conductivity can be used in order to fill the air gaps between the PA board and the TEG, in order to obtain a better thermal contact and thus improve the agreement between the simulated and measured temperature values.

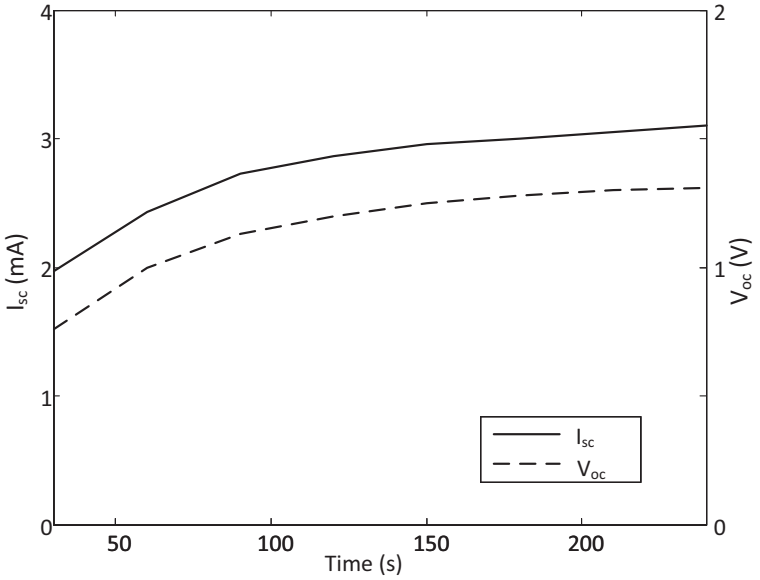

Figure 4.11: Measured TEG open circuit voltage and short circuit current from the experimental setup of Figure 4.9. The maximum measured values are V_{oc}=1.31 V and I_{sc}=3.1 mA.

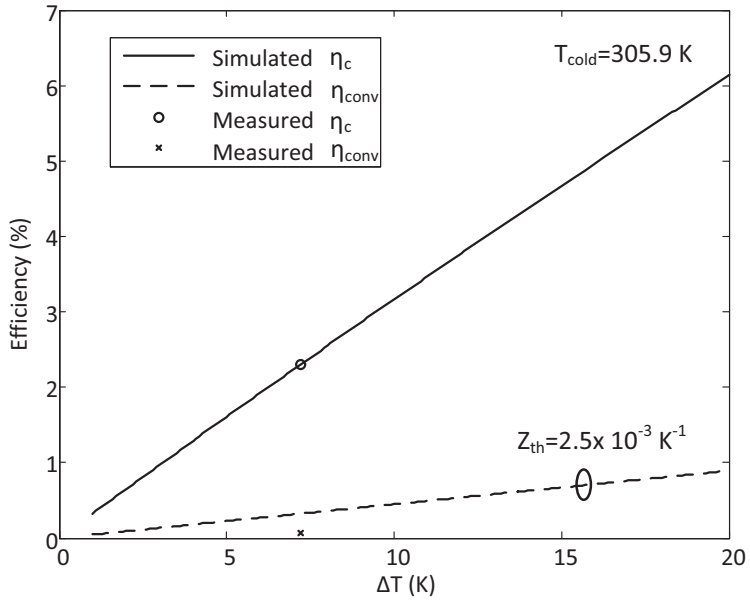

Figure 4.12: Carnot efficiency and conversion efficiency versus temperature gradient at the TEG contacts.

Parameter	Simulation	Measurements
T_{hot} (K)	318.1	313.1
T_{cold} (K)	306.7	305.9
ΔT (K)	11.4	7.2
η_c (%)	3.58	2.3
P_{max} (mW)	2.1	1.015
η_{conv} (%)	0.51	0.074

Table 4.5: Comparison of the simulated and measured results for the thermal energy harvesting experiment.

4.5 Multiple TEG Setup

This Section explores the possibility to harvest the dissipated power from the operation of a power amplifier using additional TEGs. One, two and three thermoelectric generators are placed at the thermal energy harvesting setup of Figure 4.5 in order to investigate the potential to increase the harvested DC power level. A PA with a dissipated power level of 0.76 W is used as a source of heat for these experiments.

The basic thermal energy harvesting setup that includes a single TEG has already been demonstrated in Section 4.4 and it is shown in Figure 4.5. The same set of measurements is performed using additional TEG packages in order to increase the amount of harvested power. The schematics of the thermal energy harvesting setups that consist of two and three TEGs in series are shown in Figure 4.13a and Figure 4.13b, respectively.

The major difficulty to perform these experiments is to obtain a good contact among the TEG packages. The analysis of the setup of Figure 4.13a and Figure 4.13b in terms of thermal resistances is shown in Figure 4.14a and Figure 4.14b, respectively. The photo of the experimental setup that consists of two TEGs is shown in Figure 4.15.

A performance comparison of the proposed setups is shown in Table 4.6, where the measurement results are summarized. As it can be noticed, the maximum harvested output power level, when one thermoelectric generator is used, is 0.23 mW (Figure 4.5). In the case that two thermoelectric generators are placed in the

setup (Figure 4.13a), the maximum harvested power from the TEG_1 and TEG_2 is 0.177 mW and 0.086 mW, respectively. Thus, an overall maximum harvested power of 0.273 mW is measured using the thermal energy harvesting setup of Figure 4.14. Hence, an increased harvested power level is achieved using two thermoelectric generators.

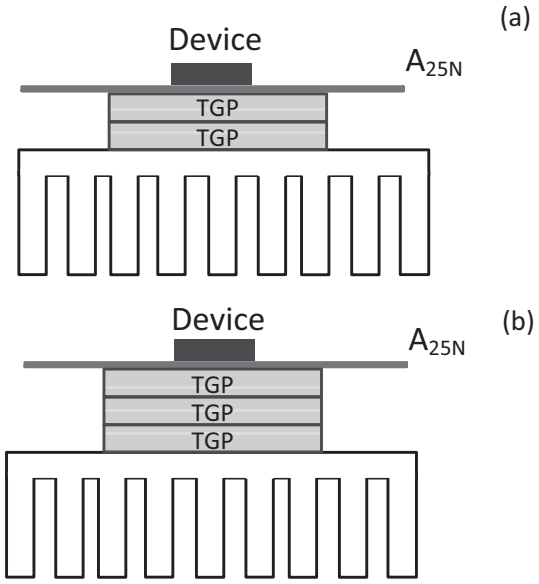

Figure 4.13: Schematic of the thermal harvesting setup with a) two TEG packages and b) three TEG packages.

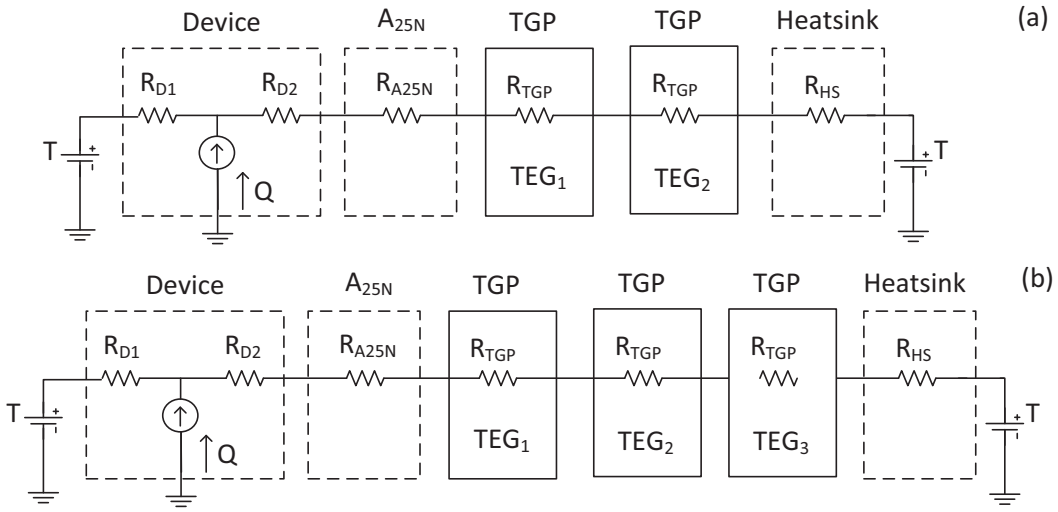

Figure 4.14: Equivalent thermal circuit of the setup of Figure 4.13a and Figure 4.13b.

In the same way, TEG_1, TEG_2 and TEG_3 produce a maximum harvested power of 0.15 mW, 0.07 mW and 0.04 mW, respectively, resulting in a total P_{max} of 0.26 mW. Therefore, by placing three TEGs in the setup, a reduced harvested DC power level is achieved if compared with the case of two TEGs.

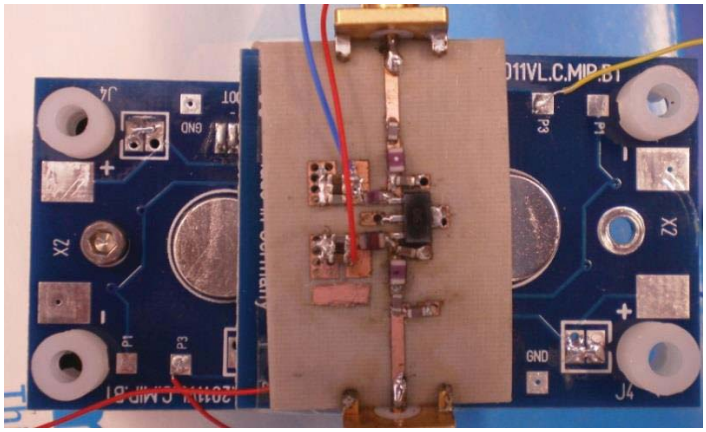

Figure 4.15: Stacked TEG topology for the heat scavenging from a power amplifier using two thermoelectric generators in series [97].

		T_{hot} (K)	T_{cold} (K)	ΔT (K)	η_c (%)	P_{max} (mW)
One TEG		302.6	299.8	2.8	0.92	0.23
Two TEGs in series	TEG_1	305.4	302.6	2.8	0.9	0.177
	TEG_2	301.5	299.3	2.2	0.73	0.086
Three TEGs in series	TEG_1	305.9	302.6	3.3	1.08	0.15
	TEG_2	302	299.8	2.2	0.73	0.07
	TEG_3	299.3	298.2	1.1	0.37	0.04

Table 4.6: Measurement results for the thermal energy harvesting experiment with one, two (Figure 4.13a) and three TEGs in series (Figure 4.13b).

One can see that that there is an optimal number of TEGs that can be put in series in a thermal energy harvesting setup in order to maximize the total harvested DC power level. Once this number is reached, adding more TEGs to the setup is not able to increase the harvested DC power mainly due to the increased thermal resistance among the TEGs.

4.6 Chapter Summary

In this Chapter, a novel idea for exploiting the power losses from power amplifier circuits and converting it to useful DC power is presented. It is experimentally shown that 1 mW of power can be harvested from a power amplifier with a dissipated power of 1.37 W using a commercial thermoelectric generator attached to the PCB of the circuit. The possibility to increase the harvested DC power using

additional TEGs is also considered. The amount of harvested power increases for high power amplifiers but even for a 1 Watt PA, the harvested power level is enough to supply low-power sensors and control circuits forming part or placed near a transmitter circuit.

Chapter 5

Design of Resistance Compression Network based Envelope Amplifier

5.1 Introduction

The design of efficient power amplifiers operating with high peak-to-average power ratio (PAPR) input signals has attracted much attention recently due to the emergence of modern communication standards. As it has been already discussed in the previous Chapters, new modulation schemes produce complex signals with high peak-to-average power ratio, in the range of 8.5 dB to 13 dB for 4G systems [8], [14]. The power amplification of such signals implies that the PA should operate efficiently over a wide range of input power levels.

At the same time, the RF power amplifier has to attain the quality of the transmitted signals and thus high linearity has to be met. The additional linearity constraints imply that the power amplifier must operate in the back off mode, resulting to poor average system efficiency, increased dissipated power level and additional running cost of the system.

To improve the efficiency in the back off region, several efficiency enhancement techniques have been proposed in the literature [11]. Among them stands the envelope tracking (ET) and envelope elimination and restoration (EER)

schemes, where a dynamic power supply is used instead of a fixed supply scheme (Figure 5.1a). In particular, the fixed power supply is usually replaced with a power converter circuit (usually indicated as envelope amplifier) that amplifies the envelope signal. ET and EER topologies can improve the PA efficiency at low-power input signals and thus minimize the dissipated power that is converted into wasted heat.

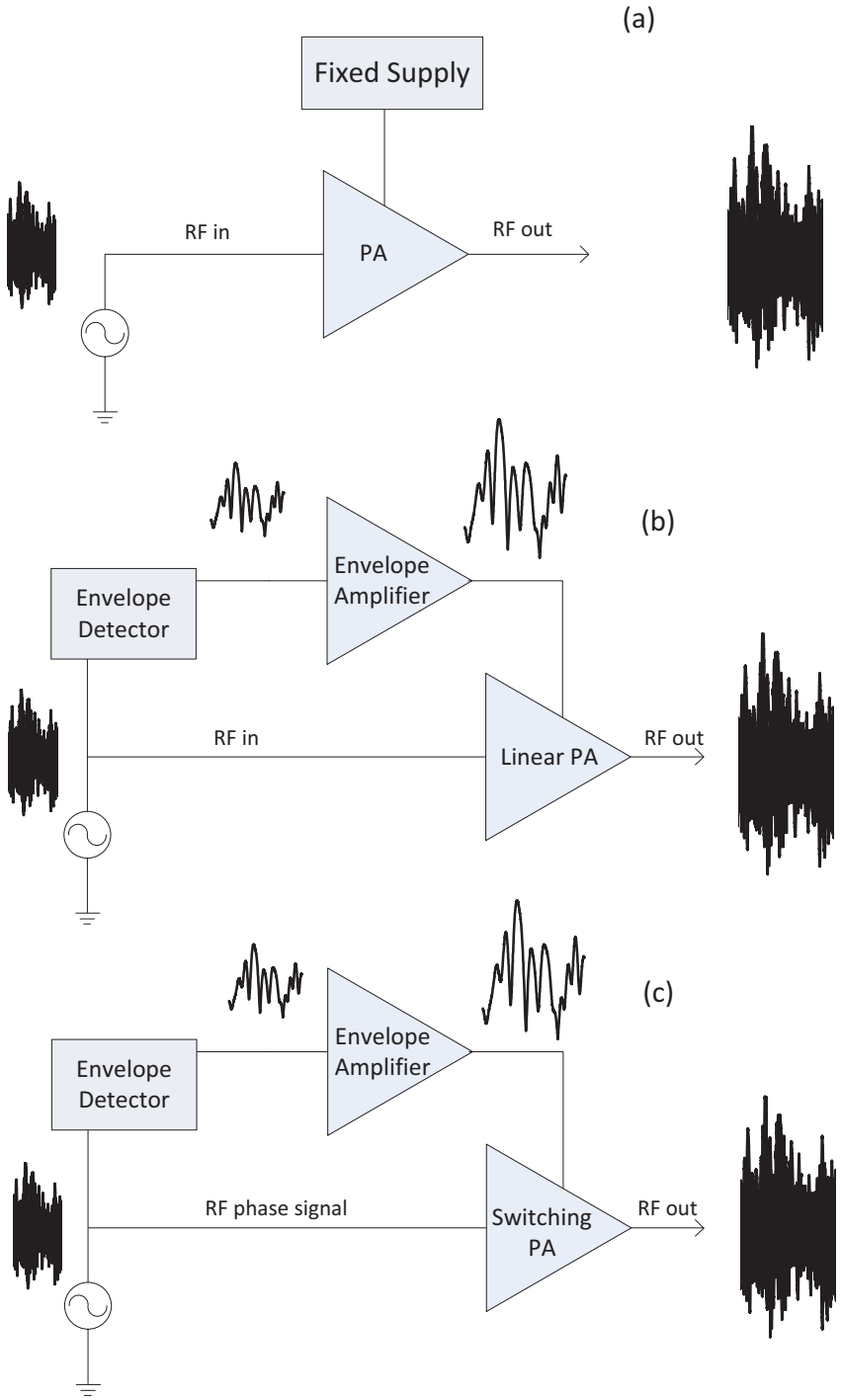

Figure 5.1: Simplified schematics of a) fixed power supply amplifier topology, b) ET topology and c) EER topology.

The ET architecture consists of an envelope amplifier (EA) and a linear (or slightly compressed) RF PA, as it is shown in Figure 5.1b. In contrast, EER technique employs a nonlinear and highly efficient RF PA that processes a constant envelope and phase modulated signal (Figure 5.1c). However, in both topologies, the envelope amplifier tracks the envelope of the RF input signal and dynamically adjusts the DC supply voltage of the RF PA (Figure 5.2b) resulting in a reduced level of dissipated power if compared with the conventional topology of Figure 5.2a.

The envelope amplifier can be either linear or switching (or a combination of both) and is placed between the drain/collector of the RF PA and the fixed supply source for both the ET and EER architectures, as it is shown in Figure 5.1b and Figure 5.1c, respectively. Buck (Figure 5.3a) and boost topologies (Figure 5.3b) are usually used for the design of switching EA circuits by virtue of their simplicity and their high efficiency operation [98]-[101]. A linear, but inefficient, stage can be combined with the DC-DC converter in order to improve the performance of the circuit resulting in a hybrid switching amplifier (HSA) topology [8], [14]. So far, such hybrid topologies have found successful application in the design of efficient power amplifier topologies in the literature [99]-[102].

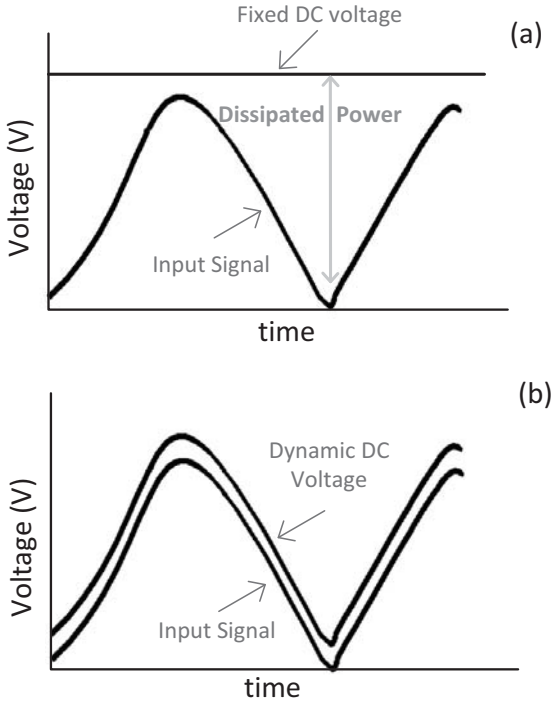

Figure 5.2: Power dissipation of a power amplifier with: a) fixed supply voltage and b) dynamic supply voltage [98].

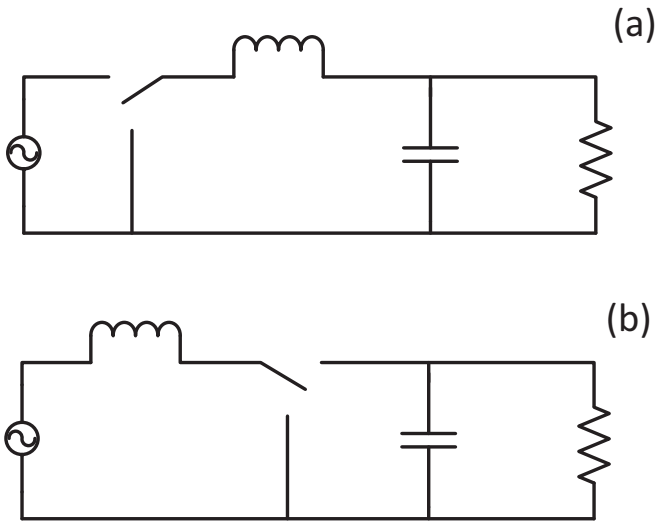

Figure 5.3: Schematic of DC/DC converters: a) buck converter topology and b) boost converter topology.

Although the ET and EER topologies can improve the efficiency of the power amplification stage (due to the reduced amount of dissipated power), special attention should be taken in the design of the envelope amplifier as the total efficiency of the system (η_{tot}) is given by the efficiency of the RF PA (η) multiplied by the efficiency of the envelope amplifier (η_{EA}), as it is shown in (5.1).

$$\eta_{tot} = \eta * \eta_{EA} \tag{5.1}$$

The efficiency of the envelope amplifier is not constant due to the impedance variations caused by the time-varying conditions of the system, such as the various drain/collector bias voltages of the RF PA [14]. Thus, the potential reduced sensitivity of the envelope amplifier to different bias voltages of the RF PA is a major challenge that could improve further the performance of ET and EER topologies.

Hybrid switching amplifiers can also find successful application in a wireless power transfer (WPT) transmitter. In contrast with the ET and EER topologies, in WPT applications high peak-to-average power ratio signals are highly desired as they can increase the RF-DC conversion efficiency in the receiver. In particular, it has been shown in [45] that signals with high PAPR are able to turn on the diode of the rectifier (Figure 5.4) for lower input power levels. Therefore, such hybrid switching amplifiers can be used to efficiently amplify the signals [103], [104].

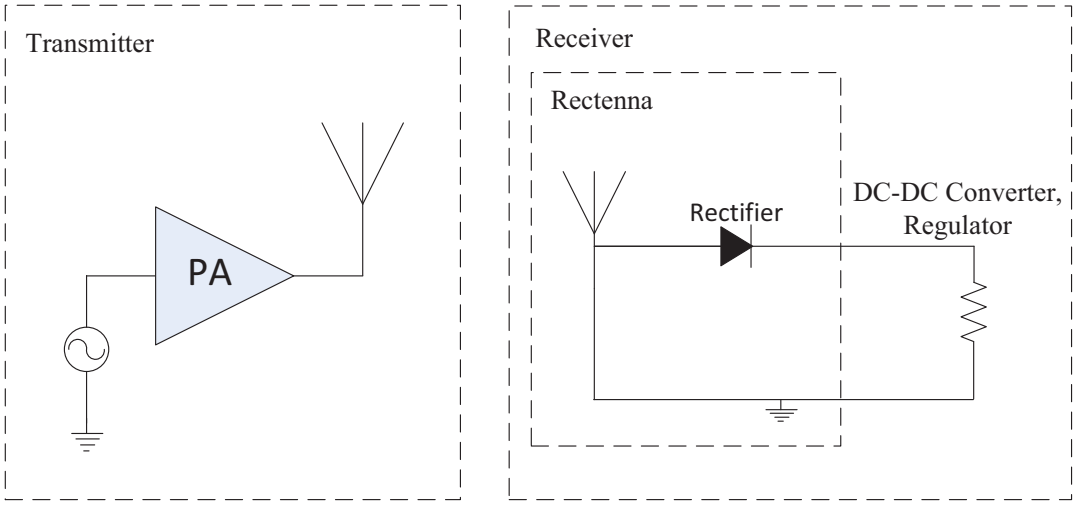

Figure 5.4: Simplified schematic of multi-sine transmitter and receiver for wireless power transfer application.

In this Chapter, the mismatch effect caused by the operating environment variations in a HSA is investigated. In particular, such an effect is alleviated by adding a resistance compression network (RCN) in the switching stage of a hybrid switching amplifier topology. A resistance compression network is a novel kind of matching network that reduces the sensitivity of electronic circuits to impedance variations [9], [10], [105]-[108]. So far, RCNs have successfully improved the performance of DC-DC converters [10], outphasing energy recovery amplifier systems [9] and rectifier circuits [105]-[107].

A novel way to implement RCNs using typical LC matching networks is proposed in this Chapter. Then, such a RCN topology is applied in the design of an envelope amplifier circuit in order to improve its performance. The obtained simulated and measured results show that the proposed design shows improved performance in comparison with a conventional HSA topology without resistance compression network.

The outline of this Chapter is as follows. Section 5.2 introduces two RCN topologies and describes their behavior in detail. In Section 5.3, the design of a conventional hybrid amplifier and the design of a HSA based on a RCN are presented. Additionally, the simulated and measured results show that the proposed structure maintains higher efficiency for different operating conditions if compared with the conventional topology. Finally, Section 5.4 discusses the obtained results.

5.2 Resistance Compression Network Theory

The structure of a RCN consists of two branches that show opposite phase response of the input impedance Z_{in} (φ and - φ) at the operating frequency, as Figure 5.5 shows. A simple way to obtain the necessary opposite phase response is by using the same network and simply reversing the input and output ports.

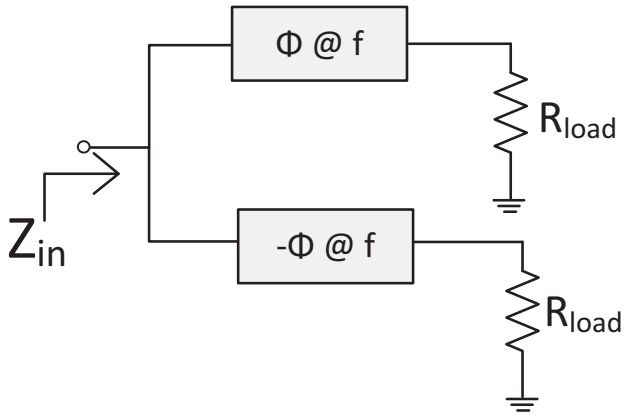

Figure 5.5: Resistance compression networks structure. Each branch exhibits an opposite phase response (φ and - φ) of the input impedance at the operating frequency.

In this Section, a novel way to achieve resistance compression, using the typical LC impedance matching networks of Figure 5.6a and Figure 5.6c is proposed. The LC matching network of Figure 5.6a exhibits an opposite phase response of the input impedance at the operating frequency f_R by simply reversing the input and output ports of the structure (Figure 5.6b). A resistance compression network can be obtained by placing the unit cells of Figure 5.6a and Figure 5.6b at the branches of a RCN topology (Figure 5.5) and the proposed RCN topology is indicated as RCN_R (Figure 5.7a).

The operating frequency of such a RCN topology can be derived with a straightforward procedure by calculating the input impedance of the topology in terms of the R_{load}, the inductor reactance Z_{ind} (as shown in (5.2)) and the capacitor reactance Z_{cap} (as given by (5.3)). Resistance compression is achieved when the network is driven at its resonance [10] and then, the input impedance (Z_{in}) of the network suffers small variations under large variations of the output load (R_{load}). The operating frequency of the RCN_R topology (Figure 5.7a) and its characteristic

impedance is given by (5.4) and (5.5), respectively.

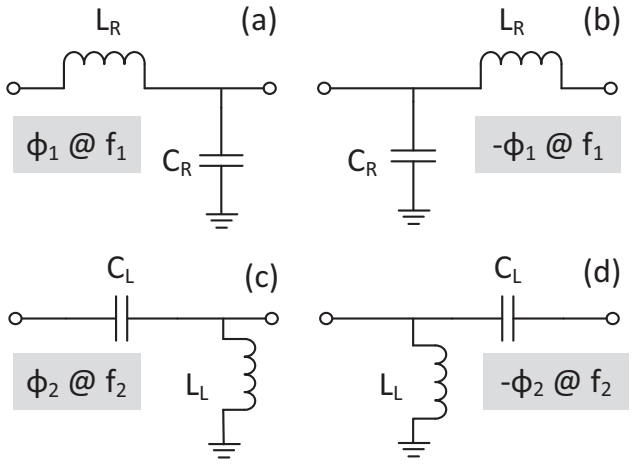

Figure 5.6: a), b), c), d) Lumped-element LC structures for RCN topologies. Figure 5.6b and Figure 5.6d show the rearranged structure of Figure 5.6a and Figure 5.6c.

$$Z_{ind} = j\omega L \tag{5.2}$$

$$Z_{cap} = \frac{1}{j\omega C} \tag{5.3}$$

$$f_R = \frac{1}{2\pi\sqrt{\frac{L_R C_R}{2}}} \tag{5.4}$$

$$Z_R = \sqrt{\frac{2L_R}{C_R}} \tag{5.5}$$

where L_R and C_R is the inductor and the capacitor of the resistance compression topology RCN_R shown in Figure 5.7a, respectively.

Resistance compression can also be achieved by using the LC impedance matching network of Figure 5.6c. A simple manner to obtain the opposite phase response of the input impedance at the operating frequency f_L is to use the same unit network but mirror it by reversing the input and output ports (Figure 5.6d). By placing the networks of Figure 5.6c and Figure 5.6d at the branches of the topology shown in Figure 5.5, resistance compression is also achieved at the resonance. The proposed topology is indicated as RCN_L (Figure 5.7b) and the operating frequency of the resistance compression network (f_L) can be calculated as described above. The operating frequency f_L and the characteristic impedance of the RCN_L topology

(Z_L) are given by (5.6) and (5.7), respectively.

$$f_L = \frac{1}{2\pi\sqrt{2L_L C_L}} \tag{5.6}$$

$$Z_L = \sqrt{\frac{2L_L}{C_L}} \tag{5.7}$$

where L_L is the inductance and C_L the capacitance value of the RCN topology shown in Figure 5.7b.

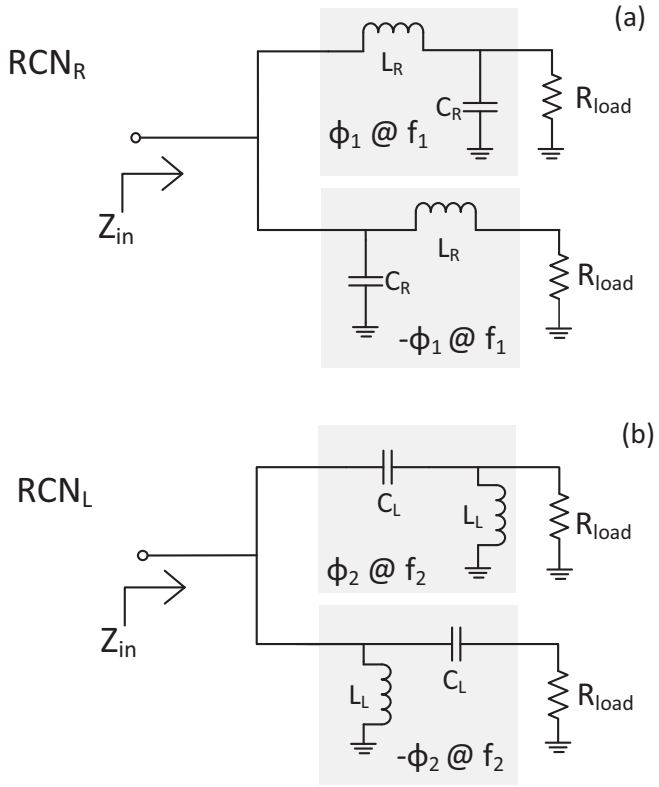

Figure 5.7: RCN topologies: a) RCN_R topology and b) RCN_L topology.

The compression characteristics of the proposed resistance compression networks are now discussed. The resistance compression topology of Figure 5.7a (indicated as RCN_R) operates at 123.9 MHz for L_R=100 nH and C_R=33 pF. It exhibits a compressed input impedance variation with a ratio of 1.7:1 ($|Z_{in}|$ varies from 78 Ω to 134 Ω) for a 10:1 load variation (R_{load} varies from 25 Ω to 250 Ω).

In the same way, the RCN_L operates at 61.9 MHz for L_L=100 nH and C_L=33 pF. For a 10:1 R_{load} variation (from to 25 Ω to 250 Ω), the magnitude of the input impedance of the structure varies from 78 Ω to 134 Ω (a ratio of 1.7:1). The magnitude of the input impedance versus load variations for the RCN_R (at 123.9

MHz) and RCN_L topologies (at 61.9 MHz) are shown in Figure 5.8.

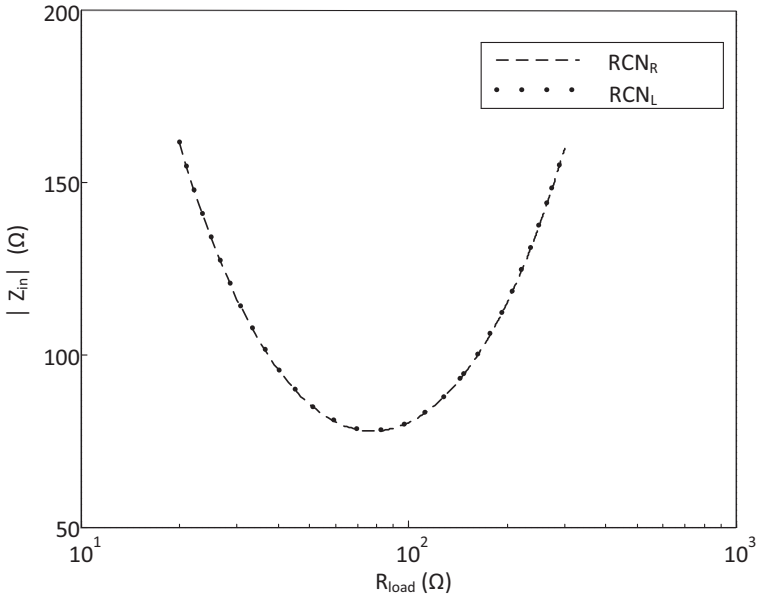

Figure 5.8: Magnitude of the input impedance ($|Z_{in}|$) of the RCN_R and RCN_L topologies versus load variations (R_{load}). The RCN_R topology operates at 123.9 MHz, while the RCN_L operates at 61.9 MHz for the same component values (L_R=L_L=100 nH and C_R=C_L=33 pF).

5.3 Envelope Amplifier Design based on RCN

5.3.1 Hybrid Switching Amplifier Topology

The key idea behind the ET and EER topologies is that the envelope amplifier follows the envelope of the RF input signal and subsequently adapts the power supply of the RF power amplifier, as it has already been discussed in the previous Section. An envelope detector is usually used to track the envelope of the transmitted signal (V_{in}), as it can be seen from Figure 5.9 where a simplified schematic of a power amplifier architecture with a dynamic power supply is shown.

The output of the envelope amplifier (V_{PA}) is connected to the drain/collector of the RF PA and is usually represented as a resistor R_{PA} (typically in the range of 1 Ω - 100 Ω [8]). The equivalent resistor is a time-varying variable that depends on the RF PA efficiency [3] and the output power and can be calculated as

$$R_{PA} = \frac{V_{PA}}{I_{PA}} = \frac{{V_{PA}}^2 \eta}{P_{out}} \tag{5.8}$$

where V_{PA} and I_{PA} is the output voltage and the output current of the envelope amplifier, respectively, η is the efficiency of the RF PA and P_{out} is the output power of the RF PA.

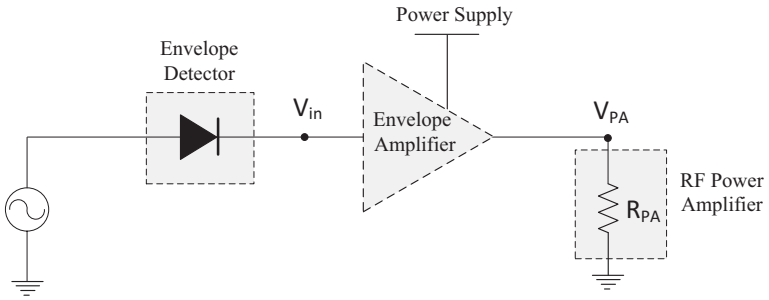

Figure 5.9: Simplified schematic of a power amplifier architecture where the drain/collector of the RF PA is connected to the output of an envelope amplifier that follows the envelope of the modulated input signal.

The topology of the conventional hybrid envelope amplifier is implemented as a hybrid switching amplifier and comprises a linear and a switching stage (Figure 5.10). An operational amplifier is used at the linear stage of the topology, while the switching DC-DC converter is implemented as a boost converter.

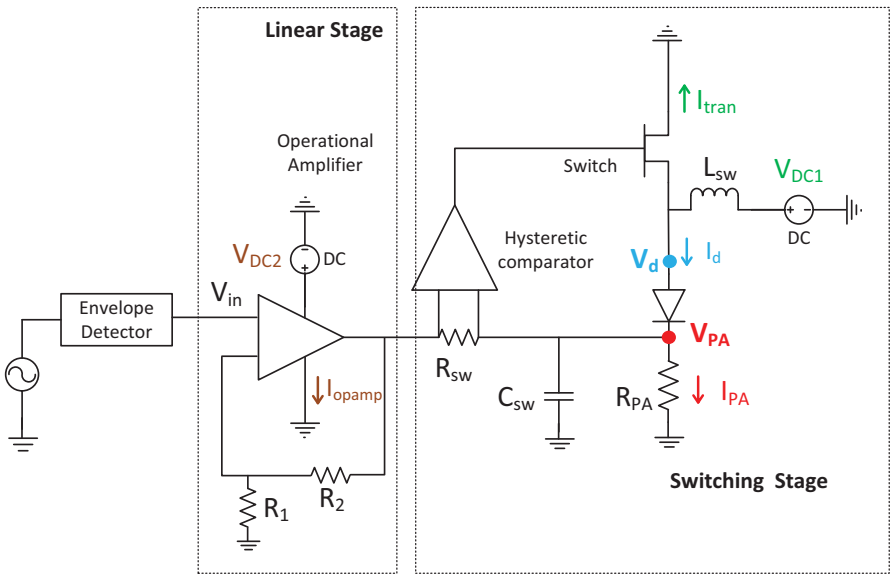

Figure 5.10: Hybrid envelope switching topology.

The schematic of the proposed EA structure with the RCN is shown in Figure 5.11, where the resistance compression network is placed at the switching stage of the proposed topology and the linear stage is identical with the conventional

approach. In particular, two Schottky diodes are placed at the switching stage (Figure 5.11) and a resistance compression network (RCN_R topology) is used as the matching network placed between the switching transistor and the Schottky diodes (Figure 5.11).

One can see that in the implementation of the RCNs that has been described in the previous Section, two separate loads are used for each of the branches of the topology, while in the proposed scheme of Figure 5.11, the RCN shares the same load. Figure 5.12 shows an equivalent simplified schematic of the section of the HSA, where the RCN has been placed.

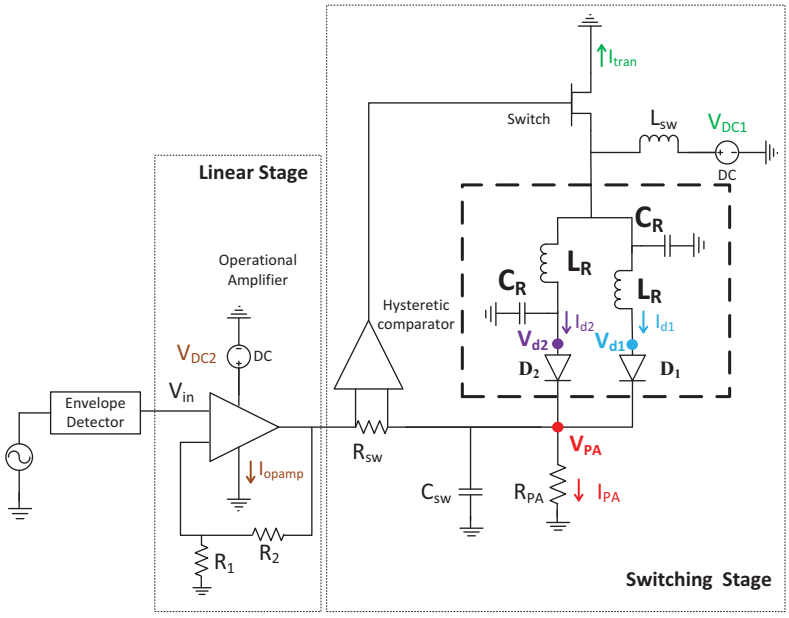

Figure 5.11: Proposed hybrid switching amplifier topology. A resistance compression network is placed at the switching stage of the hybrid topology.

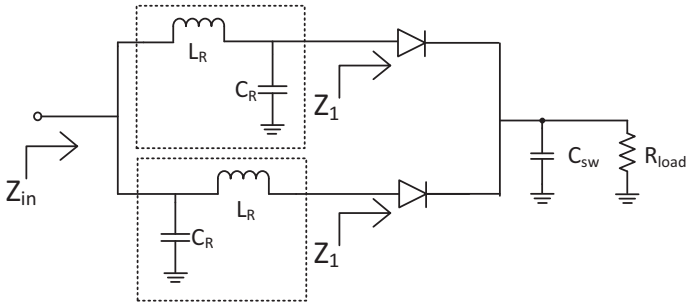

Figure 5.12: Equivalent simplified schematic of the section of the HSA, where the RCN has been placed.

It can be observed that the load of each branch of the RCN is the input impedance of the diode (Z_1) and not the R_{load}. However, variations in the output

load and the input power of the RCN (Figure 5.12) result in an impedance change at the input of the diode and thus an impedance mismatch. The proposed RCN that is placed between the switching transistor and the diodes aims at alleviating the mismatch effect caused by the various operating conditions during its operation.

5.3.2 Calculation of the Envelope Amplifier Efficiency

The design of the hybrid envelope amplifier topologies starts with the selection of the commercial components that are required. A list of the commercial components (operational amplifier, hysteretic comparator, switching transistor and Schottky diodes) that are used for the design of the circuits of Figure 5.10 and Figure 5.11 is shown in Table 5.1.

Component	Type
Operational Amplifier	LMH6639 Op-Amp [109]
Hysteretic Comparator	LMV7219 [110]
Switching Transistor	FDV302 FET Transistor [111]
Schottky Diode	ZLLS400 Packaged Diode [112]

Table 5.1: Commercial components for the implementation of linear and switching stage of the EAs of the conventional HSA (Figure 5.10) and the HSA based on RCN (Figure 5.11).

The behavior of the circuits is analyzed using the transient analysis in Agilent ADS software. The conventional (Figure 5.10) and the proposed topology (Figure 5.11) are designed and optimized for maximum efficiency when operating at 1 MHz. The efficiency of the envelope amplifier [102] can be calculated according to (5.9).

$$\eta_{EA} = \frac{P_{EA}}{P_{EA}+P_{loss}} \tag{5.9}$$

where P_{EA} is the output power of the envelope amplifier and P_{loss} is the total power losses from its operation. The total dissipated power of the topology is calculated as the sum of the dissipated power of the operational amplifier (P_{opamp}), the power losses of the switching transistor (P_{tran}) and the diode losses (P_{diode}). The dissipated

power from the operation of the comparator is not included in the calculation of the efficiency.

The envelope amplifier efficiency can be derived by calculating the envelope amplifier output power and the component power losses for one period of the signal (1 MHz). The dissipated power of the switching transistor is calculated as the supply voltage of the device (V_{DC1} in Figure 5.10 and Figure 5.11) multiplied by the current I_{tran} (see Figure 5.10 and Figure 5.11) according to

$$P_{tran} = V_{DC1}\, I_{tran} \tag{5.10}$$

In the same way, the dissipated power of the linear stage (P_{opamp}) is calculated as the supply voltage of the operational amplifier (V_{DC2} in Figure 5.10 and Figure 5.11) multiplied by the current I_{opamp} (see in Figure 5.10 and Figure 5.11) as

$$P_{opamp} = V_{DC2}\, I_{opamp} \tag{5.11}$$

The power losses of the diode (P_d) are calculated as the voltage drop across the diode terminals (V_d-V_{PA} in Figure 5.10) multiplied by the diode current (I_{d1} in Figure 5.10) as

$$P_d = (V_d - V_{PA})\, I_d \tag{5.12}$$

In the case of the proposed topology (Figure 5.11), the total power losses from the operation of the diodes should be taken into account for the calculation of the efficiency. In particular, the total losses from the diode operation is given as

$$P_{loss} = P_{tran} + P_{opamp} + P_d \tag{5.13}$$

where V_{d1}-V_{PA} and V_{d2}-V_{PA} (Figure 5.11) is the voltage drop across the diode D_1 and D_2, respectively, and I_{d1} and I_{d2} (Figure 5.11) indicate the current of D_1 and D_2. The total power losses of the HSA shown in Figure 5.10 and Figure 5.11 are given by

$$P_d = (V_{d1} - V_{PA})\, I_{d1} + (V_{d2} - V_{PA})\, I_{d2} \quad (5.14)$$

After the calculation of P_{loss}, the average efficiency of the EA can be estimated by (5.9).

In order to be able to evaluate the performance of the hybrid envelope amplifier topologies in terms of measurements, the current should be measured at various nodes of the circuit. For this reason, 1 Ω resistances are placed at different nodes of the circuit in order to calculate the current as the voltage difference across the resistance. The modified conventional and proposed envelope amplifier topologies are shown in Figure 5.13 and Figure 5.14, respectively.

In particular, a resistor (1 Ω) is placed at the ground of the operational amplifier and at the ground of the switching transistor in order to measure I_{tran} and I_{opamp}, respectively. The current that goes to the ground due to the operational amplifier (I_{opamp}) and to the switching transistor (I_{tran}) operation is calculated as the voltage drop across the 1 Ω resistances.

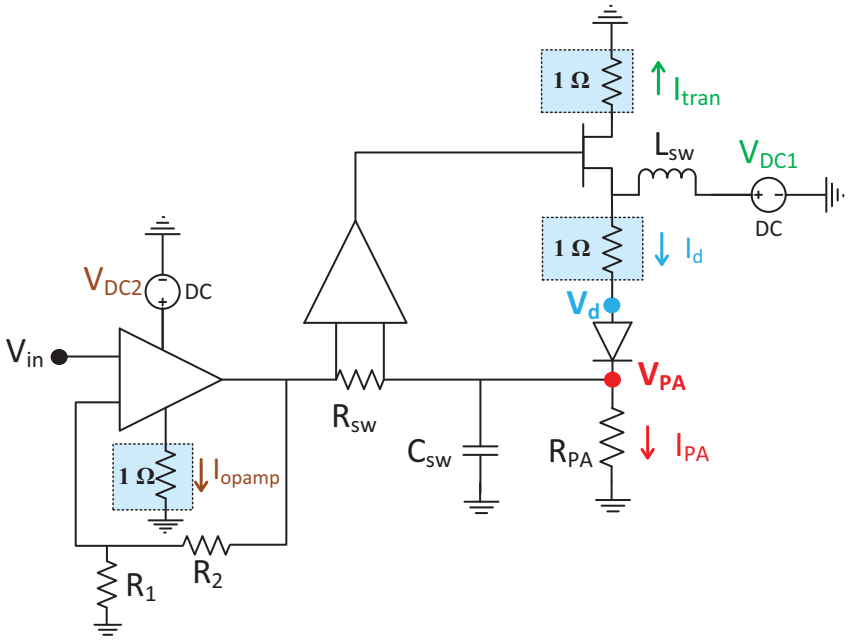

Figure 5.13: Switching amplifier topology including three 1 Ω resistors for measurement purposes.

The current that enters in the diode of Figure 5.10 (I_d) and in the diodes of Figure 5.11 (I_{d1} and I_{d2}) are also necessary for the calculation of the total power losses. For this reason, a 1 Ω resistor is placed at the input of the diode of Figure 5.10 in order to measure the voltage drop across the resistor and thus, calculate the

diode current (I_d). In the same way, two resistors (1 Ω) are placed at the input of the D_1 and D_2 (Figure 5.11) in order to estimate I_{d1} and I_{d2}.

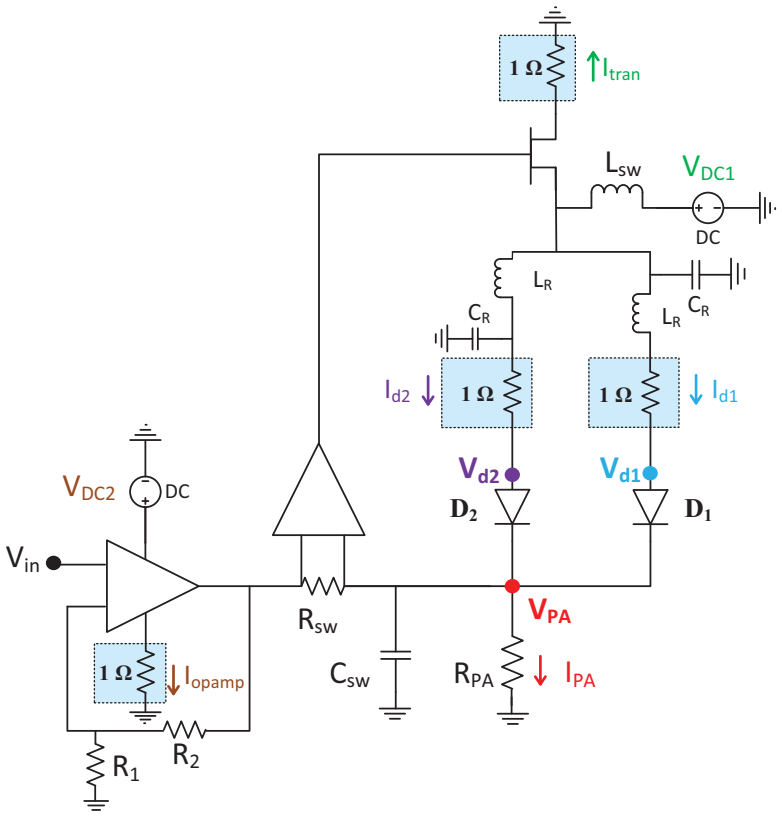

Figure 5.14: Proposed hybrid switching amplifier topology including four 1 Ω resistors for measurement purposes.

5.3.3 Design of the RCN based Envelope Amplifier

The design of the RCN based envelope amplifier starts with the selection of the RCN topology. The RCN_R topology is chosen for this design, as it has already been shown in Figure 5.14. The initial inductor and capacitor values are obtained by defining the characteristic impedance and the operating frequency of the RCN. After defining these values, the inductor and capacitor values are calculated using (5.4) and (5.5). This procedure leads to the following components values for the RCN_R topology: L_R=16.4 uH and C_R=2.8 nF.

Then, the obtained values are placed in the topology shown in Figure 5.12 and the input impedance of the RCN is investigated for different operating conditions using the LSSP analysis in Agilent ADS software. Figure 5.15 shows how the real and imaginary part of the input impedance of the topology is affected for different input power levels and output loads. As it can be observed from Figure 5.15a, the

real part of the input impedance of the network remains almost constant for a wide range of R_{load} values (from 10 Ω to 150 Ω). In the same way, the imaginary part of the input impedance (Figure 5.15b) suffers small variations for the same input power and load conditions.

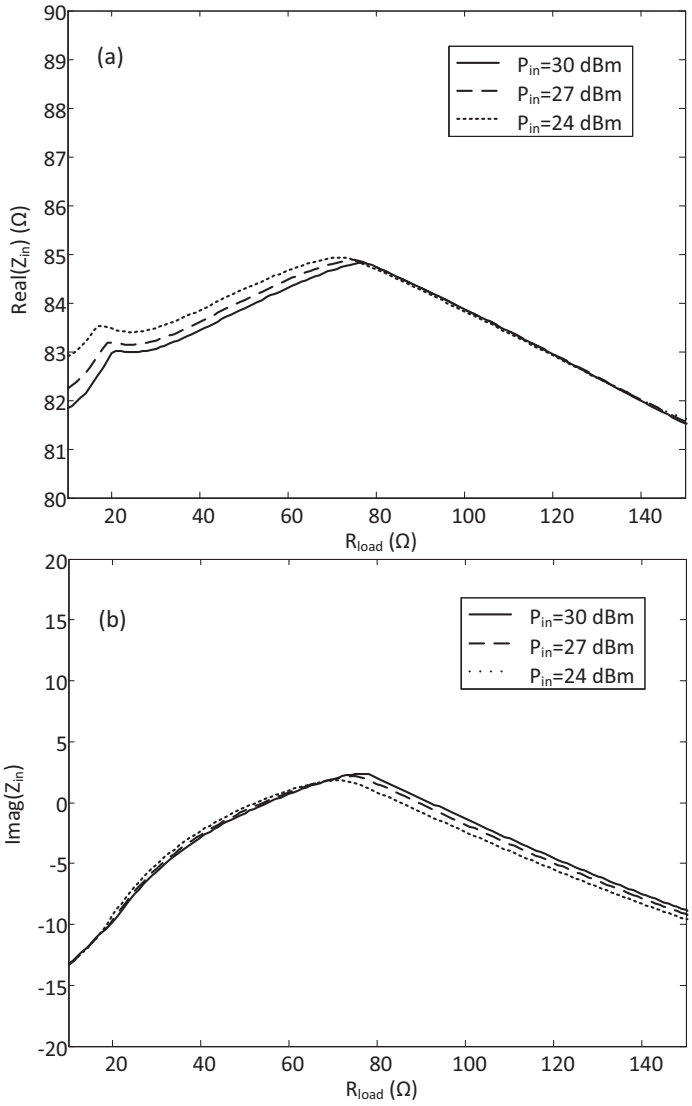

Figure 5.15: Real and Imaginary part of the input impedance of the RCN shown in Figure 5.11 versus R_{load} for various input power levels at 1 MHz.

After the design of the RCN for the proposed EA topology (Figure 5.14), the transient simulation in Agilent ADS has shown that maximum efficiency is obtained for R_1=1 kΩ, R_2=1 kΩ, R_{sw}=1 Ω, L_{sw}=8.2 uH and C_{sw}=8 nF. In the same way, using (5.9) - (5.13) and the transient analysis in Agilent ADS software, it is shown that the conventional HSA achieves maximum efficiency for R_1=1 kΩ, R_2=1 kΩ, R_{sw}=1 Ω, L_{sw}=3.3 uH and C_{sw}=2.2 nF.

The performance of the conventional and the proposed circuit is evaluated in terms of simulation for different conditions that affect the operation of the envelope amplifier. Initially, the EA circuits are simulated for different input signals that are characterized with a DC level (V_{dclev}) of 1.5 V and a peak to peak voltage (V_{pp}) of 1.6 V when the switching transistor is biased with V_{DC1}= 3 V. The simulated results that are shown in Figure 5.16a show that the proposed design is more efficient for the specific operating conditions.

Then, the proposed EA circuit is tested for the same signal and output load range, but for a different supply voltage of the transistor (V_{DC1}=2.7 V) in order to test the performance of the circuits for different power levels at the input of the RCN. The obtained simulated results of Figure 5.16b show that the RCN based envelope amplifier is more efficient for these operating conditions.

Finally, the hybrid envelope amplifier circuits are characterized for a different input signal of V_{dclev}=1.55V and V_{pp}=1.4 V and with a supply voltage of the switching transistor of V_{DC1}=3.2 V. The obtained efficiency is shown in Figure 5.16c. From the simulated results of Figure 5.16a - Figure 5.16c, it can be noticed that the proposed design exhibits higher efficiency for a wide range of operating conditions if compared with the conventional EA topology.

5.3.4 Implementation and Characterization of the Hybrid Envelope Amplifier Topologies

The envelope amplifier circuits are fabricated on 30 mil Arlon 25N substrate (ε_r=3.38 and tanδ=0.0025) using an LPKF Protomat C100/HF circuit board plotter [39]. The photos of the fabricated prototypes are shown in Figure 5.17. Figure 5.17a shows the conventional envelope amplifier topology, while in Figure 5.17b it is shown the proposed structure (with the RCN). Both prototypes are characterized in terms of measurements. The prototype of the conventional and the proposed topology has a total size of 3.8 cm x 2.8 cm and 4.8 cm x 4.5 cm, respectively.

The prototypes are tested for different input signals and load values (R_{PA}) for V_{DC1}=3 V. The input signal of the envelope amplifier is a sinusoidal with a DC level and is generated using the Agilent 33250A arbitrary waveform generator

(AWG). During the measurements, the voltage waveforms are measured using the high impedance probes of a mixed signal oscilloscope (Agilent M506054A).

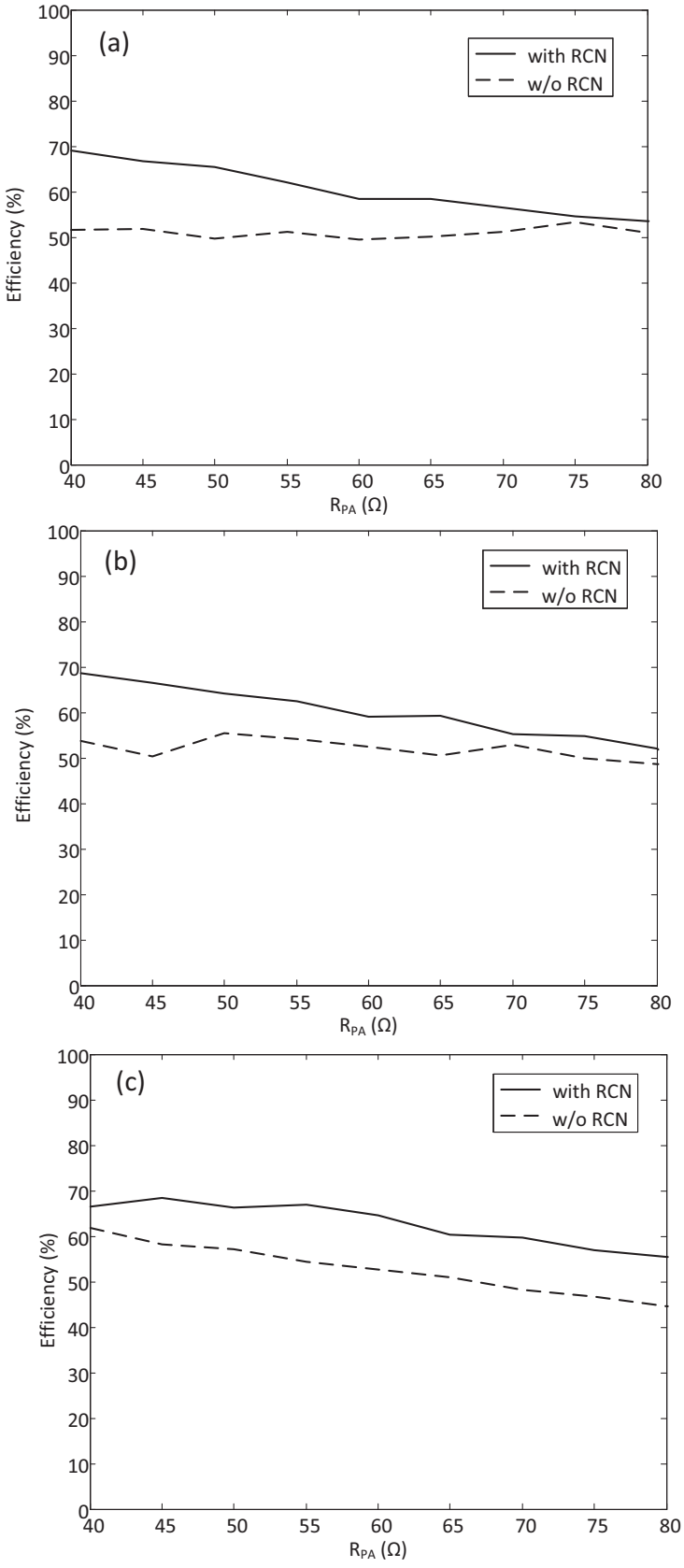

Figure 5.16: Simulated efficiency of the conventional design (Figure 5.10) and the proposed structure (Figure 5.11) at 1 MHz versus output load value (R_{PA}) for different operating conditions: a) V_{dclev}=1.5V, V_{pp}=1.6 V and V_{DC1}=3 V, b) V_{dclev}=1.5V, V_{pp}=1.6 V and V_{DC1}=2.7 V and c) V_{dclev}=1.55V, V_{pp}=1.4 V and V_{DC1}=3.2 V.

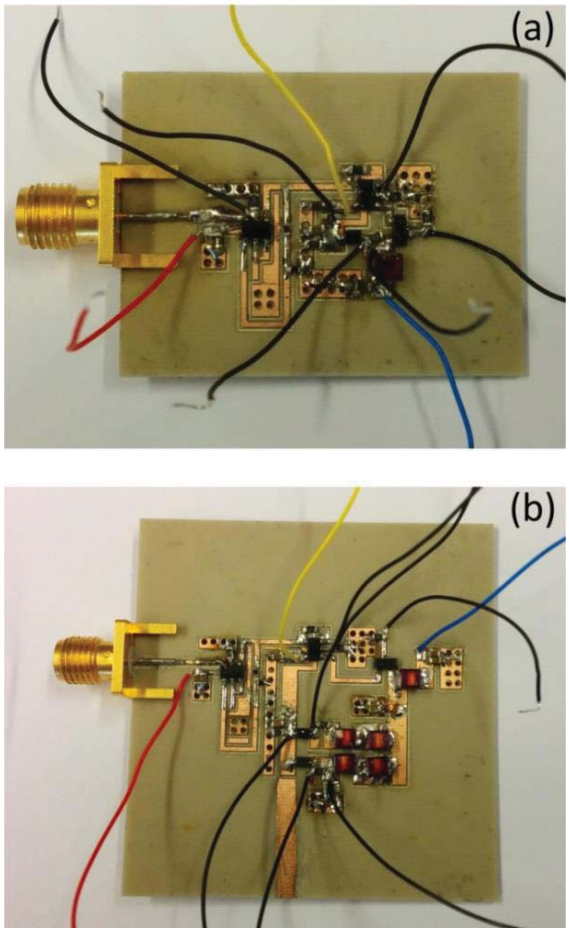

Figure 5.17: Fabricated prototypes of: a) a conventional envelope amplifier (without the resistance compression network) with a total size of 3.8 cm by 2.8 cm and b) an envelope amplifier based on a resistance compression network with a total size of 4.8 cm by 4.5 cm.

When the envelope amplifier operates with an input signal with V_{dclev}=1.53V and V_{pp}=1.6V and an output load of R_{PA}=39 Ω, the proposed envelope amplifier circuit exhibits a measured average efficiency of 67.2 % at 1 MHz. The waveforms of the input signal, the output signal and the output of the comparator are shown in Figure 5.18. The circuit exhibits higher efficiency if compared with the conventional design that shows an efficiency of 57.4 % for the same operating conditions, as Table 5.3 shows.

Both circuits are also tested with a different input signal of V_{dclev}=1.35 V and V_{pp}=0.85 V and an output load of 33 Ω at 1 MHz. In this case, the proposed design shows an efficiency of 72.1 %, while the conventional design exhibits an efficiency of 55.6 % as it is shown in Table 5.3. The measurements show that the proposed design shows improved performance due to the reduced sensitivity to input power and load variations if compared with a conventional envelope amplifier design.

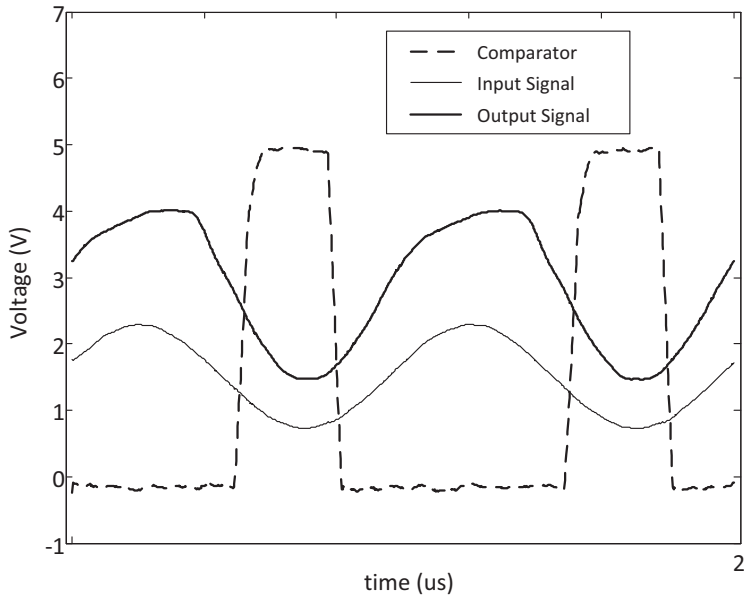

Figure 5.18: Measured input and output signal waveforms, along with the comparator output for the envelope amplifier based on RCN at 1 MHz.

	Conventional design (Figure 5.10)	Proposed design (Figure 5.11)
η_{EA}	57.4 %	67.2 %

Table 5.2: Efficiency of the conventional and proposed design for an input signal of V_{dclev}=1.53V/V_{pp}=1.6V and an output load of R_{PA}=39 Ω at 1 MHz.

	Conventional design (Figure 5.10)	Proposed design (Figure 5.11)
η_{EA}	55.6 %	72.1 %

Table 5.3: Efficiency of the conventional and proposed design for an input signal of V_{dclev}=1.53V/V_{pp}=1V and an output load of R_{PA}=33 Ω at 1 MHz.

5.4 Chapter Summary

In this Chapter, novel matching networks that show reduced sensitivity to impedance variations have been proposed and discussed. The proposed resistance compression networks are used as part of the design of an envelope amplifier that shows higher efficiency for various operating conditions if compared with a conventional hybrid envelope amplifier design.

Chapter 6

Dual-Band Resistance Compression Networks for Improved Rectifier Performance

6.1 Introduction

Microwave circuits are usually optimized for specific operating conditions, including frequency of operation, input power level and fixed output load. In a plethora of electronic circuits, such as power amplifiers and electromagnetic energy harvesters, the device has to operate with varying input power level and output loads. Such environmental changes result in a deviation from the nominal operating conditions and in an impedance mismatch of the circuit. In rectifier circuits, output load and input power level variations produce an impedance change at the input of the diode and thus, degraded performance.

Rectifiers are fundamental components for many microwave applications, such as power amplifier architectures and energy harvesting scenarios. In particular, rectifiers can be applied in outphasing power amplifier topologies that include a power recycling network to harvest the dissipated power in the power combiner [9]. In conventional outphasing power amplifier topologies, the isolator

resistance of the topology achieves maximum efficiency only at maximum output power level. When the power amplifier operates with high peak-to-average power ratio input signals, the efficiency of the topology degrades due to the isolator resistor losses at the low-power signals. In [9], the isolation resistance of the power combiner has been replaced with a rectifier that harvests the dissipated power from its operation. The proposed rectifier has shown reduced sensitivity to environmental changes and has successfully improved the isolation of the RF power amplifiers (Figure 6.1a). The obtained results have demonstrated that the resulting 48 MHz PA shows high system efficiency and linearity due to the resistance compressed rectifier. However, it is a major issue to design such multi-band rectifiers based on Resistance Compression Networks (RCNs) for the implementation of multi-band PAs architectures.

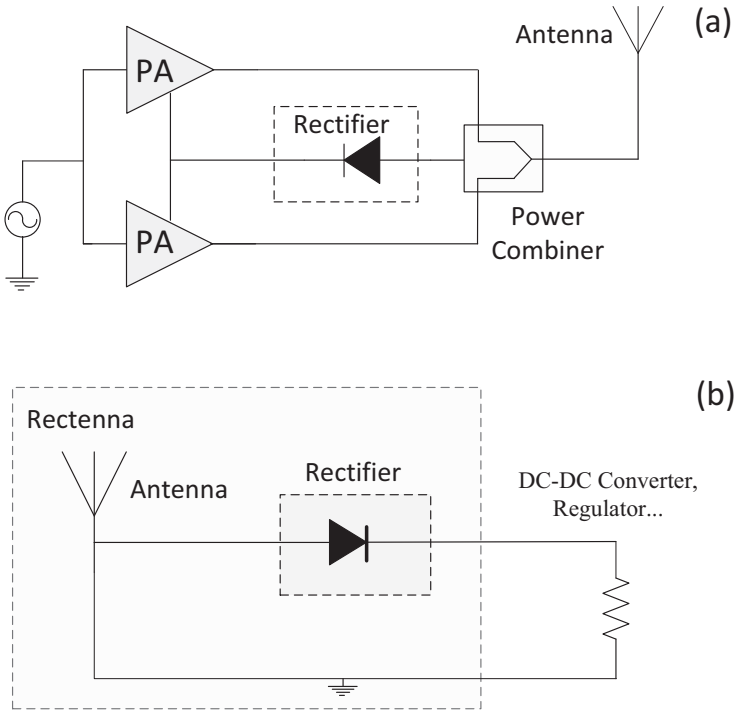

Figure 6.1: Application of rectifier circuits in a) an outphasing power amplifier topology with a power recycling network and b) energy harvesting applications.

In the same way, rectifiers are used in RF energy harvesting applications, as part of a wireless energy harvester, in order to efficiently transform the harvested power to useful DC power [113]. In such applications, the input power is not constant since the availability of the harvested power depends on the surrounding conditions, such as the propagation environment (Figure 6.2). A variation in the

available power at the input of the rectenna results in a change of the input impedance of the nonlinear rectifying device and thus a deviation from the nominal operating conditions that imply a reduced harvested power level.

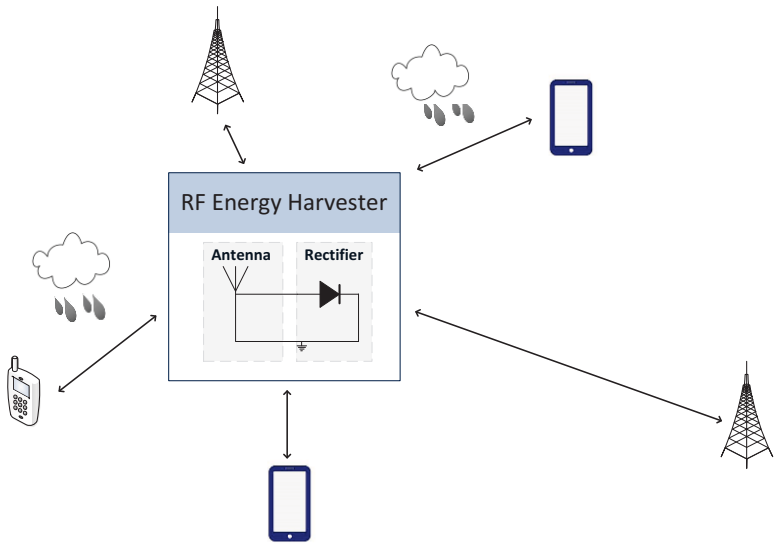

Figure 6.2: Schematic of RF energy harvesting setup where the input power level varies depending on the application, the operating frequency band and the propagation environment.

The output of the rectenna is usually connected to a varying load, such as DC-DC converter or regulator circuit, as Figure 6.1b shows. The load variation due to the time-varying operating conditions of the circuitry also results in an input impedance change in the rectifying device and thus, degraded performance. According to [114], maximum RF-DC conversion efficiency is achieved for a specific selection of output resistance value, while the optimum load varies versus frequency. The design of multi-band and broadband rectennas with reduced sensitivity to the surrounding environment conditions is an even more challenging task for increasing the harvested power level in energy harvesters.

Since ambient electromagnetic energy is available in low levels, the design of efficient energy harvesters that can harvest simultaneously the ambient energy from different frequency bands is desirable to achieve enough harvested DC power. Multi-band and broadband rectenna circuits have already been proposed in the literature [115]-[124]. In [125], the design and characterization of various rectifiers based on a single low threshold Schottky diode has been presented. A broadband rectifier in the frequency band of 800 MHz - 2.5 GHz has been

implemented, showing a maximum measured RF-DC conversion efficiency of 8 % for P_{in}=-20 dBm. A dual-band rectifier that is able to achieve RF- DC conversion efficiency around 15 % at GSM-850 and GSM-1900 for an input power of -20 dBm is also proposed. An additional dual-band rectifier operating at GSM-850 and ISM 2.45 GHz with RF-DC conversion 10 % – 12 % at both frequency bands (P_{in}=20 dBm) has also been introduced.

In [126], a four stage rectifier has been designed for the implementation of a triple-band rectifier. The maximum measured RF-DC conversion efficiency of the design is 80 % (P_{in}=10 dBm) and 47 % (P_{in}=8 dBm) at 940 MHz and 1950 MHz, respectively. A peak RF-DC conversion efficiency of 43 % is measured at 2.44 GHz for an input power level of 16 dBm.

A dual-band rectifier based on a Schottky diode for wireless power transfer (WPT) application has been introduced in [127], where the measurement results have shown that a peak RF-DC conversion efficiency of 66.8 % and 51.5 % is achieved at 2.45 GHz and 5.8 GHz for an input power level of 10 mW.

In order to reduce the sensitivity of the rectifier circuits versus load and input power variations, novel circuits have been recently proposed in the literature [10] namely resistance compression networks. These networks achieve small variations in the input impedance of the rectifier circuit under large variations of input power levels and output load values. So far, resistance compression networks operating at a single frequency have been proposed in the literature [9], [10], [105]-[108].

In this Chapter, the design of a dual-band resistance compression network based rectifier with reduced sensitivity to input impedance and output load variations is proposed [128]. In particular, two RCN topologies are introduced and their behavior is presented in detail. An analytical equation about the input impedance of the rectifying device is mathematically derived to show the dependence of the input impedance of the diode to the input RF amplitude and output DC voltage. A performance comparison between two rectifier topologies based on different RCNs is made, where it is shown that improved performance is achieved by cascading two unit cells at each branch of the RCN based rectifier. A detailed analysis of the rectifier design is also presented with an adequate set of measurements showing that the proposed rectifier shows a good RF-DC conversion efficiency with minimized sensitivity to input power and load variations.

The outline of this Chapter is as follows. In Section 6.2, the properties of the dual-band resistance compression networks are described. Section 6.3 presents some considerations for the design of the proposed topology along with the performance evaluation of the RCN based rectifier in comparison with a conventional envelope detector rectifier. In Section 6.4, the experimental results of the fabricated 915 MHz/2.45 GHz RCN based rectifier are presented showing reduced sensitivity to input power and load variations. Finally, the conclusions of the Chapter are presented in Section 6.5.

6.2 Dual-Band Resistance Compression Network Theory

A resistance compression network is a matching network that reduces the sensitivity of electronic circuits (such as rectifiers) to impedance variations due to input power and output load changes, as it has been already presented in Chapter 5. The basic structure of a resistance compression network consists of two branches that exhibit opposite phase response of the input impedance (φ and –φ respectively) at the operating frequency (f) as Figure 6.3a shows. In this topology, the input impedance of the network (Z_{in}) suffers small variations under large variations of the real load values.

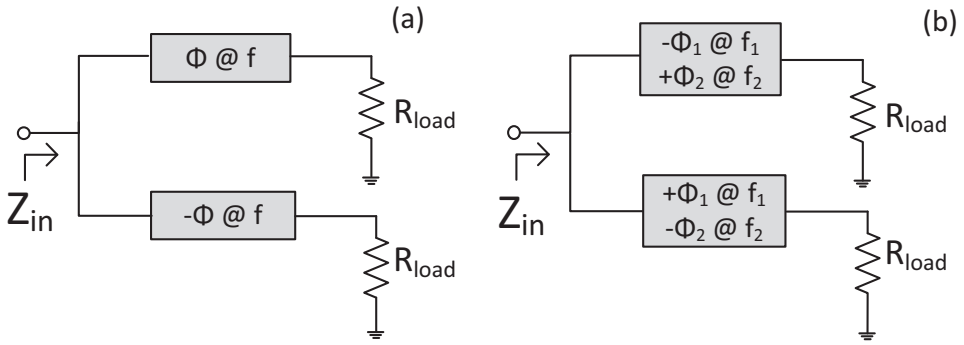

Figure 6.3: a) Resistance compression networks operating at a single frequency. Each branch exhibits opposite phase response (φ and -φ) at the operating frequency (f) and b) Dual-band RCNs.

Taking into account the operating principles of a RCN, dual-band and in general multi-band RCN should similarly exhibit opposite phase response at an arbitrary set of frequencies, as Figure 6.3b depicts for the dual-band case. A way to achieve the necessary phase conditions can be the use of bandpass unit circuit cells consisting of series and shunt LC network (Figure 6.4a) [56].

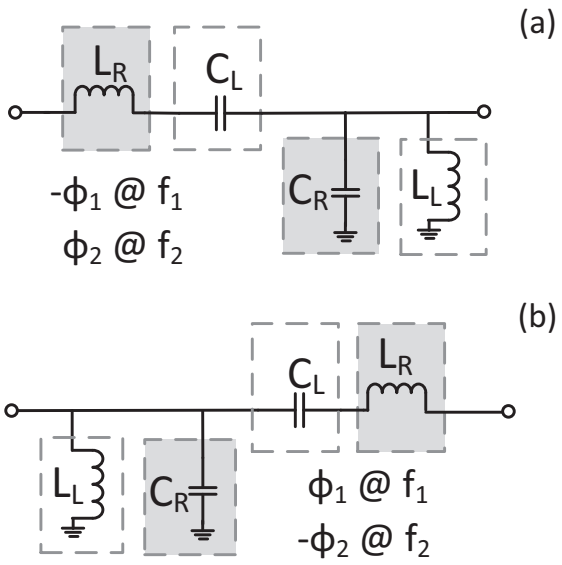

Figure 6.4: a) Unit circuit cell consisting of a series and shunt LC network and b) Rearranged circuit cell (the same network as Figure 6.4a with reversed input and output ports).

The unit cell shown in this figure can be used as a dual-band matching network operating at an arbitrary set of frequencies (f_1 and f_2). In particular, at the low operating frequency (f_1), the discrete elements C_R and L_R tend to be open and short, respectively. In the same way, C_L and L_L tend to be short and open at the high operating frequency (f_2).

The unit cell shown in Figure 6.4a exhibits a negative phase response ($-\varphi_1$) at the low operating frequency (f_1) and a positive phase response (φ_2) at the higher frequency (f_2). A simple manner to obtain the opposite phase response in the two branches is to use the same unit network but mirror it by reversing the input and output ports (Figure 6.4b). The unit cell of Figure 6.4 shows opposite phase response at the two selected frequencies if compared to the unit cell in Figure 6.4a: φ_1 at the low frequency f_1 and $-\varphi_2$ at the high frequency f_2. A dual-band resistance compression effect can be achieved by placing the conventional and reversed unit cells into the two branches of the RCN, as Figure 6.5 depicts (topology RCN_{1CELL}).

As it has been previously described, dual-band resistance compression can be achieved by using a single unit cell at each branch of the resistance compression network topology (RCN_{1CELL} in Figure 6.5). A resistance compression can also be achieved by cascading identical unit cells at each branch of the network, as shown in Figure 6.6. The structure of Figure 6.6 will be referred to as RCN_{2CELLS}. Such a structure offers more degrees of freedom in defining the resistance compression properties.

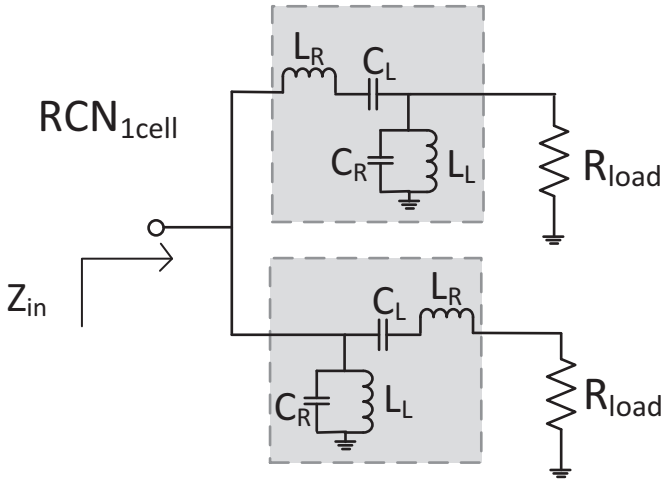

Figure 6.5: Dual-band resistance compression network implemented with a single circuit cell at each branch. The proposed topology is indicated as RCN_{1CELL}.

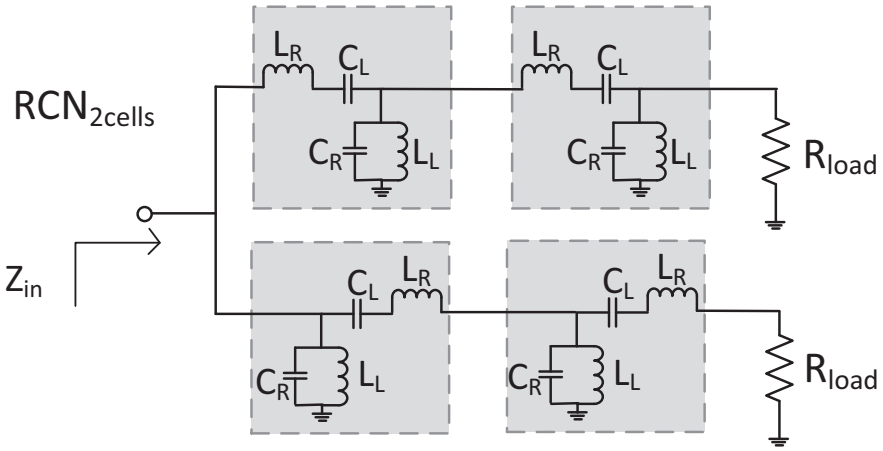

Figure 6.6: Dual-band resistance compression network. The proposed topology (with two unit cells at each branch of the network) is indicated as RCN_{2CELLS}.

The input impedance (Z_{in}) of the networks shown in Figure 6.5 and Figure 6.6 can be derived by using the equivalent model in Figure 6.7b of the unit cell of Figure 6.7a, where the series elements are represented by an impedance Z and the parallel elements by an admittance Y. Then, the dual-band RCN of the topology RCN_{1CELL} (Figure 6.5) can be represented as a combination of impedances and admittances as Figure 6.7a shows.

The same applies for the topology of RCN_{2CELLS} (Figure 6.6). The impedance and admittance of a unit cell are given by (6.1) and (6.2), respectively [56].

$$Z = j\left(\omega L_R - \frac{1}{\omega C_L}\right) \tag{6.1}$$

$$Y = j\left(\omega C_R - \frac{1}{\omega L_L}\right) \tag{6.2}$$

Straightforward calculations result in the estimation of the input impedance of such networks. For instance, the Z_{in} of the RCN_{1CELL} topology is given by (6.3) as a combination of Z, Y and R_{load}.

$$Z_{in} = \frac{(R_{load}+Z)(R_{load}+Z+R_{load}ZY)}{(R_{load}{}^2ZY^2+2R_{load}{}^2Y+R_{load}Z^2Y^2+4R_{load}ZY+2R_{load}+Z^2Y+2Z)} \tag{6.3}$$

In order to demonstrate the properties of the proposed topologies (RCN_{1CELL} and RCN_{2CELLS}) two networks are designed to have dual-band operation at 915 MHz and 2.45 GHz. The compression ratio of the input impedance is defined as the ratio between the largest and smallest values of $|Z_{in}|$ and is compared with the ratio between the largest and smallest values of the corresponding R_{load} variations, as it is shown in Figure 6.8 and Figure 6.9.

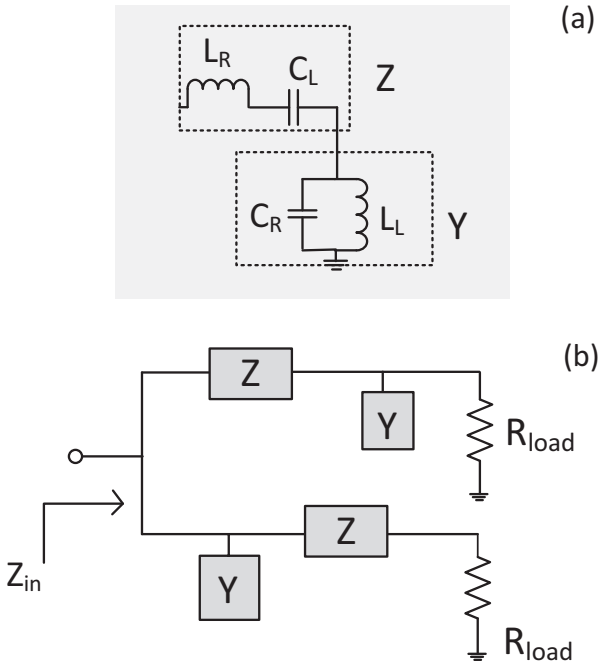

Figure 6.7: a) Equivalent network for an ideal unit cell represented as a set of complex impedance (Z) and admittance (Y) and b) Equivalent network of the dual–band RCN (RCN_{1CELL}) in terms of complex impedances.

The magnitude of the input impedance of the networks ($|Z_{in}|$) is plotted versus the output load (R_{load}) for both operating frequencies. Figure 6.8 and Figure 6.9 also show the percentage of the delivered power from the 50 Ω source to the

input of the rectifier circuit showing explicitly how the matching is affected for each R_{load} value. The values of the elements used to obtain the compression characteristics of the RCN topologies are shown in Table 6.1.

	RCN_{1CELL} topology	RCN_{2CELLS} topology
L_R	7.15 nH	5.55 nH
C_R	3 pF	1.14 pF
L_L	4 nH	10.15 nH
C_L	1.5 pF	2 pF

Table 6.1: Component values used to obtain the data at Figure 6.8 and Figure 6.9.

The compression of the RCN_{1CELL} topology (Figure 6.5) is shown in Figure 6.8. For an R_{load} range from 24.2 Ω to 242 Ω (a ratio of 10:1 around the central compression point), the $|Z_{in}|$ varies from 73 Ω to 127 Ω (a ratio of 1.74:1) at 915 MHz. In the same way, a 10:1 variation of R_{load} (from 21.2 Ω to 212 Ω) results in 1.74:1 variation of $|Z_{in}|$ (66.7 Ω to 116 Ω) at 2.45 GHz. Thus, the same compression ratio is achieved for both frequencies around the center compression point.

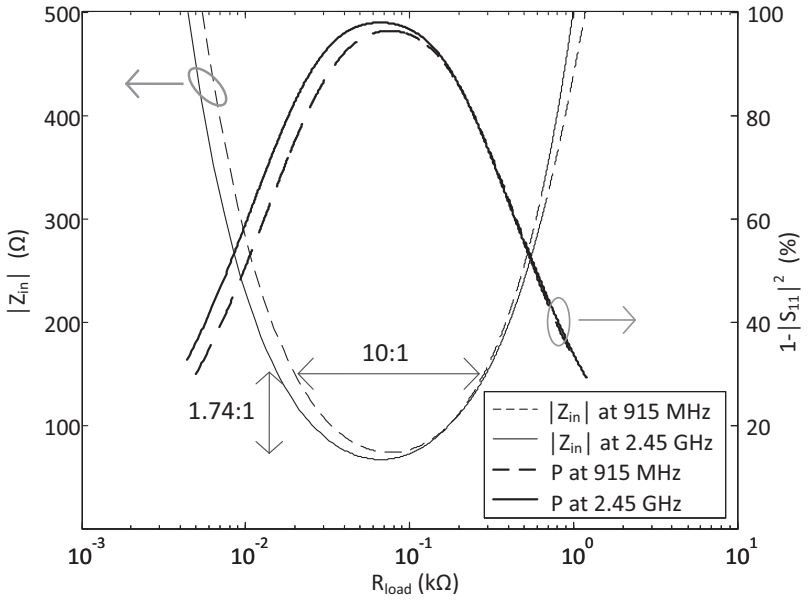

Figure 6.8: Magnitude of the input impedance ($|Z_{in}|$) and percentage of the delivered power to the input of the rectifier for the RCN_{1CELL} topology (Figure 6.5) versus load variations (R_{load}).

The compression characteristics of the RCN_{2CELLS} topology are shown in Figure 6.9. The center value of the compression curve of RCN_{2CELLS} at 915 MHz

(2.45 GHz) corresponds to the values of R_{load}=189 Ω and $|Z_{in}|$=32.2 Ω (R_{load}=179 Ω and $|Z_{in}|$=31 Ω). A 10:1 variation of R_{load} values (from 60 Ω to 600 Ω) is compressed to 1.74:1 ratio (from 32.2 Ω to 56 Ω) at $|Z_{in}|$ at 915 MHz. Finally, the same compression ratios are achieved for a variation of R_{load} from 57 Ω to 570 Ω (a ratio of 1:10) to the compressed variation of $|Z_{in}|$ from 31 Ω to 54 Ω (1:1.74) at 2.45 GHz.

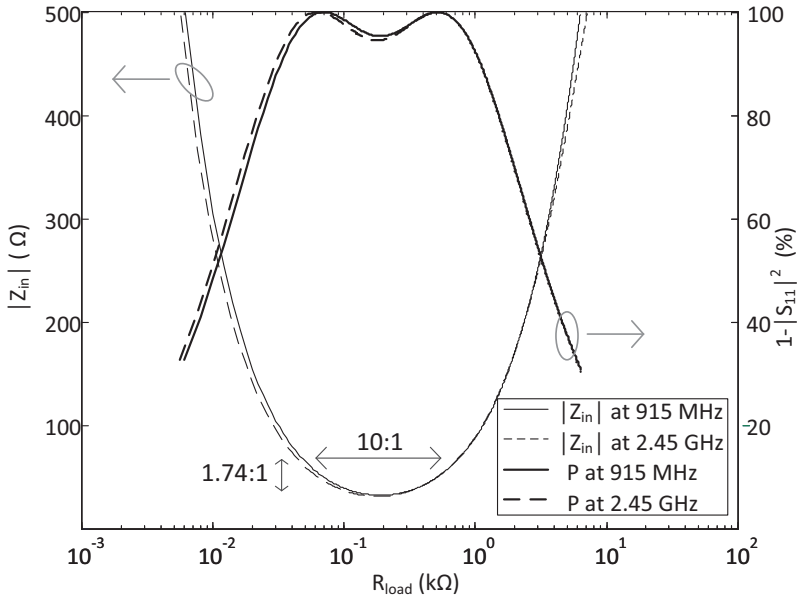

Figure 6.9: Magnitude of the input impedance ($|Z_{in}|$) and percentage of the delivered power to the input of the rectifier for the RCN_{2CELLs} topology (Figure 6.6) versus load variations (R_{load}).

6.3 Dual-Band RCN based Rectifier

6.3.1 Design Considerations for the Dual-Band RCN based Rectifier Topology

In rectifier circuits, output load and input power level variations result in an impedance change at the input of the diode and thus, degraded performance. Therefore, resistance compression network topologies have been considered, such as the ones in the previous Section, to be used in the design of rectifier circuits.

In this Section, the dual-band resistance compression networks are placed as the matching network located between the input of a Schottky diode and a 50 Ω

source. Figure 6.10a and Figure 6.10b show the RCN_{1CELL} and RCN_{2CELLS} topologies presented in the previous Section when applied for the design of a dual-band rectifier.

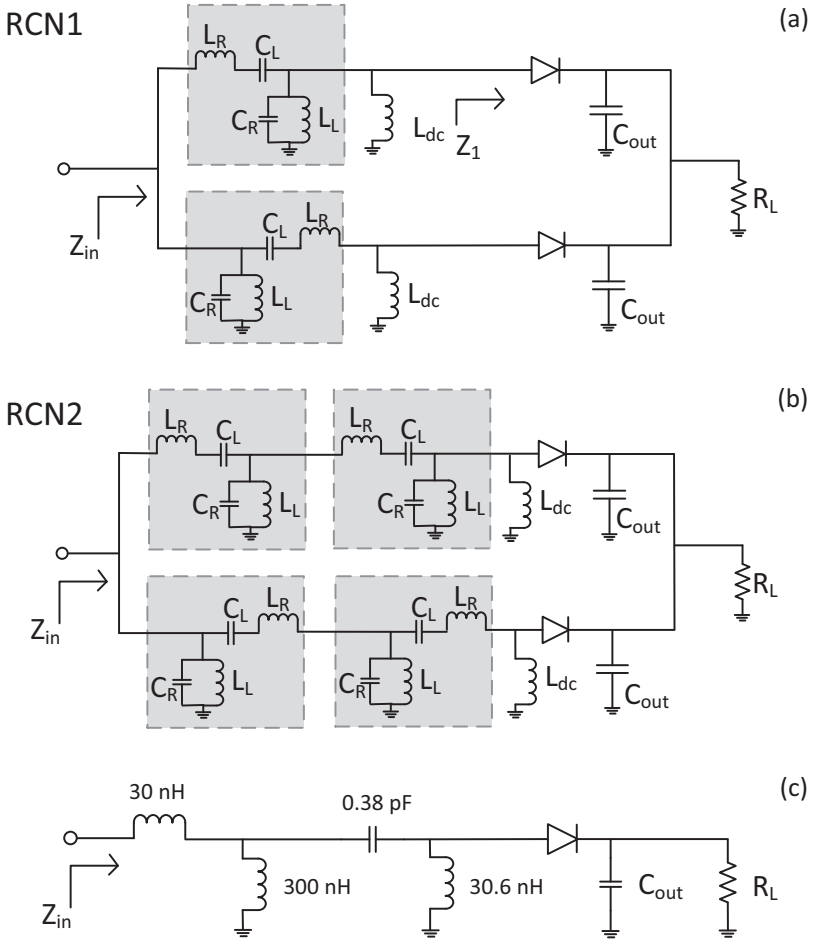

Figure 6.10: Schematics of the simulated dual-band rectifiers: a) proposed RCN based rectifier with RCN_{1CELL} topology, b) proposed RCN based rectifier with RCN_{2CELLS} topology, c) conventional envelope detector topology.

One can see that in the proposed implementations of the RCN based rectifier (Figure 6.10a and Figure 6.10b) there is only one output load if compared with the traditional implementations of RCN where two separate loads are used for each of the branches (Figure 6.5 and Figure 6.6). However it has to be considered that in the RCN based rectifier topologies, the loads of the RCN are the Schottky diodes of the rectifier. The capacitances that are placed at the output of the rectifier isolate the two branches at RF frequencies, which lead to a similar structure to the one in Figure 6.5 and Figure 6.6 where the loads are the complex input impedances of the diodes (Z_1).

The electrical behavior of the diode can be expressed as complex impedance (Z_1). The formula for the calculation of Z_1 derives from the analysis of the electrical behavior of the proposed structures (Figure 6.10a and Figure 6.10b). Let us assume a sinusoidal input signal equal to v_1=Ecos(ωt), where E is the amplitude and ω the frequency of the input signal (Figure 6.11a).

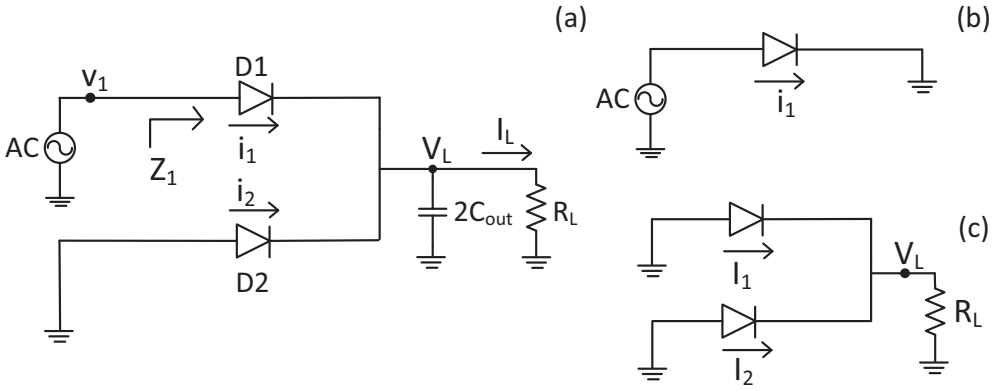

Figure 6.11: a) Simplified circuit topology of the proposed rectifier topology, b) equivalent circuit of the diode (D1) at RF and c) DC equivalent circuit of the proposed structure.

The current through the diodes D1 and D2 as a function of the voltage across the terminals of the diodes are given by (6.4) and (6.5), respectively.

$$i_1 = I_{s1}\left(e^{\frac{v_1 - V_L}{V_t}} - 1\right) \tag{6.4}$$

$$i_2 = I_{s2}\left(e^{\frac{-V_L}{V_t}} - 1\right) \tag{6.5}$$

where V_t is the thermal voltage and V_L (V_L=$I_L R_L$) is the output DC voltage of the circuit, assuming that C_{out} is ideal and provides a perfect RF short at the output of the diodes.

At RF frequencies the two branches of the proposed structure are isolated because of the DC capacitor at the output of the network. Considering only the behavior of a single diode at RF (Figure 6.11a), the diode current (i_1) can be calculated (taking into account the voltage drop across the diode that is equal to Ecos(ωt)-V_L) as

$$i_1 = I_{s1}\left(e^{\frac{E\cos(\omega t) - V_L}{V_t}} - 1\right)) \tag{6.6}$$

Taking into account the modified Bessel function series expansion, similarly to [129] and shown in (6.7), the current through the diode (i_1) can be expressed as in (6.8) and then approximated by the sum of only the DC and the first harmonic contributions as in (6.9).

$$e^{x\cos\omega t} = B_0(x) + 2\sum_{n=1}^{\infty} B_n(x)\cos(n\omega t) \tag{6.7}$$

$$i_1 = I_{s1}\left(e^{\frac{-V_L}{V_t}}B_0\left(\frac{E}{V_t}\right) - 1\right) + 2I_{s1}e^{\frac{-V_L}{V_t}}\sum_{n=1}^{\infty} B_n\left(\frac{E}{V_t}\right)\cos n\omega t \tag{6.8}$$

$$i_1 \cong I_1 + 2I_{s1}e^{\frac{-V_L}{V_t}}B_1\left(\frac{E}{V_t}\right)\cos\omega t \tag{6.9}$$

with

$$I_1 = I_{s1}\left(e^{\frac{-V_L}{V_t}}B_0\left(\frac{E}{V_t}\right) - 1\right) \tag{6.10}$$

where $B_0(x)$ and $B_n(x)$ is the modified Bessel function of order 0 and n, respectively. Note that the two branches of the proposed topologies (Figure 6.10a and Figure 6.10b) are DC coupled which affects the diode impedance. The DC equivalent circuit of the structure is shown in Figure 6.11c. At the DC analysis, the output DC current is given by

$$I_1 + I_2 = I_L \tag{6.11}$$

The output DC voltage (V_L) can be calculated by substituting (6.10) into (6.11). The result, shown in (6.12), demonstrates that V_L depends on the amplitude of the input signal E (and therefore the input power) and the output resistance (R_L).

$$I_{s1}\left(e^{-\frac{V_L}{Vt}}B_0\left(\frac{E}{V_t}\right) - 1\right) + I_{s2}\left(e^{-\frac{V_L}{Vt}} - 1\right) = \frac{V_L}{R_L} \tag{6.12}$$

The RF resistance of the diode can be calculated by dividing the RF voltage difference across the diode terminals v_1 with the RF current flowing into the diode from (6.9) which gives

$$Z_1 = \frac{E}{2I_{s1}e^{-\frac{V_L}{Vt}}B_1\left(\frac{E}{V_t}\right)} \tag{6.13}$$

From (6.12) and (6.13), one can see that the input impedance of the diode (Z_1) depends both on the input voltage (through the amplitude E) the output load R_L (through V_L). Considering that $V_L=I_LR_L$, the input impedance of the diode is also given by (6.14).

$$Z_1 = \frac{E}{2I_{s1}e^{-\frac{I_LR_L}{Vt}}B_1\left(\frac{E}{V_t}\right)} \tag{6.14}$$

6.3.2 Design of the Dual Band RCN based Rectifier

One of the most widely used metrics for the evaluation of the performance of rectifiers is the RF-DC conversion efficiency (6.15), which is calculated as the fraction of the harvested DC power (P_{dc_harv}) and the RF available power (P_{rf}) [122].

$$\eta_{RF-DC} = \frac{P_{dc\_harv}}{P_{rf}} \tag{6.15}$$

The maximum RF-DC conversion efficiency of rectifier circuits is achieved for a specific selection of output load that varies with the frequency [113]. The design of broadband and multi-band rectifier circuits implies that a compromise of the performance among the operating frequencies should be made.

A RCN based dual-band rectifier is designed to operate at f_1=915 MHz and f_2=2.45 GHz. The RCN_{2CELLS} topology is selected for this design, as simulation (Figure 6.12) has shown that the rectifier achieved improved performance with the

RCN_{2CELLS} (Figure 6.10b) topology in comparison with the RCN_{1CELL} topology (Figure 6.10a). Figure 6.12a and Figure 6.12b show the performance of the rectifier versus input power level and output load, where better results are achieved using two unit cells.

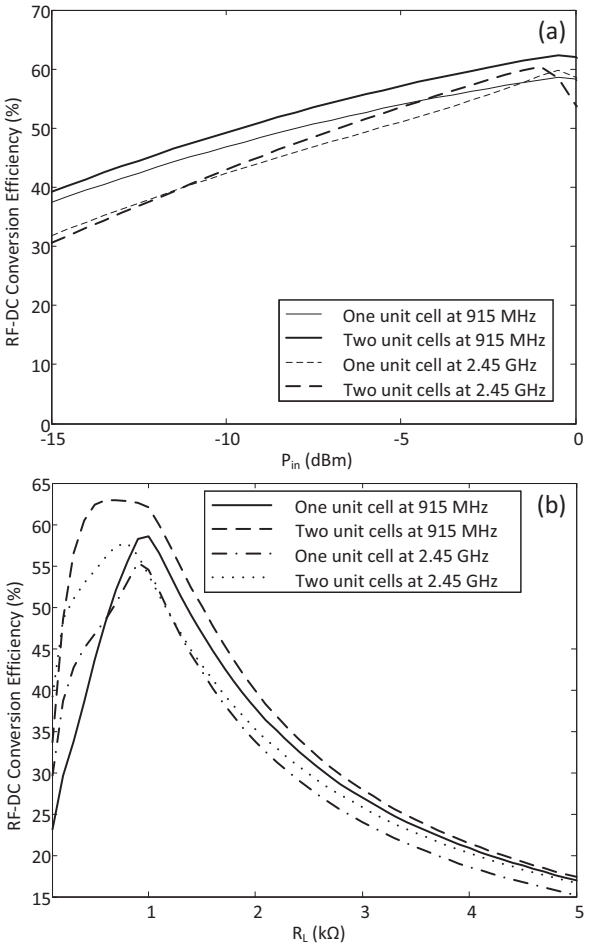

Figure 6.12: Performance comparison of a RCN based rectifier with a single (RCN_{1CELL} topology) and two unit cells at each branch of the RCN (RCN_{2CELLS} topology): a) versus input power (for R_L=1 kΩ) and b) output load (for P_{in}=0 dBm).

In order to be able to evaluate the performance of the proposed RCN based rectifier, a dual-band rectifier based on an envelope detector topology (Figure 6.10c) is also designed and optimized for maximum efficiency at 915 MHz and 2.45 GHz. The design and optimization of the two rectifiers is made using a commercial simulator (Agilent ADS). A harmonic balance analysis is used along with Large Signal S- Parameter analysis for the optimization of the circuits [122]-[124]. Optimization goals are used to impose constraints on both the minimum RF-DC conversion efficiency of the circuit and the input impedance matching (Z_{in}) at

f_1 and f_2. The selected rectifying device is a low threshold Schottky diode (SMS7630) from Skyworks [130].

The schematic of the conventional single diode envelope detector is shown in Figure 6.10c, while the proposed RCN based rectifier is depicted in Figure 6.10b. The values of the unit cells are chosen in such a way that the total phase difference for each branch has opposite sign at both operating frequencies. An additional inductor (L_{dc}=100 nH) is also placed as a DC path to the ground at the input of the diode (Figure 6.10b).

A performance comparison of the proposed RCN based rectifier and the envelope detector is presented in Figure 6.13-Figure 6.16. Their performance is evaluated in terms of the simulated RF-DC conversion efficiency versus R_L for an input power level of 0 dBm at the low operating frequency (Figure 6.13) and at the high operating frequency (Figure 6. 14). One can see that there is a larger range of output loads (R_L) for which the RF-DC conversion efficiency remains above 50 % for the case of the RCN based rectifier if compared to the envelope detector.

The RF-DC conversion efficiency versus input power level for a selected output load (R_L=1 kΩ) for both operating frequencies is also presented in Figure 6. 15 and Figure 6.16. It can be observed that the RF-DC conversion efficiency of the proposed RCN based rectifier remains higher than 50 % for a larger range of input power levels in comparison with the envelope detector rectifier.

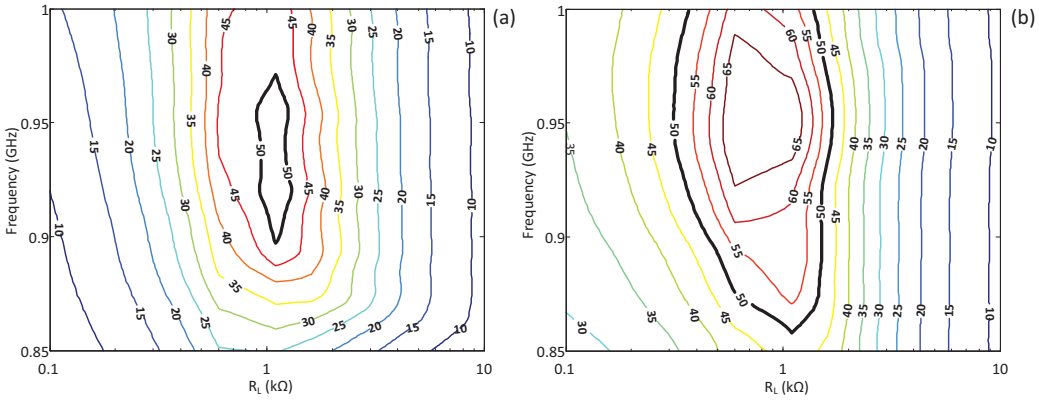

Figure 6.13: RF-DC conversion efficiency (%) of a) the envelope detector rectifier and b) the RCN based rectifier for an input power of 0 dBm at the 915 MHz band.

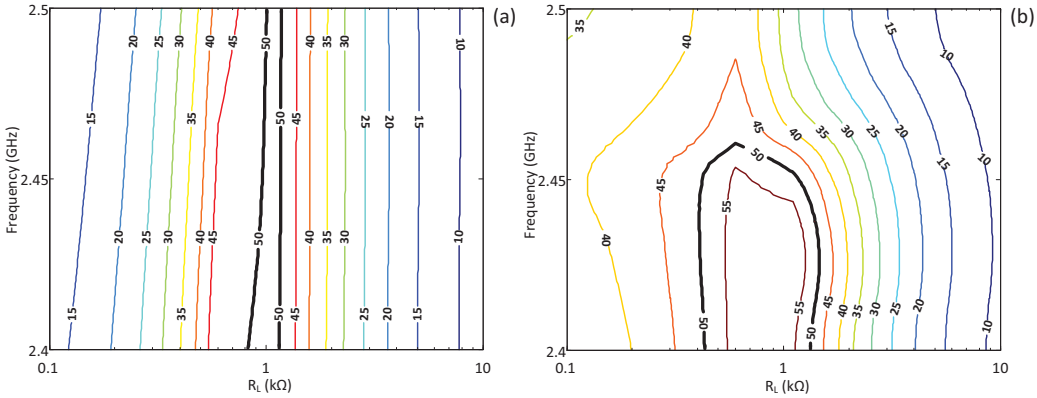

Figure 6. 14 . RF-DC conversion efficiency (%) of a) the envelope detector rectifier and b) the RCN based rectifier for an input power of 0 dBm at the 2.45 GHz band.

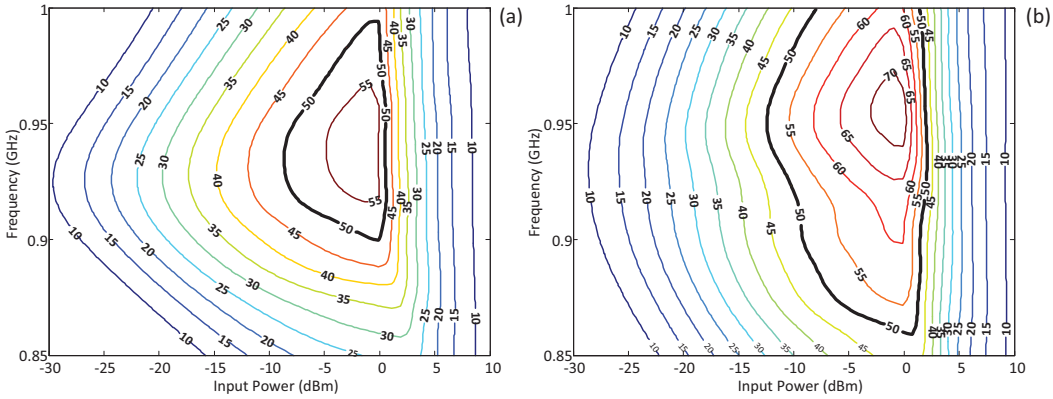

Figure 6. 15 RF-DC conversion efficiency (%) of a) the envelope detector rectifier and b) the RCN based rectifier for R_L=1 kΩ at the 915 MHz band.

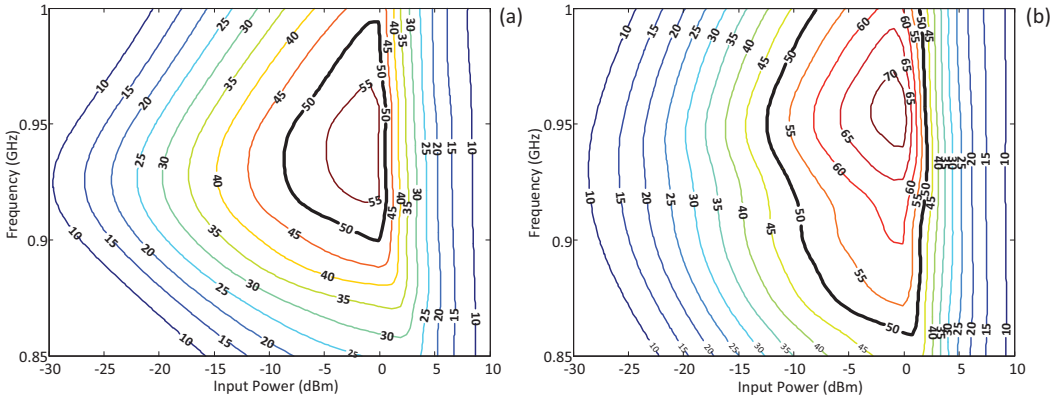

Figure 6.16: RF-DC conversion efficiency (%) of a) the envelope detector rectifier and b) the RCN based rectifier for R_L=1 kΩ at the 2.45 GHz band.

In conclusion, as it can be seen from Figure 6.13 - Figure 6.16, the proposed RCN based rectifier is less sensitive to input power and output load variations than the conventional envelope detector rectifier. Additionally the RCN based rectifier shows improved performance in terms of RF-DC conversion efficiency. The RF-DC conversion efficiency for both circuits at the two operating frequencies is also shown in Figure 6.17.

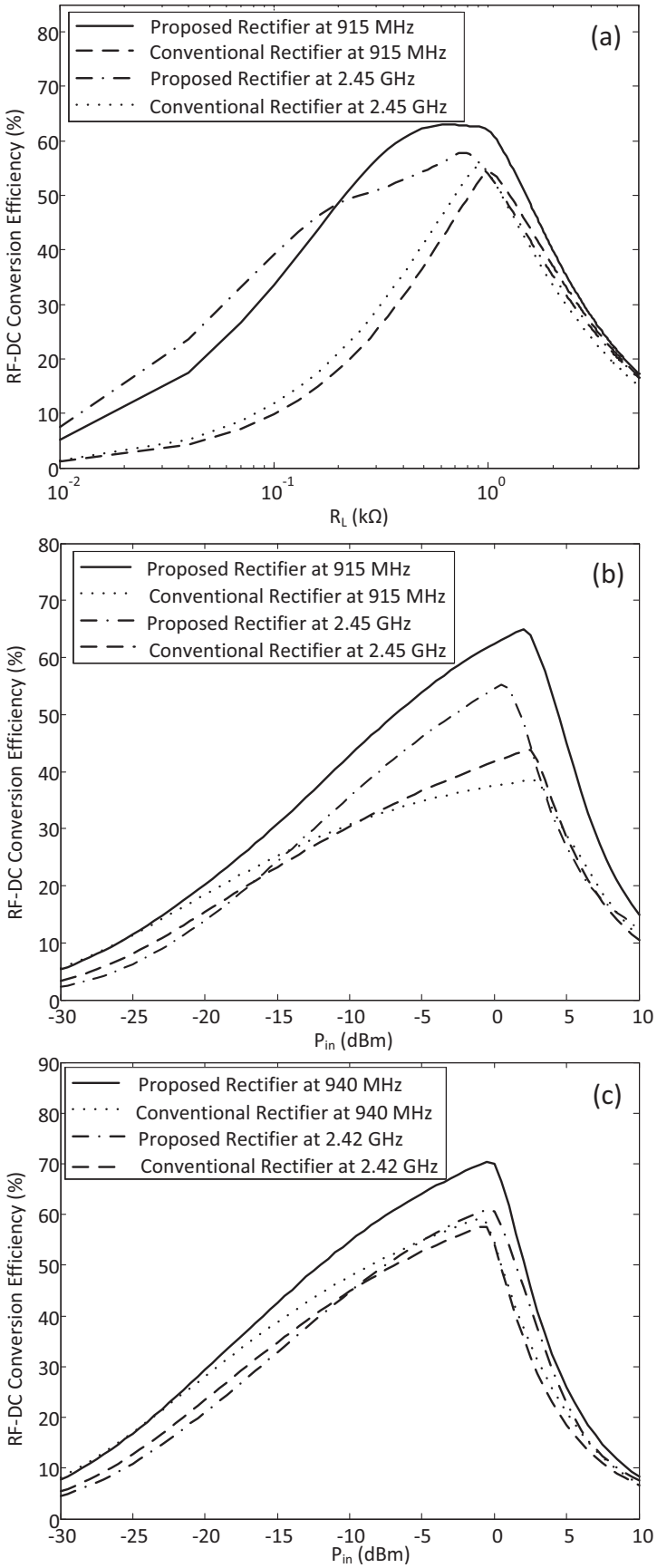

Figure 6.17: Performance comparison of the conventional envelope detector topology and the proposed RCN based rectifier versus a) output load (915 MHz/2.45 GHz), b) input power level for R_L=0.51 kΩ (915 MHz/2.45 GHz), and c) input power level for R_L=1 kΩ (940 MHz/2.42 GHz).

One can see from Figure 6.17 that the RCN based rectifier presents a flatter and higher value of RF-DC conversion efficiency versus the load resistance (Figure 6.21a for P_{in}=0 dBm). The RF-DC conversion efficiency also maintains higher values versus input power levels. It can be noticed that the improvement in the rectifier performance is more noticeable in certain load values (Figure 6.17b for R_L= 0.51 kΩ) and in certain frequency values (Figure 6.17c for R_L=1 kΩ) where the RF-DC conversion efficiency maintains a higher value in a larger range of input power levels.

It should be noted that the RCN based rectifier shows little improvement for high load values and high input power levels, which is partially attributed to the low breakdown voltage of the diode that determines its operating range and thus, the performance of the circuit. After the breakdown voltage is reached, RCN is not able to have any significant effect.

6.3.3 Final Design of the RCN based Rectifier

In the previous Sections, the RCN based rectifier has been designed using ideal lossless discrete elements. For the fabrication of the prototype, the ideal values of the lumped components have to be replaced with the models that are provided from the manufacturers. The layout of the rectifier circuit had also to be analyzed using electromagnetic (EM) simulation. A full-wave EM simulation is made for the design of the passive structure of the circuit.

In order to evaluate the impact of the substrate losses and the EM analysis of the layout on the performance of the circuit, two curves with intermediate steps are included in this Section. The RF-DC conversion efficiency of the proposed ideal rectifier (whose performance has been already analyzed in Section 6.3.2.) is shown in Figure 6.18. One can see that the rectifier presents peak RF-DC conversion efficiency at the 915 MHz and 2.45 GHz frequency bands.

The second curve of Figure 6.18 depicts how the introduction of the EM simulation affects the circuit performance. The layout of the circuit is simulated using the Agilent Momentum EM simulator and the obtained data are introduced in the circuit simulation. The capacitor C_R is implemented as a radial stub with width W=1.05 mm, length L=4.55 mm and angle 45º. By introducing these data at the

simulation, an additional peak is observed close to the second frequency band. Additionally, the peak efficiency at the high operating frequency band is slightly shifted to a higher frequency.

The third curve of Figure 6.18 shows the performance of the rectifier with real inductor and capacitor models but without substrate losses. So far, the obtained results show that the main source of losses of the topology is due to the discrete components losses and the layout of the circuit.

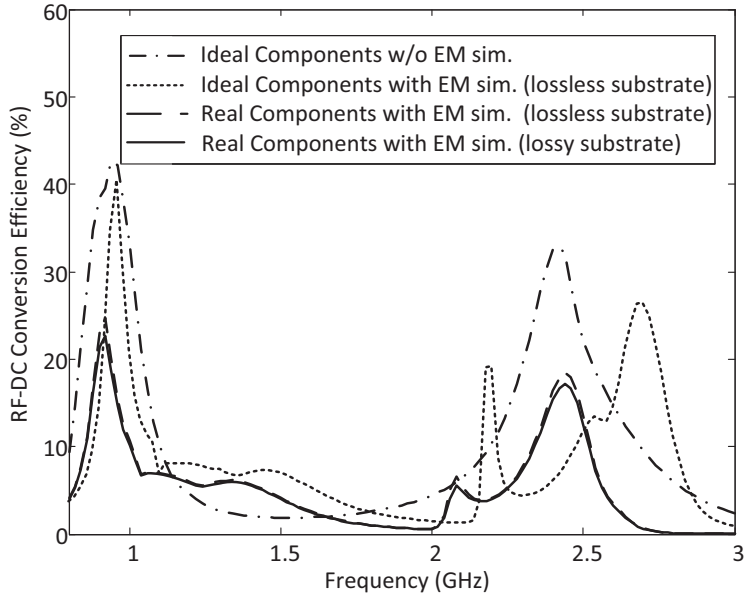

Figure 6.18: Evolution of the RF-DC conversion efficiency versus operating frequency for R_L=1 kΩ and P_{in}=-15 dBm.

Finally, the fourth curve (solid line) shows the performance of the dual-band rectifier, including losses associated with the layout, the discrete component values and the substrate material. The rectifier has reduced efficiency at the two operating frequencies in comparison with the design of the ideal rectifier as it is expected.

The simulation resulted in the component values shown in the Table 6.2. Commercial inductors from Coilcraft and capacitors from Murata have been used for the implementation of the rectifier. The prototype (Figure 6.19) is fabricated on Arlon 25N substrate with height of 30 mil, relative permittivity of 3.38 and loss tangent of 0.0025 using an LPKF Protomat C100/HF circuit board plotter [39].

The fabricated prototype has a total size of 3.8 cm x3.5 cm and it is shown in Figure 6.19. The measured results of the fabricated prototype are described in the

next Section, where the reduced sensitivity of the dual-band RCN based rectifier to input power and output load variations is demonstrated.

Component	Value	Component	Value	Component	Value
L_R	8.7 nH	L_{dc}	100 nH	C_L	27 pF
L_L	100 nH	C_R	0.8 pF	C_{out}	120 pF

Table 6.2: Component values for the fabricated dual-band RCN based rectifier.

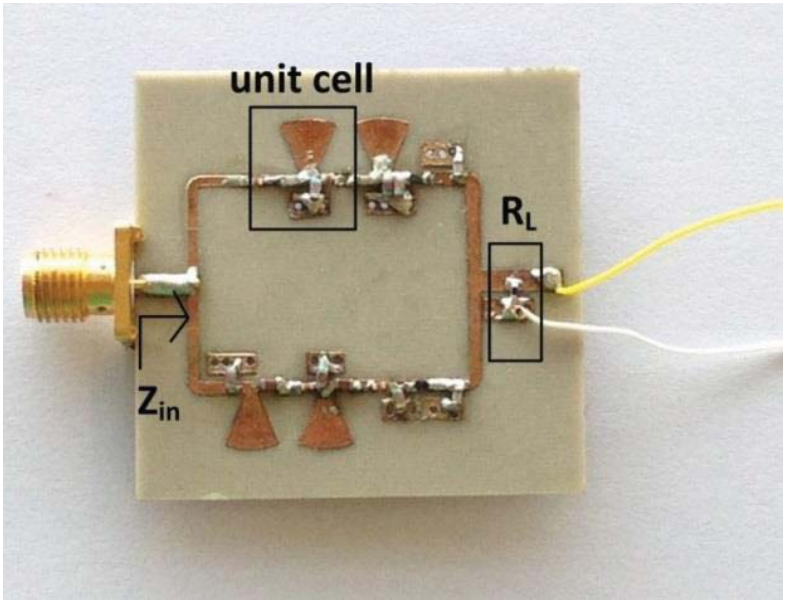

Figure 6.19: Fabricated prototype of the 915 MHz/2.45 GHz RCN based rectifier with a total size of 3.8 cm by 3.5 cm.

6.4 Experimental Results

The fabricated prototype is characterized in terms of its RF-DC conversion efficiency versus input power levels (P_{in}), output loads (R_L) and operating frequency. The performance of the circuit is shown in Figure 6.20 - Figure 6.26. Initially, the RF-DC conversion efficiency of the circuit versus operating frequency for R_L=1 kΩ and R_L=2 kΩ is measured for P_{in}=-15 dBm (Figure 6.20). One can see that the high operating is slightly shifted to a higher frequency value in comparison with the simulation results.

The slight shift of the second operating frequency to 2.5 GHz can be due to different factors, including the tolerances in the fabrication process, the surface mounted devices and the substrate material. Possible inaccuracies in the nonlinear

model of the diode could also contribute to the shift of the high operating frequency. However, the dual-band rectifier achieves RF-DC conversion efficiency of 23.2 % and 21.2 % at 915 MHz and at 2.5 GHz (R_L=2 kΩ).

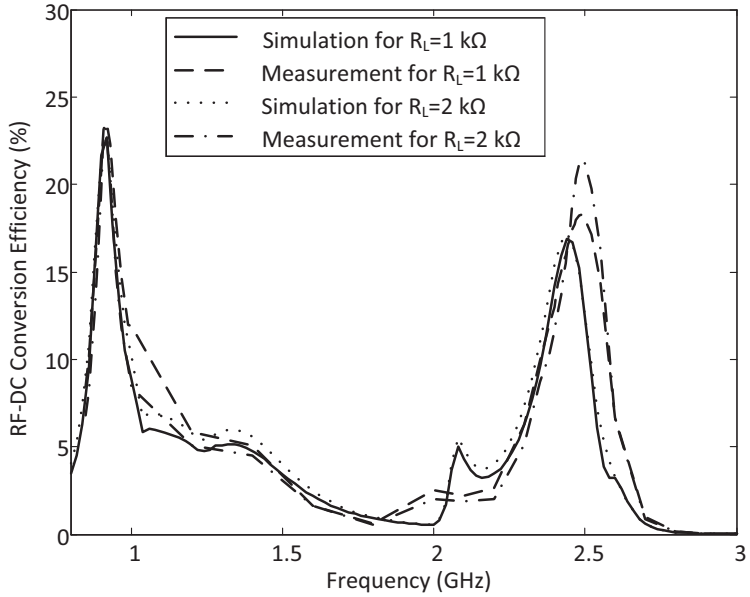

Figure 6.20: Comparison of simulated and measured RF-DC conversion efficiency for an input power of -15 dBm versus operating frequency for two different load values (1 kΩ and 2 kΩ).

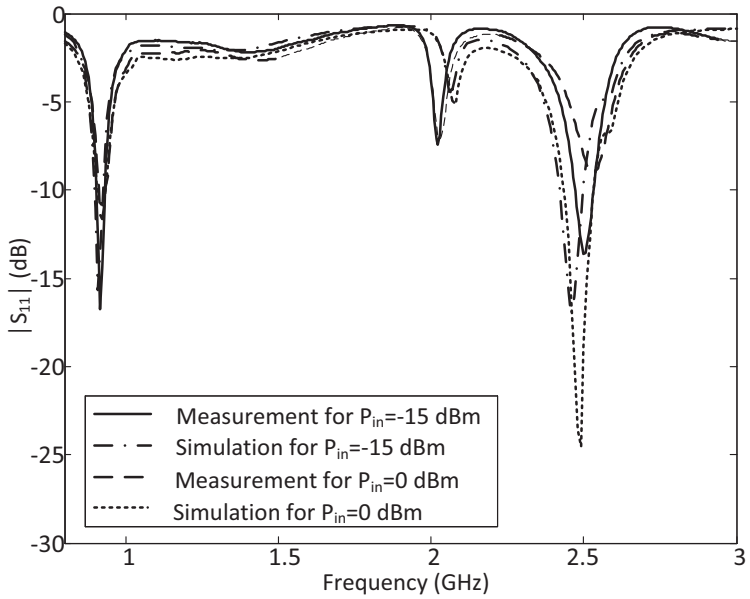

Figure 6.21: Comparison of simulated and measured reflection coefficient ($|S_{11}|$) versus operating frequency for two different input power levels (-15 dBm and 0 dBm) for R_L=2 kΩ.

A comparison between the simulated and measured reflection coefficient ($|S_{11}|$) of the RCN based rectifier for P_{in}=-15 dBm and P_{in}=0 dBm is shown in Figure 6.21. The measured results show that the rectifier remains matched for a

range of input power levels and that the measured results are in accordance with the simulation. The measured $|S_{11}|$ versus operating frequency for R_L= 0.51 kΩ, 2 kΩ and 2.7 kΩ for a fixed P_{in} (-15 dBm) is depicted at Figure 6.22 in order to show that the circuit also remains matched under a large variation of output loads (0.51 kΩ to 2.7 kΩ).

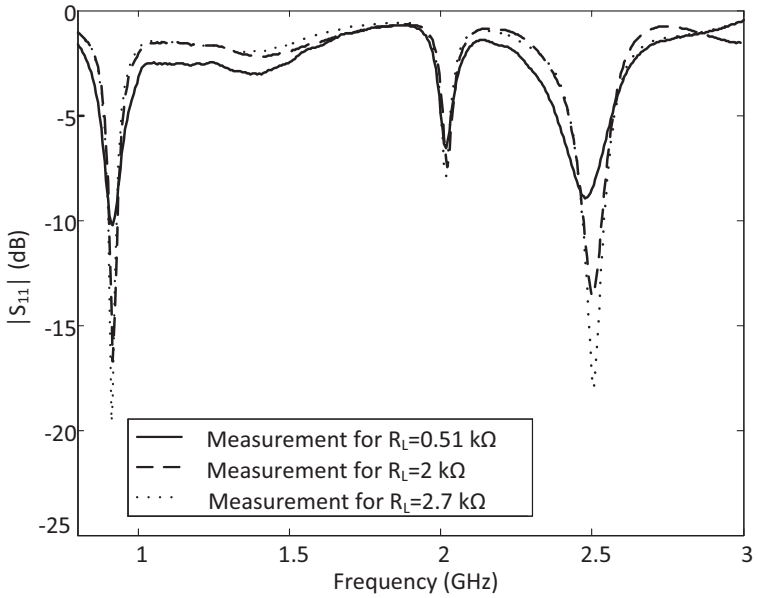

Figure 6.22: Measured reflection coefficient ($|S_{11}|$) versus operating frequency for various output loads (R_L= 0.51 kΩ, 2 kΩ and 2.7 kΩ) for an input power of -15 dBm.

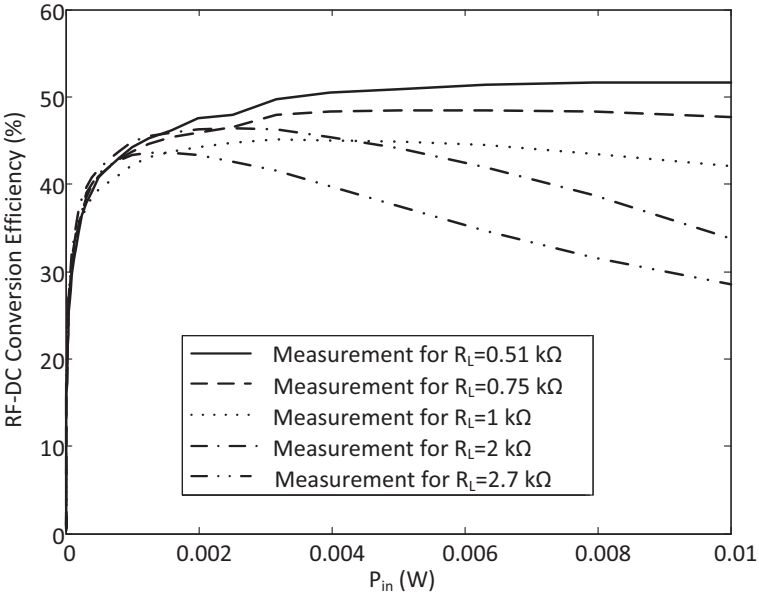

Figure 6.23: Measured RF-DC conversion efficiency versus input power for various load values (0.51 kΩ, 0.75 kΩ, 1 kΩ, 2 kΩ and 2.7 kΩ) at 915 MHz.

In order to verify the reduced sensitivity of the RCN based rectifier to input power and output load variations, a set of additional measurements is taken (Figure 6.23 to Figure 6.26). The evolution of the RF-DC conversion efficiency of the proposed rectifier versus P_{in} for different load values (0.51 kΩ, 0.75 kΩ, 1 kΩ, 2 kΩ and 2.7 kΩ) at the two operating frequencies with peak RF-DC conversion efficiency (915 MHz and 2.5 GHz) is depicted at Figure 6.23 and Figure 6.24, respectively.

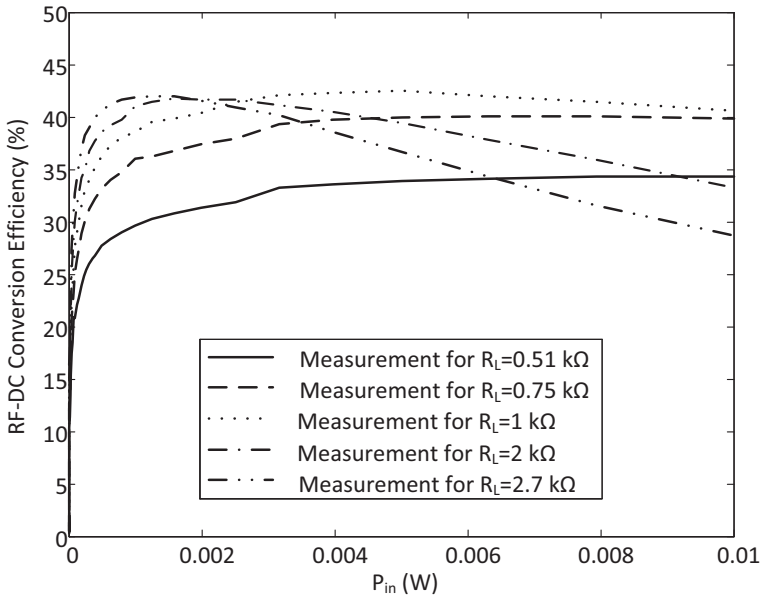

Figure 6.24: Measured RF-DC conversion efficiency versus input power for various load values (0.51 kΩ, 0.75 kΩ, 1 kΩ, 2 kΩ and 2.7 kΩ) at 2.5 GHz.

As it can be observed from Figure 6.23 and Figure 6.24, the evolution of the RF-DC conversion efficiency remains flat for a wide range of input power levels for R_L=0.51 kΩ, R_L=0.75 kΩ and R_L=1 kΩ. The resistance compression effect starts reducing for values greater than R_L=2 kΩ. However, the efficiency of the RCN based rectifier remains in high levels for a range of R_L and degrades smoothly. The measured results of Figure 6.23 and Figure 6.24 indicate that the optimum R_L that maximizes the RF-DC conversion efficiency of the rectifier is different for each frequency band [113], [115].

In order to evaluate the performance of the rectifier at low input power levels, the measured RF-DC conversion efficiency of the rectifier is plotted versus output load for low input power levels (-15 dBm, -10 dBm and -5 dBm) at 915 MHz (Figure 6.25) and 2.5 GHz (Figure 6.26). One can see that the efficiency remains nearly constant over a wide range of R_L for low levels of harvested power.

Finally, a comparison of the implemented RCN based rectifier with a selection of the state-of-the-art multi-band rectifiers is presented in Figure 6.27, demonstrating that the proposed rectifier exhibits a measured RF-DC conversion efficiency (23.2 % and 21.2 % at 915 MHz and 2.5 GHz) for P_{in}=-15 dBm and R_L=2 kΩ. Thus, the RCN based rectifier exhibits a state-of-the-art performance while at the same time shows reduced sensitivity to environmental changes.

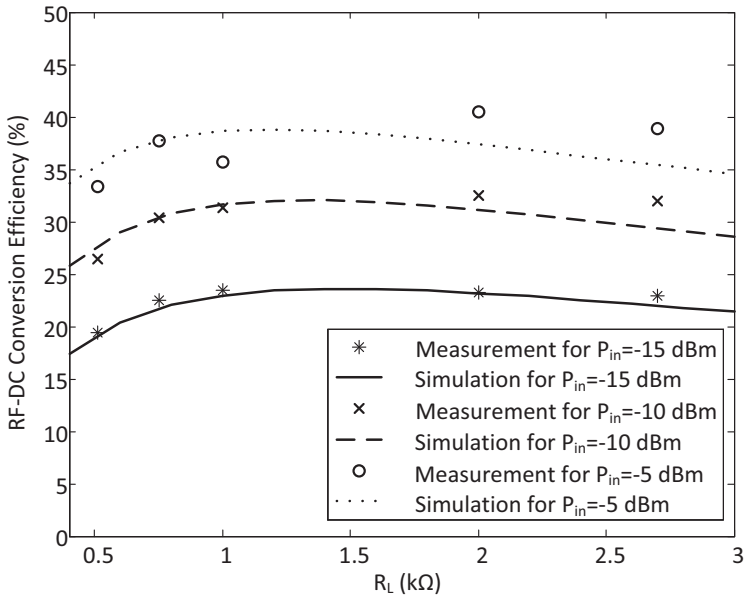

Figure 6.25: Measured RF-DC conversion efficiency versus output load for a range of input power levels from -15 dBm to -5 dBm at 915 MHz.

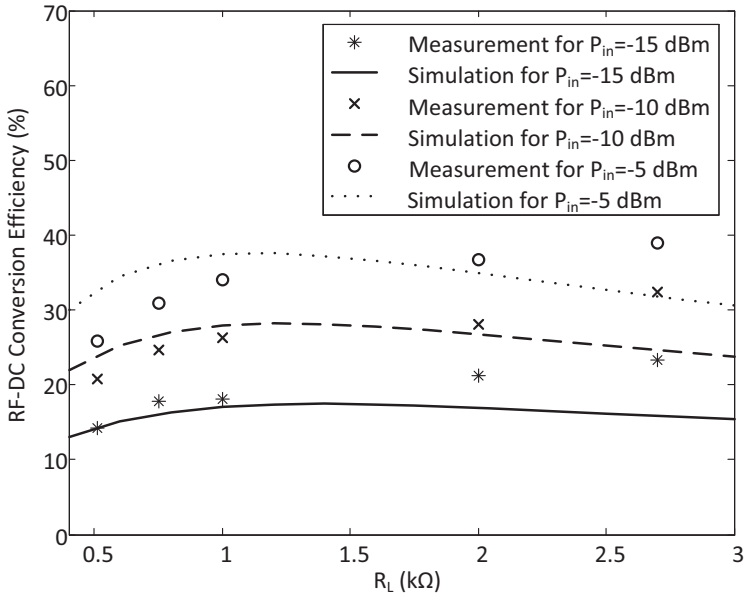

Figure 6.26: Measured RF-DC conversion efficiency versus load for a range of input power levels from -15 dBm to -5 dBm at 2.5 GHz.

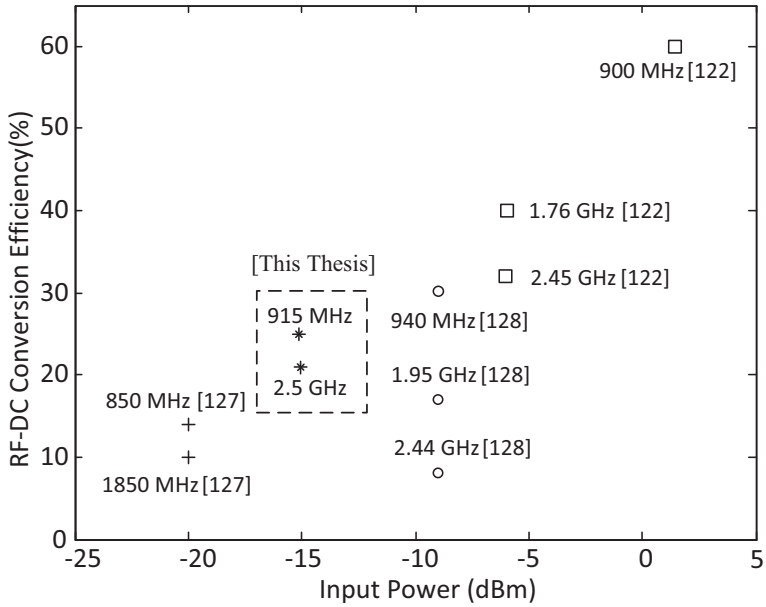

Figure 6.27: Comparison of state-of-the-art multi-band rectifiers.

6.5 Chapter Summary

In this Chapter, dual-band resistance compression networks have been introduced and experimentally demonstrated as part of the design of a dual-band rectifier. The operation principles of these novel impedance matching networks are presented in detail. The design of a dual-band RCN based rectifier operating at 915 MHz and 2.45 GHz is compared with a conventional envelope detector showing improved RF-DC conversion efficiency and reduced sensitivity to output load and input power variations. The proposed dual-band rectifier exhibits similar performance with the state-of-the-art dual-band rectifiers that have already been proposed in the literature.

Chapter 7

Conclusions and Future Work

7.1 Conclusions

This thesis has focused on the power amplification stage of modern transceivers. The main motivation has been to propose novel power amplifier architectures and investigate different topologies that can improve the performance of power amplifiers under various operating conditions. Lumped-element topologies, transmission line implementations and SIW technology has been used for the development of the prototypes.

The main contribution of this PhD thesis dissertation can be divided in two parts: i) the investigation of power amplifier topologies for modern communication systems (Chapter 2, 3 and 4) and ii) the introduction of novel resistance compression networks for power amplifier architectures in order to improve their operation under various conditions (Chapter 5 and 6). The obtained results are summarized as follows.

In Chapter 1, the motivation of the dissertation has been presented in detail. The design challenges associated with the power amplifications stage of modern transceivers have been described, along with the thesis structure.

Chapter 2 has focused on the design of a linear stand-alone power amplifier based on a GaN HEMT transistor. The proposed topology exhibits a gain of 11.7 dB and a drain efficiency of 39 % for an output power of 36.7 dBm at 2.4 GHz (P_{in}= 25 dBm) and presents some interesting characteristics. It achieves a carrier to intermodulation ratio as good as 25 dB for a two-tone input signal of 25 dBm of total power when it is not operating at its linear region. The PA despite its simple design achieves high linearity close to 1 dB compression point. This design, taking advantage of the device linearity sweet spots can be the basis for the development of an envelope tracking architecture.

Chapter 3 has dealt with the reduction of the number of circuit components needed in modern communication systems in order to minimize the cost and the size of the devices. In particular, two design approaches have been introduced for the implemetation of dual-band and broadband power amplifiers: i) the design of a 2.4 GHz/3.35 GHz power amplifier based on the use of Composite Right/Left-Handed unit cells and ii) a broadband power amplifier based on Composite Right/Left-Handed unit cells impemented in Substrate Integrated Waveguide technology. The dual-band PA has shown a maximum drain efficiency of 65 % and 52 % for an output level of 28.7 dBm and 27.5 dBm at 2.4 GHz and 3.35 GHz, respectively, demonstrating the feasibilty of such PA topologies to operate at an arbitrary set of frequencies. To that end, such a power amplifier topology has been implemented in SIW technology. The obtained results have shown that the implementation of multi-band/ broadband PAs based on Half-Mode SIW technology results in compact and easy to fabricate structures and yields numerous advantages, including the integration of the device within the packaging of the complete platform.

Chapter 4 has addressed a novel way to take advantage of the power amplification stage by exploiting the amount of dissipated power in the form of heat and converting it to useful DC power. A thermal model has been developed in a commercial simulator and it has been experimentally shown that a harvested power level of 1 mW can be achieved from a total dissipated power of 1.37 W. The harvested power, although in the order of mW, is enough to supply low-power sensors and control circuits placed near a

transmitter circuit. The possibility to increase the harvested DC power using additional TEGs has also been investigated in terms of measurements.

The last major contribution of this thesis concerns the design of resistance compression topologies to be applied in power amplifier topologies. Chapter 5 has been devoted to the design of such novel matching networks that show reduced sensitivity to environmental conditions variations based on simple LC impedance matching networks. The proposed topologies, despite their simple structure, exhibit resistance compression over a wide range of load variations and have been successfully applied in the design of a hybrid envelope amplifier topology. The simulated and measured results have shown that improved performance is achieved in comparison with a conventional envelope amplifier architecture.

Starting from the obtained results of Chapter 5, in Chapter 6 a dual-band resistance compression network scheme has been introduced. The proposed topology has been applied to the design of a dual-band rectifier. In particular, a 915 MHz/2.45 GHz has been designed and implemented showing reduced sensitivity versus output load and input power variations at the two operating frequencies. The fabricated prototype remains matched in a wide range of input power and loads and thus, exhibit higher RF-DC conversion efficiency if compared with a conventional envelope detector topology. The proposed RCN based topology can be successfully applied in a plethora of applications, from modern power amplifier topologies to RF energy harvesting scenarios.

7.2 Future Work

The topologies and the design approaches that have been proposed and discussed in this thesis have opened new lines for further investigation and research. The main goals for future work are summarized as follows.

- Chapter 2: The proposed stand-alone linear power amplifier could be used as the basis for the development of an envelope tracking topology. According to the preliminary simulation results presented in this Chapter, the power amplifier maintains high efficiency over a wide range of output power level and thus can have successful application in envelope tracking architectures.

- Chapter 3: Chapter 3 has introduced two design approaches to achieve dual-band and broadband power amplification based on the properties of the Composite Right/Left-Handed unit cells. Future work could include the design of a SIW power amplifier based on the same concept with a reduced number of unit cells and improved performance in terms of efficiency and gain.
- Chapter 4: In Chapter 4, a preliminary thermal model that predicts the amount of harvested DC power from the operation of a power amplifier circuit has been introduced. The proposed model considers a simulation approach where only steady state conditions have been considered. It is worth exploring in detail the behavior of such thermal energy harvesting setups by adopting a thermal model that will include thermal capacitances. Future work could also include the implementation of a symbolically defined device (SDD) thermal model in a commercial nonlinear circuit simulator in order to jointly simulate and optimize the electrical and thermoelectric performance of the power amplifier with the TEG system.
- Chapter 5: In Chapter 5, novel matching networks have been introduced and applied in the design of an envelope amplifier topology that has shown higher efficiency if compared with the conventional hybrid envelope amplifier topology. This can be further developed by adopting different structures and technologies that can achieve resistance compression in such envelope amplifier topologies. The design and fabrication of a RCN based envelope amplifier and RF power amplifier system, and its characterization with different input signals will constitute a great contribution.
- Chapter 6: A challenge associated with the design of multi-band and broadband resistance compression networks is the operating bandwidth of each frequency band. The increased operating bandwidth would be an important step ahead that could improve further the performance of microwave circuits. Such RCN topologies could be applied in power amplifier topologies, energy harvesting and Wireless Power Transfer applications.

Bibliography

[1] D. M. Pozar, Microwave Engineering, John Wiley & Sons, 1993.

[2] - , "The transistor — A new amplifier," *Elect. Eng*., vol. 67, no. 8, pp. 740, Aug. 1948.

[3] P. Colantonio, F. Giannini, E. Limiti, High Efficiency RF and Microwave Solid State Power Amplifiers, John Wiley & Sons Ltd, 2009.

[4] G. Gonzalez, Microwave Transistor Amplifiers, Prentice-Hall, 1997.

[5] M. Gruber, O. Blume, D. Ferling, D. Zeller, M.A Imran and E.C. Strinati, "EARTH - Energy Aware Radio and Network Technologies," *in Proc. IEEE 20th Int. Symp. Personal, Indoor and Mobile Radio Commun.,* Tokyo, 2009, pp. 1 - 5.

[6] L.M. Correia, D. Zeller, O. Blume, D. Ferling, A. Kangas, I. Gódor, G. Auer and L. Van Der Perre, "Challenges and enabling technologies for energy aware mobile radio networks," *IEEE Commun. Mag.*, vol. 48, no. 11, pp. 66 - 72, Nov. 2010.

[7] M. Rumney (ed), LTE and the Evolution to 4G Wireless: Design and Measurement Challenges, John Wiley & Sons, 2012.

[8] Z. Wang, Envelope Tracking Power Amplifiers for Wireless Communications, Artech House, 2014.

[9] P. A. Godoy, D. J. Perreault and J. L. Dawson, "Outphasing Energy Recovery Amplifier With Resistance Compression for Improved Efficiency," *IEEE Trans. Microw. Theory Techn*., vol. 57, no. 12, pp. 2895 - 2906, Dec. 2009.

[10] Y. Han, O. Leitermann, D.A. Jackson, J.M. Rivas and D.J. Perreault, "Resistance Compression Networks for Radio-Frequency Power Conversion," *IEEE Trans. Power Electron*., vol. 22, no. 1, pp. 41 - 53, Jan. 2007.

[11] F. Wang, D.F. Kimball, J.D. Popp, A.H. Yang, D.Y. Lie, P.M. Asbeck and L.E. Larson, "An improved power-added efficiency 19-dBm hybrid envelope elimination and restoration power amplifier for 802.11g WLAN applications," *IEEE Trans. Microw. Theory Techn.*, vol. 54, no. 12, pp. 4086 - 4099, Dec. 2006.

[12] S. C. Cripps, RF Power Amplifiers for Wireless Communications, Artech House, 2006.

[13] P.F. Miaja, J. Sebastian, R. Marante and J.A. Garcia, "A Linear Assisted Switching Envelope Amplifier for a UHF Polar Transmitter," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1850 - 1861, Apr. 2014.
[14] B. Kim, J. Kim, D. Kim, J. Son, Y. Cho, J. Kim and B. Park, "Push the Envelope: Design Concepts for Envelope-Tracking Power Amplifiers," *IEEE Microwave*, vol. 14, no. 3, pp. 68 - 81, Apr. 2013.
[15] D. Kimball, J.J. Yan, P. Theilmanrr, M. Hassan, P. Asbeck and L. Larson, "Efficient and wideband envelope amplifiers for envelope tracking and polar transmitters," *in Proc. IEEE Topical Conf. Power Amplifiers for Wireless and Radio Applications*, Santa Clara, CA, 2013, pp.13 - 15.
[16] S. Shinjo, Y.-P. Hong, H. Gheidi, D.F. Kimball and P.M. Asbeck, "High speed, high analog bandwidth buck converter using GaN HEMTs for envelope tracking power amplifier applications," *in Proc. IEEE Topical Conf. Wireless Sensors and Sensor Networks*, Austin, TX, 2013, pp. 13 - 15.
[17] A. Kanbe, M. Kaneta, F. Yui, H. Kobayashi, N. Takai, T. Shimura, H. Hirata and K. Yamagishi, "New architecture for envelope-tracking power amplifier for base station," *in Proc. Asia–Pacific Microw. Conf.*, Macao, 2008, pp. 296 - 299.
[18] D.F. Kimball, J. Jeong, C. Hsia, P. Draxler, S. Lanfranco, W. Nagy, K. Linthicum, L.E. Larson and P.M. Asbeck, "High-Efficiency Envelope-Tracking W-CDMA Base-Station Amplifier Using GaN HFETs," *IEEE Trans. Microw. Theory Techn.*, vol. 54, no. 11, pp. 3848 - 3856, Nov. 2006.
[19] G. Monprasert, P. Suebsombut, T. Pongthavornkamol and S. Chalermwisutkul, "2.45 GHz GaN HEMT Class-AB RF power amplifier design for wireless communication systems," *In Proc. Int. Conf. Electrical Eng./Elect. Computer Telecommun. and Inform. Technology*, Chaing Mai, 2010, pp. 566 - 569.
[20] M. Kamiyama, R. Ishikawa and K. Honjo, "5.65 GHz High-Efficiency GaN HEMT Power Amplifier With Harmonics Treatment up to Fourth Order," *IEEE Microw. Wirel. Comon. Lett.*, vol. 22, no. 6, pp. 315 - 317, June 2012.
[21] C. Hsia, D.F. Kimball and P.M Asbeck, "Effect of maximum power supply voltage on envelope tracking power amplifiers using GaN HEMTs," i*n Proc. IEEE Topical Conf. Power Amplifiers for Wireless and Radio Applications*, Phoenix, AZ, 2011, pp. 69 - 72.
[22] K. Cho, J. Kim and S.P. Stapleton, "A highly efficient Doherty feedforward linear power amplifier for W-CDMA base-station applications," *IEEE Trans. Microw. Theory Techn.*, 2005, vol. 53, no. 1, pp. 292 - 300.
[23] R.S. Pengelly, S.M. Wood, J.W. Milligan, S.T. Sheppard and W.L. Pribble, "A Review of GaN on SiC High Electron-Mobility Power Transistors and MMICs," *IEEE Trans. Microw. Theory Techn.,* vol. 60, no. 6, pp. 1764 - 1783, June 2012.
[24] U. K. Mishra, L. Shen, T. E. Kazior and Y.-F. Wu, "GaN-Based RF power devices and amplifiers," *Proc. IEEE*, vol. 96, no. 2, pp. 287 - 305, Feb. 2008.
[25] S. Lin and A.E. Fathy, "A 20 W GaN HEMT VHF/UHF Class-D power amplifier," *in Proc. IEEE 12th Annual Wireless and Microwave Technology Conf.*, Clearwater Beach, FL, 2011, pp. 1 - 4.
[26] D. Sardin and Z. Popovic, "Decade bandwidth high-efficiency GaN VHF/UHF power amplifier," *in Proc. 2013 IEEE MTT-S Int. Microwave Symp. Dig.*, Seattle, WA, 2013, pp. 1 – 3.
[27] R. Quaglia, L. Piazzon, V. Camarchia, R. Giofrè, M. Pirola, P. Colantonio, G. Ghione and F. Giannini, "Experimental investigation of bias current and load

modulation effects in phase distortion of GaN HEMTs," *Electronics Letters* , vol. 50, no. 10, pp. 773 - 775, May 2014.
[28] M. Kamiyama, R. Ishikawa and K. Honjo, "5.65 GHz High-Efficiency GaN HEMT Power Amplifier With Harmonics Treatment up to Fourth Order," *IEEE Microw. Compon. Lett.*, vol. 22, no. 6, pp. 315 - 317, June 2012.
[29] K. Kikuchi, M. Nishihara, H. Yamamoto, T. Yamamoto, S. Mizuno, F. Yamaki and S. Sano, "An 8.5–10.0 GHz 310 W GaN HEMT for radar applications," *in Proc. 2014 IEEE MTT-S Int. Microwave Symp. Dig*., Tampa, FL, 2014, pp. 1 - 4.
[30] B.J. Millon, S.M. Wood and R.S. Pengelly, "Design of GaN HEMT Transistor Based Amplifiers for 5-6 GHz WiMAX Applications," *in Proc 38th European Microwave Conf.,* 2008, pp. 1090 - 1093.
[31] K. Kuroda, R. Ishikawa and K. Honjo, "Parasitic compensation design technique for a C-band GaN HEMT class-F amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 11, pp. 2741–2750, Nov. 2010.
[32] P. Saad, H.M. Nemati, K. Andersson and C. Fager, "Highly efficient GaN-HEMT power amplifiers at 3.5 GHz and 5.5 GHz," *in Proc. IEEE Wireless Microw. Tech. Conf.,* Clearwater Beach, FL, Apr. 2011, pp. 236 – 239.
[33] F. Platz, O. Bengtsson, A. Raemer, S. Chevtchenko, W. Heinrich, "2.45 GHz ISM-Band RF-PA Demonstrator for GaN-HEMT optimization," *in Proc. of 2014 German Microwave Conference,* Aachen, pp. 1 - 4, Mar. 2014.
[34] K. Niotaki, A. Collado, A. Georgiadis and J. Vardakas "5 Watt GaN HEMT Power Amplifier for LTE*," Radioengineering*, pp. 338 - 344, Apr. 2014.
[35] CGH4006P 6W, RF Power GaN HEMT (datasheet) [Online]. Available at http://www.cree.com/RF/Products/General-Purpose-Broadband-28-V/Packaged-Discrete-Transistors/CGH40006P
[36] J.C. Pedro and N.B. Carvalho, Intermodulation Distortion in Microwave and Wireless Circuits. Artech House, 1996.
[37] N.B. Carvalho and J.C. Pedro, "Large signal IMD sweet spots in microwave power amplifiers," *in Proc. 1999 IEEE MTT-S Int. Microwave Symp. Dig*., Anaheim, CA, 1999, pp. 517 - 520.
[38] P. Colantonio, F. Giannini, R. Giofrè, E. Limit and A. Nanni, "Power Amplifier Design Strategy to null IMD asymmetry," *in Proc. 36th European Microwave Conf.*, Manchester, 2006, pp. 1304 - 1307.
[39] [Online] http://www.lpkfusa.com/RapidPCB/CircuitboardPlotters/c100hf.htm
[40] [Online] http://www.lpkf.com/_mediafiles/1792-milling-and-drilling-and-routing-tools.pdf
[41] [Online] http://www.lpkf.com/products/rapid-pcb-prototyping/through-hole-plating/chemical-free/
[42] Technical Datasheet, Conductive Epoxy [Online]. Available at http://www.farnell.com/datasheets/77553.pdf
[43] N.B Carvalho and J.C. Pedro, "Two-tone IMD asymmetry in microwave power amplifiers," *in Proc. 2000 IEEE MTT-S Int. Microwave Symp. Dig.*, Boston, MA, 2000, pp. 445 - 448.
[44] P. Colantonio, F. Giannini, E. Limiti, A. Nanni, V. Camarchia, V. Teppati and M. Pirola, "Linearity and efficiency optimisation in microwave power amplifier design," *in Proc. Microwave Integrated Circuit Conf*., 2007, pp. 283 - 286.
[45] A. Collado and A. Georgadis, "Optimal Waveforms for Efficient Wireless Power Transmission," *IEEE Microw. Compon. Lett.*, vol. 24, no. 5, pp. 354-356, May 2014.

[46] Rohde and Schwarz, “The Crest Factor in DVB-T (OFDM) Transmitter Systems and its Influence on the Dimensioning of Power Components,” Appl. Note 7TS02, Jan. 2007.
[47] N.B. Carvalho and J.C. Pedro, “A comprehensive explanation of distortion sideband asymmetries,” *IEEE Trans. Microw. Theory Techn*., vol. 50, no. 9, pp. 2090 - 2101, Sept. 2002.
[48] D. G. Taş, O. Ceylan, H. B. Yağcı, “A GaN HEMT Class AB RF Power Amplifier,” *in Proc. 12th Mediterranean Microwave Symp.*, Istanbul, 2012.
[49] K. Rawat, M.S. Hashmi and F.D. Ghannouchi, “Double the Band and Optimize,” *IEEE Microwave*, vol. 13, no. 2, pp. 69 - 82, Mar./Apr. 2012.
[50] X. Fu, D.T. Bespalko and S. Boumaiza, “Novel Dual-Band Matching Network for Effective Design of Concurrent Dual-Band Power Amplifiers,” *IEEE Trans. Circuits Syst.*, vol. 61, no. 1, pp. 293 - 301, Jan. 2014.
[51] S. Pei, J. Nan and Y. Yun, “Two kinds of dual-band power amplifier matching networks using three-section microstrip line,” *in Proc. Antennas, Propagation & EM Theory*, Xian, 2012, pp. 702 - 705.
[52] D. Kalim and R. Negra, “Concurrent planar multiharmonic dual-band load coupling network for switching-mode power amplifiers,” *in Proc. 2011 IEEE MTT-S Int. Microwave Symp. Dig*., Baltimore, MD, 2011, pp.1 - 4.
[53] K. Uchida, Y. Takayama, T. Fujitaand and K. Maenaka, “Dual-band GaAs FET power amplifier with two-frequency matching circuits,” *in Proc. Asia–Pacific Microw. Conf.*, Suzhou, 2005, vol. 1, pp. 4 – 7.
[54] A. Cidronali, N. Giovannelli, I. Magrini and G. Manes, “Compact Concurrent Dual-Band Power Amplifier for 1.9GHz WCDMA and 3.5GHz OFDM Wireless Systems,” *in Proc. 38th European Microwave Conf.*, Amsterdam, 2008, pp. 1545 - 1548.
[55] S. H. Ji, G. S. Hwang, C. S. Cho, J. W. Lee, and J. Kim, “836 MHz/1.95GHz Dual-Band Class-E Power Amplifier Using Composite Right/Left-Handed Transmission Lines,” *in Proc. 36th European Microwave Conf.*, Manchester, 2006, pp. 356 - 359.
[56] C. Caloz and T. Itoh, Electromagnetic Metamaterials: Transmission line theory and microwave applications, Hoboken, New Jersey, John Wiley & Sons, 2006.
[57] G.V. Eleftheriades, EM transmission-line metamaterials, Materials Today, vol. 12, Issue 3, pp. 30 - 41, March 2009.
[58] I-Hsiang Lin, M. DeVincentis, C. Caloz, and T. Itoh, “Arbitrary dual-band components using composite right/left-handed transmission lines,” *IEEE Trans. Microw. Theory Techn.*, vol. 52, no. 4, pp. 1142 - 1149, Apr. 2004.
[59] Y. Dong and T. Itoh, “Composite Right/Left-Handed Substrate Integrated Waveguide and Half Mode Substrate Integrated Waveguide Leaky-Wave Structures,” *IEEE Trans. on Antennas Propag.*, vol. 59, no. 3, pp. 767 - 775, Mar. 2011.
[60] Y. Dong and T. Itoh, “Promising Future of Metamaterials,” *IEEE Microwave*, vol. 13, no. 2, pp. 39-56, Mar./Apr. 2012.
[61] S. Kang, K. Jang, J. Jeon, I. Yang, K. Kahng, S.-g. Mok and J. Anguera, “Wideband and low-profile metamaterial antennas for aircrafts and automobiles,” *in Proc. 8th European Conf. on Antennas and Propagation*, 2014, pp. 976 - 977.
[62] P. Jin and R.W. Ziolkowski, “Multi-Frequency, Linear and Circular Polarized, Metamaterial-Inspired, Near-Field Resonant Parasitic Antennas,” *IEEE Trans. Antennas Propag.*, vol. 59, no. 5, pp. 1446 - 1459, May 2011.

[63] H. Mirzaei and G.V. Eleftheriades, "A wideband metamaterial-inspired compact antenna using embedded non-Foster matching," *in Proc. 2011 IEEE Int. Symp. on Antennas and Propagation*, July 2011, pp. 1950 - 1953.
[64] H. Mirzaei and G.V. Eleftheriades, "A Compact Frequency-Reconfigurable Metamaterial-Inspired Antenna, *IEEE Antennas Wireless Propag. Lett.*, vol. 10, pp. 1154 - 1157, 2011.
[65] M. Schueler, C. Mandel, M. Puentes and R. Jakoby, "Metamaterial Inspired Microwave Sensors," *IEEE Microwave*, vol. 13, no. 2, pp. 57 - 68, Mar./Apr. 2012.
[66] K. Niotaki, A. Collado, A. Georgiadis and J. Vardakas, "A dual-band power amplifier based on composite right/left-handed matching networks," *in Proc. 64th IEEE Electron. Compon. Technol. Conf.*, Orlando, FL, 2014, pp. 796 - 802.
[67] K. Niotaki, F. Giuppi, A. Collado, A. Georgiadis and J. Vardakas, "A Broadband Power Amplifier Based on Composite Right/Left-Handed Half-Mode Substrate Integrated Waveguide," *in Proc. Conf. Design Circuits and Integr. Syst.*, Donostia-San Sebastian, 2013, pp. 289 - 293.
[68] Avago technologies, Data Sheets & Technical Specifications (datasheet) [Online] www.avagotech.com/pages/en/rf_microwave/transistors/fet/atf-50189/
[69] S. Kassim and F. Malek, "Microwave FET amplifier stability analysis using Geometrically-Derived Stability Factors," *in Proc. 2010 Intell. and Advanced Syst.*, Kuala Lumpur, Malaysia, 2010, pp. 1 - 5.
[70] P. Colantonio, F. Giannini, R. Giofre and L. Piazzon, "A Design Technique for Concurrent Dual-Band Harmonic Tuned Power Amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 11, pp. 2545 - 2555, Nov. 2008.
[71] K. Rawat and F.M. Ghannouchi, "Dual-band matching technique based on dual-characteristic impedance transformers for dual-band power amplifiers design," *IET Microwaves, Antennas & Propagation*, vol. 5, no. 14, pp.1720 - 1729, Nov. 2011.
[72] S. H. Ji, C.S. Cho, J.-W Lee and J. Kim, "Concurrent Dual-Band Class-E Power Amplifier Using Composite Right/Left-Handed Transmission Lines," *IEEE Trans. Microw. Theory Techn.*, vol. 55, no. 6, pp. 1341 - 1347, June 2007.
[73] W. Ciccognani, E. Limiti and L. Scucchia, "A new structure for the design of dual band power amplifiers," *in Proc. 2011 Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits*, Vienna, 2011, pp.1 - 4.
[74] F.G.S. Silva, R.N. de Lima and R.C.S. Freire, "A 433/915-MHz class AB discrete power amplifier based on multiresonant circuits, " *in Proc. 26th Symp. on Integrated Circuits and Syst. Design*, 2013, pp. 1 - 6.
[75] M. Bozzi, A. Georgiadis and K. Wu, "Review of substrate-integrated waveguide circuits and antennas," *IET Microwaves, Antennas & Propagation*, vol. 5, no. 8, pp. 909 - 920, June 2011.
[76] W. Zhebin, S. Adhikari, D. Dousset, David, C. Park and K. Wu, "Substrate integrated waveguide (SIW) power amplifier using CBCPW-to-SIW transition for matching network," *in Proc. 2012 IEEE MTT-S Int. Microwave Symp. Dig.*, Montreal, QC, 2012, pp. 1 - 3.
[77] M. Abdolhamidi, and M. Shahabadi, "X-Band Substrate Integrated Waveguide Amplifier," *IEEE Microw. Comp. Lett.*, vol. 18, no. 12, pp. 815 - 817, Dec. 2008.

[78] Q. Lai, C. Fumeaux, W. Hong and R. Vahldieck, "Characterization of the Propagation Properties of the Half-Mode Substrate Integrated Waveguide," *IEEE Trans. Microw. Theory Techn*., vol. 57, no. 8, pp. 1996 - 2004, Aug. 2009.

[79] Y. D. Dong and T. Itoh, "Composite right/left-handed substrate integrated waveguide and half-mode substrate integrated waveguide," *in Proc. 2009 IEEE MTT-S Int. Microwave Symp. Dig.*, Boston, MA, 2009, pp. 49 - 52.

[80] M. W. Lee, Y. S. Lee and H. Jeong, "A high-efficiency GaN HEMT hybrid class-E power amplifier for 3.5 GHz WiMAX applications," *in Proc. 38th European Microwave Conf.*, Amsterdam, 2008, pp. 496 – 499.

[81] Y.-S. Lee and Y.-H. Jeong, "A high-efficiency class-E GaN HEMT power amplifier for WCDMA applications," *IEEE Microw. Wireless Compon. Lett*., vol. 17, no. 8, pp. 622 – 624, Aug. 2007.

[82] E. Khansalee, N. Puangngernmak and S. Chalermwisutkul, "A high efficiency VHF GaN HEMT class E power amplifier for public and homeland security applications," *in Proc Asia–Pacific Microw. Conf.*, Yokohama, 2010, pp. 437 - 440.

[83] M. Ozalas, "High-efficiency class-F MMIC power amplifiers at Ku-band, *in Proc. 2005 IEEE Annual Conf. Wireless and Microwave Technology*," 2005, pp. 137 – 140.

[84] A. Adahl and H. Zirath, "An 1 GHz Class E LDMOS Power Amplifier," *in Proc. 33th European Microwave Conf.*, Munich, 2003, pp. 285 - 288.

[85] Bumjin Kim, D. Derickson and C. Sun, "A High Power, High Efficiency Amplifier using GaN HEMT," *in Proc. Asia–Pacific Microw. Conf.*, Amsterdam, 2007, pp. 436 - 439.

[86] Y. S. Lee and Y. H. Jeong, "Applications of GaN HEMTs and SiC MESFETs in high efficiency class-E power amplifier design for WCDMA applications," *in Proc. 2007 IEEE MTT-S Int. Microwave Symp. Dig.*, Honolulu, HL, 2007, pp. 1099 - 1102.

[87] W. Gerhard and R. Knoechel, "A 2.14 GHz inverse class-F Si-LDMOS power amplifier with voltage second harmonic peaking*," in Proc. German Microw. Conf., Karlsruhe*, Germany, 2006, pp. 21 - 24.

[88] G. L. Solbrekken, K. Yazawa and A. Bar-Cohen, "Heat driven cooling of portable electronics using thermoelectric technology", *IEEE Trans. Adv. Packaging*, vol. 31, no. 2, pp. 429 - 437, May 2008.

[89] K. Yazawa, G. L. Solbrekken, and A. Bar-Cohen, "Thermoelectric Powered Convective Cooling of Microprocessors", *IEEE Trans. Adv. Packaging*, vol. 28, no. 2, pp. 231 - 239, May 2005.

[90] Y. Zhou, S. Paul, S. Bhunia, "Harvesting Wasted Heat in a Microprocessor Using Thermoelectric Generators: Modeling, Analysis and Measurement," *in Proc. Design, Automation and Test in Europe*, Munich, 2008, pp. 98 - 103.

[91] K. Niotaki, A. Georgiadis and A. Collado, "Thermal Energy Harvesting for Power Amplifiers," *in Proc. 2013 IEEE Radio and Wireless Symp*., Austin, TX, 2013, pp. 196 - 198.

[92] F. Giuppi, K. Niotaki, A. Collado and A. Georgiadis, "Challenges in energy harvesting techniques for autonomous self-powered wireless sensors," *in Proc. 2013 European Microw. Conf.,* Nuremberg, 2013, pp. 854 – 857.

[93] T.L. Bergman, A.S. Lavine, F.P. Incropera, D.P. DeWitt, Fundamentals of heat and mass transfer, New York: John Wiley & Sons, 2007.

[94] S. Beeby and N. White, Energy Harvesting for Autonomous Systems, Norwood, CA: Artech House, 2010.
[95] S. Lineykin, S. Ben-Yaakov, "Modeling and Analysis of Thermoelectric Modules," *IEEE Trans. Ind. Appl.*, vol. 43, no. 2, pp. 505 - 512, Mar./Apr. 2007.
[96] K.G. Biswas, T. D. Sands, B. A. Cola and X. Xu, "Thermal conductivity of bismuth telluride nanowire array-epoxy composite," *App. Physics Lett.*, vol. 94, no. 22, June 2009.
[97] TE-CORE 6/TE-CORE 7 Thermoharvesting Power Module (datasheet) [Online]. Available at www.micropelt.com/downloads/datasheet_te_core.pdf
[98] J. Kim, J. Son, S. Jee, S. Kim and B. Kim, "Optimization of Envelope Tracking Power Amplifier for Base-Station Applications," *IEEE Trans. Microw. Theory Techn*., vol. 61, no. 4, pp. 1620 - 1627, April 2013.
[99] O. Garcia, M. Vasic, P. Alou, J.A Oliver and J.A Cobos, "An overview of fast DC-DC converters for envelope amplifier in RF transmitters," *in Proc. APEC*, Orlando, FL, 2012, pp. 1313 – 1318.
[100] N. Le Gallou, D. Sardin, C. Delepaut, M. Campovecchio and S. Rochette, "Over 10-MHz bandwidth envelope-tracking DC/DC converter for flexible high power GaN amplifiers," *in Proc. 2011 IEEE MTT-S Int. Microw. Symp. Dig.*, Baltimore, MD, 2011.
[101] G. Hanington, P.Chen, P.M. Asbeck and L.E. Larson, "High-Efficiency Power Amplifier Using Dynamic Power-Supply Voltage for CDMA Applications," *IEEE Trans. Microw. Theory Techn.*, vol. 47, no. 8, pp. 1471 - 1476, Aug. 1999.
[102] M. Kwak, D.F. Kimball, C.D Presti, A. Scuderi, C. Santagati, J.J. Yan, P.M. Asbeck and L.E. Larson, "Design of a Wideband High-Voltage High-Efficiency BiCMOS Envelope Amplifier for Micro-Base-Station RF Power Amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 6, pp.1850 - 1861, June 2012.
[103] A.J.S. Boaventura and N. Borges Carvalho, "Spatially-combined multisine transmitter for wireless power transmission," *in Proc. 2013 IEEE Wireless Power Transfer*, Perugia, Italy, 2013, pp. 21 - 24.
[104] A.J.S. Boaventura, A. Collado, A. Georgiadis and N.B. Carvalho, "Spatial Power Combining of Multi-Sine Signals for Wireless Power Transmission Applications, " *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 4, pp. 1022 - 1030, Apr. 2014.
[105] J.F. Xu, W. Tai and D.S. Ricketts, "A transmission line based resistance compression network (TRCN) for microwave applications," *in Proc. 2013 IEEE MTT-S Int. Microw. Symp. Dig.,* Seattle, WA, pp. 1 - 3.
[106] T.W. Barton, J. Gordonson and D.J. Perreault, "Transmission Line Resistance Compression Networks and Applications to Wireless Power Transfer," *IEEE J. Emerg. Sel. Topics Power Electron*, Apr. 2014.
[107] J. Xu and D.S.Ricketts, "An Efficient, Watt-Level Microwave Rectifier Using an Impedance Compression Network (ICN) With Applications in Outphasing Energy Recovery Systems," *IEEE Microw. Compon. Lett.*, vol. 23, no. 10, pp. 542 - 544, Oct. 2013.
[108] W. Inam, K.K. Afridi and D.J. Perreault, "High Efficiency Resonant dc/dc Converter Utilizing a Resistance Compression Network," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4126 - 4135, Aug. 2014.

[109] LMH6639 190MHz Rail-to-Rail Output Amplifier with Disable (datasheet) [Online]. http://www.ti.com.cn/cn/lit/ds/symlink/lmh6639.pdf
[110] LMV7219 7 nsec, 2.7V to 5V Comparator with Rail-to-Rail Output (datasheet) [Online]. http://www.ti.com/lit/ds/symlink/lmv7219.pdf
[111] FDV302P Digital FET, P-Channel (datasheet) [Online]. https://www.fairchildsemi.com/datasheets/FD/FDV302P.pdf
[112] 40V Surface Mount Schottky Barrier Diode (datasheet) [Online]. http://www.diodes.com/datasheets/ZLLS400.pdf
[113] W. C. Brown, R. H. George and N. I. Heeman, "Microwave to dc converter," U.S. Patent 3 434 678, Mar. 25, 1969.
[114] A. Costanzo, M. Fabiani, A. Romani, D. Masotti and V. Rizzoli, "Codesign of ultra-low power RF/microwave receivers and converters for RFID and energy harvesting applications," *in Proc. 2010 IEEE MTT-S Int. Microw. Symp. Dig.,* Anaheim, CA, pp. 856 – 859.
[115] M.N. Ruíz, R. Marante and J.A. García, "A class E synchronous rectifier based on an E-pHEMT device for wireless powering applications," *in Proc. 2012 IEEE MTT-S Int. Microwave Symp. Dig.,* Montreal, QC, Canada, pp. 1 –3.
[116] B. Strassner and K. Chang, "A circularly polarized rectifying antenna array for wireless microwave power transmission with over 78% efficiency," *in 2002 IEEE MTT-S Int. Microwave Symp. Dig*., Seattle, WA, pp. 1535–1538.
[117] J. A. Hagerty, F. B. Helmbrecht, W. H. McCalpin, R. Zane and Z. B. Popovic, "Recycling ambient microwave energy with broad-band rectenna arrays," *IEEE Trans. Microw. Theory Techn*., vol. 52, no. 3, pp. 1014 – 1024, Mar. 2004.
[118] J. Heikkinen and J. M. Kivikoski, "A novel dual-frequency circularly polarized rectenna," *IEEE Antennas Wireless Propag. Lett.,* vol. 2, no. 1, pp. 330 - 333, Feb. 2003.
[119] Y.H. Suh and K. Chang, "A high-efficiency dual-frequency rectenna for 2.45- and 5.8- GHz wireless power transmission," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 7, pp. 1784 – 1789, July 2002.
[120] V. Rizzoli, G. Bichicchi, A. Costanzo, F. Donzelli, and D. Masotti, "CAD of multi-resonator rectenna for micro-power generation," *in Proc. 39th European Microwave Conf.,* Rome, 2009, pp. 1684 – 1687.
[121] T. Paing, J. Shin, R. Zane and Z. Popovic, "Resistor emulation approach to low-power RF energy harvesting," *IEEE Trans. Power Electron*., vol. 23, no. 3, pp. 1494 – 1501, May 2008.
[122] A. Georgiadis, G. Andia-Vera, and A. Collado, "Rectenna design and optimization using reciprocity theory and harmonic balance analysis for electromagnetic (EM) energy harvesting," *IEEE Antennas Wireless Propag. Lett.,* vol. 9, pp. 444 – 446, May 2010.
[123] A. Boaventura, A. Collado, N.B. Carvalho, and A. Georgiadis, "Optimum behavior: Wireless power transmission system design through behavioral models and efficient synthesis techniques," *IEEE Microwave.,* vol. 14, no. 2, pp. 26 – 35, Apr. 2013.
[124] C. R. Valenta and G. D. Durgin, "Harvesting Wireless Power: Survey of Energy-Harvester Conversion Efficiency in Far-Field, Wireless Power Transfer Systems," *IEEE Microwave.,* vol. 15, no. 4, pp. 108 - 120, June 2014.
[125] A. Collado and A. Georgiadis, "Conformal Hybrid Solar and Electromagnetic (EM) Energy Harvesting Rectenna," *IEEE Trans. Circuits Syst. I,* Reg. Papers, vol. 60, no. 8, pp. 2225 - 2234, Aug. 2013.

[126] B. L. Pham and A.-V. Pham, "Triple Bands Antenna and High Efficiency Rectifier Design for RF Energy Harvesting at 900, 1900 and 2400 MHz," *in 2013 IEEE MTT-S Int. Microwave Symp.*, Seattle, WA, pp. 1 - 3.

[127] D. Wang and R. Negra, "Design of a dual-band rectifier for wireless power transmission," *in Proc. 2013 IEEE Wireless Power Transfer,* pp. 127 - 130, May 2013.

[128] *Accepted for publication* - K. Niotaki, A. Georgiadis, A. Collado and J. Vardakas, "Dual-Band Resistance Compression Networks for Improved Rectifier Performance", *IEEE Trans. Microw. Theory Techn*.

[129] G. De Vita and G. Iannaccone, "Design criteria for the RF section of UHF and microwave passive RFID transponders," *IEEE Trans. Microw. Theory Techn.,* vol. 53, no. 9, pp. 2978 - 2990, Sept. 2005.

[130] Surface Mount Mixer and Detector Schottky Diodes (datasheet) [Online]. http://www.skyworksinc.com/uploads/documents/Surface_Mount_Schottky_Diodes_200041X.pdf