UNIVERSITAT POLITÈCNICA DE CATALUNYA BARCELONATECH

Advanced modeling of solid state transformer

Mohammad Ebrahim Adabi Firouzjaee

PhD Thesis

Advanced Modeling of Solid State Transformer

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Barcelona, January 2018

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"Nothing worth achieving is ever easy. It always takes smart, guts, hard work and perseverance"

List of Publications

Journal Publications:

M. Ebrahim Adabi, Juan. A. Martinez-Velasco, and S. Alepuz, "Modeling and simulation of a MMC-based solid-state transformer", *Electrical Engineering*, doi:10.1007/s00202-017-0510-x, February 2017.

J. Martin-Arnedo, F. González-Molina, Juan. A. Martinez-Velasco, and **M. Ebrahim Adabi**, "EMTP model of a bidirectional cascaded multilevel solid state transformer for distribution system studies", *Energies*, vol. 10, no. 4, pp. 521-539, April 2017.

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M. Ebrahim Adabi, and Juan. A. Martinez -Velasco, "A Survey of Solid State Transformers: Topologies, applications, and control strategies", under preparation for *Renewable & Sustainable Energy Reviews*.

Conference Publications:

J. Martin-Arnedo, F. González-Molina, Juan. A. Martínez-Velasco, and **E. Adabi,** "Implementation of a custom-made model for a multilevel solid state transformer," *EEUG Conf.*, Birmingham (UK), September 2016.

J. A. Corea-Araujo, Juan. A. Martinez-Velasco, and **E. Adabi**, "Optimum selection of parameters for a detailed model of a hybrid HVDC circuit breaker using a parallel genetic algorithm", *EEUG Conf.*, Kiel, Germany, September 2017.

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Chapter 1

The Solid State Transformer

1.1. Introduction

The future smart grid is being designed to mitigate or avoid consequences derived from power quality events (e.g., voltage dips), improve reliability indices (e.g., by reducing the number of interruptions and their duration), and increase the efficiency (e.g., by reducing losses) [1.1]–[1.2].

A key component for future smart grids is the solid-state transformer (SST). The SST provides new ways for controlling the electricity routing and also adds new functionalities to the distribution grid such as reactive power compensation, limited short-circuit currents or voltage sag compensation. However, it should be taken in to account that all of these functionalities will be achieved at the price of a more complex and expensive system [1.3]–[1.5].

The SST is foreseen to play a key role in replacement of conventional low frequency transformers [1.6]-[1.10].

The main drawbacks of conventional iron-and-copper transformers are summarized below [1.11]-[1.12]:

- the design presents bulky size and weight,
- environmental concerns happens when leaks of mineral oil occurs,
- voltage drop under load,
- inability to mitigate flicker,
- sensitivity to harmonics,
- limited performance under DC-offset load unbalances,
- inability to convert single-phase service to three-phase for powering certain types of equipment,
- no energy-storage capacity,

- unwanted voltage characteristics (e.g. voltage sags, fault occurrence) at one side are propagated to the other side,
- conventional transformers losses are relatively high at the average load level: transformers exhibit their maximum efficiency at their nominal load, while distribution transformer average load level is about 30%.

The main benefits of SSTs in comparison with conventional transformers are:

- smaller size and weight,
- fast control of bidirectional active power flow,
- enhanced power quality performance,
- easy integration of distributed resources,
- power factor correction,
- reactive power control at both SST sides,
- auto-balancing and variable-frequency,
- instantaneous voltage regulation,
- voltage sag compensation,
- harmonic compensation,
- fault isolation between the primary and the secondary sides.

However, the SST has also some disadvantages in front of the conventional transformer, they may include, among others, the following:

- The SST cost exceeds that of its conventional transformer counterpart. A need of cheap and reliable high-voltage high-power semiconductors to be competitive with the conventional transformer is therefore evident.
- The SST has a lower efficiency than the conventional transformer due to semiconductor losses.
- The SST has a more sophisticated design (e.g., needs more device and components for design) than the conventional transformer, and this adds some risks in terms of reliability.
- The SST exhibits higher EMI than the conventional transformer, which can require a better understanding of the SST impact and a better design to mitigate this impact.

In recent years, high-frequency, high-power, low-loss power electronic devices are available at a cheaper price. The advantages of the SST combined with cheaper power electronic devices supports economic feasibility of SST for replacing conventional transformer [1.11].

The combination of all these aspects with the capabilities and advantages offered by this device has also promoted a significant research into the development and application of the SST [1.12].

1.2. The SST Definition and Organization

The idea of a "solid state transformer" has been discussed since 1970. The initial purpose was to convert AC to AC for step-up or step down in a similar manner to that of a conventional transformer [1.6].

In 1970, W. McMurray form General Electric first introduced a high frequency link AC/AC converter, which became the basis for the solid state transformer based on direct AC/AC converter [1.13].

A significant literature has been published since then to study the design, operation and control of the solid state transformer [1.14].

Although the idea of the solid state transformer can be used for devices working at any voltage at both the primary and the secondary side, by default it is assumed in this thesis that this device is designed as an interface between systems working at medium and low voltages, respectively.

Several structures can realize the functionality of isolated AC-AC conversion to potentially suit the SST role in distribution systems. The classification presented here is that proposed in references [1.12], [1.15]-[1.16].

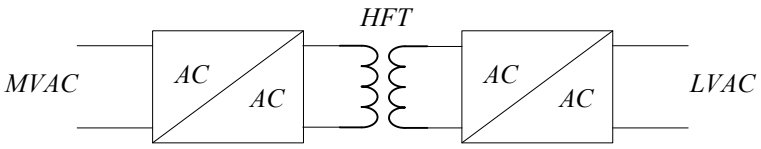
Four basic configuration can be considered for SST regarding to specific application:

1- Single stage SST (without DC link capacitances): It directly converts medium-voltage AC (MVAC) to low-voltage AC (LVAV) with a high frequency transformer as isolation.
2- Two stage SST (with DC link in the LV side): The MVAC is converted to LVDC at first stage and then the LVDC is converted to LVAC by an inverter.
3- Two stage SST (with DC link in the MV side): at first stage MVAC is converted to MVDC through AC/DC rectifier, then at second stage the MVDC is converted to LVAC without using low voltage DC link capacitance.
4- Three stage SST: The MVAC is converted to MVDC in the first stage, the MVDC is converted to LVDC through dual active bridge (DAB) in the second stage, and finally the LVDC is converted to LVAC in the third stage.

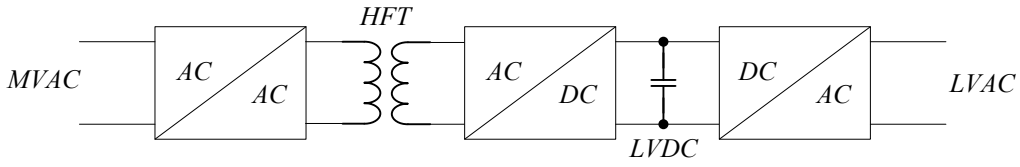
Figure 1.1 shows four basic topology configurations, namely types A, B, C, and D, which can suit SST functions [1-15], [1-16].

Most of the SST configurations designed for field application have adopted the type D since many suitable topologies can be chosen for each stage providing room to optimize its performance. Up to six representative SST topologies have been identified in reference [1.11], [1.12]:

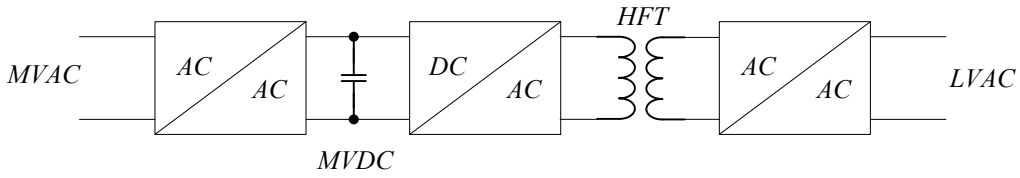
1. A single-stage SST comprising AC-AC full-bridge converter modules.
2. A single-stage SST comprising AC-AC flyback converter modules.
3. A two-stage SST comprising AC-DC isolated boost converter modules and a pulse with modulated (PWM) dual-phase inverter.
4. A two-stage SST comprising AC-DC dual active bridge (DAB) converter modules and a PWM dual-phase inverter.
5. A three-stage SST comprising a cascaded-full-bridge multilevel rectifier, DC-DC DAB modules and a PWM dual-phase inverter.
6. A three-stage SST comprising a diode-clamped multilevel rectifier, DC-DC Full-bridge converters and a PWM dual-phase inverter.



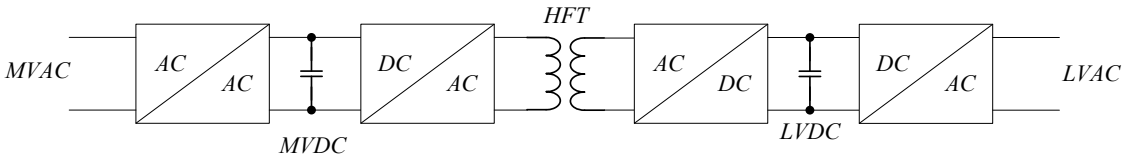
a) Single-stage SST – Type A



b) Two-stage SST with LVDC – Type B



c) Two-stage SST with MVDC – Type C



d) Three-stage SST – Type D

Figure 1.1. Classification of SST topologies [1.15], [1.16].

The design of the three-stage SST may be schematized as in Figure 1.2. It utilizes two semiconductor converter bridges and one transformer in between.

The first converter is connected to the MV side and it changes the three-phase AC voltages, with a frequency of 50 or 60 HZ, to a DC voltage in the MV DC link. The DC voltage is then converted back to AC, but with a higher frequency, by the second part of the MV-converter bridge. Thanks to the higher AC frequency, the magnetic properties of the transformer core are better utilized and the transformer can thus be made considerable smaller while maintaining the same power capability. On the LV side, a second converter bridge transforms the high frequency AC voltage first to DC and then back to the specific power frequency, 50 or 60 Hz.

As it can be seen from Figures 1.2, SSTs use power electronic converters along with high frequency transformer in order to convert medium or high voltage at the primary side to the low voltage at the secondary side. The result is a product that gives utilities an improved controllability in the grid, combined with a greatly reduced size and weight.

Note that the same or very similar design can be used to obtain a DC secondary-side waveform or a high frequency AC waveform. Although neither the configuration nor the design shown in Figure 1.2 should be significantly changed to cope with these alternatives, they are not studied in this thesis. By default the work presented in this thesis is focused on a three-stage SST for interfacing MV and LV systems.

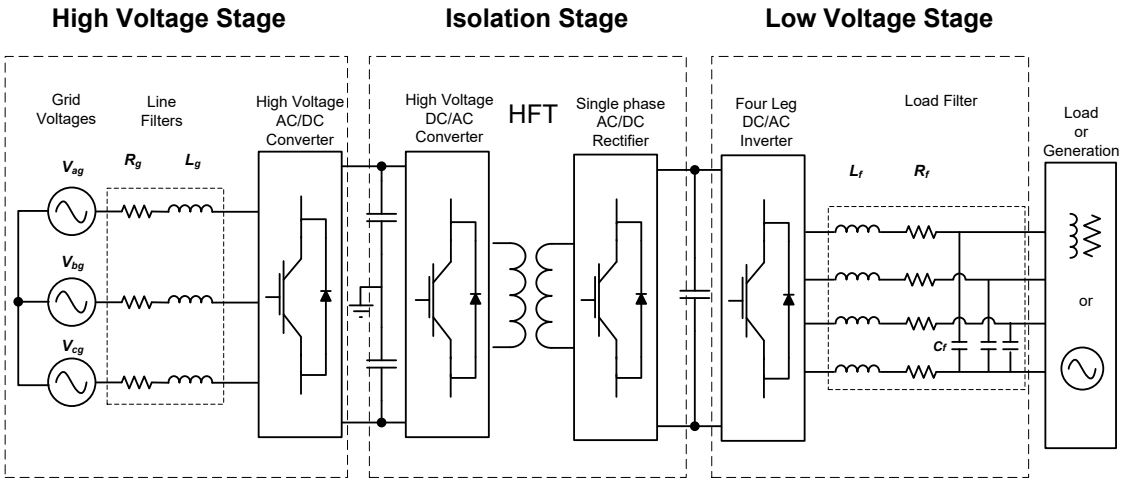


Figure 1.2. Schematic configuration of a three-stage SST.

1.3. Summary of Technologies for the Three-stage Solid State Transformer

Since standardized voltages used for MV distribution grids are usually equal or higher than 10 kV [1.17], multilevel topologies must be considered for the MV side of the SST if conventional Si-based semiconductors are used [1.18]-[1.20]; that is, a realistic SST model has to consider a multilevel converter representation at the MV side. Different topologies of multilevel converters have been proposed for SST applications. In addition, given the required number of levels, even for the lowest voltages, the selected topology has to face some important aspects such as capacitor voltage balancing and complex control strategies.

Some of the different multilevel topologies and control strategies presented to date are summarized below.

Reference [1.21] proposes a model for a bidirectional SST to study its behavior under variable operating conditions and/or in presence of disturbances, located at both sides of the transformer.

Reference [1.22] presents a dynamic average model (DAM) of SST for a bidirectional SST and its implementation in a real-time simulation platform. In this paper a four-leg inverter is proposed for low voltage side to provide high performance behavior of the SST model under different operating conditions.

Reference [1.23] presents a three-level neutral point clamped (NPC) converter configuration for the MV side of the SST.

A modular SST design is proposed in [1.24]. The main characteristic of the topology is an independent operation of each sub module (SM). The modules are connected to a common dc link that facilitates energy transfer between modules and ports. In such multiport system the ports can operate independently. This is an important feature for applications where input and output voltages are different in many parameters.

A cascaded H-Bridge Multilevel Inverter (CHMI-SST) topology is presented for different applications in [1.25]-[1-29].

Reference [1.25] presents the design of a master-slave control strategy for a dual active bridge (DAB). The goal is to reduce the controller task and simplify the modulation

algorithm. The master controller executes control and modulation calculations, while the slave controllers take care of switching and protection tasks. Due to the inherent unbalances in cascaded H-bridges, a compensation strategy based on three-phase d-q decoupled current controller is proposed: an optimum zero-sequence component is injected so that the three-phase grid currents are balanced. Additionally, a dynamic reference voltage is implemented to tightly regulate the output voltage of DAB modules. At the end, grid currents and dc-link voltage in each module can be simultaneously balanced.

Reference [1.26] presents the design and test of a CHMI-SST lab prototype that works as an active interface in smart grids. Specifically, the design of both power stages and controllers is presented, and an advanced control system is developed to achieve high-performance operation.

Reference [1.27] proposes a novel current sensorless controller for balancing the power in the DC/DC stage of a SST based on a cascaded multilevel converter. It is shown that the equalization of the active power component of duty cycles in the cascaded multilevel rectifier can be a good indicator of power balance in the DC/DC stage. Additionally, the power balance of the DC/DC stage can guarantee voltage balance in the rectifier stage if the differences among the power devices are negligible.

Reference [1.28] presents a 20 kVA SST based on 6.5 kV IGBT for interface with 7.2 kV distribution system voltage. The three-stage SST consists of a cascaded multilevel AC/DC rectifier input stage, a DAB converter isolation stage with high frequency transformers, and a DC/AC inverter output stage. A novel control strategy based on the single-phase d-q vector control is proposed to balance the rectifier capacitor voltages and the real power through the DAB parallel modules.

Reference [1.29] proposes a novel modular cascaded multilevel converter with multilinking high-frequency (MWHF) transformer for medium or high voltage applications. A cascaded H-bridge rectifier (CHBR) is connected directly with the input ac source while the traditional step-down transformer is no longer necessary. An isolated dc–dc converter composed by a group of H-bridge converters and a MWHF transformer with high power density is used to isolate the dc buses. The equivalent circuit and mathematical model of the MWHF transformer and the high frequency (HF) converter are detailed. The paper analyzes the performance of the SST under unbalanced loads and verifies the naturally balance ability.

References [1.30]-[1-32] present modular multilevel converter (MMC) configurations in which the high-voltage grid-side power converter generates high-frequency sinusoidal voltages.

A detailed analysis of topologies and control strategies proposed for three-stage SST designs are summarized in Table 1.1 [1.12]. According to the table, MMC converters can provide an effective topology for the MV side of the SST; their main advantages are modularity and scalability: the desired voltage level can be easily achieved by a series connection of MMC sub-modules (SMs). In addition, a MMC topology can provide high power quality and efficiency with reduced size of passive filters. These features makes MMC option an attractive topology for the MV stage of the SST. In addition, from the information presented in the table, it is evident that the level shifted PWM (LS-PWM) is a well suited modulation method for the MMC due to its simple algorithm and minimal hardware requirements.

As it can be deduced from the table, the single-phase Dual Active Bridge (DAB) topology provides a good efficiency while keeping the number of passive components low, which allows for a simple and compact design. The table also shows that the phase-shift modulation is simple to implement and its lower RMS currents result in lower component ratings. These advantages outweigh the higher turn-off losses faced with this method.

The three-phase four-leg (3P-4L) converter is capable of handling unbalanced loads while keeping the number of switches to a minimum. This makes the 3P-4L converter a suited topology for this stage. The 3D-SVPWM (3D-Space Vector PWM) and DPWM (discontinuous PWM) are difficult to implement because of their high computational requirements, while the CPWM (Continuous PWM) has very low hardware requirements and an easy algorithm, which makes it very suitable to use for the 3P-4L converter.

1.4. Accomplishments

The main goal of this thesis is to implement and test an advanced three-stage bidirectional MMC-based SST model in Matlab/Simulink: the implemented model must be realistic and as close as possible to the real SST design. The proposed model should duplicate the performance of a real MV/LV SST with a rated power below 1 MVA.

In order to achieve these objectives, the tasks listed below have been carried out.

High voltage stage:

Task 1: An advanced three-phase modular multilevel converter (MMC) model has been developed and implemented.

Task 2: A vector pulse width modulation control strategy has been implemented to obtain high quality MV voltage and current waveforms, and a balanced DC voltage at each MMC submodule.

Isolation stage:

Task 3: A model for the converters operating at each side of the DC-DC isolation stage has been implemented: a single-phase modular multilevel converter model at the MV side and a single-phase bridge model at the LV side.

Task 4: A proper control strategy has been implemented in order to provide high frequency multilevel voltage at the higher voltage side of the high frequency transformer.

Low voltage stage:

Task 5: A three-phase four-leg converter with enhanced control strategy has been developed and implemented to obtain an enhanced performance in both balanced and unbalanced conditions of loads and with the capability of harmonic compensation for nonlinear loads.

Task 6: Adequate values have been selected for filters in order to obtain high quality voltage and current waveforms at both sides of the SST.

Table 1.1. Comparison between topologies and control strategies

Topology/Control	Advantages	Disadvantages
AC-DC MV Input Stage		
Converter Topology		
Flying Capacitor (FC)	Modularity	Higher output levels require a large amount of capacitors Complex control Complex voltage balance control
Cascade H-Bridge (CHB)	Simple control Simple voltage balance control Modularity	High voltage DC-link not achievable
H-bridge NPC (HNPC)		Complex control Complex voltage balance control Limited modularity
Multilevel Active NPC (ML-ANPC)	Modularity	Complex control and voltage balance control Number of clamping diodes increase with square of output levels
Transistor Clamped (TTC)	Simple control Modularity	Large number of transistors required Complex voltage balance control
Modular Multilevel Converter (MMC)	Modularity and flexibility	Complex control Complex voltage balance control
Control Strategy		
Phase Shifted PWM (PS-PWM)	Simple control algorithm Minimal hardware requirements Each cell is assigned with a pair of carriers, allowing for easy control	
Level Shifted PWM (LS-PWM)	Simple control algorithm Minimal hardware requirements Slightly better harmonic cancelation	
DC-DC MV/LV Isolation Stage		
Converter Topology		
Single-phase Dual Active Bridge converter	Fewest passive components Good efficiency	Large RMS DC capacitor currents may occur
Three-phase Dual Active Bridge converter	Smaller RMS current than Dual Active Bridge Lower component ratings No need for extra inductors	High number of switches and inductors Higher losses
Bidirectional Isolated Full Bridge converter	High switching frequency and power density	Requires extra inductor Requires snubber circuit
Bidirectional Isolated Current Doubler topology	High current handling Lower conduction losses Fewer switches	Requires two extra inductors Limited operating voltage
Bidirectional Isolated Push-Pull topology	High current handling Reduced inductor requirements Fewer switches required	Ineffective use of complex transformer
Control Strategy		
Phase Shift Modulation	Simple control and algorithm	Higher losses at low power levels
Trapezoidal Modulation	High voltage range	Unable to operate under no-load
Triangular Modulation	Low switching losses	High RMS currents
DC-AC LV Output Stage		
Converter Topology		
1P-3W converter	Can handle unbalanced loads	High number of switches
3P converter	Simple circuit and control	DC-link unbalance
3P-4L converter	Can handle unbalanced loads	Complex control
Control Strategy		
3D Space Vector PWM (3D-SVPWM)	Complex implementation	Modest switching losses
Continuous PWM (CPWM)	Modest switching losses Easy implementation	
Discontinuous PWM (DPWM)	Complex implementation	Low switching losses

Modeling of semiconductor losses

Task 7: In order to obtain a realistic SST model and estimate the actual SST efficiency, some work has been focused on the representation of semiconductor losses. Several approaches for representing semiconductor losses in the various topologies selected for the different SST stages have been followed.

Case studies

Task 8: Complete tests of the two implemented SST models (without and with semiconductor losses) have been carried out in order to check the performance of a bidirectional device, running in a stand-alone manner or as a component of a MV distribution system.

As a result of the research work carried out for this Thesis, several technical papers have been submitted to different conferences and journals. The complete list of accepted and submitted papers is as follows:

1. M. Ebrahim Adabi, Juan A. Martinez-Velasco, and Salvador Alepuz, "Modeling and simulation of a MMC-based solid-state transformer", *Electrical Engineering*, doi:10.1007/s00202-017-0510-x, 2017.
2. Jacinto Martin-Arnedo, Francisco González-Molina, Juan A. Martinez-Velasco, and M. Ebrahim Adabi, "EMTP model of a bidirectional cascaded multilevel solid state transformer for distribution system studies", *Energies*, vol. 10, no. 4, pp. 521-539, April 2017.
3. M. Ebrahim Adabi, and Juan A. Martinez-Velasco, "MMC-based solid state transformer model including semiconductor losses", *Electrical Engineering*, doi: 10.1007/s00202-017-0640-1, 2017.
4. Jacinto Martin-Arnedo, Francisco González-Molina, Juan A. Martínez-Velasco, and Ebrahim Adabi, "Implementation of a custom-made model for a multilevel solid state transformer," *EEUG Conf.*, Birmingham (UK), September 2016.
5. Javier A. Corea-Araujo, Juan A. Martinez-Velasco, and Ebrahim Adabi, "Optimum selection of parameters for a detailed model of a hybrid HVDC circuit breaker using a parallel genetic algorithm," *EEUG Conf.*, Kiel (Germany), September 2017.
6. M. Ebrahim Adabi, and Juan A. Martinez -Velasco, "A Survey of Solid State Transformers: Topologies, applications, and control strategies", under preparation.

1.5. Document Structure

The remainder of this thesis is divided into four subsequent chapters plus an Appendix. The chapters will present the procedures developed for the thesis as well as detail case studies used to prove the usefulness of the proposed methods. The topics covered by each chapter are summarized below.

Second chapter

The second chapter details and analyzes the configuration selected for each stage of a bidirectional three-stage MMC-based SST. It also details the approach implemented to represent semiconductor losses and obtain a more realistic lossy model of a SST as a device connected to the distribution system.

Third chapter

The third chapter provides a detailed description of the Matlab/Simulink implementation of the MMC-based SST.

Fourth chapter

Chapter 4 presents simulation results for several case studies considering two different SST models and test systems. The first test system is simply a stand-alone SST without losses, the second test system is a medium size MV distribution system to which a lossy SST model is connected (i.e. the SST serves as interface between a MV distribution system and LV load/generation).

Fifth chapter

The last chapter summarizes the main conclusions derived from the work developed for this Thesis.

Appendix

The Appendix provides a detailed summary of SST prototypes presented to date and an up-to-date experience on SST modeling and simulation.

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Chapter 2

Modeling of a Three-stage MMC-based Solid State Transformer

2.1. Introduction

Recently, modular multilevel converter (MMC) topologies have attracted attention for high or medium voltage applications [2.1]-[2.5]. These converters can provide an effective topology for the MV side of the SST; their main advantages are modularity and scalability: the desired voltage level can be easily achieved by a series connection of MMC sub-modules (SMs). In addition, a MMC topology can provide high power quality and efficiency with reduced size of passive filters. These features made the MMC option an attractive topology for the MV stage of the SST [2.6]-[2.7]. The main goal of this thesis is to develop and implement in Matlab/Simulink the model of a bidirectional three-stage MMC-based SST which can provide an efficient performance under various operating conditions. Figure 2.1 shows the schematic configuration of the bidirectional three stage SST design, which consists of three main stages: medium voltage stage, isolation stage, and low voltage stage.

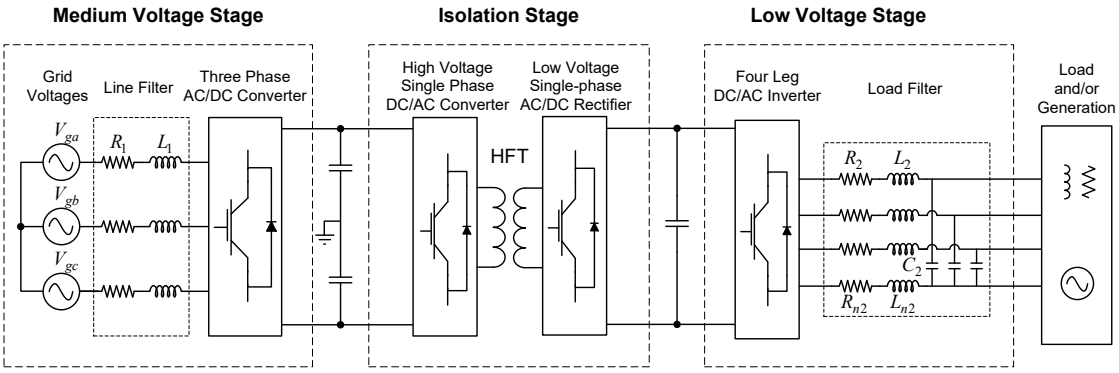


Figure 2.1. Schematic configuration of the three-stage SST design.

When the power flows from the MV side to the LV side, the input power-frequency ac voltage is converted into a MV dc voltage by the three-phase ac/dc converter, which in such case works as rectifier. The isolation stage, which includes a high-frequency transformer (HFT) and the two corresponding MV- and LV-side converters, first converts the MV-side dc voltage into a high-frequency square-wave voltage applied to the primary of the HFT; the secondary side square-wave signal is then converted to a LV dc waveform by the LV-side converter, which also works as rectifier. Finally, the output LV-side three-phase dc/ac converter, which works as inverter, provides the output power-frequency ac waveform from the LV-side dc link. The MV side (hereinafter known as *input stage*) is connected to a MV distribution grid, while the LV side (hereinafter known as *output stage*) is assumed to be connected to a LV grid to which both load and generation might be connected. When the power flows from the LV side to the MV side (i.e. the LV generation is predominant), the SST behavior is similar to that described above; basically, input and output stages swap functions. The rest of this section provides a summary of the configuration selected for each stage and the corresponding controllers.

In this work, a three-phase MMC with half-bridge SMs is used for input stage. A voltage oriented control (VOC) strategy has been used to generate proper reference signals; a level-shifted PWM method is used as modulation technique. In addition, a sorting algorithm technique is used for balancing the SM capacitance voltages.

The isolation stage is divided into three parts: a single-phase MMC, a HFT and a single-phase bidirectional PWM converter. An open-loop level-shifted PWM and a sorting algorithm have been used to control the MV single-phase MMC, while a proportional-resonant (PR) based control is applied to the LV single-phase bidirectional PWM converter.

A three-phase four-leg converter is used for the output stage. A VOC strategy with a three-dimensional SVM (3-D SVM) modulation technique has been implemented to generate proper reference signals.

2.2. Input Stage: Configuration and Control

2.2.1. Introduction

The MV stage of the SST is connected to a three-phase AC distribution system via RL filters. Figure 2.2 shows the configuration of the three-phase MMC selected for this work. If it is assumed the power flows from the MV side to the LV side of the SST, the MV-side MMC acts as a rectifier that converts the ac voltage of the grid to a dc voltage. In case of power flow reversal, the MMC passes to act as inverter that passes the DC voltage of the input stage DC link to AC voltage at power frequency. As it can be seen from Figure 2.2, each leg of three-phase MMC consists of two upper and lower arms with n similar series connected sub module (SM), an arm resistance (R_{arm}) and an arm inductance (L_{arm}). Different types of SMs such as half bridge converter, full bridge converter, three level neutral point clamp (NPC) converter, three level flying capacitor (FC) converter and different topologies of cross connected converters can be used in MMC [2.8]-[2.10]. In this work, half bridge converter is used as SM for MMC. Figure 2.3 shows the different states for operation of half bridge SM regarding to current direction. As it can be seen from this figure, half- bridge SM comprises of two IGBT switches s_1 and s_2, and a capacitor as a DC source with voltage of V_c, s_1, and s_2 are switched in complementary manner.

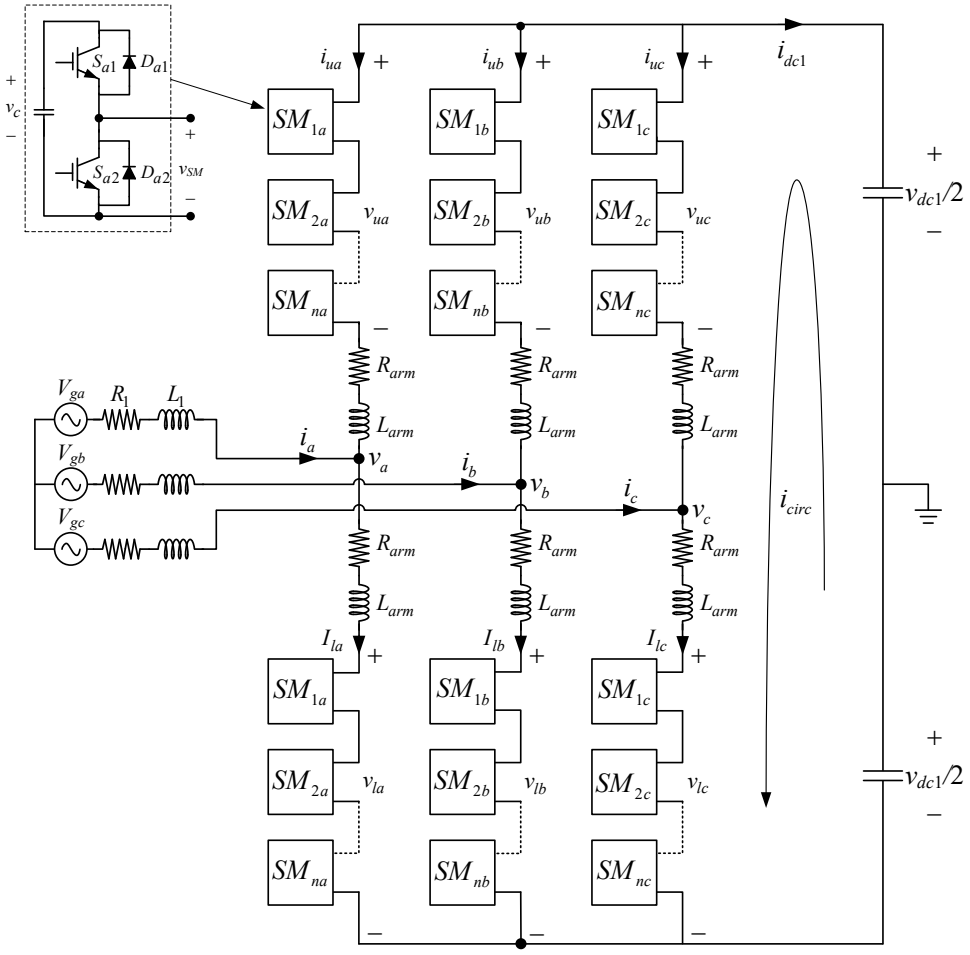


Figure 2.2. Configuration of the three-phase input stage.

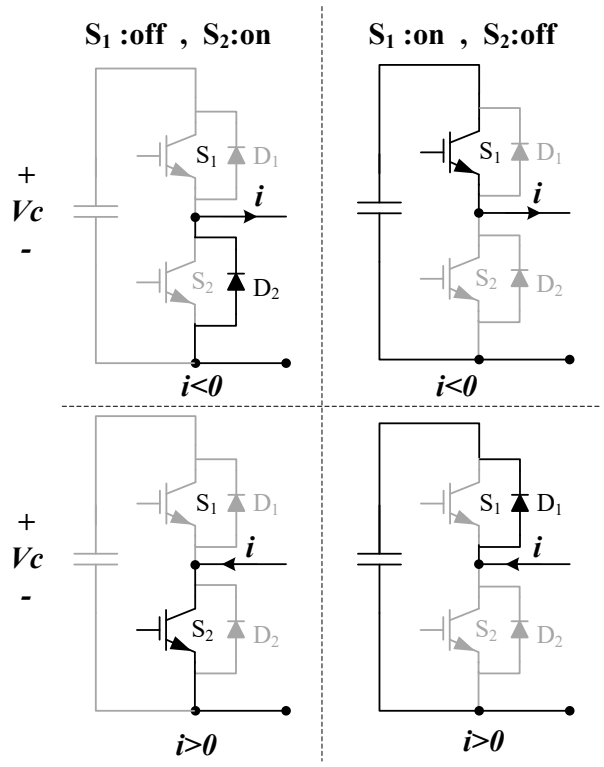


Figure 2.3. Different states of operation for half bridge SM.

When the switch s_1 is on the voltage of SM is equal to V_c, and it is said that SM is inserted. When the switch s_2 is on the voltage of SM is equal to zero and it is said that SM is bypassed. Also, when the current inserts from positive polarity of capacitor, the capacitor is charged and when the current inserts from negative polarity of capacitor, the capacitor is discharged. Since in MMC topology each arm should have the capability to work with total dc link voltage, the value of each SM capacitance voltage must be:

$$v_{cSM} = \frac{v_{dc}}{n} \tag{2.1}$$

2.2.2. Mathematical model

To better analyze the model of the MV-side MMC, Figure 2.4 shows the interaction of one MMC leg and the MV DC link [2.11]-[2.12].

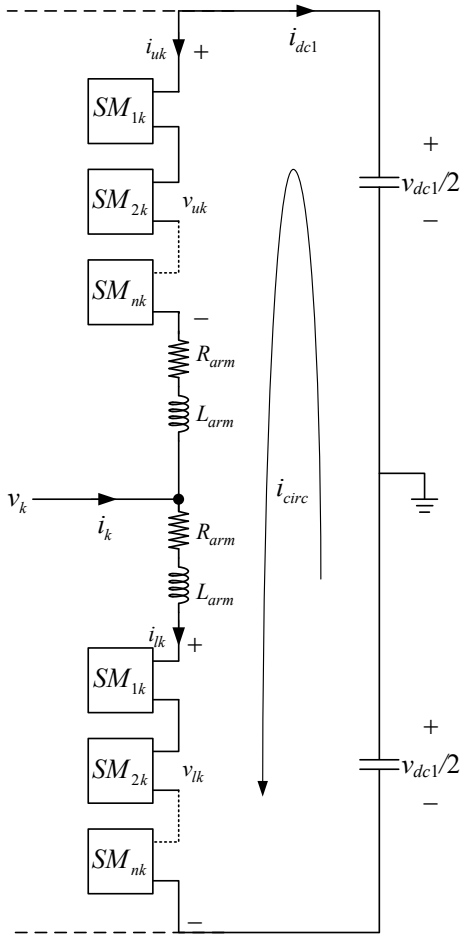


Figure 2.4. One leg configuration of the input stage MMC.

The current of the upper and lower arms of the phase k, ($k = a, b, c$), i_{uk} and i_{lk}, can be expressed as:

$$i_{uk} = i_{circ} - \frac{i_k}{2} \tag{2.2}$$

$$i_{lk} = i_{circ} + \frac{i_k}{2} \tag{2.3}$$

where i_k is the input current of phase k, and i_{circ} is the circulating current which can be achieved through adding (2.2) and (2.3):

$$i_{circ} = \frac{i_{uk} + i_{lk}}{2} \tag{2.4}$$

Upper and lower voltages of the phase k, v_{uk} and v_{lk} can be expressed as:

$$v_{uk} = \frac{v_{dc1}}{2} - v_k - R_{arm} i_{uk} - L_{arm} \frac{di_{uk}}{dt} \tag{2.5}$$

$$v_{lk} = \frac{v_{dc1}}{2} + v_k - R_{arm} i_{lk} - L_{arm} \frac{di_{lk}}{dt} \tag{2.6}$$

where v_k is the voltage of phase k at the ac side of the MMC, R_{arm} and L_{arm} are respectively the resistance and inductance of each MMC arm.

By subtracting (2.6) from (2.5) and substituting i_{uk} and i_{lk} from (2.2)-(2.3), the following form for v_k is obtained:

$$v_k = \frac{v_{lk} - v_{uk}}{2} + \frac{R_{arm} i_k}{2} + \frac{L_{arm}}{2} \frac{di_k}{dt} \tag{2.7}$$

As it can be seen from Figure 2.2:

$$v_{gk} = v_k + R_1 i_k + L_1 \frac{di_k}{dt} \tag{2.8}$$

where R_1 and L_1 are the resistance and inductance of the input filters. Upon substituting (2.7) in (2.8) the following equation is obtained:

$$v_{gk} = \frac{v_{lk} - v_{uk}}{2} + \frac{R_{arm} i_k}{2} + \frac{L_{arm}}{2} \frac{di_k}{dt} + R_1 i_k + L_1 \frac{di_k}{dt} \tag{2.9}$$

An equivalent circuit of the MMC can be derived from these results (see figure 2.5). By using the following forms [2.13]:

$$v_{eq} = \frac{v_{lk} - v_{uk}}{2} \tag{2.10}$$

$$R_{eq} = R_1 + \frac{R_{arm}}{2} \tag{2.11}$$

$$L_{eq} = L_1 + \frac{L_{arm}}{2} \tag{2.12}$$

equation (2.9) becomes:

$$v_{gk} = v_{eq} + R_{eq} i_k + L_{eq} \frac{di_k}{dt} \tag{2.13}$$

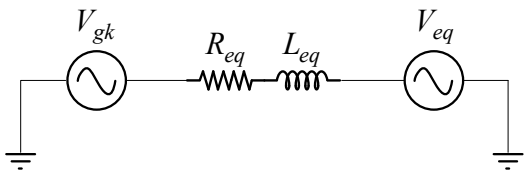


Figure 2.5. Equivalent circuit of a MMC [2.13].

2.2.3. Medium-voltage side control

A VOC strategy has been selected to generate proper reference signals for the modulation technique implemented in this work. The positive-sequence grid voltage is used to obtain the grid angle for synchronization purposes by means of a phase-locked loop (PLL).

The block diagram is shown in Figure 2.6; the VOC scheme provides the reference voltage of phase k, v_k^* [2.14]-[2.15]. From equations (2.5) and (2.6) and upon neglecting voltage drop across the arm impedance, the reference voltages for upper and lower arms of phase k, v_{uk}^* and v_{lk}^*, are obtained as follows:

$$v_{uk}^* = \frac{v_{dc1}}{2} - v_k^* \tag{2.14}$$

$$v_{lk}^* = \frac{v_{dc1}}{2} + v_k^* \tag{2.15}$$

Level shifted modulation: Different modulation techniques, such as level-shifted PWM, phase shifted PWM, phase disposition PWM, selective harmonic elimination, space vector modulation (SVM), or nearest level modulation (NLM) have been developed to control MMCs [2.16]-[2.19].

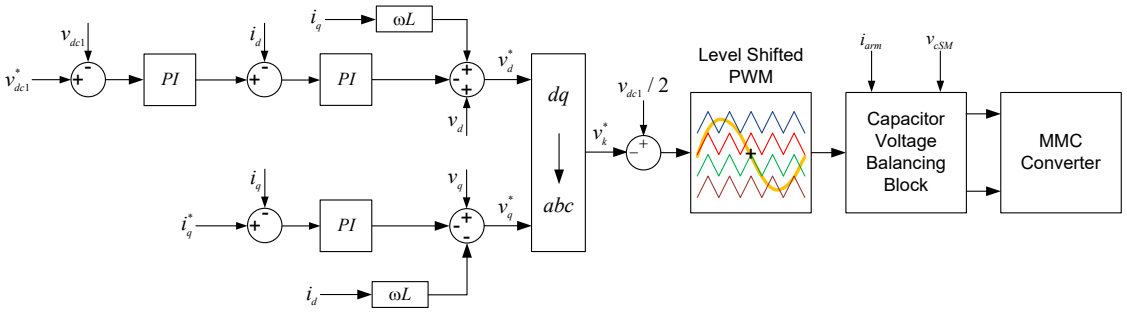


Figure 2.6. Control diagram of three-phase input stage MMC controller**.**

A level-shifted PWM strategy is used in this work [2.20]; see Figure 2.6. The reference voltages of phase arms are compared to n triangle carriers to generate the desired (n+1) output voltage levels. In this modulation technique the number of inserted SMs in upper and lower arms (n_u and n_l) are always controlled so that n SMS are inserted in each leg at any instant; therefore:

$$n_u + n_l = n \tag{2.16}$$

If the MMC converter has n SMs in each arm (see Fig 2.2), then n in-phase carrier waveforms are compared with the reference waveform of each phase as depicted in Figure 2.6.

Table 2.1 shows the different generated level for output phase voltage of one leg [2.20] when the number of SMs per arm is 6. Remember that to generate a 7-level phase voltage, the number of inserted SMs in upper and lower arms is always 6.

Table 2.1. Switching levels for each MMC leg

Level	n_u	n_l	v_{ko}
1	6	0	$-\frac{V_{dc}}{2}$
2	5	1	$-\frac{V_{dc}}{3}$
3	4	2	$-\frac{V_{dc}}{6}$
4	3	3	0
5	2	4	$+\frac{V_{dc}}{6}$
6	1	5	$+\frac{V_{dc}}{3}$
7	0	6	$+\frac{V_{dc}}{2}$

Capacitance balancing: Under practical conditions, the voltage of a SM capacitance changes due to charging/discharging states, variation of current values and different conduction times of switches. This may lead to undesired consequences such as unbalanced voltages and higher harmonic distortion. Therefore, an algorithm for proper capacitance voltage balancing must be used to keep the voltage of each arm at the desired level.

The sorting algorithm used in this work for SM capacitance voltage balancing is that proposed in [2.21]. Figure 2.7 shows the flowchart for the voltage balancing algorithm, based on that proposed in [2.20] and [2.21].

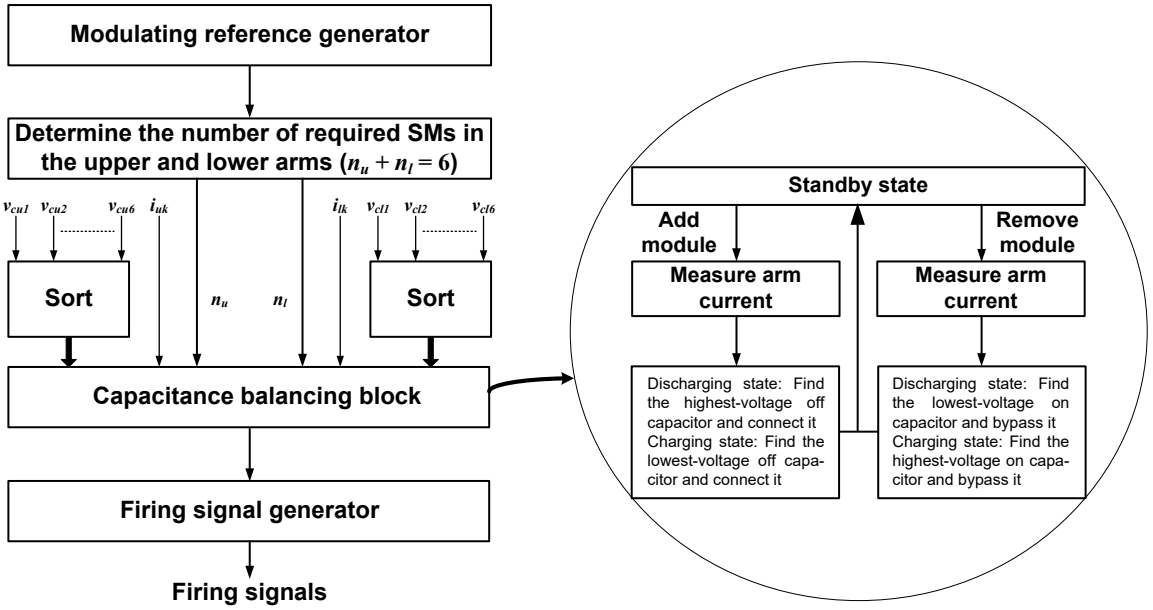


Figure 2.7. Control block diagram and sorting algorithm for MMC converter.

As shown in Figure 2.7, the algorithm block has three inputs: SM capacitor voltages of each MMC arm (which are monitored and sorted in descending order), the current direction of each MMC arm (if the arm current is positive, it is then charging SMs, which are therefore increasing their voltages; if the arm current is negative, it is then discharging SMs, which are therefore decreasing their voltages), and the level number determined by the level-shifted PWM technique (see Table 2.1).

Based on a sorting algorithm when the modulator decides to insert a SM, then SMs with minimum/maximum capacitor voltage will be inserted when the current charges/discharges the corresponding capacitor. Every time the modulator decides to bypass a SM, it is the SM with maximum/minimum capacitor voltage that is bypassed when the current charges/discharges the capacitor.

2.3. Isolation Stage: Configuration and Control

2.3.1. Introduction

The model implemented for representing the isolation stage consists of three major parts (see Figure 2.8): (1) a one-leg single-phase MMC that acts as inverter and generates n+1 level high-frequency input waveform to the HFT (in this work a 7-level, 1 kHz waveform); (2) the HFT, modeled as an ideal transformer in series with its short-circuit impedance; (3) a LV single-phase two-level full-bridge PWM converter that acts as a rectifier and provides the required dc link voltage for the output stage of the SST [2.22].

A short description of the control strategy implemented for the converters at each HFT side is given bellow.

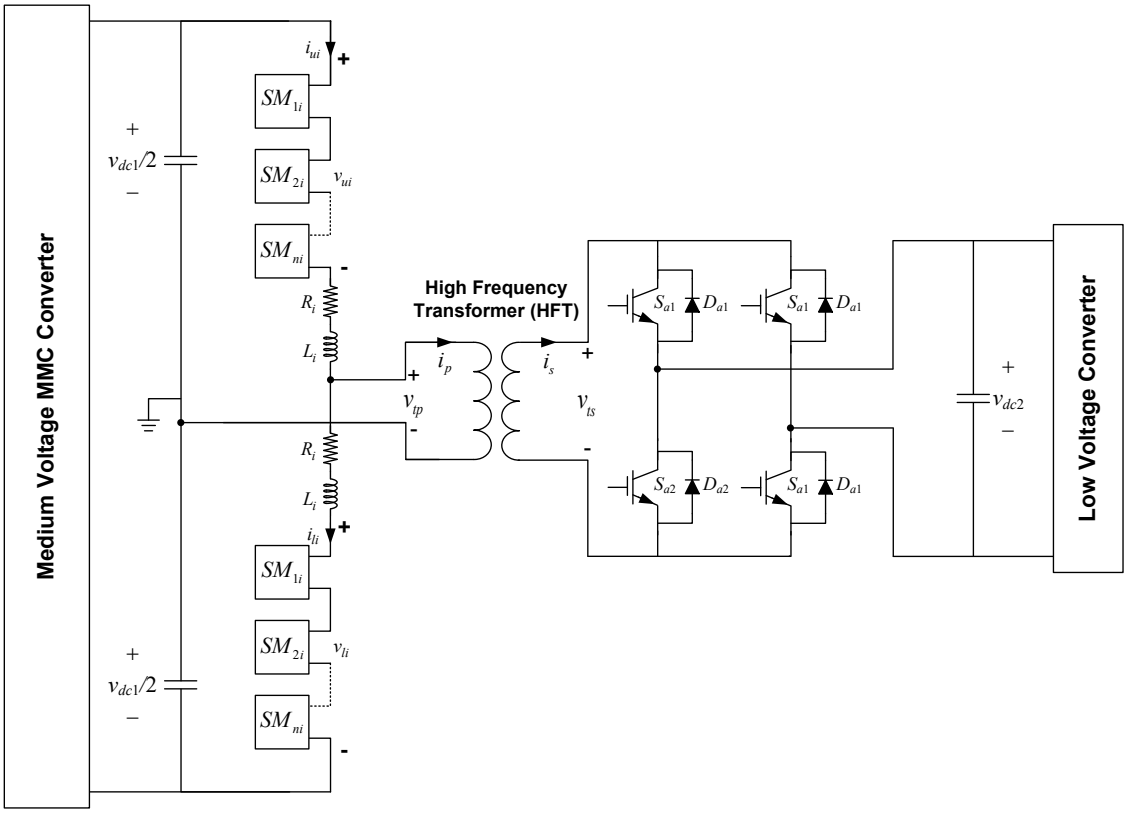


Figure 2.8. Isolation stage configuration.

2.3.2. Single-phase MMC

The control strategy implemented for this single-phase converter is similar to that discussed in the previous subsection. An open-loop level-shifted PWM and a sorting algorithm have been used for controlling the single-phase MMC. The ac reference voltage, v_{tp}^{*}, can be expressed as follows:

$$v_{tp}^{*} = m_a \frac{v_{dc1}}{2} \sin\left(2\pi f_h t\right) \tag{2.17}$$

where m_a is the modulation index of inverter, v_{dc1} is the dc link voltage at the MV side of the SST, and f_h is the operating frequency of the HFT.

The upper and lower arm reference voltages, v_{ui}^{*} and v_{li}^{*}, are obtained as follows:

$$v_{ui}^{*} = \frac{v_{dc1}}{2}\left(1 - m_a \sin\left(2\pi f_h t\right)\right) \tag{2.18}$$

$$v_{li}^{*} = \frac{v_{dc1}}{2}\left(1 + m_a \sin\left(2\pi f_h t\right)\right) \tag{2.19}$$

The level shifted PWM strategy is used to determine the number of SMs to be inserted or bypassed in each arm (n_u and n_l in Table 2.1); after that, the sorting algorithm is used to balance capacitance voltages of SMs and generate gate signals (as shown in Figure 2.7).

2.3.3. High-frequency transformer

The high frequency transformer (HFT) is required to achieve electric isolation. It also has to allow large voltage and current ratios between input and output. The usage of a HFT in the SST is the main reason for size reduction in comparison with the conventional transformers operating at power frequency (i.e. 50-60 Hz). Therefore, an optimized design of HFT in DAB is necessary to utilize the advantages of SST [2.23].

Many design considerations and challenges should be taken in to account in order to satisfy high-voltage, high-power and high-frequency operation of isolation-stage transformer. The first challenge is the selection of the magnetic material which should be adequate for providing high power density and low loss. The second challenge is the configuration of core and windings since they will have a considerable effect on the efficiency at high frequency. The third challenge is the thermal design which should avoid the breakdown of the device in high-voltage and high-power application. Finally, insulation requirement is very important in high-voltage application and compact design, mainly when the oil is eliminated [2.24]. Papers [2.25]-[2.29] present the design and optimization of transformers for SST applications.

2.3.4. Single-phase two-level full-bridge converter

The LV single-phase two-level bridge rectifies the output current of the HFT (i_s) and controls the LV-side dc link voltage (v_{dc2}) at the desired value. The diagram of the controller is shown in Figure 2.9 [2.30]-[2.31]. The dc link voltage v_{dc2} is compared to

its reference value and the resulting error is applied to a PI controller. The output signal of PI controller is used to generate the reference current (i_s^*).

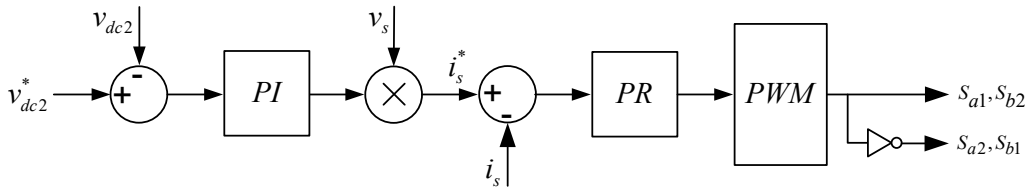


Figure 2.9. Diagram of the single-phase isolation stage MMC controller.

The error ($i_s^* - i_s$) is applied to a PR controller to generate the reference value for PWM block. The PR technique can successfully replace the typical PI-dq control scheme for three-phase systems exhibiting some advantages (e.g., improved harmonic rejection capability). In addition, a PR controller can provide a fast control with a structure simpler than other controllers such as PI control, hysteresis current control and predictive current control. A bidirectional PWM technique is applied to generate switching pulses [2.30]-[2.31].

2.4. Output Stage: Configuration and Control

2.4.1. Introduction

Four-leg converter topology is an efficient choice for applications that require accurate control for neutral current, controlled rectifier. Adding an extra leg provides a degree of freedom and better control capability in comparison with conventional three-leg converter [2.32]-[2.33].

In this thesis a three-phase four-leg PWM converter is proposed for the LV side of the SST, with an *RL* impedance for filtering currents and a capacitor bank for filtering voltages, see Figure 2.10.

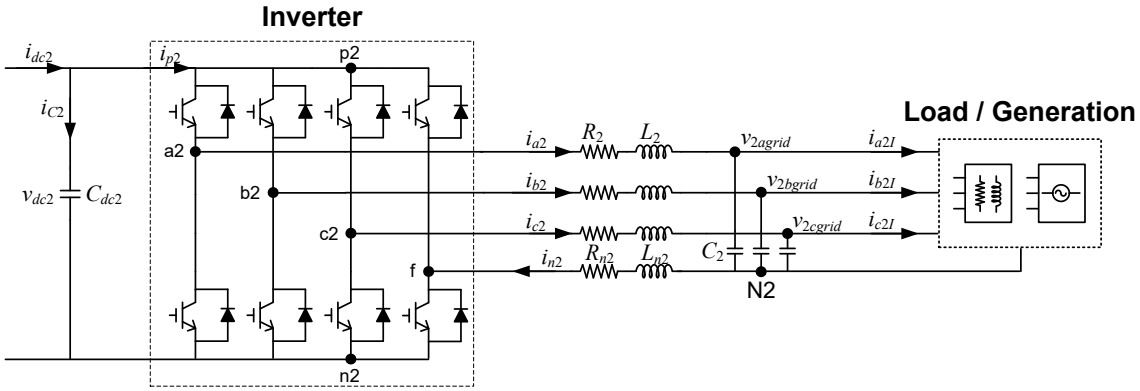


Figure 2.10. Low-voltage side converter configuration.

The main task of LV-side converter controllers is to achieve positive-sequence capacitor voltages (i.e., to obtain balanced voltages at capacitor terminals) with stable frequency and voltage, independently of the load/generation level and the unbalance of LV-side currents. Each positive-, negative- and zero-sequence has its corresponding controller; negative- and zero-sequence capacitor voltage references are permanently set

to zero to cancel these components at the filter capacitor terminals, even in presence of unbalanced load/generation currents. The positive-sequence voltage controller regulates the filter capacitor voltages.

Different types of load/generation including nonlinear load which generate harmonics, two phase load/generation which is unbalanced load can be connected to this converter. Moreover, short circuit fault may occur at the terminal of load. Thus, a universal PWM control strategy using VOC has been implemented for this converter in order to provide efficient voltage and current at the secondary side of SST in different types of transient states, load connection or fault conditions.

The converter model and its control strategy developed for this work are discussed in detail, bellow.

2.4.2. Mathematical model

The implemented VC method is aimed at generating proper references for three dimensional SVM (3-D SVM) modulation technique. The control model considers positive-, negative-, and zero-sequences [2.34]:

$$\begin{aligned}\frac{di_{d2p}}{dt} &= \omega_2 i_{q2p} - \frac{R_2}{L_2} i_{d2p} + \frac{1}{L_2}(\mathrm{v}_{d2pconv} - \mathrm{v}_{d2pgrid}) \\ \frac{di_{q2p}}{dt} &= -\omega_2 i_{d2p} - \frac{R_2}{L_2} i_{q2p} + \frac{1}{L_2}(\mathrm{v}_{q2pconv} - \mathrm{v}_{q2pgrid})\end{aligned} \tag{2.20a}$$

$$\begin{aligned}\frac{di_{d2n}}{dt} &= -\omega_2 i_{q2n} - \frac{R_2}{L_2} i_{d2n} + \frac{1}{L_2}(\mathrm{v}_{d2nconv} - \mathrm{v}_{d2ngrid}) \\ \frac{di_{q2n}}{dt} &= \omega_2 i_{d2n} - \frac{R_2}{L_2} i_{q2n} + \frac{1}{L_2}(\mathrm{v}_{q2nconv} - \mathrm{v}_{q2ngrid})\end{aligned} \tag{2.20b}$$

$$\frac{di_0}{dt} = -\frac{R_2 + 3R_{n2}}{L_2 + 3L_{n2}} i_{d2n} + \frac{1}{L_2 + 3L_{n2}}(\mathrm{v}_{0conv} - \mathrm{v}_{0grid}) \tag{2.20c}$$

$$\begin{aligned}\frac{dv_{d2pgrid}}{dt} &= \omega_2 v_{q2p} + \frac{1}{C_2}(i_{d2p} - i_{d2lp}) \\ \frac{dv_{q2pgrid}}{dt} &= -\omega_2 v_{d2p} + \frac{1}{C_2}(i_{q2p} - i_{q2lp})\end{aligned} \tag{2.20d}$$

$$\begin{aligned}\frac{dv_{d2ngrid}}{dt} &= -\omega_2 v_{q2p} + \frac{1}{C_2}(i_{d2n} - i_{d2\mathrm{ln}}) \\ \frac{dv_{q2ngrid}}{dt} &= +\omega_2 v_{d2p} + \frac{1}{C_2}(i_{q2n} - i_{q2\mathrm{ln}})\end{aligned} \tag{2.20e}$$

$$\frac{dv_{0grid}}{dt} = \frac{1}{C_2}(i_0 - i_{0l}) \tag{2.20f}$$

where i_{d2p}, i_{q2p} are the positive-sequence LV-side converter currents in the rotating *dq* frame; i_{d2n}, i_{q2n} are the negative-sequence LV-side converter currents in the rotating *dq* frame; i_0 is the zero-sequence LV-side converter current; i_{d2lp}, i_{q2lp} are the positive-

sequence LV-side load/generation currents in the rotating *dq* frame; i_{d2ln}, i_{q2ln} are the negative-sequence LV-side load/generation currents in the rotating *dq* frame; i_{0l} is the zero-sequence LV-side load/generation current; $v_{d2pconv}$, $v_{q2pconv}$ are the positive-sequence converter voltages in the rotating *dq* frame; $v_{d2nconv}$, $v_{q2nconv}$ are the negative-sequence converter voltages in the rotating *dq* frame; v_{0conv} is the zero-sequence converter voltages; $v_{d2pgrid}$, $v_{q2pgrid}$ are the positive-sequence capacitor filter voltages in the rotating *dq* frame; $v_{d2ngrid}$, $v_{q2ngrid}$ are the negative-sequence capacitor filter voltages in the rotating *dq* frame; v_{0grid} is the zero-sequence capacitor filter voltage; ω_2 is the LV-side grid angular frequency; R_2 is the LV-side filter resistance; L_2 is the LV-side filter inductance; R_{n2} is the LV-side neutral connection resistance; L_{n2} is the LV-side neutral connection inductance.

2.4.3. VOC design for a four-leg converter

In this section the aim is to design a comprehensive control strategy for four leg converter in order to have efficient performance in case of load increment, short circuit fault, unbalanced and nonlinear load connection at the output stage of SST. To achieve this control strategy, the procedure of control design will be studied separately for two case studies: unbalanced and nonlinear load connection. Finally, the comprehensive control strategy will be presented by combining these two control strategies.

Selective harmonic voltage compensation: In this work, an harmonic voltage compensation capability has been added to achieve an efficient performance of SST while connected to nonlinear load that draw currents whose frequencies differ from the frequency of the source.

It must be assumed by default that any harmonic distortion in the output currents is due to nonlinear loads supplied from the LV terminal of the SST; that is, nonlinear loads will draw currents whose frequencies differ from the system frequency. Because the harmonic currents are a result of the nature of the loads, it is appropriate to consider the load to be a source of harmonic current. As this harmonic components are injected back into the SST, they cause voltage drops (at the corresponding frequencies), creating voltage distortion in the output voltages. This voltage distortion is a direct function of the current harmonic component magnitudes and the equivalent impedance of the SST output stage. Since the SST load can include linear and nonlinear loads, the harmonic voltage distortion caused by nonlinear loads can affect the behavior of linear loads; therefore, the goal is to obtain undistorted SST output voltages. Problems caused by harmonic currents and voltages can be solved using different solutions, depending on the source of the problem and the affected equipment. The solutions can be classified into the following groups: solutions to avoid harmonic generation (e.g., by means of some control strategies), solutions to tolerate harmonics (e.g., larger conductors, power equipment de-rating), and solutions to reduce harmonics (e.g., passive and active filters). In this work, the harmonic compensation control strategy has been selected.

Assume the three-phase nonlinear load (in this work three phase diode rectifier) creates harmonics at frequencies $(6n \pm 1)\omega$, where n is any positive, real integer and ω is the fundamental system frequency. It should be noted that that all $(6n+1)\omega$ harmonics are positive sequence, and all $(6n-1)\omega$ harmonics are negative sequence [2.35].

A selective harmonic elimination control strategy can be implemented to compensate voltage harmonics. Since 5th and 7th harmonics are dominant harmonics and, in general, other harmonics can be neglected, the implemented control strategy is

composed of a negative sequence 5th harmonic controller and a positive sequence 7th harmonic controller.

Figure 2.11 displays this control strategy for the 5th and 7th harmonics: the three phase diode rectifier which is selected as nonlinear load in our work, draws nonlinear currents which can lead to harmonics distortion in load voltage with $(6n \pm 1)\omega$, most dominantly 5th and 7th harmonics order. In order to compensate the harmonics of load voltage, specific voltage control loop should be selected for each harmonic order. For selective harmonic compensation (see Figure 2.19): voltage at the terminal of the load measured in *abc* plane is transformed to αβ plane, then the transformed signal is compared with reference value (pure sinusoidal signal with fundamental frequency) and harmonics values are extracted in αβ plane. Regarding to order of harmonic compensation, the extracted error signal will be transformed to dc signals in *dq* plane with transformation angle of $-(6n-1)\theta$ and $+(6n+1)\theta$ for negative and positive sequence harmonic order, respectively. θ is the angular fundamental frequency. The resulted dc signals are passed through PI controllers to generate reference signals for input current controllers of four leg converter.

Control loop for harmonic compensation of voltage should be created in parallel with positive fundamental frequency control loop of voltage. The output signals of the voltage control block for 1st, 5th and 7th harmonics are added to form the reference signal for current controllers as it can be seen from Figure 2.11 [2.36]-[2.37].

For output current control the generated reference signals from voltage controllers would be compared by real value of current in αβ plane and passed through PR controllers both for fundamental and harmonic components. Figure 2.12 shows the positive sequence control diagram with the capability of harmonic voltage compensation for output stage of SST.

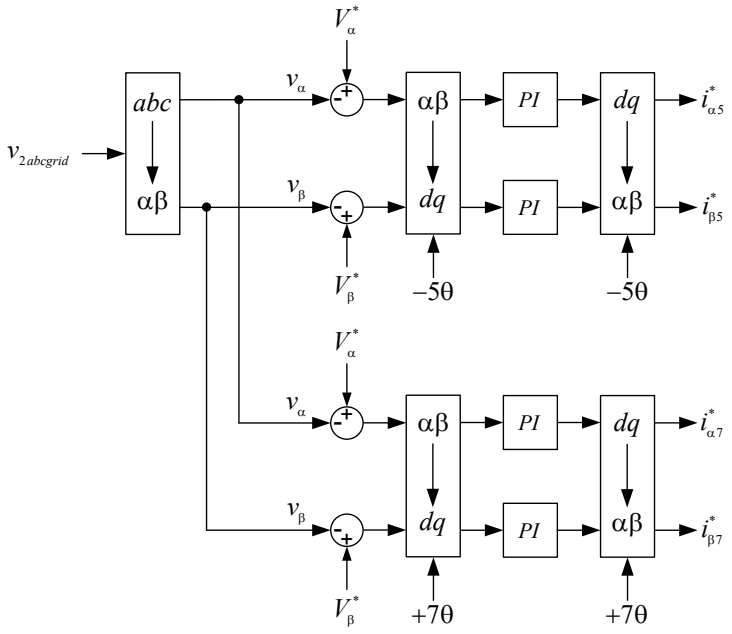


Figure 2.11. Control block diagram for harmonic compensation.

Control design for unbalanced load connection: As it can be observed from Figure 2.10, in four leg converter topology, fourth wire connects midpoint of fourth leg to the neutral point of load. The load unbalance such as two phase load connection leads to

following of current in fourth wire and voltage drop which makes the load voltage asymmetrical. An improved control strategy should be applied in order to provide balanced voltages during the load unbalance.

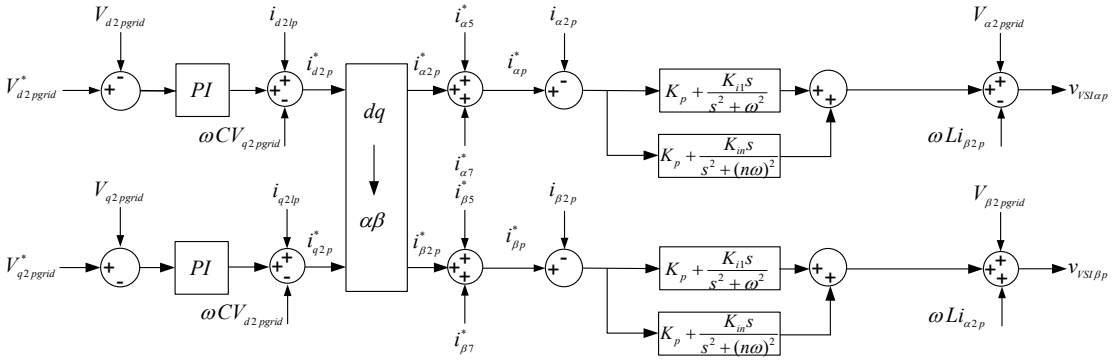


Figure 2.12. Positive sequence control diagram.

It should be noted that, in three-phase VSI control, the d and q channels are used to compensate for the rotating components (positive sequence) of the output variables (voltage and current).

In the control strategy implemented for our work, the variables (output currents and voltages) are decomposed to positive, negative and zero sequence. Then, the negative and zero sequence controllers will be added to positive sequence controllers in control block, to eliminate the negative and zero sequence distortions [2.38].

In conventional control strategy of the four-leg inverter, dq0-component of voltage and current in reference frame rotating at fundamental frequency are used. If the load is balanced, the d-and q-components are dc quantities and the 0-component is zero.

If the load is unbalanced, both d- and q-components contain an additional ac quantity, which oscillates with the double frequency of the output voltage. The 0-component is not zero and oscillates with the same frequency as the output voltage [2.39].

In order to control the negative and zero sequence component of current and voltage which are created due to unbalanced condition, the current and voltage should be transformed into three symmetrical components: positive sequence, negative sequence, and zero sequence. Then, the corresponding controllers are applied to each positive-, negative- and zero-sequence; negative- and zero-sequence capacitor voltage references are permanently set to zero to cancel these components at the filter capacitor terminals in presence of unbalanced load/generation currents.

The positive-sequence voltage controller regulates the filter capacitor voltages. Figure 2.13 shows the controller that includes control blocks for positive, negative and zero sequence, respectively.

As it can be observed from this figure, the voltage and current signals which are achieved after decomposition into symmetrical components and projection into rotating reference frame are regulated in an inner current loop and an outer voltage loop.

Both outer voltage loops and inner current loops are disposed in a three-channel arrangement. The first channel allows controlling the positive sequence of the current and voltage (see Figure 2.12), the second is for the negative sequence, and the third is for the homopolar sequence [2.34].

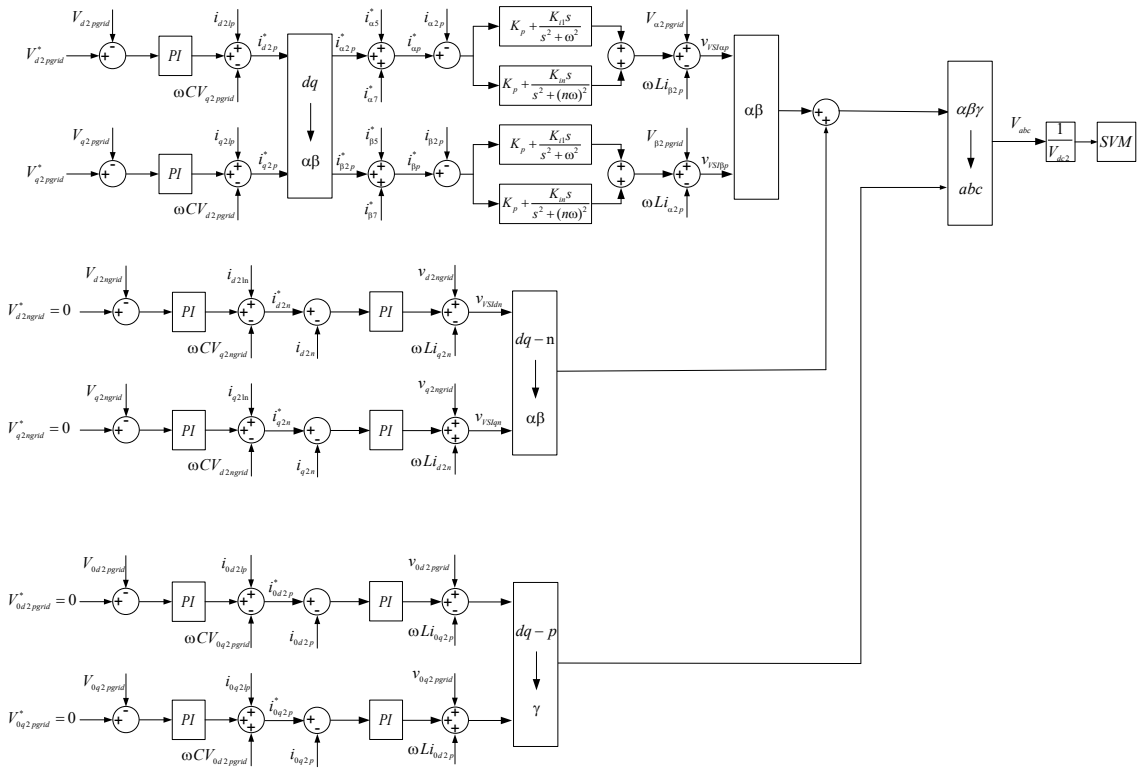


Figure 2.13. Total VOC control diagram for output stage of SST.

2.4.4. Modulation technique

Two-dimensional space vector modulation (SVM) strategy has been used in many studies for three-leg voltage source inverter [2.40]-[2.42]. This modulation uses eight switching vectors (two zero and six nonzero switching vectors) in 2-D hexagon in αβ coordinates. First, the region where voltage vector exists is determined and then the desired voltage is generated by switching active and zero vectors in each specified region.

Adding a fourth leg to a conventional three-leg converter changes the space vector from two dimensions to three dimensions, so the modulation technique becomes more complex. In this work, a 3-D SVM modulation strategy has been implemented in *abc* coordinates. This modulation technique is presented in [2.43]-[2.44]. The advantage of using *abc* coordinates are a much simpler algorithm and a reduced computational time, since there is no need for transformation.

Four leg converter has sixteen switching vectors combinations which are given in Table 2.2. For more simplicity the nominal output voltage vectors (V_{af}, V_{bf}, V_{cf}) are normalized with V_{dc2}. S_a, S_b, S_c and S_f are the gate signals of upper switch which are equal to 0 when upper switches are off and 1 when upper switches are on. It should be noted that dead times are not included in this strategy.

Sixteen switching vectors that form control region for four leg converter are all in the vertices of two cubes. Vectors V_1 through V_8 are placed in the positive region, while vectors V_9 trough V_{16} are placed in the negative region forming a dodecahedron in *abc* coordinates.

Table 2.2. Switching table of the four-leg converter

Switching state	S_f	S_a	S_b	S_c	V_{af}	V_{bf}	V_{cf}	Switching vector
1	0	0	0	0	0	0	0	V_1
2	0	0	0	1	0	0	1	V_2
3	0	0	1	0	0	1	0	V_3
4	0	0	1	1	0	1	1	V_4
5	0	1	0	0	1	0	0	V_5
6	0	1	0	1	1	0	1	V_6
7	0	1	1	0	1	1	0	V_7
8	0	1	1	1	1	1	1	V_8
9	1	0	0	0	-1	-1	-1	V_9
10	1	0	0	1	-1	-1	0	V_{10}
11	1	0	1	0	-1	0	-1	V_{11}
12	1	0	1	1	-1	0	0	V_{12}
13	1	1	0	0	0	-1	-1	V_{13}
14	1	1	0	1	0	-1	0	V_{14}
15	1	1	1	0	0	0	-1	V_{15}
16	1	1	1	1	0	0	0	V_{16}

Two switching vectors, V_1 and V_{16}, are zero switching vectors (ZSV) while the remaining vectors ($V_2 - V_{15}$) are nonzero switching vectors (NZSV). All these vectors divide the control region into 24 tetrahedrons, with three non-zero switching vectors along with the zero switching vector.

The tetrahedron in which the reference vector is included can be selected using:

$$RP = 1 + \sum_{i=1}^{6} c_i 2^{(i-1)} \tag{2.21}$$

where c_i (i = 1- 6) can be achieved as:

$$\begin{aligned} c_1 &= sign(\mathrm{INT}(\mathrm{V}_{aref} + 1)) \\ c_2 &= sign(\mathrm{INT}(\mathrm{V}_{bref} + 1)) \\ c_3 &= sign(\mathrm{INT}(\mathrm{V}_{cref} + 1)) \\ c_4 &= sign(\mathrm{INT}(\mathrm{V}_{aref} - \mathrm{V}_{breff} + 1)) \\ c_5 &= sign(\mathrm{INT}(\mathrm{V}_{bref} - \mathrm{V}_{creff} + 1)) \\ c_6 &= sign(\mathrm{INT}(\mathrm{V}_{aref} - \mathrm{V}_{creff} + 1)) \end{aligned} \tag{2.22}$$

V_{aref}, V_{bref}, and V_{cref} are normalized reference voltages.

All the 24 tetrahedrons, with their RP indexes, and the three nonzero switching vectors are given in Table 2.3.

Table 2.3. Region pointer for 24 tetrahedrons and their corresponded non-zero switching vectors

RP	V_{d1}	V_{d2}	V_{d3}	*RP*	V_{d1}	V_{d2}	V_{d3}
1	V_9	V_{10}	V_{12}	41	V_9	V_{13}	V_{14}
5	V_2	V_{10}	V_{12}	42	V_5	V_{13}	V_{14}
7	V_2	V_4	V_{12}	46	V_5	V_6	V_{14}
8	V_2	V_4	V_8	48	V_5	V_6	V_8
9	V_9	V_{10}	V_{14}	49	V_9	V_{11}	V_{15}
13	V_2	V_{10}	V_{14}	51	V_3	V_{11}	V_{15}
14	V_2	V_6	V_{14}	52	V_3	V_7	V_{15}
16	V_2	V_6	V_8	56	V_3	V_7	V_8
17	V_9	V_{11}	V_{12}	57	V_9	V_{13}	V_{15}
19	V_3	V_{11}	V_{12}	58	V_5	V_{13}	V_{15}
23	V_3	V_4	V_{12}	60	V_5	V_7	V_{15}
24	V_3	V_4	V_8	64	V_5	V_7	V_8

After selecting the NZSV, the next step is to perform the proper switching pattern which is based on minimum commutation that leads to lower switching loss. According to this switching strategy, the ZSV is selected Always as the vector V_1 ($V_{d0} = V_1$) and applied at the beginning and the end of switching period. Then, the three NZSV are distributed symmetrically along the middle of the switching period, in the order specified in Table 2.3.

The duty cycles for output desired voltages can be achieved as shown below:

$$
\begin{aligned}
V_{ref} &= \begin{bmatrix} V_{aref} \\ V_{bref} \\ V_{cref} \end{bmatrix} \\
M_d &= \begin{bmatrix} V_{d1a} & V_{d2a} & V_{d3a} \\ V_{d1b} & V_{d2b} & V_{d3b} \\ V_{d1c} & V_{d2c} & V_{d3c} \end{bmatrix} \\
d &= \begin{bmatrix} d_1 \\ d_2 \\ d_3 \end{bmatrix} \\
V_{ref} &= M_d.d, d_0 = 1 - d_1 - d_2 - d_3
\end{aligned}
\tag{2.23}
$$

where d_1, d_2, and d_3 are the duty ratios of the switching vectors, V_{d1}, V_{d2}, V_{d3}, respectively, and d_0 is duty ratio of the zero switching vector.

There are 24 different matrices $[M_{3\times3}]$ corresponding to the 24 tetrahedrons which are saved as a look-up table along with three corresponding vectors.

All elements of matrix M_d, in *abc* coordinates, are 0, 1, or -1. Therefore, all the elements in M_d^{-1} are 0, 1, or -1 as well.

Table 2.4 gives the calculated duty cycles for all 24 tetrahedrons. Once the duty cycles are obtained, the switching intervals can be calculated as T times d_i, where T is the commutation period. The table summarizes all the information required for duty cycles for different 24 tetrahedrons by considering to their region pointer and their values. Three NZSV along with one ZSV are applied in one fundamental period.

Table 2.4. Calculation of duty cycles

RP	V_{d1}	V_{d2}	V_{d3}	d_1	d_2	d_3
1	V_9	V_{10}	V_{12}	$-V_{cref}$	$-V_{bref}+V_{cref}$	$-V_{aref}+V_{bref}$
5	V_2	V_{10}	V_{12}	V_{cref}	$-V_{bref}$	$-V_{aref}+V_{bref}$
7	V_2	V_4	V_{12}	$-V_{bref}+V_{cref}$	V_{bref}	$-V_{aref}$
8	V_2	V_4	V_8	$-V_{bref}+V_{cref}$	$-V_{aref}+V_{bref}$	V_{aref}
9	V_9	V_{10}	V_{14}	$-V_{cref}$	$-V_{aref}+V_{cref}$	$V_{aref}-V_{bref}$
13	V_2	V_{10}	V_{14}	V_{cref}	$-V_{aref}$	$V_{aref}-V_{bref}$
14	V_2	V_6	V_{14}	$-V_{aref}+V_{cref}$	V_{aref}	$-V_{bref}$
16	V_2	V_6	V_8	$-V_{aref}+V_{cref}$	$V_{aref}-V_{bref}$	V_{bref}
17	V_9	V_{11}	V_{12}	$-V_{bref}$	$V_{bref}-V_{cref}$	$-V_{aref}+V_{cref}$
19	V_3	V_{11}	V_{12}	V_{bref}	$-V_{cref}$	$-V_{aref}+V_{cref}$
23	V_3	V_4	V_{12}	$V_{bref}-V_{cref}$	V_{cref}	$-V_{aref}$
24	V_3	V_4	V_8	$V_{bref}-V_{cref}$	$-V_{aref}+V_{cref}$	V_{aref}
41	V_9	V_{13}	V_{14}	$-V_{aref}$	$V_{aref}-V_{cref}$	$-V_{bref}+V_{cref}$
42	V_5	V_{13}	V_{14}	V_{aref}	$-V_{cref}$	$-V_{bref}+V_{cref}$
46	V_5	V_6	V_{14}	$V_{aref}-V_{cref}$	V_{cref}	$-V_{bref}$
48	V_5	V_6	V_8	$V_{aref}-V_{cref}$	$-V_{bref}+V_{cref}$	V_{bref}
49	V_9	V_{11}	V_{15}	$-V_{bref}$	$-V_{aref}+V_{bref}$	$V_{aref}-V_{cref}$
51	V_3	V_{11}	V_{15}	V_{bref}	$-V_{aref}$	$V_{aref}-V_{cref}$
52	V_3	V_7	V_{15}	$-V_{aref}+V_{bref}$	V_{aref}	$-V_{cref}$
56	V_3	V_7	V_8	$-V_{aref}+V_{bref}$	$V_{aref}-V_{cref}$	V_{cref}
57	V_9	V_{13}	V_{15}	$-V_{aref}$	$V_{aref}-V_{bref}$	$V_{bref}-V_{cref}$
58	V_5	V_{13}	V_{15}	V_{aref}	$-V_{bref}$	$V_{bref}-V_{cref}$
60	V_5	V_7	V_{15}	$V_{aref}-V_{bref}$	V_{bref}	$-V_{cref}$
64	V_5	V_7	V_8	$V_{aref}-V_{bref}$	$V_{bref}-V_{cref}$	V_{cref}

Figure 2.14 shows the switching pattern in region number 13. As it can be observed from figure, ZSV is applied at the beginning and the end of the period and three NZSV are applied symmetrically in the middle. d_1, d_2 and d_3 are referred to NZSV duty cycles and d_0 is referred to ZSV duty cycle.

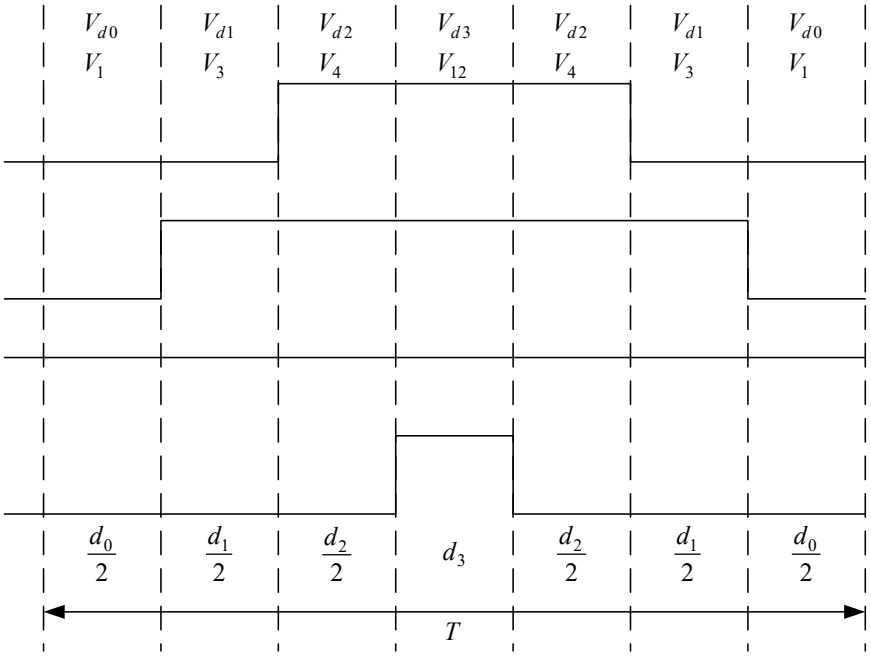


Figure 2.14. duty cycle of output voltages [2.43].

2.5. Modeling of Semiconductor Losses

2.5.1. Introduction

This section presents the approaches followed for implementing losses in semiconductor models. The first part of the section details the calculation of the various types of losses that can occur in semiconductors; the second part illustrates the way in which these losses are included in IGBT and diode models; the last part presents some simulation results. The loss calculation of any semiconductor involves the usage of a thermal model to estimate the semiconductor junction temperature; therefore, the section also includes a part aimed at detailing the implementation of semiconductor thermal models as part of loss calculations.

2.5.2. Loss calculation

There are three types of power losses in semiconductor devices: conduction losses, switching losses, and blocking losses. In general, blocking losses can be neglected, so total semiconductor losses may consist of conduction and switching losses [2.45]-[2.46].

Conduction losses: Conduction losses for IGBT and diodes ($\Delta P_{conS/D}$) can be estimated as follows:

$$\Delta P_{conS/D} = v_{conS/D}(t) \times i_{S/D}(t) \tag{2.24}$$

where $v_{conS/D}$ is the forward semiconductor voltage in conduction mode, and $i_{S/D}$ is the current through the semiconductor.

In this work, $v_{conS/D}$ is obtained from manufacturer's datasheet by using 2-D look up table with 2 inputs: $i_{S/D}$ and $T_{jS/D}$, the semiconductor junction temperature derived from its thermal model. Figure 2.15 shows the model for calculation of conduction losses.

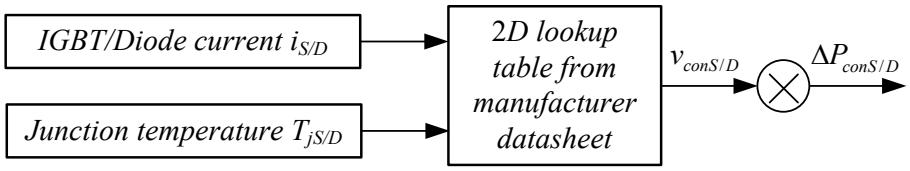


Figure 2.15. Calculation of semiconductor conduction losses.

Switching losses: These losses can be classified into two groups: turn-on and turn-off losses. In general, turn-on losses are neglected for diodes. On the other hand, diode turn-off losses are known as reverse recovery loss. The procedure for implementing each type of loss is detailed below [2-47]-[2-50].

IGBT switching losses: Switching losses occur in IGBTs during turn-on and turn-off commutations. The values of these energy losses can be obtained as follows:

$$E_{onsw} = \int_{t}^{t+t_{on}} v_{CE}(t) \times i_S(t)\, dt \tag{2.25}$$

$$E_{offsw} = \int_{t}^{t+t_{off}} v_{CE}(t) \times i_S(t)\, dt \tag{2.26}$$

where E_{onsw} and E_{offsw} are respectively turn-on and turn-off energy losses, v_{CE} is the voltage across the IGBT, while t_{on} and t_{off} are respectively the turn-on and turn-off commutation time periods.

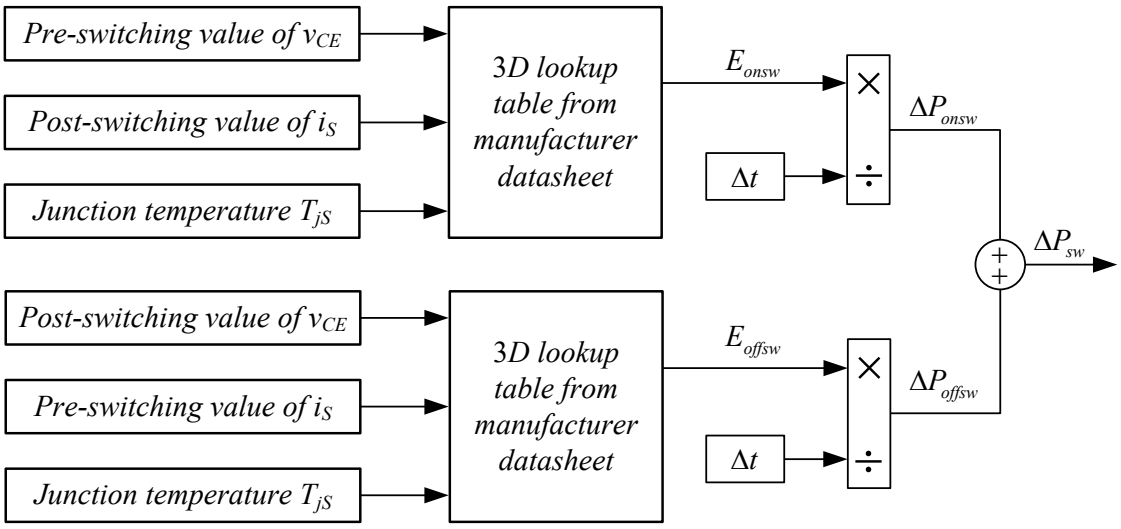


Figure 2.16. Calculation of IGBT switching losses.

Figure 2.16 shows the procedure to obtain total IGBT switching losses, ΔP_{sw}, from manufacturer datasheet. As shown in the figure, the 3D look up table provides the E_{onsw} and E_{offsw} using pre- and post-switching values of current and voltage obtained by interpolating the $E_{on/offsw}$ - i_S curves available in manufacturers' datasheets.

- To obtain E_{onsw}, three input values must be specified: the pre-switching value of the voltage between IGBT collector and emitter, v_{CE}, the post-switching value of the IGBT current, i_S, and the junction temperature of IGBT, T_{jS}.
- To obtain E_{offsw}, three input values must be specified: the pre-switching value of the IGBT current, i_S, the post-switching value of the voltage between IGBT collector and emitter, v_{CE}, and the junction temperature of IGBT, T_{jS}.

Turn-on and turn-off commutation periods of actual IGBTs will be in general different to the time step used in simulations. Switching power losses are averaged at the beginning and the end of a switching period: turn-on switching losses, ΔP_{onsw}, and turn-off switching losses, ΔP_{offsw}, are obtained after dividing turn-on and turn-off energy losses by the simulation time step, Δt (see Figure 2.16 and reference [2.47]):

$$\Delta P_{onsw} = \frac{E_{onsw}}{\Delta t} \tag{2.27}$$

$$\Delta P_{offsw} = \frac{E_{offsw}}{\Delta t} \tag{2.28}$$

With this approach, energy loses are correctly calculated, but instantaneous switching power losses are not. In this paper the simulation time step is 1μs.

Diode switching losses: As for IGBTs, diode reverse recovery losses, ΔP_{recD}, are derived from the reverse recovery energy losses, E_{recD}. The value of these losses during the reverse recovery time, t_{rec}, can be obtained as follows:

$$E_{recD} = \int_{t}^{t+t_{rec}} v_D(t) \times i_D(t)\, dt \tag{2.29}$$

where v_D is the post-switching voltage across the diode.

Figure 2.17 shows the procedure for calculation of diode reverse recovery losses. First, the reverse recovery energy of diode, E_{recD}, is obtained from a 3-D lookup table from manufacturer datasheet; then, the reverse recovery losses, ΔP_{recD}, are averaged after dividing E_{recD} by the simulation time step:

$$\Delta P_{recD} = \frac{E_{recD}}{\Delta t} \tag{2.30}$$

Note that to obtain E_{recD} it is necessary to specify the pre-switching value of the diode current, i_D, the post-switching value of the diode voltage, v_D, and the diode junction temperature, T_{jD}.

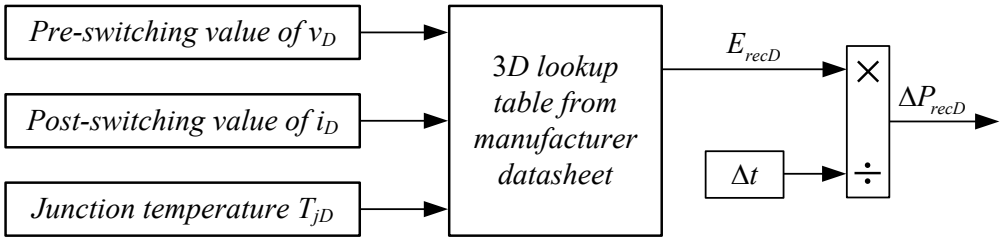


Figure 2.17. Calculation of diode switching losses.

2.5.3. Loss implementation in semiconductor models

Conduction losses: According to equations (2.24) and Figure 2.15, conduction losses of IGBTs and diodes can be obtained from $v_{conS/D}$ and $i_{S/D}$. Therefore, conduction losses, $\Delta P_{conS/D}$, can be incorporated into the semiconductor models by means of a controlled voltage source (with a value equal to $v_{conS/D}$) in series with the ideal semiconductor, either IGBT or diode; see Figures 2.18 and 2.19.

Switching losses: Two different approaches have been used to inject switching losses: (i) the "instantaneous injection" approach used for LV-side semiconductors; (ii) the "average injection" approach used for MV-side semiconductors.

Approach 1: Switching losses in LV semiconductors are implemented by means of controlled sources as follows [2.51]:

- Instantaneous IGBT turn-on switching losses, ΔP_{onsw}, are incorporated by means of a series-connected controlled voltage source, whose value v_{sw1} is obtained from the following equation:

$$v_{sw1} = \frac{\Delta P_{onsw}}{i_S} \tag{2.31}$$

- Instantaneous IGBT turn-off switching losses, ΔP_{offsw}, are incorporated by means of a parallel-connected controlled current source, whose value i_{sw} is obtained from the following equation:

$$i_{sw} = \frac{\Delta P_{offsw}}{v_{CE}} \tag{2.32}$$

- Reverse recovery diode losses, ΔP_{recD}, are incorporated by means of a parallel-connected controlled current source, whose value i_{recD} is obtained from the following equation:

$$i_{recD} = \frac{\Delta P_{recD}}{v_D} \tag{2.33}$$

Figure 2.18 shows the combined model of an IGBT and an antiparallel diode that results from the implementation of this approach.

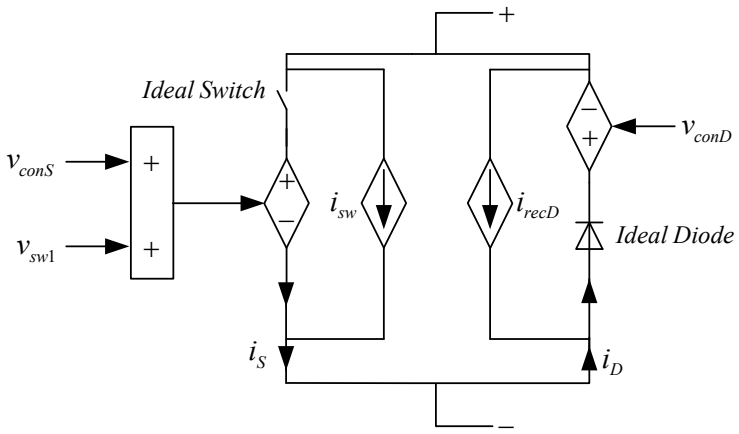
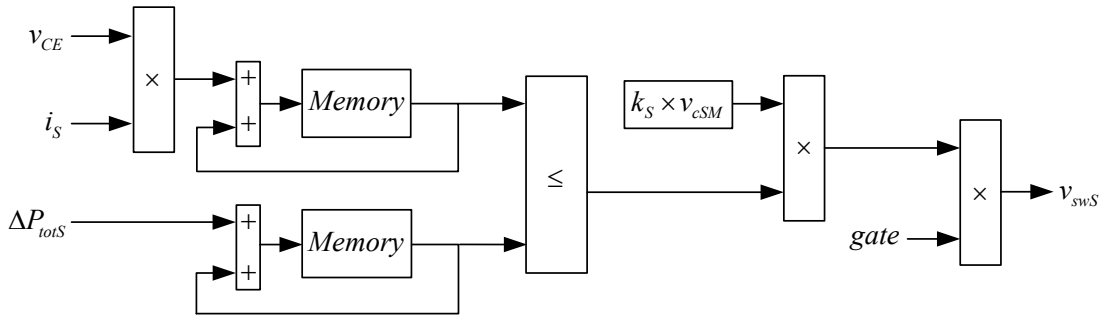


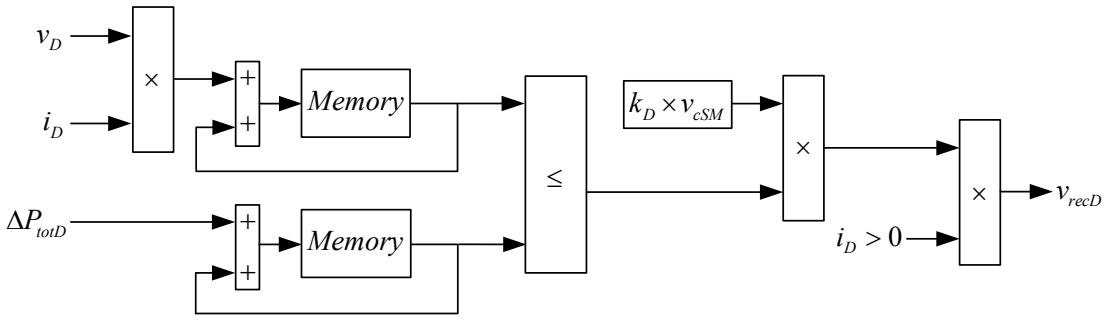
Figure 2.18. Loss model for a combination of LV IGBT and antiparallel diode – Approach 1.

Approach 2: The representation of MV semiconductor switching losses in a single simulation time step, as described above, will usually give high (or very high) values for the controlled voltage source. Since the capacitance of MMC SMs is in series with this voltage source during turn-on time, SM capacitance voltages can get distorted, create unwanted transient conditions, and lead to unstable MMC performance [2.52]-[2.55]. To overcome this problem, the switching losses are represented as a form of conduction losses in several time steps, as proposed in [2.55].

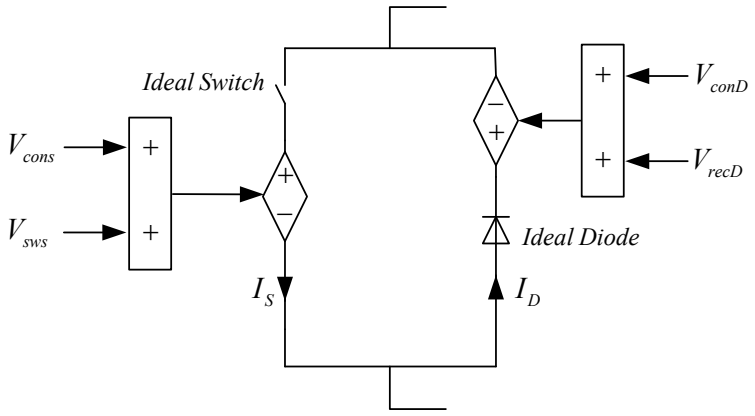
With this approach, smaller values will result for controlled voltage sources; this will solve the capacitance balancing problem issue in MMC converters and also have the capability to properly inject calculated losses in an average manner. The implementation of controlled voltage sources for injection of losses in IGBT and diode are shown in Figure 2.19.a and 2.19.b, respectively.



a) IGBT



b) Diode



c) Average loss model for a combination of MV IGBT and antiparallel diode

Figure 2.19. MV semiconductor loss models – Approach 2.

The values of the instantaneous total losses of IGBTs and diodes, ΔP_{totS} and ΔP_{totD}, are derived as shown below:

$$\Delta P_{totS} = \Delta P_{conS} + \Delta P_{onsw} + \Delta P_{offsw} \tag{2.34}$$

$$\Delta P_{totD} = \Delta P_{conD} + \Delta P_{recD} \tag{2.35}$$

These values are injected by means of a constant controlled voltage source in series with either an IGBT or a diode, and whose value is selected as a percentage, $k_{S/D}$, of the SM capacitance voltage, see Figure 2.19. This means that the controlled voltage source

remains in conduction during a period whose number of time steps is determined by the value of the selected percentage, *k*. As mentioned above, the goal is to obtain a low voltage value for the controlled source and prevent a negative impact on capacitance voltage balancing.

2.5.4. Thermal model

Semiconductors losses acts as a source of heat that affects the junction temperature, whose value will affect semiconductor losses. Therefore, semiconductor thermal models are required for estimating the temperatures that can be reached in IGBTs and diodes, as well as to asses the losses that can be produced [2.56]-[2.58]. For safety reasons, the junction temperature should be always under a maximum value, usually especified by the manufacturer.

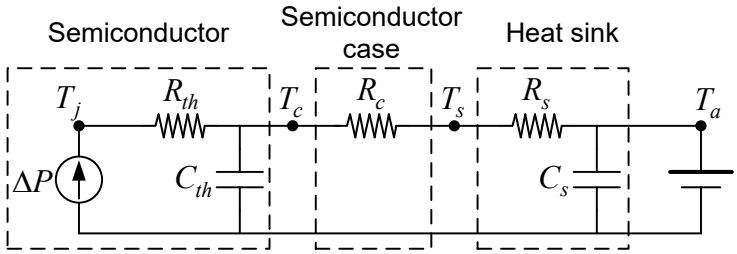
Figure 2.20 shows the thermal models implemented respectively for a single semiconductor and for several semiconductors sharing a common heat sink. As it can be seen from this figure, *RC* circuits have been considered to model the thermal behavior of semiconductors. In these figures, R_{th} and C_{th} are the thermal resistance and capacitance between semiconductor junction and semiconductor case, R_c is the thermal resistance between semiconductor case and heat sink, and R_s and C_s are the thermal resistance and capacitance between heat sink and ambient. T_j, T_c, T_s and T_a are respectively the semiconductor junction temperature, semiconductor case temperature, heat sink temperature, and ambient temperature.

The controlled current source that represents each semiconductor losses in Figure 2.20 is calculated using the procedure detailed above; see Figures 2.15 through 2.17, while the junction temperature in any semiconductor, T_j, is obtained from the models depicted in Figure 2.20 using the procedures shown in Figure 2.21. Note the closed loops that are created when implementing the semiconductor loss calculations from junction temperatures: loss calculations from manufacturer data sheets are derived from the junction temperatures whose values are estimated by means of thermal models in which semiconductor losses are to be specified.

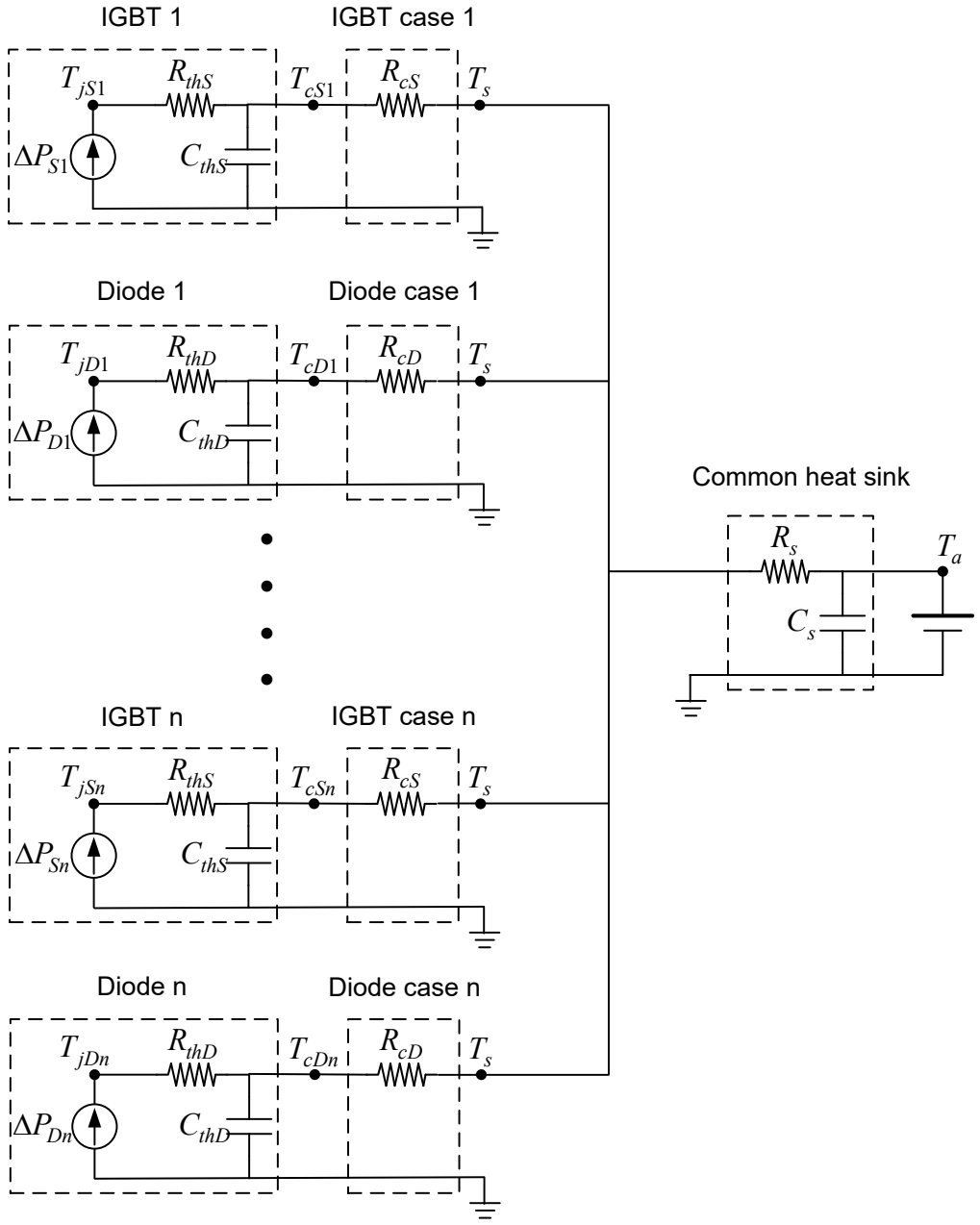
2.5.5. Characterestics of selected semiconductors

Figures 2.22 and 2.23 show the main characteristics of semiconductors selected respectively for for MV- and LV-level converters. Note that the first two plots of each figure are needed to obtain conduction losses and the corresponding curves are specified as a function of the temperature, while the third plot is needed to obtain switching losses.

Additional information required for calculating losses and implementing thermal models is provided in Tables 2.5 and 2.6 for MV and LV-level semiconductors, respectively. In general, thermal resistance values are directly provided in manufacturers' datasheets, and thermal capacitance values have to be derived from thermal time constants also provided in manufacturers' datasheets; see for instance [2.51].
Note that thermal parameters are only specified for LV semiconductors; as justified below the junction temperature for MV-side semiconductors/converters was not derived from thermal models, so these parameters are not required.

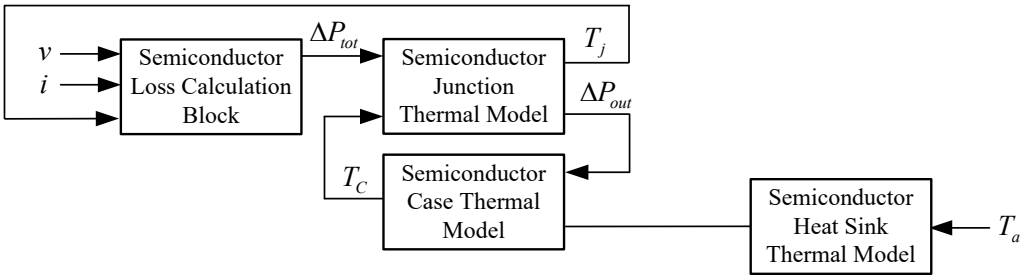


a) Single semiconductor

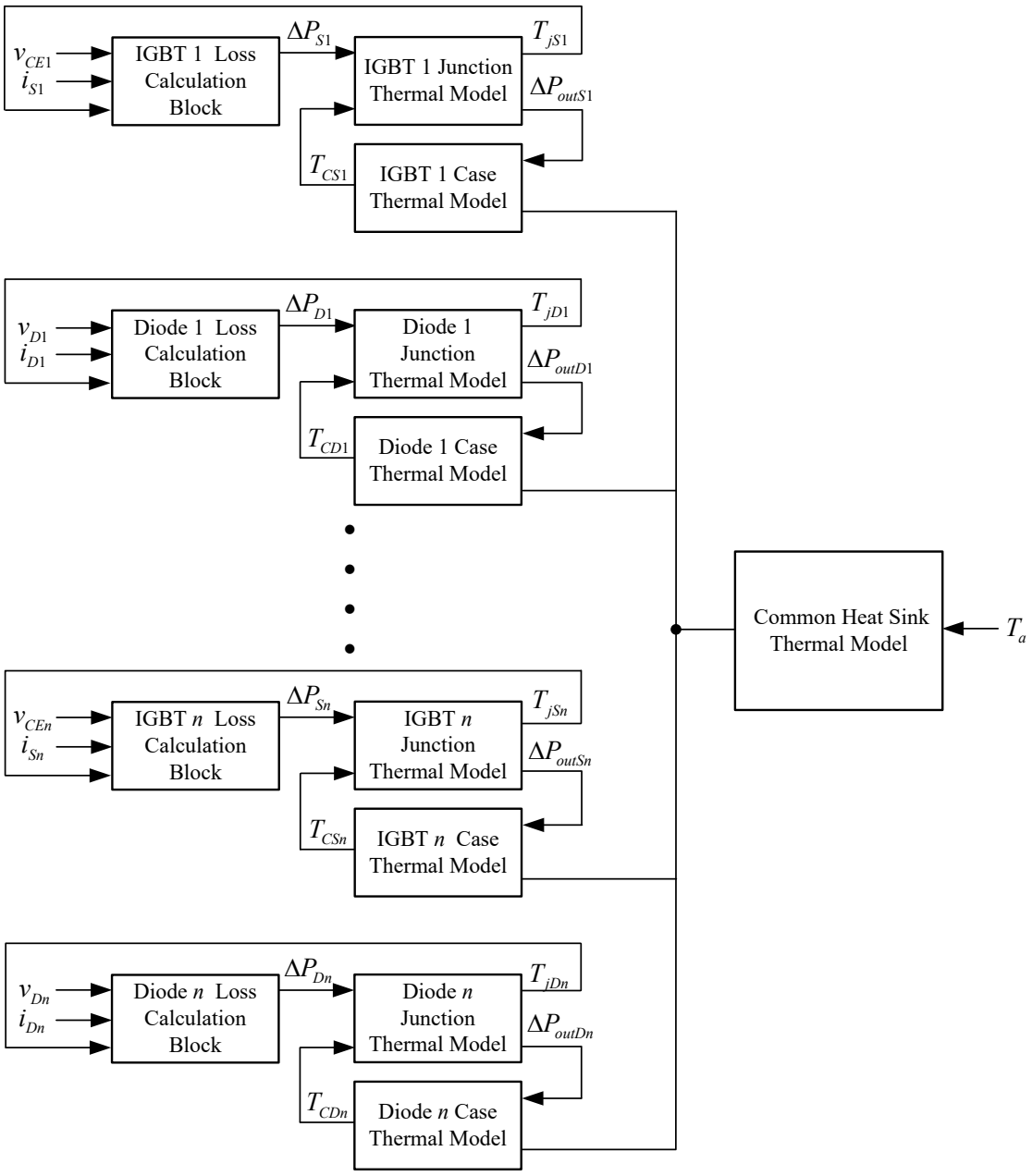


b) Various semiconductors sharing a common heat sink

Figure 2.20. Thermal model of a single LV semiconductor.

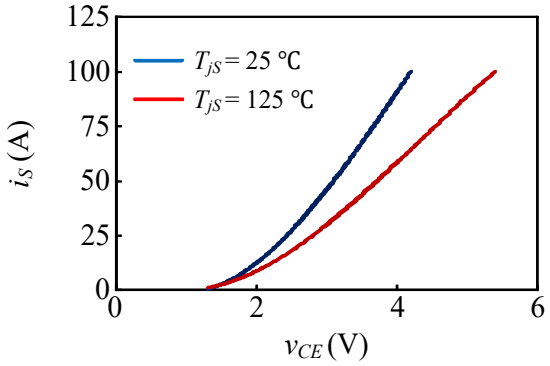


a) Single semiconductor

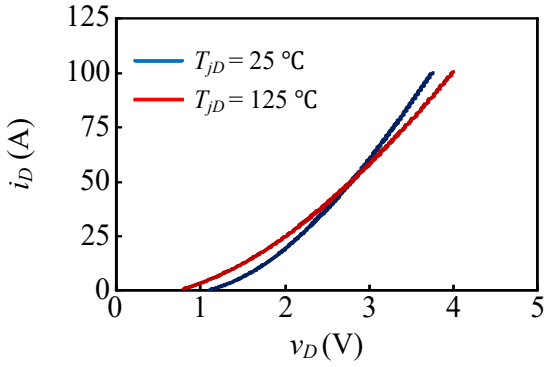


b) Several semiconductors sharing a common heat sink

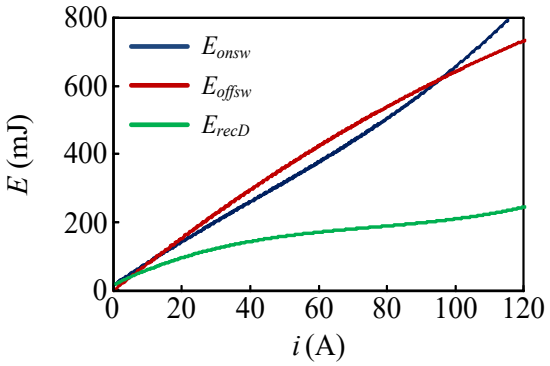
Figure 2.21. Complete thermal model implementation.



a) i_S versus v_{CE}

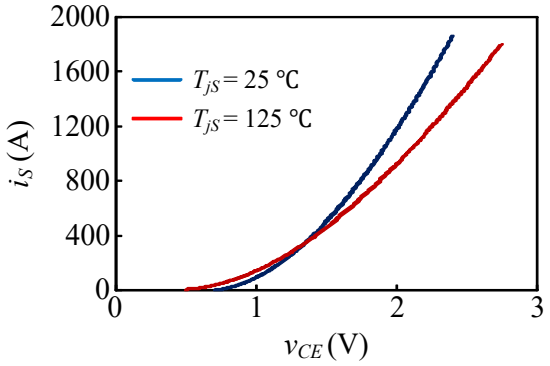


b) i_D versus v_D

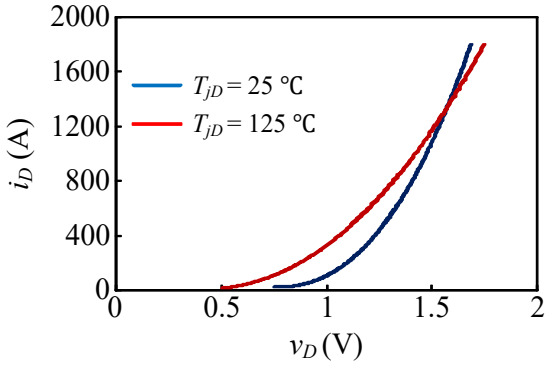


c) E_{onsw}, E_{offsw}, E_{recD} versus i

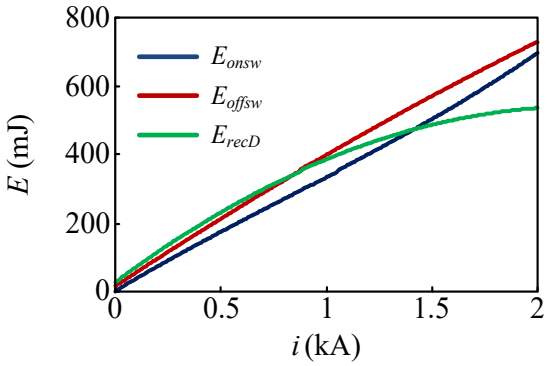
Figure 2.22. Datasheet curves for MV-level semiconductors



a) i_S versus v_{CE}



b) i_D versus v_D



c) E_{onsw}, E_{offsw}, E_{recD} versus i

Figure 2.23. Datasheet curves for LV-level semiconductors

Table 2.5. Characteristics of MV-level semiconductors

Main characteristics	
Parameter	Value
Turn-on delay time (t_{don})	0.63 µs
Rise time (t_r)	0.22 µs
Turn-off delay time (t_{doff})	1.70 µs
Fall time (t_f)	0.98 µs
Reverse recovery time (t_{rec})	0.70 µs

Table 2.6. Characteristics of LV-level semiconductors

Main characteristics	
Parameter	Value
Turn-on delay time (t_{don})	0.30 μs
Rise time (t_r)	0.19 μs
Turn-off delay time (t_{doff})	1.14 μs
Fall time (t_f)	0.17 μs
Reverse recovery time (t_{rec})	0.83 μs
Thermal parameters	
Parameter	Value
Junction to case IGBT thermal resistance (R_{thS})	0.010 ℃/W
Junction to case IGBT thermal capacitance (C_{thS})	0.270 J/℃
Junction to case diode thermal resistance (R_{thD})	0.017 ℃/W
Junction to case diode thermal capacitance (C_{thD})	0.130 ℃

2.6. Conclusion

This chapter has provided a detailed description of a bidirectional three-stage MMC-based SST model considering both ideal (lossless) semiconductors and non-ideal (lossy) semiconductors.

A three-phase MMC with half-bridge SMs is used for the MV input stage. A voltage oriented control (VOC) strategy has been used to generate proper reference signals; a level-shifted PWM method is used as modulation technique. In addition, a sorting algorithm technique is used for balancing the SM capacitance voltages. The MV/LV isolation stage is divided into three parts: a single-phase MMC, a HFT and a single-phase bidirectional PWM converter. An open-loop level-shifted PWM and a sorting algorithm have been used to control the MV single-phase MMC, while a proportional-resonant (PR) based control is applied to the LV single-phase bidirectional PWM converter. A three-phase four-leg converter is used for the LV output stage. A VOC strategy with a three-dimensional SVM modulation technique has been implemented to generate proper reference signals. The control diagram and topology of all three stages are explained in detail in order to implement a SST to have good performance under different case studies.

The chapter has proposed some procedures to obtain energy and power losses from manufacturer's datasheets, and, depending on semiconductor ratings, two approaches have been followed to incorporate losses into semiconductor models.

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Chapter 3

Matlab/Simulink Implementation of a Three-stage Solid State Transformer Model

3.1. Introduction

The implementation of the SST model detailed in Chapter 2 is a very complex and difficult task. The goal of this chapter is twofold: on one hand, it will illustrate the architecture of the SST model implemented in Matlab/Simulink; on the other hand, it will help to better understand the design and operation of the configuration selected for this thesis. The chapter provides a summary of the developed model by showing the main blocks of each SST stage and the approaches followed to incorporate losses into the semiconductor models. Figure 3.1 shows the upper-level Matlab/Simulink implementation of the three-stage SST model. The main characteristics of each stage have already analyzed in previous chapters; a short summary is provided below:

- *MV Input Stage*: A three-phase MMC with associated VOC strategy, level shifted PWM modulation technique and sorting algorithm for SM capacitance balancing has been implemented at input stage of SST.
- *Isolation Stage*: A DC/DC DAB that contains a single-phase MMC, a HFT and a single-phase full bridge rectifier bridge along with associated control strategy.
- *LV Output Stage*: A three-phase four-leg PWM converter with VOC strategy.

For a comparison between the implemented model and the diagram of the full bidirectional three-stage SST, see also Figure 1.1. The implementation of each stage is detailed in the three following sections, while the last section presents the approaches followed for implementing semiconductor losses in each converter. Each section shows the diagram of the power converters plus those of the main controller parts, without going to the last details.

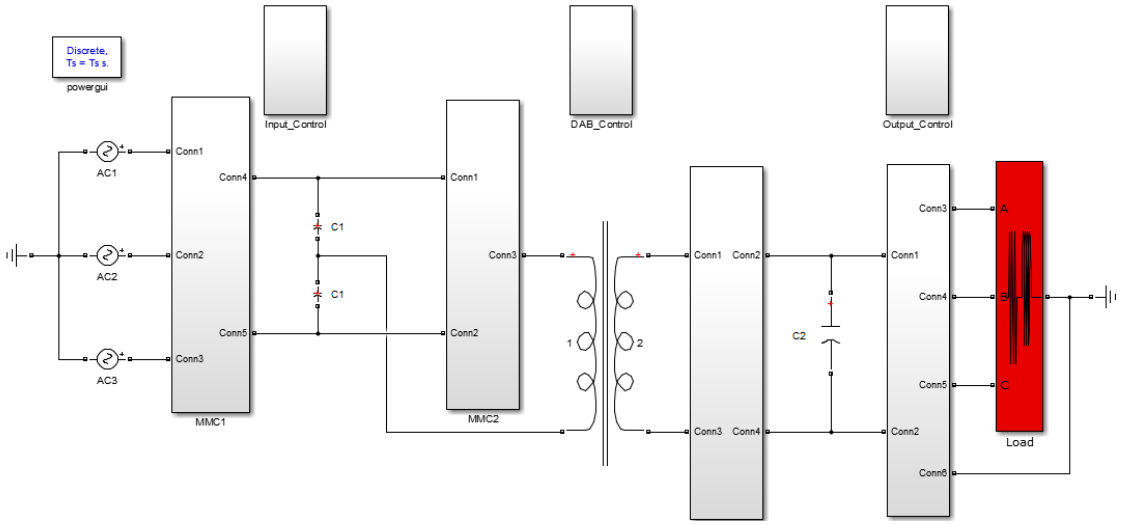


Figure 3.1. Matlab/Simulink implementation of the three stage SST model.

3.2. Implementation of the MV Input Stage

3.2.1. Configuration of the power circuit

The MV input stage three-phase MMC model with six half-bridge converter SMs per arm as implemented in Matlab/Simulink is shown in Figure 3.2. The scheme of each submodule (SM) is depicted in Figure 3.3, respectively.

3.2.2. Control blocks

Figure 3.4 shows different parts of VOC (Vector Oriented Control) strategy in input stage as implemented in Simulink. The positive-sequence grid voltage is used to obtain the grid angle for synchronization purposes by means of a three phase-locked loop (PLL); see Figure 3.4.a. The *d* and *q* axes of VOC are given in Figure 3.4.b and 3.4.c, respectively. As it can be observed from Figure 3.4.b, in *d* axis the real value of MV dc link is compared with reference value and the error is passed through voltage PI controllers which form the reference values for the current in *d* axis. The reference current for *q* axis is set to zero. These current reference values are compared with the actual values of line currents and the errors are passed through PI controllers to obtain reference values for modulation technique in *dq* frame. Finally, Figure 3.4.d shows the output references generated for modulation block in *abc* frame.

Modulation technique: As shown in Figure 3.2, each leg of the three-phase MMC consists of two upper and lower arms with six similar series connected half bridge SM, an arm resistance and an arm inductance. Since all of the arms are similar in terms of control and structure, only the control implementation for an upper arm of phase A is presented in Figure 3.5, which also shows the level-shifted PWM block.

SM control and capacitance voltage balance: Sorting algorithm technique is implemented to balance and keep the voltage of capacitors at the desired value. The capacitance balancing block has three inputs: the number of SMs that should be inserted which is determined through level shifted PWM technique (see Figure 3.5); arm current is measured consistently to determine the charging or discharging states.

The voltage of each capacitor is also measured in order to select the MMC SM that has to be inserted/bypassed (see Figure 3.6).

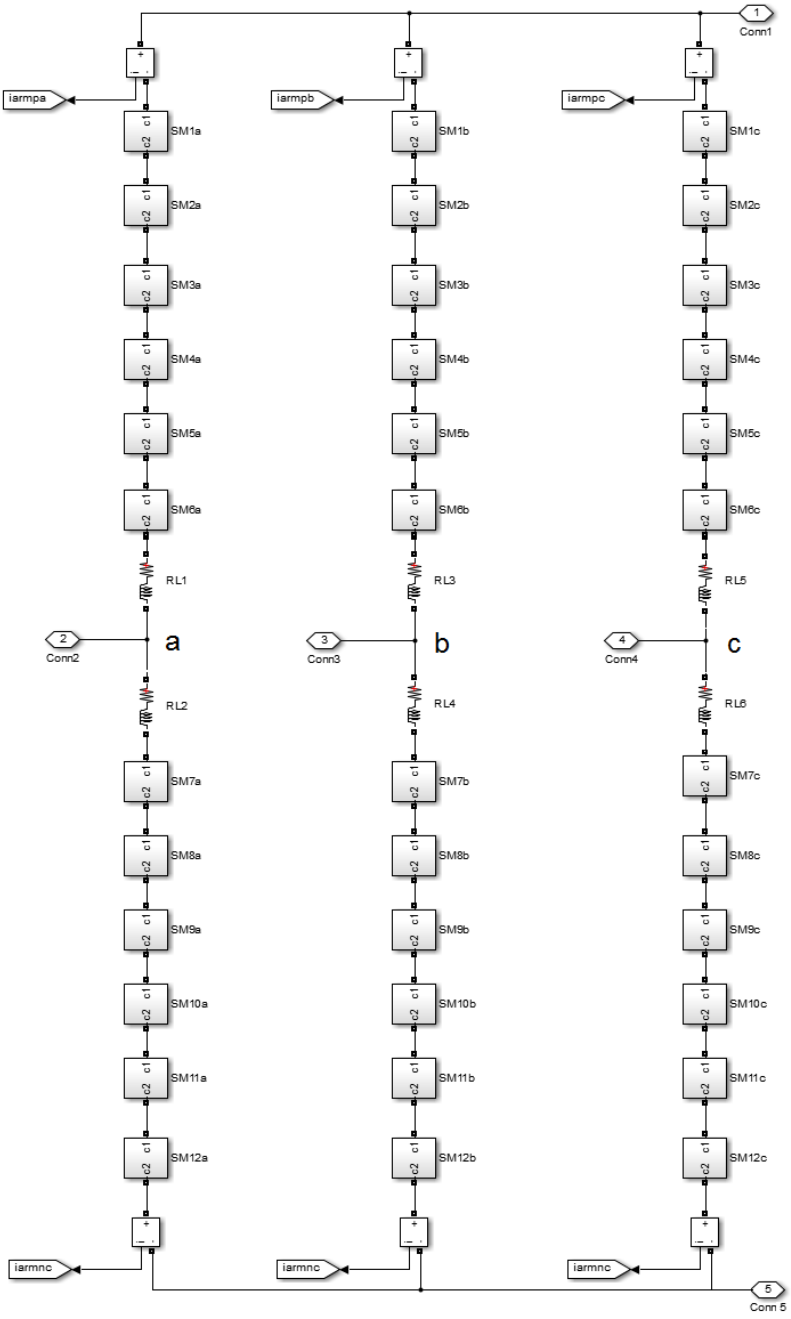


Figure 3.2. Input stage - Three-phase MMC configuration.

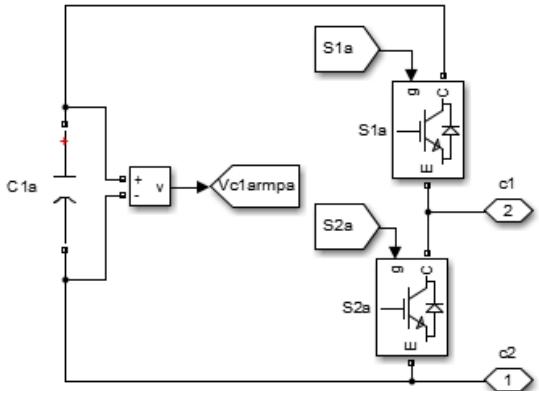
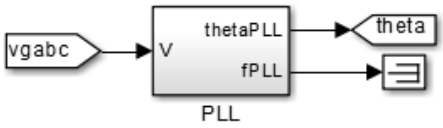
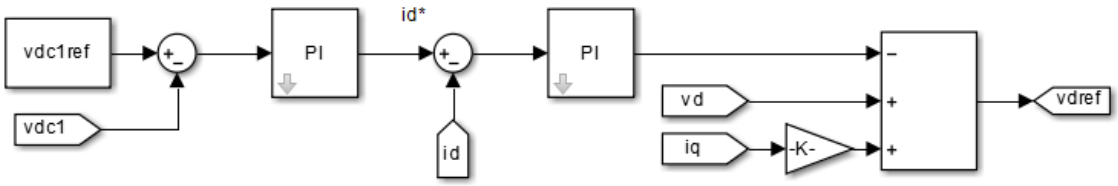


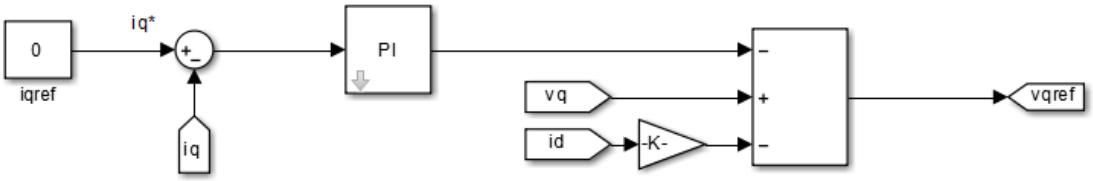
Figure 3.3. Input stage – Configuration of half-bridge submodules (SMs).



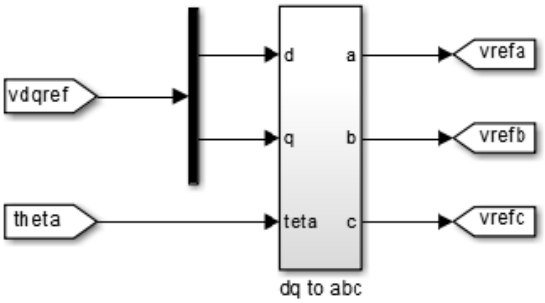
a) Input stage PLL block



b) VOC d-axis



c) VOC q-axis



d) Output of VOC reference signals

Figure 3.4. MV input stage - VOC blocks.

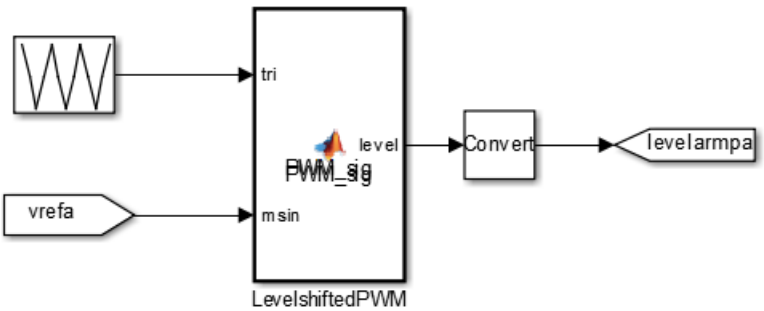
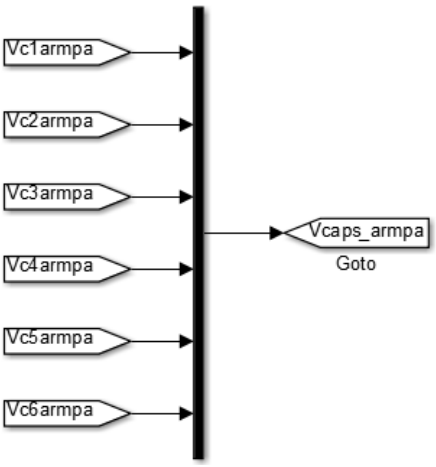
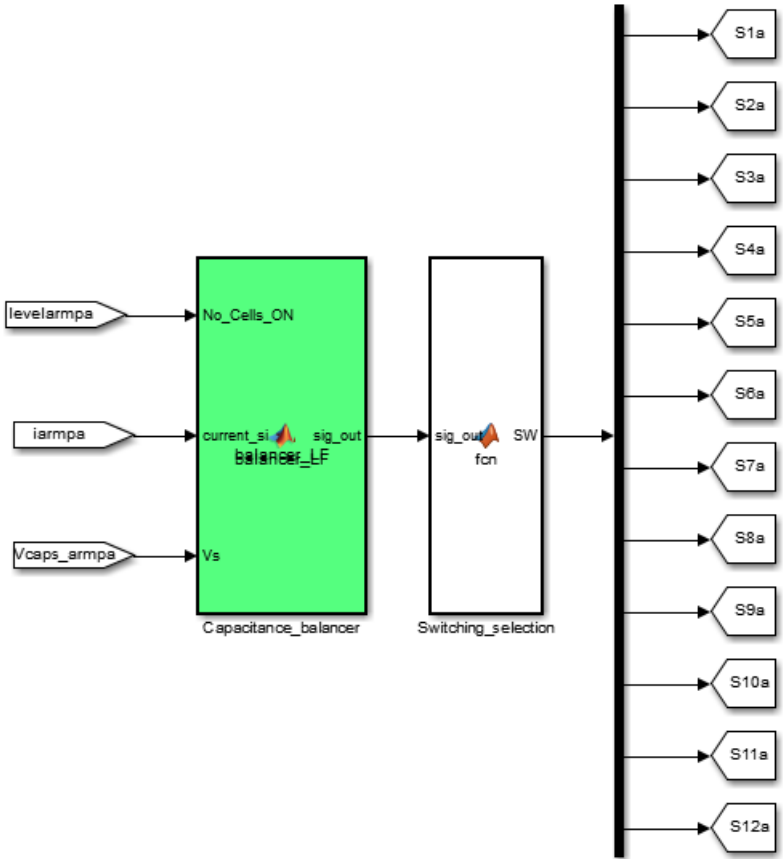


Figure 3.5. Input stage - Block of the level shifted PWM technique for upper arm of phase A.



a) Voltages of SM capacitance



b) Capacitance balancer and switching selection block

Figure 3.6. Input stage - Capacitor balancing and selection strategy.

3.3. Implementation of the MV-LV Isolation Stage

As already mentioned, the SST isolation stage consists of three different parts: single-phase MMC, the HFT, and a single-phase full PWM rectifier bridge.

Figure 3.7 shows the configuration of the single-phase MMC: it is composed of two arms with six half bridge submodules and arm impedance acting as an inverter converting the MV dc link to multilevel high frequency waveform at the primary of high frequency transformer. The control procedure for this single-phase MMC is the

same that was presented in Section 3.2.2. The reference for level shifted modulation strategy is a sinusoidal waveform which its amplitude is based on the value of modulation index.

Figure 3.8 shows the configuration of the single-phase rectifier, its filter and control blocks. As it can be observed from Figure 3.8.c, the real value of LV dc link is compared to its reference value and the error is passed through voltage PI controller. The output of PI controller is multiplied by filtered value of HFT secondary voltage which forms the reference for current. The real value of HFT secondary current is compared with obtained reference value and the error is passed through PR controller which generates the reference value for bipolar PWM technique (see Figure 3.8.a). The bipolar PWM technique generates the switching signals for single-phase two-level full-bridge rectifier.

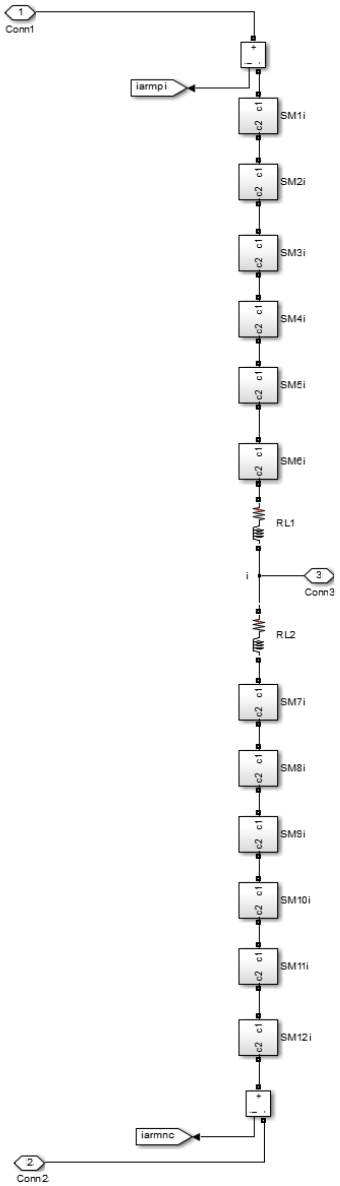
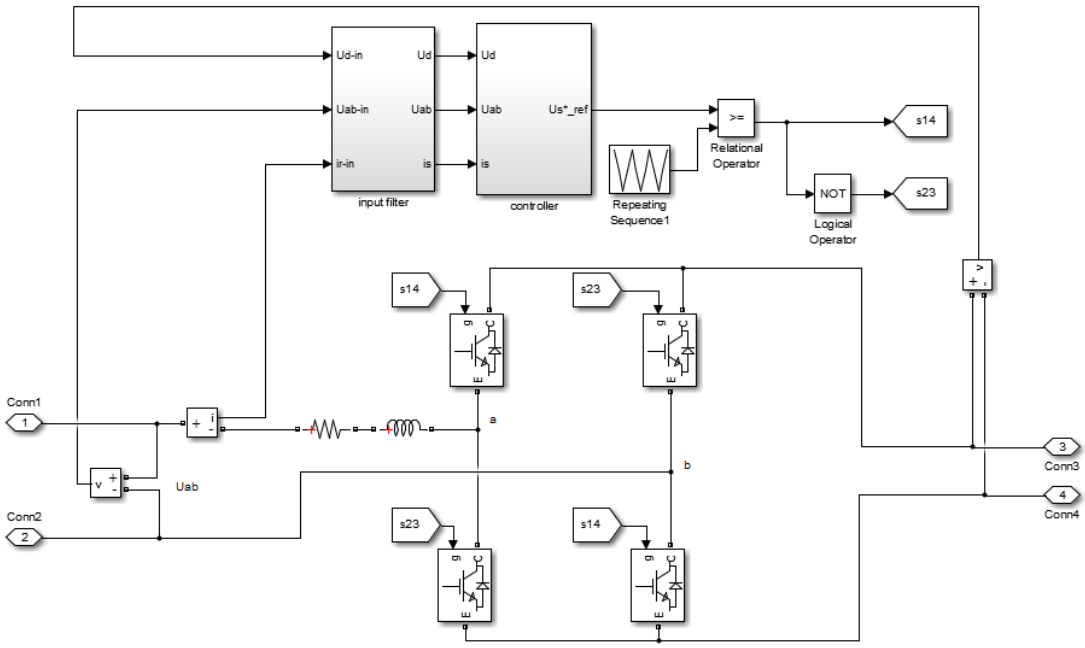
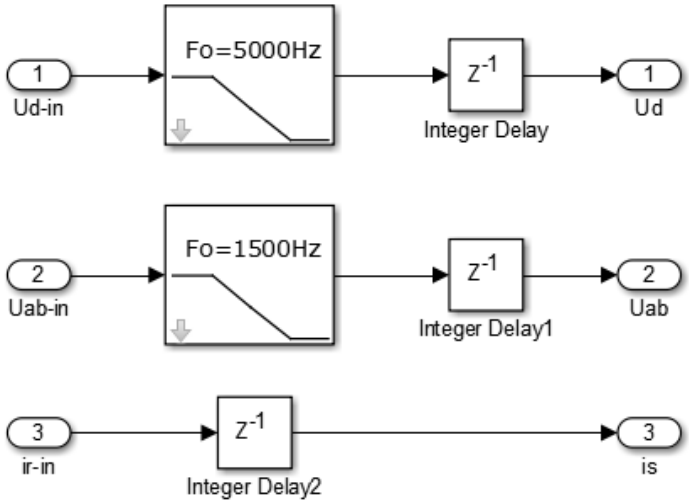


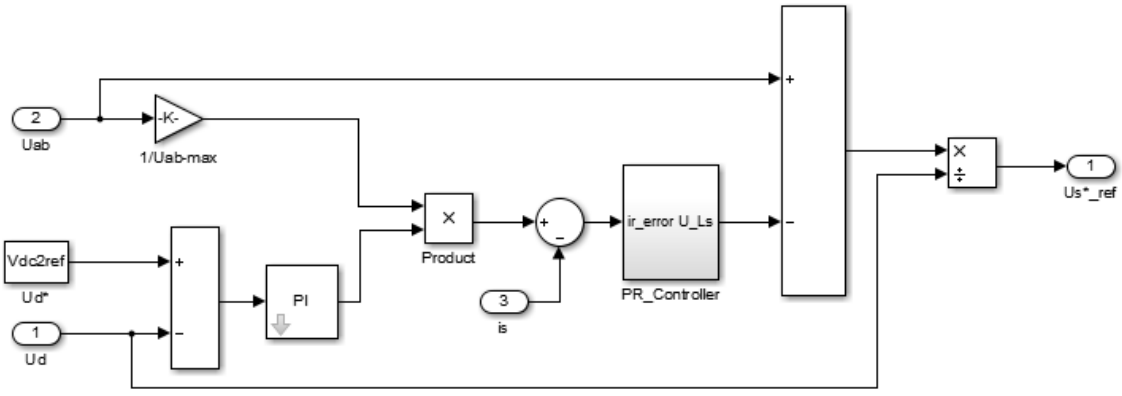
Figure 3.7. Isolation stage – Implementation of the MV single-phase MMC.



a) Isolation stage – Configuration of the LV single phase rectifier



b) Filter block



c) Control block

Figure 3.8. Isolation stage – Implementation of the LV single-phase two-level rectifier.

3.4. Implementation of the LV Output Stage

3.4.1. Configuration of the Output Stage

Figure 3.9 shows the configuration of the LV stage as implemented in this thesis: it consists of a three-phase four-leg converter plus current and voltage filters.

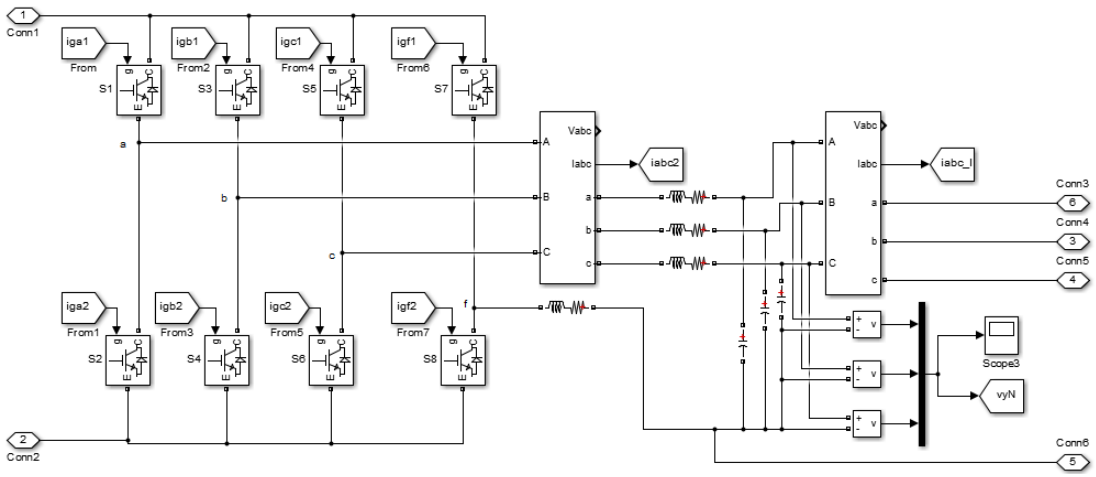


Figure 3.9. Three phase four leg converter topology.

A comprehensive VOC strategy has been implemented in order to guarantee the efficient performance of the converter under different operating conditions (e.g. unbalanced load currents, nonlinear load currents, short circuit). Figure 3.10 provides a full overview of control blocks. The control diagram constitute of voltage control blocks for decomposed positive negative and zero sequences and harmonic voltage compensation blocks for 5th and 7th harmonics. The outer voltage control blocks provide reference for inner current controllers. The inner current control block is also composed of controllers in three positive, negative and zero sequence which provide reference signals for three-dimensional space vector modulation (3D-SVM) technique that is implemented via Matlab function. The output of Matlab function is the duty cycles of switching vectors in one switching period. These duty cycles are then applied to hysteresis modulator to prepare eight switching signals for output stage converter.

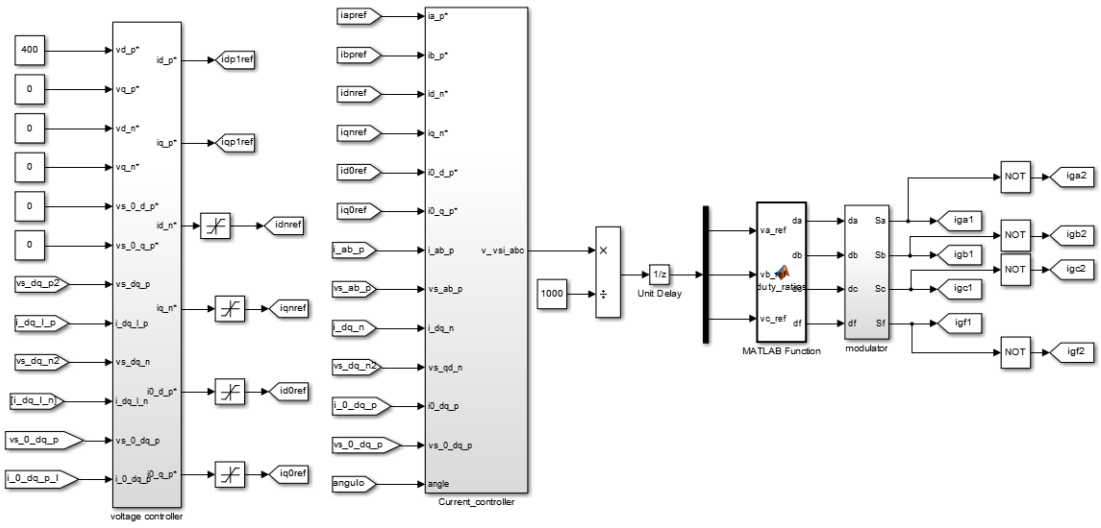
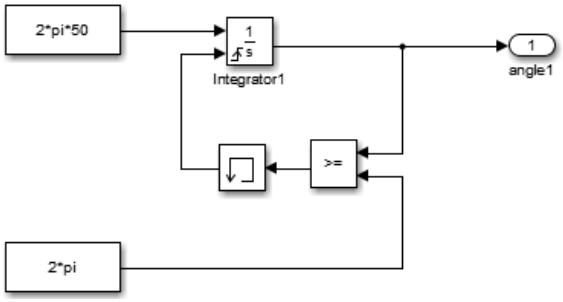
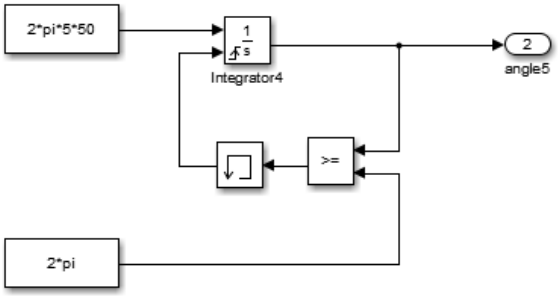


Figure 3.10. Overview of the control diagram for four leg converter.

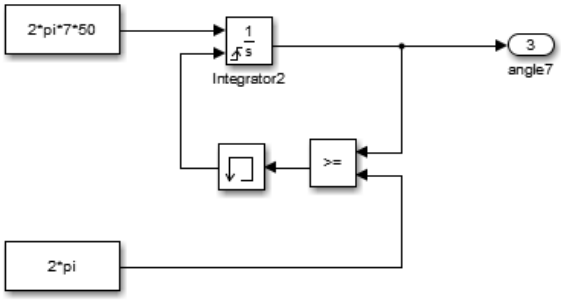
As detailed in Chapter 2, a control strategy for selective harmonic voltage compensation (namely for 1st, 5th and 7th harmonics) has been implemented: the output signal of voltage control block will be added and forms reference signal for current controllers. Figure 3.11 shows PLL for mentioned harmonics.



a) 1st harmonic PLL



b) 5th harmonic PLL



c) 7th harmonic PLL

Figure 3.11. Output stage – PLL blocks for 1st, 5th and 7th harmonics.

The *d* and *q* channels are used to prepare reference signals for modulation technique. In the control strategy implemented for our work, the variables are decomposed to positive, negative and zero sequences with transformation blocks.

Figure 3.12 shows the decomposition block for output currents and voltages. In these blocks, V_{yN} is the three phase load voltage, i_{abc2} and i_{abc_1} are the currents before and after the capacitance filters, respectively.

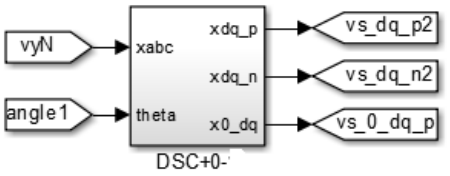
The blocks to transform variables from *abc* to αβ, αβ to *dq*, *dq* to αβ, and αβ to *abc* are based on equations (3.1) through (3.4). In equations (3.2) and (3.3), θ is equal to *angle*1 = +ω*t*, *angle*5 = -5ω*t*, *angle*7 = +7ω*t* for 1st, 5th and 7th harmonics, respectively.

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ v_\gamma \end{bmatrix} = \frac{2}{3} * \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{3.1}$$

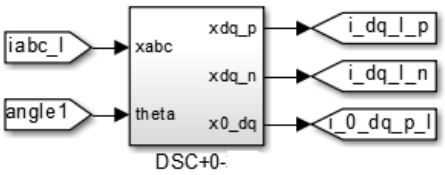
$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} +\cos\theta & +\sin\theta \\ -\sin\theta & +\cos\theta \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{3.2}$$

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} +\cos\theta & -\sin\theta \\ +\sin\theta & +\cos\theta \end{bmatrix} \begin{bmatrix} v_d \\ v_q \end{bmatrix} \tag{3.3}$$

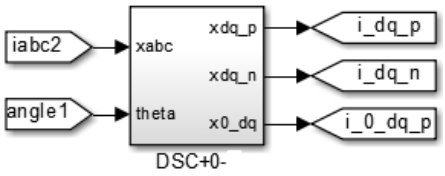
$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \\ v_\gamma \end{bmatrix} \tag{3.4}$$



a) Output voltage decomposition



b) Load current decomposition



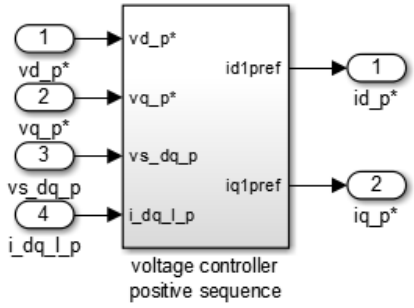
c) Inverter current decomposition

Figure 3.12. Decomposition blocks for four leg inverter.

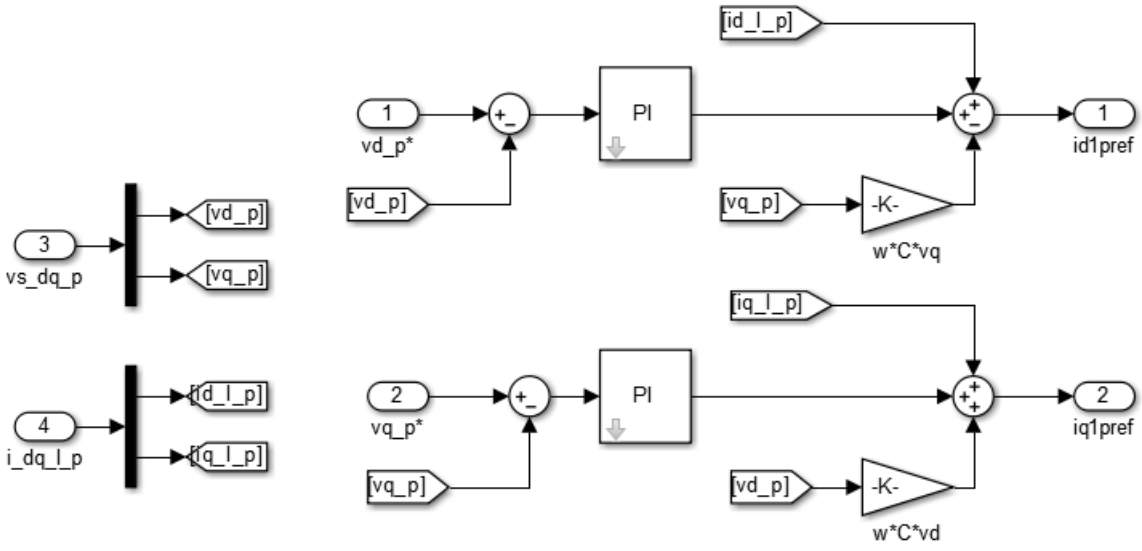
3.4.2. Voltage control blocks

Output voltage controllers prepare the reference signals of current for inner current control blocks. Figure 3.13 through Figure 3.15 show the respectively positive, negative and zero sequences of voltage control blocks for fundamental frequency.

Voltage controller for positive sequence: The masked and detailed view of voltage controllers for positive sequence channel at fundamental frequuency are given in Figure 3.13. as it can be seen from figure 3.13.b, the real values of capacitance voltages in positive sequence which are achieved after decomposition in *abc* frame are transformed to *dq* frame through using equations 3.1 to 3.4. These real values are then compared with reference value of positive voltage sequence in d and q channels and the errors are pased through voltage PI controllers to determine the reference for outer current controllers in positive chanel. The PI coeficients are tuned properly in a way that real values of load voltage could track the dc reference values in *dq* frame and therefore providing three phase sinosuidal voltage in *abc* fram as well. It should be noted that the capacitance value also has impact in determining the reference values for inner current controllers.



a) Masked block



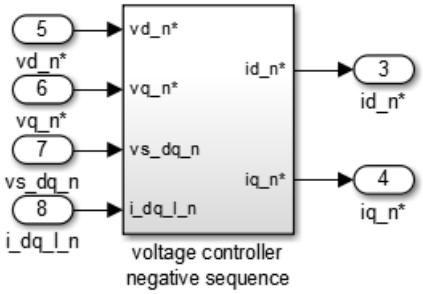
b) Control diagram

Figure 3.13. Diagram of the positive-sequence voltage controller for fundamental frequency.

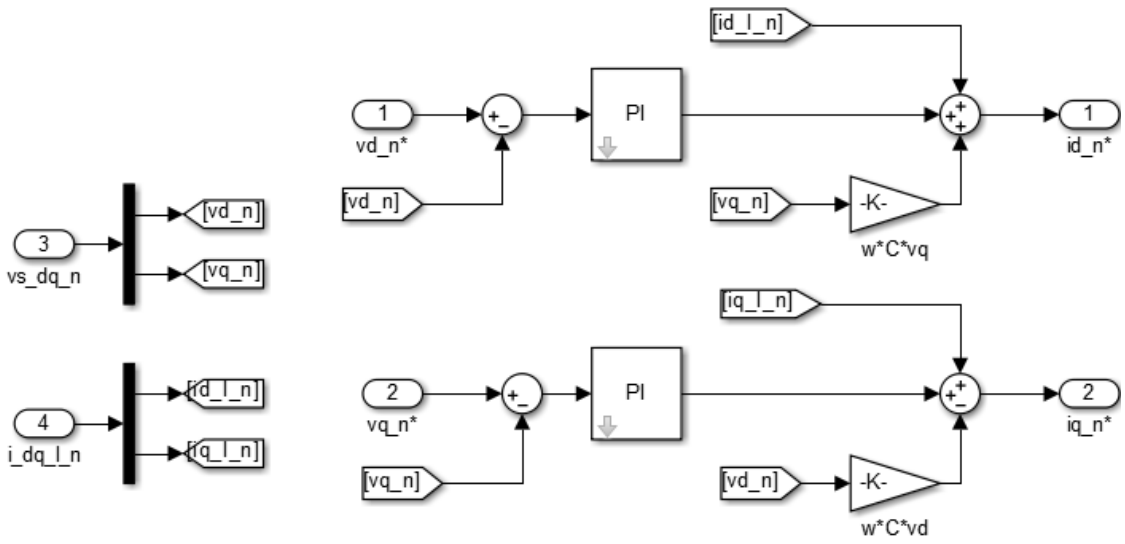
Voltage controller for negative sequence: The masked and detailed view of voltage controllers for negative sequence channel are given in Figure 3.14. As it can be seen from figure 3.14.b, the real values of capacitance voltages in negative sequence which are generated due to unbalanced load condititions and are achieved after decomposition in *abc* frame are transformed to *dq* frame through using equations 3.1 to 3.4. these valuse are compared with reference value of negative voltage sequence (which are set to zero in order to cancel negative components of voltage) in *d* and *q* channels and the errors are pased through voltage PI controllers to determine the reference for outer current controllers in negative chanel. The PI coeficients are tuned properly in a way

that real values of load voltage in negative sequence are reaching the value close to zero in *dq* frame and therefore providing three phase sinosuidal voltage in abc fram as well.

Voltage controller for zero sequence: the masked and detailed view of voltage controllers for zero sequence channel are given in Figure 3.15. as it can be seen from figure 3.15.b, the real values of capacitance voltages in zero sequence which are generated due to unbalanced load condititions and are achieved after decomposition in *abc* frame are transformed to *dq* frame through using equations 3.1 to 3.4. these valuse are compared with reference value of zero voltage sequence (which are set to zero in order to cancel zero component of voltage) in *d* and *q* channels and the errors are pased through voltage PI controllers to determine the reference for outer current controllers in zero chanel. The PI coeficients are tuned properly in a way that real values of load voltage in zero sequence are reaching the value close to zero in *dq* frame and therefore providing three phase sinosuidal voltage in abc fram as well.



a) Masked block



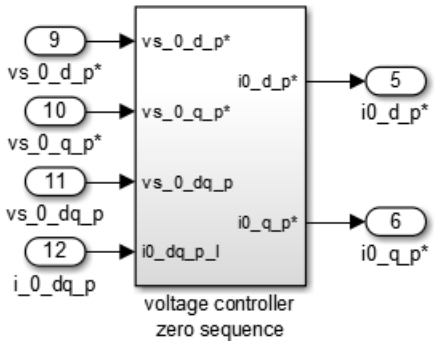
b) Control diagram

Figure 3.14. Diagram of the negative-sequence voltage controller for fundamental frequency.

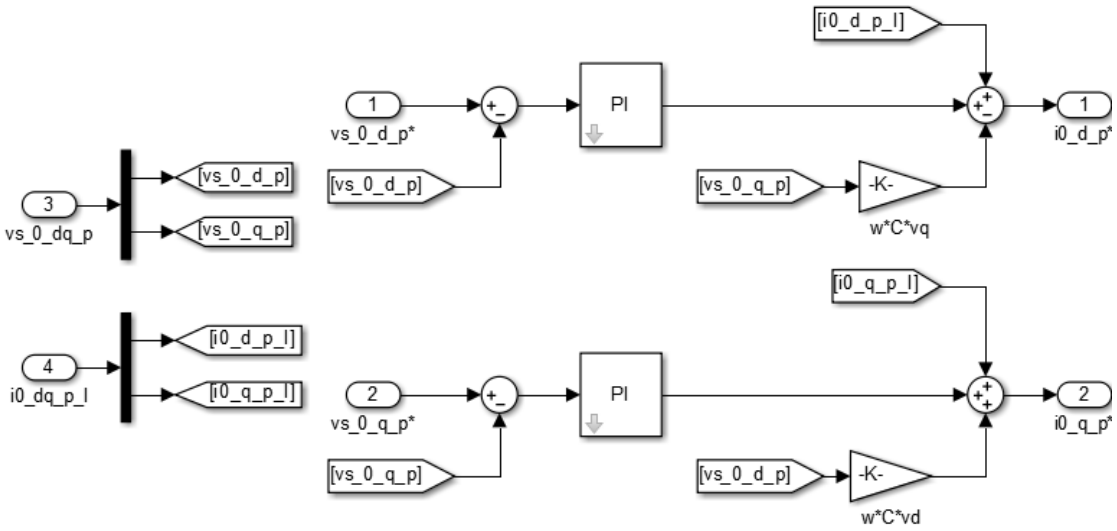
Control diagram for 5th harmonic: The masked block and detailed view of the control block for 5th harmonic voltage compensation are given in Figure 3.16. In order to compensate 5th harmonics of voltage, first it is required to extract the 5th harmonic component and then create voltage controllers in parallel with positive sequence control block at fundamental frequency. As it can be observed from Figure 3.16.b, the reference value of load voltage in αβ frame which is pure sinusoidal waveform with fundamental

frequency is compared with real value of load voltage which contains all harmonic components including fundamental component and harmonic components with the frequency of $(6n\pm1)\omega$. With this comparison the harmonics will be extracted. The main aim is to cancel most noticeable harmonic components which are 5th and 7th harmonics. The extracted harmonics in αβ frame will be transformed to *dq* component with transformation angle of -5θ which gives the 5th harmonic component of load voltage. These values are passed through PI controllers in order to compensate 5th harmonics of voltage and also providing reference values for output current controllers.

Control diagram for 7th harmonic: The masked and detailed views of the control block for 7th harmonic voltage compensation are given in Figure 3.17. In order to compensate 7th harmonics of voltage, first it is required to extract the 7th harmonic component and then create voltage controllers in parallel with positive sequence control block at fundamental frequency. As it can be observed from Figure 3.17.b, the reference value of load voltage in αβ frame which is pure sinusoidal waveform with fundamental frequency is compared with real value of load voltage which contains all harmonic components including fundamental component and harmonic components with the frequency of $(6n\pm1)\omega$. With this comparison the harmonics will be extracted. To compensate the 7th harmonics, the extracted harmonics in αβ plane will be transformed to *dq* component with transformation angle of +7θ the 7th harmonic component of load voltage will be obtained. These values are passed through PI controllers in order to compensate 7th harmonics of voltage and also providing reference values for output current controllers.

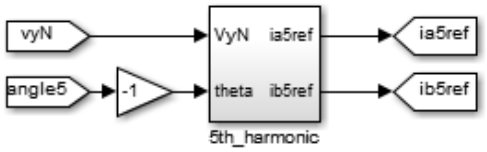


a) Masked block

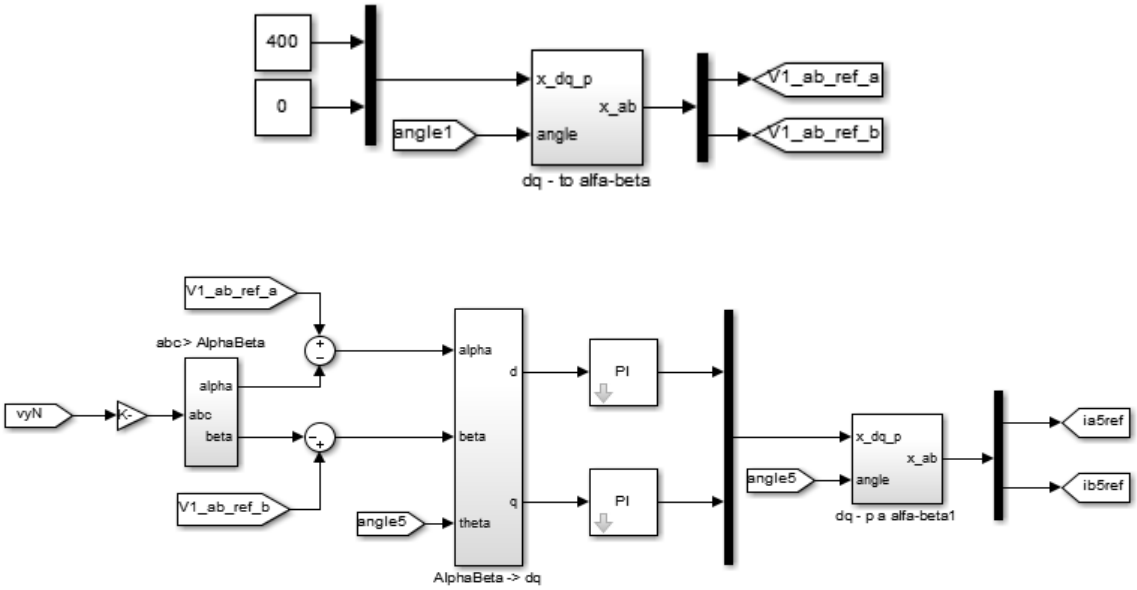


b) Control diagram

Figure 3.15. Diagram of the zero-sequence voltage controller for fundamental frequency.

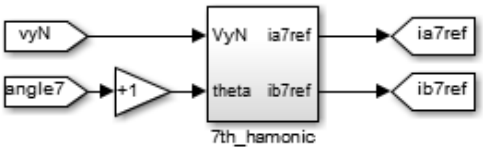


a) Masked block

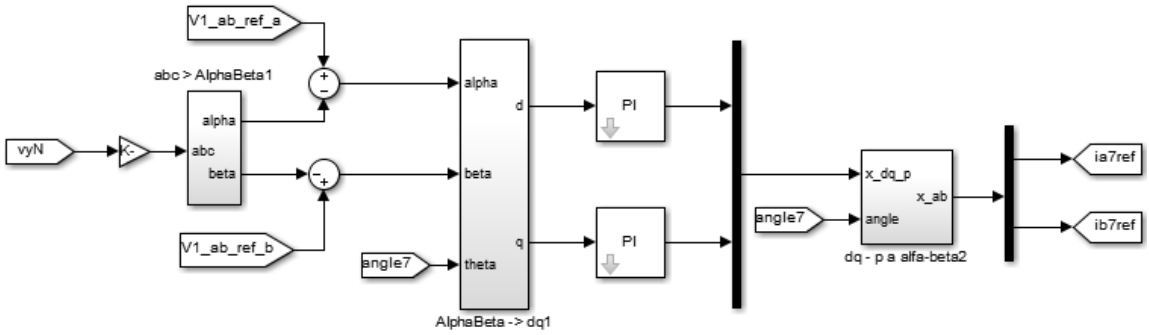


b) Control block

Figure 3.16. Diagram of the voltage control compensation of 5th harmonic.



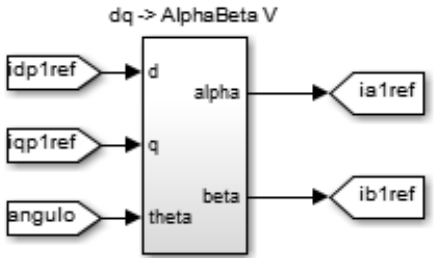
a) Masked block



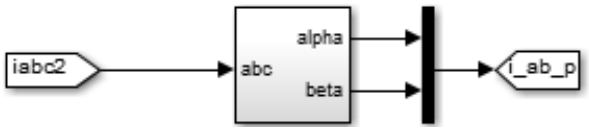
b) Control block

Figure 3.17. Diagram of the voltage control compensation of 7th harmonic.

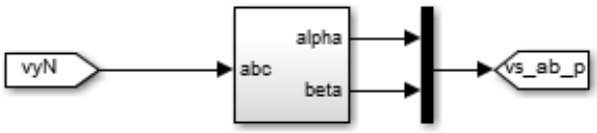
Reference signals for output current controllers: In comprehensive VOC strategy with the capability of harmonic compensation, the reference signal for positive sequence of current controller is achieved through adding reference current from positive sequence voltage controllers of fundamental frequency with output signals from 5th and 7th harmonic compensation control blocks (see Figure 3.18.d). Figure 3.18 shows the references that are needed for current control in positive sequence in αβ space.



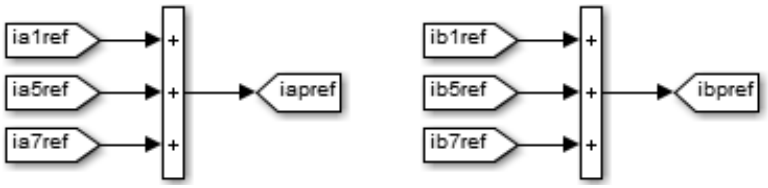
a) Current reference at the fundamental frequency in αβ frame for positive sequence



b) Inverter current in αβ frame for positive sequence



c) Load reference voltage in αβ frame for positive sequence



d) Current reference in αβ frame for positive sequence

Figure 3.18. Reference signal in αβ frame for positive sequence current control block.

3.4.3. Current controllers block

Figure 3.19 shows the masked view of inner current control blocks. The current control block provide the reference signals for 3D-SVM modulation technique. Figures 3.20 to figure 3.22 show the positive, negative and zero sequences of current control blocks.

The refence values for positive sequence current controllers in αβ frame are achievd from the voltage controllers as described in above section. the current refrence for positive sequence will be achieved by adding reference current at the fundamental frequency and reference currents related to 5th and 7th harmonics. For negative sequence and zero sequence, the current reference values will be achieved from voltage controllers in *dq* channel.

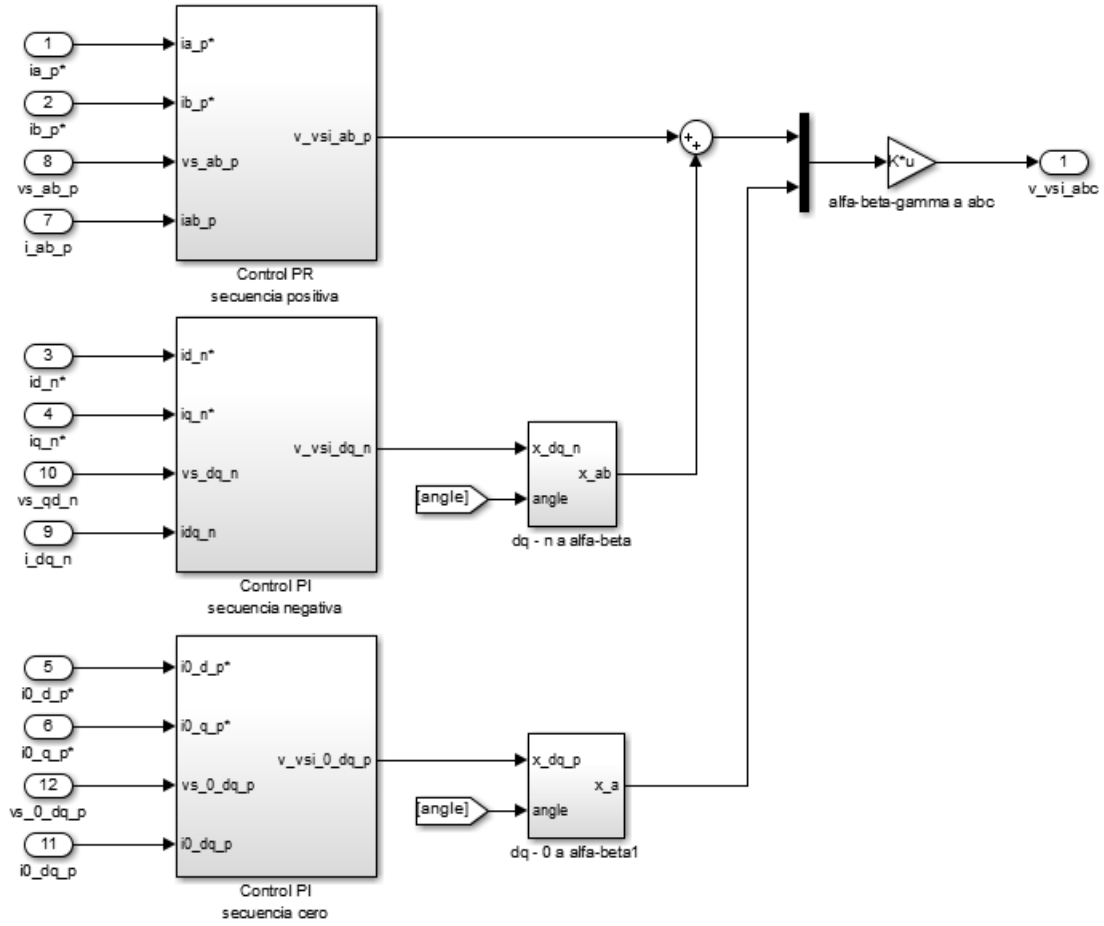


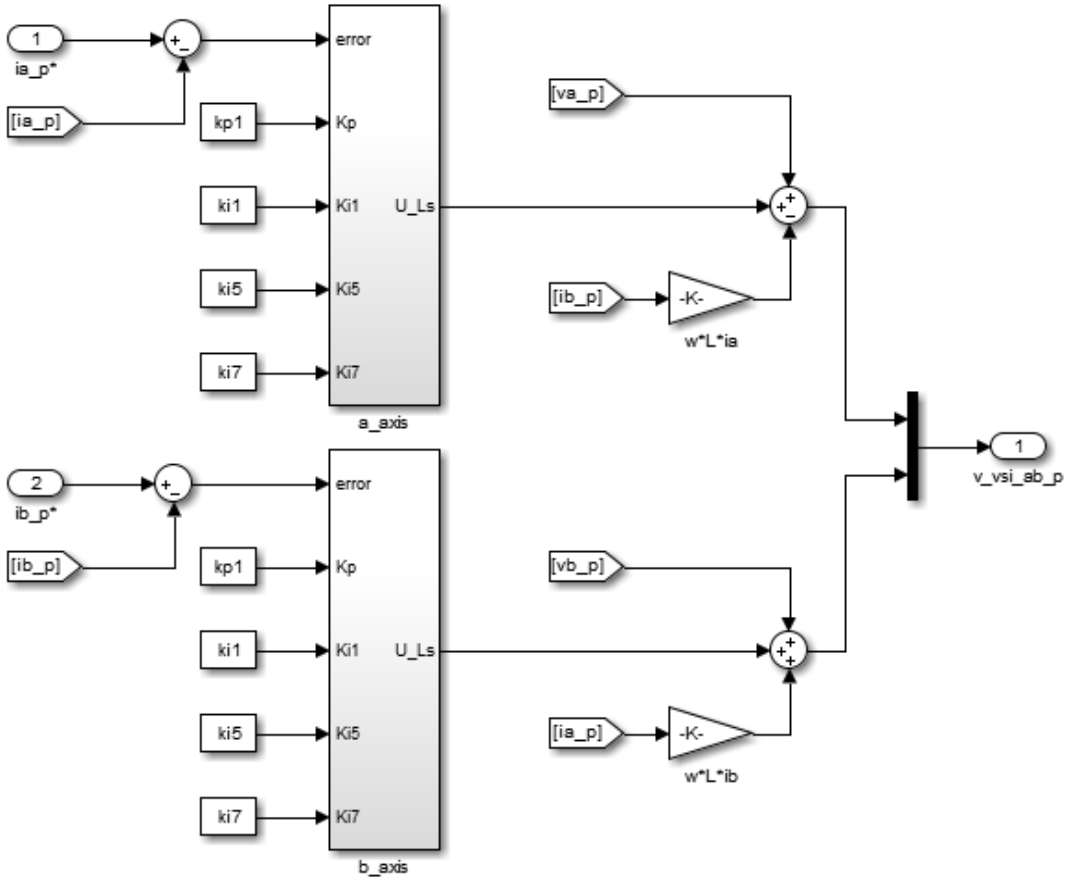
Figure 3.19. Overall view of current control blocks.

Current controller for positive sequence: The masked and detailed views of the current control block for positive sequence are given in Figure 3.20. The reference value of current are compared with their real values in αβ frame and the error is passed through PR controllers related to fundamental, 5th and 7th harmonics frequencies that generates the reference value for modulation strategy. The PR controllers in αβ frame provide efficient control when nonlinear load is connected.

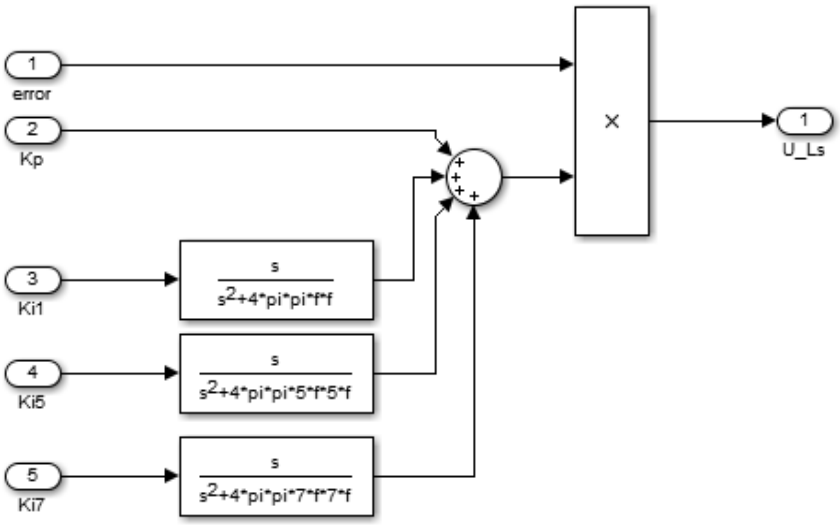
Current controller for negative sequence: Figure 3.21 shows the current control block for negative sequence. The current reference value for negative sequence in *dq* channel which is achieved through the voltage controllers in negative sequence is compared with real values of inverter current in *dq* channel and the error is passed though PI controllers which generates the reference value for Modulation strategy.

Current controller for zero sequence: Figure 3.22 shows the current control block for zero sequence. The current reference value for zero sequence in *dq* channel which is achieved through the voltage controllers in zero sequence is compared with real values of inverter current in *dq* channel and the error is passed though PI controllers which generates the reference value for Modulation strategy.

Finally, all the output signals of current controllers in positive and negative and zero sequence are added together in αβ frame and then transformed to *abc* signal to be used for three-dimensional space vector modulation strategy (3-D SVM) in *abc* frame.



a) Masked control blocks



b) PR controllers

Figure 3.20. Positive sequence current controller diagram.

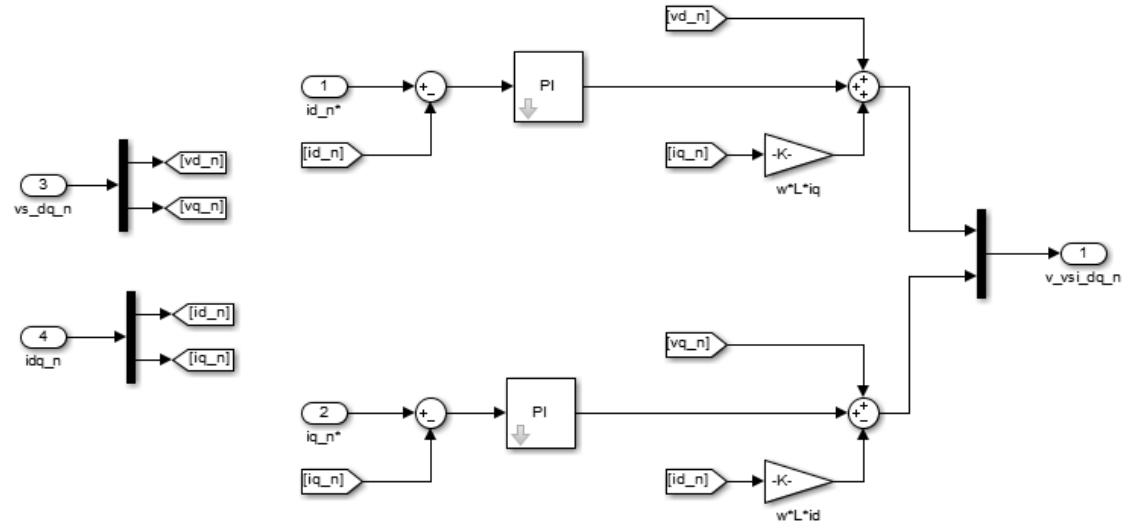


Figure 3.21. Negative sequence current controller diagram.

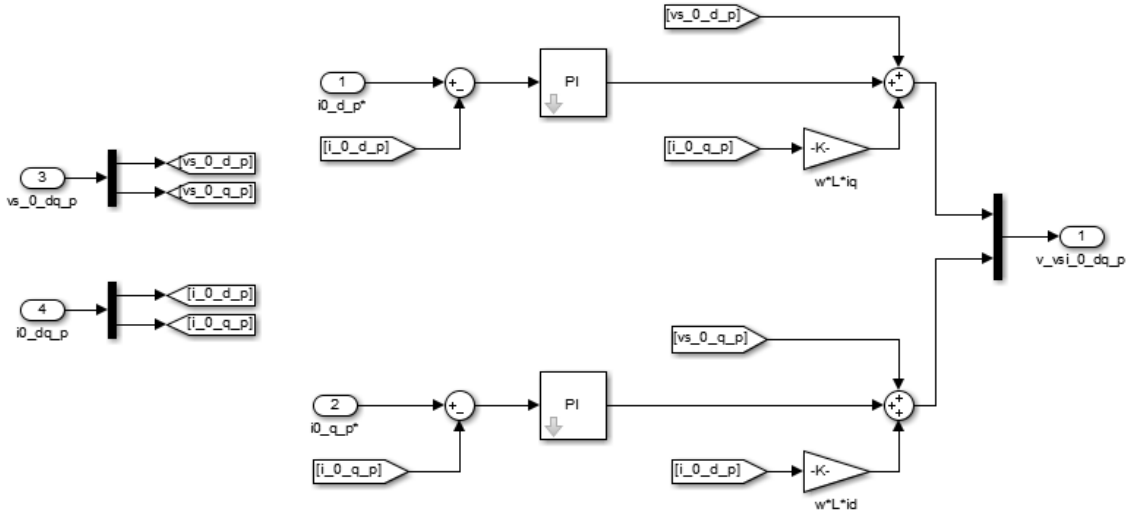


Figure 3.22. Zero sequence current controller diagram.

3.4.4. Modulation block

As it can be seen from figure 3.23, the output control signal will be applied to 3D-SVM modulation block in order to generate gate signals for four leg converter. The 3-D SVM function determines the duty cycles related to NZSV and ZSV. As it is discussed in Section 2.4.4, there are sixteen switching vectors for 3-D SVM which divide the control region to 24 tetrahedrons.

In each tetrahedron, there are three NZVS and one ZVS that their duty cycle is determined by switching look up table which is given in the form of Matlab code in Matlab function. These duty cycles are applied to the modulator which generate eight switching signals for four-leg converter. It should be noted that the modulator use hysteresis relays with upper and lower bands for generation of switching signals (see Figure 3.24).

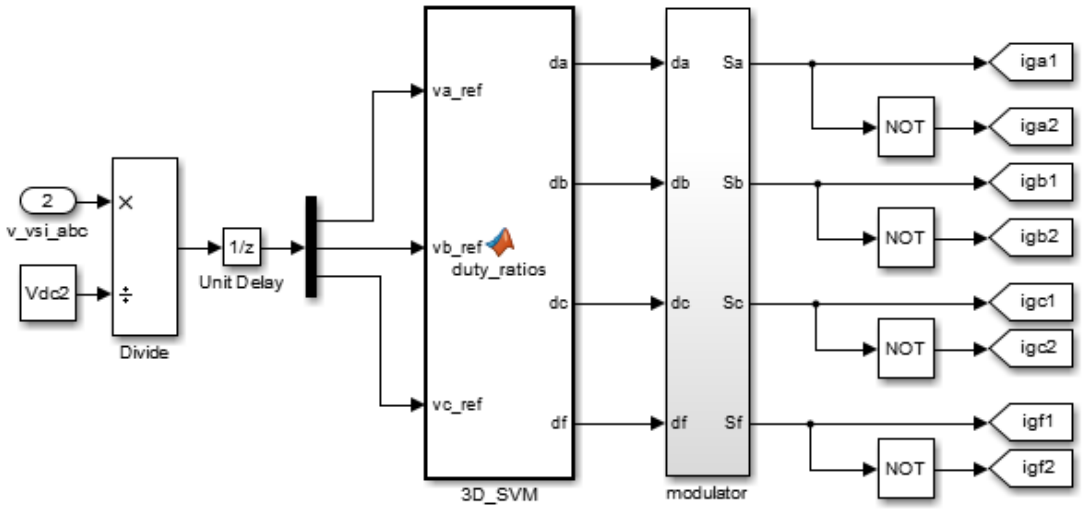


Figure 3.23. 3D-SVMmodulation block.

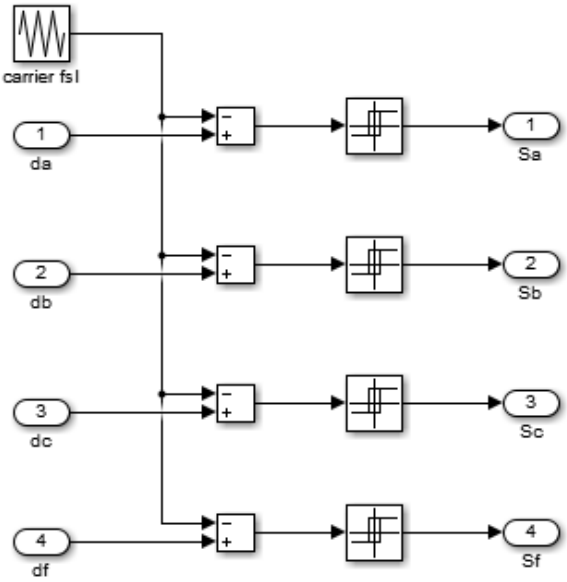


Figure 3.24. 3D-SVM modulator diagram.

3.5. Implementation of Semiconductor Losses

3.5.1. Introduction

There are three types of power losses in IGBTs and diodes: conduction, switching and blocking losses. In general, blocking losses are neglected; therefore, total semiconductor losses consist of conduction and switching losses. This section provides a summary of the approaches followed for implementing losses in Matlab/Simulink semiconductor models for IGBTs and diodes. Since the approaches implemented in this thesis account for semiconductor losses, thermal semiconductor and converters have also been implemented as part of the procedure for calculating and incorporating losses into semiconductor models.

3.5.2. Semiconductor loss calculation

Conduction loss of IGBTs and diodes: Figure 3.25 shows the calculation procedure of conduction losses for IGBT and diode ($P_{conS/D}$). The value of $v_{conS/D}$, the forward

semiconductor voltage in conduction mode, is obtained by means of a 2-D lookup table (available in manufacturer's datasheet) from two inputs: $i_{S/D}$, the current through the semiconductor, and $T_{jS/D}$, the semiconductor junction temperature derived from its thermal model.

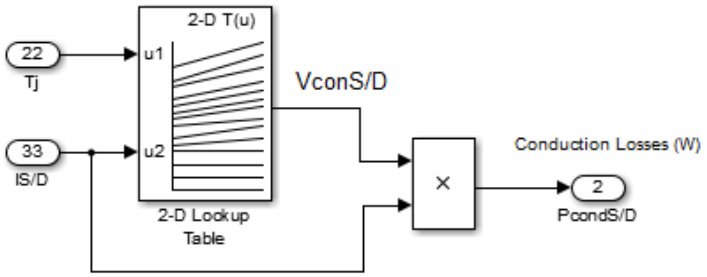


Figure 3.25. Calculation of conduction losses for IGBTs and Diodes.

Switching losses of IGBTs: Figure 3.26 shows the procedure to obtain total IGBT switching losses, ΔP_{sw}, using manufacturer datasheet (see Chapter 2). As it can be seen from this figure, ΔP_{onsw} and ΔP_{offsw} are calculated from the values of E_{onsw} and E_{offsw}. Both energy values are obtained from 3D lookup tables supplied in manufacturers' datasheets. As shown in Figure 3.26:

- Three inputs are required for the calculation of E_{onsw}: the pre-switching value of v_{CE}, the post-switching value of the i_S, and T_{jS}.
- Three inputs are required for the calculation of E_{offsw}: the post-switching value of v_{CE}, the pre-switching value of i_S, and T_{jS}.

ΔP_{onsw} and ΔP_{offsw} are obtained after dividing E_{onsw} and E_{offsw} by the simulation time step.

For the meaning of all these symbols, see Chapter 2.

Switching losses of diodes: Figure 3.27 shows the calculation of ΔP_{recD}. E_{recD} is obtained by means of a 3-D lookup table (also available from manufacturer's datasheet) from three inputs: the pre-switching value of the diode current, i_D, the post-switching value of the diode voltage, v_D, and the junction temperature in the diode, T_{jD}. The value of ΔP_{recD} is obtained after dividing E_{recD} by the simulation time step.

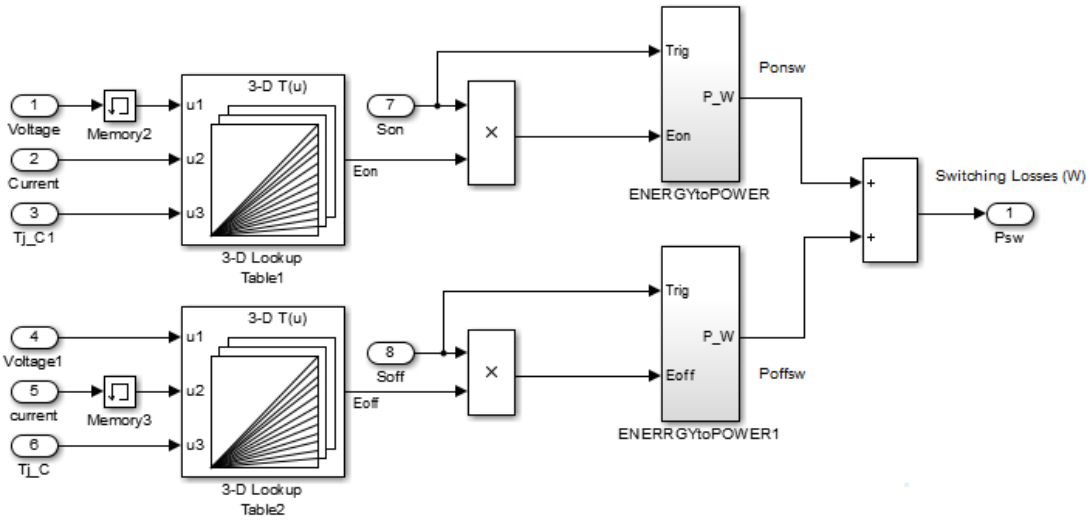


Figure 3.26. Calculation of IGBT switching losses.

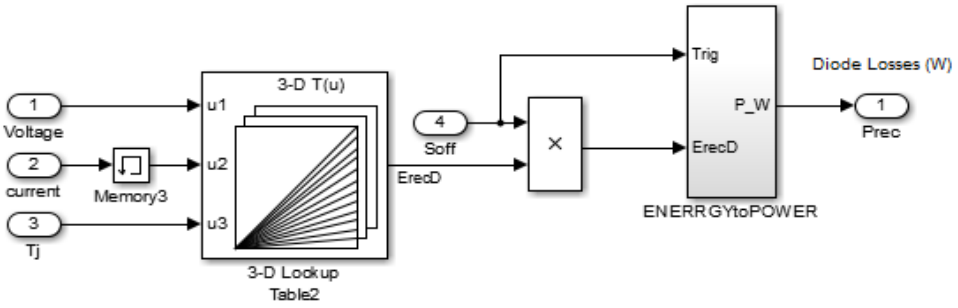


Figure 3.27. Calculation of diode switching losses.

3.5.3. Thermal models

Since semiconductor junction temperatures have some impact on semiconductor losses, the implementation of thermal models is necessary to estimate junction temperature as look up table input (see Figures 3.25 to 3.27). This implementation of thermal models in Matlab/Simulink is detailed for one leg a of the LV three-phase four-leg converter. A similar approach has been followed for the LV full bridge rectifier of the isolation stage. The thermal model developed in this work is according to that presented in [3.1]-[3.2]. As described in Chapter 2 (see Section 2.5.4), the thermal model of a semiconductor can be represented by means of a *RC* circuit, see Figure 2.20, in which R_{th} and C_{th} are respectively the thermal resistance and capacitance between semiconductor junction and semiconductor case, R_c and C_c are the thermal resistance and capacitance between semiconductor case and heat sink, and R_s and C_s are the thermal resistance and capacitance between heat sink and ambient.

Figure 3.28 shows the masked implementation block of thermal model for 16 semiconductors (8 IGBTs and 8 antiparallel diodes) which share a common heat sink for output stage converter.

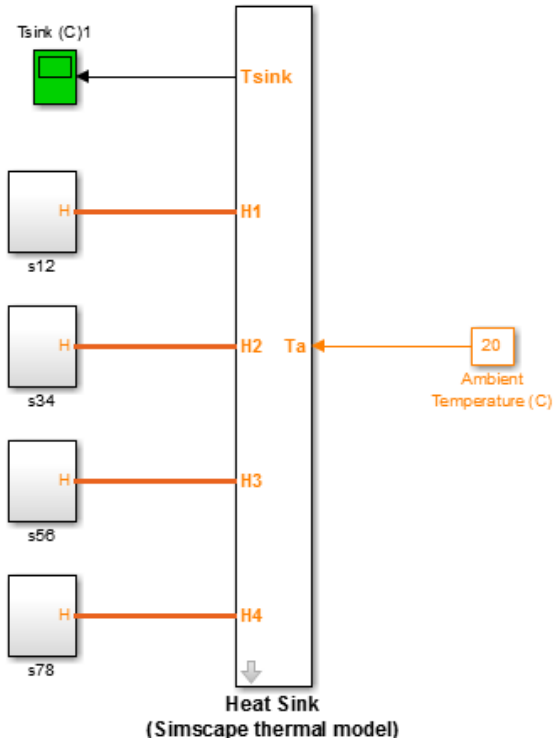


Figure 3.28. Thermal model for the LV otput stage converter.

Semiconductor case provides an interface between the semiconductor junction and heat sink. In the thermal model the total loss of each semiconductor ($\Delta P_{totS/D}$) and semiconductor case temperature serve as input for estimating the semiconductor junction temperature. These inputs are considered as state variables and thermal resistances and capacitances are the coefficients in state space equations. Since all the legs are the same in terms of thermal modeling, only the detailed implementation of leg a in output stage converter are given in this section.

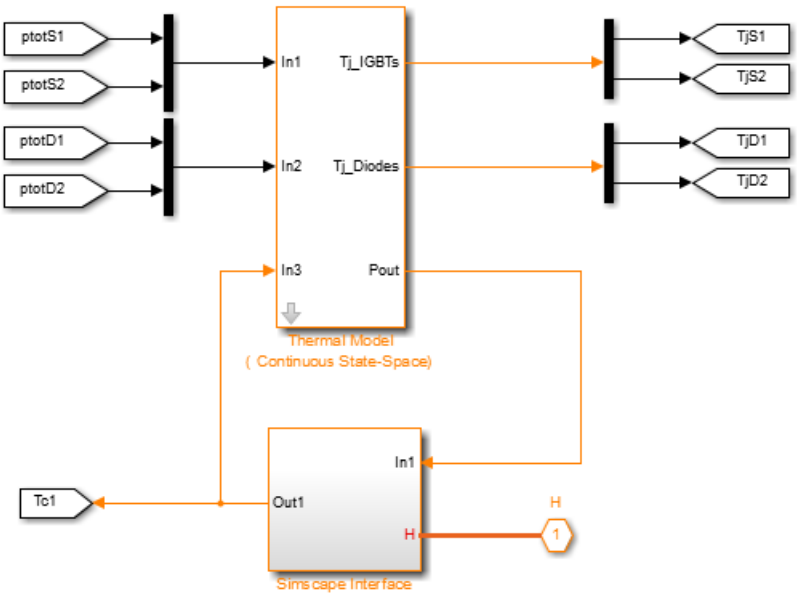
Figure 3.29 shows the state-space junction to case thermal model for one leg of the LV output stage converter. As it can be observed, the total loss of each semiconductor and semiconductor case temperature are used as inputs of the state-space thermal model. The estimated output is the semiconductor junction temperature, which is required for loss calculation, and the loss itself, which is injected to semiconductor case model. Figure 3.29.b shows the parameters of the semiconductor thermal impedance, required for estimation of semiconductor junction temperature; Figure 3.29.c shows a detailed view of the model including state-space equations; Figure 3.29.d shows a detailed view of the semiconductor case model.

Figure 3.30 shows the masked model of heat sink and detailed view of heat sink block in Matlab/Simulink. The parameters considered in the heat sink model are the thermal resistance and capacitance from semiconductor case to heat sink and semiconductor heat sink to ambient.

3.5.4. Incorporation of losses into semiconductor models

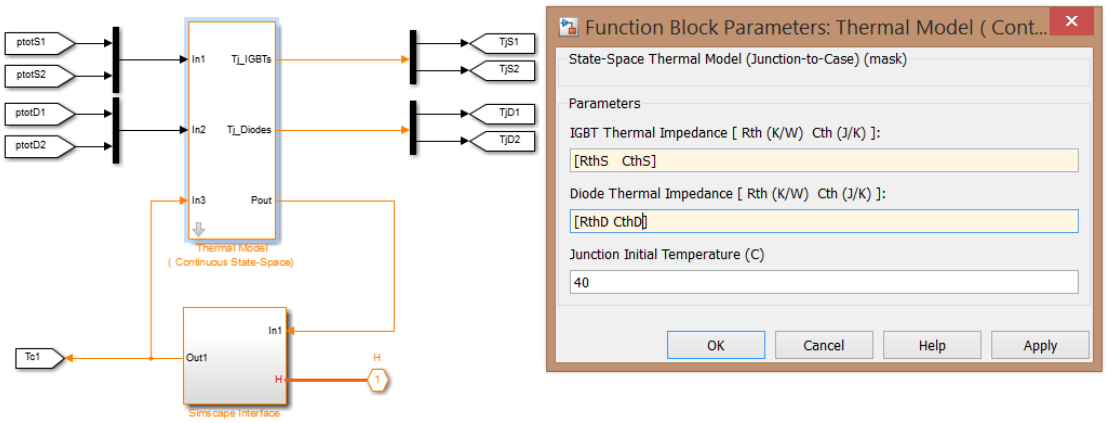
The main aim of this section is to replace ideal semiconductor models available in Matlab/Simulink with semiconductor models that incorporate losses and take into account the joint temperature effect.

Conduction losses: Conduction losses, $\Delta P_{conS/D}$, can be incorporated into the semiconductor models by means of a controlled voltage source (with a value equal to $v_{conS/D}$) in series with the ideal semiconductor, either an IGBT or a diode; see Figures 3.32 and 3.34.

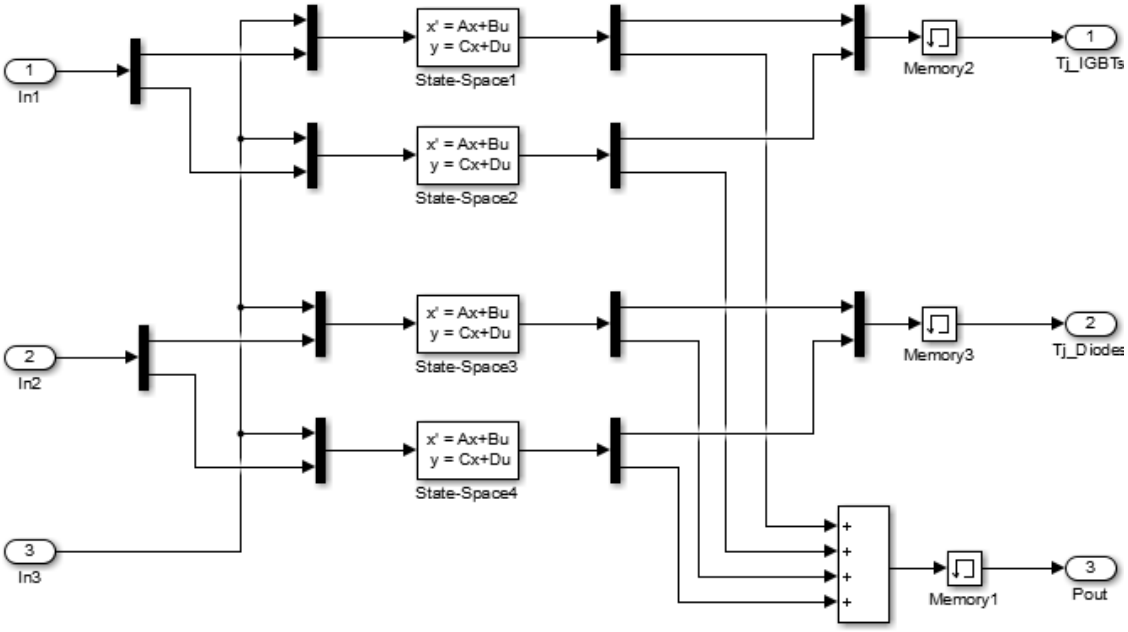


a) Masked junction-to-case thermal model

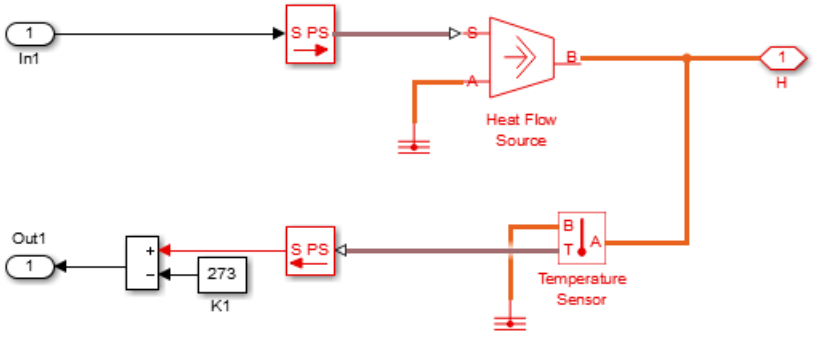
Figure 3.29. Thermal model for one leg of the LV output stage converter.



b) Junction-to-case thermal model

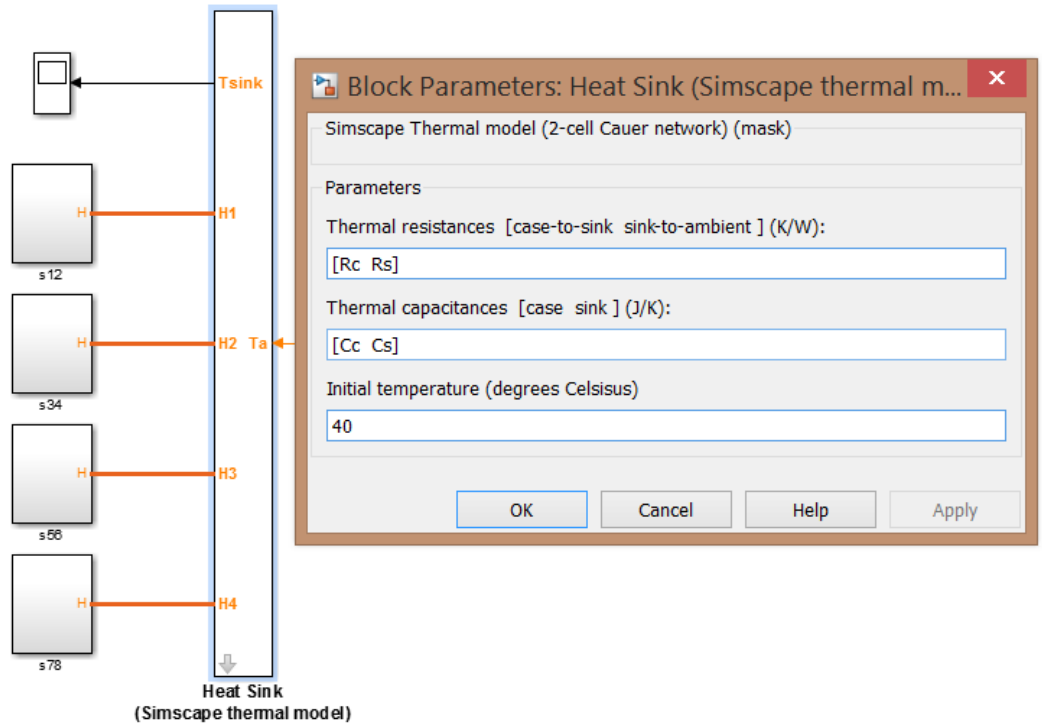


c) Junction-to-case thermal model

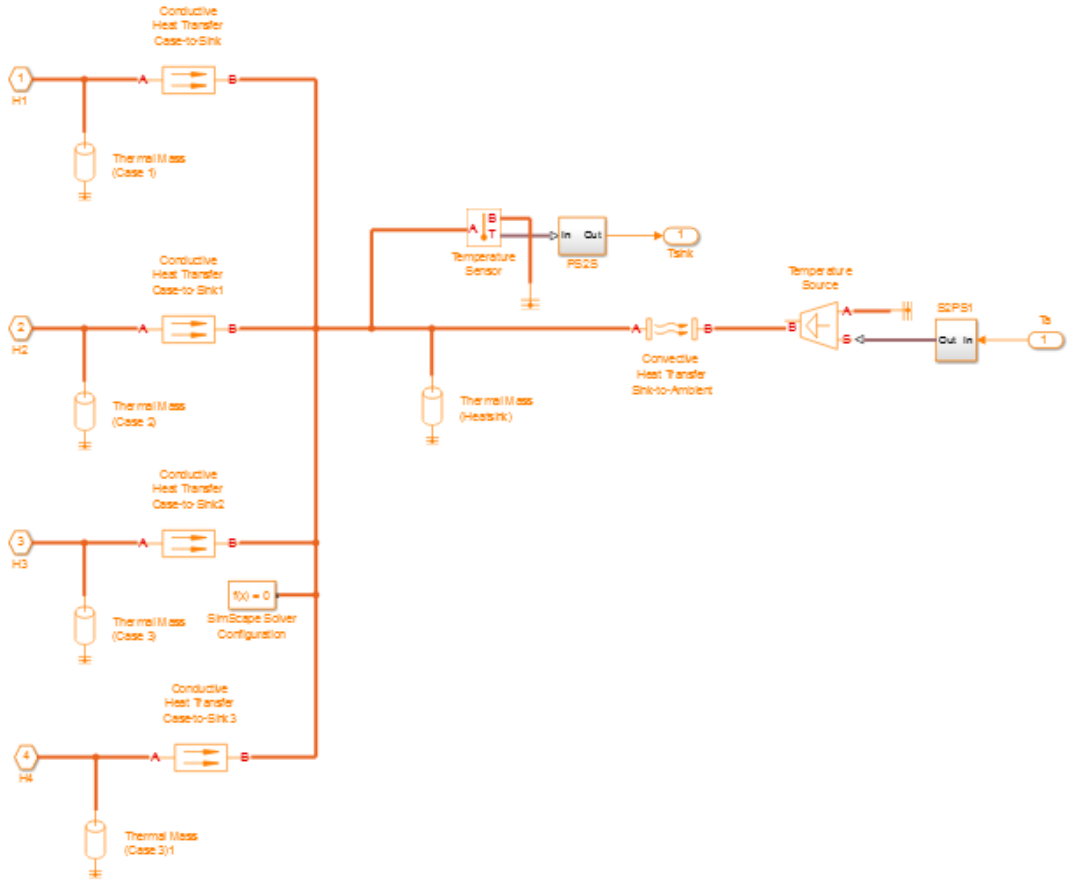


d) Detailed view inside semiconductor case

Figure 3.29. Thermal model for one leg of the LV output stage converter (cont.).



a) Masked heat sink block



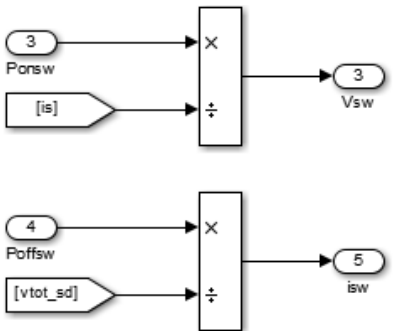
b) Detailed view of the heat sink model

Figure 3.30. The heat sink model.

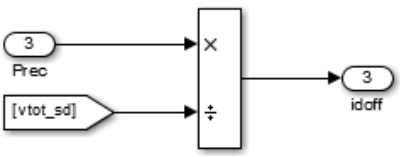
Switching losses: Two different approaches have been used to inject switching loss to switch and diode model. Instantaneous injection approach that has been used for LV side converters of SST and average injection approach that has been used for injection of switching loss to the MV side converters of SST.

Approach 1: In this approach the instantaneous value of calculated loss will be injected to semiconductor model by means of controlled voltage sources and controlled current source in one simulation time step. Instantaneous IGBT turn-on switching losses, ΔP_{onsw}, are incorporated by means of a series-connected controlled voltage source, with the value of v_{sw1}. Instantaneous IGBT turn-off switching losses, ΔP_{offsw}, are incorporated by means of a parallel-connected controlled current source, with the value i_{sw}. Reverse recovery diode losses, ΔP_{recD}, are incorporated by means of a parallel-connected controlled current source, whose value i_{recD}. Figure 3.31 shows the calculation trend for the values of controlled voltage and current sources for IGBT and diode to represent switching losses using approach 1. Figure 3.32 shows the model of IGBT and antiparallel diode with the capability of representing semiconductor losses in SST using Approach 1.

Approach 2: The representation of semiconductor losses by means of the previous approach incorporates semiconductor energy losses in a single simulation time step; this can lead to high values of the controlled voltage source and cause unstable performance of the MMC model. To solve this problem, a new approach for incorporating switching losses is proposed: conduction losses are incorporated into semiconductor models in several time steps. The values of the instantaneous total losses of IGBTs and diodes, ΔP_{totS} and ΔP_{totD}, are obtained from calculation block; then these values are incorporated in semiconductor models by means of constant controlled voltage sources (in series with either an IGBT or a diode), whose values, v_{swS} and v_{recD}, are selected as a percentage, $k_{S/D}$, of the SM capacitance voltage. This means that the controlled voltage source remains in conduction period for several time steps to model the total semiconductor losses. Figure 3.33 shows the calculation of the controlled voltage source values for IGBT and diode. Figure 3.34 shows the combined model of IGBT and antiparallel diode with the capability of representing semiconductor losses using this approach.



a) IGBT controlled voltage source and controlled current source



b) Diode controlled current source

Figure 3.31. Loss calculation block for IGBTs and diodes – Approach 1.

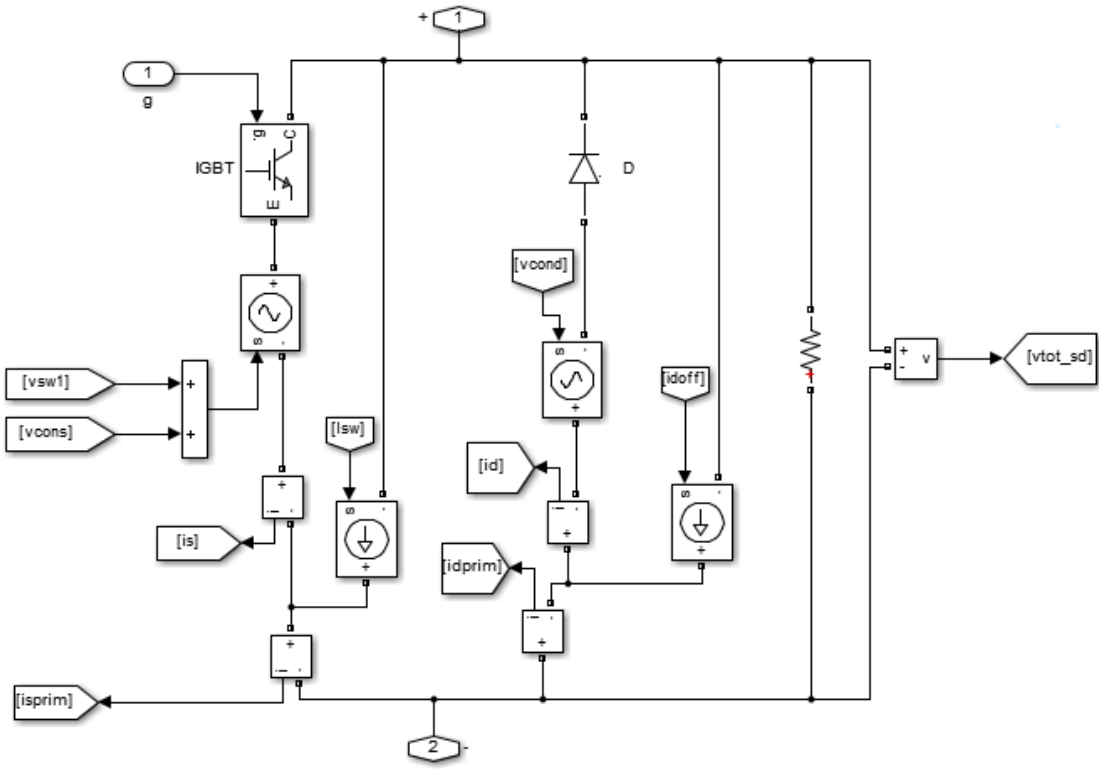
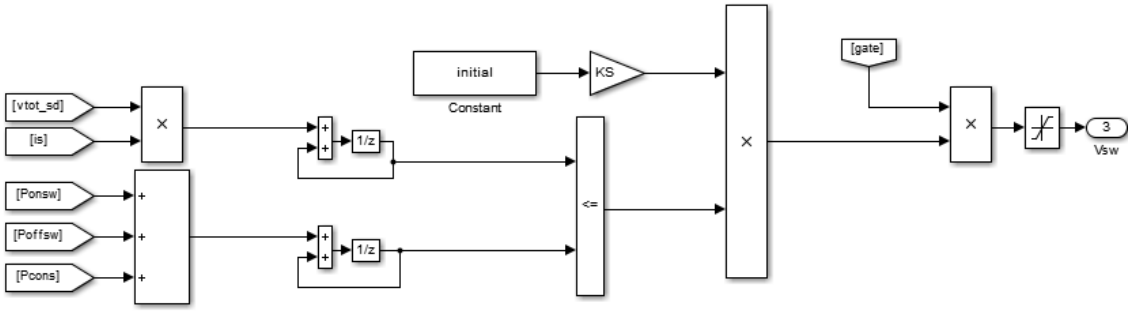
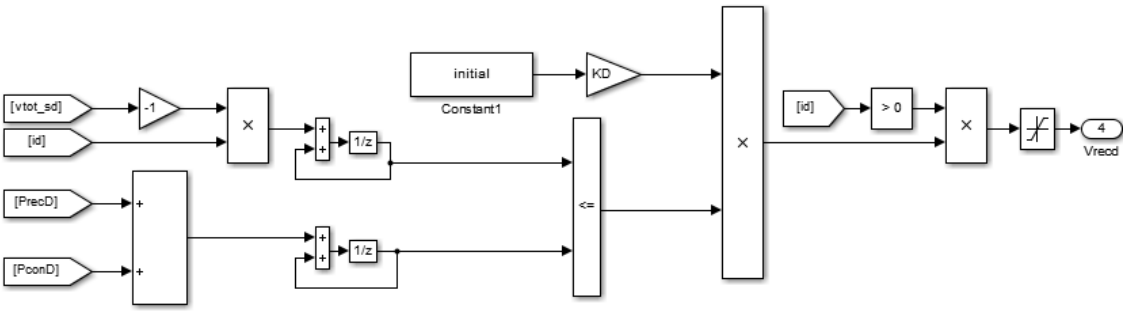


Figure 3.32. Incorporation of losses into the combined model of an IGBT and an antiparallel diode – Approach 1.



a) IGBT controlled voltage source



b) Diode controlled current source

Figure 3.33. Loss calculation block for IGBT and diode.

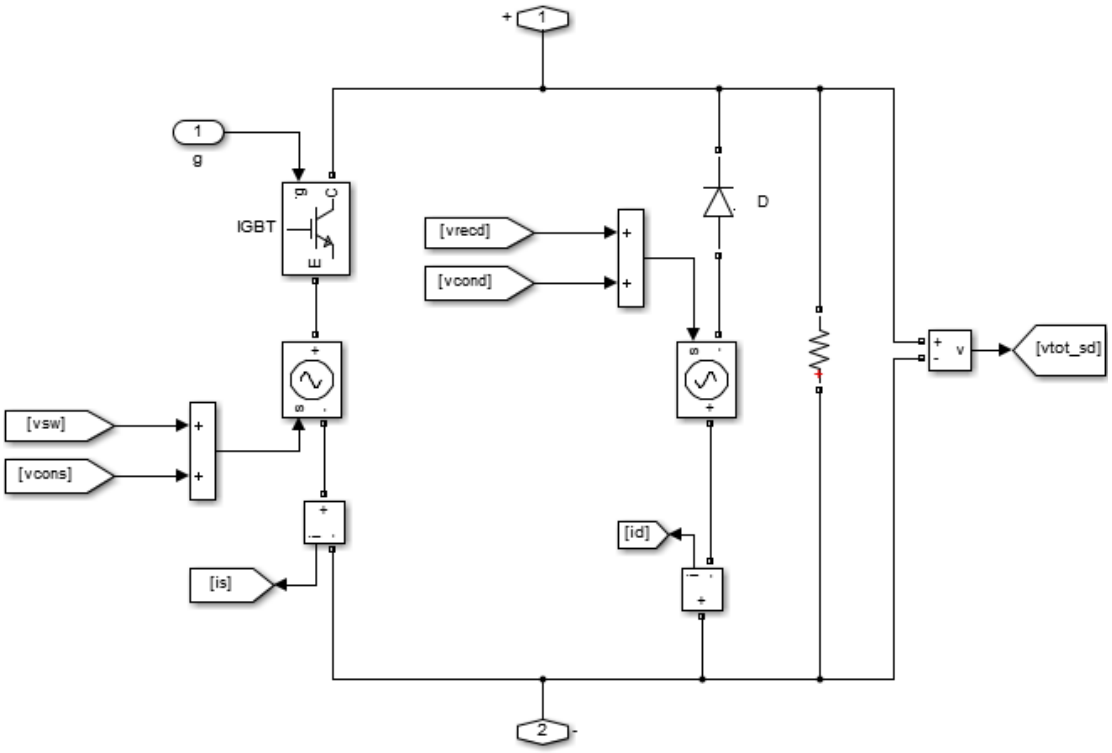


Figure 3.34. Incorporation of losses into the combined model of an IGBT and an antiparallel diode – Approach 2.

3.6. Conclusion

This chapter has summarized the MATLAB/Simulink implementation of the three-stage MMC-based SST model. A detailed description of configuration used for each stage along with control strategies are given using the figures extracted from Matlab/Simulink.

The first aim is that the three-stage SST could present an efficient performance in steady state and also under severe transient state both at the MV side and LV side: such as voltage sag occurrence at MV side and load variation, load unbalance, nonlinear load connection and short circuit occurrence at LV side. To fulfill these requirements, it is necessary to present the proper topology and proper control technique for input stage, isolation stage and output stage. The procedure of implementing topologies and control strategies for every stage are described in detail in this chapter.

The second aim is to provide realistic representation of SST with considering semiconductor losses including conduction and switching losses. To implement semiconductor losses: first, semiconductor losses are calculated from manufacturer datasheets, but since losses depend on temperature, the semiconductor thermal models are included in converter models; second, the losses are incorporated as part of the semiconductor model by means of controlled sources whose instantaneous values are obtained from the external calculation carried out in the first step. It is therefore a closed-loop approach that uses information available in manufacturer data sheets. The implementation of semiconductor losses for IGBT and diode through using controlled voltage source and controlled current source is described in this chapter in detail.

Finally, the three stage MMC-based SST has been implemented in Matlab/Simulink with and without including semiconductor losses, and have been tested under different cases studies which proves the proper performance of implemented SST.

3.7. References

[3.1] Available at: https://es.mathworks.com/matlabcentral/fileexchange/35980-loss-calculation-in-a-buck-converter-using-simpowersystems-and-simscape.

[3.2] Available at: https://es.mathworks.com/help/physmod/sps/examples/loss-calculation-in-a-three-phase-3-level-inverter.html.

Chapter4

Simulation Results

4.1. Introduction

In this chapter, simulation results derived from two test system are presented. The first test system is a stand-alone SST whose model does not consider semiconductor losses. The second test system is a MV distribution system to which a SST is connected. For this second study the SST model includes semiconductor losses. Up to six different test cases have been analyzed with the two test systems to evaluate the performance of SST. The test cases are listed below:

1. Unbalanced voltage sag and swell at the point of common coupling (PCC) at the input stage of SST.
2. Secondary side load variation.
3. Secondary side load unbalance.
4. Nonlinear load at the secondary side.
5. Short-circuit at the secondary side.
6. Power flow reversal.

Sections 4.2 and 4.3 present the test systems, the test cases simulated with each system and a discussion about the results and the performance of each SST model.

4.2. Simulation Results with a Lossless Stand-alone SST Model

4.2.1. Test system and test cases

The model of the SST has been implemented in Matlab/Simulink assuming the parameters listed in Table 4.1. The test system is that obtained when joining the three stages depicted in Figures 2.2, 2.8 and 2.10. This configuration will be used to evaluate the behavior of the SST model under dynamic and unbalanced conditions (voltage sags, load increment, load unbalance, nonlinear load, short circuit), and operation conditions

that could cause power flow reversal (i.e., active power flowing from the LV to the MV side).

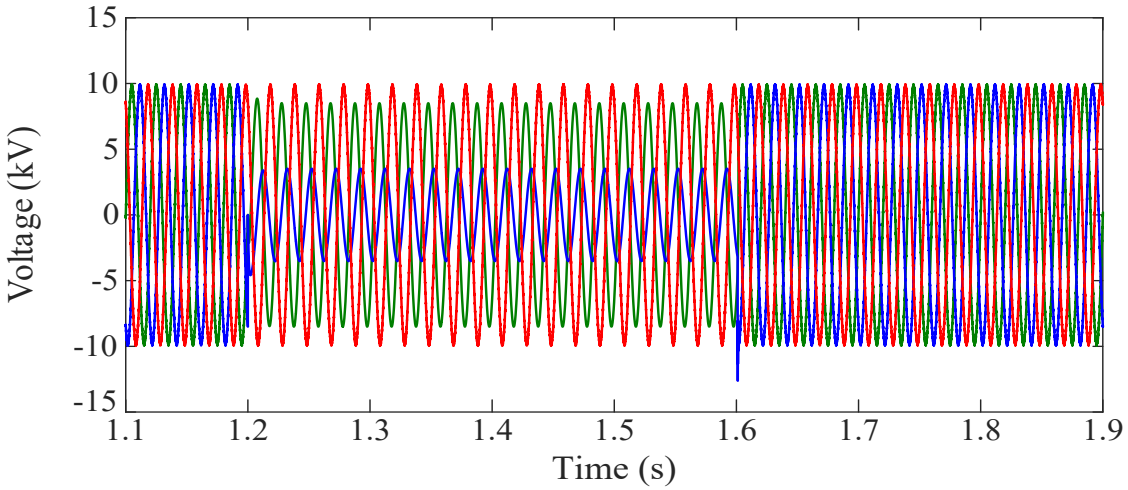
Table 4.1. Fist case study - SST parameters

Parameters	Values
Line-to-line grid voltage (rms)	12 kV
Grid-side filter resistance (R_1)	0.1 Ω
Grid-side filter inductance (L_1)	10 mH
Number of SMs per MMC arm	6
SM capacitance in MMC1&MMC2	0.4 mF
Arm resistance of MMC1	0.2 Ω
Arm inductance of MMC1	5 mH
MMC1 switching frequency	10 kHz
MV-side dc link capacitance	1 mF
Arm resistance of MMC2	0.001
Arm inductance of MMC2	0.1 mH
MV MMC2 and LV full bridge converter switching frequency	10 kHz
Transformer operating frequency	1 kHz
Transformer short-circuit resistance	0.005 Ω
Transformer leakage inductance	0.03 mH
LV-side dc link capacitance	3 mF
LV-side converter switching frequency	10 kHz
Load-side filter resistance (R_2)	0.01 Ω
Load-side filter inductance (L_2)	0.9 mH
Load-side filter capacitance (C_2)	200 μF
Neutral resistance (R_{n2})	0.01 Ω
Neutral inductance (L_{n2})	0.3 mH

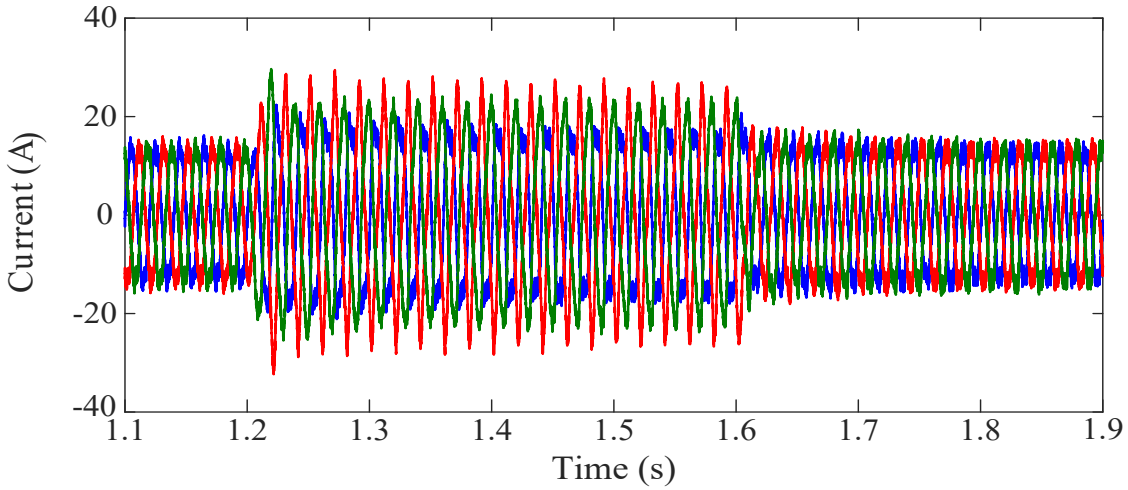
All test cases have been simulated assuming the rated power of the SST is below 250 kVA. Remember that semiconductor losses are neglected, so semiconductor ratings are irrelevant for this study. The reactive power to be measured at the MV terminals of the SST will be always close to zero; that is, the SST will compensate at the MV terminals the reactive power measured at the LV terminals, irrespective of its value and direction.

The simulation results derived from several test cases carried out to evaluate the performance of the proposed SST model are presented below. The operating conditions for each test case are based on those considered in [4.1]-[4.3].

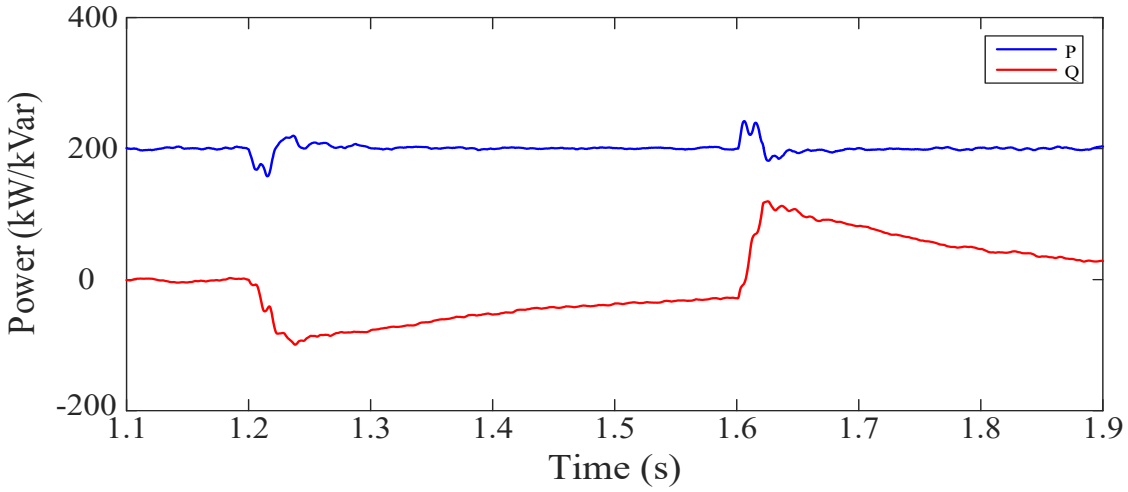
1. *Unbalanced voltage sag at the primary side* (see Figure 4.1): A voltage sag occurs at the source that feds the MV side of the SST. Between 1200 and 1600 ms voltages of phases A and B experiments a reduction. As observed from Figure 4.1, the distorted voltages and currents at MV side do not affect voltages the LV side; that is, the voltage sag is not propagated to the LV stage of the SST, and the load currents will remain balanced as they were prior to the sag occurrence (see Figure 4.1).
2. *Secondary load variation* (Figure 4.2): A load variation that causes an increment of the LV-side currents occurs between 1200 and 1600 ms. The increment of the balanced secondary currents do not cause any variation of the voltage supplied from the output stage of the SST. One can also observe from Figure 4.2 how the MV-side currents vary following a pattern very similar to that exhibited by LV-side load currents.



a) Primary side voltages

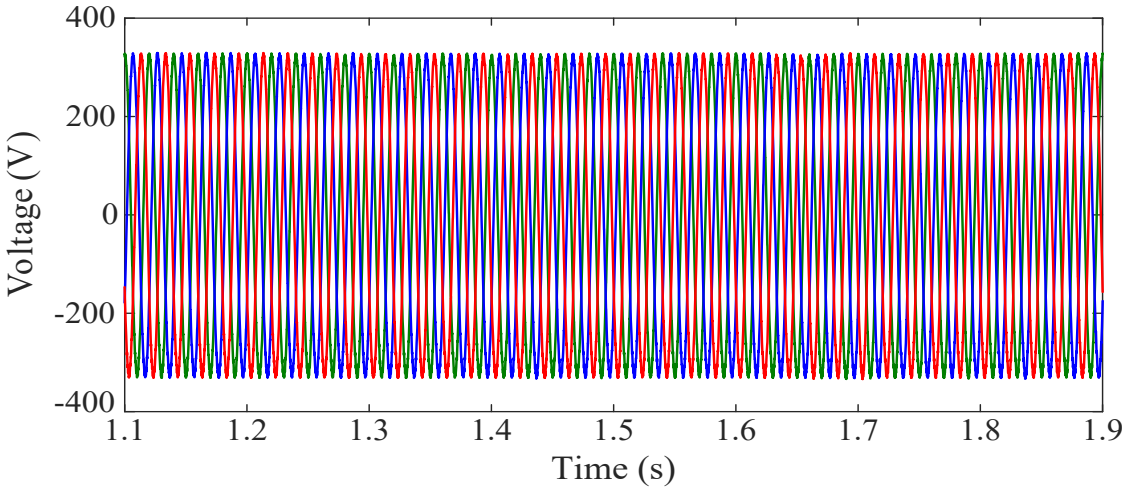


b) Primary side currents

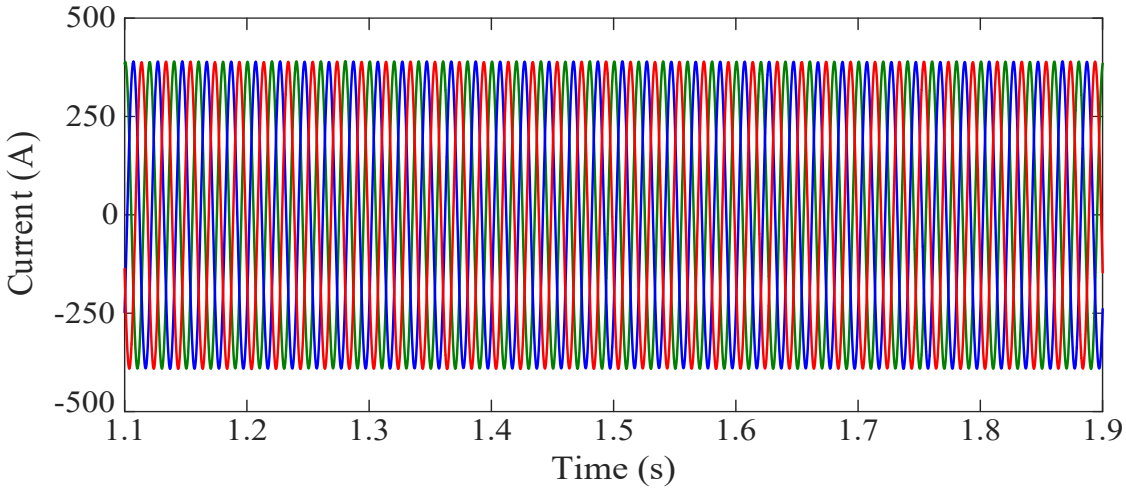


c) Primary side active and reactive powers

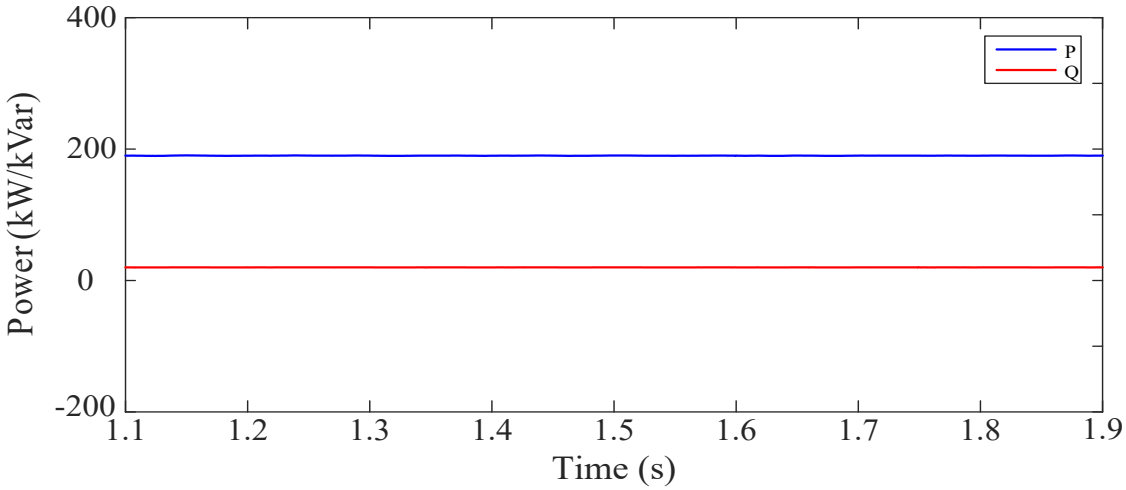
Figure 4.1. Test System 1 - Simulation results: Voltage sag at the MV side.



d) Secondary side voltages

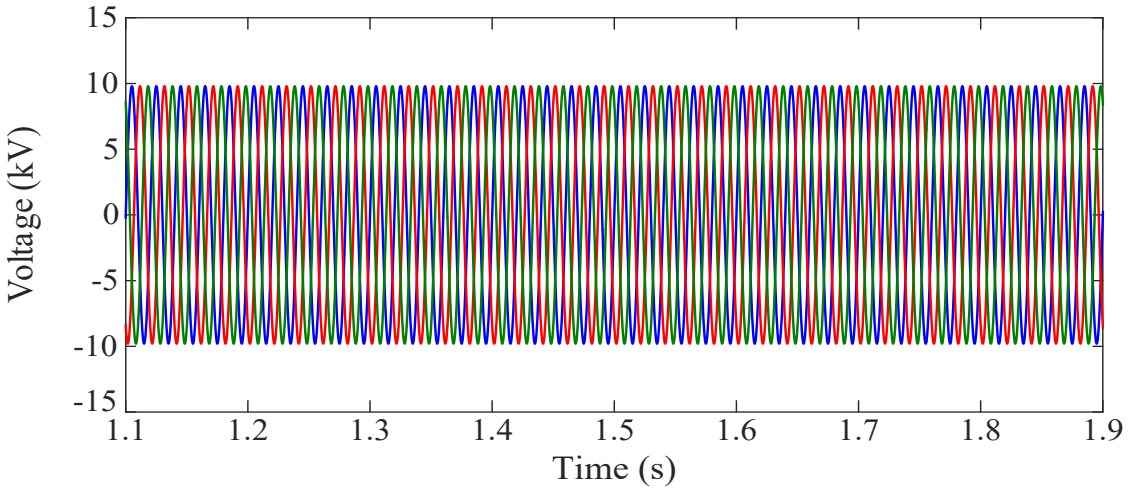


e) Secondary side currents

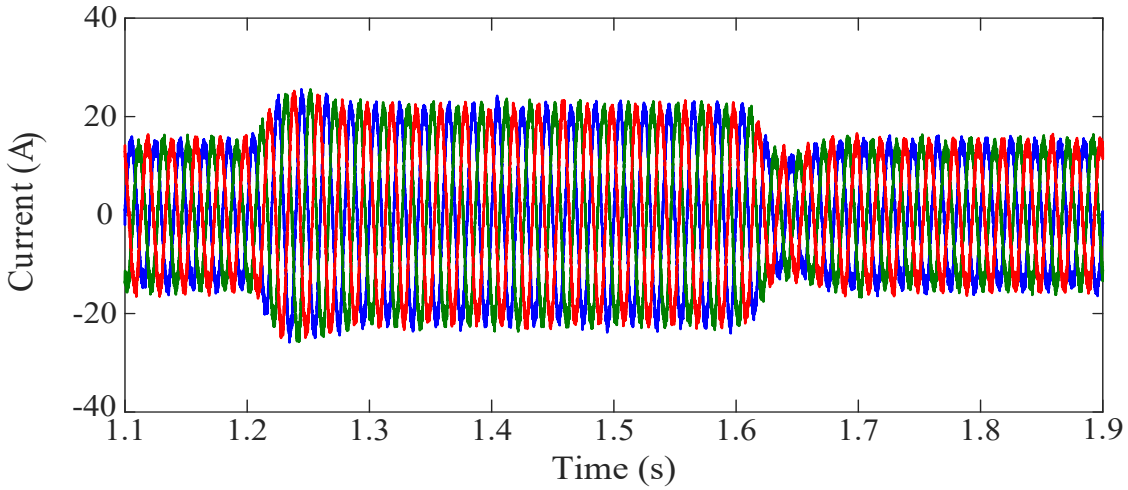


f) Secondary side active and reactive powers

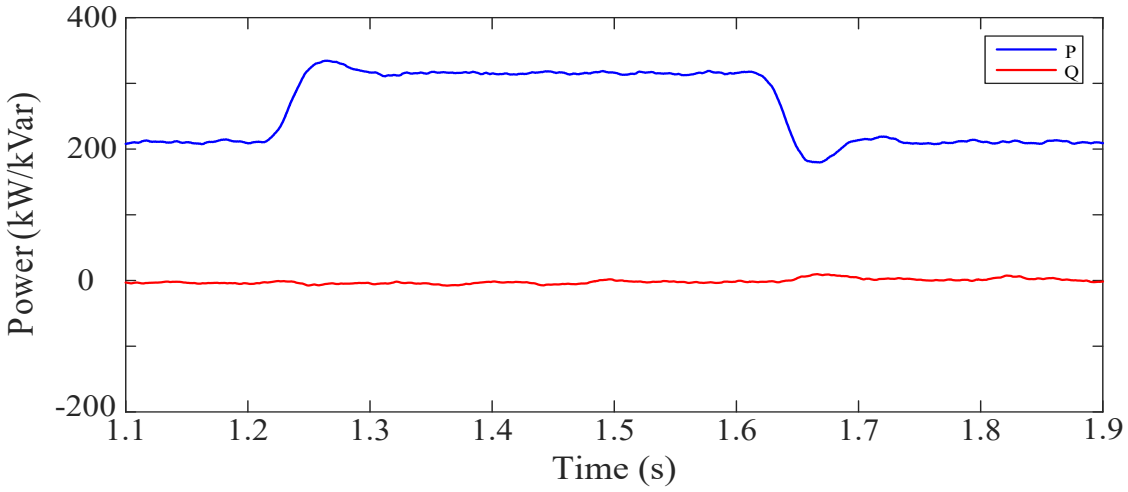
Figure 4.1. Test System 1 - Simulation results: Voltage sag at the MV side (cont.).



a) Primary side voltages

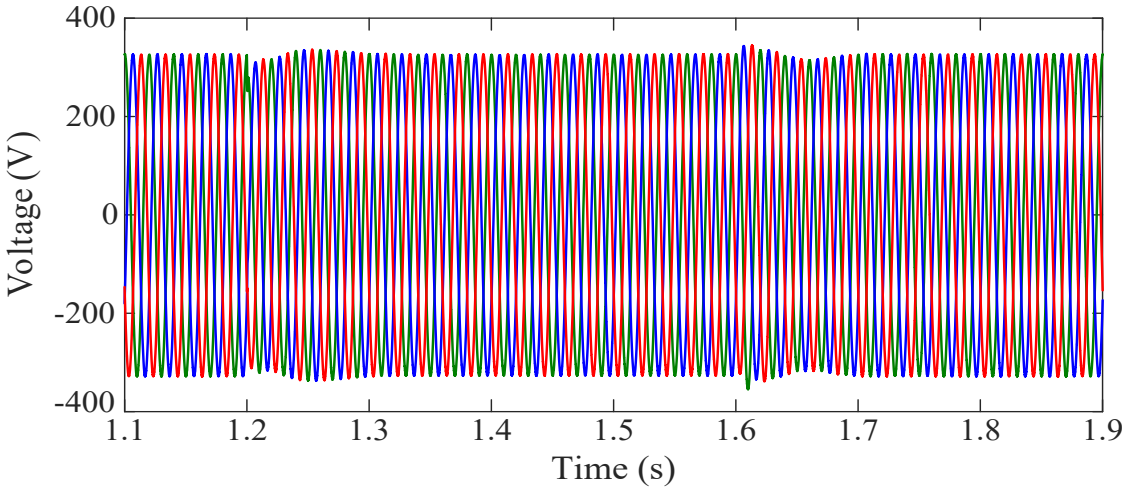


b) Primary side currents

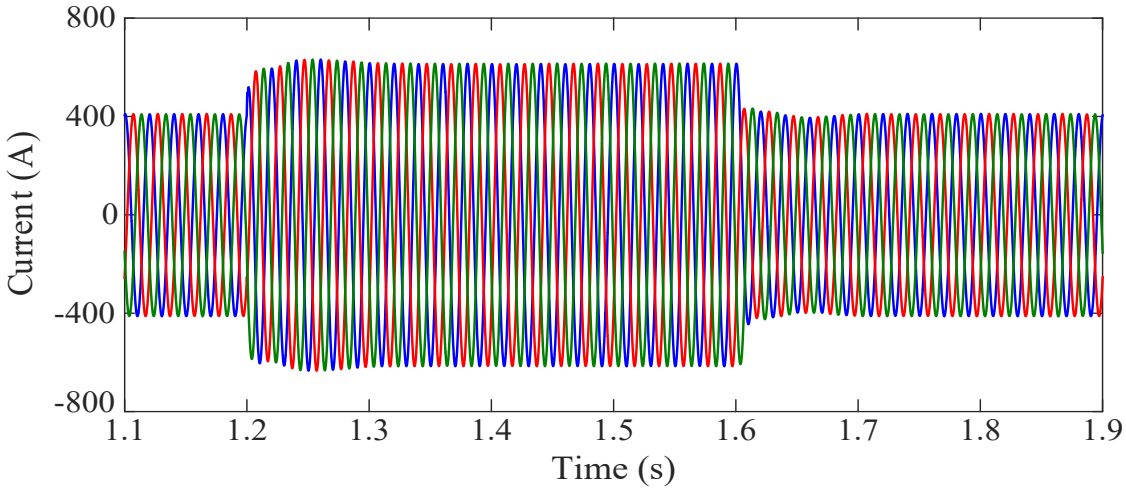


c) Primary side active and reactive powers

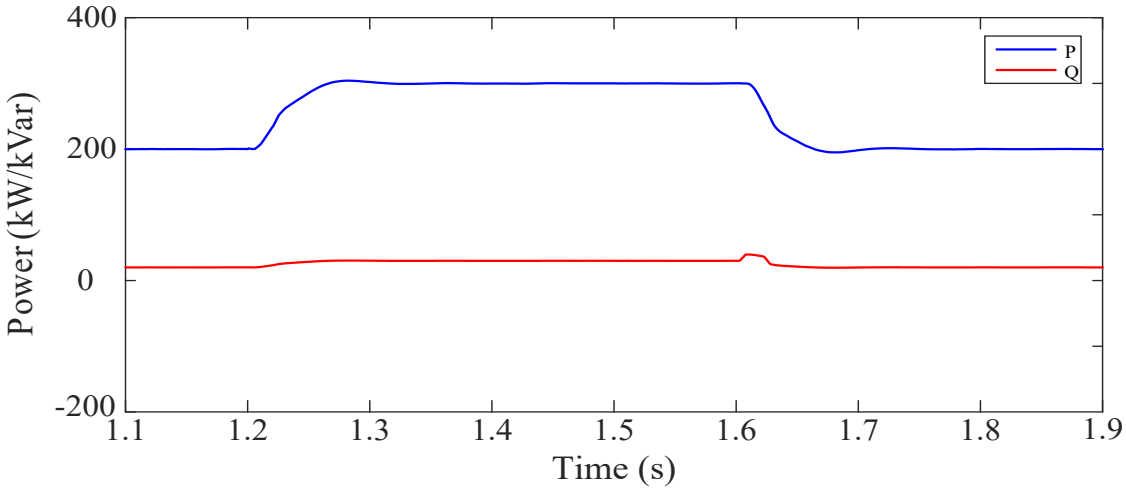
Figure 4.2. Test System 1 - Simulation results: LV-side load variation.



d) Secondary side voltages



e) Secondary side currents

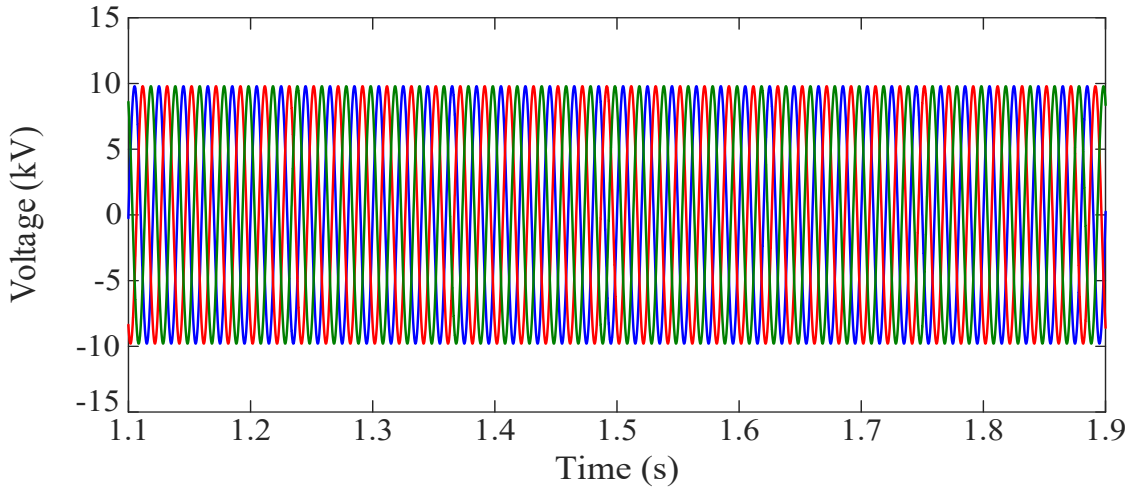


f) Secondary side active and reactive powers

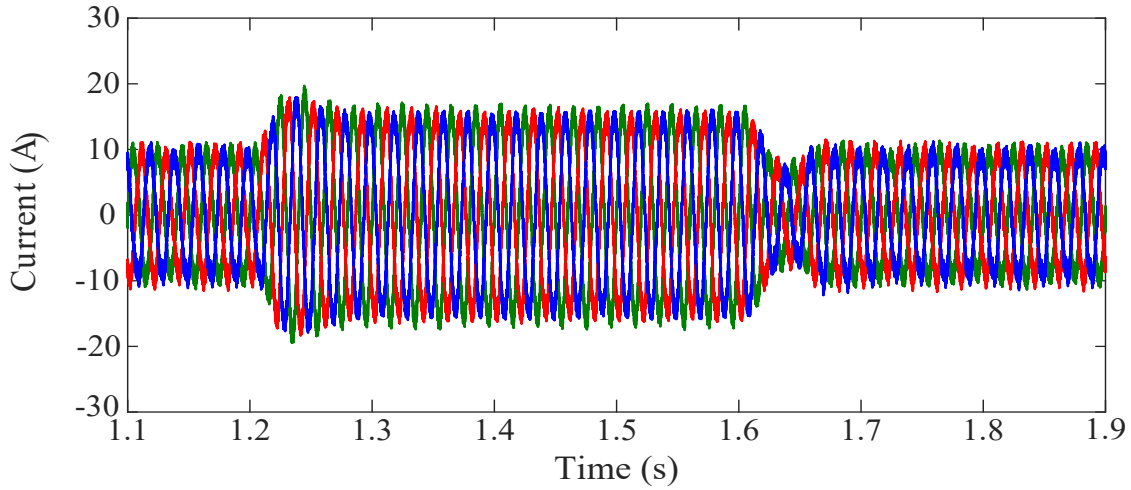
Figure 4.2. Test System 1 - Simulation results: LV-side load variation (cont.).

3. *Secondary load unbalance* (Figure 4.3): A current unbalance is caused to initially balanced load currents. The unbalance is due to an increase of the current in two load phases. Results present in Figure 4.3 proves that the secondary phase voltages remain constant during the load variation and the current unbalance is not propagated to the input stage where the three phase currents increase simultaneously without exhibiting any unbalance.
4. *Nonlinear and unbalance secondary load* (Figure 4.4): three-phase diode rectifier which serves as nonlinear load is connected to the LV stage of SST. One can also observe from Figure 4.4 that the LV-side voltages are not affected by the secondary nonlinear load/current due to the capability of HVC control strategy implemented at LV stage; however, the MV-side currents remain always balanced and they follow a similar pattern to that exhibited by the secondary LV-side currents.
5. *Short-circuit at the secondary side* (Figure 4.5): A three-phase short circuit with fault resistance of 0.1 occurs at the LV terminals of the SST. Theoretically, this should cause a large increase of the phase currents at the LV SST terminals. However, the voltage drop experienced at the secondary side of the SST significantly reduces the short-circuit currents, although the phase currents are larger than before the short-circuit occurrence. The combination of lower voltages and larger currents causes a reduction of both the active and reactive powers measured at the LV terminals. This means that the active power measured at the MV terminals will also be lower than before the short-circuit occurrence (remember that the reactive power is close to zero at the MV side). As a consequence the currents flowing into the SST at the MV terminals will be lower during the fault condition than before; that is, the SST prevents from propagating the short-circuit overcurrents to the MV grid.
6. *Power flow reversal* (Figure 4.6): The SST is initially operating in generation mode; that is, generation is initially predominant in the secondary side and the active power flows from the output stage (LV side) to the input stage (MV side) of the SST. Reactive power measured at the LV-side terminals is initially zero. A variation of the secondary load causes a reversal of the active power flow and an increment of the reactive power. Results presented in Figure 4.6 show the response of the SST: as soon as the secondary-side power flow reversal is noticed, the SST controllers act and they allow active power to flow from the MV side to the LV side, while the reactive power measured at the MV terminals remain close to zero, irrespective of the reactive power measured at the LV terminals. Other results not shown in Figure 4.6 support the feasibility of the SST since the secondary-side voltages are not affected by the transient due to the power flow reversal, and both MV- and LV-side currents remain balanced.

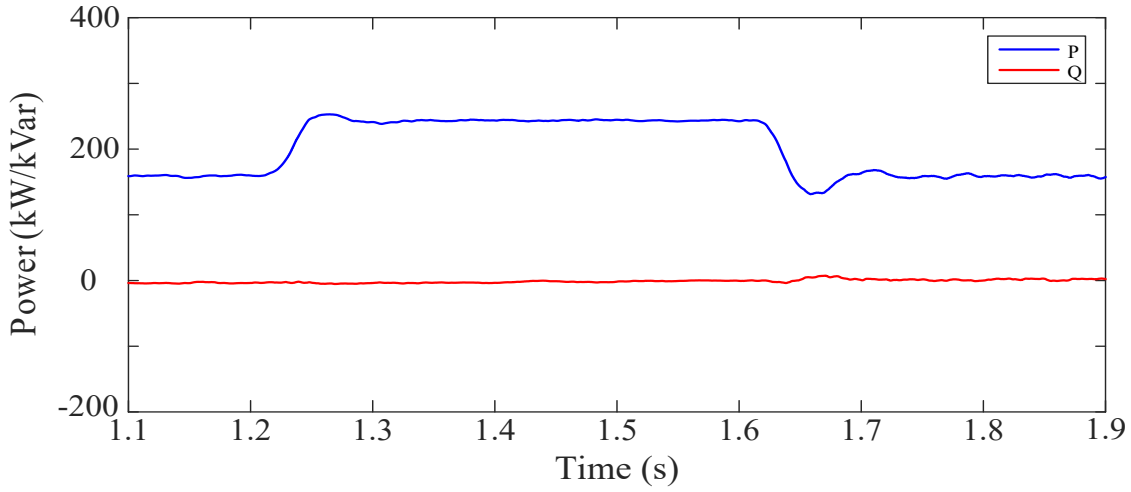
In summary, the study of these case studies proves the robustness of the SST in front of some severe operating conditions (i.e. voltage sag occurrence at the primary terminals, fault condition at the secondary terminals), the possibility of providing unity power factor at the MV side of SST, stable behavior of MV and LV DC links, balanced capacitance voltages in MMC arms under both steady state and transient conditions, capability to cancel negative and zero sequence voltage (thus providing three-phase balanced voltage when connected to unbalanced load), harmonic voltage compensation with nonlinear load, current limiting in case of short circuit at the low voltage stage, and bidirectional power flow capability.



a) Primary side voltages

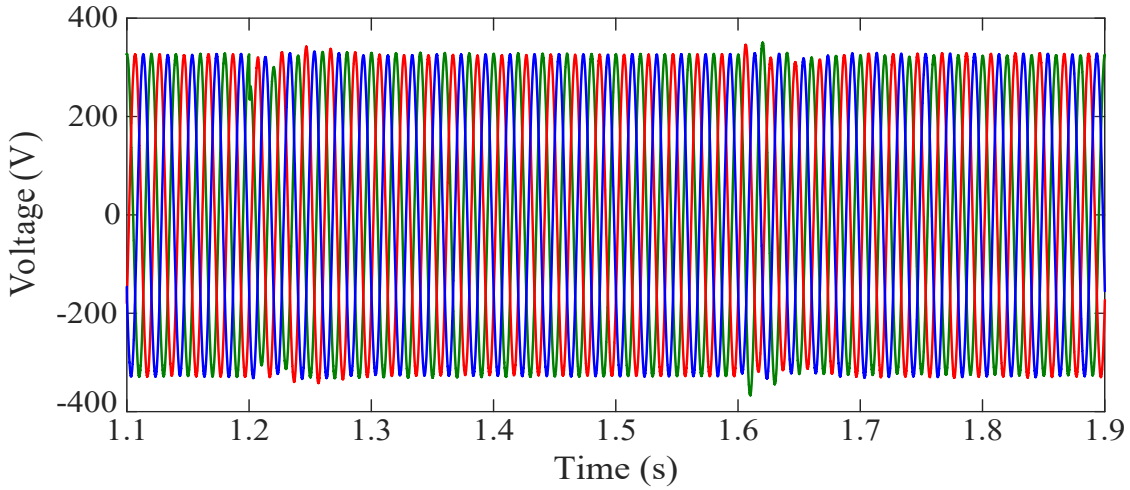


b) Primary side currents

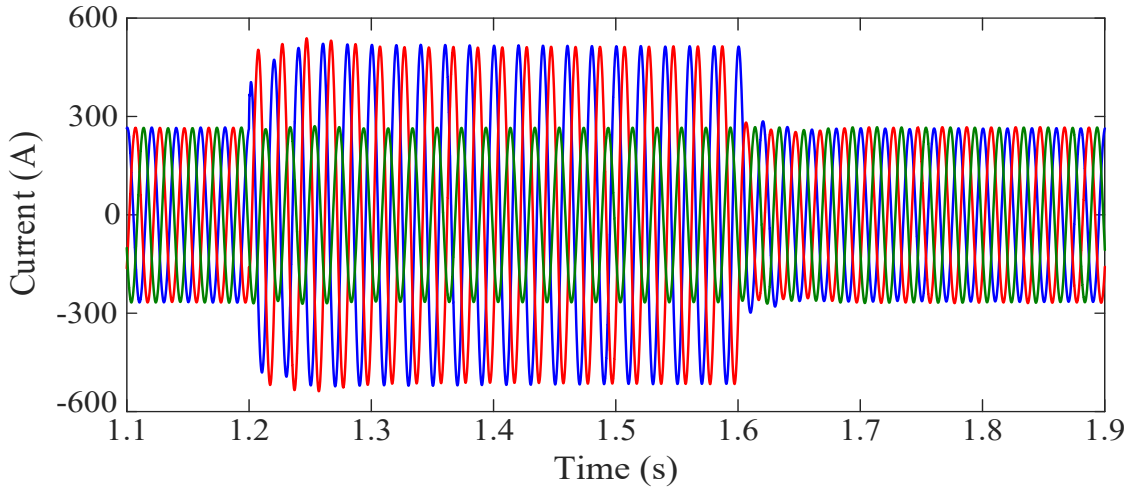


c) Primary side active and reactive powers

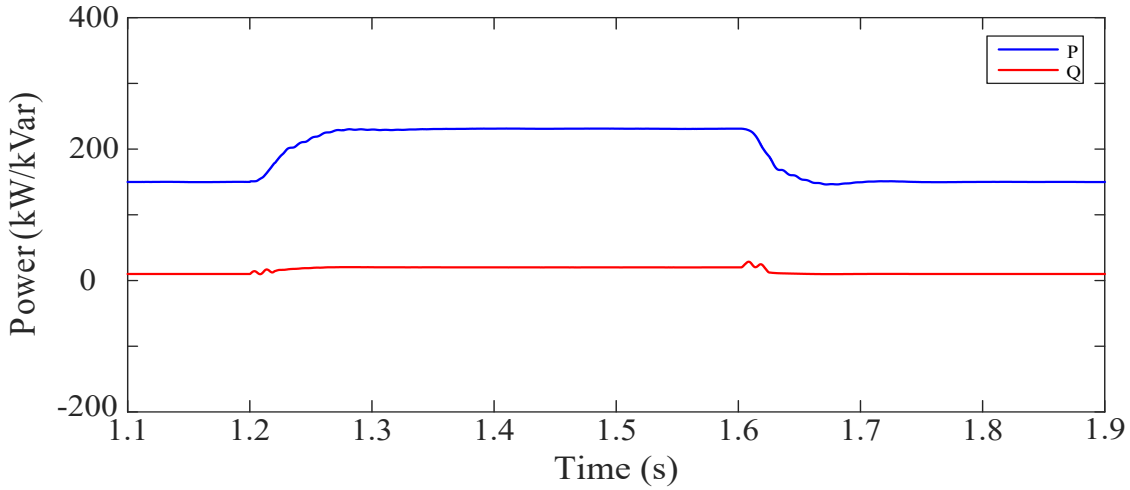
Figure 4.3. Test System 1 - Simulation results: Unbalanced LV-side load.



d) Secondary side voltages

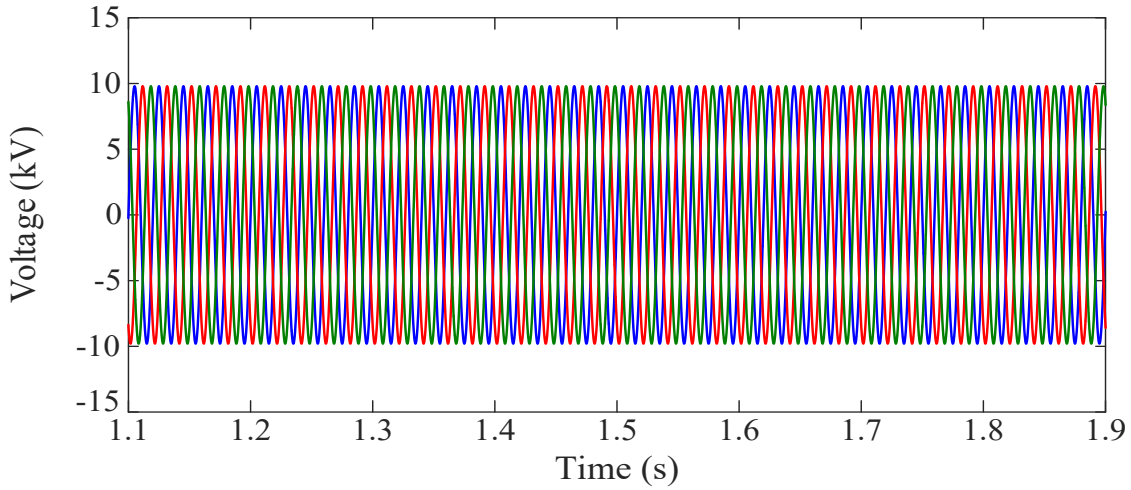


e) Secondary side currents

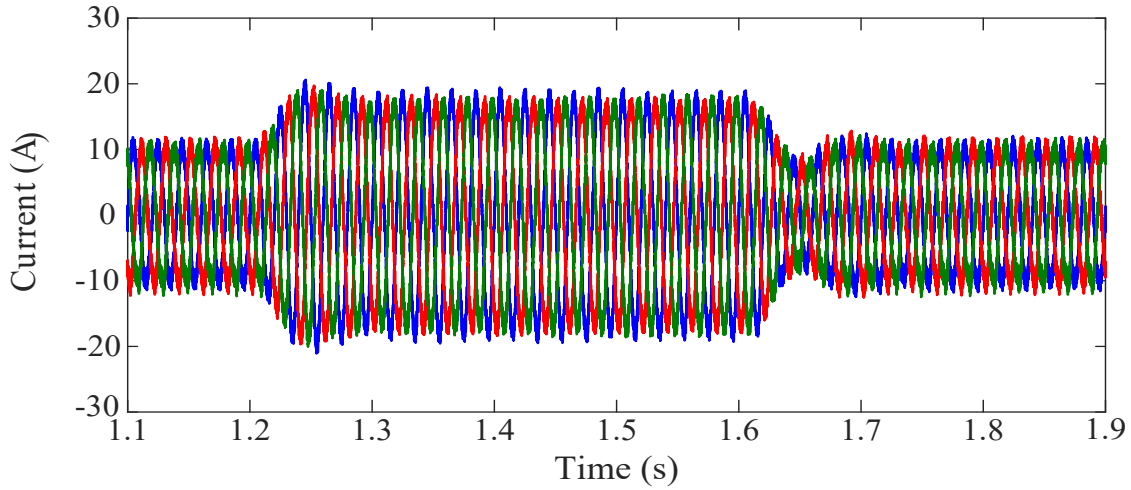


f) Secondary side active and reactive power

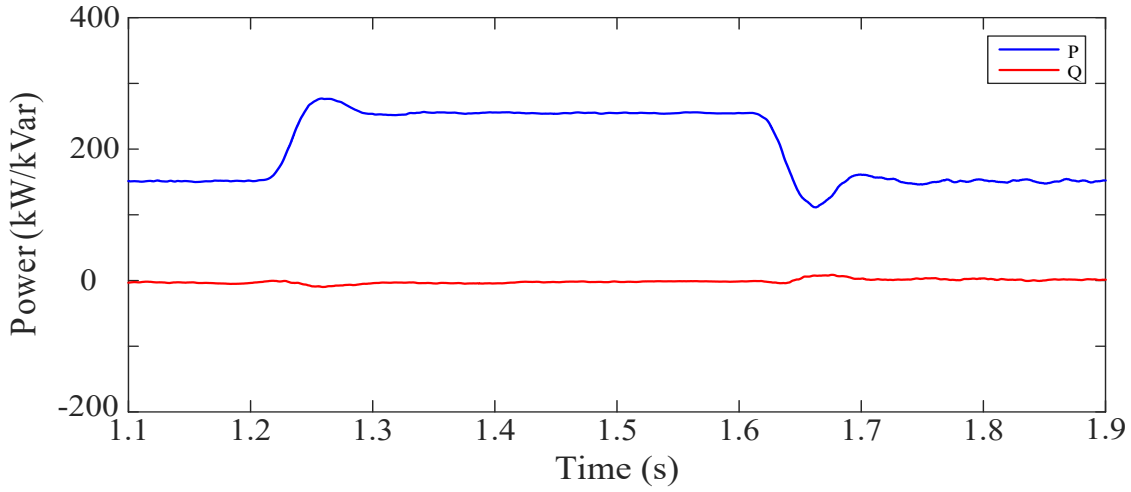
Figure 4.3. Test System 1 - Simulation results: Unbalanced LV-side load (cont.).



a) Primary side voltages

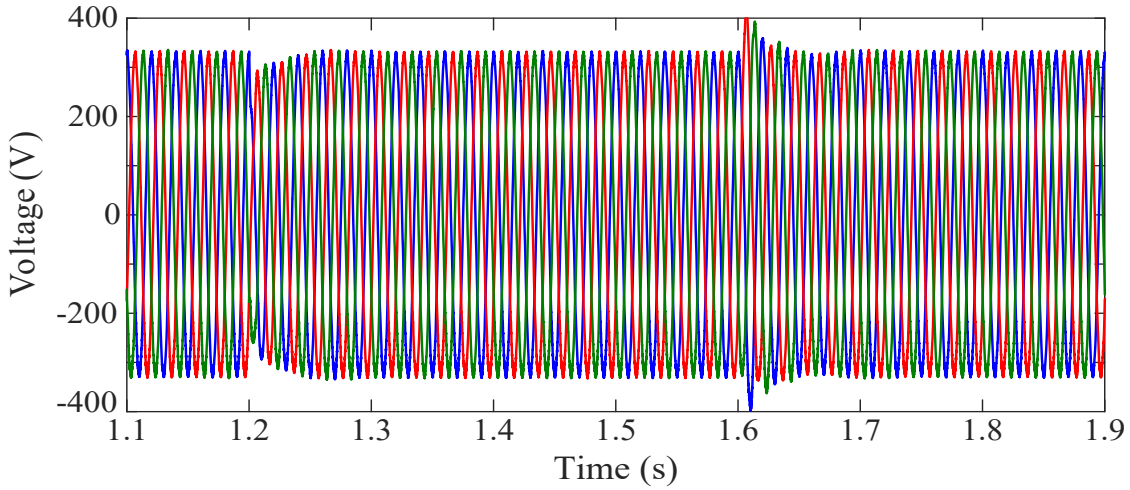


b) Primary side currents

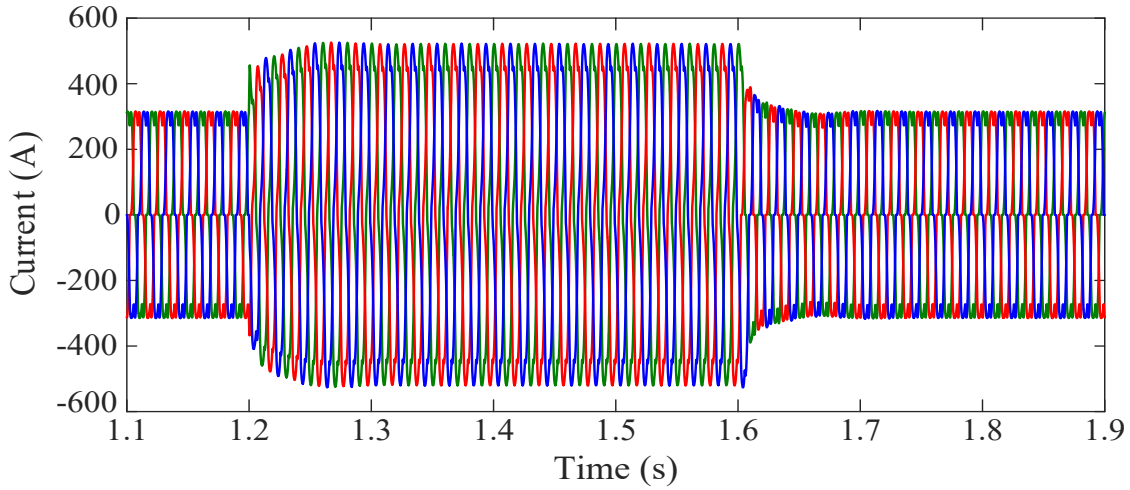


c) Primary side active and reactive powers

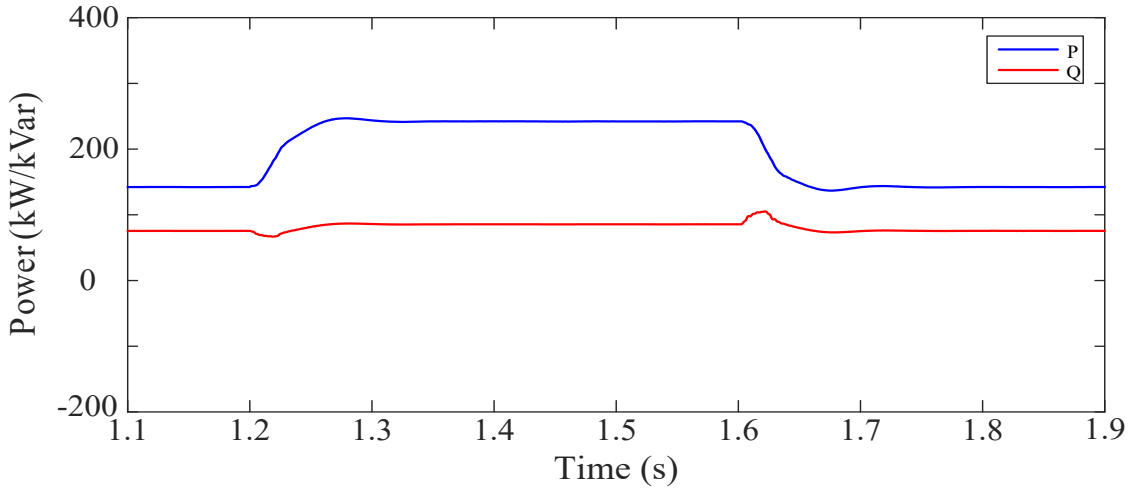
Figure 4.4. Test System 1 - Simulation results: Nonlinear LV-side load.



d) Secondary side voltages

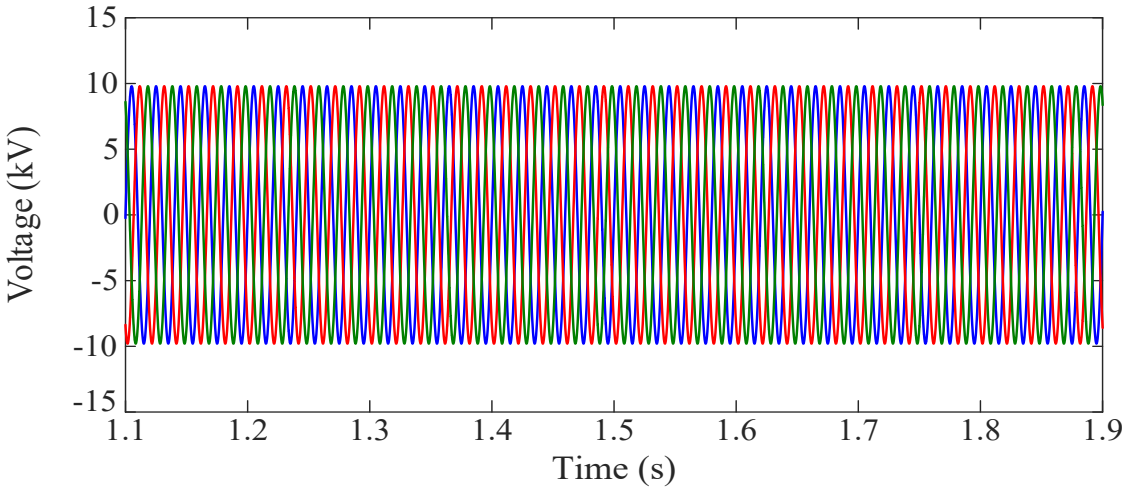


e) Secondary side currents

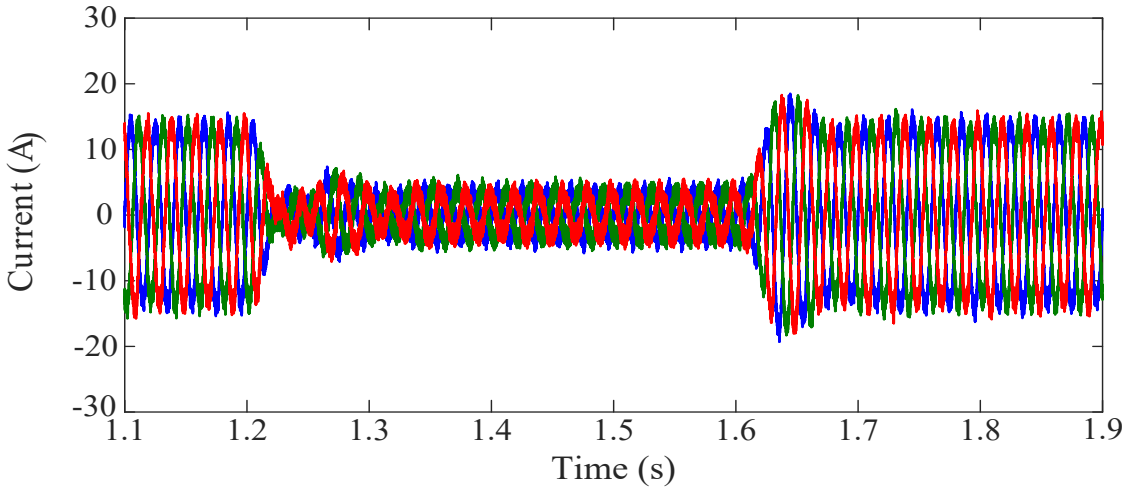


f) Secondary side active and reactive powers

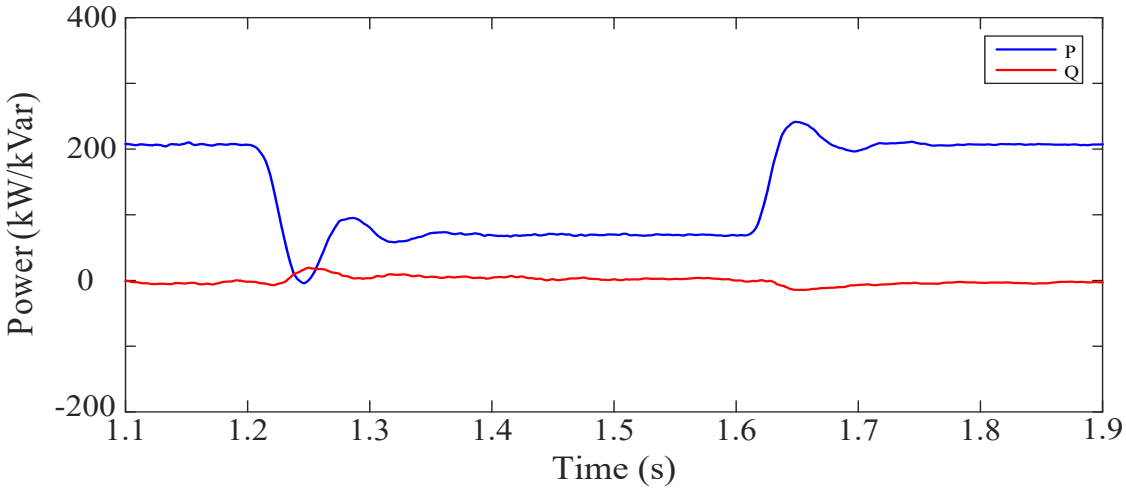
Figure 4.4. Test System 1 - Simulation results: Nonlinear LV-side load (cont.).



a) Primary side voltages

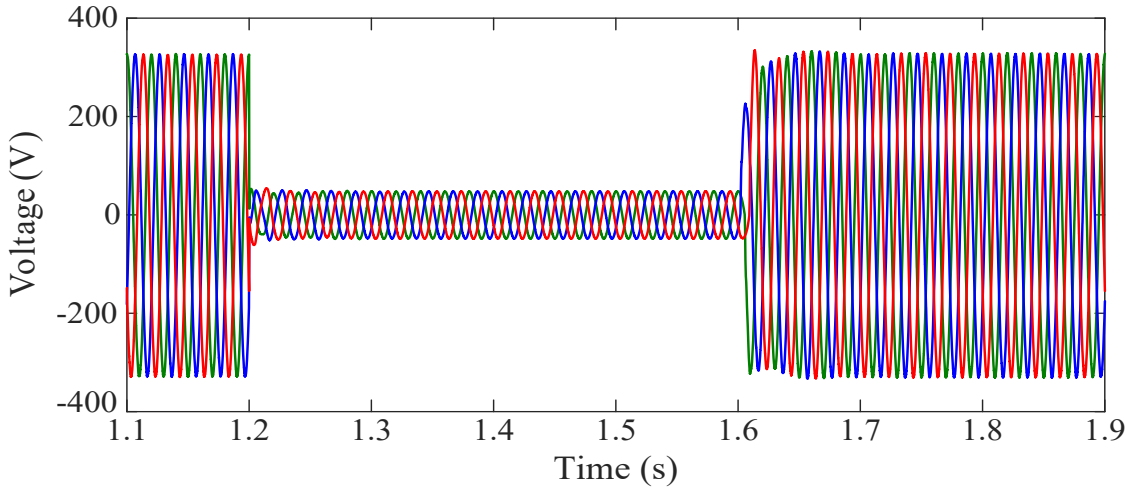


b) Primary side currents

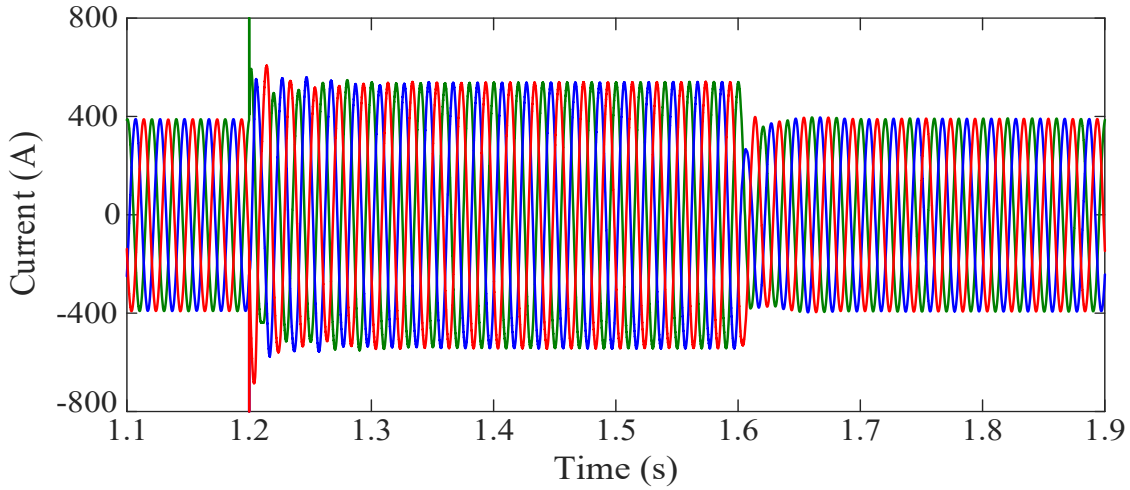


c) Primary side active and reactive powers

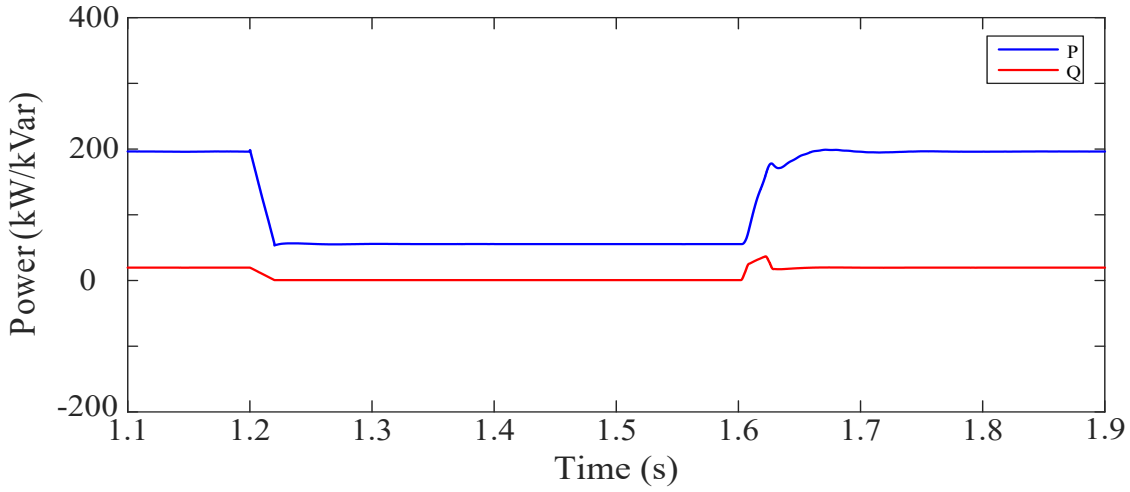
Figure 4.5. Test System 1 - Simulation results: Short-circuit at the LV terminals.



d) Secondary side voltages

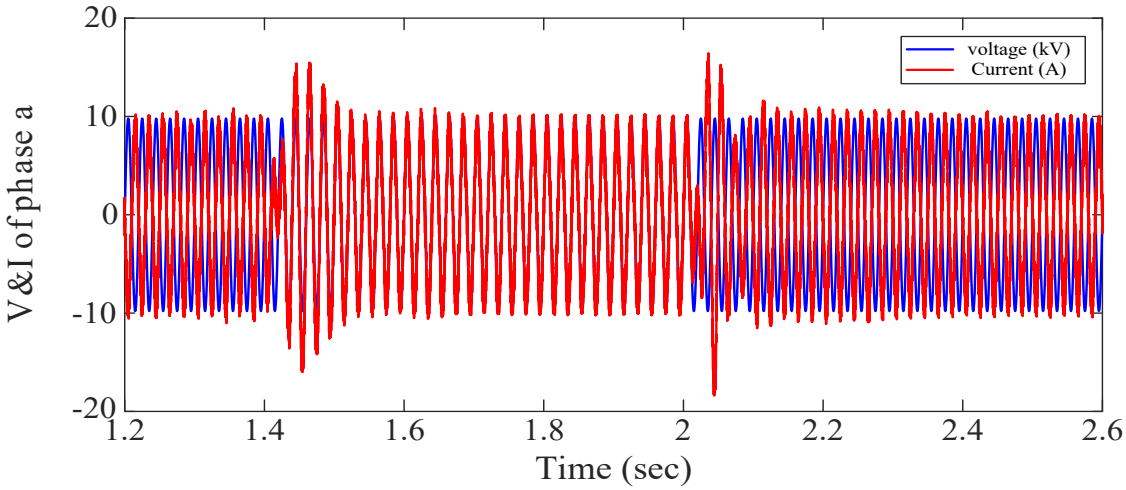


e) Secondary side currents

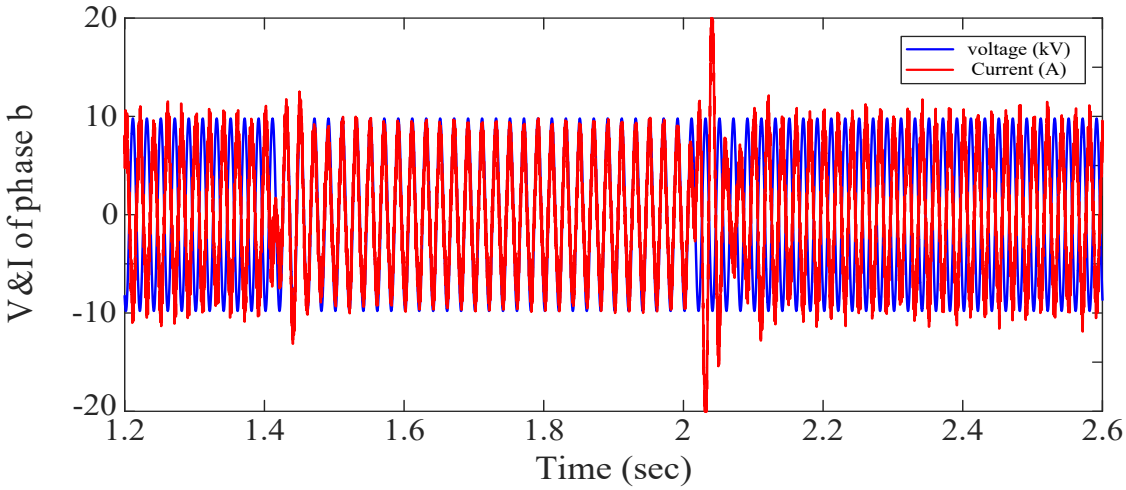


f) Secondary side active and reactive powers

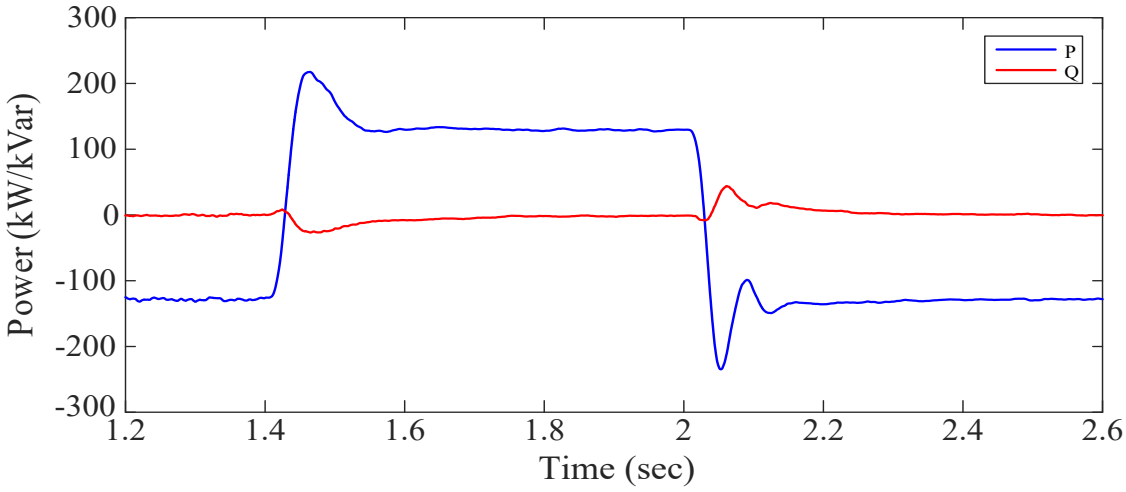
Figure 4.5. Test System 1 - Simulation results: Short-circuit at the LV terminals (cont.).



a) Primary side voltage and current - Phase A

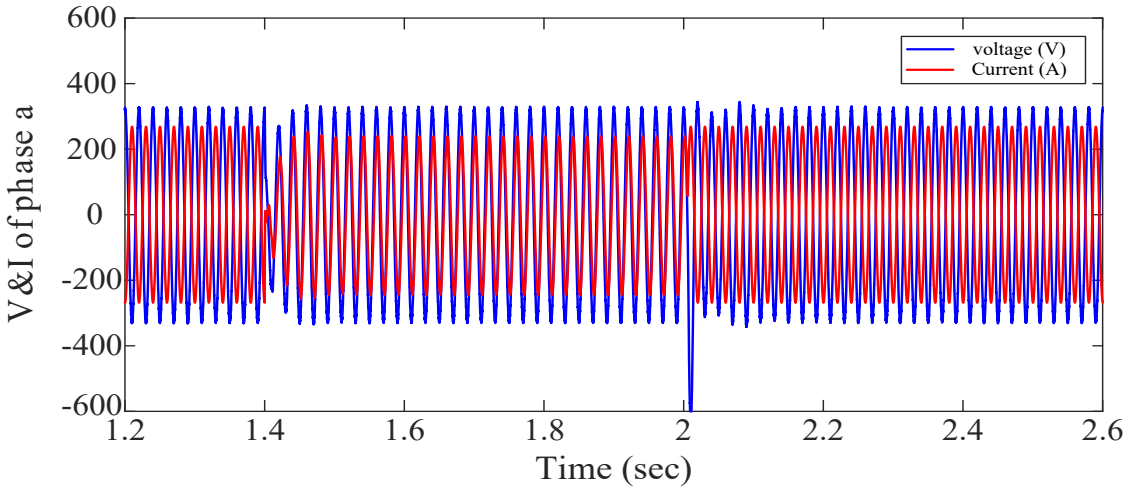


b) Primary side voltage and current - Phase B

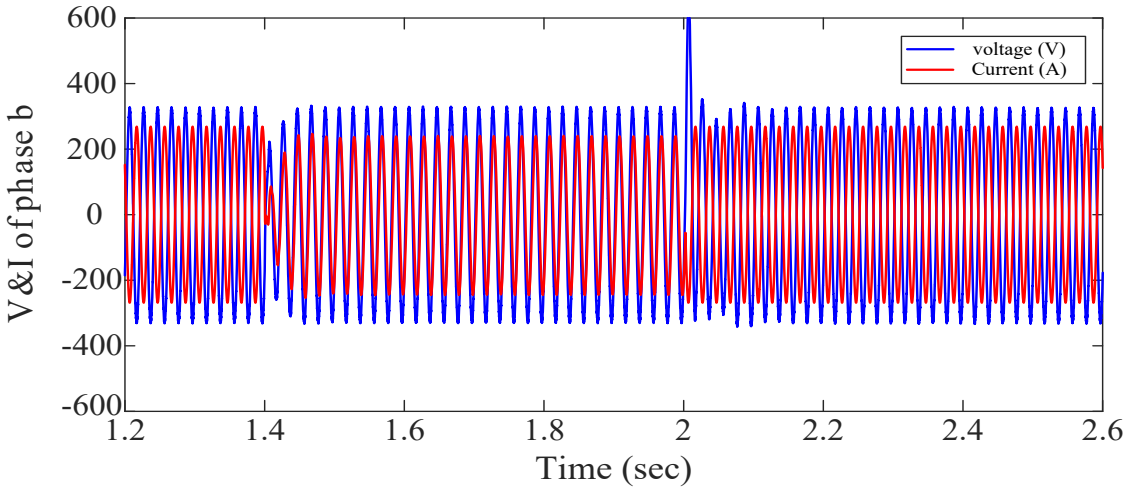


c) Primary side active and reactive powers

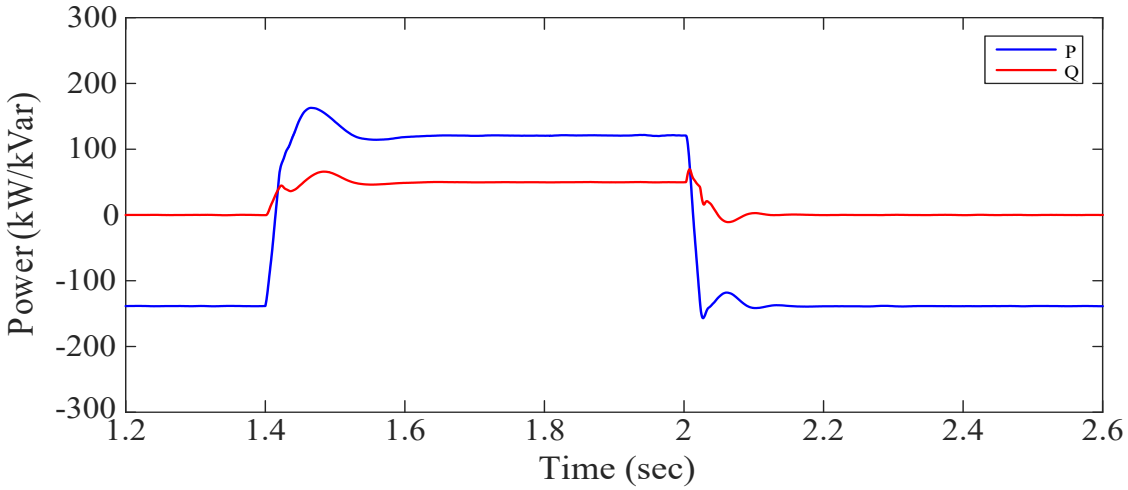
Figure 4.6. Test System 1 - Simulation results: Power flow reversal.



d) Secondary side voltage and current - Phase a



e) Secondary side voltage and current - Phase b

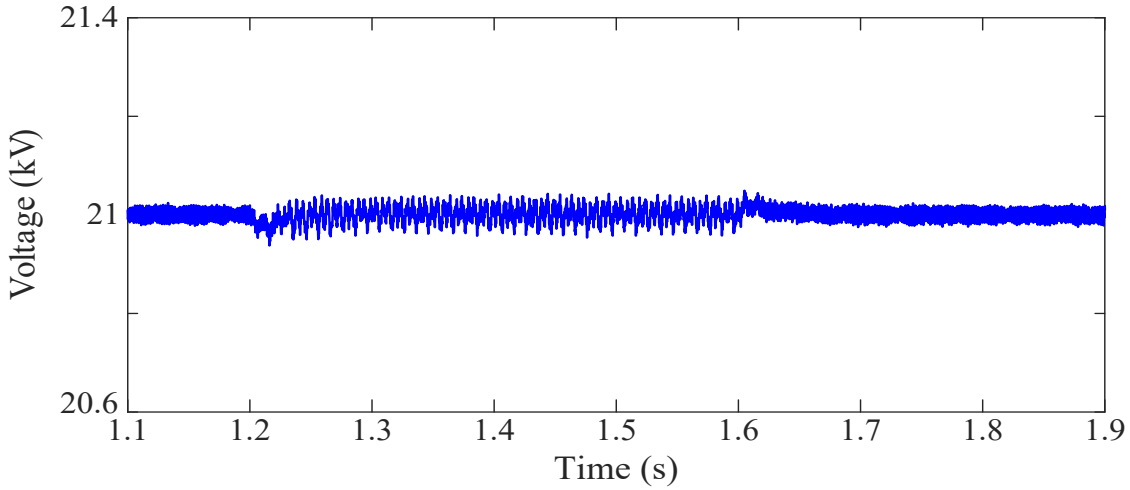


f) Secondary side active and reactive powers

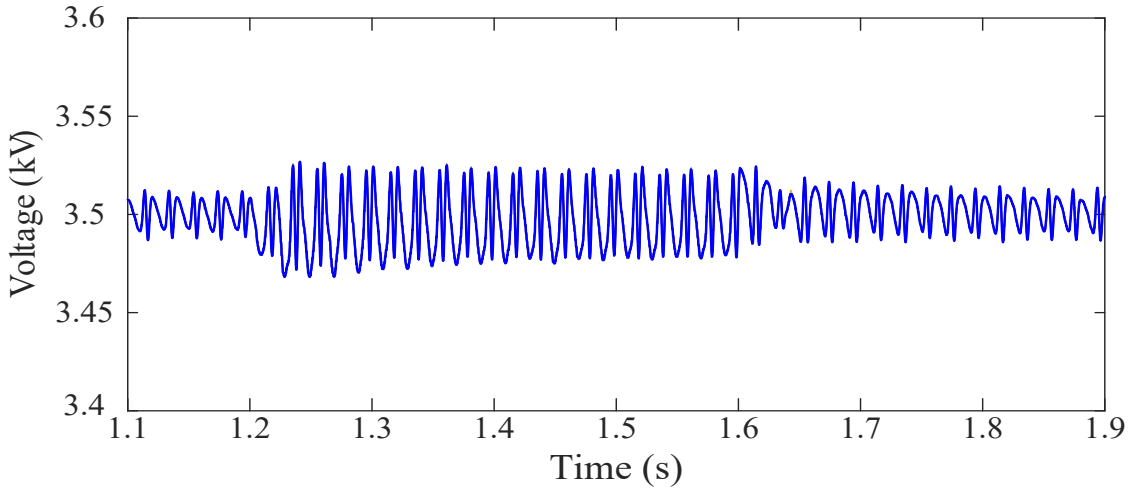
Figure 4.6. Test System 1 - Simulation results: Power flow reversal (cont.).

4.2.2. Discussion

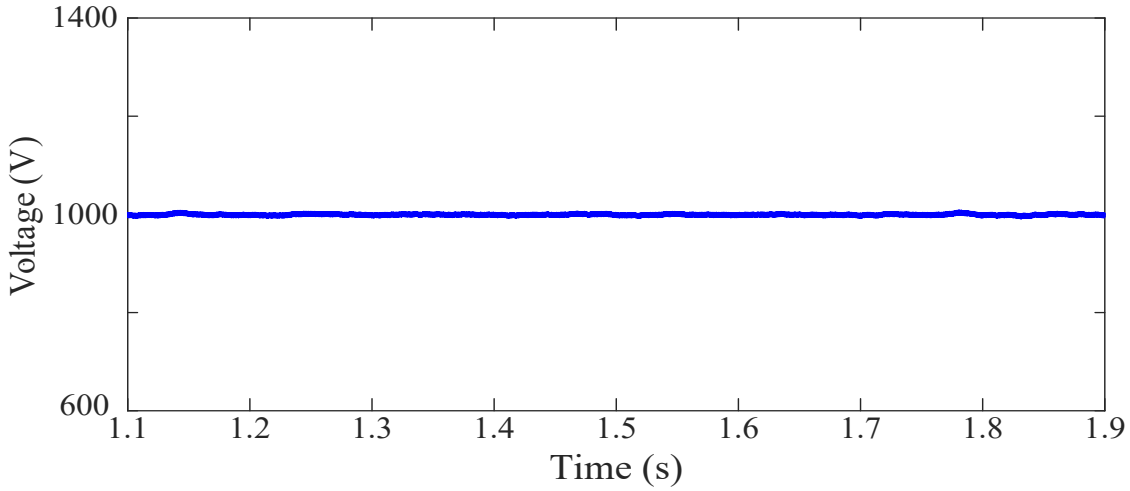
1. The behavior of the MMC-based SST can be quickly deduced from the results presented above: SST allows power flow reversal while maintaining voltages at each side to their values; unbalanced and/or non-sinusoidal currents at any SST side are not propagated to the other side; a close-to-unity power factor is maintained at the input terminals, while both active and reactive powers are measured at the LV terminals depending of the secondary side load.
2. The simulation results presented above show the SST behavior seen from both MV- and LV-side terminals. However, it is also important to analyze the response of the converter models, mainly those selected for representing the MV input stage. Figures 4.7 through 4.10 show the transient response of the voltages in MV- and LV-side dc links, as well as the transient voltage of an upper arm SM capacitance, corresponding to some of the test cases analyzed in the previous subsection. A common pattern can be deduced from all these responses:
   - DC link voltages at both the MV- and the LV-sides exhibit a quick variation at the beginning and the end of the transient, but in both moments the voltages quickly recover their initial values.
   - The voltage variation peaks depend on the event being analyzed but also on the parameters selected for representing dc links and controllers at both SST sides. Obviously larger dc link capacitors will suffer lower voltage variations. In most cases presented in Figures 4.7 through 4.10, the voltage variations are within the 1% of the selected voltage for the MV-side dc link; however, the variations of the secondary side dc link voltage can reach about 20% of the reference voltage in case of short circuit at the LV terminals or power flow reversal (see Figures 4.9.c and 4.10.c).
   - The variations of the SM capacitance voltages are within a 5% margin in all cases. On the other hand, the differences between voltages of different SM capacitances or even different MMC legs are also very smalls (i.e. within a 2% margin).
3. An important aspect to be considered is the ride-through capabilities of the SST. Just consider the case presented in Figure 4.1, which presents the SST response in front of voltage sags at the primary side. The behavior of the SST in this case is optimum; the sag is not propagated to the secondary side whose load will not notice the event. However, it is important to take into account that there is a limit to the sag severity the SST can cope with and that limit depends on the parameters selected for the power converters and their controllers.
   In other words, the SST would not be able to survive if the residual voltages at the three MV-side phase voltages were too low. A similar reasoning should be followed in case of short-circuit. If the short-circuit currents were not limited under certain value and the parameters of the secondary side converter were not adequately selected, the LV-side dc link would not be capable of recovering its voltage after a quick and deep discharge caused by a bold three-phase short circuit.



a) MV-side dc link voltage

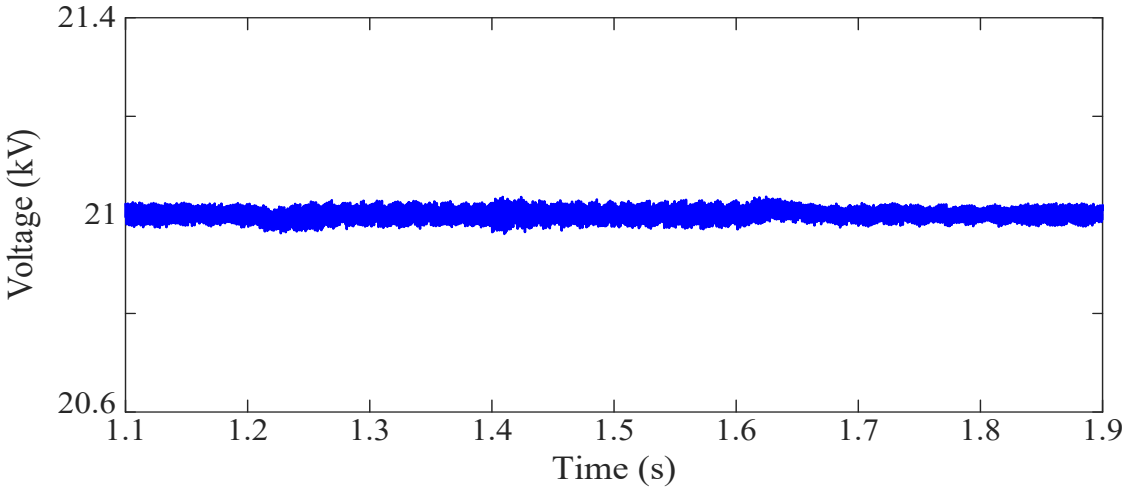


b) Capacitance voltage of upper arm of phase a

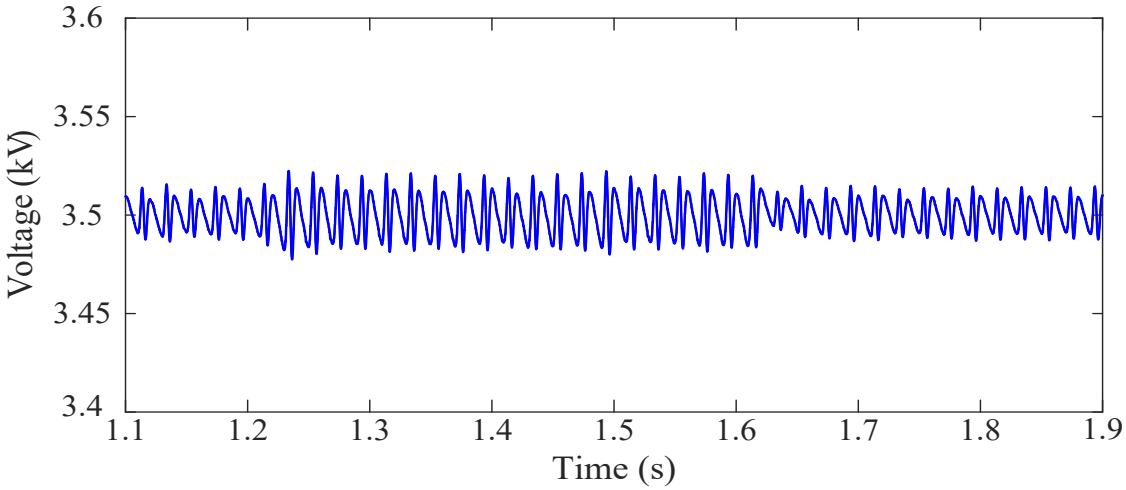


c) LV-side dc link voltage

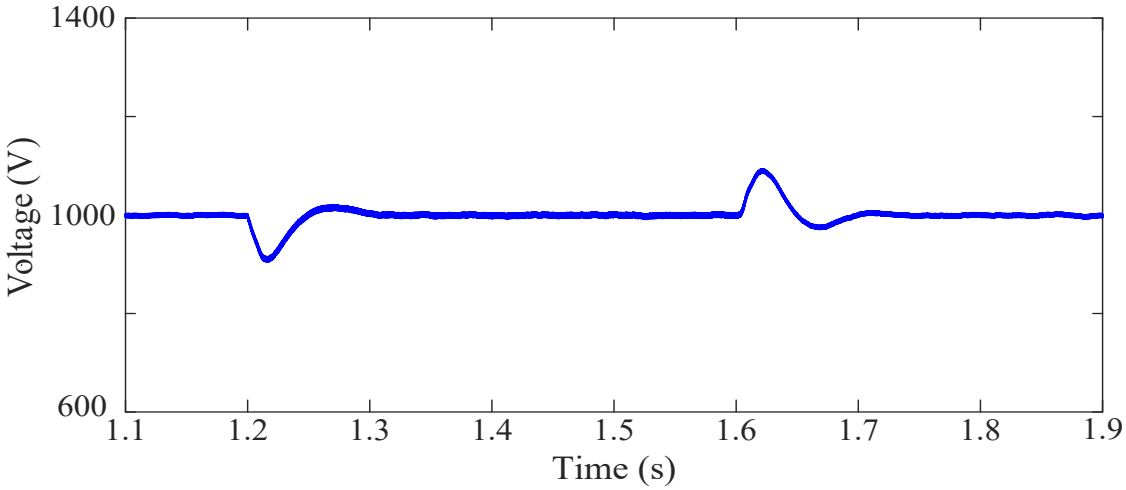
Figure 4.7. Simulation results: Voltage sag at the MV side.



a) MV-side dc link voltage

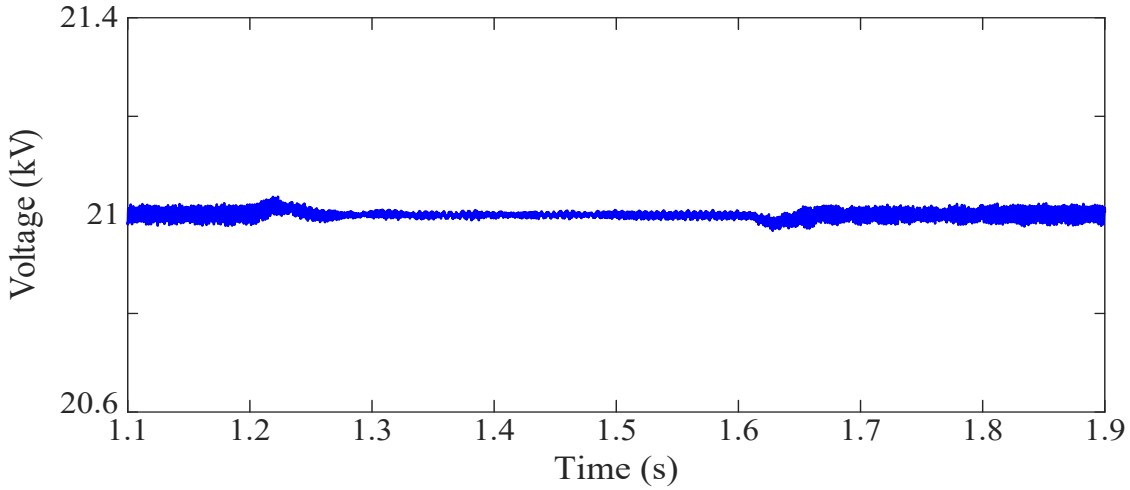


b) Capacitance voltage of upper arm of phase a

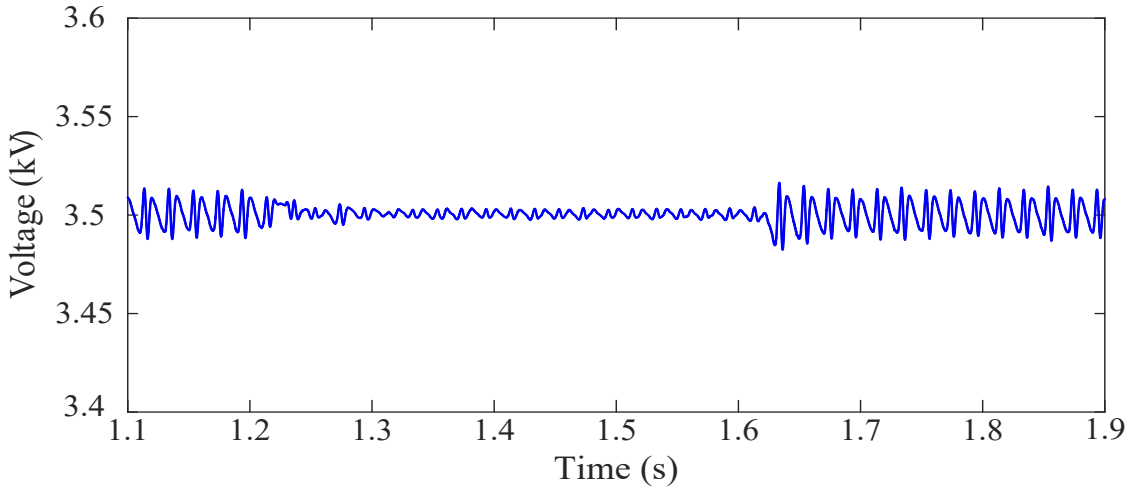


c) LV-side dc link voltage

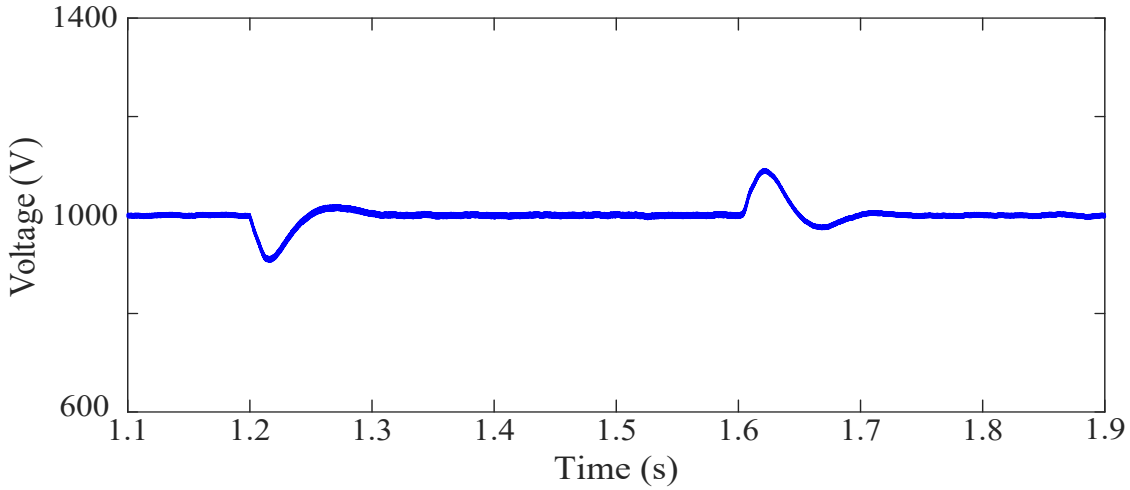
Figure 4.8. Simulation results: LV-side load variation.



a) MV-side dc link voltage

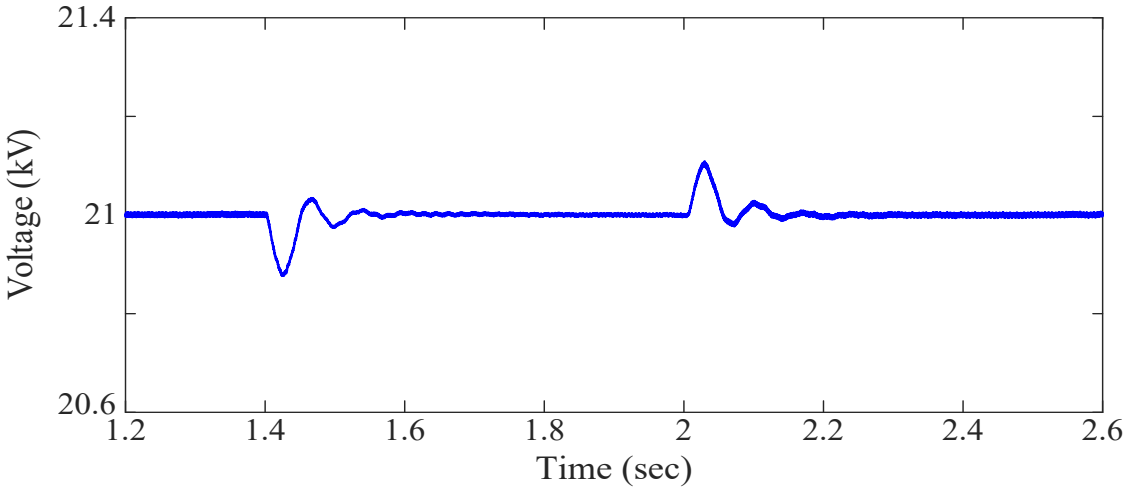


b) Capacitance voltage of positive arm of phase a

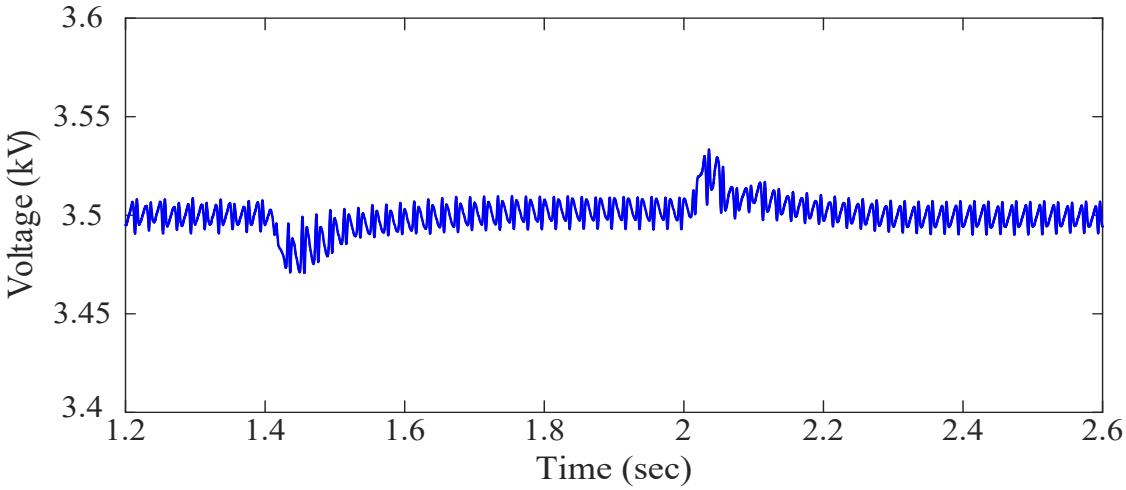


c) LV-side dc link voltage

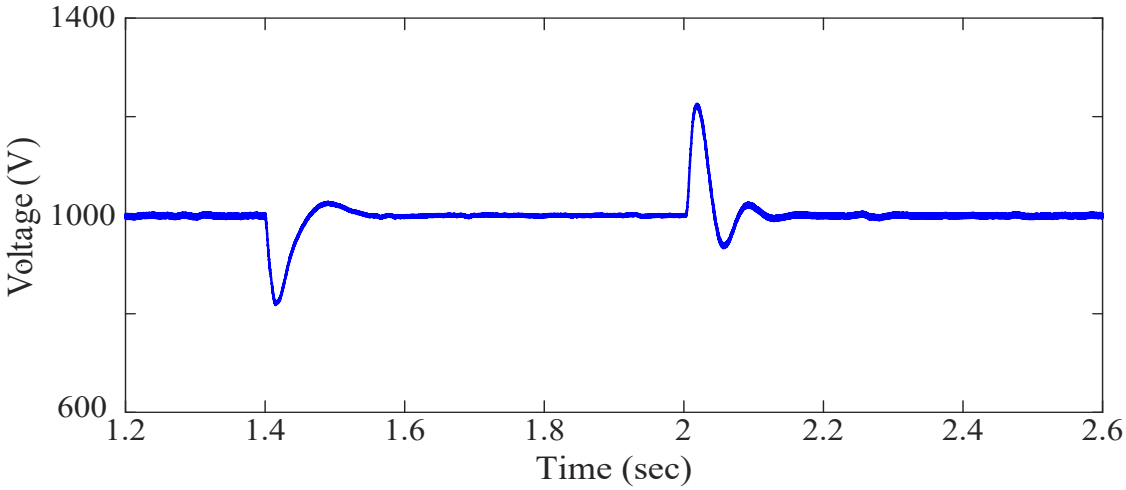
Figure 4.9. Simulation results: Short-circuit at the LV side.



a) MV-side dc link voltage



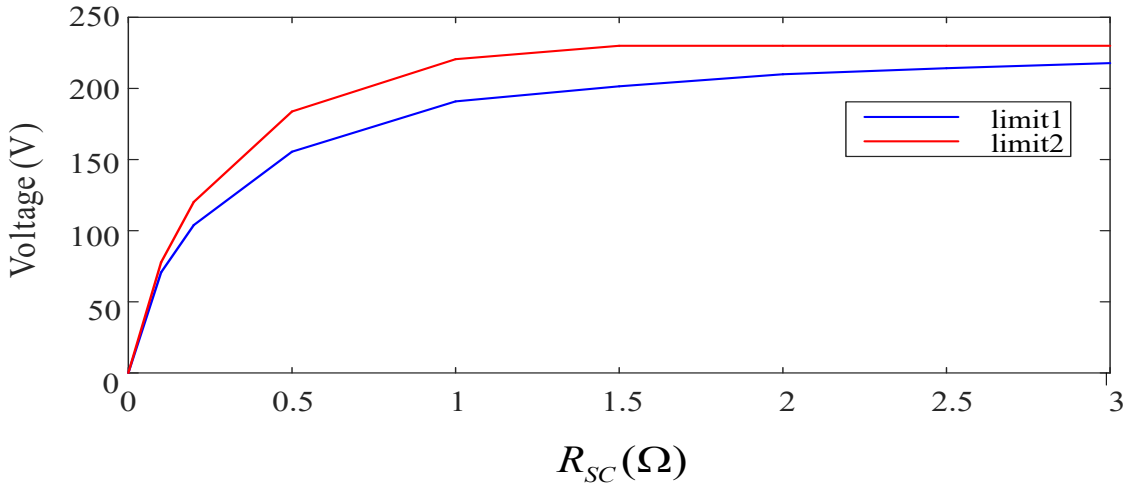
b) Capacitance voltage of positive arm of phase a



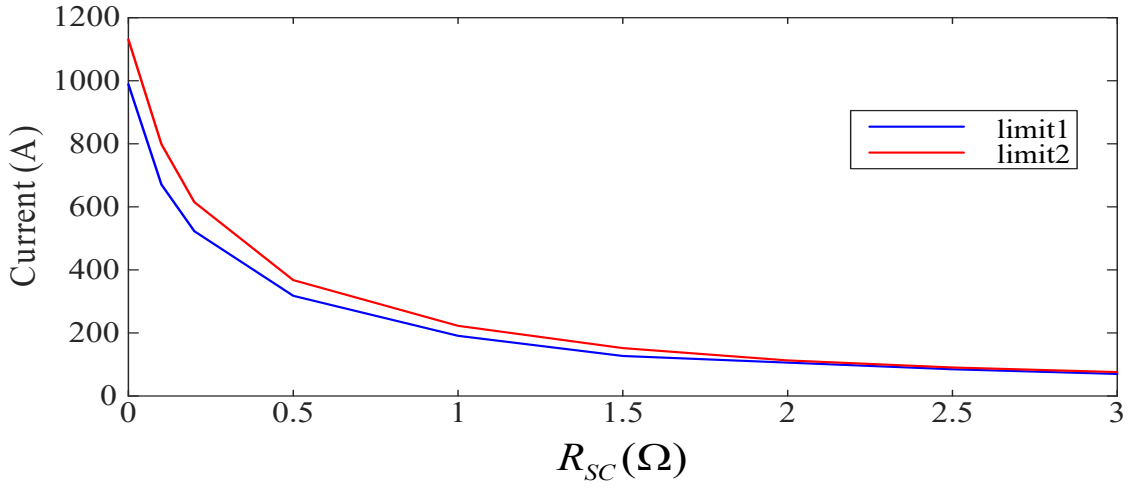
c) LV-side dc link voltage

Figure 4.10. Simulation results: Power flow reversal.

4. *Sensitivity analysis for short circuit*: In this section the aim is to study the different factors that can have an impact on performance of SST when short circuit occurs at low voltage terminal of SST. Three important factors regarding to this issue are: fault resistance (R_{sc}), the upper and lower limit of short circuit current limiter, and the control parameters. The control coefficients in outer voltage controllers and inner current controllers are tuned in order to provide desired reference signals for modulation technique (3D-SVM). The effects of R_{sc} and upper/lower limit value are going to be discussed below. It should be noted that the test system is a 500 kW SST. The load voltage (rms value) and fault current (rms value) are shown in Figure 4.11. The diagram is achieved through selecting nine different values from 0 to 3 (0, 0.1, 0.2, 0.5, 1, 1.5, 2, 2.5, 3) for fault resistance (R_{sc}) and two different values for upper and lower limit of short circuit current limiter. Limit 1 has smaller value than limit 2 (limit 1=1500 A, limit 2=1800 A). As it can be observed from Figure 4.11, the load voltage and fault current are increased and decreased respectively, by increasing R_{sc}.



a) Load voltage



b) Fault current

Figure 4.11. Simulation results: short circuit at the secondary side.

4.3. Simulation Results with Semiconductor Losses

4.3.1. SST model

The performance of the lossy SST model has been evaluated as a part of a MV distribution system. The model of the SST with semiconductor losses has been implemented in Matlab/Simulink assuming the parameters listed in Table 4.2.

Table 4.2. Second case study - SST parameters

Parameters	Values
SST rated power	500 kVA
Line-to-line grid voltage (rms)	12 kV
SST input stage filter resistance (R_1)	0.1 Ω
SST input stage filter inductance (L_1)	10 mH
Number of SMs per MMC arm	6
SM capacitance in MMC1&MMC2	0.4 mF
Arm resistance of MMC1	0.2 Ω
Arm inductance of MMC1	5 mH
MMC1 switching frequency	2 kHz
MV-side dc link capacitance	1 mF
Arm resistance of MMC2	0.01
Arm inductance of MMC2	0.3 mH
MV MMC2 and LV full bridge converter switching frequency	10 kHz
Transformer operating frequency	1 kHz
Transformer short-circuit resistance	0.001 Ω
Transformer leakage inductance	0.03 mH
LV-side dc link capacitance	8 mF
LV-side converter switching frequency	3 kHz
Load-side filter resistance (R_2)	0.001 Ω
Load-side filter inductance (L_2)	0.3 mH
Load-side filter capacitance (C_2)	800 μF
Neutral resistance (R_{n2})	0.001 Ω
Neutral inductance (L_{n2})	0.1 mH

In additional to the test of the performance of the SST model as part of the distribution system, this section includes some additional studies aimed at estimating the performance of the lossy model. The goal of the first study is to estimate the efficiency of a SST model in which semiconductor losses are accounted for. The second study analyzes the thermal behavior of the SST model.

4.3.2. SST Efficiency

A 500 kVA SST model with semiconductor losses has been studied to estimate its efficiency. The study has been carried by selecting five different values (i.e. 100, 200, 300, 400, and 500 kVA) for the apparent power of load and eight different values (i.e. 0.1, 0.2, 0.4, 0.6, 0.7, 0.8, 0.9 and 1) for the load power factor. Figure 4.12 shows the efficiency curves for SST.

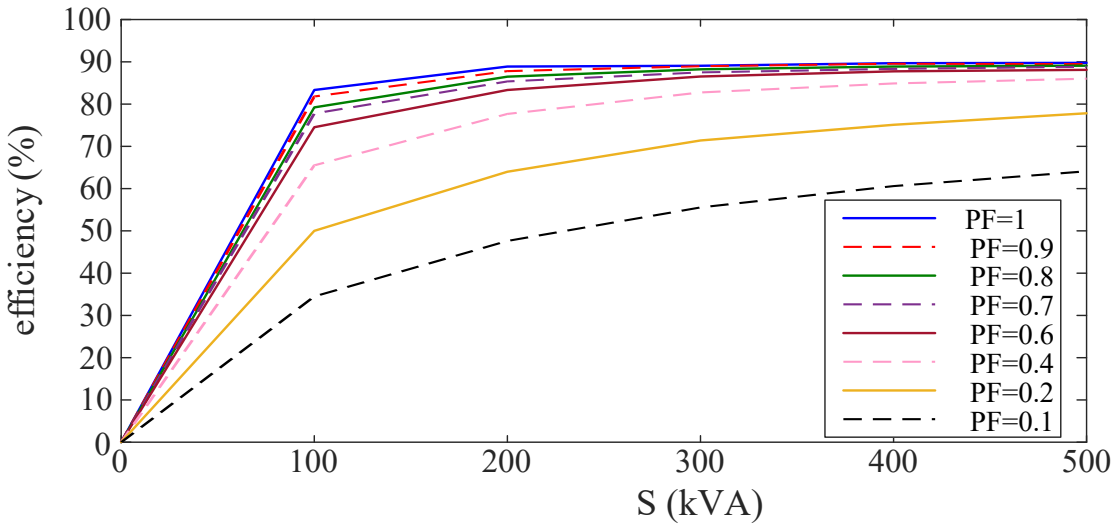


Figure 4.12. SST efficiency curves.

4.3.3. Analysis of the thermal behavior

Figure 4.13 shows the junction temperature values for the IGBT and diode of one phase (S_1 and D_1 in Figure 2.10) of the LV stage using the thermal model detailed in previous chapters. Figure 4.14 shows the junction temperature for the IGBT and diode (S_{1r} and D_{1r} in Figure 2.8) for the full-bridge rectifier of the isolation stage.

It should be noted that the results were obtained by assuming a common heat sink for each converter (see Figure 2.20); that is, up to 16 semiconductors (8 IGBTs and 8 antiparallel diodes) are mounted on one heat sink for the LV stage converter, and 8 semiconductors (4 IGBTs and 4 antiparallel diodes) are mounted on another common heat sink; see Figures 2.8 and 2.10. The thermal parameters that are needed for modeling the thermal behavior of SST in LV are given in table 2.6.

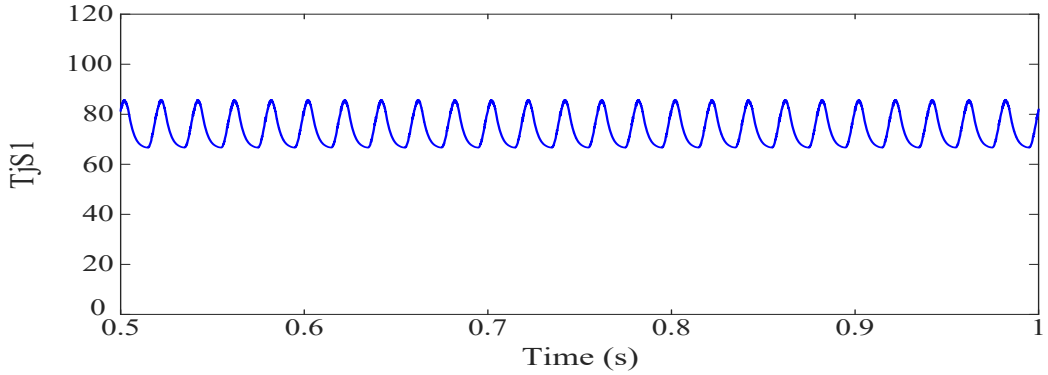
The values of resistances and capacitances selected for common heat sink thermal models are:

- Case to heat sink thermal resistance (R_c) 0.010 °C/W
- Heat sink to ambient thermal resistance (R_s) 0.010 °C/W
- Heat sink to ambient thermal capacitance (C_s) 0.250 J/°C.

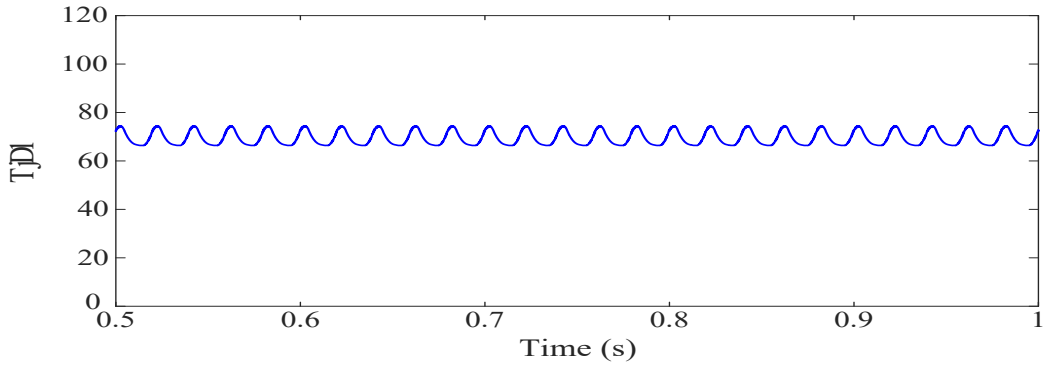
4.3.4. Test system and test cases

Figure 4.15 shows the configuration and parameters of the distribution test system analyzed in this section. Simulation results corresponding to operating conditions similar to those analyzed in the previous section with the lossless SST model are presented here. It should be noted that for theses case studies semiconductor losses has been included in semiconductor model.

Five test cases (cases 2 through 6) are basically those analyzed in the previous section, so no additional details are needed about them. The only case for which some introduction is required is the first one, in which the response of the SST in form of voltage sags and swells at the MV terminals is studied. Since the variations that MV input voltages can exhibit may lead to converter instability when connected to a weak grid, the MV-side PLL has been modified to account for large deviations of MV distribution system voltages [4.4].

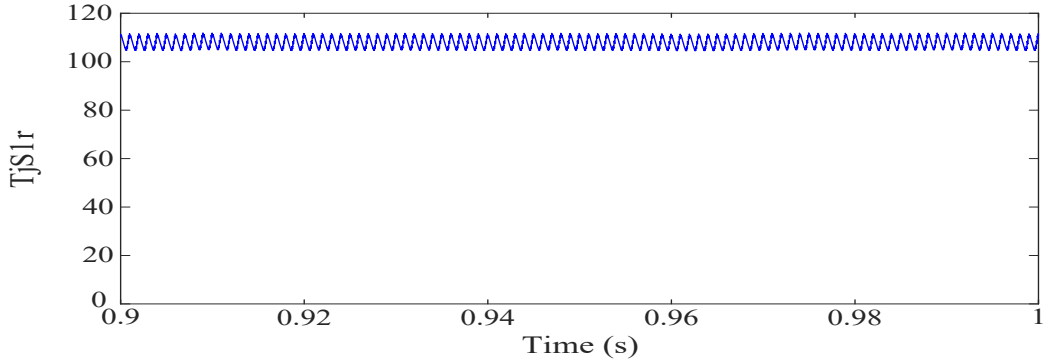


a) Junction temperature of IGBTs

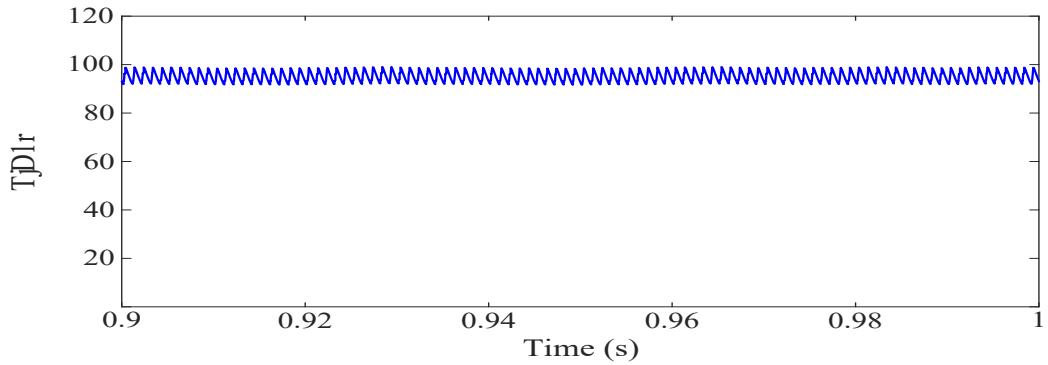


b) Junction temperature of diodes

Figure 4.13. Junction temperature of IGBTs and diodes - LV side converter – Phase a



a) Junction temperature of IGBTs



b) Junction temperature of diodes

Figure 4.14. Junction temperature of IGBT and diode of full bridge rectifier in isolation stage.

The PLL is used as a synchronization block that generates the reference angle used in controllers. PLL is going to have negative impact through increasing the real part of converter impedance and also increasing unwanted coupling to impedance of distribution grid [4.5]-[4.6]. The mentioned negative impacts of PLL are not paid attention too much when the converter is connected to stiff AC distribution grid (it means that grid with low impedance value), but in case that voltage source converters are connected to weak AC distribution grids (it means that the grids with high impedance values) it is becoming very important to avoid a distorted AC voltage at the point of common coupling (PCC).

PLL negative effect can be decreased through reduction of PI gains of PLL but it should be taken in to consideration that great reduction of gains is restricted by converter limitation performance [4.7]. In our work positive-sequence voltage at the input stage of SST is used to obtain the angle for synchronization purposes by means of a phase-locked loop (PLL). The undesirable problem of PLL negative effect has been modified through reduction of PI gains of PLL and tuning the dc voltage controller parameters as proposed in [4.8].

Assume that a two-phase-to-ground short circuit fault occurs between 1200 and 1600 ms in the distribution system (see fault location in Figure 4.15); this causes a voltage sag in two MV terminals and a voltage swell in one MV terminal of the SST. Simulation results depicted in Figure 4.16 confirm that under these conditions the currents at the primary side are balanced and the SST prevents the propagation of the voltage unbalance from the MV side to the LV side.

As it can be seen from the plots of Figures 4.16.d and 4.16.e, the voltage and current at the output stage of SST are completely balanced without being affected by the severe transient event that occurs at the MV terminals of the SST. This case illustrates the positive impact of the new PLL, which can avoid instabilities within the MV-side MMC and also the capability of three-stage SST in isolating input side from output stage through using isolation stage.

Figures 4.17 through 4.25 show the simulation results obtained with the other test cases.

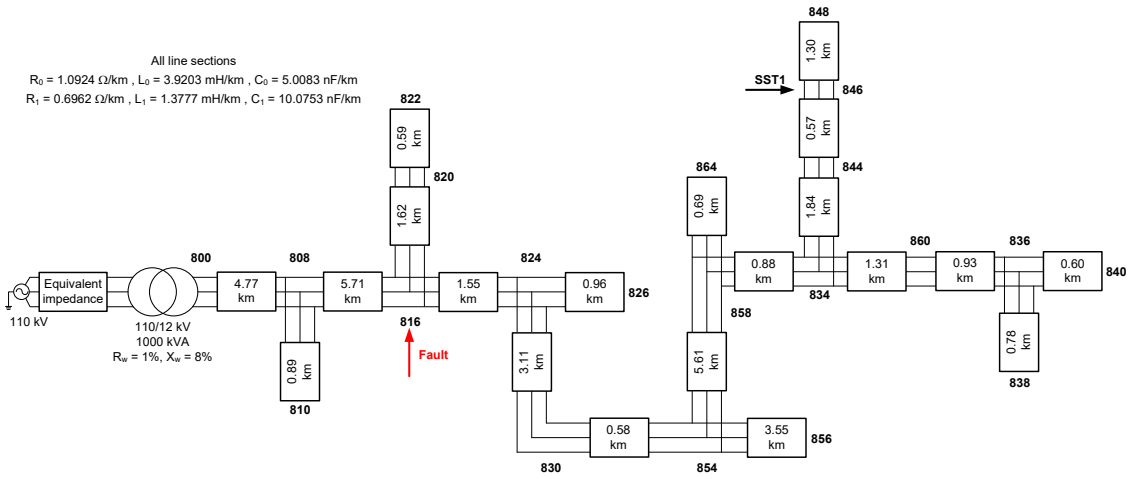
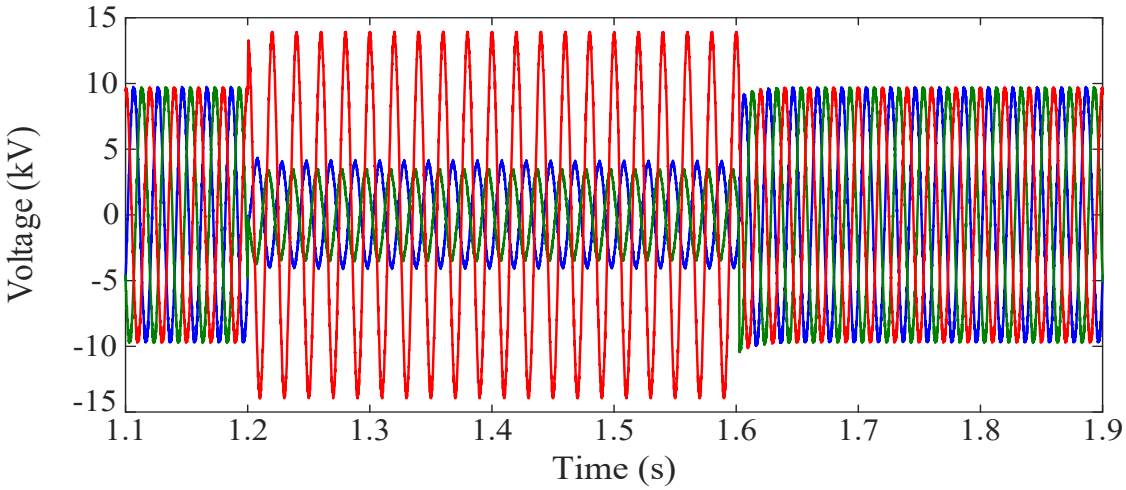
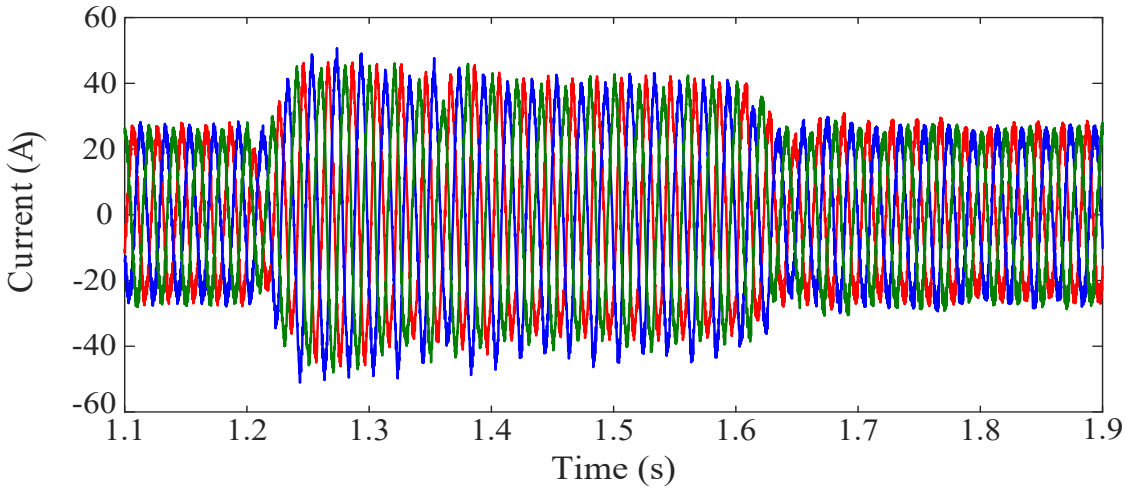


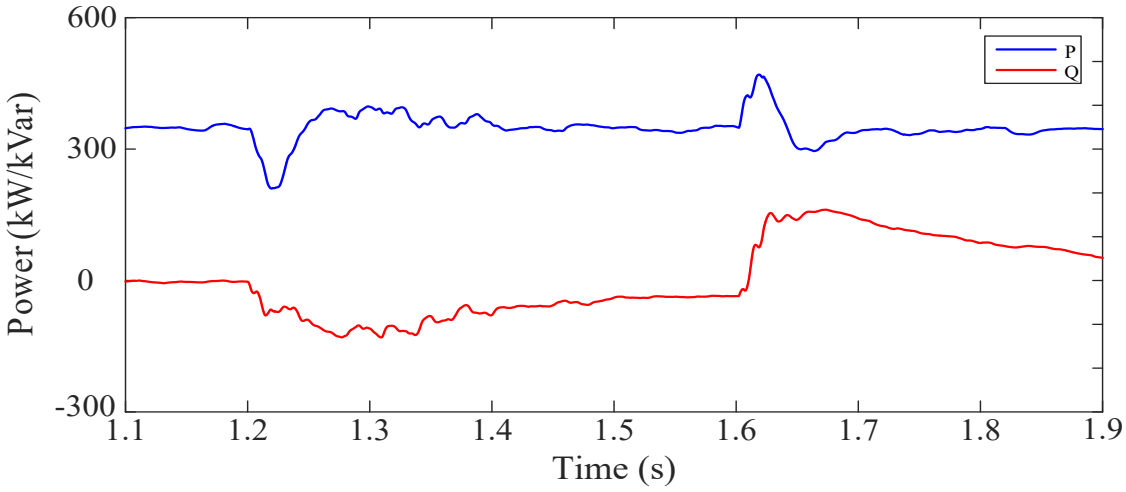
Figure 4.15. Test System 2 - Configuration of the distribution network.



a) Primary side voltages

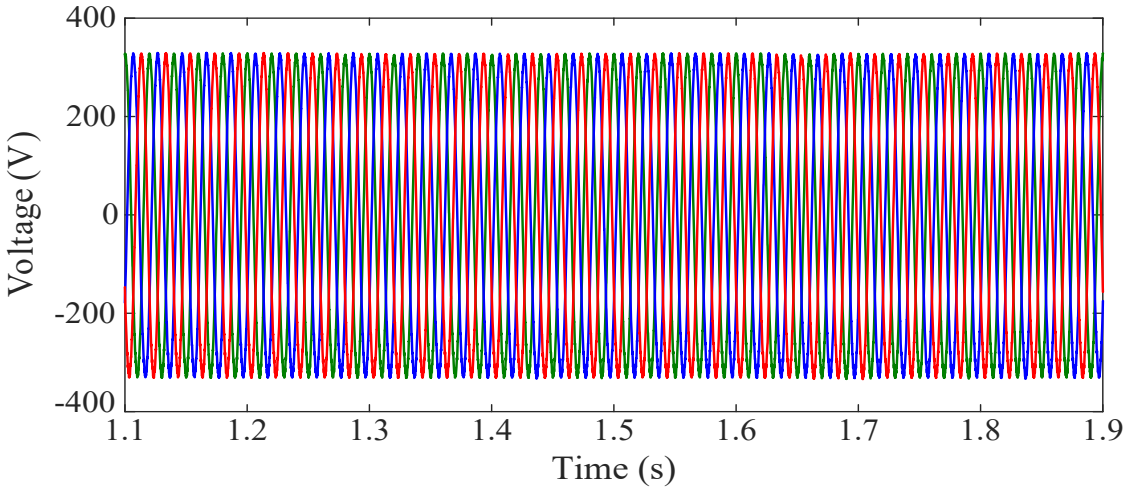


b) Primary side currents

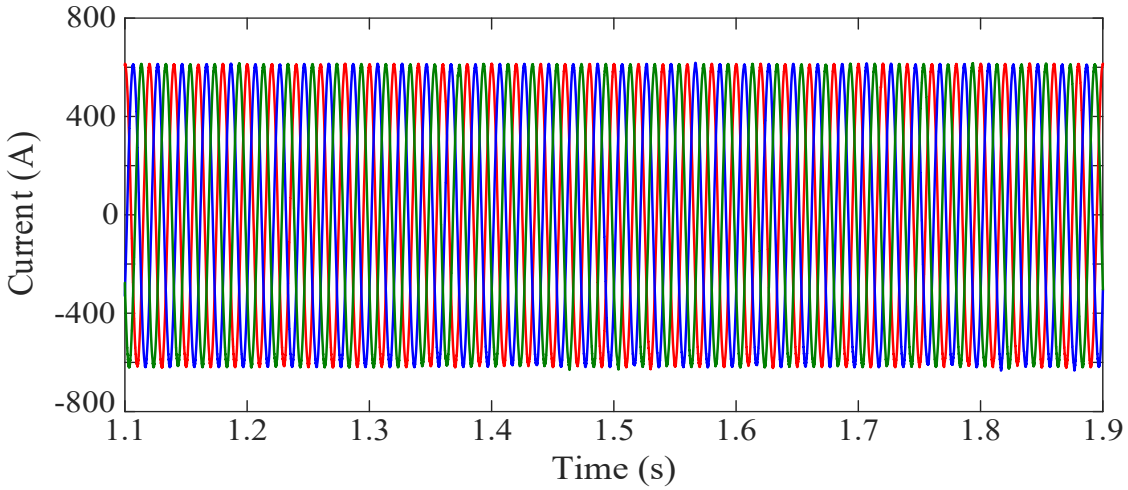


c) Primary side active and reactive powers

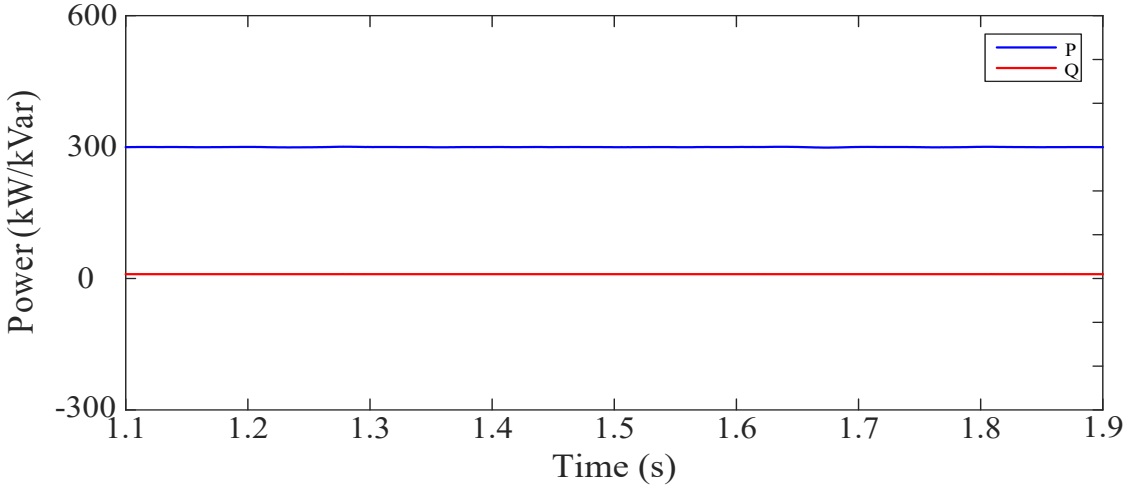
Figure 4.16. Test System 2 - Simulation results: Voltage sag at the MV side.



d) Secondary side voltages

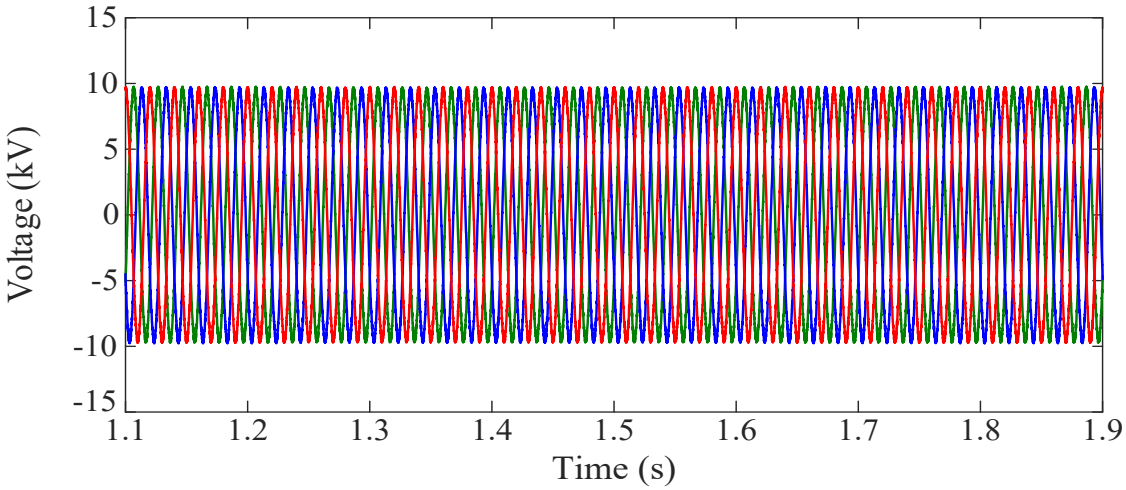


e) Secondary side currents

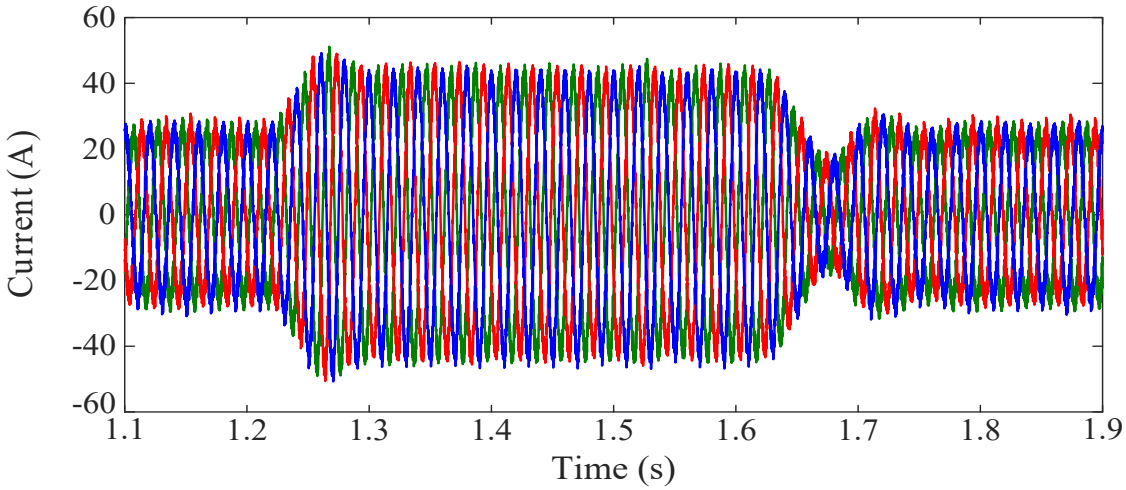


f) Secondary side active and reactive powers

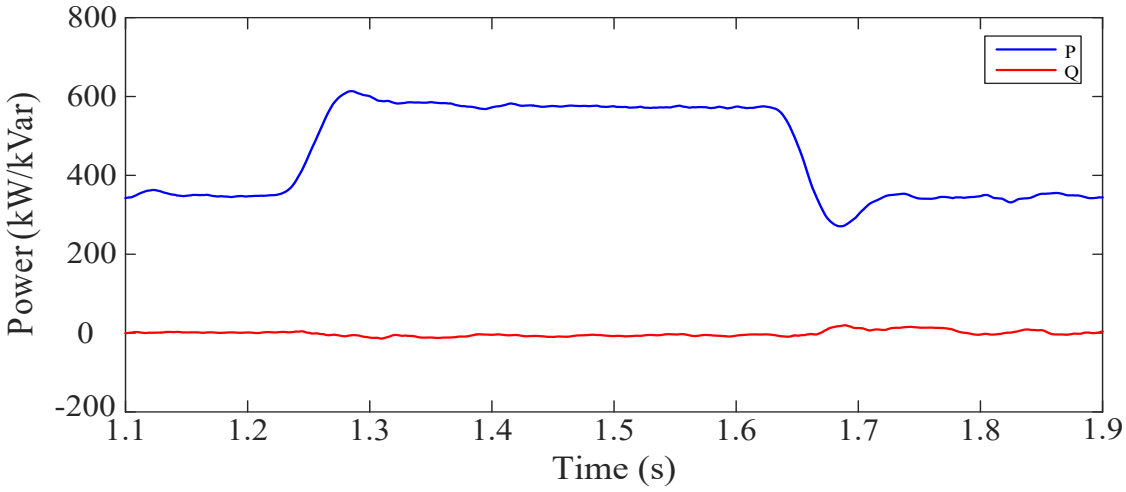
Figure 4.16. Test System 2 - Simulation results: Voltage sag at the MV side (cont.).



a) Primary side voltages

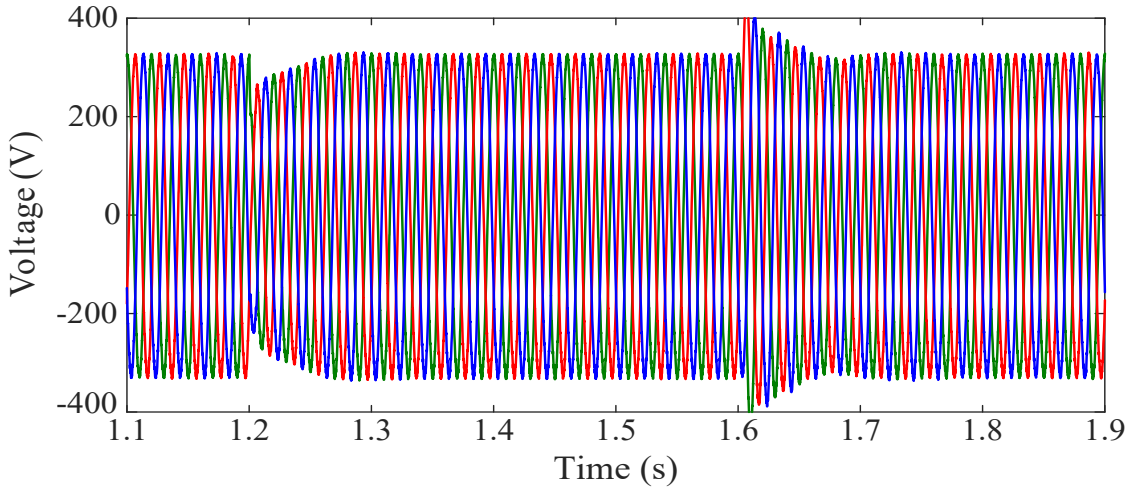


b) Primary side currents

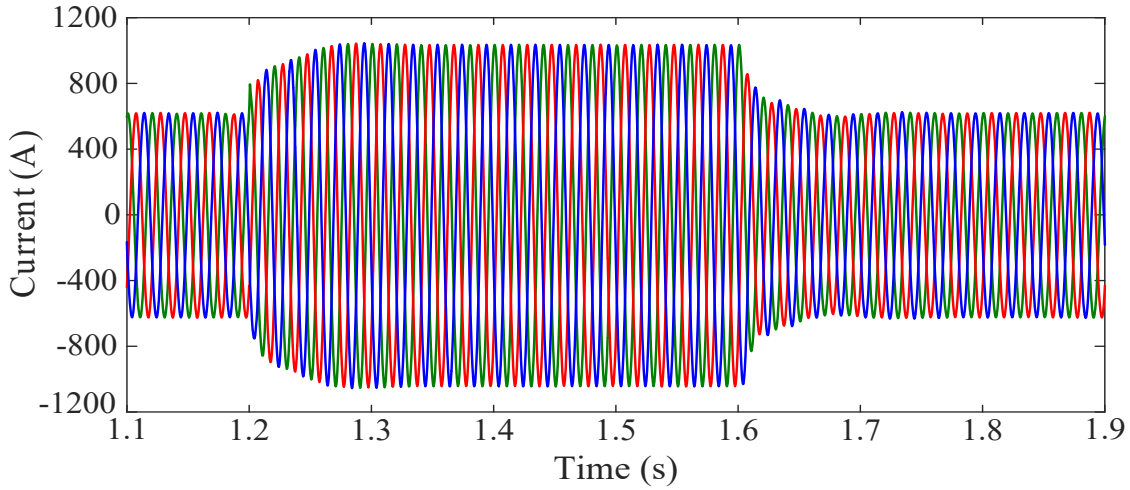


c) Primary side active and reactive powers

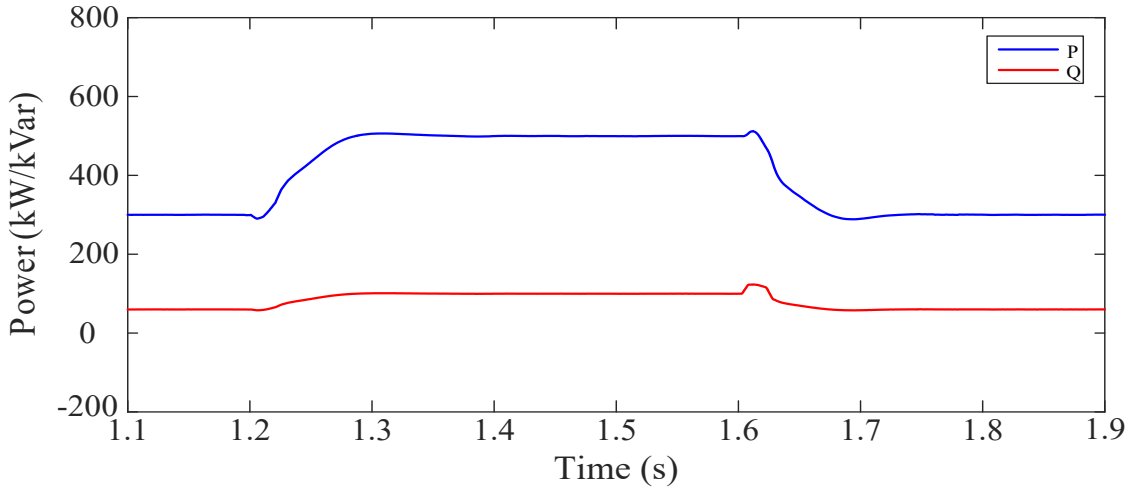
Figure 4.17. Test System 2 - Simulation results: LV-side load variation.



d) Secondary side voltages

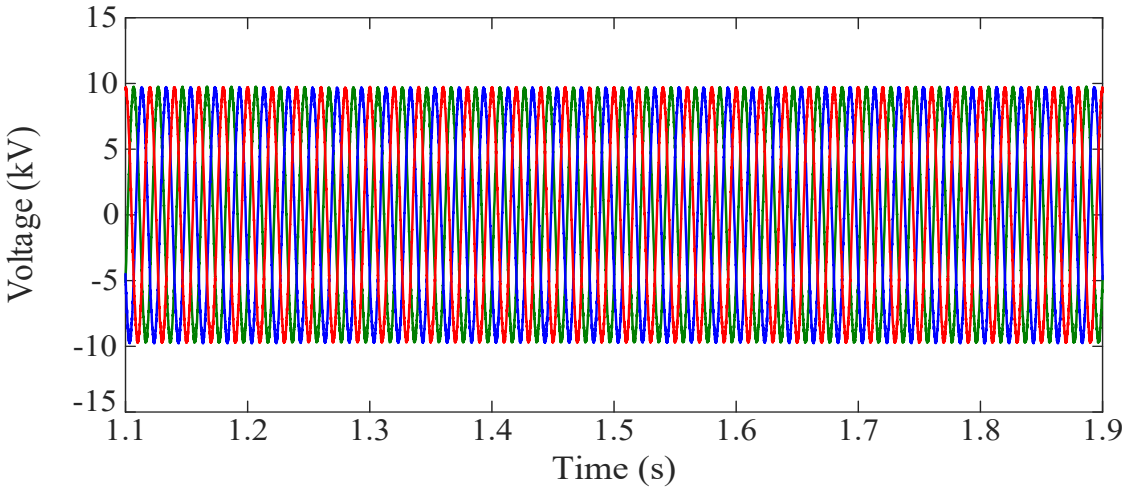


e) Secondary side currents

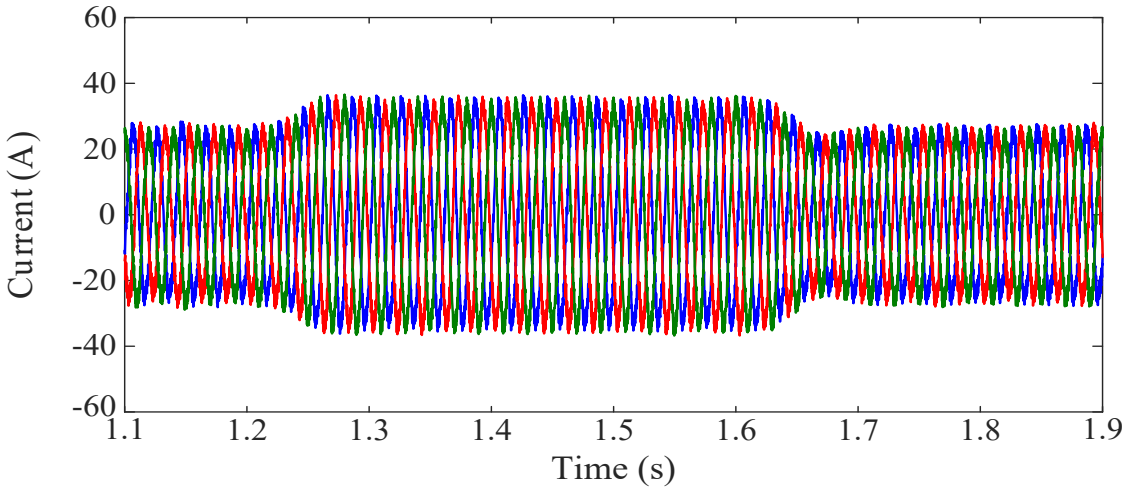


f) Secondary side active and reactive powers

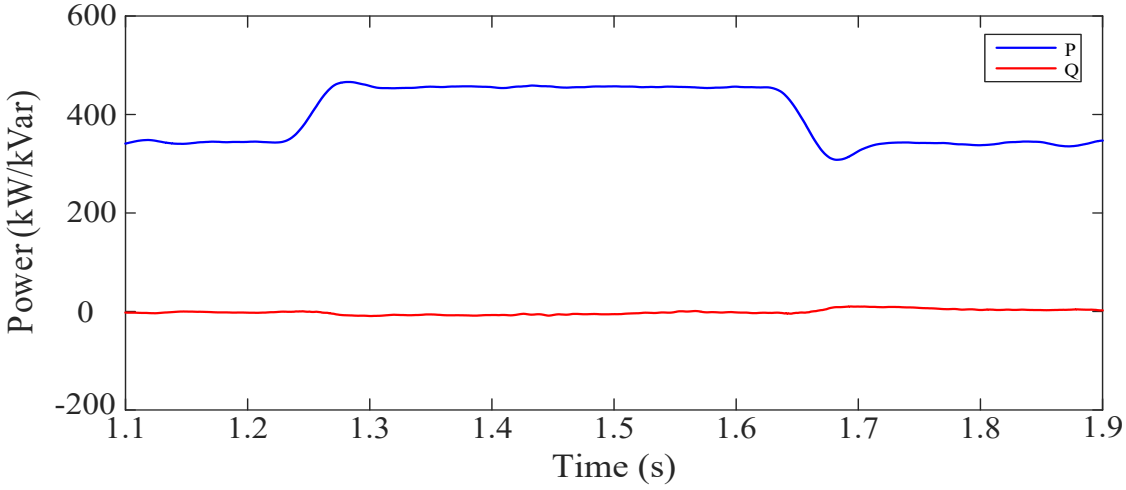
Figure 4.17. Test System 2 - Simulation results: LV-side load variation (cont.).



a) Primary side voltages

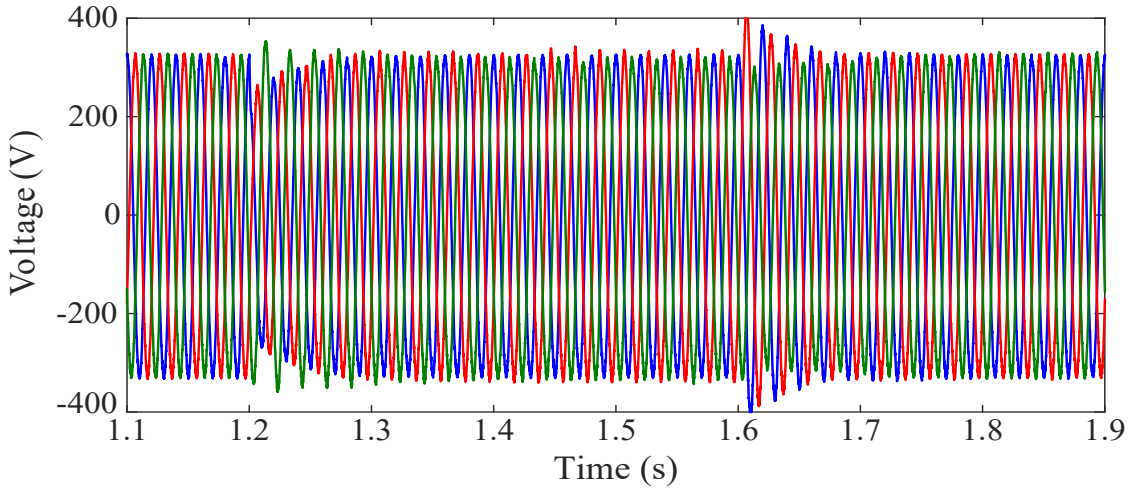


b) Primary side currents

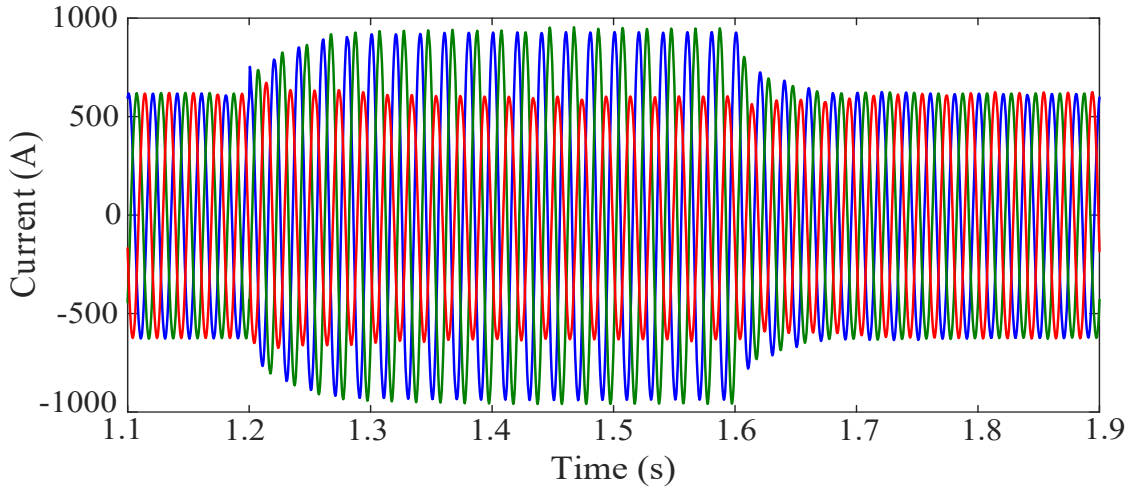


c) Primary side active and reactive powers

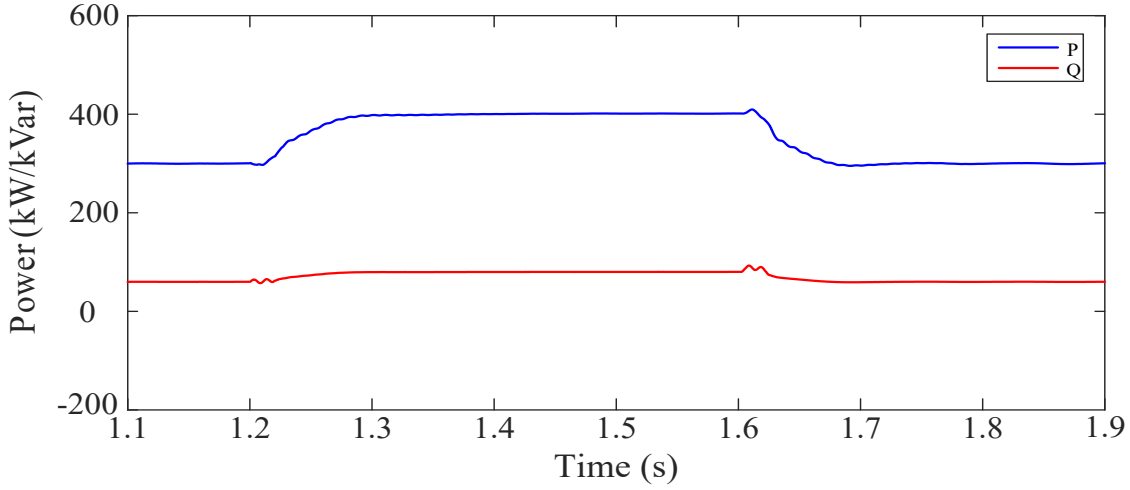
Figure 4.18. Test System 2 - Simulation results: Unbalanced LV-side load.



d) Secondary side voltages

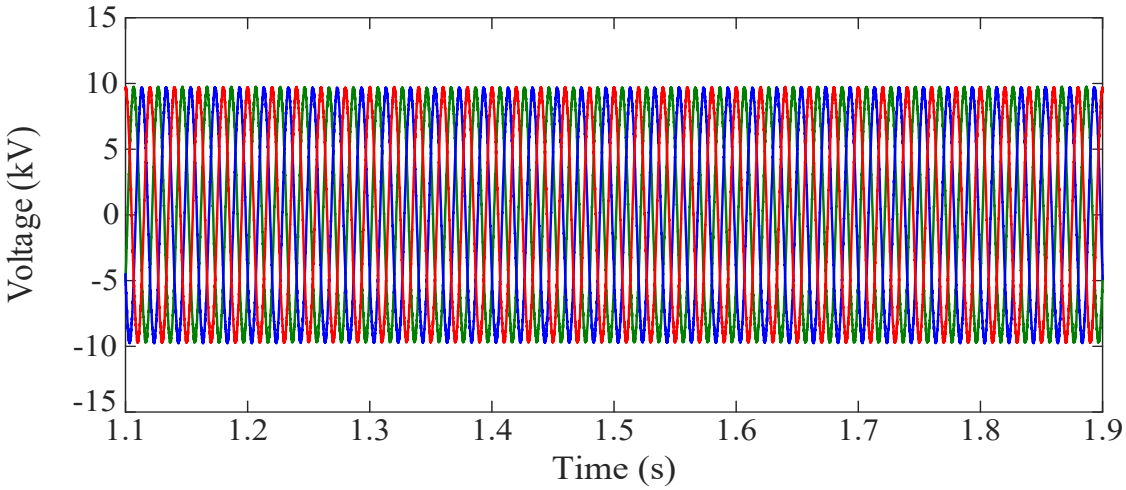


e) Secondary side currents

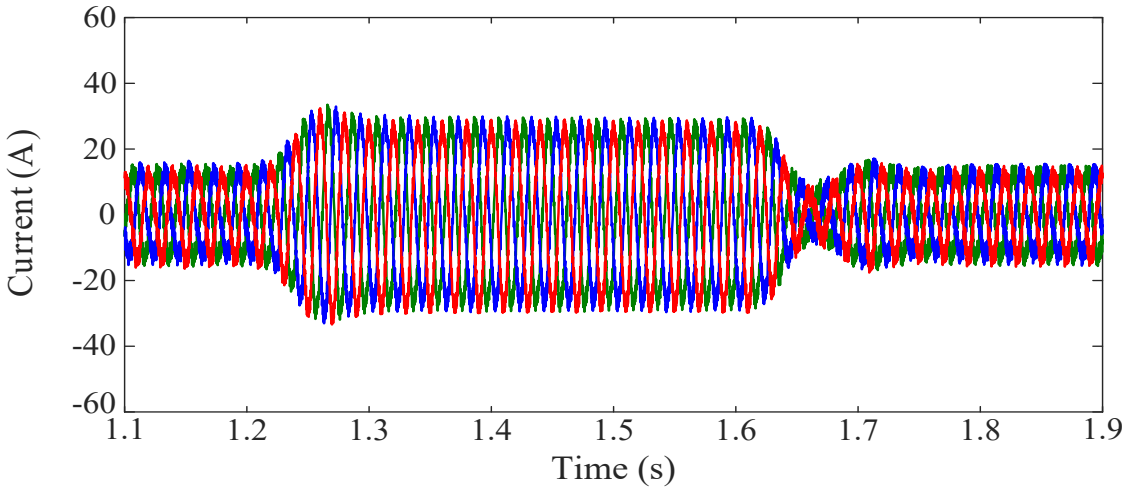


f) Secondary side active and reactive powers

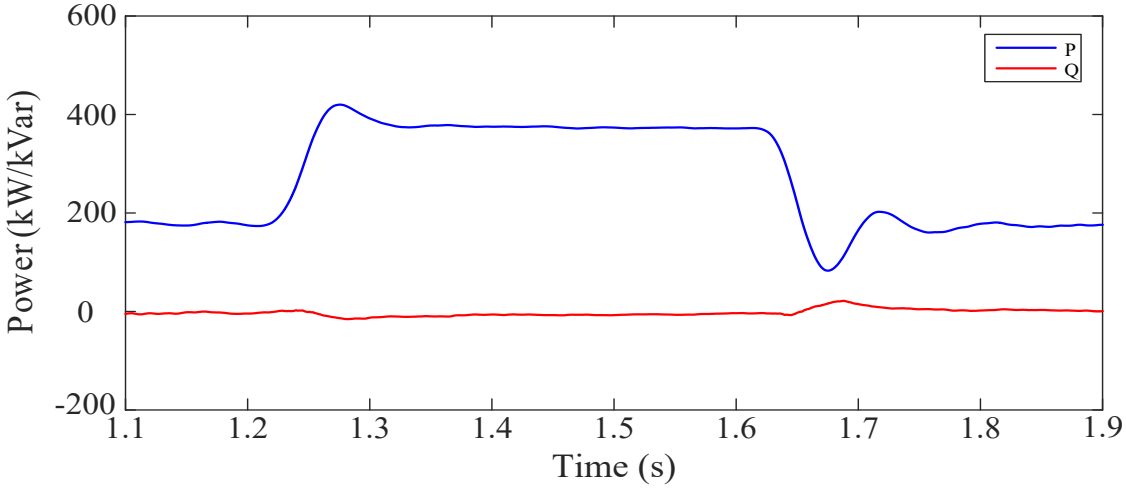
Figure 4.18. Test System 2 - Simulation results: Unbalanced LV-side load (cont.).



a) Primary side voltages

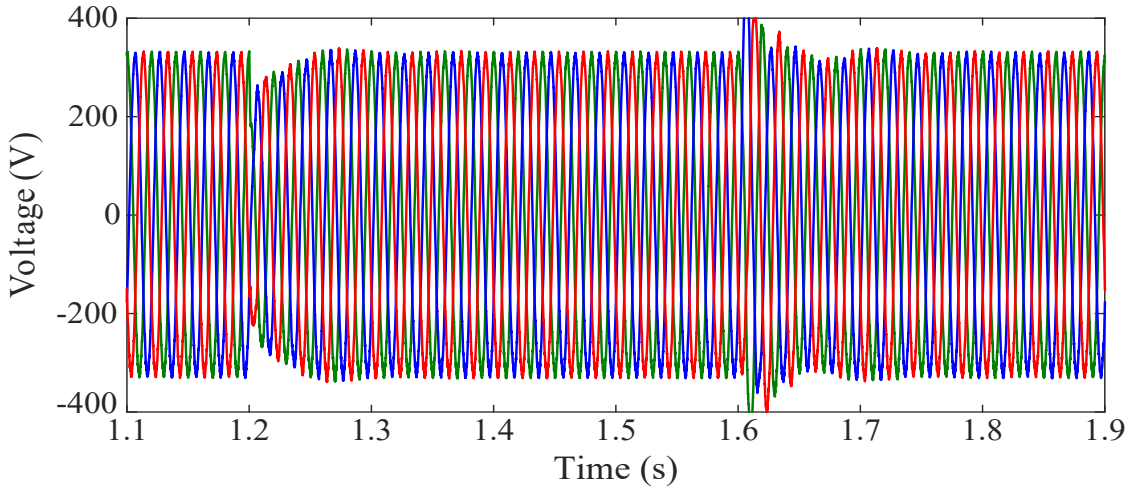


b) Primary side currents

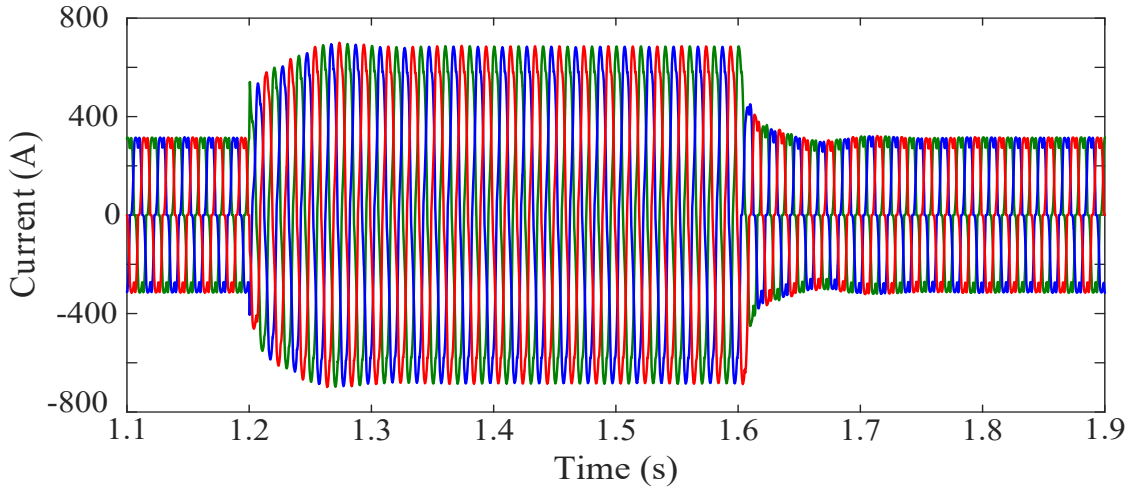


c) Primary side active and reactive powers

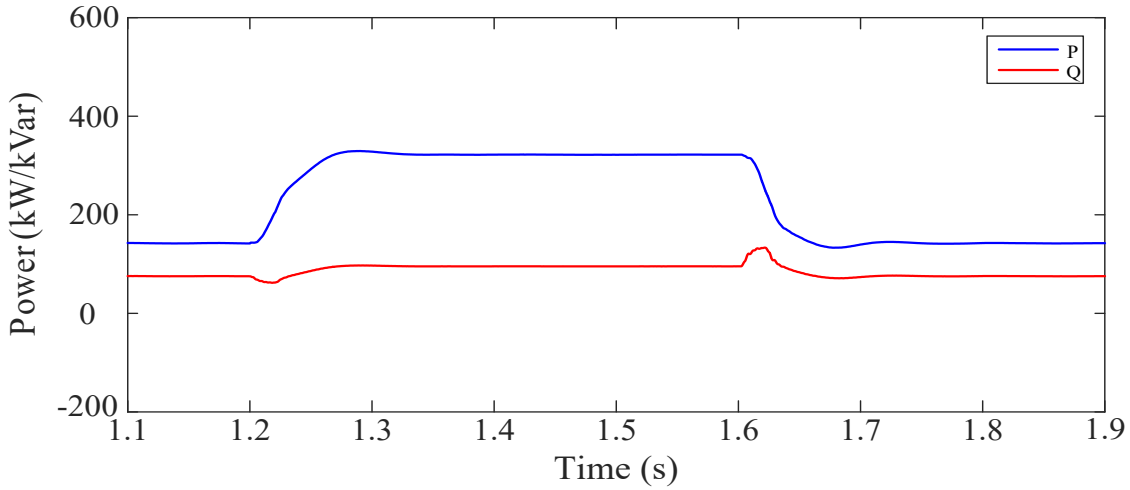
Figure 4.19. Test System 2 - Simulation results: Nonlinear LV-side load.



d) Secondary side voltages

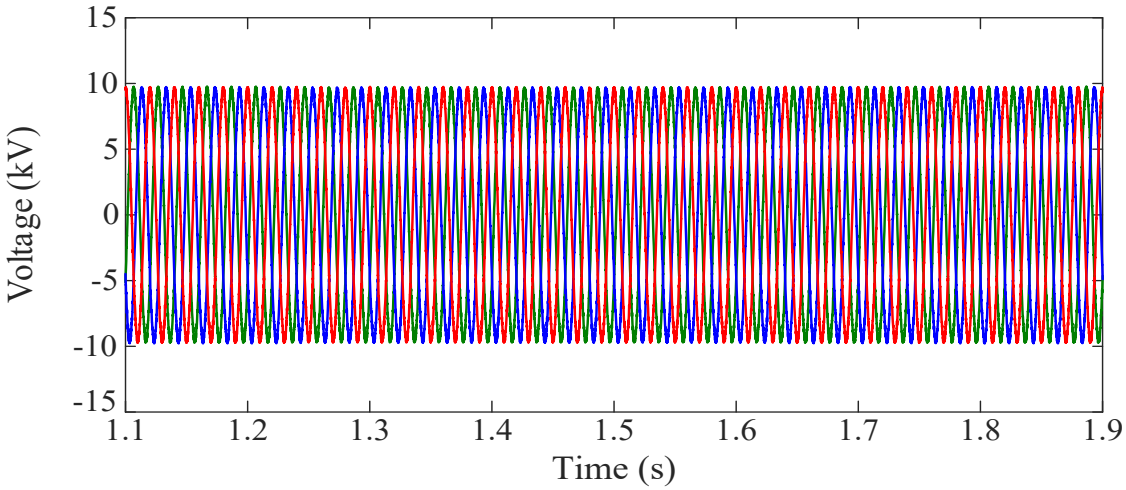


e) Secondary side currents

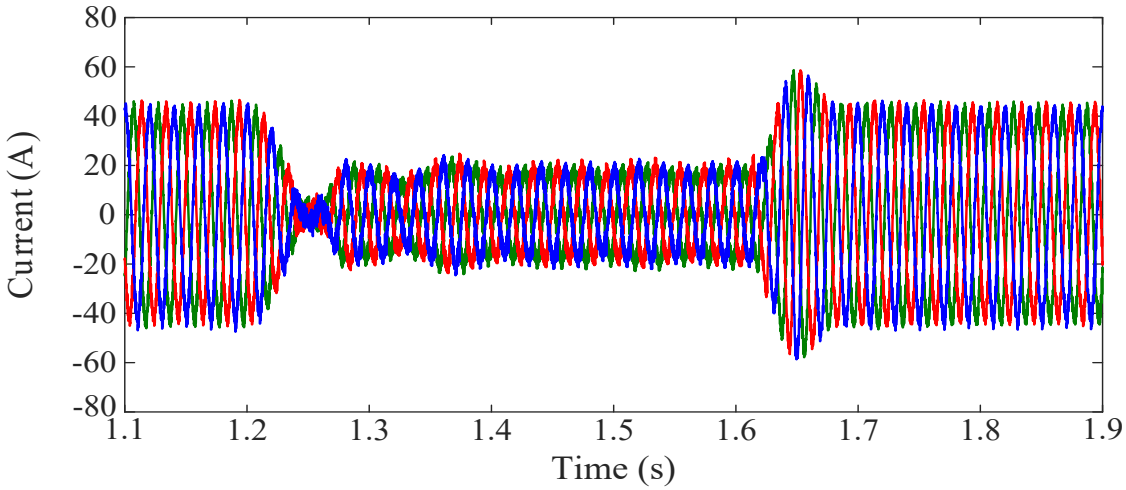


f) Secondary side active and reactive powers

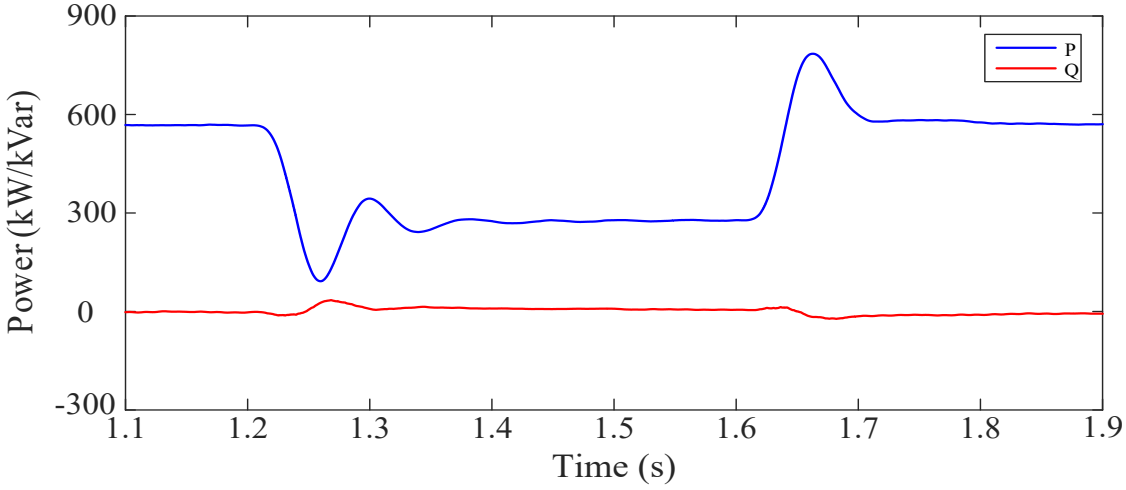
Figure 4.19. Test System 2 - Simulation results: Nonlinear LV-side load (cont.).



a) Primary side voltages

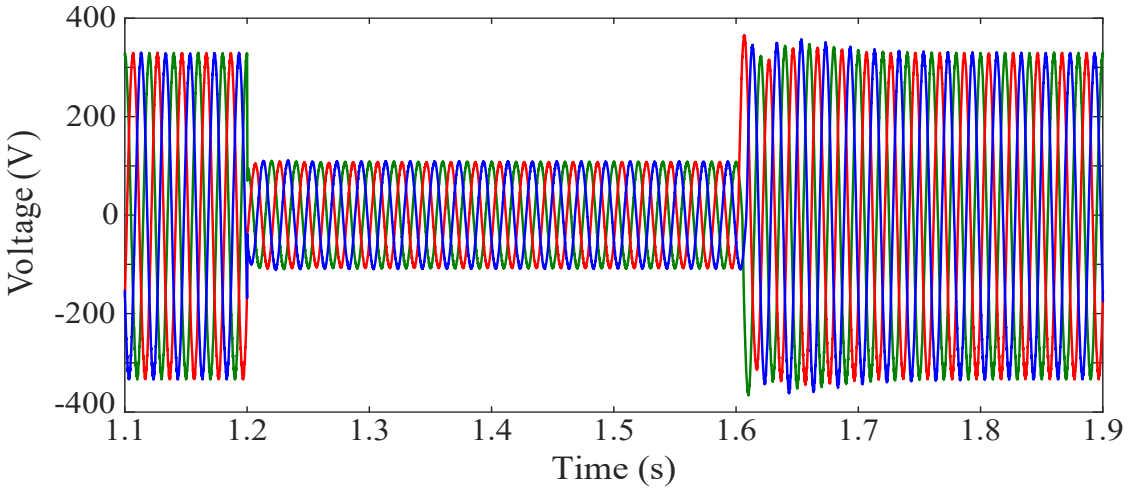


b) Primary side currents

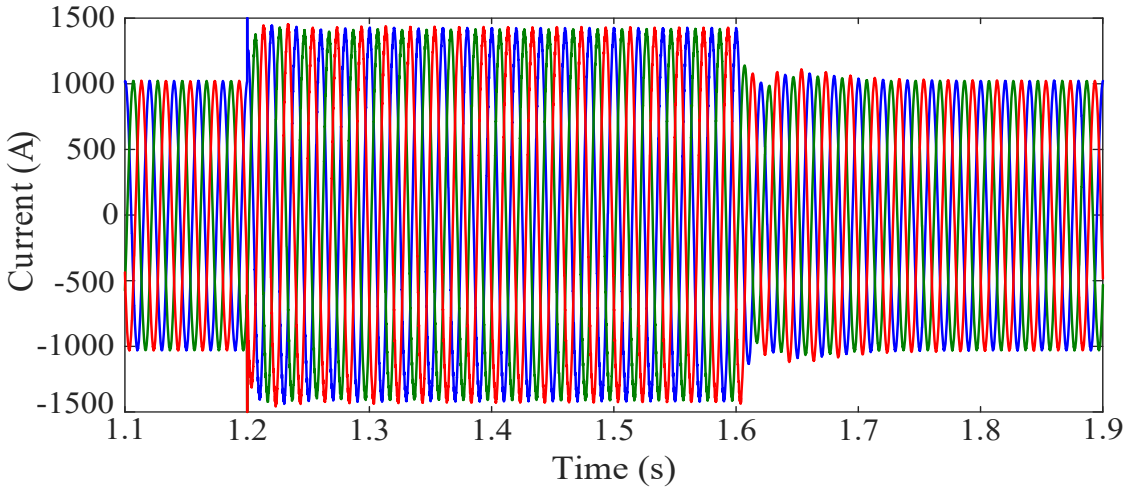


c) Primary side active and reactive powers

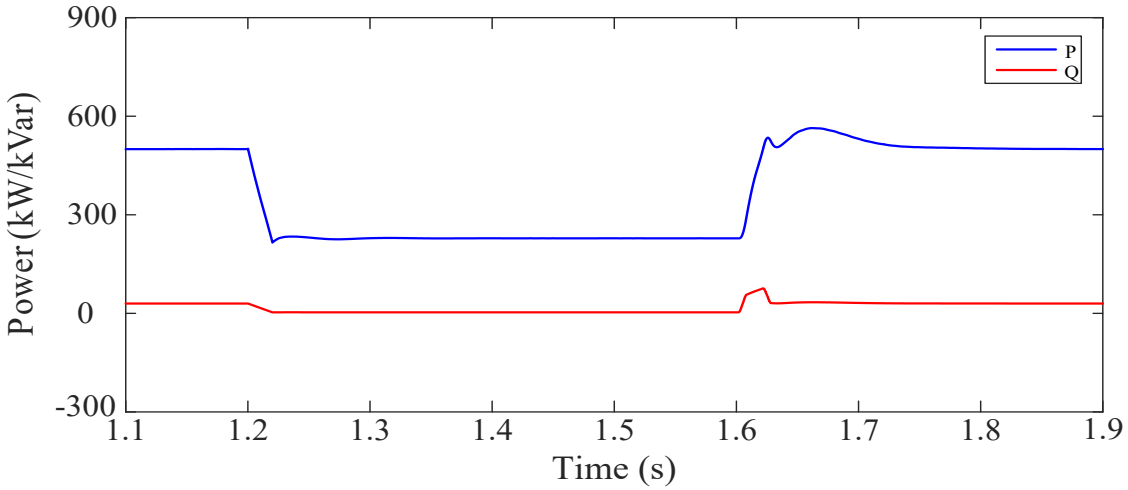
Figure 4.20. Test System 2 - Simulation results: Short-circuit at the LV terminals.



d) Secondary side voltages

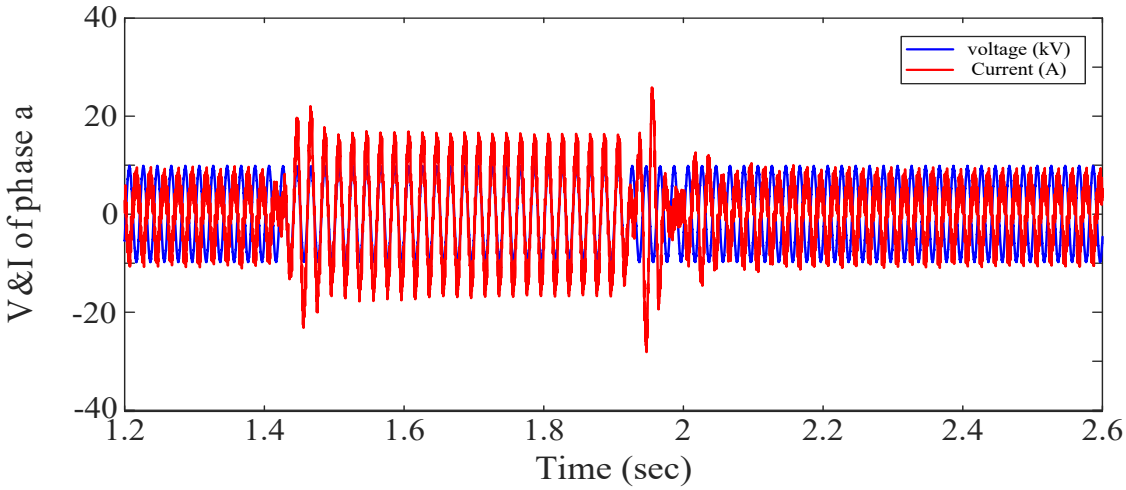


e) Secondary side currents

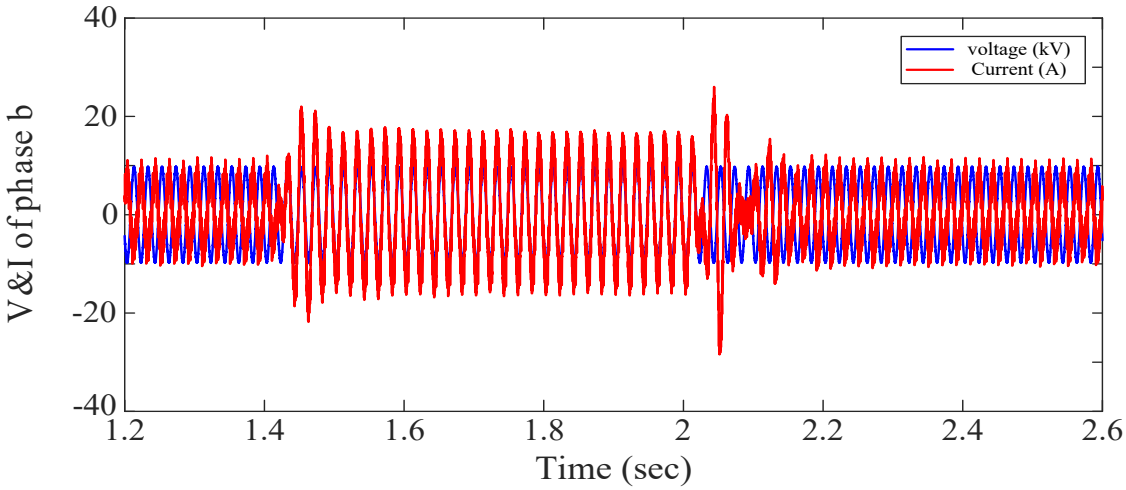


f) Secondary side active and reactive powers

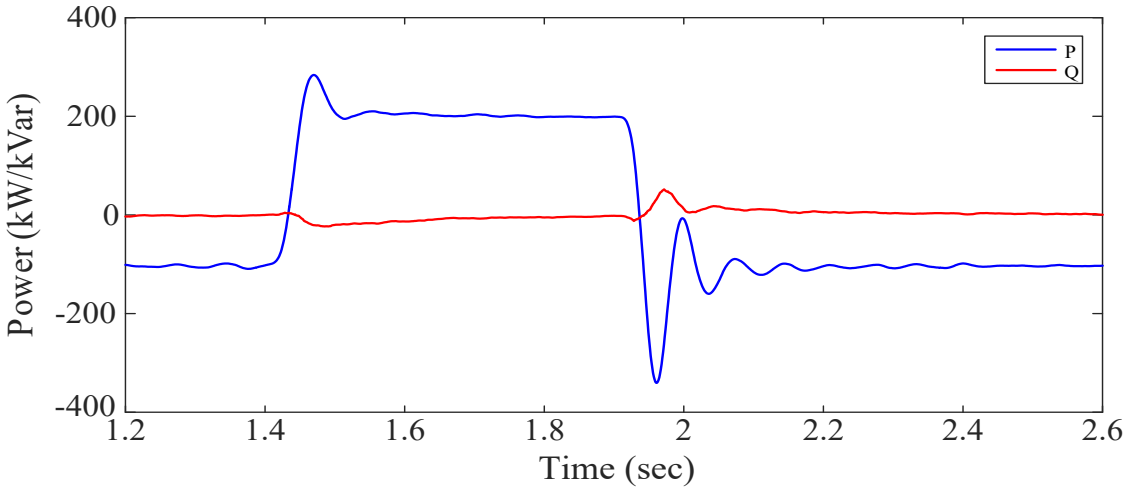
Figure 4.20. Test System 2 - Simulation results: Short-circuit at the LV terminals (cont.).



a) Primary side current and voltage - Phase A

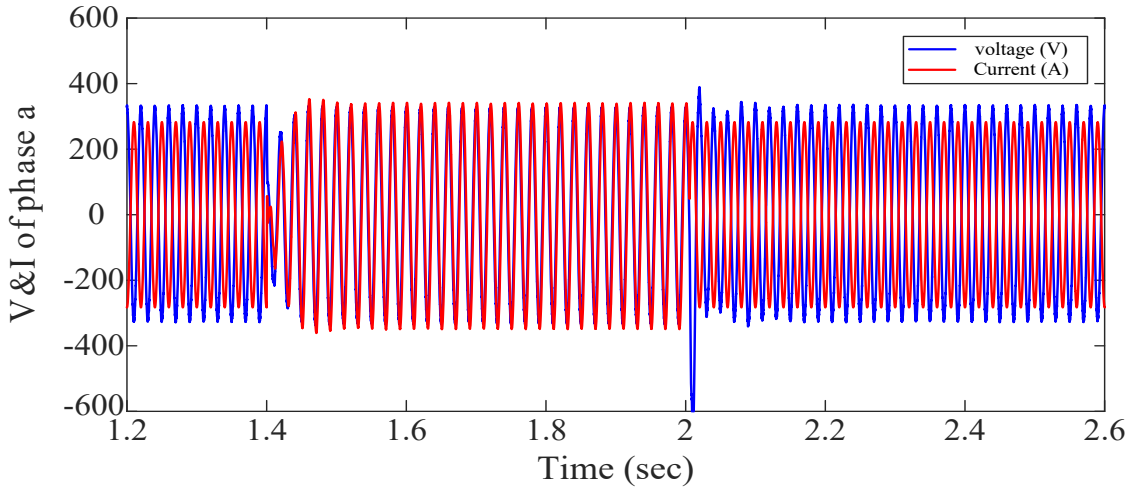


b) Primary side current and voltage - Phase B

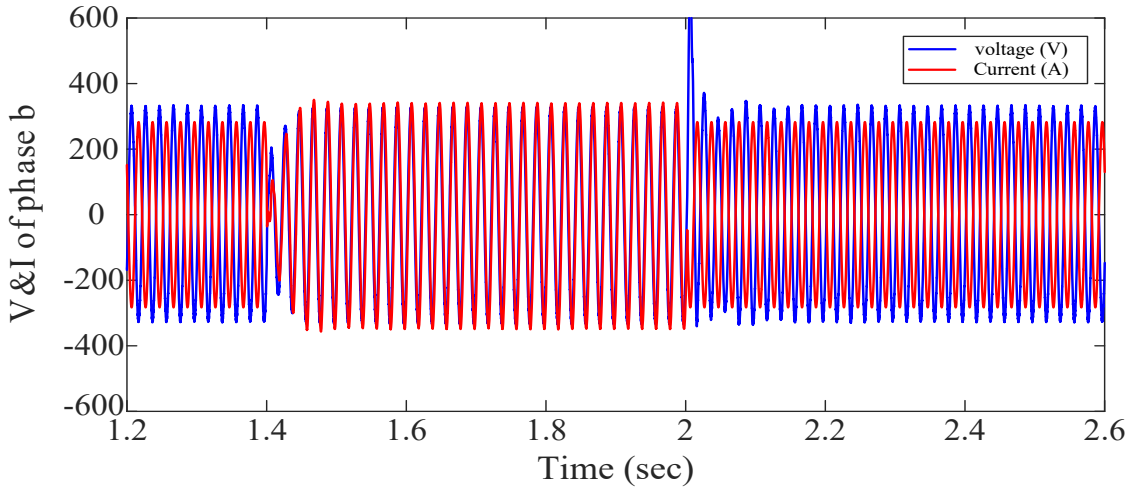


c) Primary side active and reactive powers

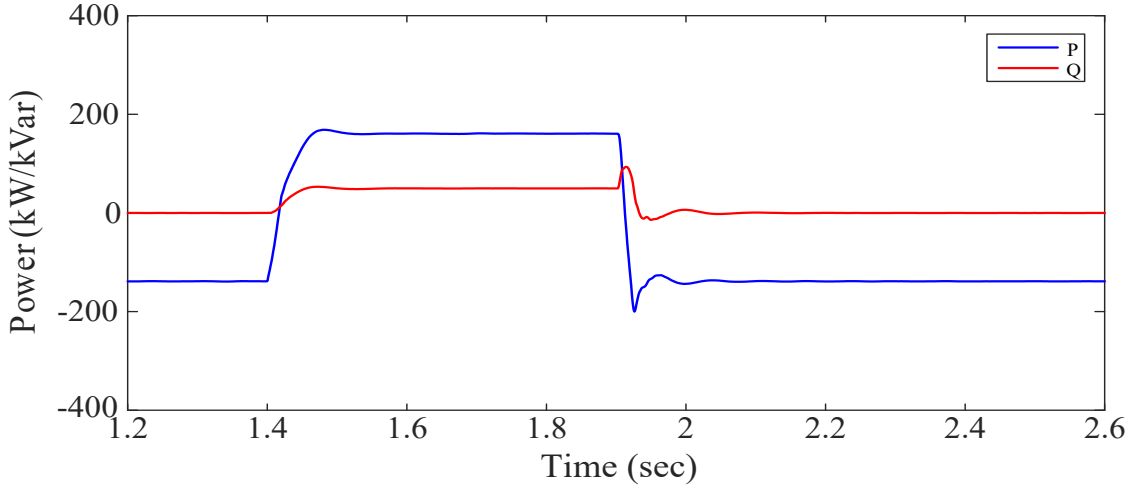
Figure 4.21. Test System 2 - Simulation results: Power flow reversal.



d) Secondary side current and voltage - Phase A



e) Secondary side current and voltage - Phase B

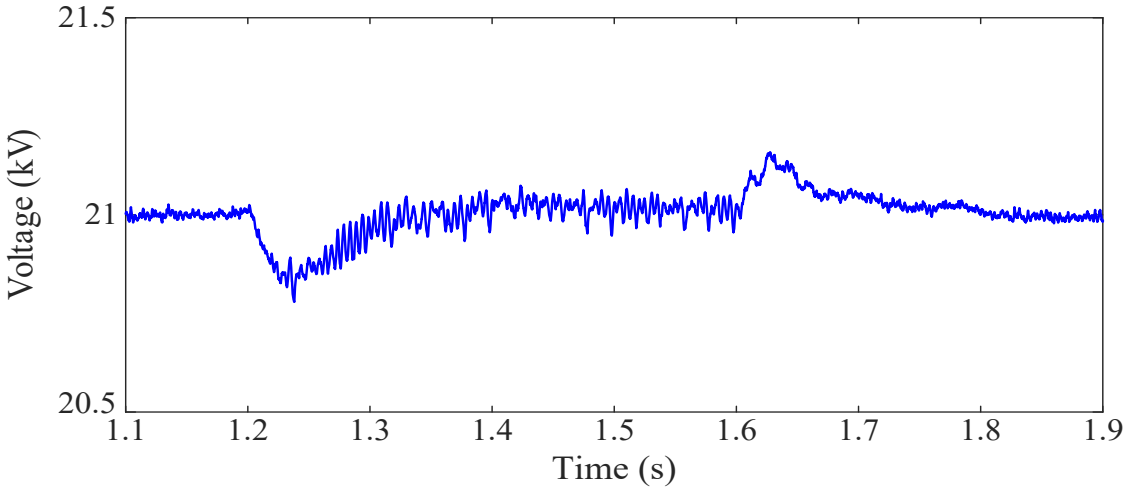


f) Secondary side active and reactive powers

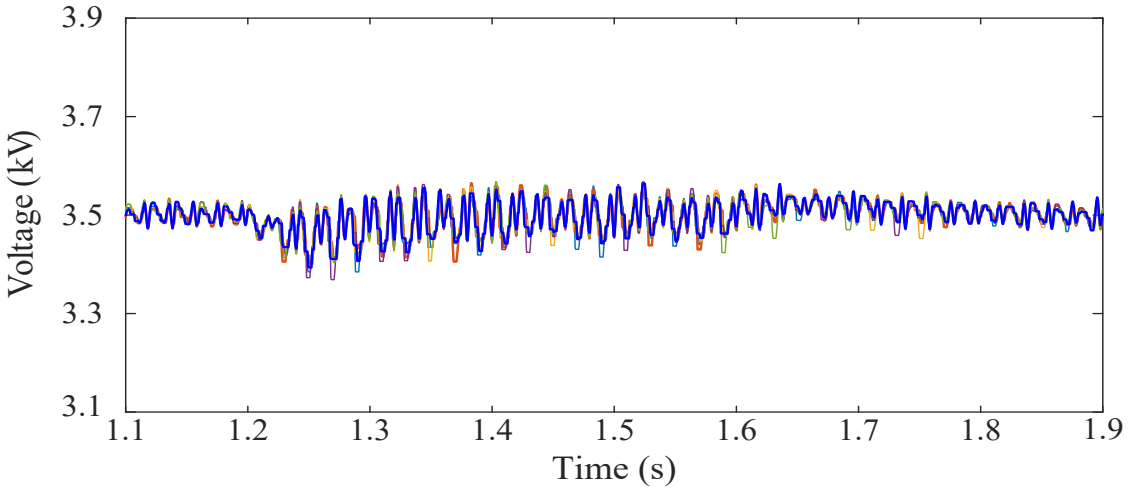
Figure 4.21. Test System 2 - Simulation results: Power flow reversal (cont.).

4.3.5. Discussion

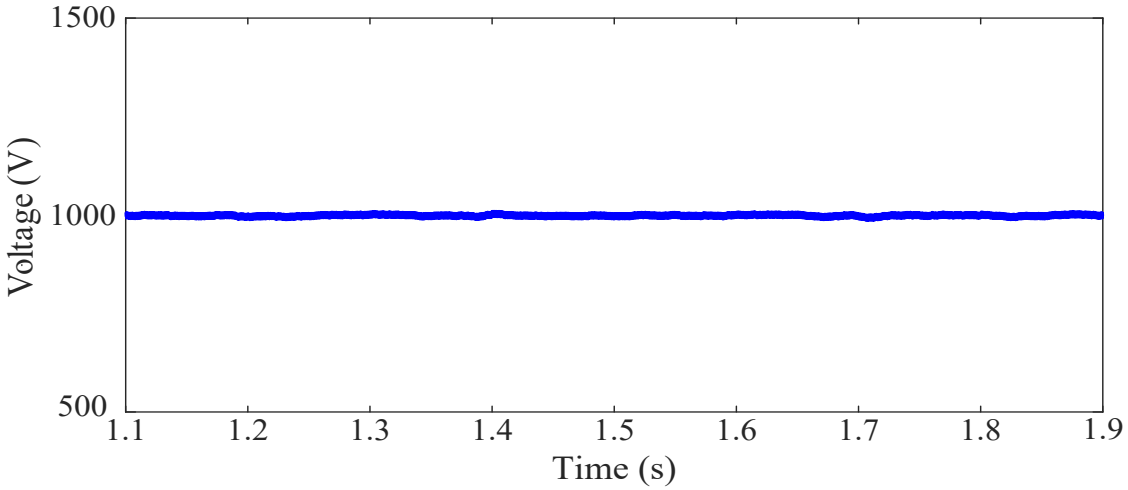
1. A simplified SST thermal model has been implemented since MV-side semiconductor losses were derived by assuming a junction temperature of all MV-side semiconductors within a given margin of values and rather small semiconductor losses. With this simplification the required CPU time could be significantly reduced, while the model performance was acceptable because MV-side currents were rather small. Obviously, for larger ratings and higher MV-side currents, a more detailed thermal model should also be implemented at the SST MV side.
2. Given that the SST model is based on that presented in section 4.2, its performance is as expected, and similar to the model without semiconductor losses; therefore, the discussion presented in section 4.2 is valid for the new SST model. Actually, only the first case study, in which the voltage sag and swell appears at the MV side to the short circuit fault occurrence in the distribution system, presents some novelty with respect to case studies analyzed in section 4.2. In any case, it is worth remembering that the SST performs as an efficient device that can provide some power quality improvements: the isolation between stages provided by the intermediate stage prevents the propagation of disturbances between input and output stages; in addition, the implemented design assures a quick SST reaction in front of disturbances. As with the discussion in previous section, SST ride-through capabilities have been analyzed (see Section 4.2.1). The new results confirm again that the SST performance is excellent: although the variation of the DC link voltages at the beginning and the end of transients depend on the type of transient and the variation is in percent much larger at the LV-side stage in case of power flow reversal, SST variables quickly recovers their initial values.
3. The capability for harmonic voltage compensation incorporated to the LV-side output converter prevents that distorted LV currents could affect the output voltage at the LV SST terminals: the proposed control (see Figure 2.13) can provide balanced secondary voltages with small THD, as one can observe from plots of Figure 4.19. Figure 4.26 presents the simulation result for nonlinear load connection with and without implementing control strategy with and without the capability of harmonic voltage compensation (HVC). As it can be observed from Figure 4.26.a, without harmonic voltage compensation capability the secondary side voltage is distorted including harmonic components.
4. It is important to keep in mind that, according to the conclusions presented in [4.9], the size, weight, and cost of the present or similar SST designs might exceed size, weight and cost of an equivalent conventional iron-and-copper transformer design. The most promising option for future SST designs is the use of SiC semiconductors: it is assumed that SST designs based on this technology will reduce size, weight, and losses with respect to a design based on conventional semiconductor technology, since a lower number of semiconductors working at very high switching frequencies (i.e. 50 kHz) will be required at the MV side; see, for instance, references [4.10]-[4.14].
5. The most challenging issue is the low SST efficiency. Although the results obtained in this work are in line with those previously presented, see [4.15]-[4.17], it is evident that the high number of semiconductors, the amount of semiconductor losses and the modulation techniques are three important factors that have some impact on efficiency. Future work will be addressed to optimize filter designs and design modulation techniques that combined with new multilevel topologies could improve SST efficiency.



a) MV-side dc link voltage

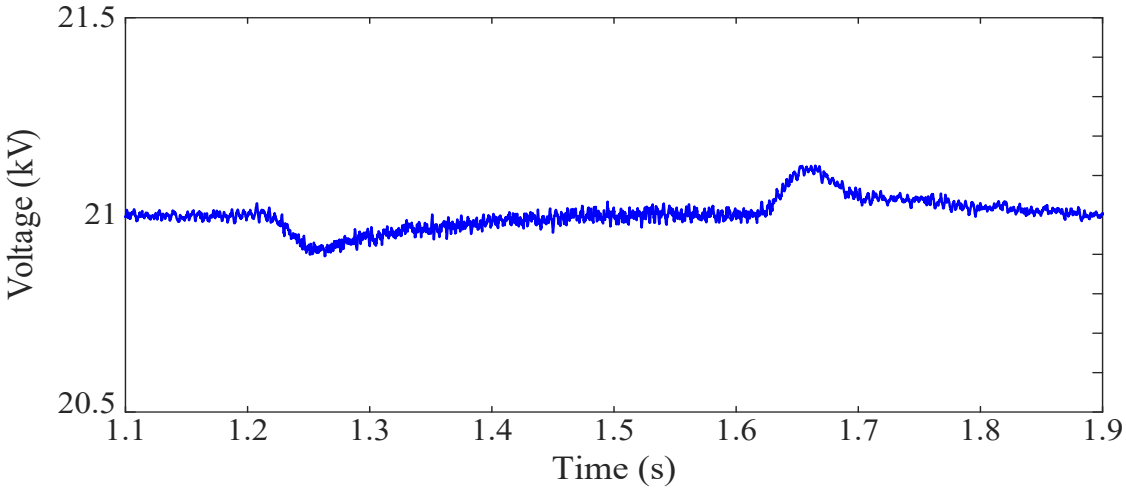


b) Capacitance voltage of upper arm of phase a

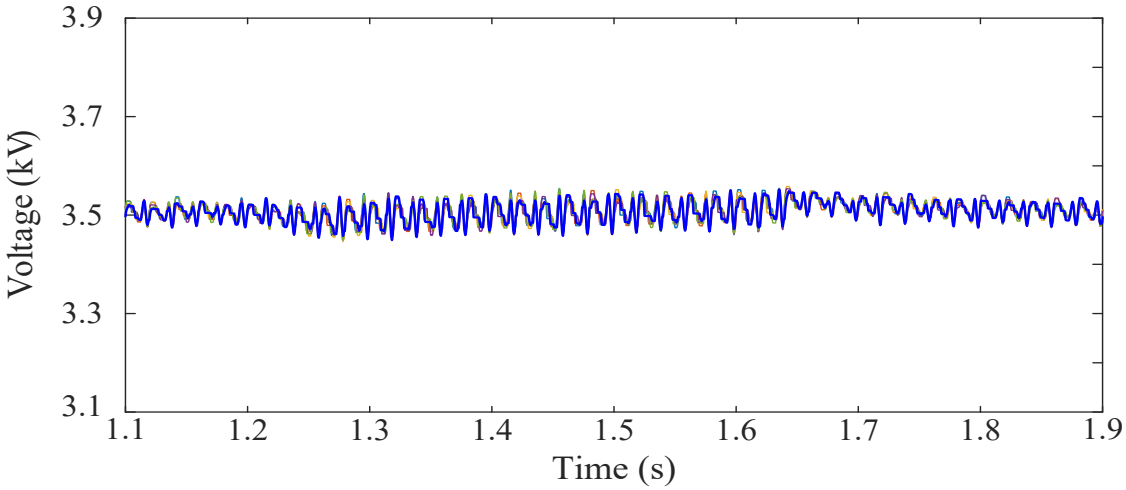


c) LV-side dc link voltage

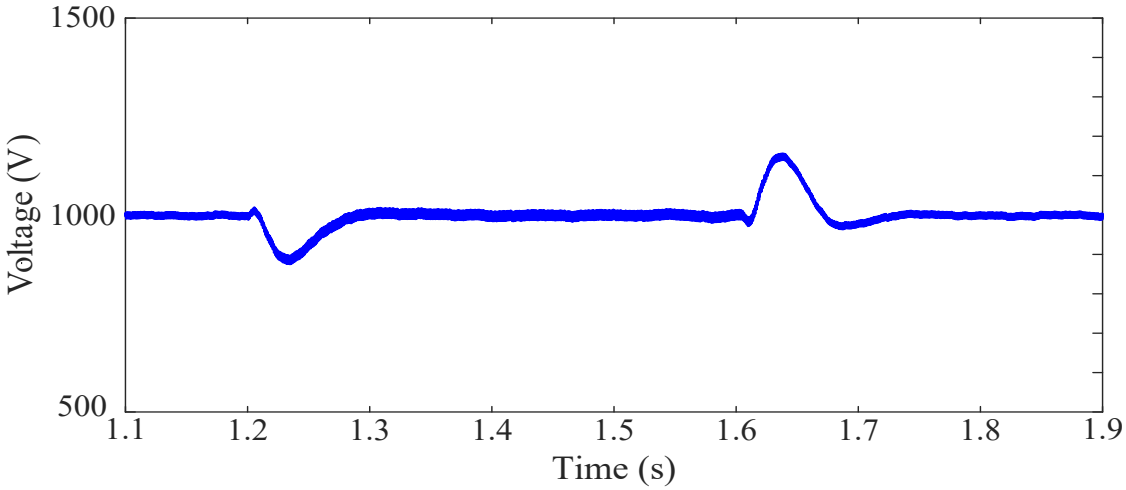
Figure 4.22. Simulation results: Voltage sag at the MV side.



a) MV-side dc link voltage

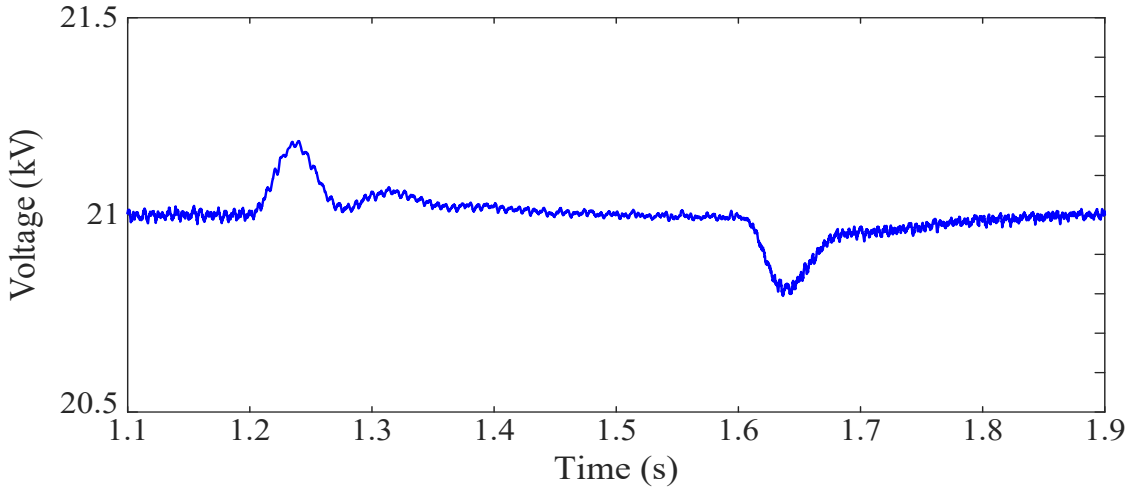


b) Capacitance voltage of upper arm of phase a

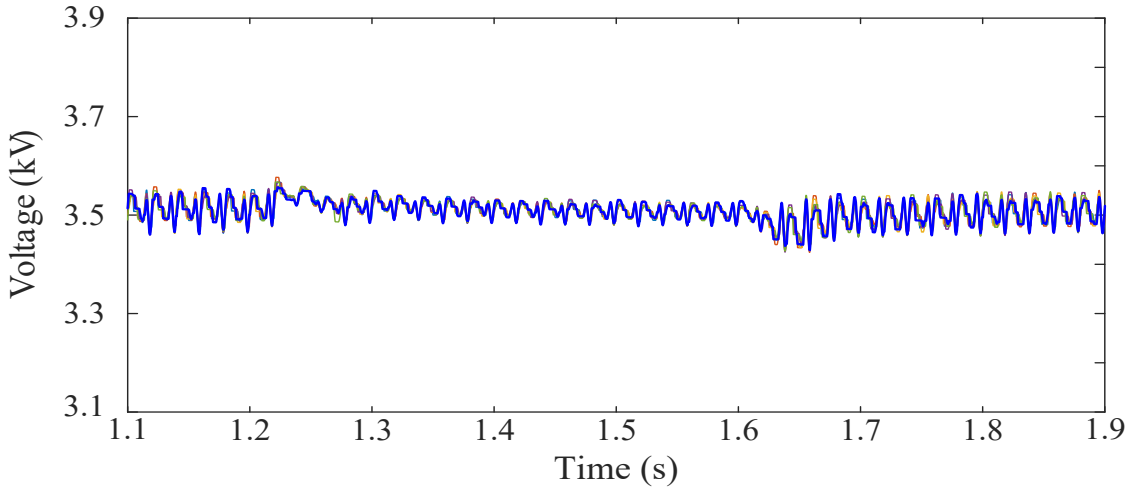


c) LV-side dc link voltage

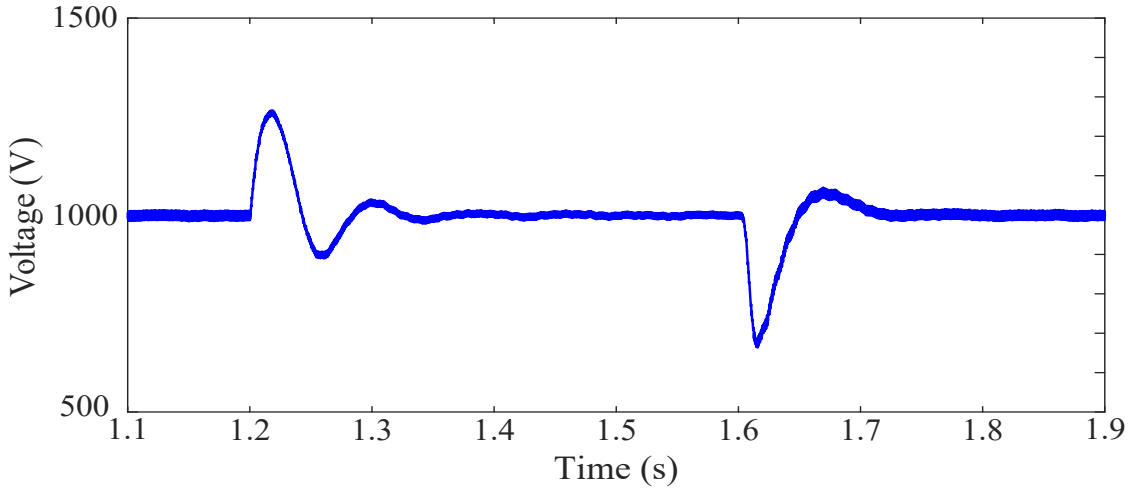
Figure 4.23. Simulation results: LV-side load variation.



a) MV-side dc link voltage

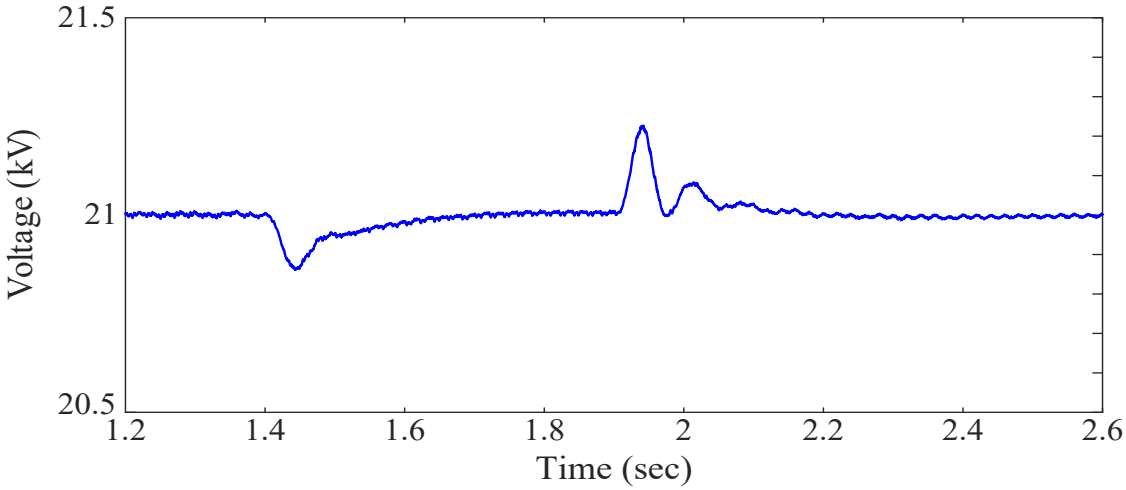


b) Capacitance voltage of positive arm of phase a

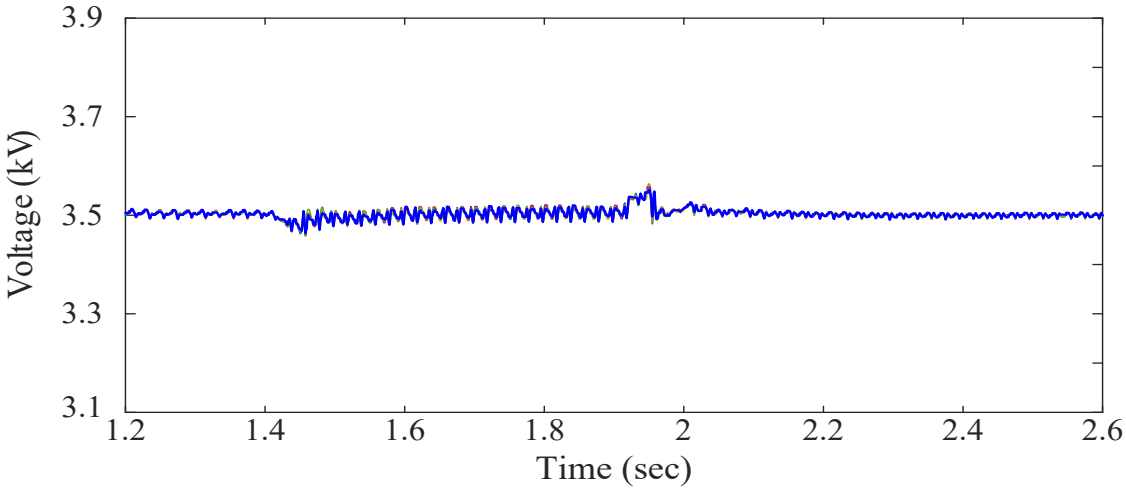


c) LV-side dc link voltage

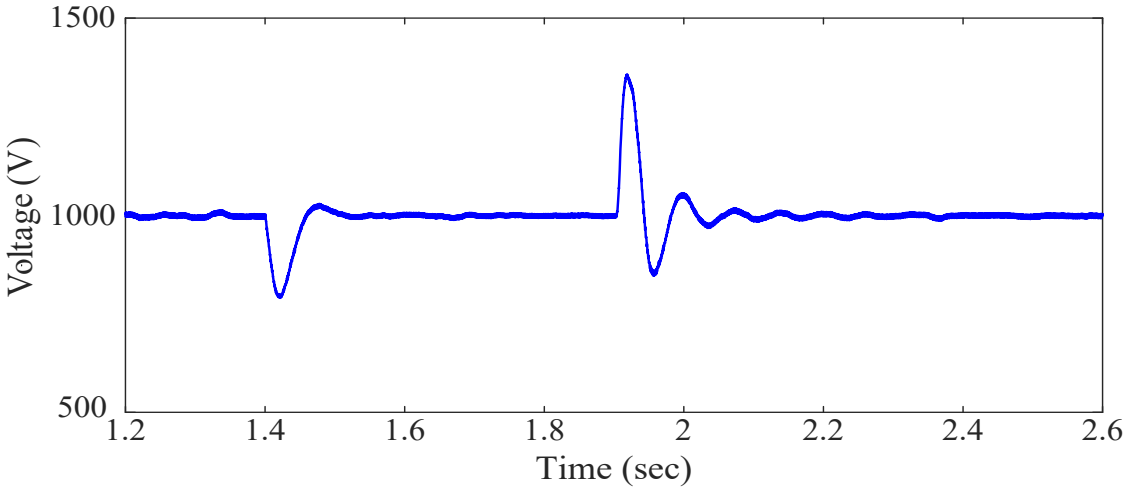
Figure 4.24. Simulation results: Short-circuit at the LV side.



a) MV-side dc link voltage



b) Capacitance voltage of positive arm of phase a



c) LV-side dc link voltage

Figure 4.25. Simulation results: Power flow reversal.

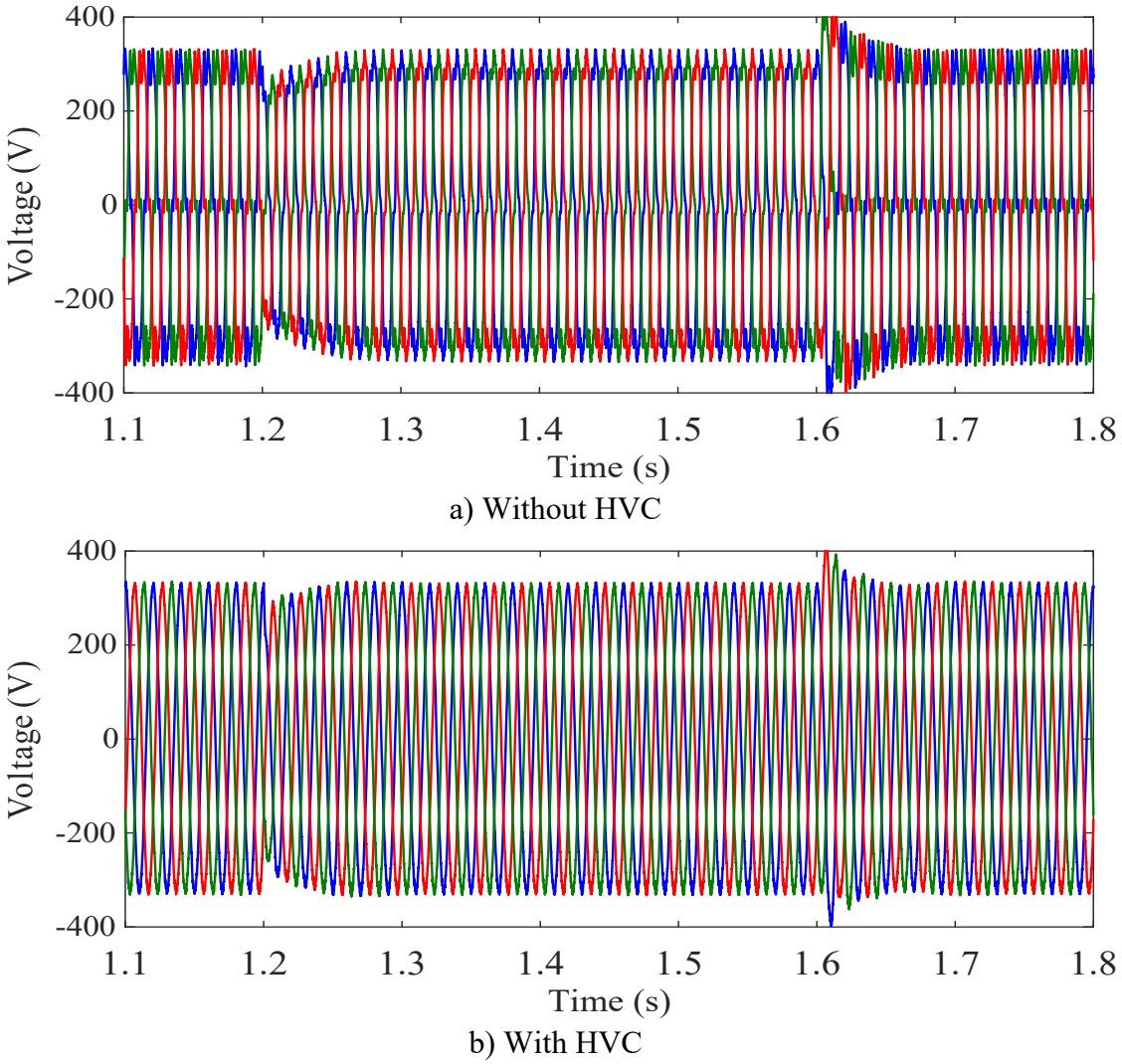


Figure 4.26. Simulation results: Nonlinear load without and with HVC.

4.4. Conclusion

This chapter has presented some simulation results from two case studies considering different test system configurations and SST models for each study:

1. A stand-alone three-stage MMC-based bidirectional SST without semiconductor losses.
2. A three-stage MMC-based bidirectional SST connected to a distribution network and with semiconductor losses.

The SST model has been simulated and tested under different operating conditions. As expected, simulation results prove the feasibility of the SST and its impact on power quality: the proposed bidirectional SST model is flexible enough to recover from voltage sag and swell at input stage and prevent its propagation to the output stage, compensate reactive power, compensate output stage voltage harmonics when supplying nonlinear loads, and prevent the propagation of short-circuit currents from the secondary to the primary side.

The most challenging issue is the low SST efficiency. Although the results obtained in this work are in line with those previously presented, see [4.15] and [4.17], it is evident

that the high number of semiconductors, the amount of semiconductor losses and the modulation techniques are three important factors that have some impact on efficiency.

4.5. References

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Chapter 5

General Conclusions

The solid state transformer (SST) is seen as a proper replacement of the conventional iron-and-copper transformer in the future smart grid. The SST offers several benefits (e.g. enhanced power quality performance or reactive power control at both primary and secondary sides) that can be of paramount importance for the development of the smart grid. In addition, the SST can provide some operational benefits, namely reduce environmental concerns by introducing a design that does not use mineral oil or other liquid dielectrics, and efficient management of distribution resources by incorporating on-line monitoring and other distribution automation functionalities.

This doctoral thesis focuses on advanced modeling of a three stage bidirectional MV/LV solid state transformer (SST) for distribution system studies. A modular multilevel converter (MMC) configuration is used in the MV side of the STT. The LV side uses a three-phase four-wire configuration that can be connected to both load and generation. The model developed for this work has been implemented in Matlab/Simulink, and its behavior has been tested by carrying out several case studies under different operating conditions. The simulation results support the feasibility of the SST and its advantages in comparison to the conventional transformer.

This thesis is aimed at:

- proposing a MMC-based SST model that can work when connected to any MV distribution network;
- implementing a more accurate representation of semiconductors by incorporating losses into their models;
- presenting more flexible and advanced SST controllers in order to provide a more efficient performance under demanding operating conditions.

Chapter 2 of this thesis gives a detailed description of a bidirectional three-stage MMC-based SST model considering both ideal (lossless) semiconductors and lossy semiconductors. The proposed configuration uses MMC technology at the MV side due to its scalability and flexibility: the design of devices with higher rated voltages at the

MV side can be derived from the design proposed by simply increasing the number of submodules and/or selecting higher-voltage submodules.

At the input stage, a three-phase MMC with half-bridge SMs is used. A voltage oriented control (VOC) strategy has been used to generate proper reference signals; a level-shifted PWM method is used as modulation technique. In addition, a sorting algorithm technique is used for balancing the SM capacitance voltages. The controllers provide the capability of voltage sag compensation.

The MV/LV isolation stage is divided into three parts: a single-phase MMC, a HFT and a single-phase bidirectional PWM converter. An open-loop level-shifted PWM and a sorting algorithm have been used to control the MV single-phase MMC, while a proportional-resonant (PR) based control is applied to the LV single-phase bidirectional PWM converter.

A three-phase four-leg converter is used for the LV output stage. A comprehensive VOC strategy with a three-dimensional SVM modulation technique has been implemented to generate proper reference signals. The proposed control can provide good performance of SST both under unbalanced load conditions and also nonlinear load connection by having the capability of harmonic voltage compensation. The control diagram and topology of all three stages are explained in detail in order to implement a SST to have good performance under different case studies.

A realistic representation of a power electronic device must incorporate semiconductor losses. This aspect is fundamental to decide about the viability of a given device design or to assess its impact as part of a large network. Although the SST is seen as a component with a crucial role in the future smart grid, the fact is that the efficiency of current SST designs is lower than that of the conventional transformer. Therefore, it is important to develop a SST model in which semiconductor losses are reliably represented. Some important aspects are required in such a model: its configuration must be as close to the real device as possible, and its model must be flexible enough to represent the performance of any semiconductor and its losses. It is evident that such a model may imply a very complex and sophisticated representation, which will be even more computer demanding in case of simulating the SST model as a part of a larger system (e.g. a large distribution system).

A simple approach is proposed for calculating and implementing semiconductor losses by using experimental values extracted from manufacturer datasheets: first, semiconductor losses are calculated from manufacturer datasheets, but since losses depend on temperature, the semiconductor thermal models are included in converter models; second, the losses are incorporated as part of the semiconductor model by means of controlled sources whose instantaneous values are obtained from the external calculation carried out in the first step. It is therefore a closed-loop approach that uses information available in manufacturer data sheets.

The implementation of the three-stage MMC-based SST in Matlab/Simulink with and without including semiconductor losses has been detailed in Chapter 3, which provides a detailed description of both power stages and control strategies.

Chapter 4 presents the simulation results for several case studies considering two different SST models and two test systems. The first test system is an ideal (lossless) stand-alone SST; the second test system is a MV distribution system to which a lossy SST is connected. The simulation results derived from both test systems have shown

that the bidirectional SST incorporates some advanced capabilities (e.g., fast voltage and power flow control, reactive power compensation, voltage sag compensation) that support its feasibility as a fundamental component of the future smart grid. Intermediate SST dc links provide stage decoupling, and prevent disturbances at one side from propagating to the other side (e.g., LV-side secondary load immunity is achieved in front of an unbalanced situation caused by a voltage sag at the MV-side input stage; unbalanced currents at the LV side are not noticed at the MV side).

The envisaged applications of the SST are many. Utilities are looking for reliable and effective components that could offer potential for remote supervision and control; new grid codes and higher penetration of distributed generation will increase the utilities interest in voltage regulation and controllability. Solar and wind power developers are other potential customers as they are aiming at using the existing and future grid as efficiently as possible. Industries are also concerned about reliability and availability of the apparatus but also about preventing the impact of disturbances in their production.

The work and results presented in this thesis have also evidenced some SST limitations: the efficiency of this device is lower that its iron-and-copper counterpart; its modular configuration requires a not-so-low volume and weight. Future work should be focused on improving those aspects that could present a wide SST application. In addition, there are some design and modelling aspects that could of paramount importance for the analysis and implementation of future SST designs. A short list of future tasks is presented below:

- Design of new SST configurations with lower number of semiconductors and a higher efficiency (SiC technologies are certainly the best candidates for achieving such a goal).
- New control strategies that could take advantage of a smaller configuration in order to obtain a better efficiency under any operating condition.
- The SST model proposed in this thesis has a very complex configuration. The simulation time required to test such model is in some case studies too long. The development of dynamic averaged models would be a solution for this drawback, and at the same time would allow their simulation in real-time platforms, an approach that could facilitate the design of new and better controllers by using HIL (hardware-in-the-loop).
- The design and performance of the filters to be installed at both the input and output stages is a crucial aspect for which some optimization is desired.

Appendix

Prototypes and Simulation Tools

Although the field experience with the solid state transformer is not too significant to date, a very high number of prototypes have been built. A high percentage of those works joined laboratory tests with actual prototypes with the implementation of a computer model that could be used to validate the model. On the other hand, it is important to keep in mind that a computer model is by itself an important contribution since not many laboratories can test a SST prototype in a real environment (e.g. as a component of an actual distribution system).

Both aspects, building and testing prototypes and computer models, are important in order to prove the feasibility of the SST and obtain experience about the best ratings, topologies, control strategies, and capabilities.

This appendix provides a summary of the prototypes and simulation models built and tested to date.

Table A1 presents a list of some SST prototypes. The list is by no means complete. At the time of deciding the works that should be included in the table those for which complete information, as presented in the table, was available were selected. Note that the required information includes rating, configuration, control strategies, capabilities and laboratory tests.

Most prototypes listed in Table A1 were tested under both steady-state and transient conditions. SST capabilities and laboratory tests that were accounted for preparing the table are listed below:

- Robustness of SST against voltage sags and swells at the primary terminals.
- Power factor correction (in general, unit power factor at the primary terminals).
- Harmonic voltage compensation in case of nonlinear load connected to the secondary side.
- Stable behavior of the dc-links and terminal voltages.

- Current limiting capabilities to provide protection in case of short circuit at the secondary side terminals.
- Bidirectional power flow to cope with reversal power flow conditions.
- Short-term ride-through capabilities in the case of voltage excursions.

Given that a multilevel configuration is presently needed for MV-side converters, an important aspect analyzed in Table A1 is the configuration of these converters. According to the table, the most common topologies are the cascaded H-bridge (CHB) topology and the modular multilevel converter (MMC) topology.

The most popular control strategies are based on pulse width modulation (PWM) for both input and output stages, and phase shift modulation strategy for the isolation stage.

Likewise, Table A2 summarizes the work carried out on SST simulation. Again, only works for which complete information was available were selected. That information covered the following items: simulation tool, modeling approach (i.e. steady-state vs. transient model, switched vs. average mode), configuration, control strategies, and a minimum of case studies that could support the feasibility of the SST as a component of the distribution system.

SST models have been implemented using the simulation tools listed below:

- Matlab/Simulink,
- Matlab/Simulink with PLECS,
- PSCAD,
- PLECS,
- SPICE,
- SPICE with PLECS,
- SABER,
- SABER with SPICE,
- PSIM,
- EMTP/ATP,
- OpenDSS,
- Digsilent Power Factory,
- Real Time Digital Simulator (RTDS),
- Opal-RT.

The greatest percentage of simulation works used Matlab/Simulink. Note also that some works were aimed at implementing SST models for real-time simulation. Take into account that RTDS and Opal-RT are real-time simulation platforms.

Note: The following acronyms have been used in Table 1.

DAB = Dual Active Bridge

MMC = Modular Multilevel Converter

NPC = Neutral point Clamped

PWM = Pulse Width Modulation

SVM = Space Vector Modulation

SVPWM = Space Vector Pulse Width Modulation

ZVS = Zero Voltage Switching

Table A1 – SST Prototypes

Ratings	Configuration	Control-strategies	Capabilities	Laboratory tests	Refs.
10 kVA, 7.2 kV/240V	Three stage, cascaded H-bridge	PWM	Unidirectional power flow, power-factor correction	Steady state, unbalanced load	[A.1], [A.2]
5 kVA, 220 V/380 V	Two stage, direct AC/AC high-frequency link, dual bridge matrix converter topology	3D SVPWM	bidirectional power flow, low harmonic distortion	Unbalanced linear load, unbalanced input voltage	[A.3]
50 kVA, 2.4 kV/ 240V/ 120V	Three stage, Three level NPC in MV side	PWM	Voltage sag compensation, fault isolation	voltage sag, load variation, unbalanced load	[A.4]
1.5 kW, 230 V/39V	Three stage, cascaded H-bridge	PWM	Bidirectional power flow, harmonic voltage compensation, reactive power compensation	Voltage sag, nonlinear load	[A.5]
2 kW, 110V/20V	Single-stage, AC/AC, two level	PWM	Bidirectional power flow, maximum power-point tracking	Steady state	[A.6]
20 kVA, 7.2 kV/240 V	Three stage, cascaded H-bridge	PWM	Bidirectional power flow	Steady-state	[A.7]-[A.17]
54 kW, 1.5 kVac/360Vdc	Two stage, cascaded H-bridge	PWM	Bidirectional power flow	Steady state, load variation, reverse power flow	[A.18], [A.19]
1.2 MVA, 15kV/16.7Hz	Two stage, cascaded H-bridge	PWM	Bidirectional power flow	Steady state, load change, reverse power flow,	[A.20], [A.21], [A.22]
1 kW, 208V/120V	Three-stage, two level	PWM	Bidirectional power flow	Start-up transients	[A.23]
100 kW, 10kVac/750V dc	Two stage, AC/DC/DC, MMC	PWM	Bidirectional power flow	Steady state	[A.24]
2 kVA, 1.9 kV/127 V	Three stage, Multilevel converter	PWM, ZVS operation	Bidirectional power flow, voltage sag compensation	Steady state, voltage sag, reverse power flow	[A.25], [A.26]
10 kW, 3.6 kV/120 V	Three stage, two level	PWM	Bidirectional power flow, harmonic voltage compensation	Steady state, nonlinear load, load variation	[A.27], [A.28], [A.29], [A.30], [A.31], [A.32]
1 kW, 353.55/220	Two stage AC/AC, MMC	PWM	Unidirectional power flow	Steady state	[A.33]
50 kVA, 480V/480V	Single stage, Dyna-C AC/AC topology	PWM	Bidirectional power flow	Steady state	[A.34], [A.35]
600 kVA, 3.3 kV dc / 3.3 kV dc	Three stage, cascaded H-bridge in MV side	PWM	Bidirectional power flow	Steady state	[A.36]

Table A1 – SST Prototypes (cont.)

Ratings	Configuration	Control-strategies	Capabilities	Laboratory tests	Refs.
5 kW, 3300Vac/380 Vdc	Two stage, cascaded H-bridge	Phase shift modulation	Bidirectional power flow	Steady state	[A.37]
2 kW, 300 V/ 60 V	Three stage, two level	PWM	Bidirectional power flow	Steady state, load variation	[A.38]
2 kVA, 380V/120V	Three stage, cascaded	PWM	Bidirectional power flow	Steady state, power flow reversal, startup	[A.39]
5.8 kVA, 5kVdc/800Vdc	Three stage, NPC with SiC	PWM	Bidirectional power flow	Steady state	[A.40]
150 kVA, port1:750Vdc, port2:375Vdc, port3: 750Vdc	Triple active-bridge with energy storage	Phase shift modulation	Bidirectional power flow	Steady state	[A.41], [A.42]
3-kVA, 2.4kV/127V	Three stage, two level	PWM	Unidirectional	Steady state, nonlinear load	[A.43]
10 kVA, 208 V	Single stage AC/AC, two level, soft-switching solid state transformer	Soft-switching, ZVS	Bidirectional power flow	Steady state	[A.44]
2 kW, 600Vdc/200Vdc	Three phase modular multilevel dc/dc converter	PWM, ZVS, dual-phase-shift method	Bidirectional power flow	Steady state	[A.45]
10 kVA, 3.8 kVdc/200Vdc	Three stage, single phase single converter cell based SST for wind energy conversion system	PWM	Bidirectional power flow	Steady state, load variation	[A.46]
2 kW, 400V/208V	Single stage, AC/AC, matrix based	Predictive Control	Bidirectional power flow	Steady state, load variation, unbalanced voltage and current	[A.47], [A.48]
100 kVA, 13.8 kV/120V or 240 V	Three phase, three stage, cascaded blocks	PWM	Unidirectional power flow	Steady state, unbalanced load, voltage sag, non-linear loads, capacitor switching transient, load step transient	[A.49]
20 kVA, 2.4kV/120Vac or 240Vac or 48V dc	Single phase, three stage, NPC multilevel, multiport-output DC/AC inverter	PWM	Unidirectional power flow	Steady state, load change, load unbalance, nonlinear load, voltage sag	[A.50], [A.51], [A.52]

Table A2 – SST simulation tools

Simulation tool	Modeling approach	Configuration	Refs.
Matlab/Simulink	Switching model	Three phase input matrix converter, three-phase four-wire output matrix converter	[A.53]
Matlab/Simulink	Average model	Three phase, three stage, two level	[A.54]
Matlab/Simulink	Switching model	Single phase, three stage, cascaded H-bridge	[A.55], [A.5]
Matlab/Simulink	Switching model	Three phase, single stage AC/AC, matrix converter topology	[A.56], [A.57], [A.58]
Matlab/Simulink	Average model	Three phase, three stage, two level	[A.59]
Matlab/Simulink	Average model	Three phase, three stage, multi transformer in isolation stage, two level	[A.60]
Matlab/Simulink	Average model	Single phase, three stage, cascaded H-bridge	[A.61], [A.62]
Matlab/Simulink	Switching model	Direct dc/ac matrix based converter topology	[A.63]
Matlab/Simulink	Switching model	Single power conversion stage ac/ac matrix based power converter topology	[A.64]
Matlab/Simulink	Average model	Single-phase, three stage, cascaded H-bridge	[A.65], [A.66], [A.67]
Matlab/Simulink	switching model	Three phase, three stage, two level	[A.68], [A.69], [A.70], [A.71]
Matlab/Simulink	Switching model	Single phase, cascaded H-bridge	[A.72]
Matlab/Simulink	Switching model	Three phase, single stage AC/AC SST, with two matrix converter at the primary and secondary	[A.73], [A.74], [A.75]
Matlab/Simulink	Average model	Three phase, three stage, two level	[A.76], [A.77]
Matlab/Simulink	Switchin model	Three phase, three stage, matrix converter at LV side	[A.78], [A.79], [A.80], [A.81]
Matlab/Simulink	Switching model	Three stage, NPC at MV side	[A.82], [A.83], [A.84], [A.85]
Matlab/Simulink	Average model	Single phase, three stage, cascaded H-bridge	[A.86]
Matlab/Simulink	Average model	Three stage, two level	[A.87], [A.88], [A.89], [A.90], [A.91]
Matlab/Simulink	Switching model	Single phase, three stage, MMC topology in MV side	[A.92], [A.93], [A.94], [A.95]
Matlab/Simulink	Switching model	Three phase, three stage, cascaded H-bridge	[A.96]
Matlab/Simulink	Average model	Single phase, three stage, two level	[A.97]
Matlab/Simulink	Switching model	Single phase, three stage, cascaded H-bridge	[A.16]
Matlab/Simulink	Switching model	Three phase, three stage, two level in input and isolation stage, nine-switches in its output stage	[A.98]
Matlab/Simulink	Average model	A modular design of the sub-module of the modular multilevel converter, two stage	[A.99]
Matlab/Simulink	Average model	Single phase, both two stage and three stage, cascaded H-bridge in MV side	[A.100]
Matlab/Simulink	Switching model	Single phase, three stage, CHB in MV side	[A.101], [A.102]
Matlab/Simulink	Average model	multiport dc-dc converter based SST, two stage and three stage, QAB-based SST with PV and storage integrated through HFT	[A.103]
Matlab/Simulink	Switching model	Three stage, QAB-based SST with PV and storage integrated through HFT	[A.104]
Matlab/Simulink	Switching model	Three phase, three stage, MMC converter in MV side ,three phase matrix converter in output stage	[A.105]
Matlab/Simulink	Switching model	Multifed three stage, two level,	[A.106]
Matlab/Simulink	Average model	Single phase, three stage, two level	[A.107]
Matlab/Simulink	Switching model	Three Phase Modular Multilevel DC/DC Converter	[A.108]

Table A2 – SST simulation tools (cont.)

Simulation tool	Modeling approach	Configuration	Refs.
Matlab/Simulink	Average model	Three phase, three stage, cascaded multilevel in input and output stage	[A.36]
Matlab/Simulink	Switching model	Three phase, three stage, cascaded multilevel in input and output stage	[A.109]
Matlab/Simulink	Switching model	Single phase, three stage with bidirectional LLC resonant DC-DC converters as isolation unit, CHB in input stage, multi/output port	[A.110]
Matlab/Simulink	Average model	Two stage, two level, DAB and output stage	[A.111]
Matlab/Simulink	Switching model	Two stage, two level, DAB and output stage	[A.112]
Matlab/Simulink	Switching model	Three phase, single stage, modular multilevel dc/dc converter	[A.45]
Matlab/Simulink	Switching model	Three phase, three stage, MMC based	[A.113], [A.114]
Matlab/Simulink	Switching model	Three phase, three stage, NPC in MV side, matrix converter in LV side	[A.115]
Matlab/Plecs	Switching model	Cascaded Ac-Ac dual active bridge converter	[A.116]
Matlab/Plecs	Average model	Two stage, Cascaded H-bridge	[A.11]
Matlab/Plecs	Switching model	Three phase, three stage, flying capacitor topology in MV side	[A.117]
Matlab/Plecs	Average model	three stage and two stage, multi-port dc/dc converter, quad-active-bridge (QAB) converter, integrate PV and storage	[A.118], [A.119], [A.120]
Matlab/Plecs	Switching and average models	Single phase, three stage, two level	[A.121]
Matlab/Plecs	Switching model	Single phase, three stage ,AC/DC,DC/DC and DC/DC	[A.122]
Matlab/Plecs	Switching model	series resonant three port, two stage, AC/DC/DC	[A.123]
Matlab/Plecs, RTDS	Average model	Single phase, three stage, two level	[A.124]
PLECS	Switching model	Matrix Converter based Power Electronic Transformer	[A.125]
PLECS	Average model	Single phase, three stage, cascaded H-bridge	[A.15]
PLECS	Average model	Single phase, three stage, two level	[A.126]
PLECS	Average model	Single phase, three stage, cascaded H-bridge	[A.127]
SPICE/PLECS	Dynamic phasor-based model	Three phase, three stage, modular and a cascade model of SST	[A.128]
SPICE	Switching model	Two stage, AC/DC/DC, special topology	[A.129], [A.130]
PSPICE	Switching model	Single phase, three stage, two level with bidirectional LLC resonant DC/DC converter	[A.30]
Saber	Switching model	Dual active bridge	[A.131]
SABER/SPICE	Switching model	Five-level flying capacitor DC/DC Converter	[A.132]
PSCAD	Average model	Single phase, three stage, cascaded H-bridge	[A.133]
PSCAD	Average model	Three stage, two level	[A.134], [A.135], [A.136], [A.137]
PSCAD	Switching model	Three phase, three stage, two level	[A.138]
PSCAD	Average model	Three phase, three stage, cascaded H bridge topology	[A.139]
PSCAD	Switching model	Three phase, three stage, MMC in input stage, multi-transformer in DAB	[A.140]
PSCAD/EMTDC	Switching model	Tri-directional power electronic transformer, single stage dc/ac	[A.141]

Table A2 – SST simulation tools (cont.)

Simulation tool	Modeling approach	Configuration	References
PSCAD/EMTDC	Switching model	Single phase, single stage, dc/ac	[A.142]
PSCAD/EMTDC	Switching model	Three phase, three stage, NPC in MV side	[A.143]
PSCAD/EMTDC	Switching model	Three phase, three stage, push-pull Converter in DAB stage	[A.144]
PSCAD/EMTDC	Switching model	Single phase, three stage, multilevel	[A.25]
PSCAD/EMTDC	Switching model	Three phase, three stage, cascaded H-bridge in input and output stages	[A.145]
PSCAD/EMTDC	Switching model	Single phase, three stage, cascaded H-bridge	[A.146], [A.147]
PSCAD/EMTDC	Switching model	Three phase, three stage, two level	[A.148]
PSCAD/EMTDC	Switching model	Multi-source fed power electronic transformer, three stage, NPC in MV side	[A.149]
PSCAD/EMTDC	Switching model	Triple port active bridge converter based multi-fed PET, three stage, two level	[A.150]
PSCAD/EMTDC	Switching model	MMC, DC/DC stage for DC microgrid	[A.151]
PSIM	Switching model	DC/DC isolation stage, two level	[A.152], [A.153]
PSIM	Switching model	DC/DC isolation stage, NPC based	[A.154], [A.155]
PSIM	Switching model	Single phase, two stage, cascaded topology, AC/DC/DC	[A.37], [A.156]
PSIM	Switching model	Three phase, three stage, cascaded H-bridge	[A.157], [A.158]
PSIM	Average model	AC-AC hybrid dual active bridge	[A.159]
EMTP	Switching model	Three stage, two level	[A.160]
EMTP	Switching model	Three phase, three stage, NPC based	[A.161]
EMTP	Switching model	Three phase, three stage, cascaded modular structure in MV side	[A.162]
OPENDSS	Steady-state model	Three phase, three stage, two level	[A.163]
Simplorer	Switching model	Three phase, three stage, NPC based	[A.164]
RTDS	Average model	Single phase, three stage, cascaded H-bridge	[A.165]
RTDS	Average model	Single phase, three stage, two level	[A.166]
OPAL-RT	Switching model	Multiple Resonances Mitigation of Paralleled Inverters in a Solid-State Transformer enabled ac microgrid, three stage	[A.167]
Multisim/Labview	Switching model	Single phase, two stage, matrix based converter	[A.168], [A.169]
Digsilent Power Factory	Average model	Three phase, three stage, two level	[A.170]

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