# DESIGN OF CLUSTERED SUPERSCALAR MICROARCHITECTURES

**Joan-Manuel Parcerisa**

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# ABSTRACT

Over the past decade superscalar microprocessors have achieved enormous improvements in computing power by exploiting higher levels of parallelism in many different ways. High-performance superscalar processors have experienced remarkable increases in processor width, pipeline depth and speculative execution. All of these trends have come at an extremely high increase in hardware complexity and chip resource consumption. Until recently, their main limitation has been the availability of such resources in the chip, but with current technology shrinks and increases in transistor budgets, other limiting factors have become preeminent, such as power consumption, temperature and wire delays. These new problems greatly compromise the scalability of conventional superscalar designs.

Many previous works have demonstrated the effectiveness of partitioning the layout of several critical hardware components as a means to keep most of the parallelism while improving the scalability. Some of these components are the register file, the issue queue and the bypass network. Their partitioning is the basis for the so called clustered architectures. A clustered processor core, made up of several low complex blocks or clusters, can efficiently execute chains of dependent instructions without paying the overheads of a long issue, register read or bypass latencies. Of course, when two dependent instructions execute in different clusters, an inter-cluster communication penalty is incurred. Moreover, distributed structures usually imply lower dynamic power requirements, and they simplify power management via techniques such a selective clock/power gating and voltage scaling.

The purpose of this thesis is to study several key aspects of a clustered architecture with fully distributed components. The first target of this research is the distribution of instructions among clusters, since it plays a major role on performance. The main goals of a cluster assignment algorithm are to keep the workload balanced and to reduce critical communications among clusters. Several techniques are proposed to achieve these goals from two different perspectives: slice-based algorithms, that assign groups of dynamic instructions, and algorithms that operate on a per-instruction basis. The second contribution of this thesis proposes value prediction as a means to mitigate the penalties of inter-cluster communications while also improving workload balance. The third aspect considered is the cluster interconnect, which mainly determines communication latency. Several techniques are proposed to design it seeking for the best trade-off between cost and performance. Finally, the last contribution proposes techniques for clustering the main components of the processor front-end, i.e. those involved in branch prediction, instruction fetch, decoding, cluster assignment and renaming.

# AGRAÏMENTS

En primer lloc, gràcies a Antonio González, de qui he après tantes coses sobre l'ofici de la recerca, i sobre l'arquitectura de computadors al llarg d'aquests anys. Gràcies per la seva confiança, els seus savis consells i la seva tenaç iniciativa.

A en Ramon Canal, en Julio Sahuquillo, en José Duato i en Jim Smith, entusiastes col.laboradors amb qui he tingut fèrtils discussions tècniques i que han proporcionat significatives contribucions a aquesta tesi.

A Jordi Cortadella i Mateo Valero per confiar en mi per al primer projecte amb què vaig debutar al DAC, i que va suposar el meu primer contacte amb la recerca científica.

A tots els companys del departament, de qui he rebut sempre mostres de suport i amb els quals he tingut sempre converses estimulants. La llista és llarga, i segur que em deixo algú, però vull esmentar especialment a Pedro, Ramon, Josep-Llorenç i Fernando, amb qui he compartit les millors gresques i hem passat les millors estones. També a en Pepe, Suso, Josep-Ramon, Daniel, Enric, Cristina, Miguel, Agustín, Fermín, Josep, Luisma, Jordi, David, Llorenç, Chema i els antics companys de despatx Susana i Fernando. Gràcies també al personal tècnic de sistemes i de secretaria, que m'han ajudat sempre amb promptitud i eficàcia, i als organismes públics que han finançat aquest treball[1].

A la Roser, per la seva paciència, suport i afecte, amb qui he compartit els moments dolços i els difícils d'aquesta tesi durant tots aquests anys, i amb qui espero compartir nous projectes durant molts anys més.

I finalment, vull agrair a tota la meva família, pares Josep i Manuela i germans Josep, Jordi i Ramon, que sempre m'han guiat i encoratjat, i junt amb els quals he après a conèixer el valor de l'esforç, el plaer de l'aprenentatge, i tantes altres virtuts sense les quals no hauria reeixit. Gràcies en especial al meu pare, que em va brindar l'oportunitat d'iniciar, ja tardanament, els estudis d'informàtica.

1. This work was supported by the Spanish Ministry of Education under contracts TIC-95-0429, TIC-98-0511 and TIC-2001-0995, and by the CEPBA (European Center for Parallelism of Barcelona)

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