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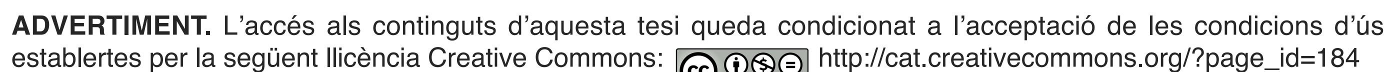
ADVERTIMENT. L'accés als continguts d'aquesta tesi queda condicionat a l'acceptació de les condicions d'ús establertes per la següent llicència Creative Commons:  http://cat.creativecommons.org/?page_id=184

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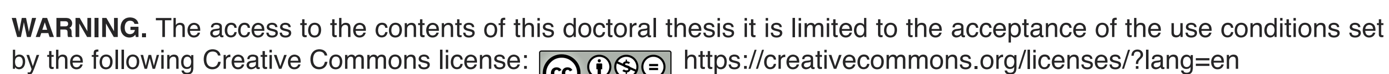
WARNING. The access to the contents of this doctoral thesis it is limited to the acceptance of the use conditions set by the following Creative Commons license:  https://creativecommons.org/licenses/?lang=en

ANALYSIS OF IMPACT OF NANOSCALE DEFECTS ON VARIABILITY IN MOS STRUCTURES

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in the

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APRIL 2018

The undersigned, Dr. Marc Porti Pujal and Javier Martín Martínez, Associated Professors of the Electronic Engineering Department (Engineering School) of the *Universitat Autònoma de Barcelona*

CERTIFY:

that the thesis entitled *"Analysis of impact of nanoscale defects on variability in MOS structures"* submitted by Carlos Couso Fontanillo to the School of Engineering in fulfillment of the requirements for the degree of Doctor of Philosophy in the Electronic Engineering program has been performed under their supervision.

Dr. Marc Porti Pujal — Dr. Javier Martín Martínez

Bellaterra, April 2018

In the sciences, the authority of thousands of opinions is not worth as much as one tiny spark of reason in an individual man.

Galileo Galilei

Agradecimientos

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Bellaterra, Abril 2018

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Preface

Over the last years, the information and its analysis have become in the corner stone of growth of our society allowing the sharing economy, globalization of products and knowledge, block-chain technology etc. Huge companies such as: Amazon, Facebook, Google... which were aware of the potential of these resources, are developing vast infrastructures in order to extract as much information as possible about our environment (Internet of Things) or ourselves (social media, smart-phones...), process this information (Big Data Centers) and transmit it quickly all over the world. However, this challenge requires electronic devices with higher performance and low power consumption, which cannot be developed using the conventional scaling techniques because the dimensions of devices have reached the atomic range. In this range of dimensions, the impact of the discrete of matter and charge increases inevitably the variability of devices. Among different variability sources, Interface traps (IT), Random Dopant Distributions (RDD), Line Edge Roughness (LER) and Poly Gate Granularity (PGG) have been identified as the most prominent ones. Consequently, the scientific community is exploring new solutions such as, alternative device materials and/or structures, in order to overcome the different issues owing to the scaling. In this context, this thesis, which is structure in 7 chapters, will try to contribute to solve this problem, analyzing the impact of interface traps and defects on device variability.

In order to introduce to the reader in chapter 1 the charge transport theory through a semiconductor and metal junction (Schottky contact) and the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) device are explained. Besides, the concept of variability and different sources of variability are also presented.

In the second chapter, advanced characterization techniques, such as, Conductive Atomic Force Microscopy (CAFM) and Kelvin Prove Force Microscopy (KPFM) used to obtain nanoscale information are described in detail. After that, the device simulator ATLAS, which is a Technology Computer-Aided Design (TCAD) simulator mainly used in this these, is explained. Here, the models and their limitations to simulate the electronic devices are discussed.

Third chapter is devoted to describe the impact of threading dislocation (TD) defects on the conduction through a schottky contact formed by a III-V semiconductor material (InGaAs) and a metal. Here, different conduction mechanisms, Poole Frenkel (PF) and Thermionic Emission (TE), have been associated to the conduction through areas with TD and without TD, respectively, proving that III-V materials with high density of TD showing higher leakage current.

In chapter four, the development of a simulator called (NAnoscale MAp Simulator (NAMAS)) to generate automatically topography and density charge maps from inputs obtained from CAFM measurements (topography and current maps) of a given sample is explained. From the generated maps, the impact of the oxide thickness and the charge density fluctuations on MOSFET variability is studied.

In chapter five, the impact of interface traps in the gate oxide on device variability is analyzed. Firstly, the impact of interface discrete fixed charges on 65 nm technology MOSFET devices with different dimensions is studied (time-zero variability), where a deviation of Pelgrom's law is proved by experimental and TCAD simulation data. Next, the dynamic behavior of traps is analyzed by TCAD transient simulation in order to estimate their physical parameters of traps from empiric parameters.

Chapter six is devoted to study the performance and power consumption trade-off in Ultra-thin Body and Buried Oxide Fully Depleted Silicon on Insulator (UTBB FDSOI) MOSFET when it is operated in near-threshold voltage. Besides, the impact of traps in gate oxide / channel and in buried oxide / channel interfaces on the performance and power consumption of device is also analyzed.

Finally, in the last chapter of this thesis the more relevant conclusions are highlighted.

Chapter 1.

Fundamentals of devices: Schottky diode and MOSFET

1.1. Introduction

SINCE the invention of the transistors based on solid state (Bipolar Junction Transistor (BJT) in 1947 and the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) in 1960), the electronic industry has experimented an unprecedented growth changing the way people work and live. This growth of the electronic industry has been mainly based on three keys (device scaling, R&D and high demand of more powerful devices), which have led this industry to become one of the most important and profitable around the world. With respect to scaling, the MOSFET device is the best paradigm because not only its parameters improve when it is scaled, but also more devices can be manufactured in the same area leading to better and more complex circuits. This fact led Gordon Moore to enunciate a law, nowadays called ”the Moore's law”, which predict the growth of number of devices in a given area as a function of time. On the other hand, the growth of the electronic industry would not have been possible without the incessant research and development of models, simulators or new technology processes. Finally, the last key of the growth of electronic industry is the high demand of more powerful devices which are more and more necessary in our life to entertain, work, help us in our housework, etc.

The proposal of this chapter is to give a general overview of the main theoretical concepts that are used in this thesis. Firstly, the Schottky diode, which is based on a metal-semiconductor junction, is explained. In particular, how a potential barrier is formed on a metal and semiconductor junction and the current mechanisms used in this thesis are introduced. Then, the basic concepts of MOSFET devices are explained as well as how these devices have evolved introducing different materials (high-k dielectric, III-V semiconductor) or changing their structure (SOI devices). Finally, the main sources of variability to time

zero and degradation mechanism in MOSFET devices are introduced, being their study the mainstream of this thesis.

1.2. Schottky diode: Metal-Semiconductor juntions

The metal-semiconductor rectifying system discovered by Braun in 1874, can be considered one of the oldest semiconductor devices (diode). He observed that the resistance in a chalcopyrite sample depend on the polarity of the applied voltage [1]. However, the behavior of these solid-state devices was not explained until 1931 by Wilson, who developed the first acceptable theory to describe the transport in semiconductors based on the band theory of solids [2]. Eight years later, Schottky using this theory, could explain the rectify behavior of the metal-semiconductor junctions through the formation of a potential barrier [3]. In his honor, metal-semiconductor devices are frequently referred as *Schottky barrier devices*. Another theoretical model known as Mott barrier was developed later, whose calculus complete the description of these kind of junctions for other voltage conditions [4]. These models were further enhanced by Bethe in 1942 to become the *thermionic-emission model* [5]. In the following sections, metal-semiconductor junction are described in detail.

1.2.1. Formation of potential barriers

To understand the formation of potential barriers when a metal contacts a semiconductor, the energy band diagram for three different cases using metals with different workfunctions (ϕ_m) and a n-type semiconductor are shown in figure 1.1, being the upper and lower parts of the figure show the metal-semiconductor system before and after contact, respectively. The analysis for p-type semiconductors would be analogous and therefore it is not shown.

Figure 1.1(a) shows an *accumulation contact* in which the ϕ_m is bigger than the semiconductor work function (ϕ_s). As it can be observed, when both materials are in contact, their Fermi levels (metal (E_{fm}) and semiconductor(E_{fs})) are aligned, being the Schottky barrier near to zero or even negative. In these cases, the electrical behavior is ohmic (i.e. a contact with voltage independent resistance) because the carriers are free to flow through the semiconductor. Figure 1.1(b) shows a *neutral contact*, in which the Fermi levels of the metal and semiconductor are equal, so that, bands are not bent. Finally, figure 1.1(c) shows a *depletion contact*, in which the ϕ_m is lower than ϕ_s creating a potential barrier in the metal-semiconductor interface. In this case, the bands are bent forming a depletion zone (W), where the majority carriers are thrown out.

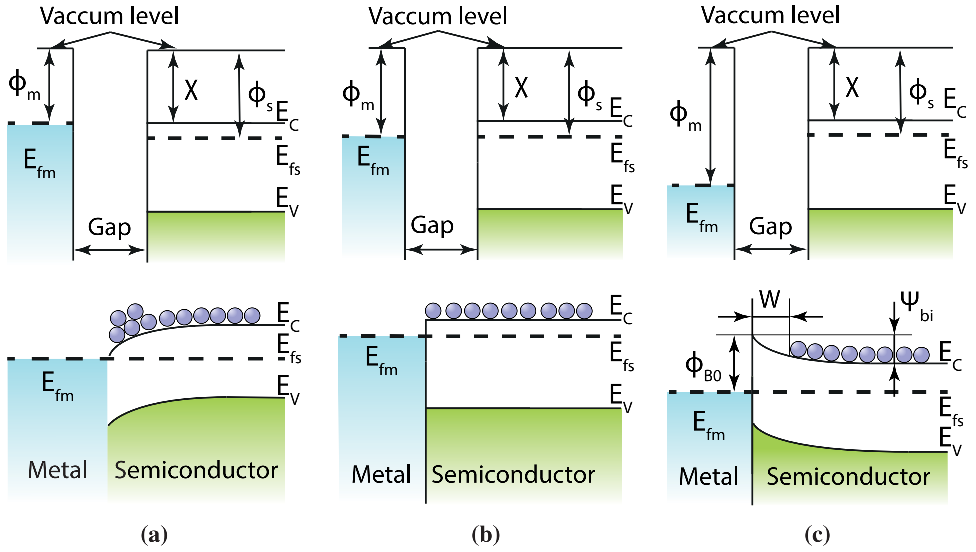


Figure 1.1: Metal-semiconductor contacts according to Schottky model: accumulation contact (a), neutral contact (b) and depletion contact (c). The upper and lower parts of the figure show the metal-semiconductor system before and after contact, respectively.

Due to the matter of the research of this thesis, the case shown in figure 1.1(c) is studied with more detail. Thus, taking as reference figure 1.1(c), the expression to define the potential barrier height (ϕ_{B0}), also known as Schottky barrier height, can be obtained as:

$$\phi_{B0} = \phi_m - \chi \tag{1.1}$$

being (χ) the electron affinity of the semiconductor. Besides, the built-in potential (ψ_{bi}), also known as contact potential, can be written as:

$$\psi_{bi} = \phi_m - \phi_s \tag{1.2}$$

From these equations and assuming that only the carriers with enough thermal energy can flow through the barrier, the rectifying behavior of these junctions can be explained by Thermionic Emission (TE) theory. The carriers flow from semiconductor to metal easier because, the potential barrier height ϕ_{B0} is lower than when the carriers flow from the metal to semiconductor ψ_{bi}, see figure 1.1(c).

Deviations of ideal conditions

Generally, the expressions 1.1 and 1.2 are acceptable as a simple approximation. However, in many cases, the experimental values of the barrier height do not correspond exactly to the predicted values by such equations, because these expresions are not enough to get an accurate description of the junction [6]. The main reasons of the deviations of equations 1.1 and 1.2 are the second-order effects, which are listed below and represented in figure 1.2.

1. **Interface states:** the metal-semiconductor interface has imperfections such as, impurities, incomplete chemical bonds or defects in the lattice which create interface states modifying the barrier height. The barrier height can be increased or decreased depending on the interface state and the semiconductor doping [6, 7].
2. **Interface layer (δ):** As well as interface states in the metal-semiconductor junction, a interface layer of the order of atomic distance (δ) can appear between both materials provoking a potencial drop, and therefore modifying the Schottky barrier [8].
3. **Image-force barrier lowering:** also known as Schottky effect, it modifies the potential barrier at metal-semiconductor junction due to electrostatic attraction between an electron and a metallic surface [9].
4. **Quantum-mechanical tunneling:** it is a mechanism that allows the electrons to go through the potential barrier generating an extra current contribution. This phenomenon is called *tunnel effect* or Field Emission (FE) and its contribution to the total current can become very important when the barriers are low and thin [10]. Although, this phenomenon does not change the barrier height by itself, its current contribution can be comparable to a junction with a lower barrier height.

1.2.2. Charge transport

Once the basic concepts of the metal-semiconductor junctions in equilibrium and without bias has been established, the transport models, when a bias (V_a) is applied, are described. This analysis is focused on the Schottky contact (see figure 1.1(c)) when n-type semiconductor is considered because the analysis to p-type semiconductor is similar.

Schottky or Thermionic Emission Theory

The thermionic-emission theory developed by Bethe is based on the following assumptions:

1. The barrier height ϕ_{B0} is much larger than the product of the Boltzmann constant (k_B) by the temperature (T), k_BT.

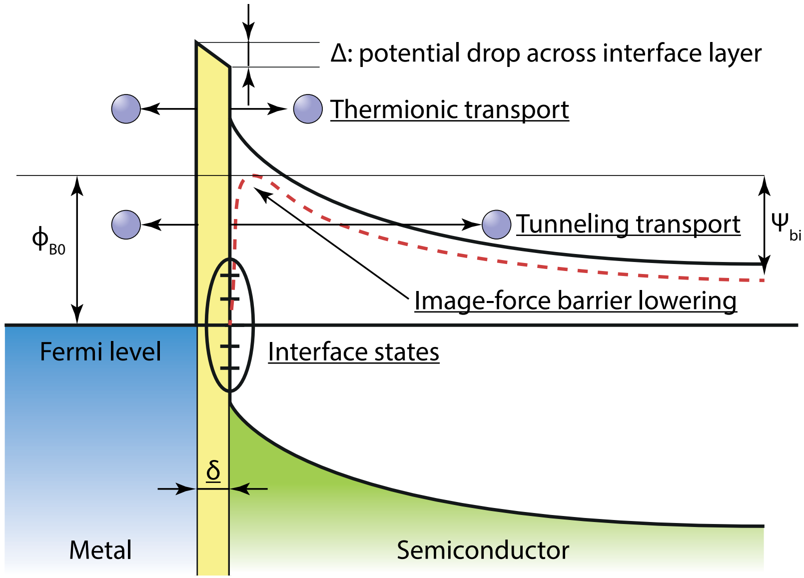


Figure 1.2: Energy-band diagram of a metal-semiconductor junction incorporating the representation of interface states, interface layer, the image-force barrier lowering and the quantum-mechanical tunneling.

2. Thermal equilibrium is established at the plane that determines emission, which is perpendicular to the current flow.

3. The existence of a net current flow does not affect the thermodynamic equilibrium, *quasi-static* condition.

Taking into account these assumptions, the net current through the junction is due to the current contribution of the electrons from the metal with sufficient energies to overcome the Schottky barrier ϕ_{B0} towards the semiconductor, and the electrons from the semiconductor with energies sufficient to overcome the potential contact ψ_{bi} towards the metal, which depend solely of the barrier height and the applied bias. A schematic representation of this mechanism can be seen in figure 1.2, highlighted with the name "Thermionic transport".

In order to quantify the net thermionic current through this junction, taking into account the assumptions explained above, the equation 1.3 was developed. The procedure to obtain this expression can be found in [6, 11].

$$J_{TE} = \left[\frac{4k_B^2 q \pi m_e^*}{h^3} T^2 exp\left(\frac{-(\phi_{B0})}{k_B T} \right) \right] \left[exp\left(\frac{-qV_a}{k_B T} \right) - 1 \right] \tag{1.3}$$

where (J_{TE}) is the thermionic emission current density, (q) is the elementary charge, (h) is the Planck constant and (m_e^*) is the electron effective mass. Assuming that m_e^* is equal to the mass for free electron (m_e), the constant terms can be grouped in one, called Richardson constant (A_0) and whose value is 120 A/cm^{2}K^2 for electrons [8].

$$A_0 = \frac{4k_B^2 q\pi m_e}{h^3} \tag{1.4}$$

For semiconductors with isotropic effective mass in the lowest minimum of the conduction band such as n-type GaAs, relation between the A_0 and a effective Richardson constant (A_1^*) can be expressed by,

$$\frac{A_1^*}{A_0} = \frac{m_e^*}{m_e} \tag{1.5}$$

For multiple-valley semiconductors the appropriate Richardson constant associated with a single energy minimum is given by,

$$\frac{A_2^*}{A_0} = \frac{1}{m_e^*}\sqrt{l_1^2 m_y^* m_z^* + l_2^2 m_z^* m_x^* + l_3^2 m_y^* m_x^*} \tag{1.6}$$

where l_1, l_2 and l_3 are the direction cosines of the normal to the emitting plane relative to the principal axes of the ellipsoid, and m_x^*, m_y^* and m_z^* are the components of the effective mass tensor. Usually the nominal value of Richardson constant can be modified to introduce effects such as the image-force barrier lowering aforementioned [6].

Poole-Frenkel emission (PF)

Poole-Frenkel emission (PF) emission is a conduction mechanism assisted by traps and based on thermal excitation of electrons. In figure 1.3 an schematic energy band diagram of this mechanism is represented showing how the traps can modify the potential barrier in a Schottky contact. The electrons may flow easily through a potential barrier being trapped/emitted from traps that are usually located in the interface between the metal and semiconductor. This mechanism is typically used to estimate currents in Metal-Insulator-Metal (MIM) and Metal-Insulator-Semiconductor (MIS) structures. The measumrement of the current through these structures allows to evaluate the electrical properties in the dielectric films such as; trap energy level, dielectric relaxation time or the density of states in the conduction band. This mechanism, in the same way that TE, is based on the thermal excitation of electrons, but taking into account that the carriers are emitted through the traps of the barrier [12]. Although this mechanism is assumed to occur in MIM / MIS structures,

due to the deviations of ideal conditions of Schottky contacts (see 1.2.1), in many works, these contacts have been studied using the PF equation 1.7 obtaining good agreement with experimental data, [13–15]. PF emission is based on the equation;

$$J_{PF} \propto q\mu n_s E exp\left[\frac{-q}{k_B T}\left(\Phi_t - \sqrt{\frac{qE}{\pi\varepsilon_0\varepsilon_r}}\right)\right] \quad (1.7)$$

where (J_{PF}) is the Poole-Frenkel current density, (Φ_t) is the trap energy level, E is the electric field in the contact, (ε_s) is the relative dielectric constant, (μ) is the the field independent carrier mobility and n_s is the density of states. Usually, q, μ and n_s magnitudes are grouped in a constant whose value can be measured experimentally.

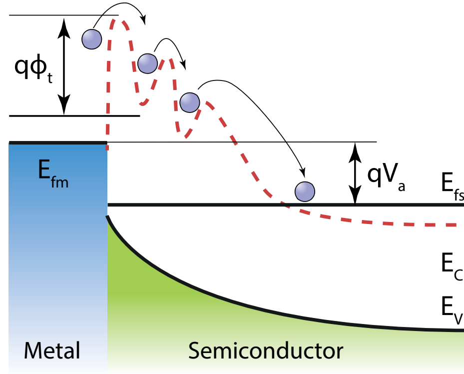


Figure 1.3: Schematic energy band diagram of Poole-Frenkel emission in a non ideal Schottky contact.

1.2.3. Measurement of the barrier height

As shown in section 1.2.1, the barrier height is a critical parameter to estimate the current through contacts. Essentially, there are three methods to measure the experimental value of the barrier height of a metal-semiconductor contact [16]:

1. **Current-Voltage:** from the equations 1.3 or 1.7 (depending on the mechanism under consideration) and using logarithms, the current density expressions can be obtained as a function of 1/T at a fixed-bias voltage (Arrhenius plot). Identifying the y-intercept and slope in the equation 1.8 and 1.9 the barrier height and others parameters can be obtained.

$$ln\left(\frac{J}{T^2}\right) = ln\left(A^*\right) + \left(\frac{-\phi_{B0}}{k_B}\right)\frac{1}{T} \quad (1.8)$$

$$ln\left(\frac{J}{E}\right) = ln\left(\frac{q}{k_B T}\sqrt{\frac{q}{\pi\varepsilon_0\varepsilon_r}}\right)\frac{1}{T} + \frac{-q\Phi_t}{k_B}\frac{1}{T} + ln\left(C\right) \tag{1.9}$$

2. **Capacitance-Voltage measurement:** The barrier height can also be determined by the capacitance measurement. When a small ac voltage is superimposed upon a dc bias, incremental charges of one sign are induced on the metal surface and charges of the opposite sign in the semiconductor. In order to calculate the ϕ_{B0}, 1/C^2 is represented as a function of voltage and the intercept on the voltage axis gives the built-in potential ψ_{bi} from which the barrier height can be determined,

$$\phi_{B0} = \phi_{bi} + \phi_n + \frac{k_B T}{q} - \Delta\phi_{BL} \tag{1.10}$$

   This method is very useful to characterize the doping concentration of semiconductors [17] or the density of interface traps [18].

3. **Photoelectric measurement:** The photoelectric measurement is a direct method of determining the barrier height [19]. It is based on the photocurrent generated when a monochromatic light is incident upon a metal surface. The main advantage of this method is that it allows to estimate the value of the barrier lowering, as well as the dependence of the height of the barrier with the temperature [20]. More details of this method can be found in [6].

In this thesis, the electrical properties of a Schottky contact junction formed by a III-V semiconductor (InGaAs) is studied at the nanonoscale using a Atomic Force Microscopy techniques. In particular, the *current voltage analysis* procedure and the PF and TE conduction mechanisms are considered to the analysis (chapter 3).

1.3. MOSFET device

The idea of modulating the conductance of a semiconductor by the application of an electric field was first described in 1930 by Lilienfeld [21]. However, the first working MOSFET was realized in 1960 by Kahng and Attala [22], being thirteen years later than the first Bipolar Junction Transistor BJT. After this moment, the progress of MOS technology has been exponential leading Gordon Moore to enunciate his famous empiric law, known as Moore's law, which predict the exponential growth of integration density with time [23]. Thus, nowadays, MOSFET is the most widely used semiconductor device and is at the heart of every digital circuit.

1.3.1. Structure of MOSFET device

Figure 1.4(a) shows the schematic of a n-type MOSFET. As it can be seen, MOSFET devices have four electrodes or contacts designated as *gate* (G), *source* (S), *drain* (D) and *bulk* or *substrate* (B). The gate contact is usually made of metal or heavily doped polysilicon and it is separated from the semiconductor substrate by a thin insulator layer, usually formed by an oxide (gate oxide). Silicon oxide (SiO_2) was the first oxide used as gate, whose manufacture was possible by thermal oxidation of silicon. However, during the last years, due to the problems related to the continuous scaling down of the device dimensions, the gate oxide has been replaced by new advanced dielectrics (see section 1.3.3). Finally, the semiconductor substrate is usually made of silicon and it is divided in three regions. The first region called *channel* is under the gate oxide and it is slightly doped with acceptor impurities (P) for n-type devices (see figure 1.4(a)) or doped with donor impurities (N) for p-type devices (not shown). The other two regions are called source and drain, and they are heavily doped with donor impurities (N^+) for n-type devices and acceptor impurities (P^+) for p-type devices. From these two types of device, the Complementary Metal-Oxide-Semiconductor (CMOS) was invented in 1963, where n-MOSFET and p-MOSFET are fabricated side by side on the same substrate and connected in series (see figure 1.4(b)) [24]. Notwithstanding that these devices were slower compared to BJT, MOSFET became most useful for electronic industry because Integrate Circuits (ICs) manufactured using CMOS technology have less standby power dissipation, what meant an advantage when the number of devices integrated on a chip grew [11]. Besides silicon substrates, other materials such as germanium and III-V materials are used for High-Mobility-Channel MOSFET's (see section 1.3.3).

1.3.2. Electrical characteristics

Before explaining the main operation modes of a MOSFET, the working principle of a MOS capacitor will be reviewed when different biases are applied between the gate and bulk contacts. For a to better understanding of the explanation, only a n-substrate device was assumed.

1. **Accumulation:** If a positive bias is applied to the metal gate ($V_{GB} > 0$) while the silicon bulk is grounded, a large number of electrons are attracted to the oxide surface. Therefore, the concentration of electrons in the semiconductor under the oxide is larger than the rest of the bulk. It can be explained from the band theory of solids (see figure 1.5(a)), where the E_{fm} level is pushed downwards bending the conduction band and allowing the accumulation of majority carriers (electrons) in the conduction band.

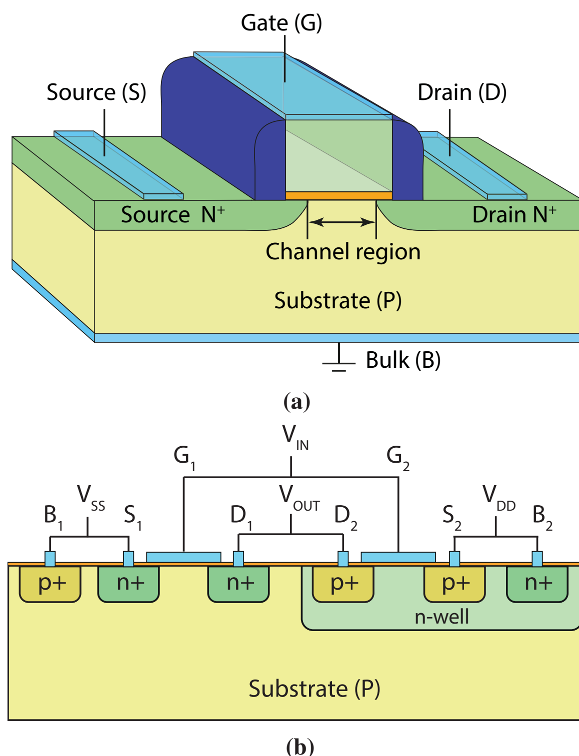


Figure 1.4: Scheme of a n-type MOSFET (a) and cross section of two transistors in a CMOS gate, in an N-well CMOS process (b).

2. **Depletion:** If a slightly negative bias is applied to the gate contact ($V_{GB} < 0$), electrons near the oxide are repelled, depleting the semiconductor under the gate. Since the fixed donor charge remains in the depleting region, this region is charged positively. Figure 1.5(b) shows a band diagram representing the depletion region where there are not any free charges to contribute to current.

3. **Inversion:** If a larger positive voltage is applied to the gate ($V_{GB} \ll 0$) the electron concentration near the surface will continue decreasing while the hole population will increase: free holes (minority carriers in the n-substrate) are attracted near the insulator semiconductor interface creating an inversion layer. Figure 1.5(c) shows the inversion region where free holes can be observed.

Similar behavior can be described for p-bulk MOS structure. However, in order to reach the different operation modes, inverted polarities must be applied. Notice that the behavior previously described corresponds to the ideal situation, which occurs when there is not trapped charge in the oxide and the difference between the metal and semiconductor work-function is close to zero. Unfortunately, this is not the general rule and therefore, more

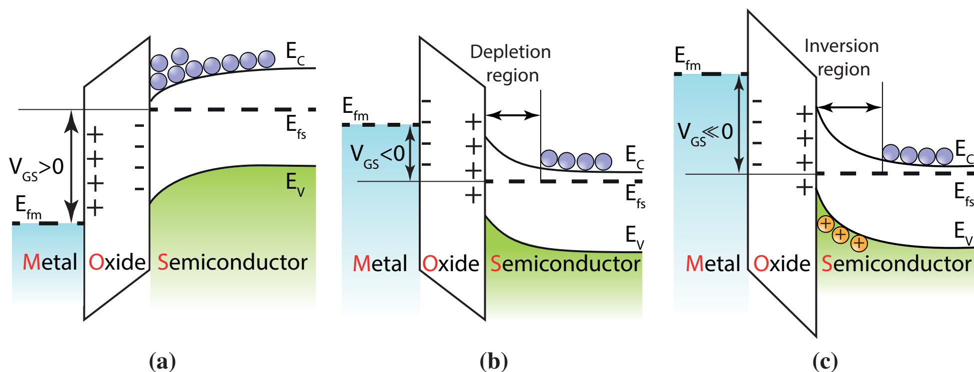


Figure 1.5: Different operation modes of an ideal MOS capacitor: (a) accumulation, (b) depletion and (c) inversion.

realistic situations must be studied to understand the working principle and variability of devices, especially at nano-scales, where little fluctuations can change the electrical behavior of the devices.

From the understanding of the different regimes showed for a MOS capacitor, the working principle of MOSFET and the operation modes are easily understandable. If the source (V_S) and bulk (V_B) contacts are grounded and the drain is biased to a positive voltage (V_D), tuning the gate voltage (V_G) the current through the channel can be controlled. The V_G at which the transition between weak and strong inversion takes place in the MOSFET channel is called (V_{TH}). Thus, controlling the gate and drain voltage three operation modes can be observed.

1. **Cut-off or weak-inversion mode:** if $V_G < V_{TH}$ is applied, the inversion layer under the gate is not created and therefore the source-to-drain contacts correspond to two p-n junctions connected back to back. Therefore, transistor is turned off. There is a minimum conduction between source and drain I_{DS} even when a V_D is applied.

2. **Linear region or ohmic mode:** when a sufficiently gate bias is applied $V_G > V_{TH}$ to form a inversion layer between the source and drain contact and the drain voltage is $V_D < (V_G - V_{TH})$ the current transport has a behavior that is similar to a resistor. Besides, the conductance of this channel can be modulated by varying the gate voltage.

3. **saturation or active mode:** if $V_G > V_{TH}$ and $V_{DS} > (V_G - V_{TH})$, the channel is ”pinched off” at the drain end. It occurs because the relative voltage between the gate and the semiconductor is reduced. The drain voltage and the drain current, which saturates, at this point is designated as V_{sat} and I_{sat} respectively. Thus, beyond the pinch-off point, the current remains almost constant independently of V_D.

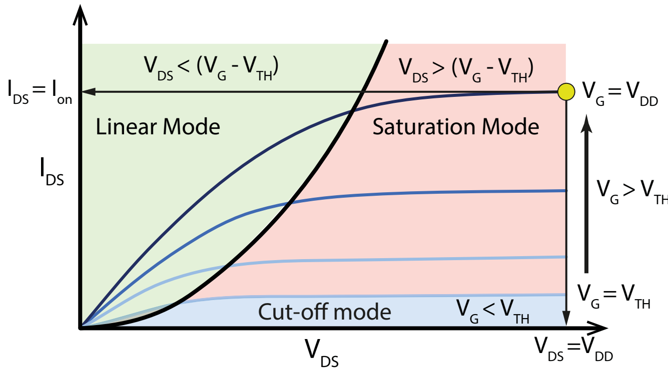


Figure 1.6: MOSFET output characteristics. Different operation modes can be observed depending on bias applied.

Regarding the I-V curves showed in figure 1.6, different parameters to define the performance of a MOSFET device can be established. In this thesis, V_{TH}, (I_{on}) and (I_{off}) will be considered more in detail due to the matter of the studies performed. In order to estimed V_{TH}, there are numerous methods to extract this parameter, being one of the most used; *constant-current method*, *extrapolation in the linear region method* or *transconductance extrapolation method in the linear region* [25]. In the different studies included in this thesis, V_{TH} was mainly calculated as degradation parameter of the devices, and the method used to extract V_{TH} was the *constant-current method*. Moreover, I_{on} and I_{off} were analyzed as important parameter for applications in digital circuits, being the I_{on} the current measured through device at $V_G = V_{DD}$ and $V_{DS} = V_{DD}$ and the I_{off} the current measured at $V_G = 0$ and $V_{DS} = V_{DD}$.

1.3.3. Advanced materials of MOSFET: high-k insulators and III-V materials

Until the end of the 20st century, devices were scaled following the conventional theory [26, 27]. However, since this moment, the voltage was not scaled as fast as the dimensions, leading to an increasing of the electric field in the devices. Besides, the more advanced technology nodes started to experiment quantum effects and Short-channel Effect (SCE) related to their small dimensions. In order to overcome these new challenges and achieve the scaling goals many solutions were proposed. For instance, the substitution of the gate SiO_2 by high-k oxides to avoid leakage currents due to tunneling effect [28, 29], the introduction of other semiconductor substrates as III-V materials that allow a better performance of devices [30]

or 2D materials... graphene, phosphorene... [31, 32]. In this section, the implementation of high-k materials in advanced technology nodes is explained. Besides, the current challenges of this materials are dealt, proposing new methodologies to study them. On the other hand, a brief overview of III-V materials in MOSFET devices is explained. In particular, structural defects called (Threading Dislocations (TDs)) in these materials is introduced, suggesting the use of nanoscale techniques (Conductive Atomic Force Microscopy (CAFM) to analyze them.

High-k insulators

The replacement of SiO_2 layers for high-k dielectrics allows to reduce the leakage current through gate oxide, keeping constant the capacitance per unit area. It is possible because high-k materials have equivalent performance than SiO_2 using a larger physical thickness [33, 34]. Figure 1.7 shows how the leakage tunneling current is reduced using high-k dielectrics, taking into account that both MIS structures have the same capacitance.

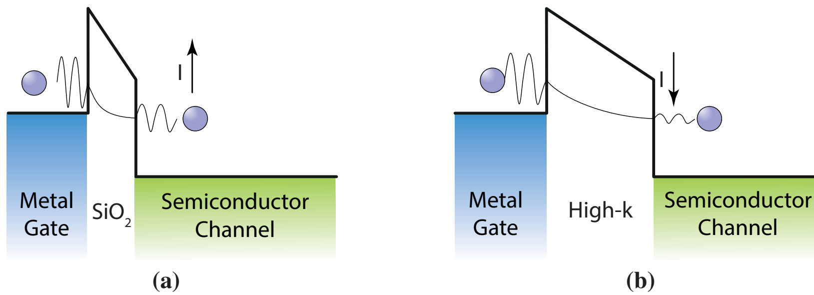


Figure 1.7: Band diagram when SiO_2 (a) is substituted by a high-k dielectric (b) with same capacitance, using a larger thickness, which leads to a reduction of the leakage current.

To compare the electrical behavior of high-k dielectrics to SiO_2, the Equivalent Oxide Thickness (EOT) parameter was defined as the equivalent thickness of a SiO_2 layer needed to obtain the same capacitance than the one obtained by the high-k dielectrics (equation 1.11),

$$EOT_{high-k} = th_{high-k} \frac{\kappa_{SiO_2}}{\kappa_{high-k}} \tag{1.11}$$

where (κ) and th are the dielectric constant and physical thickness, respectively, of the materials indicated in subscript (high-k and SiO_2). Therefore, high-k dielectrics provide two primary advantages: they offer a significant gate leakage current reduction and have potential to provide significantly lower EOT values allowing the use of lower gate voltages [34].

However, although many high-k materials have been studied as candidates to substitute SiO_2, such as, ZrO_2, Al_2O_3, LaZrO or La_2O_3 [35–37], it has not been easy to find a good candidate. Despite of having high dielectric constant, high-k materials must satisfy other requirements [35], such as;

1. To have a large energy band gap to avoid excessive leakage current.
2. The defect density should be low at Si/dielectric interface to provide high mobility of carrier in the channel.
3. High-k materials should be compatible with CMOS processing, overall getting good thermal stability.

Finally, the semiconductor industry found a good candidate based on hafnium (HfO_2) with $\kappa \sim 20 - 25$. The 45 nm technology node was the first CMOS generation with high-k gate dielectrics and metal gate electrodes were used (HKMG), being the high-k stoichiometric formula $HfSi_xO_y$ [38, 39]. But even HfO_2, which has been integrated successfully in advanced technology nodes [40], has drawbacks due to its polycrystalline morphology. This phenomenon was widely studied using CAFM techniques by REDEC group [41, 42]. Figure 1.8 is one of the examples reported in [43], which shows the polycrytaline surface and the correlation between topography 1.8(a) and current 1.8(b) obtained at V_G = 6.5 V on a HfO_2/SiO_2/p-Si structure. This report highlighted the high surface variability in these kind of oxides, which could be translated to the performance of electronic device.

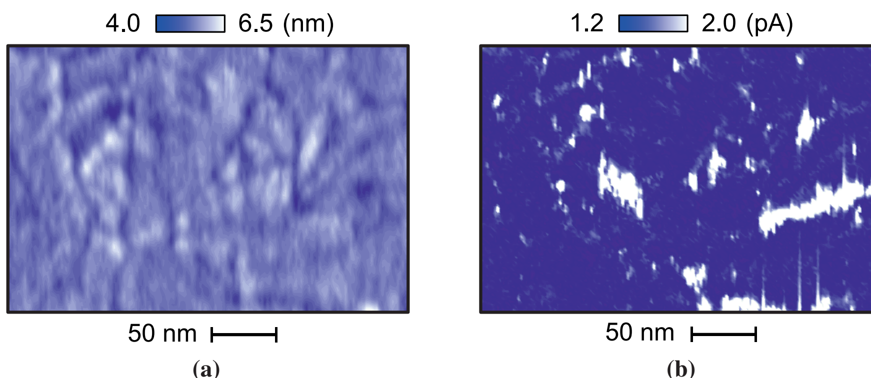


Figure 1.8: Topography (a) and current (b)CAFM maps examples of polycystalline structure of HfO_2.

From these previous works, in this thesis a methodology to extract quantitatively the charge density distribution and to evaluate the impact on the variability of electric device parameters such as, V_{TH}, I_{on}, I_{off} due to polycrystalline morphology of the hafnium oxide has been developed (chapter 4).

III - V materials

One of the first studied III-V semiconductors was GaAs in 1929 by Goldschmidt [44]. However, until 1952 the GaAs was not identified as a semiconductor by Welker. The first device exploiting the direct band-gap of GaAs dates from 1962, when Hall [45] and Redhiker [45], independently, obtained the first semiconductor laser. In the same year, Gunn (IBM) discovered the transferred electron effect and developed the first solid state microwave oscillator [46]. During the next decades, many III–V compound semiconductors were developed, such as AlAs, InAs, InP and their ternary and quaternary alloys, combining elements in columns III and V of the periodic table to have unique optical and electronic properties. Due to their efficiency to emit and detect light, they are often used in lasers, light-emitting diodes, detectors for optical communications, instrumentation and sensing. Besides, some of them (GaAs, InGaAs and InAs) exhibit outstanding carrier transport properties [30]. Figure 1.9 shows a comparison of electron mobility among several III-V materials, silicon and germanium substrates. As it can be observed, the electron mobility of InGaAs or InAs is more than 10 times higher than in silicon at a comparable sheet density.

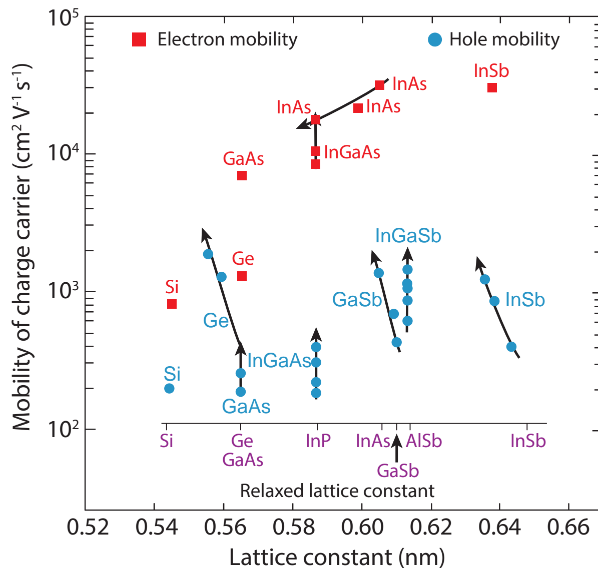


Figure 1.9: Electron and hole mobility for several semiconductor as a function of the lattice constant. No strain lattice are indicated in the bottom part. This figure has been extracted of [30].

However, manufacturing high quality substrates of III-V materials may involve growing over a Si substrate, and due to the lattice mismatch between these materials, the growth of III-V materials tend to develop a significant density of structural defects [47]. These

kind of defects in III-V semiconductors have demostrated to be the dominant source of high leakage currents at room temperature. In particular TDs [48, 49], increase the device-to-device variability due to the formation of multiple parallel paths with different conductivity [50]. Therefore, understanding the main conduction mechanisms through the defects is an important step to improve the behavior of the III-V semiconductor materials. In chapter 3 of this thesis, the defects in InGaAs are studied at the nanoscale using AFM techniques.

1.3.4. Further than conventional MOSFET device

One of the keys in the growth of the semiconductor industry during the last 50 years has been the continuous scaling of devices following a geometrical law [51, 52]. Each time, the minimum line width is reduced creating new technology nodes, as for instance, the technologic nodes of 90 nm, 65 nm, 45 nm, 28 nm, 14 nm... where the number indicates the minimun metal line width [53]. In addition, these scaling techniques have led to an increase of the switching speed and transistor density exponentialy [54, 55]. Therefore, the scaling has been considered as the microelectronic revolution, but can it go on forever?

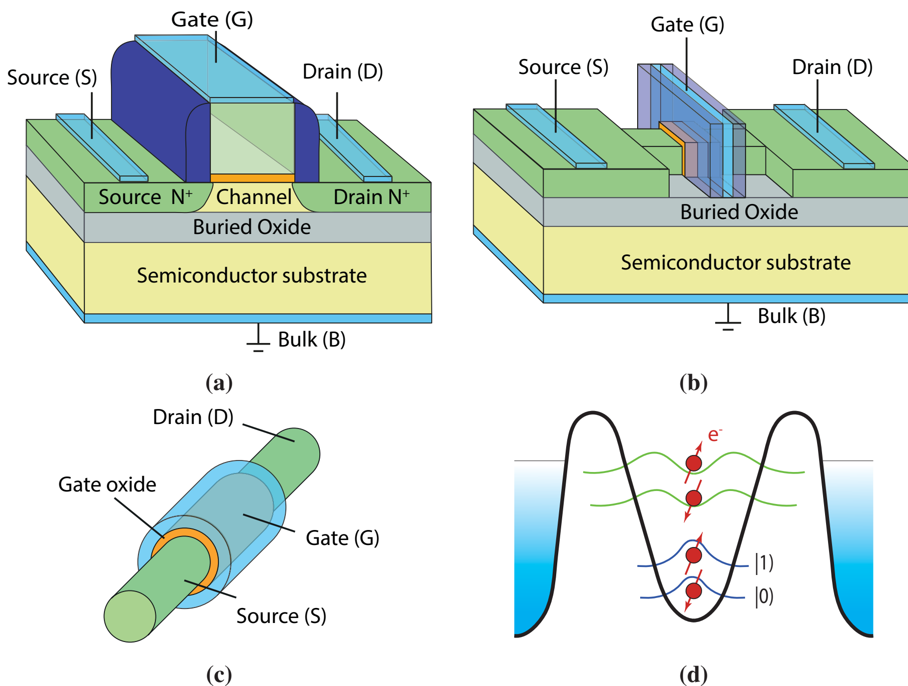


Figure 1.10: Several alternative devices to conventional MOSFET: (a) single gate Ultra-thin Body and Buried Oxide on Insulator Fully Depleted MOSFET(UTBB FDSOI) transistor, (b) trigate Fin Field Effect Transistor (FinFET), (c) Nanowire (NW) transistor and (d) Quantum Dot (QD) well.

One of the most important research lines in order to continue the scaling is to develop alternative structures to conventional MOSFET. Figure 1.10 shows some examples of these promising devices, such as: Ultra-thin Body and Buried Oxide Fully Depleted Silicon on Insulator (UTBB FD-SOI) MOSFET, trigate Fin Field Effect Transistor (FinFET), Nanowire (NW) transistor or Quantum Dot (QD) well. In this thesis, the variability of parameters of UTBB FD-SOI MOSFET inverter gate is studied by Technology Computer Aided Design (TCAD) simulators. For this reason, this device is explained in the following section.

UTBB FD-SOI MOSFET

With the exception of Silicon-on-Sapphire (SOS), which was first introduced in 1964, the development of Silicon-on-Insulator (SOI) technology can be situated around 1980. At first, the purpose of these devices was very limited to some aerospace and military niche markets due to its high radiation tolerance [56]. However, at the beginning of 21th century, the quality of SOI wafers improved sufficiently to manufacture SOI devices to be used in commercial microprocessors [57]. Nowadays, SOI technology is quickly evolving to provide devices, whose main competitive advantage is the low power consumption, because the stagnant of supply voltages (V_{DD}) is leading to a dramatic increase of the power density and energy consumption of the chips [58]. Moreover, emerging applications, as Internet of Things (IoT) demand strongly devices that do not need a high performance but their energy consumption must be as low as possible. In particular, the UTBB FD-SOI MOSFET devices, when are biased in near-threshold voltage Near-Threshold Voltage (NTV) [59], are taken advantage to become one of the most used in IoT revolution [60–63]. Another advantage of UTBB FD-SOI MOSFET technology is that their manufacture involves similar processes than a conventional MOSFET, being the main difference between them a buried SiO_2 layer which separates the silicon channel and the bulk. Figure 1.10(a) shows an example of this kind of device. Other inherent advantages of SOI devices over bulk CMOS are listed below [11].

1. **Low junction capacitance:** The source and drain junction capacitance is almost entirely eliminated because capacitance through the thick buried oxide layer to the substrate is very small.
2. **No body effect:** The threshold voltage of stacked devices in SOI is not degraded by the body effect.
3. **Increased voltage range:** UTBB FD-SOI MOSFET gives a higher performance for the same power consumption thanks to the better behavior of transistors at low operation voltage than the bulk technology. For this reason they are good candidates to operate in the NTV [58].

4. **Robustness against process variability:** Random Dopant Fluctuation (RDF) is suppressed because the threshold voltage adjustment does not require channel doping [62, 64].

These devices are presented as good candidates to be used in low power consumption applications in IoT. However, when they are operated using low gate voltage, silicon/oxide interface trapped charge in the gate or buried oxide can impact critically on electrical parameters of the devices generating variability. Therefore, the understanding of this variability source and how they affect to energy consumption of circuits is mandatory for developing new technology devices (chapter 6).

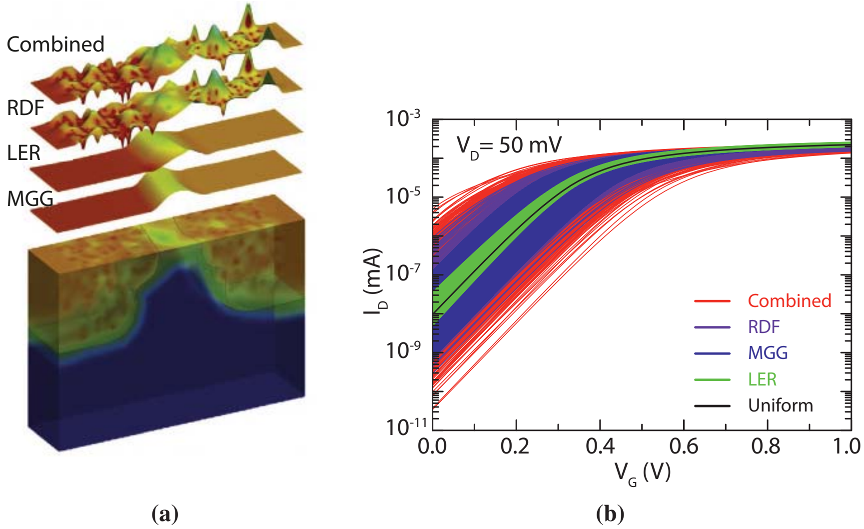
1.4. Ultra-scale device variability

One of the most important features of ultra-scale CMOS technology is its increasing of variability of the main electrical parameters of devices such as: V_{TH}, I_{on}, transconducntace, which impacts directly on the performance of Very Large Scale Integration (VLSI) circuits [65]. Variability sources are typically classified in two types; intrinsic sources realated to random variability of wafer fabrication processing steps [66, 67] called *time-zero variability* and *time-dependent variability*, understood as the variability associated to how the devices are degraded when they are working on operation voltage [68, 69].

1.4.1. Time-zero variability

Time-zero variability can be grouped as stochastic and systematic variability. The stochastic variability is defined as a local process variability that provokes parametric fluctuations or mismatch between identically designed devices. On the other hand, systematic variability is defined as a global process variability causing a shift in the mean value of the sensitive design parameters, including the dimensions of device: length (L), width(W) or thickness of gate oxide (T_{OX}), as well as the Doping concentration (N_a), and so on [65]. Although both variability contributions have been studied for a long time, since 45nm technology node, stochastic variability contribution was more studied because its impact on device varibility is more dominant due to its impat on the electrical parameters as V_{TH}, I_{on}, I_{off}... [70]. The major sources of stochastic variability in advanced CMOS technologies include RDF, Line-Edge Roughness (LER), Line-Width Roughness (LWR), Poly-silicon Gate Granularity (PGG) and Metal Gate Granularity (MGG) as is shown in [66, 67, 71, 72]. Figure 1.11(a) shows a statistical study of simulated devices in which different sources of variability were included. As it can be observed, the contribution of different variability sources are summed

as independent statistical variable (combined), obtaining finally a good approximation of the global behavior of devices 1.11(b).



(a) (b)

Figure 1.11: Electron density of simulated in a bulk device showing the combination of RDF, LER and MGG (a). I_D-V_G curves for the different sources of variability (b). Figures obtained from [73].

In summary, due to the atomistic nature of matter, it is impossible to reduce completely the statistical variability, even in a hypothetical "ideal" fabrication processes where process and systematic variability are absent. Therefore, to minimize the impact of the variability on transistors and circuits is mandatory to study this phenomenon statistically from the nanoscale to circuit level.

Area dependence: the Pelgrom's law

In 1989, Marcel J. M. Pelgrom demonstrated that the time-zero variability of electrical parameters such as V_{TH} of MOS transistors has a dependence with the area of device [74]. In particular, this relation, known as Pelgrom's law, establishes that the time-zero variability of threshold voltage is inversely proportional to square of device active area, as it is shown in equation 1.12.

$$\sigma(V_{TH}) = \frac{A_{TH}}{\sqrt{W \cdot L}} \tag{1.12}$$

where $\sigma(V_{TH})$ is the variability of V_{TH} and A_{TH} is a constant related to the device technology.

This relationship was found assuming that the device-to-device mismatch is the result of several random processes (sum of all sources of time zero variability) which occur during the fabrication phase of the devices [74]. This relationship worked quite well for technology nodes developed until beginning of XXI century. However, significant deviations from this rule were reported on experimental data in 65 nm technology node and beyond [75–77]. In these works RDF, interface traps or SCE were pointed out as the origin of this mismatch, nevertheless it has not been fully clarified yet. In this thesis, a new explanation of the origin of the mismatch of the Pelgrom's law is described, since experimental and simulation data.

1.4.2. Time-dependent variability

Unlike time-zero variability, whose origin derives from the fabrication process, time-dependent variability is due to the degradation that the devices experiment during their operation time. Although the time-dependent variability has been studied since several decades ago [78], nowadays, it has became to cause researchers concern due to aggressive scaling in device dimensions [79, 80]. This scaling has led devices to operate under extremely high electric fields, increasing reliability problems to the long-term operation of the device. The degradation depends mainly on operation time, the applied operating conditions and the temperature. Depending on this operating conditions or nature of the phenomenon, different mechanisms have been described in literature, such as, Bias Temperature Instability (BTI), Random Telegraph Noise (RTN), Hot Carrier Injection (HCI) and Time-Dependent Dielectric Breakdown (TDDB) [69, 80–83].

Bias Temperature Instabilities (BTI)

BTI is a degradation mechanism characterized mainly by the increase of the V_{TH} in MOSFET devices. In order to study this mechanism, the degradation is usually induced by a *stress voltage* (V_s) applied during a time, called *stress time*, (t_s) in the gate contact while the other contacts are connected to ground. Besides, the device recovery can be also studied by measuring I_D-V_G curves a determinated time, called relaxation time t_r, after the stress. Figure 1.12 shows an usual BTI degradation in the I_D-V_G curves measure just after the stress (t_r = 0) of a pMOS device, which has experimented several degradation processes ($\mid V_s \mid$ = 2.1 V for different t_s = 100, 1000, 10000 s). Note that V_{TH} increases at the stress processes. For this case, the BTI degradation is called *negative* BTI or NBTI because the working polarization of gate contact for p-type device is negative, and for positive polarization (n-type device), the name is *positive* BTI or PBTI.

Nowadays, there are several physical models to explain the BTI and its dependence with

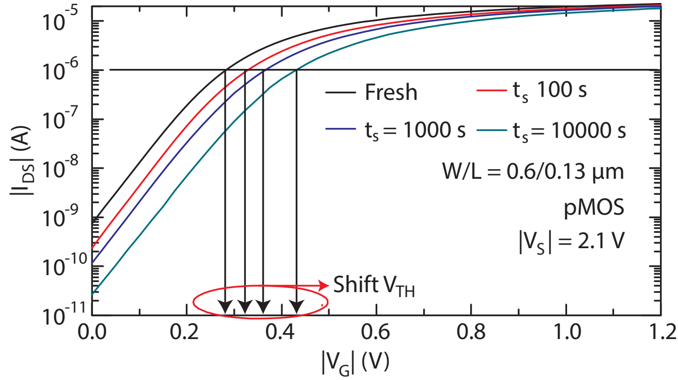


Figure 1.12: Characteristic curve shift after serveral NBTI stresses with different times (0, 100, 1000, 10000 s) and a constant stress voltage V_s = 2.1 V.

the temperature and the relax and stress time [84–86]. In spite of their differences, all of them have in common that the cause of this phenomenon is due to the charge/discharge of traps localized in the gate oxide and/or in the interface oxide/bulk. When these traps are charged, they create a barrier that can hinder the electron transport along the channel, reducing of drain current [87]. This reduction in the drain current can be also measured as a increasing of V_{TH}, being this parameter extensively used in the models of BTI degradation [84–86].

In particular, in this thesis, the assumptions of Probabilistic Defect Occupancy (PDO) model [86] are considered. PDO model describes the shift of the V_{TH} (ΔV_{th}) in a MOSFET device when a BTI stress (V_s) is applied in a certain time, called stress time (t_s), or when following a stress time, the device come back to previous bias state (V_r) in a certain time, relaxation time (t_r). This model assumes that each device has a number of defect (N), and when they are charged/discharged provokes a shift of the V_{TH} (η), which is different for each defect [86]. Besides, each defect has associated a emission time (τ_e) and capture time (τ_c), which are the average times that a defect takes discharged and charge respectively. From these assumptions, the equation of PDO can be written as,

$$\Delta V_{th}(t_s, t_r) = N < \eta > \int_0^{\infty} \int_0^{\infty} D(\tau_e, \tau_c) P_{occ}(\tau_e, \tau_c; t_s, t_r) d\tau_e d\tau_c + P_p \qquad (1.13)$$

where N is the number of defects, $< \eta >$ is the average of shift of the V_{TH} when the defects change their state, D is the distribution of defects for each τ_e and τ_c and P_p is called permanent part, which it is associated to charged defects whose emission time are much larger than the times measured in the lab and therefore they seem permanent charged. Notice

that this thesis is focused on ultra-scaled devices, where instead of the impact of defect distributions D, the impact of individual traps on variability device is evaluated. Figure 1.13(a) shows a typical defect distribution, which is integrated in equation 1.13 to evaluate its impact on the V_{TH}. On the other hand, figure 1.13(b) represents the dynamic behavior of only one trap (charged or discharged) and whose value impacts on the V_{TH} in the ulta-scaled devices.

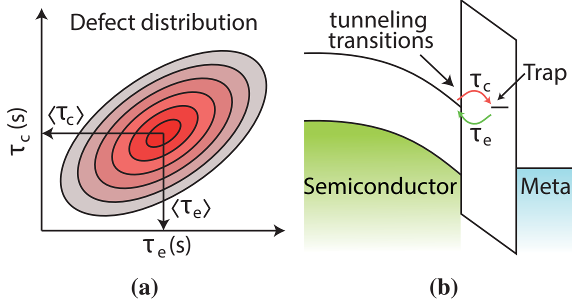


Figure 1.13: Example of defect distribution in a bidimensional graph ($\tau_c - \tau_e$) (a). Dynamic behavior of a trap where emission τ_e and capture τ_c times are highlighted (b).

Finally, P_{occ} is the occupancy probability for each defect which depend on τ_e,τ_c, t_s,t_r, being its expression,

$$P_{occ}(t_{r/s}) = P_{occ}(t_i) + \left(\frac{\tau_e(V_{r/s})}{\tau_e(V_{r/s}) + \tau_c(V_{r/s})} - P_{occ}(t_i)\right) \left(1 - exp\left(\frac{t_i - t_{r/s}}{\tau_{eff}(V_{r/s})}\right)\right) \tag{1.14}$$

where (t_i) is the initial time and $\tau_{eff}(V_{r/s})$ follows the next expression,

$$(\tau_{eff}(V_{r/s}))^{-1} = (\tau_e(V_{r/s}))^{-1} + (\tau_c(V_{r/s}))^{-1} \tag{1.15}$$

the term $V_{r/s}$ indicates that the values τ_{eff}, τ_c and τ_e correspond to the stress voltage (V_s) or the relaxation voltage (V_r). Figure 1.14 shows an schematic representation of a pristine device during a BTI stress (t = 0). When a stress voltage (V_s) is applied to the gate contact, the occupancy probability of traps in the oxide rises. The effect of the charged traps, as it was explained previously, can be modeled as a device V_{TH} increase. After this perturbation, gate voltage is reduced to (V_r) and the charged traps in the oxide gradually are discharged (occupancy probability of traps in the oxide decreases) and the system is returning to the previous equilibrium, recovering partially or totally the V_{TH} level.

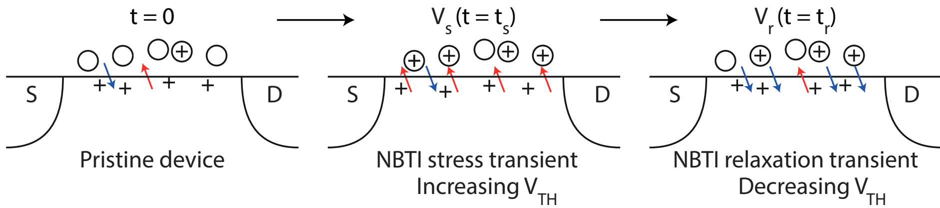


Figure 1.14: Schematic representation of NBTI phenomenon.

Random Telegraph Noise (RTN)

As it has been explained the variability increases when the devices become smaller and smaller, to the point that the impact of charge and discharge modifies significantly the electrical parametres of devices. In particular, the phenomenon, called RTN, is characterized in MOSFET devices by random fluctuations between discrete levels of drain current (I_d), when the gate and drain contacts are biased to a constant voltage (generally close to V_{TH}) while the other contacts are grounded [83, 88]. Figure 1.15(a) shows a experimental RTN signal obtained pMOS device of technology 65 nm [89], where six discrete levels can be observed. Since the relation between current levels and the number of traps given by $N_{levels} = 2^{N_{traps}}$ [90], three different traps with similar emission and capture times each one of them are identified. Figure 1.15(b) represents the schematic top view (upper) and front view (lower) of three traps in a MOSFET device. When they are charged, they hinder the transport of carriers through the channel, depending mainly on their *depth* within the gate oxide and their location along the channel *length* and *width* [91], and therefore less level of current in the drain is obtained.

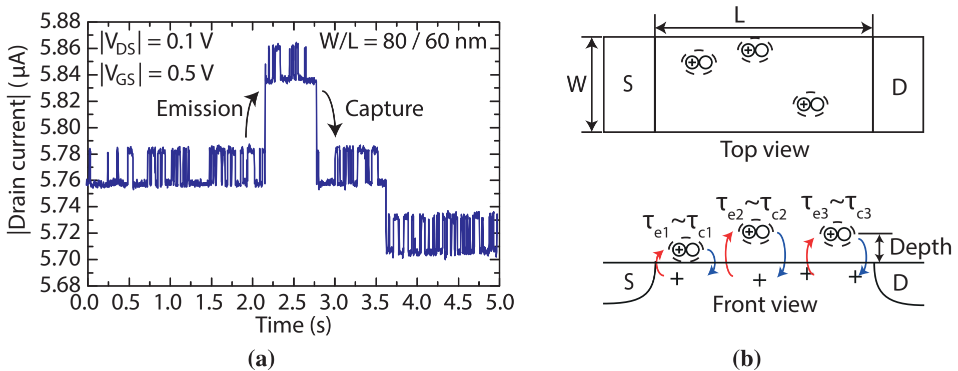


Figure 1.15: Experimental RTN signal obtained to $|V_{DS}| = 0.1$ V and $|V_{GS}| = 0.5$ V in a PMOS device (a) [89]. Schematic representation of NBTI phenomenon (b).

As it has been shown, RTN is an intrinsically stochastic process that varies the device

V_{TH} over time, but also is different from device to device, because the number of device defects in a set of devices is statistically distributed following a Poisson distribution [92], the V_{TH} shift (η) associated to each defect is exponential or weibull distributed [93] and the emission and capture times are widely distributed, covering several time decades [91]. Therefore, this phenomenon as well as BTI are widely studied in order to evaluate its impact on the circuit functionality. In particular, in this tesis, the occupancy probability for only one defect is analyzed in detail in order to relate the parameters τ_c and τ_e, whose values can be obtained experimentally [94], to physical parameters of the trap, such as E_{trap}, σ_{trap}, being the energy level and the effective cross section of the trap respectively (chapter 5).

1.4.3. Variability further than device scale

Nowadays, in this direction there are projects, such as RELAB [68] or SyRA [95], focus on extract information about variability mechanisms in the nanoscale to extend this information until circuit level as it is shown in figure 1.16. On this way, IC designers can introduce suitable countermeasures into the fabrication processes, device architecture and/or circuit design to manage the inherent trade-offs in prediction and protection of system functionality.

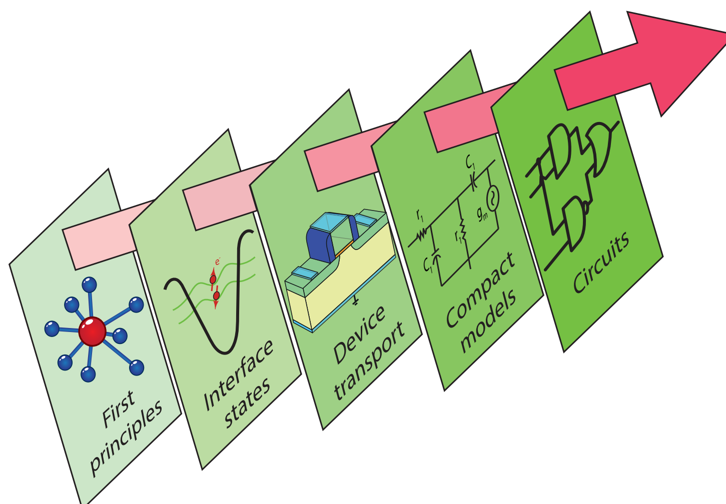


Figure 1.16: Schematic representation that how the information is propagated up to circuit design.

Chapter 2.
Experimental and simulation tools

2.1. Introduction

ONCE the theoretical background has been explained in the chapter 1, in this chapter, the main experimental techniques and the simulation tools used in this thesis are described. Firstly, the experimental techniques, in particular, the Atomic Force Microscopy (AFM) and the associated related techniques, such as; CAFM and the Kelvin Probe Force Microscopy (KPFM) are described in detail. Then, the TCAD tool used to perform device simulations is explained. Finally, an overview about how the experimental data are introduced in the device simulations is expounded.

2.2. Nano-scale characterization tool: AFM

Due to the ultra-reduced dimensions reached by current transistors, inhomogeneities and micro-structural defects associated to the discrete nature of matter and charge could have a strong impact on the global behavior of the device, and for this reason, they must be taken into account and studied [96, 97]. In fact, these local fluctuations in VLSI technology are intimately related to the main sources of variability describe in the previous chapter. Therefore, considering that these phenomena occur at the nano-scale, macroscopic analyses or standard characterization techniques are not suitable/enough to study them. Thus, measurement techniques with high lateral resolution such as AFM, which resolution is at the same scale as the material inhomogeneities, become indispensable for a better undestanding of these phenomena [42, 43].

AFM technique, in contrast with conventional microscopy, does not use light to create the images, but the images are created using the data obtained when an extremely sharp tip at the end of a cantilever scans the sample surface [98, 99]. Its work principle is based on the measurement of the interaction forces that appear between the tip and the sample when

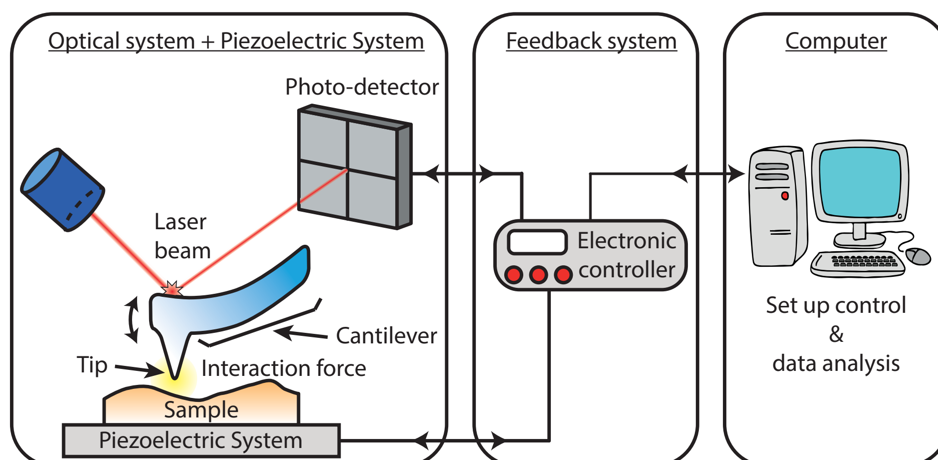


Figure 2.1: AFM schematic representation which can be divided in four parts. First one is the optical system, that is used to detect the cantilever deflection when the tip contacts the surface. Second part is the feedback system, which controls piezoelectric system (third part), moving the sample according to the received data of photo-detector. The last part consists in a computer, where a software sets up the experimental parameters and receives the surface data.

the distance between both is at the nanometric range. These kind of tools requires a complex control system, and generally it is formed by four parts; *optical system*, *feedback system*, *piezoelectric system* and *computer*. Figure 2.1 shows an AFM schematic representation with their main components. The *optical system* consists of a laser which is reflected on the back of the cantilever and a photo-detector to collect the reflected laser beam. The photo-detector has four side-by-side photo-diodes that allows measuring the vertical and lateral deflections of the cantilever when interaction forces between the tip and the sample surface appear. Once the tip is at a certain distance of the sample, the piezoelectric system starts scanning the surface. The feedback system moves (depending on the roughness of the sample) the tip up or down in order to hold constant the distant between the tip and sample. Finally, from the feedback system information, a 3D image of the sample surface can be obtained by a software in a computer. In addition, depending on how the tip interacts with the sample three different operation modes can be defined; contact mode, non-contact mode and tapping mode [100–102].

2.2.1. Conductive Atomic Force Microscope (C-AFM)

The CAFM technique goes one step further than AFM technique, allowing the measurement of topography and electrical conductivity simultaneously, and therefore, the spatial char-

acteristics of the sample can be correlated with its conductivity. Moreover, this technique allows to measure voltage-current curves in specific points of the sample with an area of the order of 100 nm^2, what is appropriated to analyze electrically nanoscale structures with high accuracy. However, to use this technique, conventional AFM must be additionally equipped with, a conductive tip, a voltage source and a very low noise preamplifier, see figure 2.2.

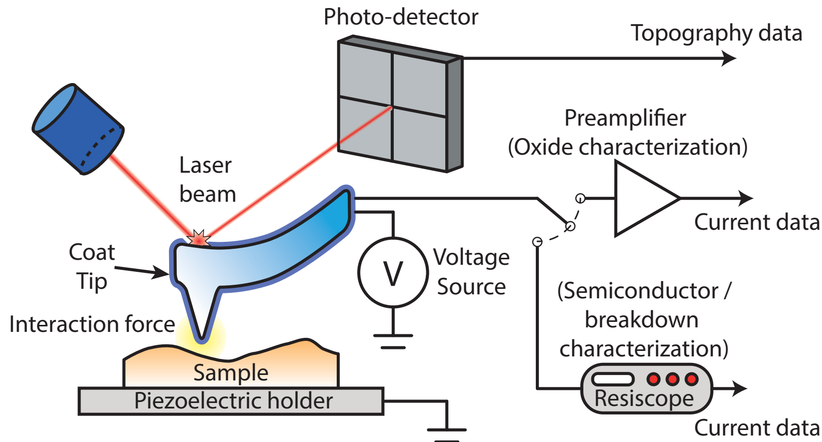


Figure 2.2: CAFM schematic representation. Different setups (preamplifier and resiscope module) used in this thesis to characterize semiconductor and oxide are represented.

Conventional tips for AFM measurements are manufactured of Si or N_4Si_3 and they are not conductive. In order to manufacture conductive tips for CAFM, usually they are covered with a metallic alloy or diamond. Another option is to manufacture tips entirely with a conductive material [103, 104]. The voltage source is used to force a current through the sample whose value is measured using the high quality preamplifier.

CAFM technique is widely used to study the electrical properties of gate oxides, semiconductors and 2D materials. However, the conventional preamplifiers are limited approximately to 3 orders of magnitude (pA to nA), which represents a problem to study conductive samples or breakdown phenomena. In order to extend this range, an extra module called Resiscope (see figure 2.2) is added to the CAFM [105]. With this setup it is possible to get I-V spectroscopy curves for each measured point as well as current maps over 10 decades with a high sensitivity and resolution. In this thesis, the conventional CAFM preamplifier was used to analyze the electrical properties of a HfO_2 sample (chapter 4). In addition, I-V spectroscopy curves were performed to evaluate the electrical properties of TDs in InGaAS (chapter 3).

2.2.2. Kelvin Prove Force Microscope (KPFM)

Developed in 1991 by Nonnenmacher, the KPFM is a noncontact variant of AFM, which allows measuring the contact potential difference (CPD) between the tip and surface simultaneously to the topography [106]. In particular, KPFM detects the difference between the tip and the sample surface work function. This parameter is related to many surface phenomena, including reconstruction of surfaces, doping and band-bending of semiconductors or charge trapping in dielectrics [107]. Therefore, KPFM can provide complementary information to that measured with a CAFM.

Figure 2.3 shows the energy band diagram of the sample and AFM tip for 3 cases to explain the working principle of KPFM. Figure 2.3(a) shows two metals (tip and sample) without electrical contact between them. It can be seen there is a difference between the workfunction of both materials (V_{CPD}). When tip contacts electrically the sample, the electrons of the metal with higher workfunction flow towards to metal with less workfunction until the fermi levels are aligned, see figure 2.3(b). Due to the charge transport a potential difference between both metals is created inducing an electrical force. This force can be nullified by applying an external bias (V_{DC}) having the same magnitude as the V_{CPD} with opposite signed, figure 2.3(c). Note that the V_{DC} value that nullifies the electrical force is equal to the work function difference between the tip and sample. So, the goal of a KPFM is to measure such voltage difference.

KPFM was developed as a double-pass technique, because topography and V_{CPD} could not be measured at the same time. Therefore, in the first scan, the topography is calculated in tapping mode. In the second pass, the tip scans the surface measuring the V_{CPD} using the previous topography information. However, during the last years, single-pass KPFM technique has been developed, which allows to measure topography (tapping mode) and V_{CPD} at the same time using two fundamental vibration modes of the cantilever. This technique improves some problems of the double-pass technique such as; topography information without drifting or the lower V_{CPD} resolution of the second scan because the tip is situated at a certain constant distance of the sample [108]. In this work, KPFM technique was used to calculate the trapped charge in a HfO_2 layer in order to complement and extend the information obtained with CAFM technique.

2.3. Introduction to TCAD tools

The cornerstone of the exponential electronic technology rise is based on the synergy between *manufacture*, *characterization*, *modeling* and *simulation* of the electronic devices.

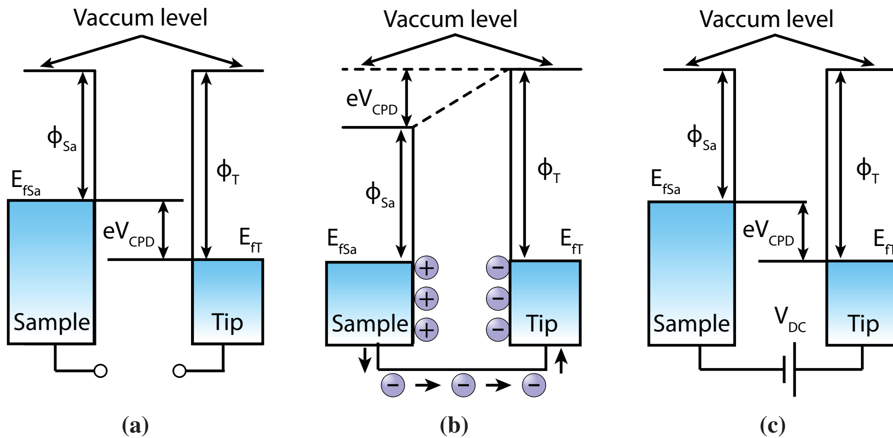


Figure 2.3: Energy band diagram of the sample and AFM tip for three cases: tip and sample are not in contact (a), tip and sample are in electrical contact (b), and a V_{DC} is applied between tip and sample to nullify the CPD (c).

The last section was focused on different characterization techniques used to study the electrical properties in this thesis. The goal of this section is to discuss the fundamental concepts of TCAD simulations (advantages and limitations) and describe the main models used to perform studies related to this thesis.

TCAD is often referred as the branch of electronic design that models semiconductor fabrication by process simulators and semiconductor device operation by device simulators and Simulation Program with Integrated Circuits Emphasis (SPICE) tools. This tool started its develop focusing on BJT technology and the challenges of isolated junctions and double and triple-diffused transistors in the 1960s [109]. During the next decade many contributions to 1D [110, 111] and 2D [112, 113] simulation from a large number of researchers were reported improving TCAD tools. In the early 1980s, CMOS became the dominant driver for integrated electronics and the device size became smaller and their designs more complex. Therefore, 2D numerical simulations started to be inadequate, leading to the development of 3D numerical simulators [114]. Currently, TCAD tools are essential to develop new device architectures and optimize process flows, being Silvaco Inc. [115] and Synopsys [116] the major providers of commercial TCAD tools [117]. Figure 2.4 shows the growth of fiscal results of Synopsis indicating the importance of these tools in the electronic industry. In fact, according to International Technology Roadmap for Semiconductors (2005), the development costs of electronic devices are reduced by about 40 percent by the efficient use of TCAD tools [118].

In this thesis, ATLAS module, which is included in Silvaco TCAD tool, was used to

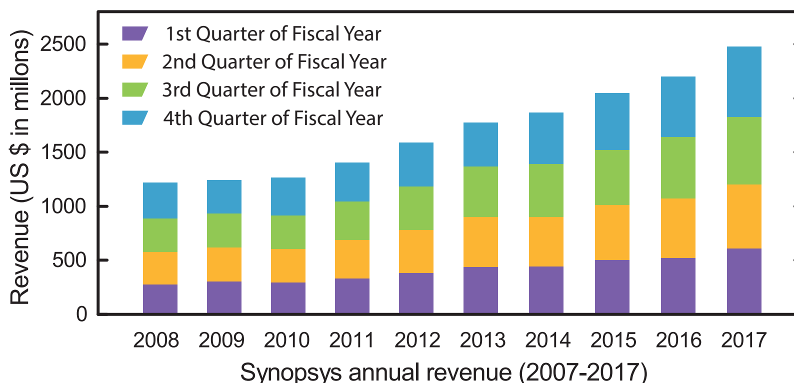


Figure 2.4: Synopsys revenue growth in the decade (2008 - 2017). Source of Synopsys financial report (https://www.synopsys.com/company.html).

perform the 2D/3D device simulations. In particular, ALTAS is a physically-based device simulator that calculates the electrical characteristics associated with the defined structure and bias conditions by applying a set of differential equations. Besides, Silvaco TCAD tool includes ATHENA module, which is a process simulator to calculate the physical structures that result from processing steps. However, Reliability of Electron Device and Circuits (REDEC) group does not have access to processing data, and therefore, this module was not used in this work.

2.3.1. Device simulator: ATLAS module

Atlas module is a general two and three dimensional simulator of semiconductor devices. Figure 2.5 shows the sub-modules (blue filled boxes) of the ATLAS simulator. As it can be seen, ATLAS includes a structure and mesh editor (input 1) where any device can be designed. Once the device is designed, the statements to indicate the models, numerical methods and boundary conditions are introduced by a command file (input 2). From these two files, the device simulator solves the equations of the models using the selected numerical methods and taking into account the device structure (geometry, material properties, interfaces...) and boundary conditions. The outputs of the simulator are the electrical parameters such as; current, voltage, capacitance... and the physical parameters for each mode of device such as; mobility, life times of carriers, electric field...

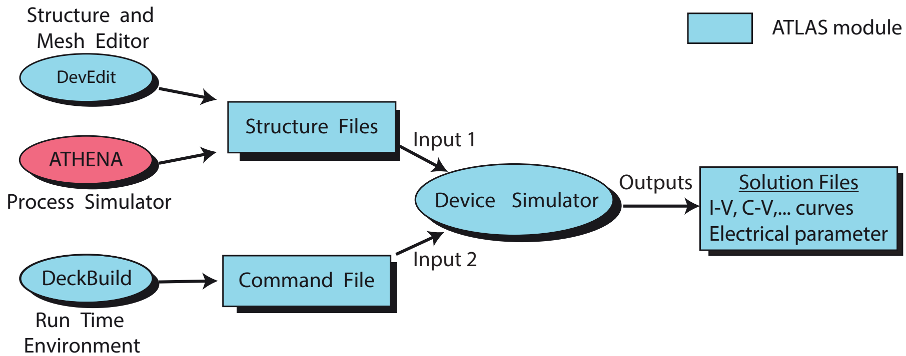


Figure 2.5: Scheme of sub-modules and simulation flow of ATLAS device simulator.

Structure and mesh editor

This sub-module of ATLAS allows to design any device, which is formed by semiconductors, metals and oxides included in the simulator library. Besides, this editor includes an auto-mesh program, which can be previously used to define a regular mesh. A mesh consists of a number of points known as nodes (N) where the equations of models are solved by the simulator. The accuracy of results and the convergence of the equations are directly related to the goodness of the mesh [117], being this step (meshing) one of the most critical in the simulation. Doping and contacts have also to be defined using this editor. Figure 2.6 shows the channel of a MOSFET device using an optimized mesh. As it can be observed, the mesh size changes being more fine under the gate, where higher electric fields and density carrier can be reached, and more course in the rest of device. On this way, the accuracy and convergence criteria are satisfied and the simulation time is optimized.

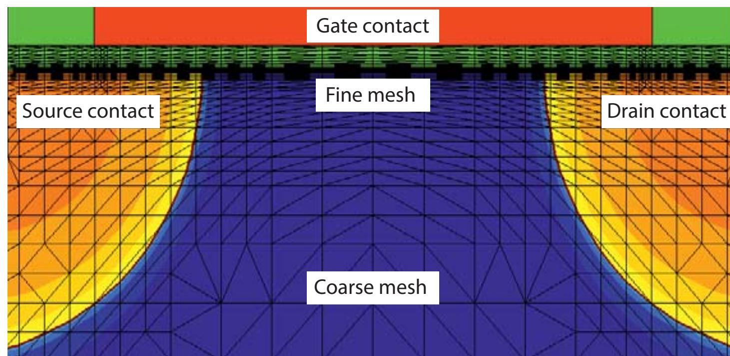


Figure 2.6: Detail of a channel of MOSFET device. An optimized mesh is proposed.

Command file

As it was explained previously, the models used to solve the carrier transport and obtain the electrical characteristics given a bias conditions must be specified in the command file. These mathematical models consist of a set of fundamental equations which link the electrostatic potential and the density of carriers within the simulation domain. These equations, which are solved in any general purpose device simulator, have been derived from Maxwell's laws and consist of *Poisson's Equation* 2.1 and the *continuity equations* (2.2 and 2.3) [115].

Poisson's electrostatic equation relates variations in electrostatic potential to local charge densities, where ψ is the electrostatic potential, ρ is the local space charge density and ε is the local permittivity.

$$\nabla^2 \varphi = -\frac{\rho}{\varepsilon} \tag{2.1}$$

Continuity equations guarantee the principle of mass conservation in the device, where n and p are the electron and hole concentration, $\vec{J}_{n/p}$ are the current densities, $G_{n/p}$ are the generation rates and $R_{n/p}$ are the recombination rates.

$$\frac{\partial n}{\partial t} = \frac{1}{q} div \vec{J}_n + G_n + R_n \tag{2.2}$$

$$\frac{\partial p}{\partial t} = \frac{1}{q} div \vec{J}_p + G_p + R_p \tag{2.3}$$

These equation (2.1,2.2 and 2.3) provide the general framework for device simulation. But, in addition to these equations, other equations are needed to specify particular physical models for: $\vec{J}_{n/p}$, $G_{n/p}$ and $R_{n/p}$.

The transport equations describe the way that the electron and hole densities evolve as a result of transport, generation and recombination processes ($\vec{J}_{n/p}$). Usually, these equations are obtained by applying approximations and/or simplifications to the Boltzmann Transport Equation [119]. These assumptions can result in a number of different transport models such as the *drift-diffusion model* or the *energy balance model* (see table 2.1).

1. **Drift Diffusion model:** this is the simplest model of charge transport used in this thesis. This model is adequate when the thermal effects can be neglected and the main forces of transport are the electric field and diffusion of carriers [120]. Their main

Simulation models	
Drift Diffusion Model	**Energy Balance model**
Transport Equations	*Transport Equations*
$\vec{J}_n = qn\mu_n\vec{E}_n + qD_n\nabla n$	$\vec{J}_n = qD_n\nabla n - qn\mu_n\nabla\psi + qnD_n^T\nabla T_n$
$\vec{J}_p = qp\mu_p\vec{E}_p - qD_p\nabla p$	$\vec{J}_p = -qD_p\nabla p - qp\mu_p\nabla\psi - qpD_p^T\nabla T_p$

Table 2.1: Comparison between the equations of Drift Diffusion and Energy Balance model transport.

equations are written on the left in the table 2.1, where $\mu_{n/p}$ are the mobility rate, $\vec{E}_{n/p}$ are the effective electric field and $D_{n/p}$ are the diffusion coefficients

2. **Energy Balance model:** this model, unlike drift diffusion model, takes into account non-local transport effects such as velocity overshoot, diffusion associated with the carrier temperature and the dependence of impact ionization rates on carrier energy distributions. To do that, this model introduces carrier temperature for electrons and holes $T_{n/p}$ as new independent variables and the thermal diffusivities $D^T_{n/p}$. This makes this model to be more adequate to simulate devices whose dimensions are some tens of nanometers or devices that can experiment self-heating due to the electrical stress. Their main equations are written on the right in the table 2.1.

A complete description of these models can be found in [121, 122]. In this thesis the drift diffusion model is used to simulate MOSFET transistors of 65 nm technology node (chapter 5), and the energy balance model is used to simulate UTBB FD-SOI MOSFET of 28 nm technology node (chapter 6). Besides, for each device simulation carried out, specific models of mobility, generation/recombination $G_{n/p}$ and $R_{n/p}$ or introduction of quantum effects were taken into account.

Limitations and challenges of TCAD simulations

Nowadays, although TCAD tools are essential for the research, development and/or optimization of electronic devices, they have some limitations. They must be taken into account when the results of simulations are interpreted. Some limitations of TCAD tools are:

1. **Simulation structure:** the simulated device created using a process simulator or with CAD operations must be as close to the real device as possible. However, this task is not easy, because the real devices dimensions, material quality, interfaces, doping levels and so on, cannot be estimated with accuracy. Usually, to solve this problem, TCAD simulation are calibrated using test devices.

2. **Quantum effects:** although the quantum mechanics is well known since the last century, its implementation in TCAD is more recent (when the nanoscale devices started to be manufactured). Therefore, other limitation of these simulators is that some part of the relevant physics must be incorporated into the simulators and adequately validated.
3. **Range of validity of a model:** TCAD tools usually incorporate a lot of models (some of them are empiric model with many parameters) in order to be the most general as possible. However, to know what is the best model or if the values of simulation are in the range of validity of models is not easy. If this issue is not carefully considered, it could lead to wrong results.

2.4. How to link the simulator and the experimental data

A great part of this thesis is focused on studying how nanoscale phenomena impact on the variability of device parameters of merit of devices and circuits. To do that, several devices (MOSFET and UTBB FD-SOI MOSFET) are designed (pristine devices), and then little changes in these devices are introduced such as: fixed individual charges, gate oxide roughness, charge density distribution... On this way, variability due to different phenomena as, BTI, RTN, LER... can be studied. However, to perform realistic variability simulations, a lot of nanoscale information about the properties of materials that form the device is mandatory. In this thesis this information is obtained by CAFM as images, which must be analyzed and processed. However, the CAFM maps are experimentally hard and expensive to obtain, because the CAFM tip is quickly degraded when the images are performed in contact mode and high resolution. This fact motivated the development of a software tool called Nanoscale Map Simulator (NAMAS), which take advantage of the nanoscale experimental data obtained by CAFM (topography and current maps) can simulate automatically a lot of statistically similar data (topography maps) and calculate their corresponding charge density maps knowing the electric information through current map and the materials and geometry of the sample. This software produces the necessary nanoscale information (topography and charge density) to study the variability in devices through device simulators (chapter 4).

Chapter 3.

Nanoscale electric characterization of TDs in InGaAs

As it was explained in the chapter 1, many authors are studying the conduction properties of defects in III-V materials. These III-V semiconductors are often grown locally over the Si substrate and due to the lattice mismatch between these materials, they tend to form structural defects [15]. In particular, in the literature, TDs defects have been mainly studied using two different strategies; measuring the electrical properties at *device level* or at the *nanoscale*.

First strategy, based on measuring I-V characteristics of fully processed devices, such as MOS capacitors, MOSFETs, and Schottky diodes, to study the conduction mechanism through III-V materials was used in [15, 48, 123]. In these works, the reverse current measured in Schottky diodes has been attributed to PF emission. However, employing this methodology, the electrical characteristics of the measured devices could not be strictly attributed to the electrical properties of the TDs, because the measured characteristics were also affected by the properties of the active non-TD device area.

On the other hand, since TDs cross-section dimensions can be in the nanometer range, other works are focused on studing the TDs using CAFM techniques following the second strategy [50, 124–126]. These studies demonstrate that the structurally defective sites (which are detected as pits in the topographical images) exhibit lower turn-on voltages and enhanced leakage currents measured in forward and reverse bias, respectively. Besides, forward currents through TDs were attributed either to the PF conduction mechanism [124, 125] or to a lowering of the barrier height of the TE conduction mechanism between the tip and the sample [50]. However, all these previously works were performed at only one temperature (ambient temperature). Only, in a limited number of studies, the CAFM data (only topography) has been combined with I-V curves collected at different temperatures [127], but at device level.

In the present chapter, CAFM measurements to localize TDs and analyze the electri-

cal conduction through TDs (*on-TDs*) and through areas without defects (*off-TDs*) are performed. Moreover, nanoscale measurements using CAFM at different temperatures were performed to study the conduction mechanism of TDs.

3.1. Sample and measurement equipment

The analyzed sample is a multi-layer stack, which consists of Te:InGaAs 30 nm/InGaAs 120 nm/InP 600 nm/GaAs 500 nm/Si. Figure 3.1 shows a cross section Transmission Electron Microscopy (TEM) image obtained of this stack. This image demonstrates the presence of TDs in the InGaAs film (white arrows). Some of these TDs are propagated from the substrate interface through the III-V film thickness and reach the surface, where they can be detected as pits by CAFM (white circle). Therefore, these pits can be assigned to high defect density areas.

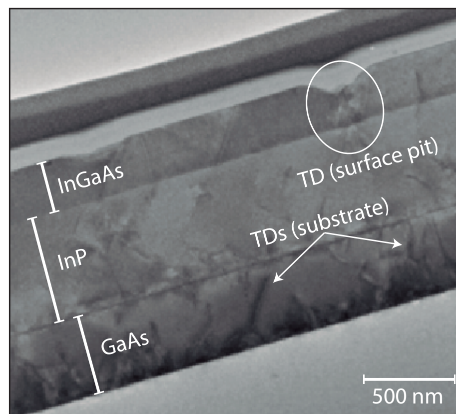


Figure 3.1: TEM cross section image where is highlighted the main layers of the stack and a possible threading dislocation (circle)

The measurement equipment used to analyze this sample was a CAFM Asylum MFP3D. Due to that the sample is highly conductive, the module called ORCA to measure wide current ranges (from 100 pA to 10 μA) was used. Besides, a *PolyHeater* sample stage was added to control the temperature range up to 500 K. In order to ensure the stability of tip properties during the experiments, the Pt bulk tips were used in all measurements.

3.2. Morphology and electric characterization

The characterization of the electric properties of III-V semiconductor bulk, and in particular, of the TDs was performed in two steps. The first one was to identify the TDs locations on the surface. To do that, topographical and current maps were measured simultaneously by scanning on randomly selected surface areas of the stack. Figure 3.2 shows topographical (a) and current maps (b) at 2 V, injection from the tip. As it can be seen, there is a correspondence between the topography pits and current spots, which are attributed to TDs. Once the TDs are identified, the second step was to measure I-V curves on-TDs and off-TDs to compare both electrical conduction. Since the tip is metallic, the tip-sample contact was modeled as a Schottky junction. Taking into account that a reverse-bias leakage current is of a special interest in devices containing III-V materials, this study was focused on the analysis of electrical conduction only under reverse bias conditions.

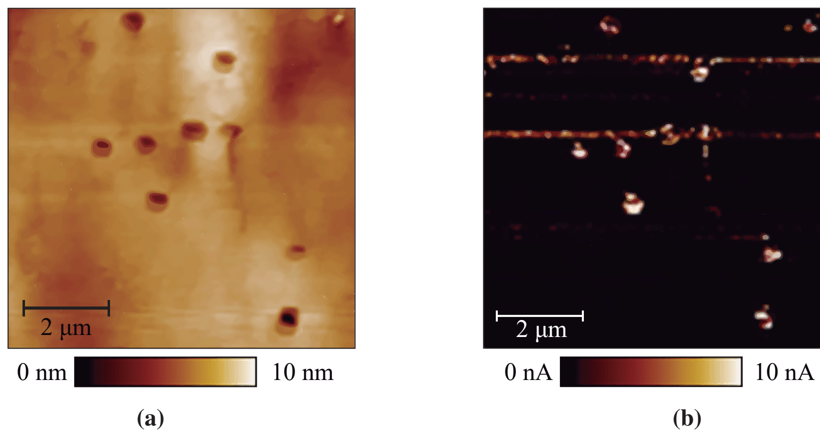
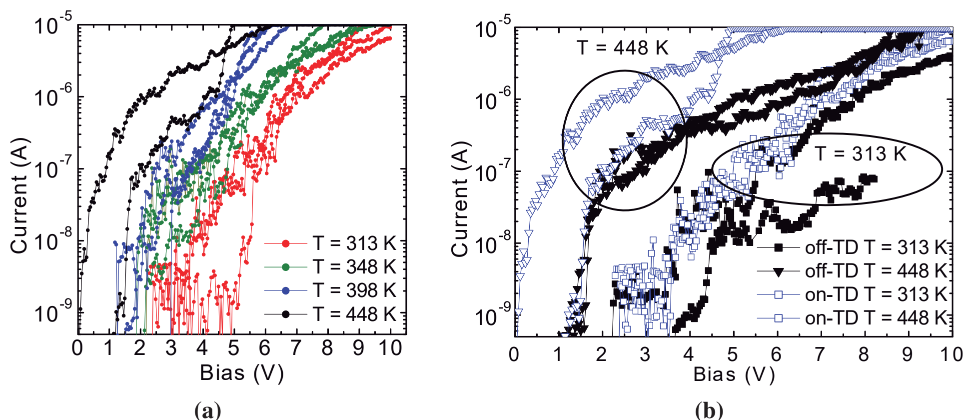


Figure 3.2: C-AFM topography image (a) and reverse current image measured at 2 V (b). It can be seen a correspondence between the topography and current spots. Two bright lines in the upper region of a current map correspond to AFM artifacts.

Moreover, to compare temperature dependencies of the conduction through on-TDs and off-TDs sites, CAFM I-V measurements were performed at several temperatures (313, 348, 398 and 448 K) at both sites. It is important to note that the CAFM-based I-V measurements at different temperatures are technically rather complex to execute. To change temperature, the tip must be withdrawn from the sample surface, and then it has to be re-positioned on the same site, which is a challenging task in the case of the required highly scaled area range. On the other hand, the measurement itself could modify the electrical properties of the stack (charge trapping), hindering a fair comparison between all measurement [128]. To mitigate such uncertainty, a statistical analysis of the electrical conductivity data collected at each

temperature on different TD sites was carried out (I-V curves were not measured repeatedly on the same site). This method was found to be more accurate than measuring a fixed TD site at different temperatures.

Figure 3.3(a) shows examples of I-V curves measured on-TDs at 4 different temperatures within the 313 K - 448 K range. Temperature dependence is clearly seen, which indicates an increase of current when the temperature is higher. Similar measurements have been performed off-TDs surface sites. Figure 3.3(b) shows a comparison between I-V curves measured on-TDs (open symbols) and off-TDs (solid symbols) at 313 K and 448 K, demonstrating that the on-TD currents are higher than those of the off-TDs, consistent with the data in the images in figure 3.2.



(a) (b)

Figure 3.3: Set of I-V curves measured on different TDs sites (same tem- perature color) (a). Example of I-V curves measured on-TDs (open symbols) and off-TDs (solid symbols) at 313 K and 448 K (b).

3.3. Transport mechanisms

Assuming that higher currents could be associated to the presence of defects in TDs, the I-V curves were fitted to PF emission, which considers the charge and discharge of traps to assist the conduction of carriers [12]. Besides, this mechanism is widely use in the literature to model this type of junctions. On the other hand, in the off-TDs sites the quantity of defects was assumed negligible, therefore the conduction mechanism more adequate to describe the conductive behavior is TE [12]. In the next sections, experimental data are fitted to the equation of proposed models.

3.3.1. Poole Frenkel transport mechanism

In order to fit the experimental I-V curves for the different temperatures to the PF transport mechanism, the equation 1.7 was linearized applying natural logarithm to both sides of equation. The results are;

$$ln(J_{PF}/E) \propto R(T)\sqrt{E} + S(T) \tag{3.1}$$

$$R(T) = \frac{q}{KT}\sqrt{\frac{q}{\pi\varepsilon_0\varepsilon_r}} \tag{3.2}$$

$$S(T) = -\frac{q\Phi_t}{KT} + log(C) \tag{3.3}$$

where $R(T)$ and $S(T)$ are the slope and y-intercept respectively of a line equation, when the y-axis is $ln(J_{PF}/E)$ and the x-axis is $\sqrt{E}$.

If the I-V curves show in figure 3.3(a) are represented in a graph where the y-axis $ln(J_{PF}/E)$ and the x-axis is $\sqrt{E}$ a linear behavior must be found, see rigure 3.4(a). To better understanding of the graph, only a single I-V curve is represented for each temperature. As it can be observed, for each temperature the experimental data follow (although with fluctuations) a linear trend, suggesting that the conduction through the TDs is consistent with the PF mechanism.

In figure 3.4(b) the average of all y-intercept values of the fit (solid) lines of the figure 3.4(a) $S(T)$ as a function of $1/T$ (triangles) is represented. The number of I-V curves to do the average for each temperature was 6. These experimental data were fitted to the equation 3.3 whose dependency on $1/T$ is described by linear behavior. Therefore, identifying terms, the emission barrier height Φ_t is proportional to the $S(T)$ slope (0.51 eV), being this value compatible to the reported ones [129].

Similarly, the average of all slopes of the fit lines in figure 3.4(a), $R(T)$, is also represented as a function of $1/T$ (squares) in figure 3.4(a). Since equation 3.2, ε_r is estimated to be about 4.52. It must be noted that the calculated values of Φ_t and ε_r have been obtained from a linear fitting of the $S(T)$ and $R(T)$ average values at different temperatures. The $S(T)$ and $R(T)$ average values (at a given T) used in the linear fitting correspond to the average values of S and R obtained from the data collected on different TDs sites. Therefore, the calculated values of Φ_t and ε_r correspond to an average value of the analyzed sites.

To verify the validity of the PF mechanism in TDs, the on-TDs current was calculated

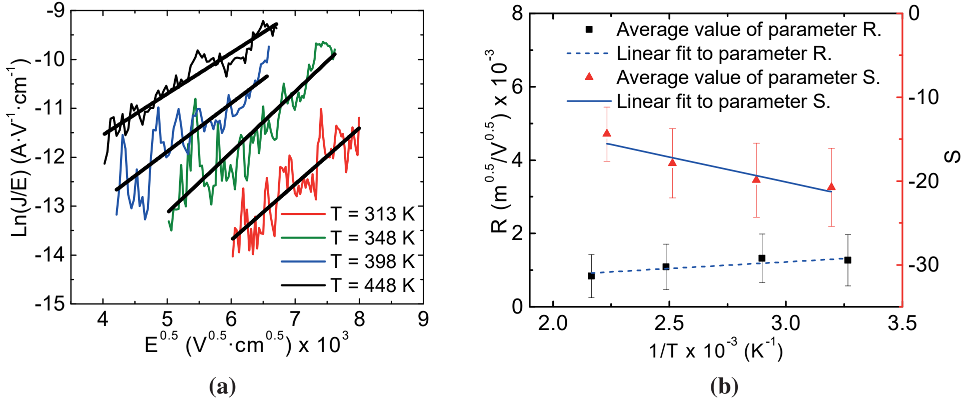


Figure 3.4: Measured I-V curves in 3.3(a) are plotted (one curve per each T) following the expression (3.1) (a). Linear fittings are also represented. $R(T)$ (black squares) and $S(T)$ (red triangles) mean values in the y-axis, which are the slope and the y-intercept values of the entire set of measured I-V curves respectively, as a function $^1/_T$ (b). Continuous lines show the linear dependency of $R(T)$ and $S(T)$ versus $^1/_T$ in (3.2 and 3.3).

introducing the average value of the calculated physical parameters (Φ_t and ε_r) in the equation 1.7. Figure 3.5 shows the comparison between the experimental data (symbols) and I-V dependencies calculated using the PF equation (solid lines) with the experimentally determined parameters. As it can be seen, I-V trends based on the PF emission mechanism fit well the measured ones. Notice that, only one I-V curve for each T is shown to a better representation. Besides, the data at low biases (noise level of the setup) and very high biases (possible other current contribution), are not shown.

Although the on-TDs conduction is generally higher than that of the background areas, the off-TD conductivity is not negligible (see figure 3.3(b)) and, therefore, it was also evaluated. In order to check if neglect the defects in off-TDs areas is a correct assumption, the I-V curves in these sites were evaluated by the PF model, using the same procedure applied to on-TDs sites. The calculated values of the physic parameters were Φ_t = 0.53 eV and ε_r = 2.56. However, when the I-V curves are calculated using these parameters and compared to the experimental data they do not match (see 3.5(b)). Hence, this analysis demonstrates that the PF emission is the dominant process in the TD sites.

3.3.2. Schottky Emission transport model

On the same way, I-V curves measured under the reverse-bias on the off-TD sites were analyzed by the same procedure than on the on-TD. However, in this case the equation to fit the experimental data is the TE model (3.4), which can be also linearized as (3.5)

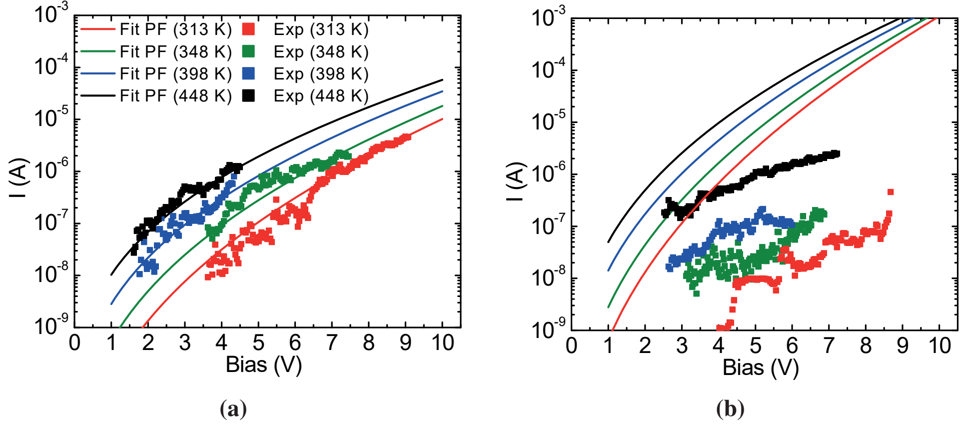


Figure 3.5: I-V curves (symbols) measured on-TD (a) and off-TD (b) sites at different temperatures. Solid lines correspond to the calculated PF current using the parameters obtained by the fitting of $S(T)$ and $R(T)$.

$$J_{TE} \propto A^{*}T^{2}exp\left(-\frac{q}{k_{B}T}\left(\phi_{B0}-\sqrt{\frac{qE}{4\pi\varepsilon_{0}\varepsilon_{r}}}\right)\right) \tag{3.4}$$

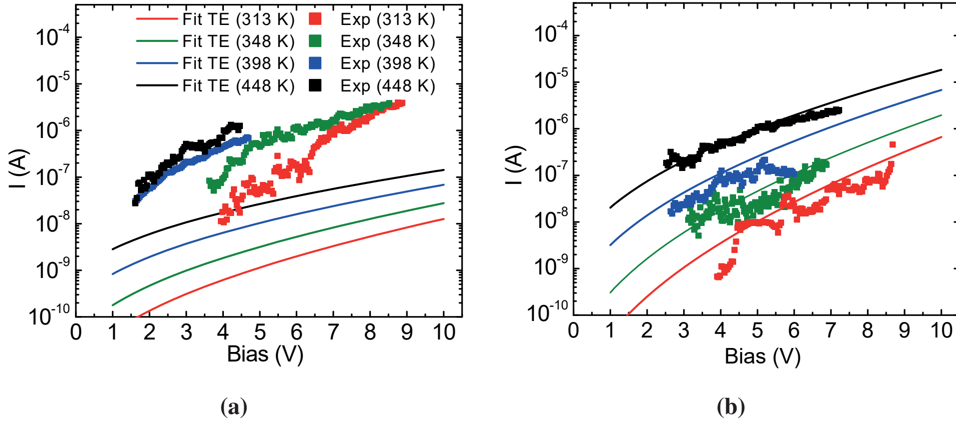
$$ln(J_{TE}/T^{2}) \propto R^{*}(T)\sqrt{E}+S^{*}(T) \tag{3.5}$$

$$R^{*}(T)=\frac{q}{KT}\sqrt{\frac{q}{4\pi\varepsilon_{0}\varepsilon_{r}}} \tag{3.6}$$

$$S^{*}(T)=-\frac{q\Phi_{B0}}{KT}+log(A^{*}) \tag{3.7}$$

where $R^{*}(T)$ and $S^{*}(T)$ are the slope and y-intercept respectively of a line equation, when the y-axis is $ln(J_{PF}/T^{2})$ and the x-axis is $\sqrt{E}$. The barrier height and permitivity for the off-TD sites were found to be Φ_{B0} = 0.61 eV and ε_{r} = 3.9, respectively.

Figure 3.6(b) shows the comparison between the experimental data in off-TD (symbols) and calculated current using equation 3.4 and the values obtained from the experimental data (Φ_{B0} = 0.61 eV and ε_{r} = 3.9) for each temperature (solid lines). As can be seen, the experimental data matches very well to the TE-based calculations (especially at a higher temperature, when the TE process dominates). Therefore, off-TD current could be described by considering electrons with enough energy to overcome the barrier when the electron transport assisted by defects can be negligible. The observation of high off-TDs currents under



(a) (b)

Figure 3.6: I-V curves (symbols) measured on the on-TDs (a) and off-TD (b) sites at different temperatures. Solid lines correspond to the calculated TE current using the parameters obtained by the fittings of S'(T) and R'(T).

the reverse bias conditions could be understood by considering a low barrier height for the electrons injected from the metal (Φ_{B0} = 0.61 eV), which depends, in our case, on the materials in a CAFM tip and top layer of the analyzed sample. Following the procedure employed in the previous section, I-V curves measured in on-TDs were fitted using the TE emission model. The physical parameters Φ_{B0} = 0.37 eV and ε_r = 11.7 were obtained. However, the I-V curves calculated by using these parameters in equation 3.4 do not match the experimental data (3.6(a)). This result further supports the conclusion that the conduction through the on-TD sites can be described by considering the PF emission, but not the TE process, and viceversa. Moreover, the data indicate that TDs are a major component of enhanced reverse-leakage current through III-V materials.

3.4. Summary and discussion

In this chapter is based on paper IEEE EDL (May-2016) where conduction through TDs sites in the III-V materials have been investigated using CAFM-based measurements at different temperatures. The conductivity of TDs, observed as surface pits in topographical maps, is found to be higher than that of the off-TD sites. In both on- and off-TD sites, the currents were observed to increase with temperature. The on-TD electrical conduction can be described by accounting for the PF emission process suggesting that it can be the dominant conduction mechanism at these sites. Conductivity of the off-TD sites, in particular, at higher temperatures, seems to be controlled by the thermionic emission mechanism. In summary, the results demonstrate that the CAFM technique is well-suited for evaluating the TDs

electrical properties with the nanoscale resolution, required to identify material structural features affecting device performance.

Chapter 4.

Development of a CAFM-based Nanoscale Map Simulator (NAMAS) to study the impact of the gate oxide fluctuations on MOSFET variability

As it was introduced in the chapter 2, the nanoscale information is crucial to understand important phenomena in the sub-micrometer electronic devices, such as the variability of device parameters or the increasing of leakage current [130, 131]. However this information is usually hard to obtain, even when the most advanced techniques such as CAFM or KPFM are used. This fact motivated the development of the simulator NAMAS, which take advantage of the nanoscale experimental data obtained by CAFM (topography and current maps) can simulate automatically a lot of statistically similar data (topography maps) and calculate their corresponding charge density maps, in order to use them in variability studies. In particular, the development of this tool was based on the CAFM measurement of polycrystalline HfO_2 samples, which have been previously studied by REDEC group in the works [41–43]. Although, the developed simulator was only tested in HfO_2, any polycrystalline oxide sample could be studied using this tool.

This chapter is presented in three sections. Firstly, the manufacture details of the sample are described and the morphology and electric characteristics obtained by CAFM are quantitatively analyzed. In the next section, the NAMAS simulator is explained in detail. Finally, NAMAS simulator is used to obtain the needed nanoscale information, which is introduced in a device simulator developed by *University of Santiago de Compostela* [132, 133], to study the impact of the local defect density (ρ_{ox}) and thickness of the gate dielectric (HfO_2) T_{OX} on the $I_D V_G$ curves of MOSFET devices.

4.1. Sample description

The analyzed sample consists of 5.3 nm thick film of HfO_2 deposited by Atomic Layer Deposition (ALD) on a 0.7 nm SiO_2 interface layer, which was grown on a Si epitaxial P-substrate. The stack was annealed at 1000 °C in order to induce the crystallization of the high-k layer. The thickness of each layer were checked by X-Ray Reflectivity technique [43].

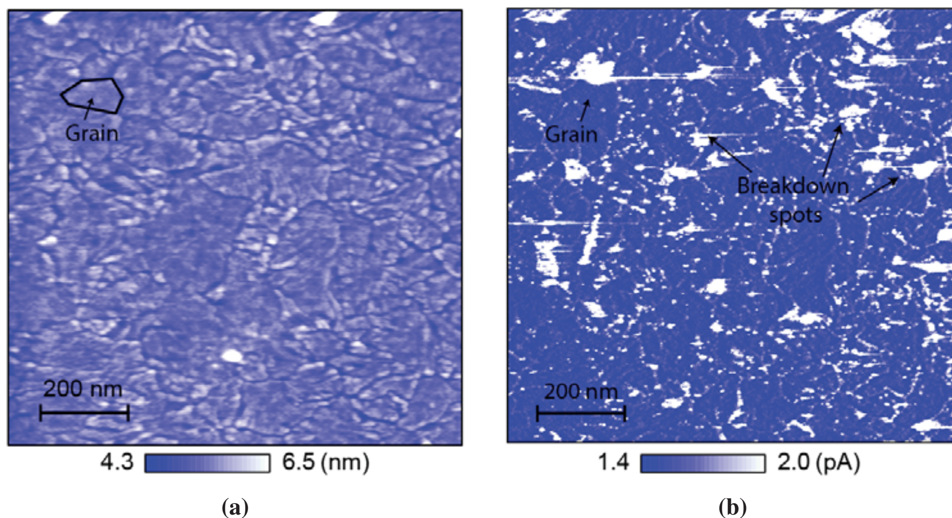


Figure 4.1: Topography (a) and current (b) maps obtained at V_G = 6.5 V on a HfO_2/SiO_2/p-Si structure (1000 nm x 1000 nm) [43]. Grains, grain boundaries and breakdown spots are highlighted.

The morphological and electrical properties of the polycrystalline dielectric are studied by a CAFM in Ultra High Vacuum (UHV) ($\approx 10^{-10}$ mbar). Figure 4.1 shows a topographical 4.1(a) and current 4.1(b) map (obtained at 6.5 V, substrate grounded), which were measured in contact mode using a diamond-coated silicon tip. Figure 4.1(a) shows a polycrystalline surface where Grain Boundaries (GBs) (deeper areas) and Grains (Gs) (higher areas) can be distinguished. An example of grain is highlighted in black in the top left of topography map. The thickness of HfO_2 at each site of the surface is estimated by assuming that the average thickness of the oxide layer measured by X-Ray Reflectivity (5.3 nm) corresponds to the average height of the topographical map. Any height deviation with respect to the topographical average at any site of figure 4.1(a) is attributed to a deviation from the average of T_{OX}. Figure 4.1(b) shows the corresponding current map to the topography (figure 4.1(a)), where higher currents are measured at GBs. Besides, some breakdown spots (white areas) can be also observed [43].

Figure 4.2 shows the dependence of the current through the sample as a function of its

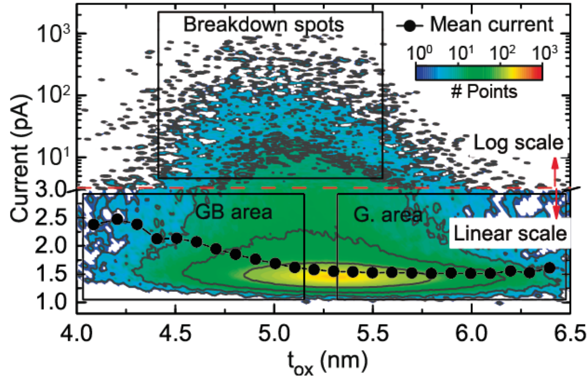


Figure 4.2: Relationship between topography and current in the CAFM maps pixel by pixel. Color map shows the density of pixels for each pair of current and T_{OX} values. Dotted line shows the measured average current vs. T_{OX} (neglecting the contributions of breakdown spots).

thickness of HfO_2, T_{OX}. The data corresponding to GBs, Gs and breakdown spots (shown in figure 4.1(b)) are indicated with rectangles. The color scale indicates the number of pixels found in the images of figure 4.1 with a given current and T_{OX}. Note that more than 90 % of the sites are in the range of few pA, indicating that the image sites linked to breakdown spots are negligible, so that the CAFM data are representative of the oxide. In addition, the mean current (black points) was calculated for each T_{OX} denoting that the current in GBs regions is higher than in the Gs. Although GBs show higher currents than Gs, notice also that GBs and Gs sites show a great variability in current values for a given T_{OX}, indicating that, in addition to T_{OX}, the current through the stack also depends on other parameters. Some works have pointed out that polycrystalline HfO_2 layers show larger ρ_{ox} at GBs, due to oxygen vacancies, which could affect the current through the sample [43, 134, 135]. Therefore, besides of T_{OX} as a varibility source, the impact of ρ_{ox} on MOSFET device parameters can also be important and it is studied in this thesis.

4.2. NAMAS simulator

4.2.1. Topographical map simulator

This module was designed to provide topography maps statistically equivalent to those obatianed experimentally. To reproduce the topography of a given sample, the relevant statistical information of one experimental topographycal map must be previouly obtained. In this thesis, free software called Gwyddion [136] was used to extract the necessary information of figure 4.4(a) (see table 4.1). Table 4.1 (left) shows the parameters related to the sample

morphology, that are obtained to be the inputs of the NAMAS simulator.

Parameter	Experimental		Simulated	
	Mean	SD	Mean	SD
Size (Grain)	33.2	8.2	38.5	11.3
Height (Grain)	2.46	0.19	2.18	0.23
Width (GB)	3.3	1.4	2.1	1.2
Depth (GB)	1.13	0.26	0.98	0.31

Table 4.1: Statistical parameters obtained from a topographical map 4.1(a) layer (experimental columns) and the same parameters obtained from the simulated topographic maps (simulated columns) 4.4(b).

In figure 4.3 some steps used to generate a polycrystalline surface grain by grain by mean of Monte Carlo techniques is shown. Firstly, each grain is assumed as one polygon with N sides, randomly obtained between a minimum and a maximum (8 and 15 were used, respectively), and whose center (C) also is randomly selected at a given position on the surface. The distance of each vertex to the center of the polygon (R_N) is calculated from the statistical distribution of size grain, and assuming that the angle between two consecutive vertexes can be randomly calculated (see figure 4.3(a)). To complete the grain, the GB surrounding the grain is created using a statistical distribution with the parameters *width GB*, figure 4.3(b). Finally, this process is repeated until the surface simulation is completed, figure 4.3(c). This procedure was published in the paper JVST-B (Jun-2015)). However a new version of the algorithm is being developed (2018), in order to simplify the generation procedure using Voronoi diagram.

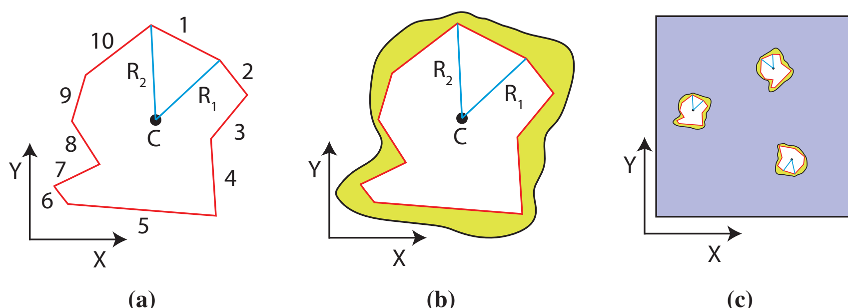


Figure 4.3: Sketch of the process for creating one grain (a). The surrounding GB (b). Several grains and GBs were created on the simulation surface (c).

Once the polycrystalline surface is obtained, the height of each grain and GB is calculated

from the height probability inputs obtained from CAFM experimental images. In addition, in order to perform more realistic simulation, the impact of the tip radius is introduced in the simulation. It is carried out by the application a convolution algorithm [137] and assuming that the tip has a semispherical shape. To validate the simulation procedure, in figure 4.4 is shown a comparative study between experimental a simulated maps. In figure 4.4(a) an experimental topography map is represented. In figure 4.4(b) a simulated map using as inputs the data of this experimental map (table 4.1 experimental column) is shown. Note that both images show grains with similar sizes and random shapes (see highlighted grains in both maps).

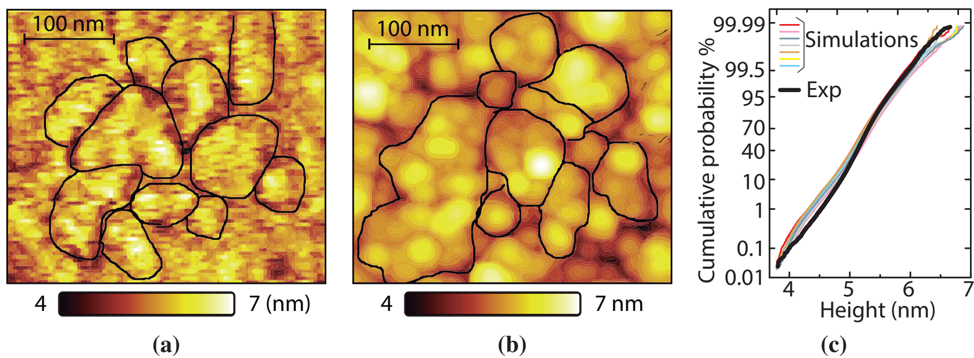


Figure 4.4: Detail of the experimental topography images of the sample (a) and simulated (b). Thickness cumulative probability obtained from the experimental (dots) and several simulated (lines) topography maps (c). Various simulation random seeds are used for the simulations.

In addition to the visual comparison, two statistical validations are carried out. The first validation is based on the comparison of the experimental statistical parameters shown in Table 4.1 to those obtained from the simulated map (Table 4.1 simulated columns). Note that, when the standard deviations are considered, fairly good agreement is observed. On the other hand, the thickness cumulative distributions of the experimental maps (figure 4.4(a)) and several of the simulated maps are plotted in figure 4.4(c). The black line represents the data corresponding to the experimental map and the color lines correspond to the simulated maps. The different simulated maps were obtained by using as input the same statistical parameters (obtained from figure 4.4(a)) but changing the simulation random seed were used. Note that all the simulated thickness cumulative distributions are very similar to the experimental one. The small differences can be related to the fact that different seeds. Therefore, simulated maps are statistically similar but their surfaces are different as it is expected. The good match between the experimental and simulated statistical parameters (shown in table 4.1) and the distributions obtained from experimental and simulated maps indicates that the proposed

simulation methodology accurately reproduces the topography of polycrystalline structures. Once the topography simulator is checked, simulated maps could be used as inputs in a device simulator to analyze how the topography impact on the device parameters.

4.2.2. Charge density map simulator

As it was explained in the first section of this chapter, the experimental data indicates that ρ_{ox} in the oxide can also explain the variability conduction through the analyzed stack. In order to estimate the ρ_{ox} at each site of the dielectric area from the data obtained at the nanoscale with CAFM, the tunneling current through the stack must be previously calculated. This current is calculated taking into account the next assumptions;

1. Sample topography fluctuations is only due to the thickness variation of HfO_2. The thickness of SiO_2 layer is considered constant.

2. The electrical properties of materials are considered ideal and they were obtained from literature [138, 139]. Table 4.2 shows the values used in the calculus.

Parameter	Value	Parameter	Value
Electron affinity (Si) (χ_s)	4.03 eV	Metal Fermi level (φ_m)	5.5 eV
Electron affinity (SiO_2) (χ_1)	0.95 eV	Effective mass (Metal)	1
Electron affinity (HfO_2) (χ_2)	2.65 eV	Effective mass (Si)	0.98
Dielectric constant (HfO_2)	25	Dielectric constant (SiO_2)	3.7
Si Fermi level (φ_s)	4.65	Flat band voltage (V_{FB})	0.87

Table 4.2: Main material parameters used to calculate the current through the stack.

3. An additional barrier between the tip and sample was assumed because the tip-sample contact in CAFM experiments is not ideal [134, 140]. The extra barrier is considered as vacuum, because the experimental data were performed in vacuum. Besides, the thickness of this barrier (T_{vac}) depends strongly on the force applied to the tip [140], whose value was remained constant during the scans, therefore T_{vac} was also assumed constant.

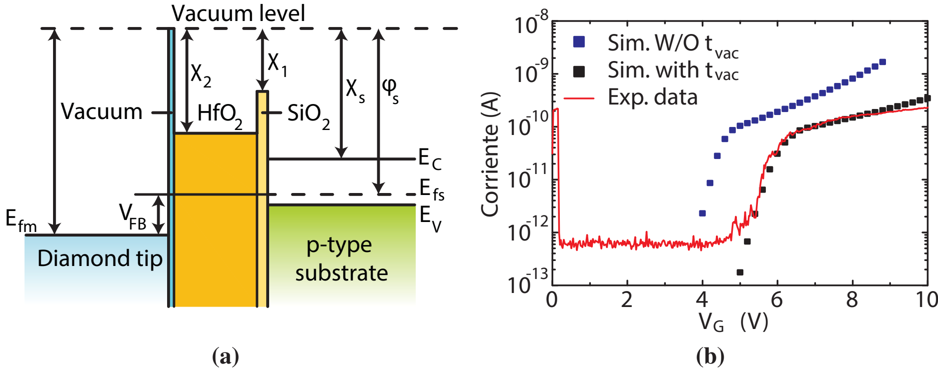
4. The trapped charge in grains of HfO_2 (T_{OX} = 5.75 ± 0.05 nm estimated from figure 4.2) was assumed as ρ_{ox} = $8 \cdot 10^{19}$ cm^{-3} and constant along the oxide thickness (as in [134, 141, 142]), whose value was obtained from [134], where the same sample was analyzed.

From previous considerations, figure 4.5(a) shows the energy band diagram of the stack in a flatband condition, where the main energy values of table 4.2 are represented. In addition, the extra vacuum layer is also plotted. From this energy band diagram, the exact solution of one-dimensional Poisson equation [143, 144] is solved for a given polarization (V_G). Once the biased band diagram is determined, the tunneling current density through the barrier is calculated using the equation 4.1 [143],

$$J = \frac{q\sum_1^l n_{vl}m_{dl}}{2\pi^2\hbar^3}\int_0^\infty T(E)kTln\left\{\frac{\left(1+exp\left(E_{fm}-\frac{E}{kT}\right)\right)^\lambda}{1+exp\left(E_{fm}-E+(\Delta-qV_{ox})\right)}\right\}dE \tag{4.1}$$

where l is the valley number, n_v is the valley degeneracy, m_d is the density-of-states mass per valley, k is the Boltzmann constant, T is the temperature, and V_{ox} is the oxide voltage. $\lambda = m_{ta}/m_{tb}$ is the ratio between the transverse effective mass of electron in the metal gate, m_{ta},and that in the conduction band edge of the silicon substrate, m_{tb}, where m_{tb} = $\sum_1^l n_{vl}m_{dl}$. $T_e(E)$ is the electron transmittance that was calculated using the Airy function solution to the one-electron Schrodinger equation by the transfer matrix approach [145, 146]. By comparing the simulated current for T_{OX} = 5.75 ± 0.05 nm (Grains) with the mean measured current at the same T_{OX} in CAFM maps, a barrier of T_{vac} = 0.40 nm was obtained. Figure 4.5(b) shows a experimental (red line) and simulated without T_{vac} (blue dots) and with T_{vac} (black dots) I_G-V_G curves. As it can be observed, the simulated curve using the extra barrier match with experimental data, verifying the methodology used to calculated the current.

Once T_{vac} is calibrated, ρ_{ox} is the only fitting parameter for the current simulation. By the assumption of an equivalent constant ρ_{ox} along the oxide thickness, ρ_{ox} is estimated at each site of figure 4.1(a) by considering its corresponding T_{OX} thickness and by matching the simulated current with the measured current of figure 4.1(b). It is important to note that breakdown spots are excluded of the analysis because they are not representative of the background sample behavior. Besides, sites with currents below 1.3 pA are neglected because the noise level could affect the data. Figure 4.6(a) shows the simulated positive charge density map calculated from the experimental maps shown in figure 4.1 and using the explained methodology. The comparison of figures 4.1(a) and 4.6(a) shows that, T_{OX}



(a) (b)

Figure 4.5: An energy band diagram of a diamond tip/HfO2/SiO2/p-Si MOS structure (a). Experimental (red line) and calculated without T_{vac} (blue dots) and with T_{vac} (black dots) I_G-V_G curves comparison.

and ρ_{ox} are related, showing higher ρ_{ox} at GBs than at Gs. In particular, a linear relation between both parameters (T_{OX} and ρ_{ox}) was found (inset figure 4.6(b)).

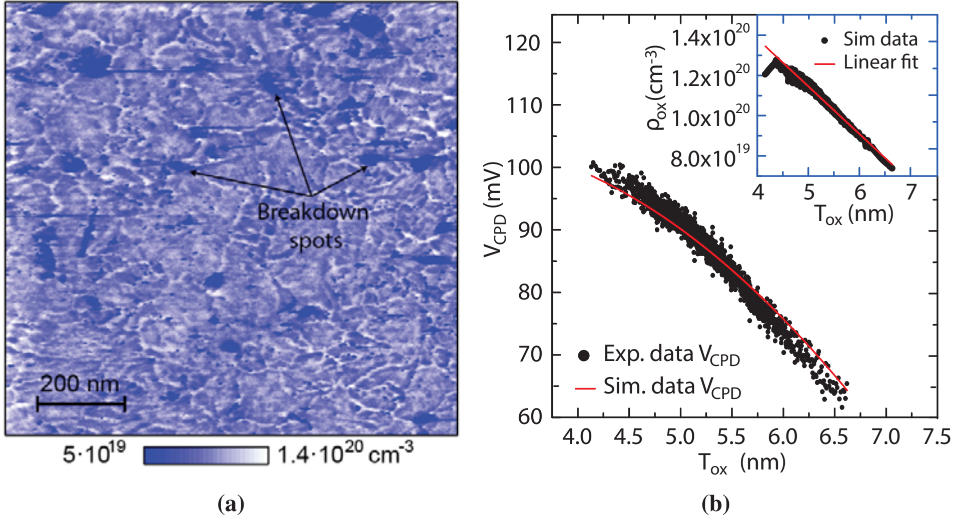
In order to validate the methodology used to calculate ρ_{ox}, KPFM measurements on the same sample (see [41]) are used to extract the correlation between the topography and tip-sample V_{CPD}. This potential is related to the V_{CPD} of the MOS structure. The expression of V_{CPD} is given by,

$$V_{CPD} = \varphi_{s-m} + \frac{Q_i}{C_{s-m}} \tag{4.2}$$

where φ_{s-m} and C_{s-m} are the work-function difference and capacitance between the semiconductor and tip (metal), respectively. Q_i is the equivalent surface density charge which is related to ρ_{ox} by (4.3) [147].

$$Q_i = \frac{q}{T_{OX}} \int_0^{T_{OX}} x\rho_{ox} dx \tag{4.3}$$

From this equations (4.2 and 4.3) and the relationship found between T_{OX} and ρ_{ox} (inset figure 4.6(b)) the V_{CPD} can be calculated and compared to experimental V_{CPD} data obtained by KPFM. Figure 4.6(b) shows the comparison between the experimental data from KPFM and the calculated V_{CPD}, where a good match between both data is observed. This analysis proves by an independent way the goodness of the performed calculus of the charge density.



(a) (b)

Figure 4.6: Charge density map estimated from experimental data of figure 4.1. Experimental V_{CPD} (dots) was obtained from KPFM maps measured on the same sample [41] (b). The inset shows the found relationship between ρ_{ox} and T_{OX}. Lines are fittings of the experimental data

4.3. Variability device simulation using nanoscale information

Once the simulator NAMAS explained and validated, it can be used to generate nanoscale information (T_{OX} and ρ_{ox}), which can be introduced in a simulator devices in order to evaluate the impact of T_{OX} and ρ_{ox} on the device electrical characteristics. In particular, a 3D in-house built parallel drift-diffusion device simulator [148] was used for this purpose, which includes quantum corrections through the density-gradient approach [133]. The finite-element method is applied to discretize the equations, which allows the simulation of complex domains with great flexibility. A full description of the simulation methodology can be found in [133].

To test the introduction of nanoscale data (T_{OX} and ρ_{ox}) into the simulator device, a test n-type Si MOSFET device of (W/L = 50/50 nm) gate area with a HfO_2/SiO_2 gate stack was considered. The source and drain doping profiles were obtained from the appropriate scaling of a 67 nm effective gate length MOSFET that was calibrated against experimental data [132]. The introduction of nanoscale properties were carried out in two steps. First, a reference device is simulated with uniform HfO_2 thickness and charge density (figure 4.7(c) dotted line), which correspond to the mean values of the experimental maps (figures 4.1(a) and 4.6(a)), 5.3 nm and 1.08 10^{20} cm^{-3}, respectively. Then, in order to study the influence of

polycrystallization of the gate dielectric on the device electrical properties, other two maps were chosen as gate areas of the MOSFET devices. Figures 4.7(a) and 4.7(b) show experimental topography map and its corresponding calculated charge density map, respectively. From these maps, two areas (50 x 50 nm) were chosen, where one of them contains GBs (red square) and the other does not (green square). These data (T_{OX} and ρ_{ox}) are introduced into the device simulator to set the gate oxide properties. Figure 4.7(c) shows the I_D-V_G characteristics at V_D = 50 mV for the three MOSFETs with different gate oxides. Red/green I_D-V_G curves correspond to devices with dielectrics with/without GBs. Note that different currents can be observed in both devices, which, moreover, differ from those observed in the reference transistor. The differences in the currents of the devices with/without GBs (red/green I_D-V_G curves) correspond to differences in their V_{TH} of 29.3 mV. Note that this V_{TH} shift is comparable to the time-zero variability observed in devices with the same size [149], showing the relevance of the impact of GBs on the device electrical characteristics and their device-to-device variability.

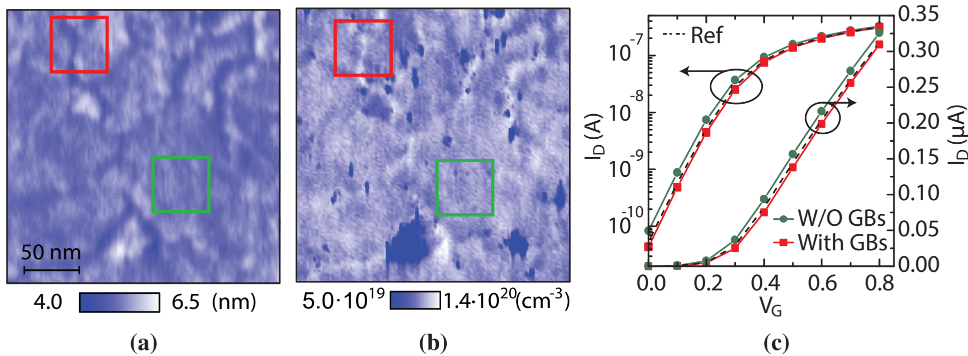


Figure 4.7: Topography (a) and charge density (b) maps, where two squares are highlighted one of them contains GBs (red square) whereas the other does not (green square). I_D-V_G characteristics simulated at V_D = 50 mV, where Red/green curves correspond to the simulated I_D-V_G curves of devices when dielectrics in the red/green squares in 4.7(a) and 4.7(b) are considered. Dotted curve corresponds to a reference device, with uniform HfO_2 thickness (5.3 nm) and trapped charge density (1.08 10^{20} cm^{-3}).

Finally, the development of NAMAS simulator has allowed is used to compare the impact of thickness and charge density fluctuations separately on the device variability. To do this, 90 maps of (W/L = 50/50 nm) from figures 4.1(a) and 4.6(a) are extracted, taking into account that their surfaces cannot be overlapped and that the breakdown areas are neglected.

From the 90 maps (topography and charge density) and applying the same procedure previously shown, 90 I_D-V_G curves are simulated and their V_{TH} calculated. Besides, in order to evaluate separately the impact of topography and charge density on V_{TH} variability,

topography and charge density data are individually introduced. That is, when the oxide thickness is used as variability source data in the simulator, the charge density data are hold as a constant value (the average of the sample 1.08 10^{20} cm^{-3}). On the same way, when the charge density variability data are introduced in the simulator as variability source, the oxide thickness is considered as a constant (the average of the sample 5.3 nm). Figure 4.8 shows the statistic distribution of V_{TH}, centering the mean in zero, when the thickness (line red), the charge density fluctuations (blue line) and both (black line) are taking into account in the simulation devices.

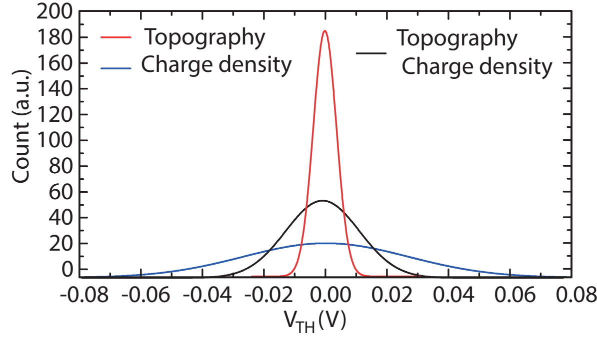


Figure 4.8: Statistical distribution of V_{TH} for simulated devices when topography (red line), charge density (blue line) or both (black line) nanoscale data are taken into account.

As it can be observed, the impact of oxide thickness fluctuations on V_{TH} variability is less than the impact of charge density, being the standard deviation due to the topography, $\sigma(V_{TH|T})$ = 3.9 mV and due to the charge density, $\sigma(V_{TH|CD})$ = 27.5 mV. In addition, the V_{TH} variability when both phenomena are considered at the same time is not the statistic sum of the impact of oxide thickness and charge density separately on V_{TH} variability. It can be explained because the charge density and topography are not independent variables (see inset figure 4.6(b)). Therefore, the total variability must be described by a bivariate normal distribution, whose expression is;

$$f(V_{TH|T}, V_{TH|CD}) = \frac{1}{2\pi\sigma(V_{TH|T})\sigma(V_{TH|CD})\sqrt{1-\rho^2}}$$
$$exp\left\{-\frac{1}{2(1-\rho^2)}\left(\frac{V_{TH|T}^2}{\sigma(V_{TH|T})^2} + \frac{V_{TH|CD}^2}{\sigma(V_{TH|CD}^2}) + \frac{2\rho V_{TH|T}V_{TH|CD}}{\sigma(V_{TH|T})\sigma(V_{TH|CD})}\right)\right\} \quad (4.4)$$

where $V_{TH|T}$ and $V_{TH|CD}$ are the V_{TH} due to topography and charge density respectively. ρ is the correlation coefficient of bivariate distribution, whose value indicates the grade of correlation between the variables, being 1 a perfect linear correlation and 0 is not a linear

correlation. Figure 4.9 shows a contour map where the x-axis represents the $V_{TH|T}$ and the y-axis the $V_{TH|CD}$. The colors of contour map represent the probability of distribution of the experimental data. Besides color lines are added, which are obtained using the bivariate equation (4.4) in order to compare the experimental results. The obtained correlation in this fitting is ρ = 0.86. The good match between color map and lines validates the assumption that the bivariate normal distribution describes the impact of topography and density charge on the V_{TH} variability.

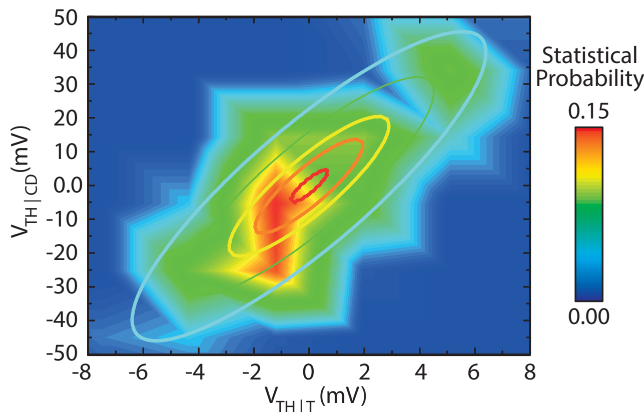


Figure 4.9: Contour map where $V_{TH|T}$ is plotted as a function of $V_{TH|CD}$. Color lines represent the fitting of experimental data to a bivariate normal distribution, being the correlation coefficient 0.86.

4.4. Summary and discussion

In this chapter, which is based on papers JVST-B (Jun-2015) and IEEE EDL (May-2017), the simulator NAMAS to generate thickness and charge density maps of polycrystalline gate oxides from CAFM experimental data has been explained. The proposed simulator were validated using experimental data. In particular, the extraction of density charge was validated by the comparison of KPFM measurements. This nanoscale information was used as input to a device simulator, which allowed to evaluate the corresponding I_D-V_G curves of MOSFETs. These curves show a clear device-to-device variability, as a result of the presence of GBs after crystallization. Besides, the V_{TH} variability due to the impact of thickness and density charge fluctuations in the gate oxide was analyzed separately indicating that this variability sources are not independent, and therefore they must be study using bivarite normal distribution. This proposed methodology to evaluate MOSFET variability can be extended to any dielectric whose electrical properties depend on thickness and defect density.

Chapter 5.

Analysis of trap physic parameters and their impact on device variability

To improve the performance of integrated circuits, the size of devices has been progressively reduced and, currently, the nanometer range has been reached. As a consequence of this scaling, the discreteness of charge is reflected in the electrical performance of devices, leading to device variability [73, 80]. For instance, charge trapping/detrapping in/from interface states can be observed in the form of RTN and/or BTI, which introduce random and/or permanent shifts in the V_{TH} [150, 151]. Therefore, understanding the physics behind this variability and how it impacts the device behavior is essential to introduce suitable countermeasures into the fabrication processes, device architecture and/or circuit design.

In this chapter, Atlas TCAD simulator, which was explained in chapter 2, and experimental data are used to explain how traps can impact on a MOSFET device *time-zero* and *time-dependent* variability. In particular, in the first section of the chapter, TCAD simulations and massive I_D-V_G experimental curves are used to give an explanation of the deviations of the Pelgrom's law (see chapter 1). In the second section, TCAD simulations are used to estimate the physical parameters that define the dynamic behavior of a trap ((E_{trap}), (σ_{trap}) and (Q_{trap})), from trap parameters whose values can be experimentally extracted ((τ_c), (τ_e) and ΔV_{TH}(IT)). Once the trap physical parameters are known, they could be used to study time-dependent variability such as RTN and BTI using TCAD simulations.

5.1. Dependence of MOSFETs threshold voltage variability on channel dimensions

Understanding the dependencies of V_{TH} time-zero variability of MOS devices constitutes a challenge that must be faced in order to optimize the circuit design to better performance. According to Pelgrom's law, MOSFET V_{TH} variability is inversely proportional

to the square root of the active transistor area [74]. However, significant deviations from this rule have been reported on experimental data, especially in 65 nm technologies and beyond [76, 77]. The origin of this deviation has been already studied, where several sources of variability, such as, RDF or/and interfacial traps, were pointed out as the possible reason of this mismatch [77, 149]. However, this matter was not fully clarified. In next section, experimental data indicating a deviation of Pelgrom's law are shown. In order to elucidate the physical origin of the different dependence TCAD simulations are performed, which suggest that the dimensions W and L should be decoupled of the Pelgrom's equation. Finally, a empirical model is proposed and validated.

5.1.1. Analysis from experimental data (V_{TH})

A large set of pMOS and nMOS devices of different W and L manufactured in a 65 nm CMOS technology were characterized. Table 5.1 indicates the number of *DUTs* tested for each device geometry. Note that in some cases W and L are fixed (yellow and green cells in table 5.1), which allows to study the V_{TH} variability when only one of the dimensions is swept. The studied geometries were chosen to cover the range of device areas allowed in this technology. The V_{TH} of each device is calculated by applying the constant current method to the devices I_D-V_G curves (V_D = 100 mV). The constant drain current is assumed as 10^{-7} x (W / L) A to determine V_{TH}.

	Experimental device dimensions W/L (nm)							
DUTs	592	16	16	16	36	36	36	36
W	80	200	600	800	1000	1000	1000	1000
L	60	60	60	60	60	100	500	1000

Table 5.1: Number of devices experimentally analyzed for each type (nMOS and pMOS) and W and L values used for the V_{TH} variability study.

Regarding the different geometries of experimental devices to study the dependence of $\sigma(V_{TH})$ with W and L, equation 1.12 was written as equation 5.1 or 5.2 for fixed values of L (L_{cte}) or W (W_{cte}), respectively.

$$\sigma(V_{TH})L_{cte} = \frac{A_{TH|L_{cte}}}{\sqrt{W}} \tag{5.1}$$

$$\sigma(V_{TH})W_{cte} = \frac{A_{TH|W_{cte}}}{\sqrt{L}} \tag{5.2}$$

Figure 5.1 shows the $\sigma(\mathrm{V_{TH}})$ when only the width or length is varied, figures 5.1 and 5.1(a), respectively. Experimental data (symbols) were fitted by equations 5.1 and 5.2 (lines), for n- (black) and p- (red) MOSFETs. As it can be observed, slopes ($A_{TH|L_{cte}}$ and $A_{TH|W_{cte}}$) are different for both nMOS and pMOS devices, specially for nMOS transistors, when W and L are independently varied. The exact values of the slopes are shown in table 5.2. Therefore, the different slopes indicate that to take into account correctly the variability dependence on device area, different dependence of σ(Vth) on W and L should be considered, unlike to the Pelgrom's law.

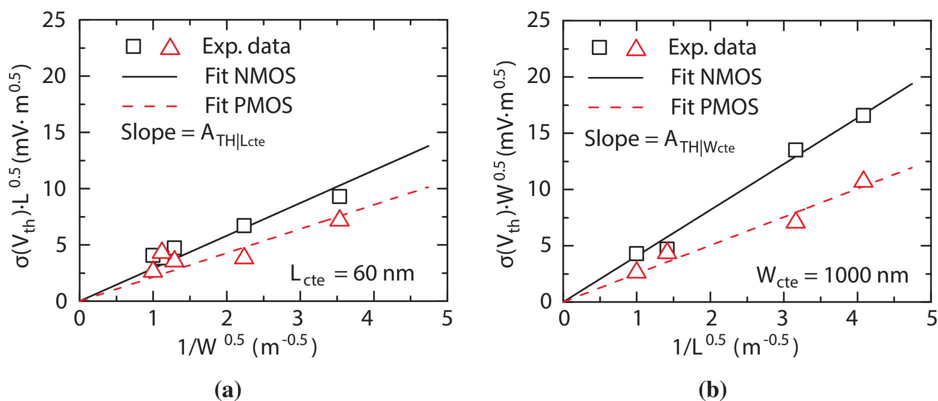


Figure 5.1: Experimental σ(Vth) (dots) as a function of 1/W$^{0.5}$ (a) and 1/L$^{0.5}$ (b). The lines correspond to linear fittings, with slopes in table 5.2.

	$\Delta\mathbf{V_{TH\|Lcte}}$	$\Delta\mathbf{V_{TH\|Wcte}}$
nMOS	$2.906 \cdot 10^6$ (mV $\cdot$ μm)	$4.088 \cdot 10^6$ (mV $\cdot$ μm)
pMOS	$2.138 \cdot 10^6$ (mV $\cdot$ μm)	$2.517 \cdot 10^6$ (mV $\cdot$ μm)

Table 5.2: Slopes of the linear fittings of the data in figure 5.1, to equations 5.1 and 5.2

5.1.2. Simulation procedure to reproduce $\mathrm{V_{TH}}$ variability in MOSFET

To elucidate the physical origin of the difference observed in the slopes of figure 5.1, and therefore, the deviations of the Pelgrom's law, TCAD simulations are performed with ATLAS Silvaco simulator. First, a nMOSFET structure is defined in the TCAD tool using gaussian doping profiles well-tempered from MIT [152] and an EOT = 2 nm. The mod-

els used in the simulations were: drift diffusion model to solve the transport, the Lombardi model (CVT) for carrier mobility, the Shockley-Read-Hall (SRH) model for recombination, and the Fermi-Dirac model for the carrier statistics. Figure 5.2 shows the net doping profile and the dimensions of the simulated device. Several devices with different W and L are considered. Table 5.3 shows the 4 selected values of L and W, which are combined to simulate 16 different areas.

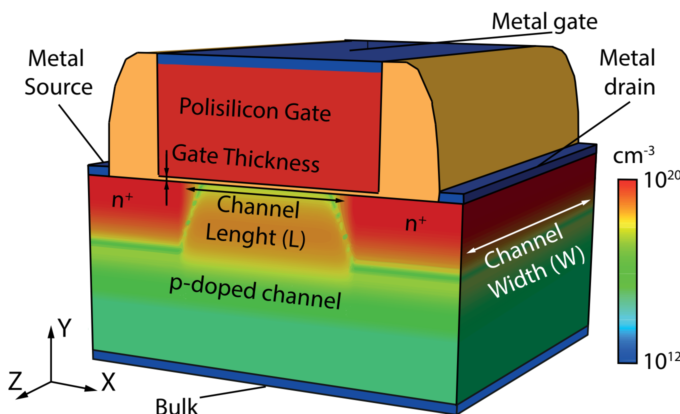


Figure 5.2: MOSFET simulated structure showing the net doping profiles. The main device parameters have been represented.

Once the I_D-V_G device characteristics can be simulated, the V_{TH} variability is introduced in the simulations. Since one of the main sources of device-to-device variability is associated to the presence of Discrete Fixed Charge (DFC) in the oxide or at the gate oxide/channel interface [149], the impact on V_{TH} of random distributions of these charges in the gate dielectric is evaluated for several device geometries. To simulate a DFC by TCAD, a trap always charged (fixed charge) at the gate oxide/channel interface with a value of Q_{trap} = 1e$^-$ was assumed. In order to reproduce the variability typically observed in the experimental data, the average of number of DFC ($\langle N \rangle$) introduced in the smallest device (50x50 nm) is assumed as $\langle N \rangle = 9$, being this value similar to other works [80, 83]. Notice that the $\langle N \rangle$ must be scaled in larger devices with area. In this way, the average of interface charge density (D_{it}) is kept constant in all the devices, with value $3.6 \cdot 10^{11}$ cm^{-2} and whose equation is 5.3. For devices with the same area, the number of DFC to each particular device (N) is calculated by mean of the generation of random numbers that follow a Poisson distribution with mean value $\langle N \rangle$ [73]. Besides, each of the fixed charges is randomly located at some position of the device interface.

$$D_{it} = \frac{\langle N \rangle}{W \cdot L} \tag{5.3}$$

	Simulated device dimensions W/L (nm)			
W	50	80	100	200
L	50	80	100	120

Table 5.3: L and W values considered for the V_{TH} variability study. A total of 16 areas was simulated

Figure 5.3 shows a current density map calculated at the oxide/channel interface of a device L/W = 80/200 nm in which N = 58 fixed charges (black points) are introduced. The applied bias were V_D = 0.1 V and V_G = 0.50 V, being the last value close to the average V_{TH} measured for this geometry. As it can be observed, the current density decreases near the DFCs. In some cases, the high population of traps located in small regions of the device interface blocks the current density in this area and originates percolative paths through the device. Therefore, a different DFC random distribution (in number and localization) is considered for each device, leading to a device-to-device variability of V_{TH}, which is analyzed below.

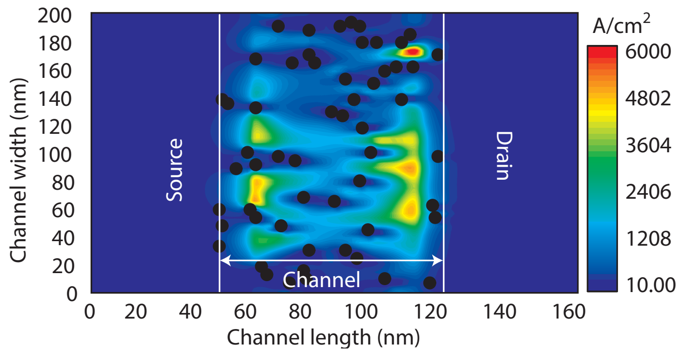


Figure 5.3: Current density map at the oxide/semiconductor interface when 58 DFC are randomly located. The biases applied are; V_D = 0.1 V and V_G = 0.50 V.

Figure 5.4 shows the dependence of the V_{TH} variability as a function of $1/W^{0.5}$ 5.4(a) and $1/L^{0.5}$ 5.4(b), for simulated devices with different L and W, respectively. As it can be seen, by changing the device dimensions, the slopes are modified with different dependencies. These results suggest that the statistical distribution of charges in the device leads to the V_{TH} variability and to deviations of Pelgrom's law as those observed experimentally in figure 5.1.

Of course other variability sources also contribute to this effect.

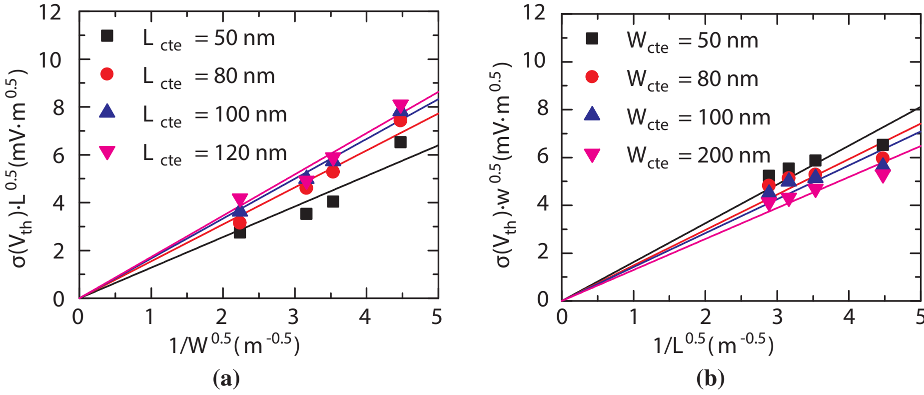


Figure 5.4: Simulated σ(Vth) (symbols) as a function of 1/W0.5 (a) and 1/L0.5 (b). The lines correspond to linear fittings.

Once the random charge distribution in the oxide is demonstrated to be a V_{TH} variability source, which leads to deviations from the Pelgrom's law, further simulations are performed to elucidate the possible origin of such asymmetry in the L and W dependences. To do this, and for simplicity, one DFC is swept along the channel length and width of the device and its impact on the V_{TH} is evaluated. Figure 5.5 shows TCAD simulations of the change in the device of V_{TH} (ΔV_{TH}) when a DFC is swept along L and W of the device, figures 5.5(a) and 5.5(b) respectively. Notice that devices with several geometries are considered, so that the normalized trap location is plotted in the x-axis of both graphics. It can be seen, the impact of the DFC on V_{TH} depends on the charge position along L, especially for shorter devices, black and red curves in figure 5.5(a). On the other hand, when the DFC is swept along W, the value of V_{TH} remains essentially constant. This asymmetry in the V_{TH} impact, depending on the trap location along W or L, is assumed to be the root of the differences observed in figure 5.1.

5.1.3. Empirical model to describe the dependence of the V_{TH} variability ion channel dimensions

Since V_{TH} variability for ultra-scaled devices seems not to follow Pelgrom's rule, for a better fitting of the data, the dependences of V_{TH} variability on W and L are decoupled, proposing the equation 5.4 to describe the V_{TH} variability. In this expression α and β are free fitting parameters that are used to take into account the different dependence of σ(Vth) on L and W.

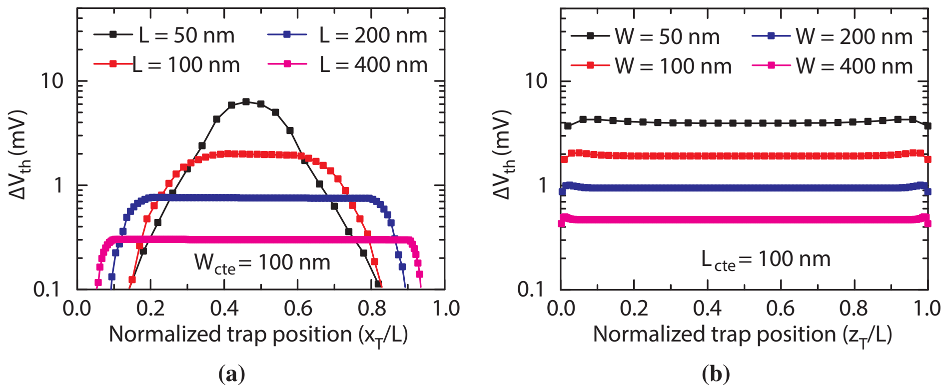


Figure 5.5: TCAD simulation of the change in the device V_{TH} (ΔV_{TH}) when a DFC is swept along the channel length (a) and width (b) of the device. Devices with several dimensions are considered, so that the normalized trap location is plotted in the x-axis of both graphics.

$$\sigma(V_{TH}) = \frac{B_{TH}}{W^{\alpha} L^{\beta}} \tag{5.4}$$

With the aim of comparing the goodness of model and Pelgrom's law, in figure 5.6 the fittings of V_{TH} variability obtained experimentally in nMOS (figures 5.6(a)/5.6(b)) and pMOS (figures 5.6(c)/5.6(d)) to Pelgrom's law (5.6(a), 5.6(c)) and our model (5.6(b), 5.6(d)) are shown. As it can be observed, for all devices, the proposed model reproduces better the data.

To compare quantitatively the fittings, the α, β, A_{TH}, B_{TH} and R-square coefficients parameters were calculated (see Table 5.4). For both cases (nMOS and pMOS), the error obtained using the proposed model is lower than that obtained with the Pelgrom's law. Note that the new incorporated coefficients, α and β , could depend on the technology. Therefore, the empirical proposed equation could be used to estimated more accurately the time-zero variability to ulta-scale devices.

	Fit parameters)				**R-square**	
Unit	-	-	mV· μm	mV· μm$^{\alpha+\beta}$	-	-
nMOS	0.342	0.493	$2.95 \cdot 10^6$	$4.03 \cdot 10^5$	0.907	0.994
pMOS	0.329	0.578	$2.15 \cdot 10^6$	$3.89 \cdot 10^5$	0.816	0.897

Table 5.4: Slopes of the fittings of the experimental data in figure 5.1 to equations 1.12 and 5.4.

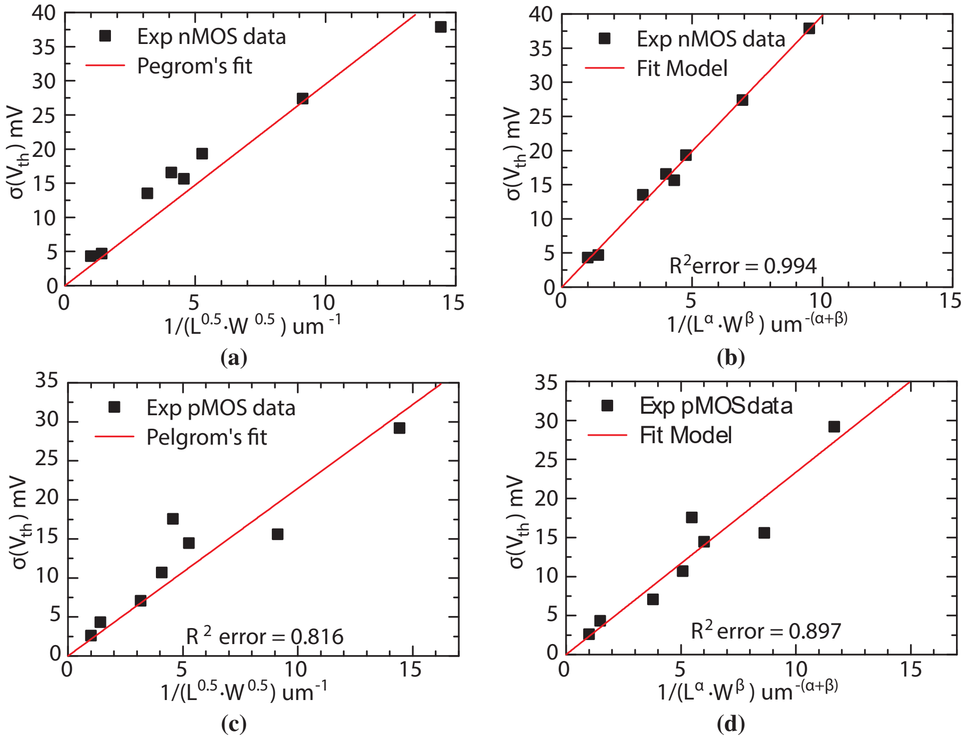


Figure 5.6: Comparison between the fittings the Pelgrom's law ((a), (c)) and the proposed model ((b), (d))

5.2. Methodology to extract interface traps parameters for TCAD simulations

In the previous section, time-zero variability was associated to the presence of DFC or traps (always charged) with a value of Q_{trap} = 1e⁻ in the oxide/channel interface. However, the study of time-depend variability requires that the traps have a dynamic behavior (charging and discharging) along the time. TCAD simulations can be a fast and adequate approach to evaluate, from experimental data, the statistic impact of interface traps on the V_{TH} shift of a MOSFET device. To do that, in addition to Q_{trap}, two extra physical parameters, the energy of trap E_{trap} and the effective cross section σ_{trap}, must be defined in the simulation. In this section this kind of traps are called Interface trap (IT), because unlike of DFC, the IT can be charged or discharged. Nevertheless, these physical parameters differ from those that can be experimentally obtained, such as capture τ_c and emission τ_e times and single trap induced threshold voltage shift (ΔV_{TH}(IT)). In this section, a procedure to translate the empirical trap parameters (τ_c, τ_e and ΔV_{TH}) into the main TCAD physical parameters (E_{trap}, σ_{trap}

and Q_{trap}) is explained.

5.2.1. Calibration of simulated MOSFET from experimental I_D-V_G curve

On the same way that in previous section (5.1.2), a bulk nMOSFET structure is defined in ATLAS TCAD using the same simulation models. In this case, the simulated device is calibrated using experimental I_D-V_G curves measured in transistors (W/L=300 nm/300nm). Figure 5.8(a) shows the adopted flow diagram for device calibration procedure. First, since simulation time in 2D is shorter than in 3D, 2D devices are simulated using the nominal device parameters and gaussian doping profiles. The error between the simulated and one representative measured I_D-V_G curve is minimized by varying doping and other technological parameters (as the EOT or underlapping length). When the 2D calibration is finished, that is, when the error is less than a given value set by the user (1% in this thesis), the final 2D fitting parameters are saved. Then, this parameters are used as initial parameters in 3D simulations, where the same algorithm was repeated. This procedure reduces the computation time (hours) because most of the simulations are performed in 2D. Figure 5.8(a) shows the net doping profile and some dimensions of the device obtained after the calibration. Figure 5.8(b) shows the final simulated (red line) and measured (black squares) I_D-V_G curves in linear and logarithmic scale; the good agreement validates the calibration procedure.

Considerations of the simulation

The I_D-V_G characteristics in figure 5.8(b) are considered as reference, and the effect of additional IT on the device (V_{TH}) is analyzed. As can be observed in figure 5.8(b), the V_{TH} ($\sim 0.37V$) is calculated by applying the constant current method, where the constant drain current is assumed as 10^{-6} A. To improve the simulation accuracy, around the IT location the mesh is refined (steps of 1 nm). Multiple traps (N_{trap}) are expected in the device interface, which are characterized by their E_{trap}, σ_{trap} and Q_{trap}, and whose spatial distribution and number change from device-to-device. Traps in the oxide bulk are not taken into account in this work because their effect could be estimated using the presented approach by simply considering interface traps with different trapped charge. Moreover, other sources of variability as RDF or LER, whose effects could be combined with ITs [73], have not been considered in this work in order to analyze exclusively the ΔV_{TH} related to ITs. Notice that although these phenomena are not considered, they only affect to calculate the parameter Q_{trap}. Besides, the RDF effect on V_{TH} variability could be included in the proposed methodology, since RDF could be somehow equivalent to the ITs introduced in the oxide,

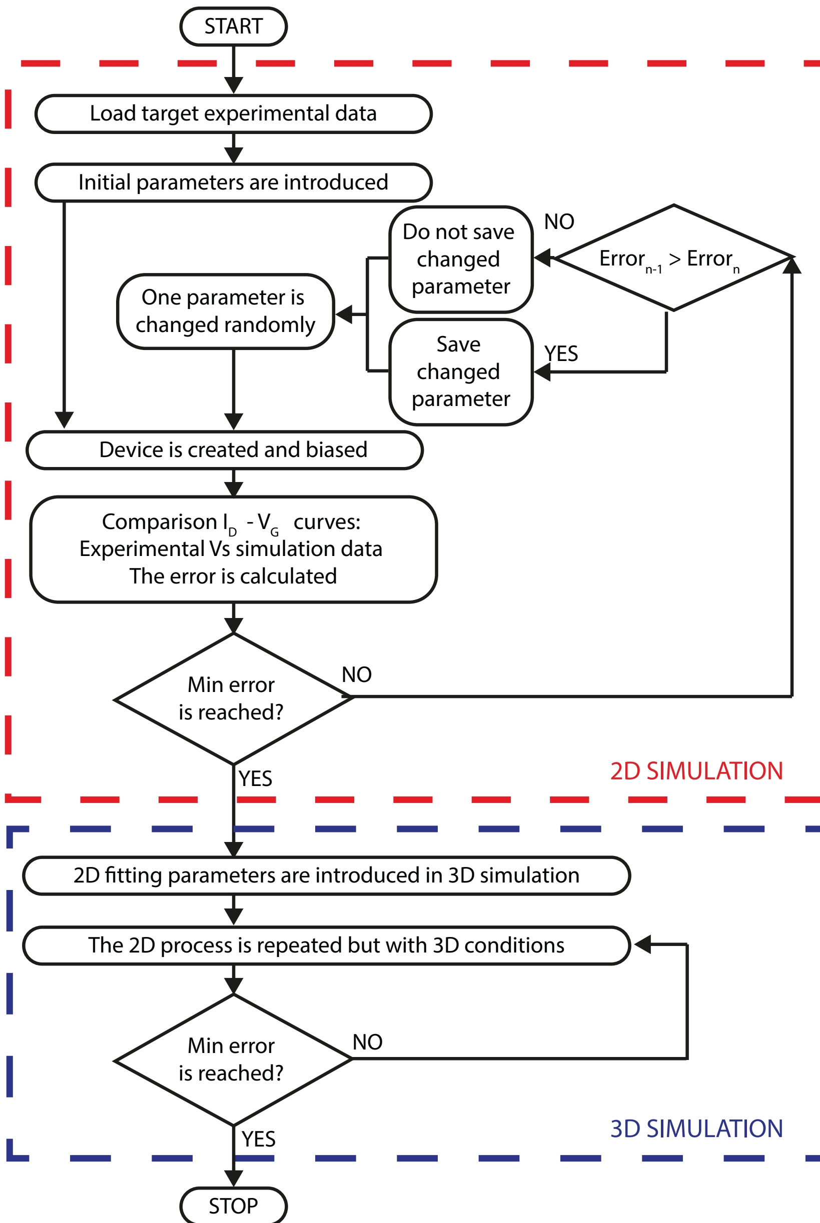


Figure 5.7: Flow diagram of the TCAD device calibration procedure.

affecting the Q_{trap} parameter. Regarding LER, further characterization and analysis should be considered to include this variability source in the simulation procedure.

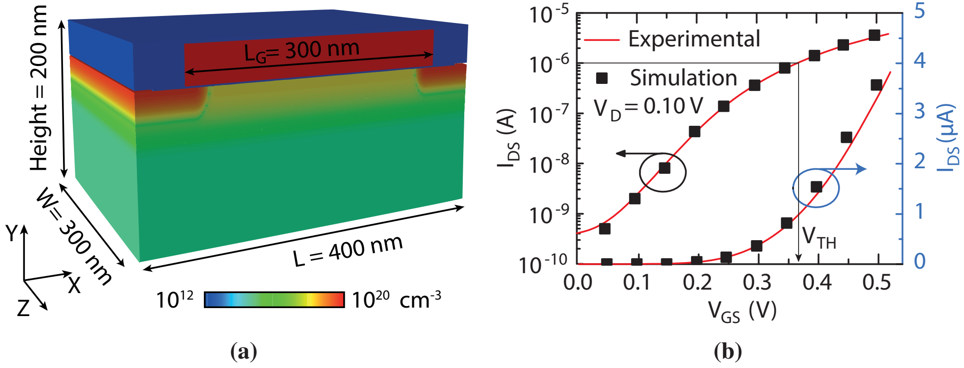


Figure 5.8: MOSFET structure showing the net doping profile (a). Experimental (black squares) and simulated (red lines) I_D-V_G curves of the device (b). The nominal V_{TH} of the device is 0.37 V and the estimated EOT is 1.5 nm.

5.2.2. Q_{trap} estimation by static simulations

To estimate Q_{trap} parameter of trap, the contribution to the device ΔV_{TH} of each IT is evaluated by mean of static simulations. These simulations are performed introducing IT in several reference devices (previously fitted) and calculating for each introduced IT their impact in the V_{TH}. Figure 5.9(a) shows an example of simulated current density map at the oxide/semiconductor interface for one device with N_{trap} = 12 and Q_{trap} = e^-. Numbers indicate the order in which the traps were introduced in the simulated device. On the same way that in previous section (5.1.2), the current density decreases near the ITs, leading to a change of V_{TH}. Figure 5.9(b) shows how each trap in figure 5.9(a) individually impacts the device V_{TH}, introducing a ΔV_{TH}(IT). Note that ΔV_{TH}(IT) varies from trap to trap. The trap impact on V_{TH} depends on its position within the channel (see section 5.1.2): traps in the channel (i.e. 1, 2, 4, 6, 7, 11) cause larger ΔV_{TH}(IT) than traps closer to the source/drain contacts (i.e. 3, 5, 8, 9, 10).

To evaluate the value of Q_{trap}, the simulation of 20 devices for 4 different values of Q_{trap} (0.25, 0.50, 0.75, 1 times the electron charge) was performed and the ΔV_{TH}(IT) of all devices was measured. Notice that Q_{trap} values lower than 1 e^- should be interpreted as traps which are deeper in the oxide bulk, having a lower impact on V_{TH}. The number of traps for each device (N_{trap}) is assumed to be Poisson distributed, with an average N_{trap} = 12. This value represent a D_{it} = 1.3 · 10^{-10} to Q_{trap} = 1 e^-, being this value similar to other works [80, 83]. Also, their position along the interface is randomly selected. Figure 5.10(a) shows the statistical distribution taking into account the data of 20 devices for each Q_{trap} value. Note that, when Q_{trap} increases the distributions shift towards larger values (higher ΔV_{TH}(IT) by IT, though their slopes seem to remain constant. Experimental data from [150]

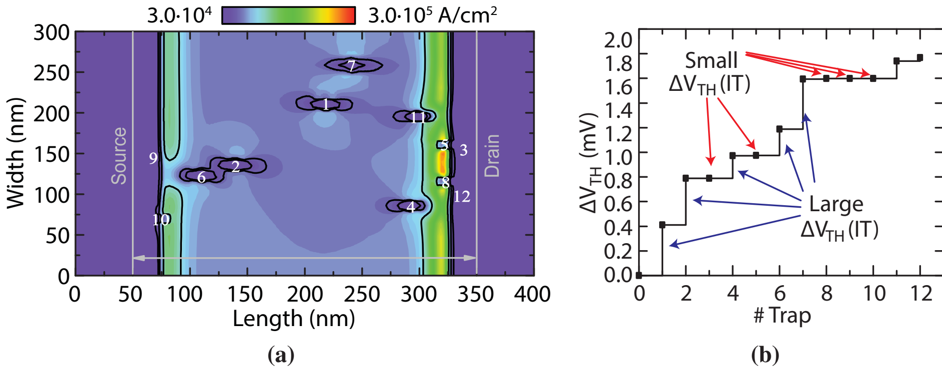


Figure 5.9: Current density map at the oxide/semiconductor interface when 12 ITs are randomly located (a). Total ΔV_{TH} of the device due to ΔV_{TH}(IT) induced by each introduced trap (b)

are plotted in order to compare the distribution obtained. The distributions of figure 5.10(a) were fitted to a Weibull distribution [93], equation 5.5

$$f(\Delta V_{TH}(IT), \eta, \beta) = \frac{\beta}{\eta}\left(\frac{\Delta V_{TH}(IT)}{\eta}\right)^{\beta-1} e^{\left(-\frac{\Delta V_{TH}(IT)}{\eta}\right)^{\beta}} \tag{5.5}$$

where β is the shape parameter and η is the scaling factor, which is related to the average $\langle \Delta V_{TH}(IT)\rangle$. Moreover, the variance σ 2 of the ΔV_{TH}(IT) is given by equation 5.6 [93],

$$\sigma^2 = 2\eta \langle \Delta V_{TH}(IT)\rangle \tag{5.6}$$

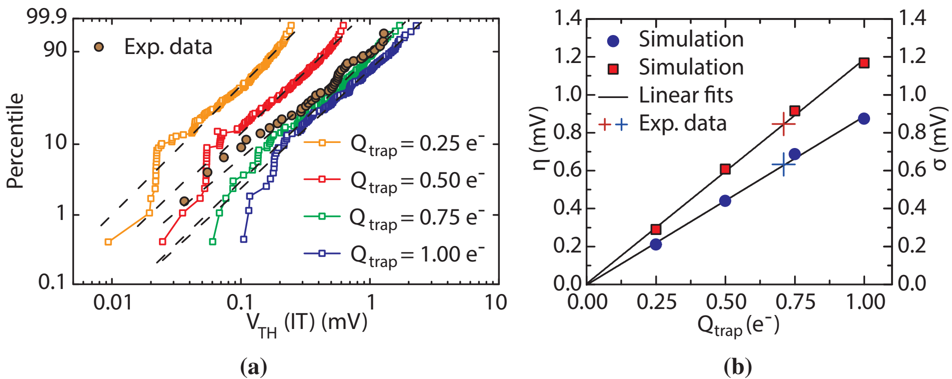


Figure 5.10: Statistical distributions of ΔV_{TH}(IT) obtained in 20 devices with average N_{trap} = 12 (Poisson distributed) and random spatial distribution for 4 values of Q_{trap}. Discontinuous lines represent the Weibull distribution fits (a). Plots of the scale parameter η and standard deviation σ vs. Q_{trap} (b) of the Weibull distributions in (a).

The η and σ values obtained from the simulated distributions in figure 5.10(a) are ex-

tracted and plotted vs. Q_{trap} in figure 5.10(b) (circles and squares). As can be seen, the η and σ increases linearly with Q_{trap}, being their slopes equal to 0.80mV/e$^-$ and 1.07mV/e$^-$ respectively. These two parameters can be obtained from measurements, so that their comparison to the simulated data (figure 5.10(b)) allow to obtain the Q_{trap} value that better represents the experimental behavior observed in the considered technology. In particular, the experimental data from [93] give a Q_{trap} = 0.72, which can indicate that some charges are not in the interface oxide / channel. So, the experimentally observed (statistically distributed) effect of ITs on the device ΔV_{TH} (ΔV_{TH}(IT)), which depends on the random spatial location of traps, can be fitted using Q_{trap} as single fitting parameter.

5.2.3. E_{trap} and σ_{trap} by transient simulation

In this section, the relation between the trap parameters σ_{trap} and E_{trap} (in TCAD tool) and (experimental data) τ_e and τ_c is described. 2D-transient simulations are performed considering one acceptor trap, i.e. E_{trap} is defined as the energy below the conduction band, in the center of the channel and using σ_{trap} and E_{trap} input parameters. Figure 5.11 (black squares) shows the occupancy probability ($(P_{occ}(t))$) of the trap, for an electron capture cross section σ_{trap} = 10^{-15} cm^2 and energy level E_{trap} = 0.15 eV, when the gate applied bias (blue line) is changed from V_G = 0.10 V to V_G = 0.20 V (at time 0 s) and back to V_G = 0.10 V (at time 1 ns) with V_G = 0.10 V. Notice that ramp voltages are performed in 30 ps.

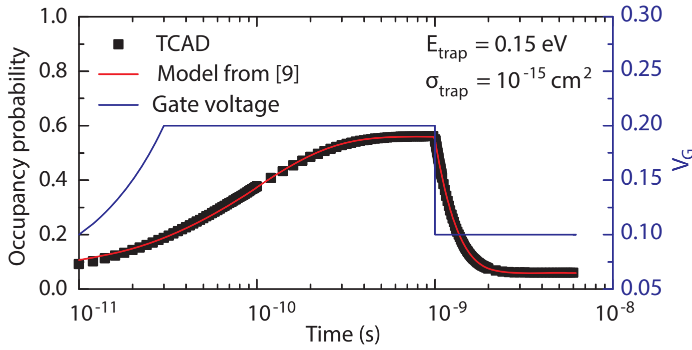


Figure 5.11: Trap occupancy probability obtained during a transient simulation (black squares) and the analytic model (equation 1.14 fit(red lines), when the gate voltage applied is changed (blue line). Notice that ramp voltages are performed in 30 ps.

The simulated results (black squares) are fitted to an analytic model (equation 1.14) to obtain the corresponding τ_e and τ_c, which are assumed to describe the occupancy probability of a trap during a BTI stress [86]. Figure 5.11 shows the fitting of the TCAD simulation

(black squares) to the analytic model equations (red line), from which τ_e (V_G = 0.20 V) = 0.45 ms, τ_c (V_G = 0.20 V) = 0.35 ms, τ_e (V_G = 0.10 V) = 0.10 ms and τ_c (V_G = 0.10 V) = 1.61 ms were obtained. To consider traps with different properties, E_{trap} and σ_{trap} parameters were swept (σ_{trap} from 10^{-14} to 10^{-17} cm^2 and E_{trap} from 0.05 to 0.25 eV) and the associated τ_e and τ_c evaluated, using the same procedure shown in figure 5.11. Figure 5.12(a) shows a (τ_e-τ_c) map obtained for V_G = 0.20 V and V_D = 0.10 V. The results show that τ_c is reduced when E_{trap} is increased, whereas the opposite behavior is observed for τ_e, indicating that the electrons can be more easily captured in/emitted from deep/shallow traps. Moreover, Figure 5.12(a) also shows that both times decrease when σ_{trap} is increased. Once this kind of plot is constructed, the associated (σ_{trap} - E_{trap}) for a given experimental (τ_e-τ_c) can be evaluated. An arbitrary example (yellow star) is shown where τ_c = 0.2 ms, τ_e = 3 ms are considered as experimental parameters, so that E_{trap} = 0.22 eV σ_{trap} = 10^{-16} cm^2 are found.

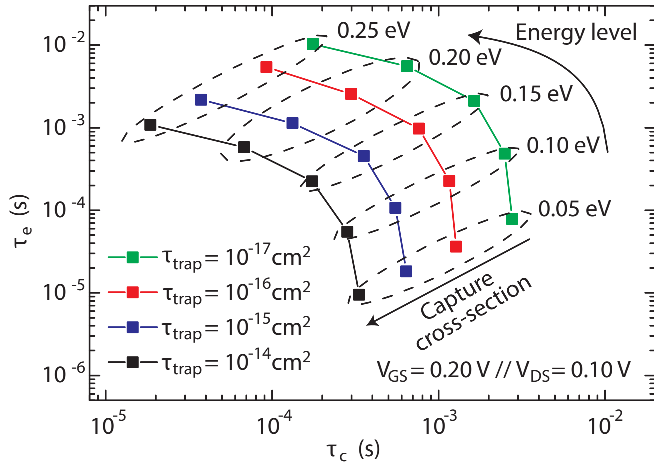
Once the TCAD parameters (E_{trap}, σ_{trap}), which are independent of operation conditions, of a trap characterized by (τ_e-τ_c) at a given voltage are obtained, they can be used to calculate the τ_e,τ_c) at other voltages and temperatures without the need of experimental data at those new conditions. As an example, figure 5.12(b) shows how the (τ_e,τ_c) map plotted in figure 5.12(a), represented as blue surface, changes if the gate voltage is increased from 0.2 to 0.3 V (red surface). V_D is remained constant at 0.10 V. Notice that, when the gate voltage is increased, capture times are reduced, and the emission times are increased for lower E_{trap} values and are kept almost constant for higher E_{trap} values, in agreement with [153]. The same methodology would apply for different operation temperatures. Therefore, these results show that, given an experimental (τ_e,τ_c) distribution at given bias/temperature conditions, the associated TCAD parameters can be obtained and then used to simulate the same device under different operation conditions, simplifying the characterization process. Therefore, the trap statistical effect on the device electrical characteristics at different conditions, also out of the experimental window, could be studied easier.

5.3. Summary and discussion

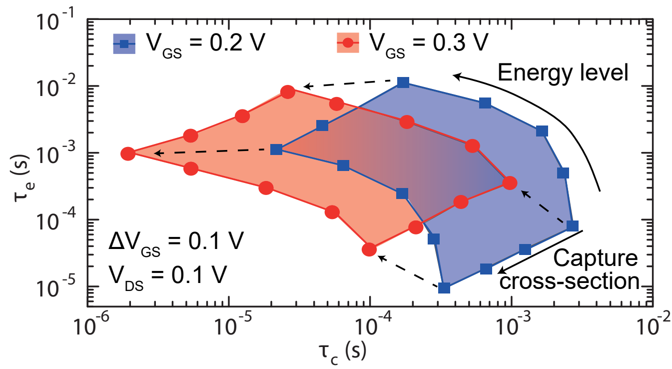
This chapter is based on the conference EUROSOI-ULIS (Mar-2017) and the paper IEEE MEE (Apr-2017), where analysis of trap physic parameters and their impact on device variability is study. In the first section, massive I_D-V_G experimental curves and TCAD simulations are used to evaluate the time-zero variability (due to trapped charges) of V_{TH} for several geometries, which is usually fitted by the Pelgrom's scaling law. However, the exper-

imental results, point out a deviation from this law for 65 nm technology. In order to clarify the origin of this deviation, TCAD simulations have been performed to evaluate the impact of random distribution of DFC on the device V_{TH}. The results show that this source of variability leads to deviations from Pelgrom's law, which could be related to the different impact on V_{TH} of charges depending on their location along W and L. Taking this into account, an empirical equation is proposed to fit the data, in which two parameters are introduced to separately account for the W and L dependence. With the proposed equation, better fits of the experimental data are obtained in the analyzed area range.

In the second section, an interface trap parameter extraction procedure has been presented, which allows efficient statistical TCAD simulations of their effects in the MOSFET V_{TH} variability. In particular, the methodology evaluates the physical parameters that describe the interface trap behavior in TCAD simulators (E_{trap}, σ_{trap} and Q_{trap}) from typical experimental (BTI or RTN) data (τ_e,τ_c and ΔV_{TH}(IT)). First, traps are included (with a number that is Poisson distributed) as fixed charges, randomly located at the interface, and the change in the V_{TH} induced by each trap is calculated. The comparison of the experimental and simulated statistical distributions of this magnitude allows determining the value of the charge per trap that better describes the experiments. To account for the trap dynamics, transient simulations were performed, where the trap energy and cross section were input parameters. The occupancy probability of the traps was obtained by fitting the simulation transient results to an analytical model. From the fittings, the relationships between (E_{trap}, σ_{trap})and (glsTe,τ_c) are obtained. The values of (glsTe,τ_c) at other bias/temperature conditions can be also obtained through simulation (without the need of additional experimental data), leading to a complete set of parameters with less experimental effort. Once these parameters are available, a statistically representative number of devices can be simulated, allowing the study of RTN and/or BTI related variability through TCAD simulations, in reasonable computing times.



(a)



(b)

Figure 5.12: Capture and emission times extracted from simulations with different E_{trap} and σ_{trap}. Applied voltage in all simulations was $VV_G = 0.20$ V and $VV_D = 0.10$ V. Yellow star shows an arbitrary example where experimental $\tau_c = 0.2$ ms, $\tau_e = 3$ms are considered, with corresponding $E_{trap} = 0.22$ eV $\sigma_{trap} = 10^{-16}$ cm^2 (a). (τ_e, τ_c) maps for different V_G (0.20 (red) and 0.3 V (blue)). Arrows indicate how the points shift when the V_G is changed (b).

Chapter 6.

Analysis of UTBB FD-SOI MOSFET Inverters operated at NTV

In chapter 1, an overview about the structure and main characteristics of UTBB FD-SOI MOSFET were explained. In particular, the UTBB FD-SOI MOSFET technology is suggested as a promising candidate to improve the power consumption operating in NTV [58]. On the other hand in chapter 5, how the trapped charges in the gate oxide impact on the electric behavior in bulk devices was described. This chapter tries to go one step further and studied an inverter logic gate based on UTBB FD-SOI MOSFET devices. Specifically, the static and dynamic energy consumption of an inverter logic gate operating in NTV are estimated using Silvaco TCAD simulations. Two structural parameters of the device, i.e., channel thickness (T_{SI}) and BOX oxide thickness (T_{BOX}), and one operation parameter (V_{BB}), are considered to optimize the energy consumption of the inverter gate. These results could be assumed as a reference to be extended to more complex circuits. Finally, the impact of a trapped charge in the gate and BOX oxide interfaces on energy consumption and operation frequency of the inverter gate is studied through simulations.

6.1. Device simulation

In order to simulate a UTBB FD-SOI MOSFET 28 nm device the structure and doping data of devices from [63, 154] where different simulations and experimental are presented for UTBB FD-SOI MOSFET technology are considered. Besides, similar V_{BB} values to those reported in [154] are chosen. Table 6.1 shows a summary of the dimensions and doping taken into account in this work for a n-type device. For the simulation of a logic gate CMOS balanced circuits was assumed [62], the p-type device is considered to have the same electric behavior (i.e., same currents and capacitances for the same applied voltages) than the n-type transistor and therefore it is not needed to be simulated in TCAD, saving computational

time. Figure 6.1 shows the 3D simulated structure, the net doping level in the channel and the metallization contacts for n-type device.

Parameter	Value	Parameter	Value
Oxide thickness (T_{OX})	*1.5 nm*	Channel thickness (T_{SI})	*(10 - 25) nm*
Box thickness (T_{BOX})	*(10 - 25) nm*	Substrate thickness (T_{SUB})	*60 nm*
Gate length (L_G)	*28 nm*	Substrate doping (S_{DOP})	10^{16} cm^{-3}
Channel doping (T_{BOX})	$3 \cdot 10^{18}$ cm^{-3}	Device Width (W)	*100 nm*
Back Biasing Voltage (V_{BB})	*(0-4) V*	Device Length (L)	*50 nm*

Table 6.1: Parameters considered in the simulations.

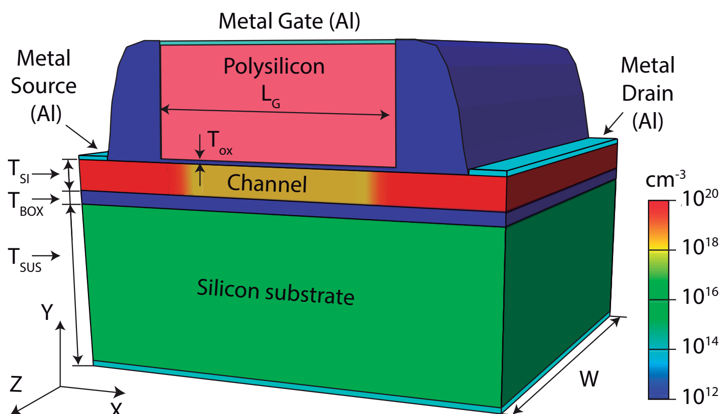


Figure 6.1: 3D TCAD structure of the simulated device showing the doping profile (not at scale)

For the simulations, a non-regular mesh is considered in the structure in order to have a resolution less than 1 nm under the gate in the Y-axis and (1-2) nm in the X-axis and Z-axis. Thus, the electric potential can be accurately calculated when the impact of one trap on the device performance is studied. Besides, a refined meshing in the channel is carried out proportional to the gradient of the doping profile. Once the structure is defined, the models needed to simulate the device are chosen considering the next assumptions:

1. **Energy balance model:** as it was explained in chapter 2, in order to perform more realistic simulations of the sub-100 nm UTBB FD-SOI MOSFET device, energy balance model must be assumed insted of drive-diffusion model, because it takes into account non-local effects such as velocity overshoot, diffusion associated with carrier

temperature gradients and the dependence of impact ionization rates on carrier energy distributions [155].

2. **Quantum effects:** due to the ultra-thin channel, significance of quantum confinement of carrier becomes conspicuous, therefore the quantum effects are taken into account. They are introduced using density gradient quantum correction.

3. **Recombination model:** Shockley-Real-Hall (SRH) recombination is considered in all simulations.

4. **Impact ionization model:** the Selberherrs model is assumed because it includes temperature dependent parameters.

Figure 6.2(a) shows the comparison between the simulated I_D-V_G curves of the UTBB FD-SOI MOSFET device performed with 3 different models; drive-diffusion (DD) (black line), energy balance (EB) (red line) and energy balance and quantum effects (EB + SCH) (green line). Notice that the most complete model (EB + SCH) converge to the simplest model when the temperature of carriers and the quantum effects are neglected, and as it can be seen there are differences between the models, which indicates that (EB + SCH) model must be used in order to performce more accurate simulations. Therefore, all simulation in this chapter are carried out using the energy balance transport model and quantum effects. Figure 6.2(b) shows different I_DV_G curves for a nMOS device (T_{SI} = 15 nm, T_{BOX} = 15 nm and V_{DS} = 0.1 V), for several V_{BB} from 0 to -4 V. Obtained current values are compatible with other works [17], [18], where devices of the same technology are studied. As it can be seen, when the $|V_{BB}|$ increases, I_DV_G curves show less current through the device modifying the V_{TH}. Figure 6.2(c) shows the V_{TH} variation as a function of V_{BB} where a linear relationship is found. Notice that the V_{TH} values range between 0.1 to 0.3 V, for the considered V_{BB} range.The V_{TH} is calculated from I_DV_G curves applying the extrapolation in the linear region method. Similar correlations of V_{BB} with V_{TH} has been reported in [156]. Therefore, the analysis shown until now demonstrate that the structure, models and simulations are representative of the UTBB FD-SOI MOSFET devices.

6.2. Simulation of UTBB FD-SOI MOSFET inverter power consumption

In this section the power consumption of a UTBB FD-SOI MOSFET inverter is simulated by Atlas TCAD simulator. To determine the energy consumption, two power dissipation

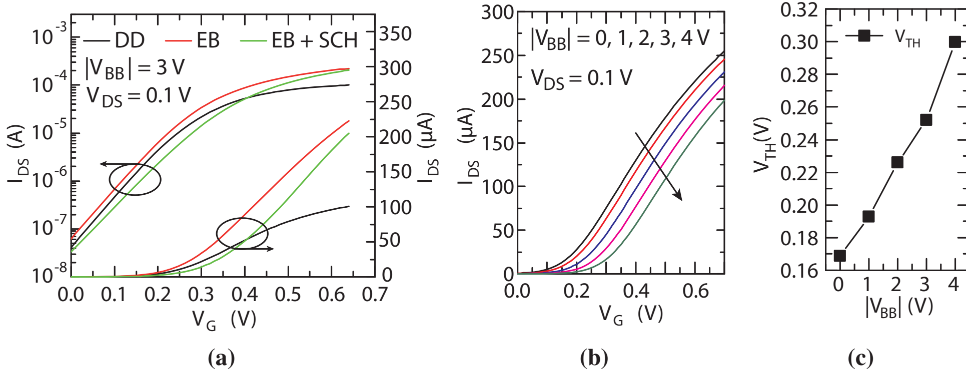


Figure 6.2: Comparison of simulated I_D-V_G curves of the UTBB FD-SOI MOSFET device performed with 3 different models; drive-diffusion (DD) (black line), energy balance (EB) (red line) and energy balance and quantum effects (EB + SCH) (green line) (a). I_DV_G curves simulated for several $|V_{BB}|$ for an MOSdevice (T_{SI} = 15 nm, T_{BOX} = 15 nm and V_{DS} = 0.1 V) (b) (b). The V_{TH} obtained from $_DV_G$ curves, as a function of $|V_{BB}|$ (c).

mechanisms in an CMOS logic gate must be taken into account: the static power consumption (P_S), which is the result of the leakage current through the contacts of the devices in the circuit for the two logical states, and the dynamic power consumption (P_D), which is calculated by considering a capacitive load that is charged and discharged when the logic gate is switching. To evaluate this power consumption, a circuit simulator such as SPICE can be used, considering a compact model to describe the electrical behavior of devices [61]. However, in this work, instead of a compact model, a TCAD simulator is used to evaluate the leakage currents at all contacts and the parasitic capacitances required to calculate the power consumption. The key advantages of using TCAD simulation instead of compact models are that all device parameters can be changed easily, what allows parametric studies, and the parameters introduced in TCAD have a physical meaning. For instance, variability sources such as bias temperature instabilities BTI or random telegraph noise RTN can be introduced in the simulation, changing the physical parameters (trap parameters) which describe these phenomena, as it is performed in the chapter 5. As main drawback, the TCAD simulations consume more computational resources than compact models and therefore complex circuits cannot be easily simulated.

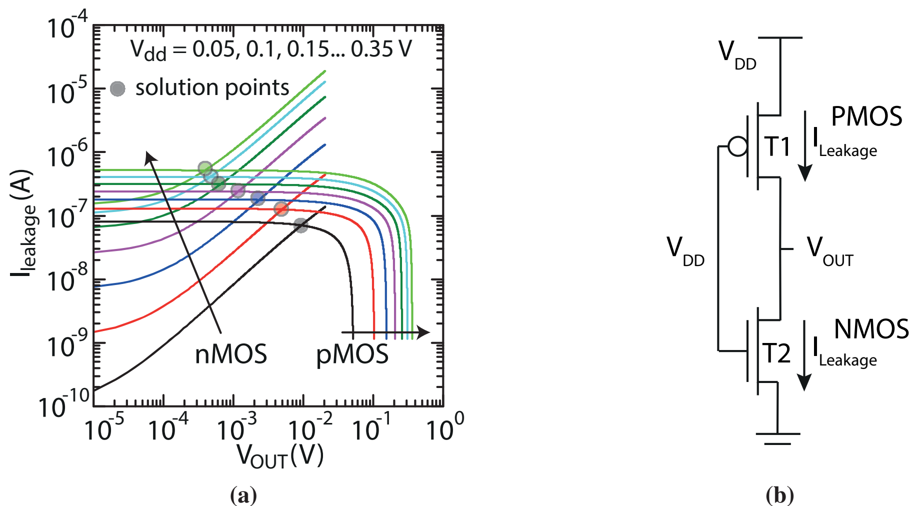
6.2.1. Static energy consumption of a UTBB FD-SOI MOSFET Inverter

The static power consumption is a function of supply voltage (V_{DD}) and leakage current ($I_{leakage}$) flowing through the devices. The drain-source current is considered as main con-

tributions to the leakage current. Other leakage current contributions, such as gate and bulk leakage current, are neglected, because the applied voltages are close to the threshold voltage.

Figure 6.3(a) shows the $I_{leakage}$ simulated for the n-type device as a function of output voltage of the inverter (V_{OUT}), for different V_{DD}. These curves are estimated when the output of the logic gate is logic "0", i.e., the nMOS device is ON and pMOS OFF. Notice that pMOS device is considered electrically equivalent to the nMOS 6.3 and therefore it is not simulated, saving computational time.

Taking as reference the circuit shows in figure 6.3(b), the crossing points of the curves in figure 6.3(a) represent the circuit solution, where the $I_{leakage}$ flowing through both transistors is the same, for a given V_{OUT}. Note that in the case of evaluating the configuration of a logic "1", the voltages applied to devices would change, being nMOS in the OFF state and pMOS in the ON state.



(a) **(b)**

Figure 6.3: $I_{leakage}$ as a function of V_{OUT} for different V_{DD} in an inverter logic gate (b). The crossing points for the nMOS and pMOS curves represent the solution points of the circuit, where $I_{leakage}$ of both devices are equal. Scheme of the inverter gate, highlighting $I_{leakage}$ for each transistor and V_{OUT} (b).

The equation used to calculate the static power consumption is;

$$P_s = I_{PMOS}(V_{DD} - V_{OUT}) + I_{NMOS}(V_{OUT} - 0) \tag{6.1}$$

where I_{PMOS} and I_{NMOS} are the currents flowing through the devices. To calculate the energy consumed per cycle, the power consumption is multiplied by the propagation delay

(t_p) of one cycle, which can be calculated from the dynamic analysis in the next described section.

6.2.2. Dynamic energy consumption of a UTBB FD-SOI MOSFET Inverter

CMOS dynamic power consumption is due to the current that flows when the inverter is switching from one logic state to the other. In order to estimate this energy consumption, the t_p is evaluated using a lumped load capacitance to ground (C_L). This load capacitance is the sum of all interconnect capacitances (including gate-drain capacitance (C_{GD}), drain-bulk capacitance (C_{DB}) and fan-out gates (C_G), (see figure 6.4(a)) connected to the output of the CMOS circuit [59]. Figure 6.4(b) shows an example of gate parasitic capacitance as a function of gate voltage calculated by TCAD simulator. The other capacitances are also simulated and C_L calculated. The fan-out of the logic gate is considered equal to 1. The equation that allows to calculate the dynamic energy consumption is;

$$E_d = C_L V_{DD}^2 \tag{6.2}$$

To evaluate the dynamic energy consumption from equation 6.2, the propagation delay, t_p must be previously estimated. To do that, the current capacitor is integrated when it is charged and discharged. Equation 6.3 is a good approximation to calculate t_p from TCAD data [157];

$$t_p = 0.69 C_L \frac{R_{eqn} + R_{eqp}}{2} \tag{6.3}$$

where R_{eqn} and R_{eqp} are the equivalent resistance of nMOS and pMOS devices respectively. This propagation delay represents the minimum time needed to switch from one state to the other. However in real circuits the logic gates are not switching as faster as possible, since their switching depends on the input signals. This effect is considered by adding an activity factor, whose value in this work is kept constant, to 0.001.

Figure 6.5(a) shows the total power consumption and maximum operating frequency (a) and the energy consumption per cycle (including the static and dynamic contributions) (b) as a function of V_{DD}. The considered parameters for those simulations are T_{SI} = 15 nm and T_{OX} = 15 nm and the V_{BB} is equal to -3/3 V for n/p type. As it can be seen, when V_{DD} is scaled down (from 0.7 V to 0.4 V) the performance is reduced 1.7X (see figure 6.5(a)), however, the energy consumption is improved 3.2X (see figure 6.5(b)). This indicates that

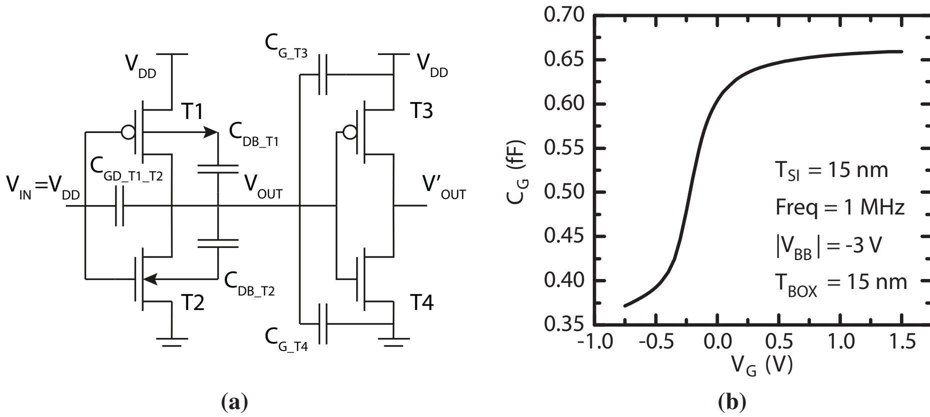


Figure 6.4: Parasitic capacitances impact the transient behavior of the inverter, with fan-out equal to one (a). An example of one gate parasitic capacitance (b).

operating near the threshold voltage reduces significantly the energy consumption [59]. Similar results have been obtained in circuits for other device technologies in [40] or for the same technology [61] validating the methodology used in this thesis.

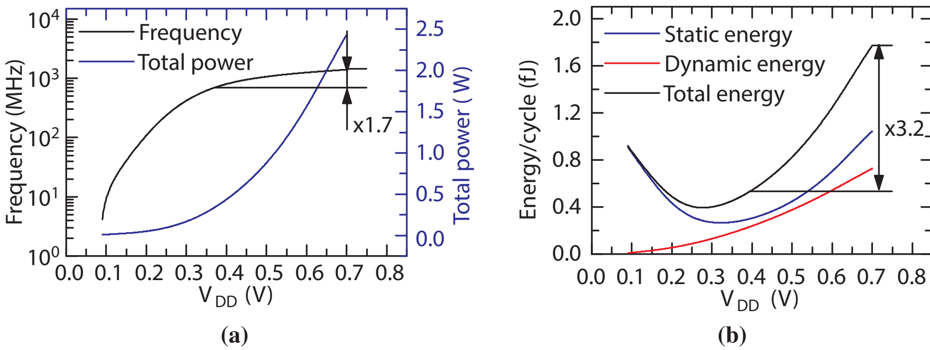


Figure 6.5: Simulated power, frequency and energy per cycle in a CMOS inverter implemented with UTBB FD-SOI MOSFET devices (T_{BOX} = 15 nm, T_{SI} = 15 nm) and the $|V_{BB}|$ = 3 V.

6.3. Parametric study of UTBB FD-SOI MOSFET Inverter

$|V_{BB}|$ and device structural parameters (such as T_{SI} and T_{OX}) can impact on the performance of UTBB FD-SOI MOSFET devices, and consequently, on the inverter. Therefore, a detailed parametric study of ($|V_{BB}|$, T_{SI}, T_{OX}) has been carried out in order to evaluate the dependence of the energy consumption and I_{on}/I_{off} ratio of the inverter with those

magnitudes.

6.3.1. UTBB FD-SOI MOSFET Inverter operation study (V_{BB})

Firstly, the impact on the energy consumption and I_{on}/I_{off} ratio of the $|V_{BB}|$ applied to the devices in the inverter is analyzed. This current ratio is also included in the study, because in digital applications values around 1000 are required for this ratio (International Roadmap for Devices and Systems (IRDS 2016)) in order to distinguish the logic states. The simulations are performed in 2D because device properties are assumed to be completely homogeneous in the Z-axis direction. This assumption reduces the computational time (minutes) compared to 3D simulations (hours). Figure 6.6(a) and 6.6(b) show the energy consumption and the I_{on}/I_{off} ratio as a function of V_{DD}, respectively, for different V_{BB} ranging (from 0 to -4/4 V in n/p type devices). Structure parameters are kept constant with values T_{SI} = 15 nm and T_{OX} = 15 nm. As it can be observed, when the $|V_{BB}|$ is increased (negative values in nMOS and positive values in pMOS) the performance and consumption of the circuit improves. In fact, when $|V_{BB}|$ = 0, V_{DD} for minimum energy is less than zero. These results can be explained through TCAD simulations. Higher $|V_{BB}|$ prevents the creation of the inversion layer under the gate. Therefore, the carrier concentration decreases (not shown), what rises the V_{TH} of devices and consequently reduces the current. Regarding the increase of the I_{on}/I_{off} ratio with $|V_{BB}|$ rises, it can be explained because I_{on} is only slightly reduced but I_{off} is diminished 2 orders of magnitude approximately. Notice that, the V_{DD} that minimizes the energy consumption (yellow points figure 6.6(a)) and maximize the I_{on}/I_{off} ratio (yellow points figure 6.6(b)) are not coincident. Therefore, an operation point that correspond to the best trade-off between the two parameters is represented in figure 6.6(c), and it is calculated as the ratio between the I_{on}/I_{off} ratio and energy consumption. Note that this figure of merit has a maximum for a determined V_{DD} (yellow points Fig. 6c) whose value, V_{OP}, is proposed as an operation point of the inverter.

Figure 6.6(d) shows the minimum energy consumption and the maximum I_{on}/I_{off}, as a function of $|V_{BB}|$. The studied devices show a linear dependence of the minimum energy consumption on $|V_{BB}|$. It is worth highlighting that this linear dependence is not accurate at the extreme values of $|V_{BB}|$ (0 and 4 V) indicating a possible saturation of the tendency. On the other hand, a logarithmic dependence is found for the maximum I_{on}/I_{off} as a function of $|V_{BB}|$. This kind of relationships could be useful in order to optimize the $|V_{BB}|$ voltage because they allow to predict the minimum $|V_{BB}|$ required to reach a target parameter.

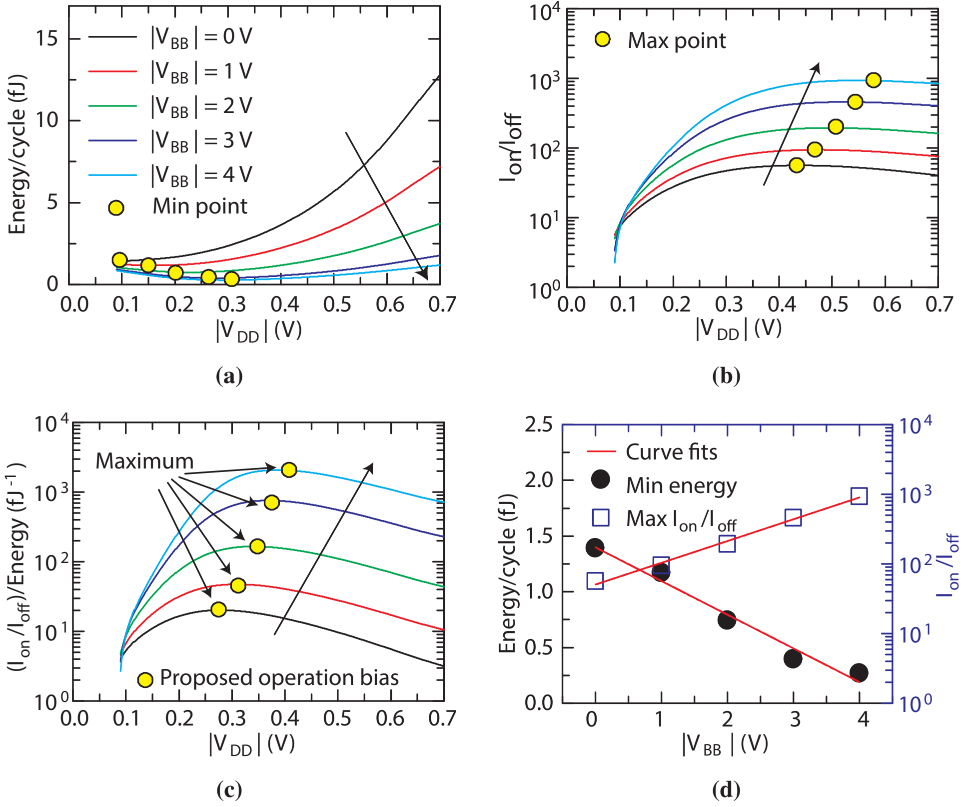


Figure 6.6: Total energy consumption (a), I_{on}/I_{off} ratio (b) and I_{on}/I_{off} and energy consumption ratio as a function of V_{DD} (c), for different $|V_{BB}|$ values. Minimum energy consumption (black solid circles) and maximum I_{on}/I_{off} ratio (blue empty squares) as a function of $|V_{BB}|$ (d). Red lines represent the data fitting. T_{SI} = 15 nm and T_{BOX} = 15 nm. I_{on}/I_{off}.

6.3.2. UTBB FD-SOI MOSFET Inverter structure study (T_{box}, T_{si})

A similar study to that shown in the previous section has been performed, but now, sweeping T_{BOX} between 10 and 25 nm, while the other parameters are kept constant T_{SI} = 15 nm and $|V_{BB}|$ = 3 V. Figure 6.7(a) represents the ratio I_{on}/I_{off} - energy as a function of V_{DD} showing that the V_{OP} increases when the T_{OX} decreases. This dependence can be explained because smaller T_{OX} leads to a higher influence on the carriers of the channel, increasing the device current. Minimum energy consumption and maximum I_{on}/I_{off} ratio as a function of T_{BOX} is represented in figure 6.7(b). Moreover, similar dependence of the minimum energy (linear) or maximum I_{on}/I_{off} (logarithmic) on T_{BOX} is observed as for the case of $|V_{BB}|$ in figure 6.6(d). The results indicate that a thinner T_{BOX} improves the electrical characteristics of the

devices, reducing the energy consumption and rising the I_{on}/I_{off} ratio.

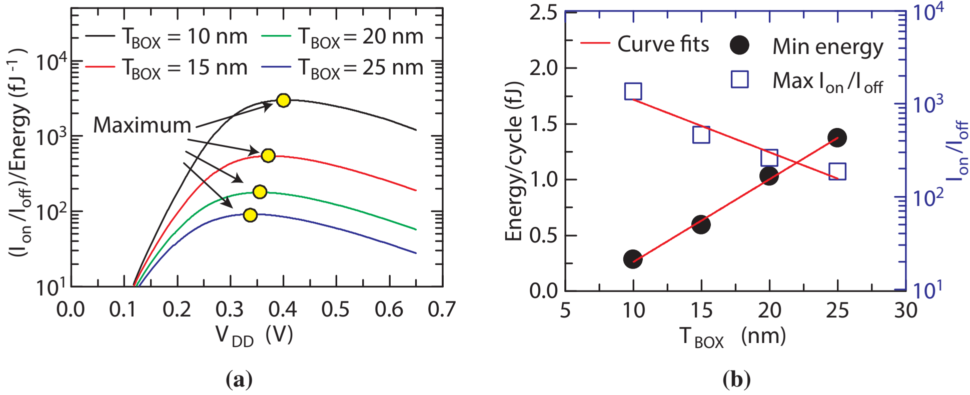


Figure 6.7: I_{on}/I_{off} and energy consumption ratio as a function of V_{DD}, for different T_{BOX} (a). Minimum energy consumption (black solid circles) and maximum I_{on}/I_{off} ratio (blue empty squares) as a function of T_{BOX} (b). Red lines represent the data fitting. T_{SI} = 15 nm and $|V_{BB}|$ = 3 V. Finally,

Finally, the impact of T_{SI} is analyzed in figure 6.8 (T_{BOX} = 15 nm and $|V_{BB}|$ = 3 V). Figure 6.8(a) shows V_{OP} (yellow points) for the different values of T_{SI}, obtaining similar values than those when T_{OX} is swept. Minimum energy consumption and maximum I_{on}/I_{off} ratio as a function of T_{SI} are represented in figure 6.8(b). When T_{SI} is diminished, the energy consumption and I_{on}/I_{off} improve significantly. This improvement in the energy consumption can be explained because the current flowing through the channel is smaller for thinner T_{SI}. On the other hand, the improvement of I_{on}/I_{off} ratio can be explained because the gate exerts more control over the channel. Besides, similar dependence is observed when T_{SI} is changed than when T_{OX} is varied. Nevertheless, in our structure, the energy consumption shows a higher dependence on T_{OX} than on T_{SI}, whereas the opposite is observed for the case of the I_{on}/I_{off} ratio. These relations indicate that a trade-off between both device parameters could be considered in order to optimize circuits for a particular propose.

In order to contextualize our results in the frame of the requirements for future technologies, the energy consumption per cycle and I_{on}/I_{off} ratios obtained for each V_{OP} estimated previously (see Fig. 6c, 7b and 8b) are compared to those given by [23]. To do this, in figure 6.9 the I_{on}/I_{off} ratio as a function of the energy consumption per cycle is represented. In solid black squares, the International Roadmap for Devices and Systems (IRDS) projected electrical specifications of logic core devices for each year are shown. The empty symbols represent our best result obtained for each of our studies ($|V_{BB}|$ = 4V red circle, T_{OX} = 10 nm green triangle and T_{SI} = 10 nm blue diamond), for the corresponding V_{OP}. Our results show lower energy consumption than projections beyond 2027 for all the studied cases,

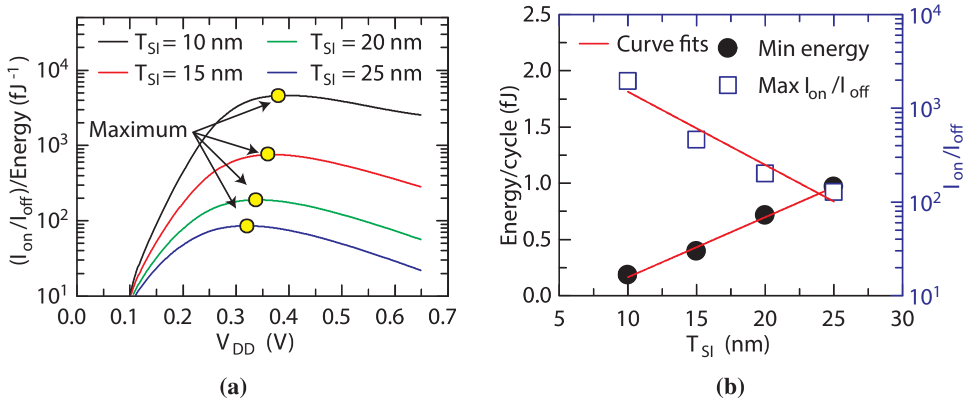


Figure 6.8: I_{on}/I_{off} and energy consumption ratio as a function of V_{DD} for different T_{SI} (a). Minimum energy consumption (black full circles) and maximum I_{on}/I_{off} ratio (blue empty squares) as a function of T_{SI}.Red lines represent the fitting performed (b). T_{BOX} = 15 nm and $|V_{BB}|$ = 3 V. In

pointing out that UTBB FD-SOI MOSFET operating at NTV, with suitable —V_{BB}—, is an attractive candidate for low power applications [61,63]. However, the I_{on}/I_{off} ratio for $|V_{BB}|$ = 4 V and T_{BOX} = 10 nm are 46 % and 22 % smaller than prediction respectively. Only when T_{SI} = 10 nm, the I_{on}/I_{off} ratio is comparable to the projections. This result indicates that T_{SI} parameter can play an important role to optimize this kind of devices.

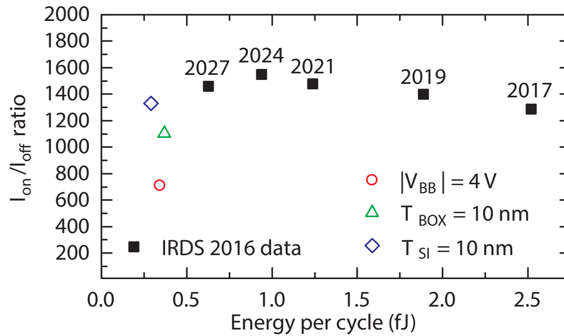


Figure 6.9: Comparison of energy consumption per cycle and $_{on}/I_{off}$ ratio of IRDS 2016 predictions from 2017 to 2027 (black solid squares) and our results (empty symbols).

6.3.3. Impact of oxide trapped charge

Until now, simulated devices have not been considered to be affected by any variability source. In this section, the impact of interface traps charged with 1e$^-$ on the frequency and energy consumption per cycle is analyzed. In particular, as a preliminary analysis, the study

is focused on the comparison of these parameters in the pristine device to these devices where one trap is present in the gate oxide-channel (6.10(a)), in the T_{BOX} oxide-channel interface (see figures 6.10(b)) or when both traps are simultaneously present (not shown). Since the presence of discrete charges in the devices breaks their homogeneity, the simulations are performed in 3D, with W = 100 nm. In the simulations T_{SI} = 15 nm, T_{OX} = 15 nm and the $|V_{BB}|$ = 3 V are considered. The bias applied to gate and drain contact is 0.35 V. As it can be observed in figure 6.10, the trap modifies the device potential, hindering the carriers flow in the channel and consequently decreasing the current through the channel. Therefore, the changes in the electrical behavior of devices due to the interface traps can provoke variations in the performance of logic gates. To show this point, frequency and energy consumption per cycle are analyzed, because large variations of these parameters in logic gates could be critical for design circuit [158].

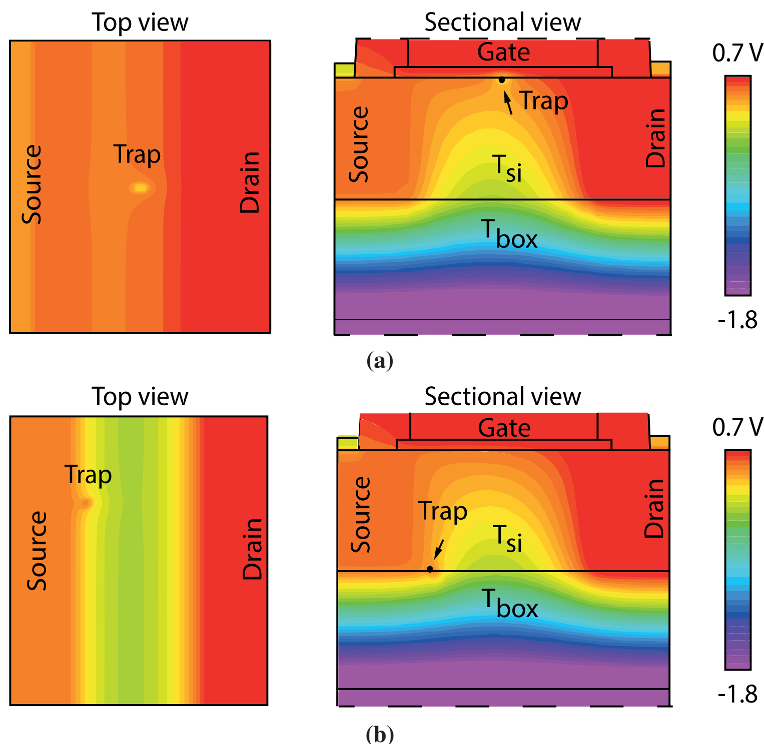


Figure 6.10: Potential maps of top and sectional view of the device (T_{SI} = T_{BOX} = 15 nm and V_{BB} = -3 V) when the trap is located at the gate oxide (a) and at the BOX (b) interface. Gate and drain contacts are biased V_{GS} = V_{DS} = 0.35 V

Figure 6.11(a) shows the frequency variation when charges are present compared to pristine devices. The impact of trap location is studied simulating three different scenarios; trap

located at gate interface, BOX interface or both simultaneously. As it can be seen, the trap located at the gate (red) has more impact than the trap located at the BOX (blue) interface. Besides, the impact of both traps (simultaneously in the device) almost correspond to the sum of each trap separately, pointing out that the simulated traps, in our case, are independent. Also, the frequency variation depends on V_{DD}, being higher than 10 % when V_{DD} is smaller than 0.30 V. Figure 6.11(b) shows the variation of energy consumption per cycle. Note that the variations are negative indicating that introducing traps in the device slightly improves the power consumption, around 4 %. The cause of this improvement could be attributed to the reduction of leakage currents through the channel.

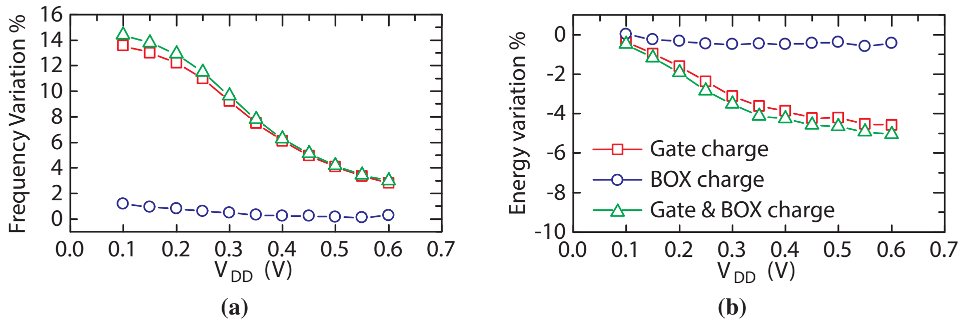


Figure 6.11: Frequency (a) and (b) energy consumption shift when traps are present at gate (red squares), BOX (blue circles) and both simultaneously (green triangles) as a function of power supply V_{DD}.

6.4. Summary and discussion

This chapter is based on paper IEEE J-EDS (Nov-2017) where new strategies are developed in order to reduce the power consumption of devices used for IoT. In particular, UTBB FD-SOI MOSFET devices, which have been demonstrated to be good candidates for low power applications, have been considered to be operated at NTV for digital applications. The electrical characteristics of the devices have been simulated using Silvaco TCAD tool. The TCAD results were used to calculate the energy consumption and operation frequency of an inverter logic gate. The dependence of these parameters on two structural properties of devices (T_{OX} and T_{SI}) and operation conditions (V_{BB}) has been studied. Our results indicate that higher $|V_{BB}|$ and thinner T_{SI} and T_{BOX} improve significantly the energy consumption and I_{on}/I_{off} ratio of the logic gate. However, their impacts are different, and therefore an optimization criterion, which will depend on the application, must be considered. As an example, an operation point (V_{OP}) has been selected which could be useful on digital applications because it provides a good trade-off between the I_{on}/I_{off} ratio and the energy

consumption. These results were compared to IRDS projections pointing out UTBB FD-SOI MOSFET devices with thin T_{SI} and T_{BOX} operating at NTV as a promising technology in low power applications. Finally, the impact of interfacial traps on the frequency and energy consumption of the logic gate was studied obtaining variations in the frequency larger than 10 %. Therefore, the variability related to the presence of charges in the gate and BOX oxide interfaces can be critical for the performance of circuits based on these devices operating in NTV.

Chapter 7.
Summary and conclusions

The high demand of high performance electronic devices, computers, smart-phones, tablets... has led the semiconductor industry to become one of the most important business around the world. The growth of this industry has been based on the scaling of electronic devices, in particular the MOSFET device, which has allowed to reduce exponentially the production price of integrated circuits. However, nowadays, the device scaling is dealing with physical limitations due to the fact that devices have been reached atomic range. Despite considerable efforts to control extrinsic process variations, the discrete nature of matter and charge causes significant fluctuations in the the device characteristics among nominally identical transistors. For this reason, the device variability issue has been intensively studied during the last decade. This thesis is a contribution in the field of variability and electrical properties of MOSFETs and devices based on MOS structures. In particular, how variability sources measured at the nanoscale with CAFM and how the presence of trapped charges in the gate oxide of MOS structures is analyzed from simulation and electrical characterization.

In the chapter 3 of this thesis, experimental technique with nanoscale resolution (CAFM) have been used to characterize the impact of TDs on the electrical properties of a III-V semiconductor (InGaAs) at different temperatures. The main results are;

1. Current through TDs (on-TD sites), observed as surface pits in topographical maps, is found to be higher than through areas without defects (off-TD sites).
2. Different conduction mechanisms are associated to on-TD sites and off-TD sites. In particular, the current through on-TD sites is described by Poole Frenkel mechanism and the current through off-TD sites is explained by thermionic emission mechanism.
3. CAFM technique is well-suited for evaluating the TDs electrical properties with the nanoscale resolution, required to identify material structural features affecting device performance.

In chapter 4, the impact of topography and charge density of polycrystalline HfO_2 used as gate oxide on MOSFET variability has been studied, obtaining the next conclusions:

1. A simulator tool (NAMAS) has been developed to generate topography and density charge maps since inputs obtained from CAFM measurements (topography and current maps) of a given sample. In particular, in this thesis polycrystalline HfO_2 was analyzed.

2. The procedure to generate topography maps has been validated comparing the generated maps to experimental maps by cumulative probability graphs. The procedure to generate charge density maps has been also validate through the comparison of the obtained values with those measured with KPFM.

3. The local thickness (experimentally obtained) and calculated charge density were the inputs to a device simulator, which allowed evaluating the corresponding I_D-V_G curves of MOSFETs, demonstrating a clear device-to-device variability, as a result of the presence of GBs after crystallization.

4. V_{TH} variability due to the impact of topography and density charge has been analyzed separately indicating that this variability sources are not independent, and therefore they must be study using bivarite normal distribution.

5. Though polycrystalline high-k dielectrics have been considered as case study, the proposed methodology can be extended to any dielectric whose electrical properties depend on thickness and defect density.

In the chapter 5, the impact of traps in the gate oxide on the variability of MOSFET has been also studied using TCAD tools. Besides, a methodology to characterize the physic parameters of traps has been developed. The main results are:

1. Experimental and simulated I_D-V_G curves for several geometries of ultra-scaled devices are used to demonstrate that the V_{TH} time-zero variability (due to trapped charges) has a deviation of the Pelgrom's scaling law.

2. Simulation data have indicated that the origin of such deviation could be related to the different impact on V_{TH} of traps depending on their location along W and L of device.

3. An empirical equation has been proposed to improve the fitting of Pelgrom's law to ulta-scale devices, in which two parameters are introduced to separately account for the W and L dependence.

4. A methodology to evaluate the physical parameters that describe the interface trap behavior in TCAD simulators (E_{trap}, σ_{trap} and Q_{trap}) from experimental τ_e, τ_c and ΔV_{TH}(IT) data has been proposed.
5. From static simulations Q_{trap} has been obtained. Transient simulations of occupancy probability of the traps has been performed and compared to PDO analytical model in order to obtain the E_{trap}, σ_{trap} of the traps.
6. Once physical parameters of the traps are available, any TCAD simulation changing the bias or temperature conditions can be easily performed. Using this proposed methodology RTN and/or BTI related variability through TCAD simulations can also be performed, in reasonable computing times.

Finally, in chapter 6, since UTBB FD-SOI MOSFET devices, which have demonstrated to be good candidates for low power applications, the static and dynamic energy consumption of an inverter logic gate based on this kind of devices and operated at near-threshold voltage for digital applications has been studied from TCAD. In particular, the performance and power consumption trade-off and the impact of interface traps on these parameters of this logic gate have been studied. As the main results are highlighted:

1. The dependence of two structural parameters of devices (T_{OX} and T_{SI}) and operation conditions (V_{BB}) has been studied. The results indicate that higher $|V_{BB}|$ and thinner T_{SI} and T_{BOX} improve significantly the energy consumption and I_{on}/I_{off} ratio of the logic gate.
2. An operation point (V_{OP}) has been selected which could be useful on digital applications because it provides a good trade-off between the I_{on}/I_{off} ratio and the energy consumption.
3. The impact of interface traps on the frequency and energy consumption of the logic gate was studied obtaining variations in the frequency larger than 10 %. Therefore, the variability related to the presence of charges in the gate and BOX oxide interfaces can be critical for the performance of circuits based on these devices operating in NTV.

Overall, the work developed in this thesis has shown new methodologies to translate nanoscale information obtained by CAFM and KPFM, to TCAD simulator, in order to estimate its impact on device variability. On the other hand, TCAD simulations have been performed to explore new methodologies in MOSFET and UTBB FD-SOI MOSFET devices, which allow estimate the impact of interface traps on variability device.The most of the results included in this manuscript have been disserted in specialized journals and international conferences.

Acronyms

Acronym	Description	Page
AFM	Atomic Force Microscopy	25
BJT	Bipolar Junction Transistor	1
BTI	Bias Temperature Instability	20
CAFM	Conductive Atomic Force Microscopy	12
CMOS	Complementary Metal-Oxide-Semiconductor	8
CPD	contact potential difference	27
DFC	Discrete Fixed Charge	60
EOT	Equivalent Oxide Thickness	13
FE	Field Emission	4
FinFET	Fin Field Effect Transistor	16
GBs	Grain Boundaries	46
Gs	Grains	46
HCI	Hot Carrier Injection	20
ICs	Integrate Circuits	8
IoT	Internet of Things	17
IRDS	International Roadmap for Devices and Systems	82
IT	Interface trap	63
KPFM	Kelvin Probe Force Microscopy	25
LER	Line-Edge Roughness	18
LWR	Line-Width Roughness	18
MGG	Metal Gate Granularity	18
MIM	Metal-Insulator-Metal	6
MIS	Metal-Insulator-Semiconductor	6
MOSFET	Metal Oxide Semiconductor Field Effect Transistor	1
N_a	Doping concentration	18
NAMAS	Nanoscale Map Simulator	34

Acronym	Description	Page
NTV	Near-Threshold Voltage	17
NW	Nanowire	16
PDO	Probabilistic Defect Occupancy	21
PF	Poole-Frenkel emission	6
PGG	Poly-silicon Gate Granularity	18
QD	Quantum Dot	16
RDF	Random Dopant Fluctuation	17
REDEC	Reliability of Electron Device and Circuits	29
RTN	Random Telegraph Noise	20
SCE	Short-channel Effect	12
SiO_2	Silicon oxide	8
SOI	Silicon-on-Insulator	17
SOS	Silicon-on-Sapphire	17
SPICE	Simulation Program with Integrated Circuits Emphasis	29
TCAD	Technology Computer Aided Design	16
TDDB	Time-Dependent Dielectric Breakdown	20
TDs	Threading Dislocations	12
TE	Thermionic Emission	3
TEM	Transmission Electron Microscopy	36
UHV	Ultra High Vacuum	46
UTBB FD-SOI	Ultra-thin Body and Buried Oxide Fully Depleted Silicon on Insulator	16
VLSI	Very Large Scale Integration	18

List of Symbols

Symbol	Description	Unit
A_0	Richardson constant.	A/cm^{2}K^2
χ	Electron affinity.	eV
D_{it}	Interface Charge Density.	Q m$^-$2
E_{fm}	Fermi level of a metal.	eV
E_{fs}	Fermi level of a semiconductor.	eV
ε_s	Relative optical dielectric constant.	F/m
h	Planck constant.	J·S
J_{PF}	Poole-Frenkel density current.	A/m^2
J_{TE}	Thermionic emission density current.	A/m^2
κ	Dielectric constant.	–
k_B	Boltzmann constant.	JK^{-1}
L	Device length.	m
L_G	Gate length.	m
m_e^*	Effective electron mass.	Kg
m_e	Electron rest mass.	Kg
μ	the field independent carrier mobility.	m^2/(V·s)
ϕ_{B0}	Potential barrier height.	V
ϕ_m	Metal work function.	V
ϕ_s	Semiconductor work function.	V
Φ_t	Trap energy level.	V
$P_{occ}(t)$	Occupancy probability.	-
ψ_{bi}	Contact potential or built-in potential.	V
q	Elementary charge.	C
Q_{trap}	Trapped charge.	C
ρ_{ox}	Local charge density.	cm$^-$3
S_{DOP}	Substrate doping.	cm$^-$3
E_{trap}	Trap energy.	m^2

Symbol	Description	Unit
σ_{trap}	Trap effective cross section.	m^2
T	Temperature.	K
T_{BOX}	Buried oxide thickness.	m
τ_c	Trap capture time.	s
τ_e	Trap emission time.	s
T_{OX}	Oxide thickness.	m
T_{SI}	Channel thickness.	m
T_{SUB}	Gate oxide thickness.	m
T_{vac}	Thickness of vacuum layer between AFM tip and sample.	m
V_{TH}	Threshold voltage.	V
I_{on}	On-current.	V
I_{off}	Off-current.	V
V_{DD}	Circuit supply voltage.	V
V_{CPD}	Contact different potential.	V
V_{BB}	Back Biasing Voltage.	V
V_{OUT}	Circuit output voltage.	V
V_a	Applied voltage.	V
W	Device width.	m

Appendix I

Paper: JVST-B (Jun-2015)

JVSTB
Journal of Vacuum Science & Technology B

Conductive-AFM topography and current maps simulator for the study of polycrystalline high-k dielectrics

Carlos Couso, Marc Porti, Javier Martin-Martinez, Vanessa Iglesias, Montserrat Nafria, and Xavier Aymerich

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Conductive-AFM topography and current maps simulator for the study of polycrystalline high-k dielectrics

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In this work, a simulator of conductive atomic force microscopy (C-AFM) was developed to reproduce topography and current maps. In order to test the results, the authors used the simulator to investigate the influence of the C-AFM tip on topography measurements of polycrystalline high-k dielectrics, and compared the results with experimental data. The results show that this tool can produce topography images with the same morphological characteristics as the experimental samples under study. Additionally, the current at each location of the dielectric stack was calculated. The quantum mechanical transmission coefficient and tunneling current were obtained from the band diagram by applying the Airy wavefunction approach. Good agreement between experimental and simulation results indicates that the tool can be very useful for evaluating how the experimental parameters influence C-AFM measurements. © *2015 American Vacuum Society*.
[http://dx.doi.org/10.1116/1.4915328]

I. INTRODUCTION

High-k materials are applied as gate dielectrics for current and emerging technologies. However, several issues impede the complete optimization of these materials. One of the most relevant concerns is polycrystallization of the high-k material after thermal annealing, which increases the leakage current and its variability in ultrascaled devices.[1–3] High-k polycrystallization takes place at the nanometer scale, and therefore, a complete characterization of this phenomenon is required. In this context, conductive atomic force microscopy (C-AFM) has been demonstrated to be a very powerful technique to evaluate the topographic and electrical properties of high-k dielectrics at the nanoscale.[4,5] In particular, this technique was successfully used in several studies to evaluate the impact of polycrystallization.[5–7] One of the most relevant conclusions of these works was that, in polycrystalline HfO_2 layers, the gate leakage current mainly flows through grain boundaries (GBs). This is because of the reduced oxide thickness at these sites and the variation in electrical properties at the GBs, which are related to an excess of oxygen vacancies.[5] However, several intrinsic factors of the C-AFM technique, such as the tip conductivity and shape, and its progressive wear unavoidably affect the measurements, leading in some cases to erroneous results. Evaluating how these factors influence measurements can be complicated or nearly impossible in many cases if only C-AFM is used. To deal with this problem, a C-AFM simulator has been developed. Our simulation tool takes into account the morphology and electrical properties of a high-k dielectric in contact with a sharp conductive tip, reproducing the conditions of a C-AFM characterization. Using this approach, problematic factors, such as the tip geometry or others can be analyzed and their impact on the C-AFM measurements studied in detail.

In order to test the simulator, its output was compared to C-AFM experimental data obtained for a polycrystalline high-k dielectric.[5] Particularly, topographical maps were measured with a C-AFM working in contact mode. Metallic-coated silicon tips were used for these measurements. The stack under analysis has the following structure: HfO_2 film with a nominal thickness of 5 nm, deposited by atomic layer deposition on a native 1-nm thick SiO_2 layer. The dielectric stack was grown on a p-type Si epitaxial substrate.

II. MODELING

To develop the simulator, two different modules have been considered. The topography module, which reproduces the high-k morphology when measured with C-AFM, and the current module, which calculates the tunneling current through the high-k stack at each point from the map obtained with the topography module.

A. Topography module

To perform a topography simulation, some input parameters related to the sample morphological properties must be provided. In our case, these parameters were extracted from C-AFM morphology measurements. In particular, for a polycrystalline structure, statistical geometrical parameters related to the grain size and the GB width and depth (with respect to grains) are necessary. These parameters can be easily estimated from the statistical analysis of an experimental map [such as that in Fig. 3(a)] by means of the open processing software.[8] Table I shows, as an example, some parameters related to the sample morphology that can be obtained and that are of interest for our simulations. In the "experimental" column in Table I, the mean and standard deviation (SD) are shown for different geometrical and topographical parameters obtained from the experimental image.

These experimental parameters were used as input parameters for the simulator. The polycrystalline topography surface was generated by using Monte Carlo simulation through

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TABLE I. Statistical parameters obtained from a polycrystalline HfO_2 layer (experimental columns) and the same parameters obtained from the simulated topographic maps (simulated columns).

Parameter	Experimental		Simulated	
	Mean	SD	Mean	SD
Radius grains (nm)	33.2	8.2	38.5	11.3
Height grains (nm)	2.46	0.19	2.18	0.23
Width GB (nm)	3.3	1.4	2.1	1.2
Height GB (nm)	1.13	0.26	0.98	0.31

the acceptance–rejection method.[9] Each grain was approximated to one polygon with n sides, randomly obtained between a minimum and a maximum (in this work, 8 and 15 were used, respectively), whose center also was randomly selected at a given position on the surface (P in Fig. 1). The distance of each side to the center P [R1 and R2 in Fig. 1(a)] and the angle between R1 and R2 were statistically estimated based on the experimental data obtained from topographical images [Fig. 1(a)]. Then, the morphology of the GB surrounding the grain [Fig. 1(b)] also was estimated, using the experimental data shown in Table I. This process was repeated until the surface simulation was full [Fig. 1(c)]. Finally, the height of each grain and GB was calculated from the height probability inputs obtained from C-AFM experimental images.

As previously was explained, when surfaces are measured with C-AFM, the resulting topography is affected by the tip geometry. To investigate this point, a convolution algorithm[10] was applied to the simulated surfaces, with the assumption that the tip has a semispherical shape. To validate this simulation technique, the resulting topography maps were compared with experimental C-AFM images. Detailed results are provided in Sec. III. Section II B is focused in the current module.

B. Current module

Once the simulated topographic map was obtained, a model was developed to simulate the current through the C-AFM tip. The following parameters were used as inputs: the oxide thickness at each point on the map, dielectric constant, barrier height, effective mass, the work function of the tip and the applied voltage. With these inputs, the structure band diagram can be calculated using open-source software.[11,12] To determine the oxide thickness at each point, the simulator accounted for the statistical surface parameters of the top and bottom interfaces of the different layers of the stack. However, in this work, the SiO_2–HfO_2 interface was not experimentally measured because the SiO_2–HfO_2 interface roughness tends to be much lower than the HfO_2 superficial roughness. The native SiO_2 roughness also was neglected. Thus, only the roughness of the top HfO_2 surface is considered for our purposes.

To calculate the current, the size and shape of the tip also were considered, because not all the points of the tip apex are in contact with the sample [Fig. 2(a)]. Consequently, for each point of the surface, the current were evaluated by considering the current through that site and also through the surrounding region. Figure 2 shows an example of this approach. When the current is evaluated for a particular site

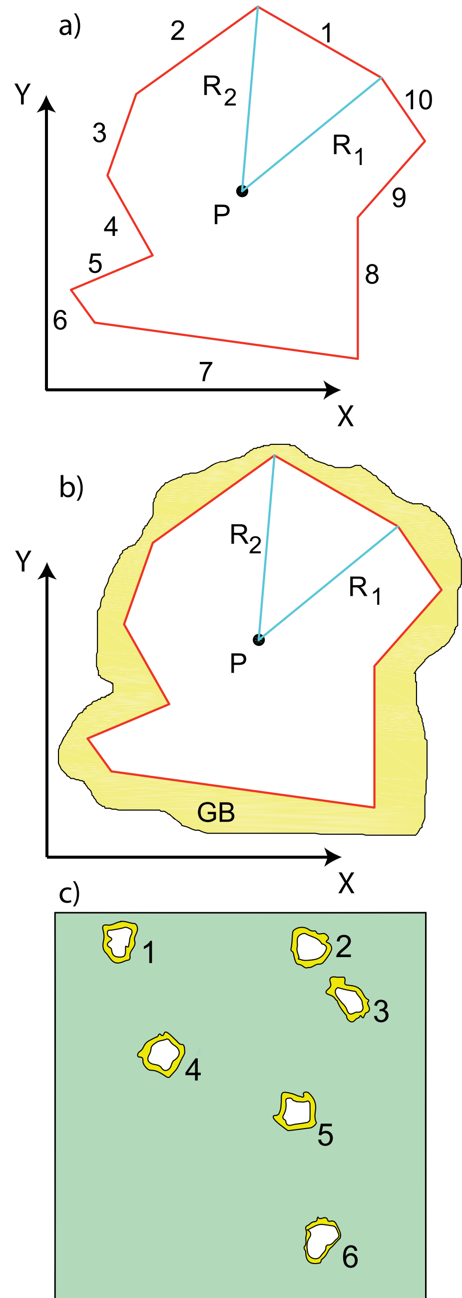

FIG. 1. (Color online) (a) Sketch of the process for creating one grain. (b) The surrounding GB. (c) Several grains and GBs were created on the simulation surface.

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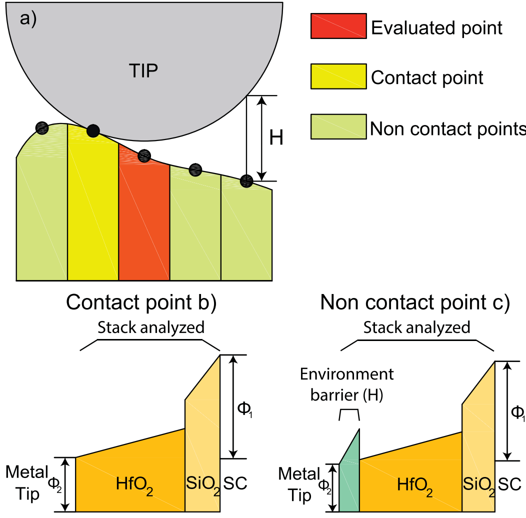

FIG. 2. (Color online) (a) 2D sketch of a tip on a surface. Several contact conditions between tip and sample can result. (b) Band diagram for a contact point. (c) Band diagram with extra barrier due to the environment effect at the "noncontact points".

of a surface [evaluated point in Fig. 2(a)], depending on the local topography, it is possible that the tip was not in contact with the "evaluated point." This is because the tip could contact to a higher site: "contact point." At the contact points, the band diagram in Fig. 2(b) was considered. In the sites without contact (noncontact points), the band diagram was added to a gap with a barrier height that depended on the considered environment (vacuum, N_2, atmosphere, etc.) and a thickness (H) equal to the distance between the tip and that site [Fig. 2(c)]. Thus, all the sites below the C-AFM tip were considered when calculating the total current. Therefore, the tip geometry, sample topography and environment were taken into account for the current calculation.

From the band diagram at each site, the quantum mechanical transmission coefficient (QMTC) can be calculated by applying the Airy wavefunction approach.[13] In order to solve any barrier shape, the algorithm has been implemented by means of a transfer-matrix procedure.[14,15] Finally, the current density at each point was calculated using the following expression:[16]

$$J_z = \frac{e\sum_l n_{vl} m_{dl}}{2\pi^2\hbar^3}\int_0^\infty T(E_z)kT\ln \times \left\{\frac{(1+\exp[(E_F-E_Z)/kT])^\lambda}{1+\exp\left[(E_F-E_Z-(eV_{\rm ox}-\Delta))/kT\right]}\right\}dE_z,$$

where e is the electron charge, l is the valley number, n_v is the valley degeneracy, m_d is the density-of-states mass per valley, $\hbar$ is the reduced Planck constant, $T_e(E_z)$ is the electron transmittance, E_z is the electron energy perpendicular to the sample surface, k is the Boltzmann constant, T is the temperature, E_F is the Fermi level, and $V_{\rm ox}$ is the oxide voltage.

The term λ is expressed as $\lambda = m_{ta,e}/m_{tb,e}$, which is the ratio between the transverse effective mass in the tip, $m_{ta,e}$, and that in the conduction band edge of the silicon substrate, $m_{tb,e}$, where $m_{ta,e} = \Sigma|n_v|m_{dl}$.

III. RESULTS AND DISCUSSION

A. Topography results

Figure 3(a) shows an experimental topography map of a HfO_2 polycrystalline layer with a nominal thickness of 5 nm measured using the C-AFM technique. From this experimental map, the necessary parameters were calculated and introduced as inputs in the simulator (Table I experimental columns). Figure 3(b) shows a simulated topographic map

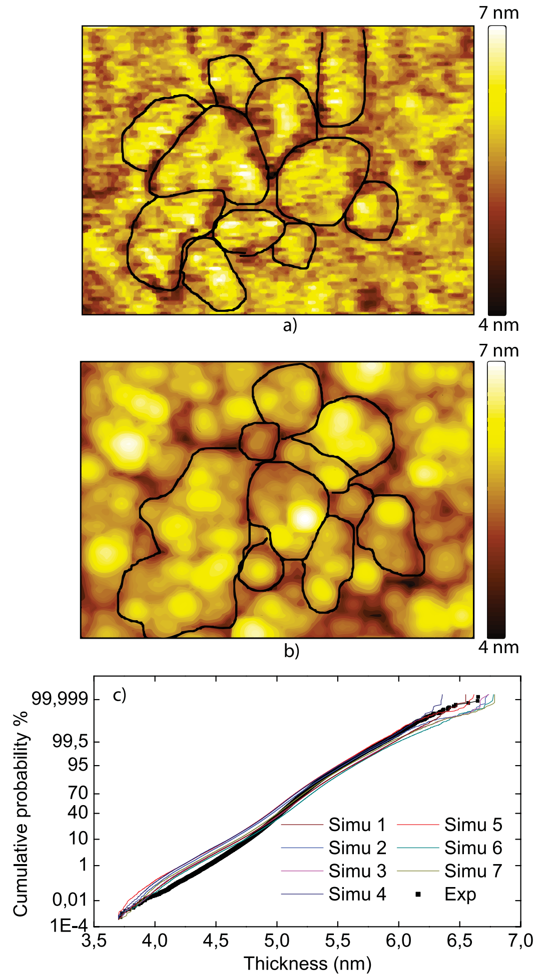

FIG. 3. (Color online) Experimental (a) and simulated (b) topography images of $HfO_2/SiO_2/Si$ structure (area of 400 × 300 nm^2). (c) Thickness cumulative probability obtained from the experimental (dots) and several simulated (lines) topography maps. Various simulation random seeds are used for the simulations.

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obtained from the extracted parameters of the experimental image [Fig. 3(a)]. Note that both images show grains with similar sizes and random shapes (see highlighted grains in both maps). However, it is important to emphasize that the algorithms used to generate the polygons (i.e., the grains in the simulated image) and to take into account the convolution with the C-AFM tip are not directly related to any experimental parameter. Therefore, they should be quantitatively validated. To do so, the experimental statistical parameters shown in Table I have been compared to those obtained from the simulated map (Table I simulated columns). Note that, when the standard deviations are considered, fairly good agreement was observed. Moreover, the thickness cumulative distributions of the experimental maps [Fig. 3(a)] and several of the simulated maps are plotted in Fig. 3(c). The black line represents the data corresponding to the experimental map and the color lines correspond to the simulated maps. The different simulated maps were obtained by inputting the same statistical parameters [obtained from Fig. 3(a)] but changing the simulation random seed. Note that all the simulated thickness cumulative distributions are very similar to the experimental one. The small differences can be related to the fact that different seeds and, therefore, different random areas are simulated which, although being similar from a statistical point of view, are not identical (as expected). The good match between the experimental and simulated statistical parameters (shown in Table I) and the distributions obtained from experimental and simulated maps indicates that the proposed simulation methodology accurately reproduces the topography of polycrystalline structures.

Once the simulator has been checked, the influence of experimental factors such as the tip radius, environment or tip shape can be evaluated separately. As an example, in this manuscript, the impact of the AFM tip radius on the topography measurements was investigated. Figure 4 shows the roughness (RMS) obtained from experimental (black triangles) and simulated (empty color squares) topographical maps. To obtain the experimental data, several topography maps of the same sample were measured using tips with different radii. The simulated data were obtained by inputting the parameters extracted from the experimental image shown in Fig. 3(a) and varying the radius parameter. Both the experimental and simulated images show that the tip radius affects the observed roughness. Specifically, when the tip radius is increased, the roughness of the surface decreases, as expected. However, the roughness is a parameter strongly dependent on the mean depth of the GB. Therefore, simulations were performed with varying mean depths ($\mu_{GBdepth}$), as shown in the plot. The best match between the simulations and experimental data was obtained at a mean GB depth of 1.3 nm. This example shows that this type of simulations can be used to evaluate how the C-AFM tip affects topography measurements and get a more accurate picture of the surface under study.

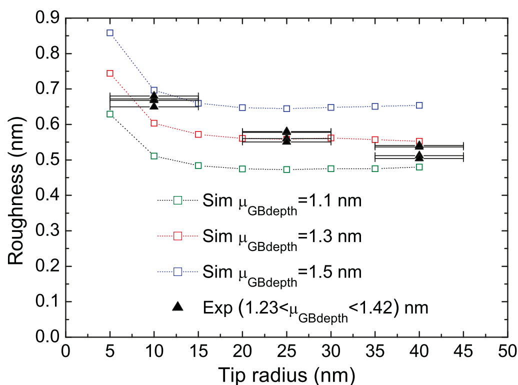

FIG. 4. (Color online) Roughness as a function of tip radius. Simulations were performed for various GB depths.

B. Current results

After the topography of the polycrystalline HfO_2 layer was simulated, the current through the stack under study was determined following the procedure described in Sec. II B. A

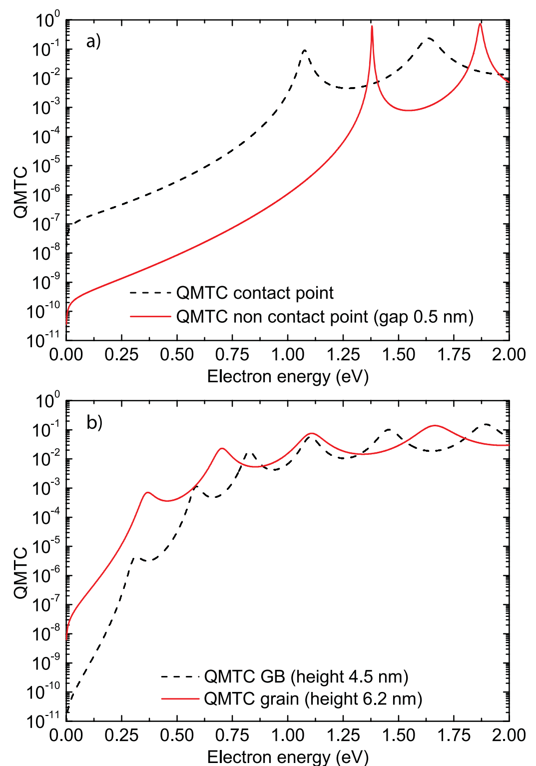

FIG. 5. (Color online) QMTC as function of electron energy with bias equal to 1 V. (a) Difference between a contact point and a noncontact point (environment gap of 0.5 nm). (b) Difference between a grain (6.2-nm height) and at a grain boundary (4.5-nm height).

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5-nm HfO_2/1 nm SiO_2/Si p-type stack was simulated, i.e., the same structure that was experimentally measured. Figure 5(a) shows the QMTC as a function of the electron energy at a contact point (dash) and a noncontact point (line) with an extra barrier of 0.5 nm associated with an air environment. The QMTC decreases quickly if there is a gap related to the environment, as expected. Therefore, from Fig. 5(a), it is evident that tunneling transport occurs preferentially through the contact point. These results emphasize that a good contact between the sample and tip must be ensured to avoid appearance of an extra barrier that could modify the current obtained through the stack. Figure 5(b) represents the QMTC at two sites of differing physical natures (a 6.2-nm thick grain and a 4.5-nm thick GB). Note that the transmittance is higher for a GB and, consequently, larger current should be expected there. These results are confirmed in the simulated and experimental current maps in Figs. 6(a) and 6(b).

Figures 6(a) and 6(b) show an experimental (a) and simulated (b) current map, which correspond to the structures whose topography maps are shown in Figs. 3(a) and 3(b), respectively. Note that, in both cases, the current flows preferentially through the GBs and higher currents are obtained at the GBs (thinner regions). To analyze the relation between the current level and the depth of the GBs, the current as a function of HfO_2 thickness, obtained from different experimental maps and simulated surfaces, is plotted in Figs. 6(c) and 6(d), respectively. Areas larger than those shown in Figs. 3 and 6 have been considered, so that the analysis is statistically meaningful. Note that in Fig. 6(d) (corresponding to simulated data) a clear relation between current and gate stack thickness is observed, as expected. However, there is not a univocal correspondence between current and thickness. This is because the current does not depend on the layer thickness at a given site, but also on the contact characteristics. Therefore, other surrounding points could also contribute to the global current measured by the C-AFM tip at a given site.

In Fig. 6(c), corresponding to the experimental data, two clear regions can be distinguished. Above a thickness of approx. 6 nm, a constant current around 1 pA is registered, which corresponds basically to the noise level of the C-AFM. Below 6 nm, the relation between the current and the oxide thickness is not as clear as in the simulated image.[5] Moreover, Fig. 6(c) also shows that experimental currents can be higher than the simulated currents. These differences could be explained because up to now, only differences in depth and geometry surface have been considered and the simulation has not taken into account the HfO_2–SiO_2 and SiO_2-substrate roughnesses. Other effects,

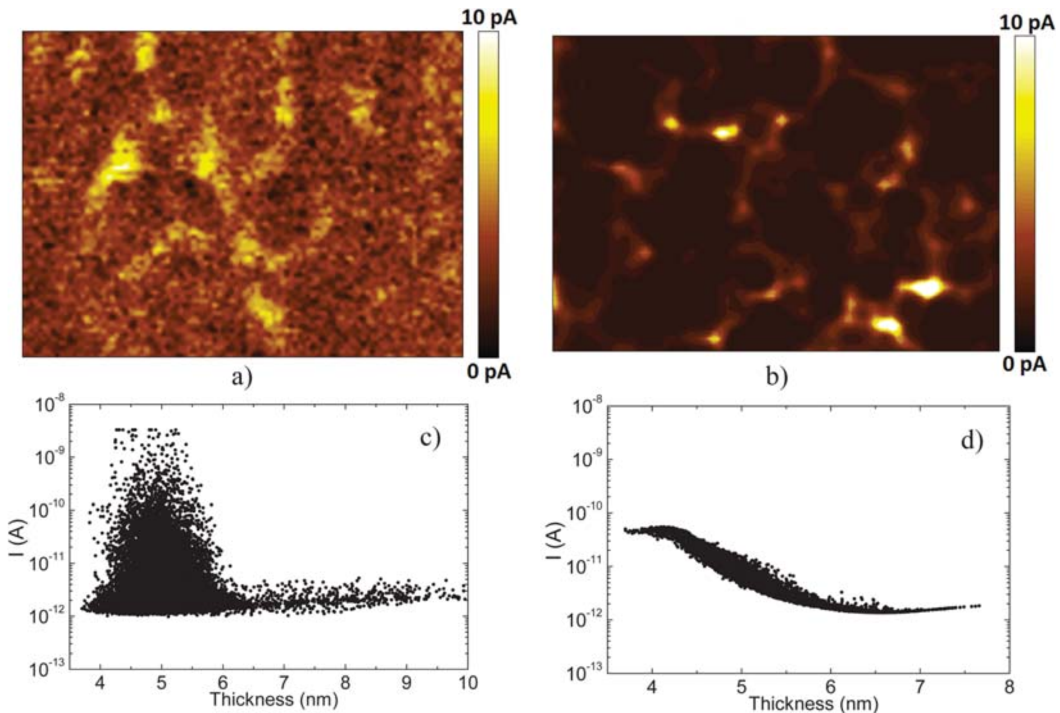

FIG. 6. (Color online) (a) Experimental current image corresponding to the topography map in Fig. 3(a) (area of 300 × 400 nm^2). The applied bias was 6 V. (b) Simulated current image corresponding to the topography map in Fig. 3(b) (area of 300 × 400 nm^2). The applied bias was 2 V. (c) Experimental current as a function of thickness and (d) simulated current as a function of thickness.

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such as the presence of traps in the high-k dielectric (not included yet in the simulator) that could favor trap assisted tunneling through GBs, or different electrical properties between grain and GBs,[17] also could explain the observed differences between the experimental data and the simulations. In fact, in one study, C-AFM experimental data and a simulation model that considered different dielectric constants for grains and GBs were used to demonstrate that the faster degradation observed at GBs in HfO_2/SiO_x stacks could be attributed to an enhanced electric field across the SiO_x layer beneath the thinner HfO_2 film at these sites.[17]

IV. SUMMARY AND CONCLUSIONS

In this work, we presented a simulation methodology that allows reproduction of topography AFM images based on several experimental aspects, such as tip radius or tip material. Good agreement was found between the simulations and experimental results. In addition, current through the dielectric stack was calculated from the band diagram at each point on the surface. The current calculation took the morphology and electrical properties of the high-k material and C-AFM tip into consideration. This simulation method can be very useful for evaluating the unavoidable experimental effects intrinsic to the C-AFM technique.

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Efficient methodology to extract interface traps parameters for TCAD simulations

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A B S T R A C T

In this work, a methodology to estimate ATLAS TCAD simulation parameters from experimental data is presented, with the aim of analyzing the impact of interface traps in the MOSFET threshold voltage variability of a particular technology. The method allows to calculate the parameters that define the trap behavior in TCAD simulations (trapped charge, trap energy level and capture cross section) from the parameters that can be experimentally measured (capture and emission times and single-trap threshold voltage shift). The availability of these simulation parameters will allow to study RTN and/or BTI-related variability through TCAD simulations, in reasonable computing times.

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1. Introduction

To improve the performance of integrated circuits, the size of devices has been progressively reduced and, currently, the nanometer range has been reached. As a consequence, the discreteness of charge is reflected in the electrical performance of devices, leading to device variability [1–3]. For instance, charge trapping/detrapping in/from interface states can be observed in the form of Random Telegraph Noise (RTN) and/or Bias Temperature Instabilities (BTI), which introduce random and/or permanent shifts in the threshold voltage [4,5]. Therefore, understanding the physics behind this variability and how it impacts the device behavior is essential to introduce suitable countermeasures into the fabrication processes, device architecture and/or circuit design.

TCAD simulations can be a fast and adequate approach to evaluate, from experimental data, the statistical impact of interface traps (ITs) on the threshold voltage shift (ΔV_{th}) of MOSFETs of a particular technology [6]. It must be taken into account, however, that the parameters that describe the IT behavior in these simulators, i.e. energy level (E_{trap}), cross section (σ_{trap}) and trapped charge (Q_{trap}) differ from those that can be experimentally obtained, such as capture (τ_c) and emission (τ_e) times and single-trap induced threshold voltage shift ($\Delta V_{th}(IT)$), so that the simulation-experiment link is not straightforward. In this work, a procedure to translate the empiric trap parameters (τ_c, τ_e and $\Delta V_{th}(IT)$) into the main TCAD physical parameters (E_{trap}, σ_{trap} and Q_{trap}) is proposed.

It will be shown that Q_{trap} can be estimated from static simulation data, whereas the relation between (E_{trap}, σ_{trap}) and (τ_c, τ_e) can be evaluated from transient data, considering a suitable compact model. The proposed methodology will allow RTN and BTI variability studies using TCAD simulations.

2. Device structure and simulation methodology

2.1. Device structure

A bulk nMOSFET structure was defined in ATLAS TCAD tool (from Silvaco) and calibrated using experimental I_D-V_G curves measured in transistors (W/L = 300 nm/300 nm). Fig. 1 shows the adopted flow diagram for device calibration procedure. First, since simulation time in 2D is shorter than in 3D, 2D devices were simulated using the nominal device parameters and a Gaussian doping profile. The error between the simulated and one representative measured I_D-V_G curve was minimized by varying doping and other technological parameters (as the EOT or underlapping length).

When the 2D calibration was finished, that is, when the error was less than a given value set by the user (1% in this work), the final 2D fitting parameters were used as initial parameters in 3D simulations, where the same algorithm was repeated. This procedure reduces the computation time (hours) because most of the simulations were performed in 2D. Fig. 2a shows the net doping profile and some dimensions of the device obtained after the calibration. Fig. 2b shows the final simulated (red line) and measured (black squares) I_D-V_G curves in linear and logarithmic scale; the good agreement validates the calibration procedure.

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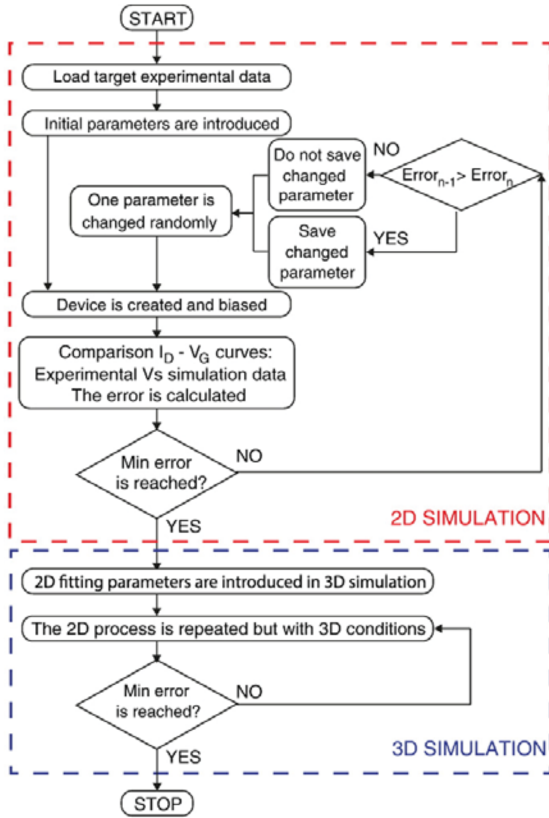
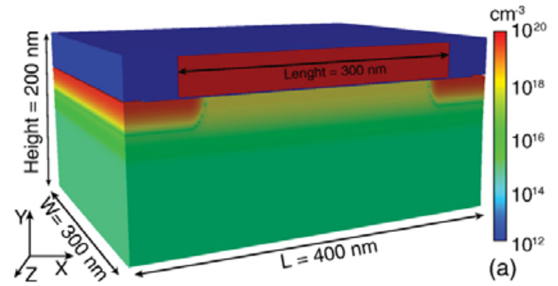


Fig. 1. Flow diagram of the TCAD device calibration procedure.

2.2. Simulation methodology

The I_D-V_G characteristics in Fig. 2b were considered as reference and the effect of additional discrete traps located at the semiconductor/oxide interface on the device threshold voltage (V_{th}) was analyzed. To improve the simulation accuracy, around the IT location the mesh was refined (steps of 1 nm). Multiple traps (N_{trap}) were expected in the device interface, which were characterized by their E_{trap}, σ_{trap} and Q_{trap}, and whose spatial distribution and number change from device to device. Traps in the oxide bulk were not taken into account in this work because their effect could be estimated using the presented approach by simply considering interface traps with different trapped charge. Moreover, other sources of variability as Random Dopant Fluctuations (RDF) or Line Edge Roughness (LER), whose effects could be combined with those of ITs [3], although not negligible in real devices, in this work have not been considered, in order to analyze exclusively the shifts in the threshold voltage, ΔV_{th}, related to ITs. However, although not considered, it should be emphasized that: first, RDF and/or LER would only affect the parameter Q_{trap} of our methodology (not those parameters related to the dynamic simulations) and, second, the RDF effect on V_{th} variability could be included in the proposed methodology since RDF, as fixed traps, could be somehow equivalent to the ITs introduced in the oxide, affecting the Q_{trap} parameter. Regarding LER, further characterization and analysis should be considered to include this variability source in the simulation procedure.

To understand the impact of each analyzed parameter (E_{trap}, σ_{trap} and Q_{trap}), simulations where two parameters were kept constant while one was changed were performed.



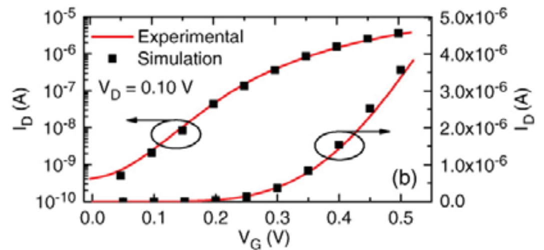


Fig. 2. MOSFET structure showing the channel doping (a). Experimental (black squares) and simulated (red lines) I_D-V_G curves of the device (b). The nominal Vth of the device was 0.37 V and the estimated EOT was 1.5 nm.

3. Static simulations

In this section, 3D-static simulations were performed to evaluate the effect of the traps spatial distribution and the value of Q_{trap} on the device threshold-voltage shift (ΔV_{th}), when changes in σ_{trap} and E_{trap} were neglected. In this case, the ITs in the device were considered to be charged with a charge equal to Q_{trap} (so, these simulations are equivalent to consider that there is a charge Q_{trap} at the position of the IT). Device V_{th} was calculated from the simulated I_D-V_G curves using the constant current method, for a threshold current $I_{th} = 1$ μA, when $V_D = 0.10$ V was applied.

3.1. Spatial distribution of traps

The contribution to the device ΔV_{th} of each individual trap, ΔV_{th}(IT), was analyzed. Fig. 3a shows a simulated current density map at the oxide/semiconductor interface for one device with $N_{trap} =$ 12 and $Q_{trap} = e^-$ (arbitrarily chosen). Numbers indicate the order in which the traps were introduced in the simulated device. As it can be observed, the current density decreases near the ITs, which can be explained because the traps create a barrier that can hinder the electron transport [7], leading to a change of V_{th}. Fig. 3b shows how each trap in Fig. 3a individually impacts the device V_{th}, by introducing a change ΔV_{th}(IT). Note that ΔV_{th}(IT) varies from trap to trap. As already demonstrated in [2,7], the trap impact on V_{th} depends on its position within the channel: traps in the channel (i.e. 1, 2, 4, 6, 7, 11) cause larger ΔV_{th}(IT) than traps closer to the source/drain contacts (i.e. 3, 5, 8, 9, 10).

To analyze in more detail this behavior, Fig. 4 shows the impact of one IT on V_{th} (IT) when it was swept along the z-axis (width) (Fig. 2a) and x-axis (length) (Fig. 2b). As it can be observed, the trap impact on V_{th} does not depend on the position along the z-axis (width). On the other hand, ΔV_{th}(IT) depends on the trap location along x-axis, dramatically decreasing when traps were close to the source/drain diffusions.

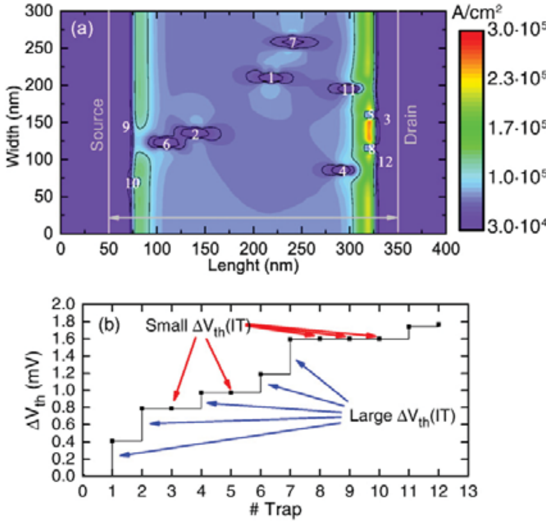


Fig. 3. Current density map at the oxide/semiconductor interface when 12 ITs are randomly located (a). Total ΔV_{th} of the device due to $\Delta V_{th}(IT)$ induced by each of the traps in panel a (b).

3.2. Charge per trap

The impact of Q_{trap} on ΔV_{th} was also evaluated. Fig. 5a shows, for 4 values of Q_{trap}, the statistical distribution of $\Delta V_{th}(IT)$ in 20 devices. Q_{trap} values lower than $1e^-$ should be interpreted as traps which are deeper in the oxide bulk, having a lower impact on V_{th}. The number of traps for each device (N_{trap}) was assumed to be Poisson distributed, with an average $N_{trap} = 12$. Besides, N_{trap} was assumed to be small enough to avoid any interaction between traps and, therefore, the results concerning $\Delta V_{th}(IT)$ are independent of the chosen N_{trap} value. Also, their position along the interface was randomly selected. Note that, as Q_{trap} increases, as reasonably expected, the distributions shift towards larger values, though their slopes seem to remain constant. The distributions in Fig. 5a were fitted to a Weibull distribution [8], as given by Eq. (1).

$$f(\Delta V_{th}(IT), \eta, \beta) = \frac{\beta}{\eta}\left(\frac{\Delta V_{th}(IT)}{\eta}\right)^{\beta-1} e^{\left(-\frac{\Delta V_{th}(IT)}{\eta}\right)^{\beta}} \quad (1)$$

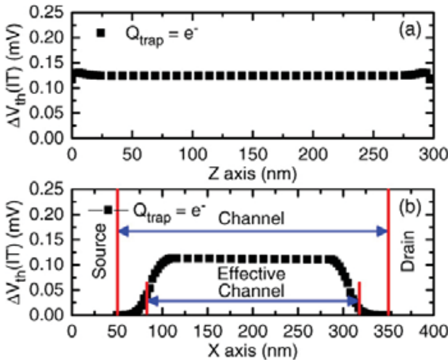


Fig. 4. ΔV_{th} (IT) for ITs located at different positions along z-axis (width) (a) and x-axis (length) (b). In (b) $\Delta V_{th}(IT)$ is smaller when traps are closer to the source and drain contacts. No dependence on Z was found.

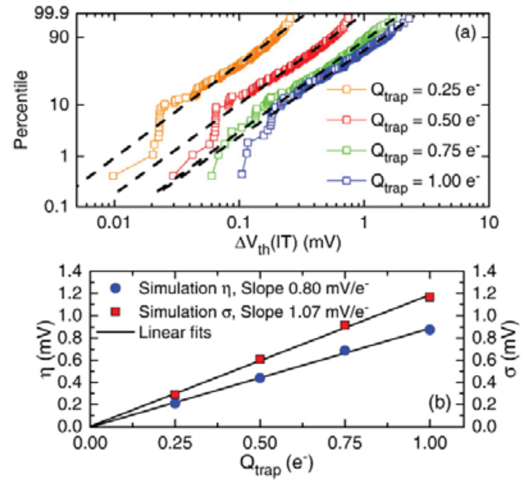


Fig. 5. Statistical distributions of $\Delta V_{th}(IT)$ obtained in 20 devices with average $N_{trap} = 12$ (Poisson distributed) and random spatial distribution for 5 values of Q_{trap}. Discontinuous lines represent the Weibull distribution fits (a). Plots of the scale parameter η and standard deviation σ vs. Q_{trap} (b) of the Weibull distributions in (a).

where β is the shape parameter and η is the scaling factor, which is related to the average $\langle \Delta V_{th}(IT) \rangle$. Moreover, the variance σ^2 of the $\Delta V_{th}(IT)$ is given by Eq. (2) [1,8]

$$\sigma^2 = 2\eta\langle \Delta V_{th}(IT)\rangle \quad (2)$$

The η and σ values obtained from the simulated distributions in Fig. 5a were extracted and plotted vs. Q_{trap} in Fig. 5b (circles and squares). As can be seen, the η and σ increases linearly with Q_{trap}, being their slopes equal to 0.80 mV/e^- and 1.07 mV/e^- respectively.

These two parameters can be obtained from measurements, so that their comparison to the simulated data (Fig. 5b) will allow to obtain the Q_{trap} value that better represents the experimental behavior observed in the considered technology. So, the experimentally observed (statistically distributed) effect of ITs on the device ΔV_{th}, $\Delta V_{th}(IT)$, which depends on the random spatial location of traps, can be fitted using Q_{trap} as single fitting parameter.

4. Transient simulations

In this section, the relation between the trap parameters σ_{trap} and E_{trap} (in TCAD tool) and (experimental data) τ_e and τ_c is described. 2D-transient simulations were performed considering one acceptor trap, i.e. E_{trap} is defined as the energy below the conduction band, in the center of the channel and using σ_{trap} and E_{trap} input parameters. Fig. 6 (black squares) shows the occupancy probability ($P_{occ}(t)$) of the trap, for an electron capture cross section $\sigma_{trap} = 10^{-15}$ cm^2 and energy level $E_{trap} = 0.15$ eV, when the applied bias is changed from $V_G = 0.10$ V to $V_G = 0.20$ V (at time 0 s) and back to $V_G = 0.10$ V (at time 1 ns) with $V_D = 0.10$ V.

Then, the simulated results (black squares) were fitted to an analytical model (Eqs. (3) and (4)) to obtain the corresponding τ_e and τ_c, which was assumed to describe the occupancy probability of a trap during a BTI stress [9].

$$P_{occ}(t) = P_{occ}(t_i) + \left(\frac{\tau_e(V_H)}{\tau_e(V_H) + \tau_c(V_H)} - P_{occ}(t_i)\right)\left(1 - e^{\left(\frac{t_i - t}{\tau_H}\right)}\right) \quad (3)$$

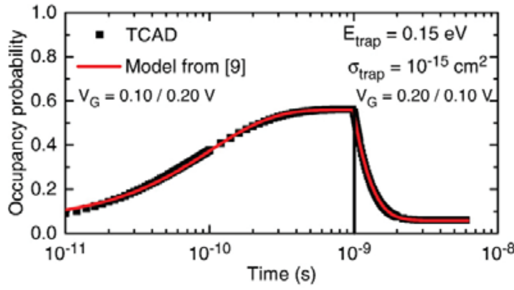


Fig. 6. Trap occupancy probability obtained during a transient simulation, when applied bias voltage changes are $V_G = 0.10/0.20$ V and $V_D = 0.10$ V (black squares). Analytical model fit (red lines).

$$P_{occ}(t) = \frac{\tau_e(V_L)}{\tau_e(V_L) + \tau_c(V_L)} + \left(P_{occ}(t_i) - \frac{\tau_e(V_L)}{\tau_e(V_L) + \tau_c(V_L)}\right) e^{\left(\frac{t_i - t}{\tau'_L}\right)} \quad (4)$$

where $P_{occ}(t)$ is the occupancy probability as a function of time, t_i initial time, τ_e and τ_c the trap emission and capture times for the particular applied stress voltage (V_L for low voltage and V_H for high voltage) and $(\tau')^{-1} = (\tau_e)^{-1} + (\tau_c)^{-1}$.

Fig. 6 shows the fitting of the TCAD simulation (black squares) to the analytical model equations (red line), from which τ_e ($V_G = 0.20$ V) = 0.45 ms, τ_c ($V_G = 0.20$ V) = 0.35 ms, τ_e ($V_G = 0.10$ V) = 0.10 ms and τ_c ($V_G = 0.10$ V) = 1.61 ms were obtained. To consider traps with different properties, E_{trap} and σ_{trap} parameters were swept (σ_{trap} from 10^{-14} to 10^{-17} cm^{-2} and E_{trap} from 0.05 to 0.25 eV) and the associated τ_e and τ_c evaluated, using the same procedure shown in Fig. 6. Fig. 7 shows a ($\tau_e - \tau_c$) map obtained for $V_G = 0.20$ V and $V_D = 0.10$ V. The results show that τ_c is reduced when E_{trap} is increased, whereas the opposite behavior is observed for τ_e, indicating that the electrons can be more easily captured in/emitted from deep/shallow traps. Moreover, Fig. 7 also shows that both times decrease when σ_{trap} is increased. Once this kind of plot has been constructed, the associated ($\sigma_{trap} - E_{trap}$) for a given experimental ($\tau_e - \tau_c$) can be evaluated. An arbitrary example (yellow star) is shown where $\tau_c = 0.2$ ms, $\tau_e = 3$ ms were considered as experimental parameters, so that $E_{trap} = 0.22$ eV $\sigma_{trap} = 10^{-16}$ cm^2 were found.

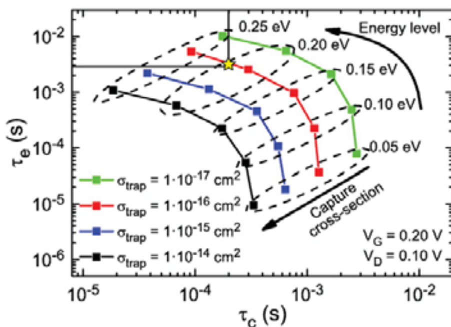


Fig. 7. Capture and emission times extracted from simulations with different E_{trap} and σ_{trap}. Applied voltage in all simulations was $V_G = 0.20$ V and $V_D = 0.10$ V. Yellow star shows an arbitrary example where experimental $\tau_c = 0.2$ ms, $\tau_e = 3$ ms are considered, with corresponding $E_{trap} = 0.22$ eV $\sigma_{trap} = 10^{-16}$ cm^2.

Once the TCAD parameters (E_{trap}, σ_{trap}), which are independent of operation conditions, of a trap characterized by (τ_e, τ_c) at a given voltage were obtained, they can be used to calculate the (τ_c, τ_e) at other voltages and temperatures without the need of experimental data at those new conditions. As an example, Fig. 8 shows how the (τ_c, τ_e) map plotted in Fig. 7, represented as blue surface, changes if the gate voltage is increased from 0.2 to 0.3 V (red surface). V_D is maintained constant at 0.10 V. Notice that, when the gate voltage is increased, capture times are reduced, and the emission times are increased for lower E_{trap} values and are kept almost constant for higher E_{trap} values, in agreement with [10]. The same methodology would apply for different operation temperatures. Therefore, these results show that, given an experimental (τ_c, τ_e) distribution at given bias/temperature conditions, the associated TCAD parameters can be obtained and then used to simulate the same device under different operation conditions, simplifying the characterization process. Therefore, the trap statistical effect on the device electrical characteristics at different conditions, also out of the experimental window, could be studied easier.

5. Conclusions

An interface trap parameter extraction procedure has been presented, which allows efficient statistical TCAD simulations of their effects in the MOSFET V_{th} variability. In particular, the methodology evaluates the physical parameters that describe the interface trap behavior in TCAD simulators (E_{trap}, σ_{trap} and Q_{trap}) from typical experimental (BTI or RTN) data (τ_c, τ_e and $\Delta V_{th}(IT)$). First, traps are included (with a number that is Poisson distributed) as fixed charges, randomly located at the interface, and the change in the V_{th} induced by each trap is calculated. The comparison of the experimental and simulated statistical distributions of this magnitude allows determining the value of the charge per trap that better describes the experiments. To account for the trap dynamics, transient simulations were performed, where the trap energy and cross section were input parameters. The occupancy probability of the traps was obtained by fitting the simulation transient results to an analytical model. From the fittings, the relationships between (E_{trap}, σ_{trap}) and (τ_e, τ_c) are obtained. The values of (τ_e, τ_c) at other bias/temperature conditions can be also obtained through simulation (without the need of additional experimental data), leading to a complete set of parameters with less experimental effort. Once these parameters are available, a statistically representative number of devices can be simulated, allowing the study of RTN and/or BTI-related variability through TCAD simulations, in reasonable computing times.

Acknowledgements

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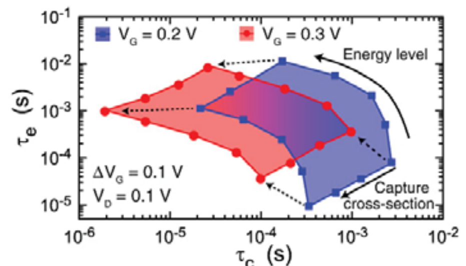

Fig. 8. (τ_e, τ_c) maps for different V_G, $V_G = 0.20$ V (red) and $V_G = 0.30$ V (blue). Arrows indicate how the points shift when the V_G is changed.

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Local Defect Density in Polycrystalline High-k Dielectrics: CAFM-Based Evaluation Methodology and Impact on MOSFET Variability

C. Couso, M. Porti, J. Martin-Martinez, A. J. Garcia-Loureiro, N. Seoane, and M. Nafria

***Abstract*— A methodology to determine with nanometer resolution the defect density in polycrystalline HfO_2 layers has been developed. This methodology is based on experimental data measured with conductive atomic force microscopy and the obtained results have been validated using Kelvin prove force microscopy measurements. The local defect density (ρ_{ox}) and thickness (t_{ox}) of the gate dielectric have been included into a device simulator to evaluate their impact on the $I_D V_G$ curves of MOSFETs.**

***Index Terms*— CAFM, KPFM, high-k, polycrystalline dielectric, MOSFET.**

I. Introduction

THE aggressive scaling of MOSFET devices to improve the performance of integrated circuits has led to the replacement of traditional gate oxides (as SiO_2) by high-k dielectrics [1]. However, under high temperature annealings, some high-k materials become polycrystalline [2], [3], so that variations of the oxide thickness and charge trapping can occur mainly at Grain Boundaries (GBs), which can affect the properties of scaled devices [4] and increase the device-to-device variability. Understanding this variability and how it impacts the device behavior is essential to introduce suitable countermeasures into the fabrication processes, device architecture and/or circuit design.

In this work, a new simulation methodology, with inputs coming from the nanoscale characterization of the dielectric, is proposed to evaluate the impact of high-k polycrytallization on the device electrical parameters (as threshold voltage, ΔV_{th}, I_{on} or I_{off}) of MOSFETs of a particular technology. From Conductive Atomic Force Microscopy (CAFM) topography and current maps, the insulator thickness and the defect density in the dielectric is estimated with nanoscale spatial resolution. These data are the inputs of a device simulator, which will evaluate their impact on the device characteristics.

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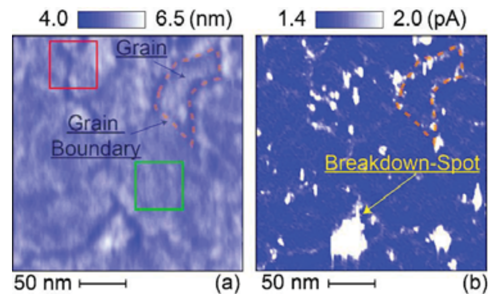

Fig. 1. Topography (a) and current (b) maps obtained at $V_G = 6.5$ V on a HfO_2/SiO_2/p-Si structure (250 nm × 300 nm). Grains, grain boundaries and breakdown spots are highlighted. Red and green squares correspond to the active area of MOSFETs whose I_D-V_G simulated curves are shown in Fig. 5.

II. Experimental Data

Experimental data were obtained from a gate stack consisting in a 5.3 nm thick atomic layer deposited HfO_2 film on a 0.7 nm SiO_2 interface layer (measured by X-Ray Reflectivity), which was grown on a Si epitaxial P-substrate. The gate stack was annealed at 1000 °C, which induced the crystallization of the high-k layer. In order to study the morphological and electrical properties of the polycrystalline dielectric with nanoscale resolution, topographical (Fig. 1a) and current (Fig. 1b) maps (obtained at 6.5 V, substrate grounded) were measured with a CAFM in vacuum using a diamond-coated silicon tip. Fig. 1a shows a polycrystalline surface where grain boundaries (GBs) (deeper areas) and grains (Gs) (higher areas) can be distinguished. Fig. 1b shows higher current at GBs than at grains (an example is highlighted in orange in the top right of topography and current maps). Besides, some breakdown spots were also detected [3].

III. Nanoscale Analysis

The dependence of the gate current with the HfO_2 thickness (t_{ox}) is shown in Figure 2. t_{ox} at each site of the surface, as shown in Fig. 1a, was estimated by assuming that the average thickness of the oxide layer measured by X-Ray Reflectivity (5.3 nm) corresponds to the average height of the topographical map. Any height deviation with respect to the topographical average at any site of Fig. 1a has been attributed to a deviation from the average t_{ox} of the same value. In Fig. 2, the data corresponding to GBs, Gs and breakdown spots (shown in Fig. 1) are indicated with rectangles. The color

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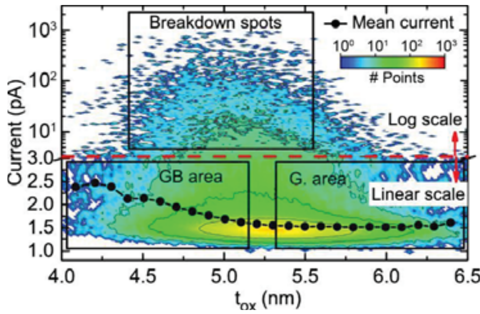

Fig. 2. Relationship between topography and current in the CAFM maps pixel by pixel. Color map shows the density of pixels for each pair of current and t_{ox} values. Dotted line shows the measured average current vs. t_{ox} (neglecting the contributions of breakdown spots).

scale of Fig. 2 indicates the number of pixels found in the images of Fig. 1 with a given current and t_{ox}. Note that more than 90% of the sites are in the range of few pA, indicating that the image sites linked to breakdown spots are negligible, so that the CAFM data are representative of the oxide before any degradation. In addition, the mean current (black points) was calculated for each t_{ox} denoting that the current in GBs regions is higher than in the Gs.

Although GBs show higher currents than Gs, notice also that GBs and Gs sites show a great variability in current values for a given t_{ox}, indicating that, in addition to t_{ox}, the gate current also depends on other parameters. Some works have pointed out that polycrystalline HfO_2 layers show larger defect densities at GBs, due to oxygen vacancies, which could affect the gate current [3], [5], [6]. This defect density (ρ_{ox}) could also affect the electrical characteristics and variability of MOSFETs and, therefore, it should be estimated in order to be introduced into the device simulator.

IV. Defect Density Estimation

In order to estimate the defect density, ρ_{ox}, at each site of the dielectric area in Fig. 1a (from the data obtained at the nanoscale with CAFM), the tunneling current at each pixel of the map in Fig. 1a was simulated using a previously developed simulator [7]. In [7], from the band diagram of the device and the measured t_{ox} (Fig 1a), the Quantum Mechanical Transmission Coefficient (QMTC) and tunneling current was found by applying the Airy wavefunction approach. However, the experimental current (Fig. 1b) does not match the calculated one (as its was shown in [7]) because in [7] the presence of ρ_{ox} was not taken into account. The difference between both currents (experimental and simulated) was assumed to be caused by the presence of ρ_{ox}, which, in this work, has been estimated with the following procedure.

First, a generic energy band diagram of the gate stack was determined by considering the material properties found in the literature [8], [9]. Notice that the tip-sample contact in CAFM experiments is not ideal. It depends on different experimental factors as, for example, the force applied to the tip [10] and/or the presence of a water meniscus for measurements in air [5]. Whatever the experimental conditions, to take into account the non-ideality of the contact, an additional barrier between

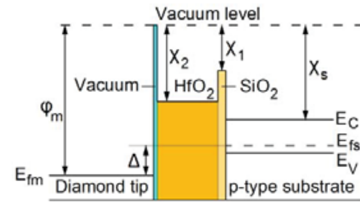

Fig. 3. An energy band diagram of a diamond tip/HfO_2/SiO_2/p-Si MOS structure.

the tip and sample is assumed, as it was also considered in [5], whose thickness will have to be calibrated (Fig. 3). Since in our case the measurements are performed in vacuum, the thickness of this extra barrier will be named t_{vac}.

To evaluate t_{vac}, (which is assumed to be uniform in all the sample), the band diagram is first determined at Gs by assuming an average t_{ox} = 5.75±0.05 nm (estimated from Fig. 2), $\rho_{ox} = 4 \cdot 10^{19}$ cm^{-3} (obtained from [5], [10], where the same sample was analyzed) and including the extra barrier with thickness t_{vac}. Then, the exact solution of one-dimensional Poisson equation [12], [13] is solved. Once the band diagram is determined, the tunneling current density was calculated using the equation (1) [9]:

$$J_{z,e} = \frac{e\sum_1^l n_{vl} m_{dl}}{2\pi^2\hbar^3}\int_0^\infty T_e(E_z)\,kTln \left\{\frac{\left(1+\exp\left[E_{fm}-E_z/kT\right]\right)^\lambda}{1+\exp\left[E_{fm}-E_z+(\Delta-eV_{ox})/kT\right]}\right\} dE_z \quad (1)$$

where l is the valley number, n_v is the valley degeneracy, m_d is the density-of-states mass per valley, k is the Boltzmann constant, T is the temperature, and V_{ox} is the oxide voltage. $\lambda = m_{ta,e}/m_{tb,e}$ is the ratio between the transverse effective mass of electron in the metal gate, $m_{ta,e}$, and that in the conduction band edge of the silicon substrate, $m_{tb,e}$, where $m_{tb,e} = \Sigma_l n_{vl} m_{dl}$. $T_e(E_z)$ is the electron transmittance that was calculated using the Airy function solution to the one-electron Schrodinger equation by the transfer matrix approach [14], [15]. By comparing the simulated current for t_{ox} = 5.75±0.05 nm (Grains) with the mean measured current at the same t_{ox} in CAFM maps, a barrier of t_{vac} = 0.40 nm was obtained.

Once t_{vac} was calibrated, ρ_{ox} was the only fitting parameter for the current simulation. Assuming an equivalent constant ρ_{ox} along the oxide thickness (as in [5], [11], and [16]), ρ_{ox} was estimated at each site of Fig. 1a by considering its corresponding t_{ox} thickness and by matching the simulated current with the measured current (Fig. 1b). It is important to note that breakdown spots were excluded of the analysis because they are not representative of the background sample behavior. Besides, sites with currents below 1.3 pA were neglected because the noise level could affect the data.

Fig. 4a shows the simulated positive charge density map calculated from the experimental maps shown in Fig. 1 and using the explained methodology. The comparison of Fig. 1a and Fig. 4a shows that, t_{ox} and ρ_{ox} are related, showing higher ρ_{ox} at GBs than at Gs. In particular, a linear relation between both parameters (t_{ox} and ρ_{ox}) was found (inset fig 4b).

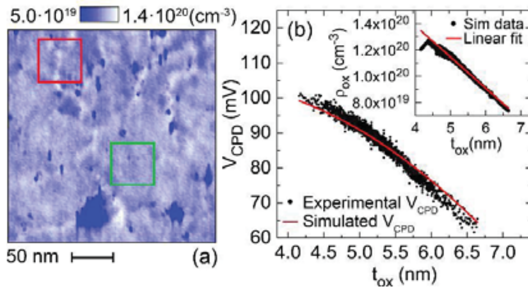

Fig. 4. Charge density map estimated from experimental data of Fig. 1 (a). Experimental V_{CPD} (dots) was obtained from KPFM maps measured on the same sample [17] (b). The inset shows the corresponding charge density. Lines are fittings of the experimental data.

In order to validate the methodology used to calculate ρ_{ox}, Kelvin Prove Force Microscopy (KPFM) data measured on the same sample (see [17]) was used to measure the topography and tip-sample Contact Potential Difference (V_{CPD}, which is related to the flat-band voltage of the MOS structure) of the same sample.

Then, the experimental V_{CPD} obtained (obtained with KPFM in [17]) was compared to the theoretical V_{CPD} (2) calculated from the relationship found between t_{ox} and ρ_{ox} (inset Fig. 4b) and taking into account the following equations:

$$V_{CPD} = \varphi_{s-m} + \frac{Q_i}{C_{s-m}} \tag{2}$$

where φ_{s-m} and C_{s-m} are the work-function difference and capacitance between the tip and semiconductor, respectively. Q_i is the equivalent surface density charge which is related to ρ_{ox} by (3) [14].

$$Q_i = \frac{q}{T_{ox}} \int_0^{T_{ox}} x \cdot \rho_{ox}(x) \cdot dx \tag{3}$$

V. Device Simulation

In order to evaluate the impact of the nanoscale properties (t_{ox} and ρ_{ox}) on the device electrical characteristics, a 3D in-house built parallel drift-diffusion (DD) device simulator [18] was used, which includes quantum corrections through the density-gradient (DG) approach [19]. The finite-element method has been applied to discretize the DD-DG equations, which allows the simulation of complex domains with great flexibility. A full description of the simulation methodology can be found in [19]. The 3D DD-DG simulator has been widely employed in the modelling of different sources of variability affecting semiconductor devices, such as random dopants [18], high-k gate dielectric [20], line-edge roughness [21], or grains in the metal gate [18]–[21].

As a test device, a WxL = 50 × 50 nm^2 gate area n-type Si MOSFET with a HfO_2/SiO_2 gate stack was considered, for simplicity. The nanoscale properties of the stack (morphology and defect density), given by Fig. 1a and Fig. 4a, were inputs of the device simulator. The S/D doping was obtained from the appropriate scaling of a 67 nm effective gate length MOSFET that was calibrated against experimental data [20].

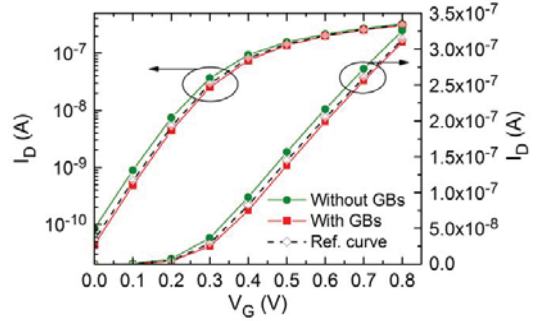

Fig. 5. I_D-V_G characteristics simulated at V_D = 50 mV for three 50 × 50 nm^2 MOSFETs. Red/green curves correspond to the simulated I-V curves of devices when dielectrics in the red/green squares in Fig. 1a and 4a are considered. Dotted curve corresponds to a reference device, with uniform HfO_2 thickness (5.3 nm) and trapped charge density ($1.08 \cdot 10^{20}$ cm^{-3}). The difference between the Vths of the devices with/without GBs (red/green I_DV_G curves) is 29.3 mV.

Fig. 5 shows the I_D-V_G characteristics at V_D = 50 mV for three MOSFETs with different gate oxides. First, a reference device was simulated (dotted line in Fig. 5) with uniform HfO_2 thickness and charge density, which correspond to the mean values of the maps color squares in Fig. 1a and 4a, 5.3 nm and 1.08 10^{20} cm^{-3}, respectively. Then, in order to study the influence of polycrystallization of the gate dielectric on the device electrical properties, two 50 × 50 nm^2 regions (see color squares in Fig. 1a and Fig. 4a) were chosen as gate areas of the MOSFET devices. One of them contains GBs (red square) whereas the other does not (green square). These data (t_{ox} and ρ_{ox}) were introduced into the device simulator to set the gate oxide properties. The simulated I_D-V_G curves are shown in Fig. 5 (continuous lines). Red/green I_D-V_G curves correspond to devices with dielectrics with/without GBs. Note that different currents can be observed in both devices, which, moreover, differ from those observed in the reference transistor. The differences in the currents of the devices with/without GBs (red/green I_DV_G curves) correspond to differences in their threshold voltages (V_{th}) of 29.3 mV. Note that this Vth shift is comparable to the time-zero variability observed in devices with the same size [22], showing the relevance of the impact of GBs on the device electrical characteristics and their device-to-device variability.

VI. Conclusion

A new methodology to evaluate, from CAFM measurements (topography and current maps), the trapped charge at each site of a polycrystalline dielectric, with nanometer resolution, has been presented. The procedure has been validated through the comparison of the obtained values with those measured with KPFM. The local thickness (experimentally obtained) and calculated charge density were the inputs to a device simulator, which allowed evaluating the corresponding I_D-V_G curves of MOSFETs. These curves show a clear device-to-device variability, as a result of the presence of GBs after crystallization. Though polycrystalline high-k dielectrics have been considered as case study, the proposed methodology can be extended to any dielectric whose electrical properties depend on thickness and defect density.

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Performance and Power Consumption Trade-Off in UTBB FDSOI Inverters Operated at NTV for IoT Applications

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ABSTRACT Power consumption and I_{on}/I_{off} ratio of an ultra-thin body and buried oxide fully depleted silicon on insulator CMOS inverter circuit has been calculated at near-threshold voltage operation from TCAD simulations. TCAD outputs (current, voltage, and capacitance) were used as parameters to solve the inverter circuit. Besides, a bias operation point (V_{OP}) has been proposed, which provides a good trade-off between the I_{on}/I_{off} ratio and the energy consumption. Variations of this operation point, due to the presence of interface traps, have been also analyzed.

INDEX TERMS Near-threshold voltage, power consumption, CMOS inverter, TCAD, IoT, UTBB FDSOI.

I. INTRODUCTION

The exponential increase of the number of transistors packed on chips and the stagnant of supply voltages (V_{DD}) is leading to a dramatic increase of the power density and energy consumption of the chips [1]. Moreover, Internet of Things (IoT) is changing the way of obtaining information from our environment (remote sensors) or even about ourselves ("wearables" or implantable devices). Devices used with this purpose have two common characteristics; they do not need to show a high performance but the energy consumption must be as low as possible. Therefore, the development of low-power technology is becoming one of the major design challenges [2].

In order to overcome this bottleneck, two solutions have been mainly reported in literature. On the one hand, ultra-thin body and buried oxide (BOX) fully depleted silicon on insulator (UTBB FD-SOI) technology could be a promising candidate to improve the power consumption, by adjusting the threshold voltage (V_{TH}) by applying body biasing voltage (V_{BB}) [3], [4]. On the other hand, devices operating in near-threshold voltage (NTV) improve the energy efficiency (10X or higher) at the cost of performance [5], [6]. Therefore, the study of energy consumption of logic gates composed by UTBB-FD-SOI devices, operating in NTV, could help to design a new generation of circuits [1].

Nevertheless, when circuits operate at NTV, not only their performance is reduced, but also their functional failures increase [7]. Variability sources such as random dopant fluctuation (RDF) or trapped charge in the gate or buried oxide can lead to functional failure or timing failure [7]. Therefore, an exhaustive study of energy consumption of circuits and the effects of such variability sources must be considered.

In this paper, the static and dynamic energy consumption of an inverter logic gate based on UTBB-FD-SOI devices operating in NTV are calculated from TCAD data. The TCAD tool used was ATLAS Silvaco [8]. Two structural parameters of the device, i.e., channel thickness (T_{SI}) and BOX thickness (T_{BOX}), and one operation parameter (V_{BB}), were considered to optimize the energy consumption of the inverter gate. These results could be assumed as a reference to be extended to more complex circuits. Finally, the impact of trapped charges in the gate oxide and BOX on energy consumption and operation frequency of the inverter gate was studied.

II. DEVICE SIMULATION

UTBB FD SOI 28 nm devices were considered to study the energy consumption in an inverter circuit from TCAD simulations using ATLAS Silvaco. The structure and doping data of devices were obtained from [3], [9], and [10] where different simulations and experimental results are presented

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for UTBB FD SOI technology. Similar V_{BB} values to those reported in [9] and [11] were considered. Table 1 shows a summary of the dimensions and doping taken into account in this work for a n-type device. By assuming CMOS balanced circuits [4], [12], the p-type device was considered to have the same electric behavior (i.e., same currents and capacitances for the same applied voltages) than the n-type transistor and therefore it was not needed to be simulated in TCAD. Fig. 1 shows the 3D simulated structure, the net doping level in the channel and the metallization contacts for n-type device.

TABLE 1. Parameters considered in the simulations.

Parameter	Value
Oxide thickness (T_G)	1.5 nm (EOT)
Channel thickness (T_{SI})	(10 – 25) nm
Oxide thickness BOX (T_{BOX})	(10 – 25) nm
Substrate thickness (T_{SUB})	60 nm
Gate length (L_G)	28 nm
Substrate doping (S_{DOP})	10^{16} cm^{-3}
Channel doping (C_{DOP})	$3\cdot10^{18}$ cm^{-3}
Width (W)	100 nm
Back Biasing voltage ($\|V_{BB}\|$)	(0 – 4) V

For the simulations, a non-regular mesh was considered in the structure in order to have a resolution less than 1 nm under the gate in the Y-axis and (1 – 2) nm in the X-axis and Z-axis. Thus, the electric potential can be accurately calculated, to study the impact of one trap on the device performance. Besides, a refined meshing in the channel was done proportional to the gradient of the doping profile.

Once the structure was defined, the models needed to simulate the device were chosen considering the next assumptions. The gate length is in the sub-100 nm regime and the FDSOI design is subjected to non-local effects such as velocity overshoot, diffusion associated with carrier temperature gradients and the dependence of impact ionization rates on carrier energy distributions [13], [14]. To this respect, the energy balance transport model, which adds the temperature as extra parameter in the transport of carriers, is used over the conventional drift-diffusion model, although the convergence and speed of simulation are slightly lower. Besides, in the ultra-thin channel, significance of quantum confinement of carrier becomes conspicuous, therefore the quantum effects must be taken into account. They are introduced using density gradient quantum correction [15]. Regarding the impact ionization, the Selberherr's model is assumed, because it includes temperature dependent parameters [16]. Finally, Fermi Dirac statistics and Shockley-Real-Hall (SRH) recombination are also considered in all simulations.

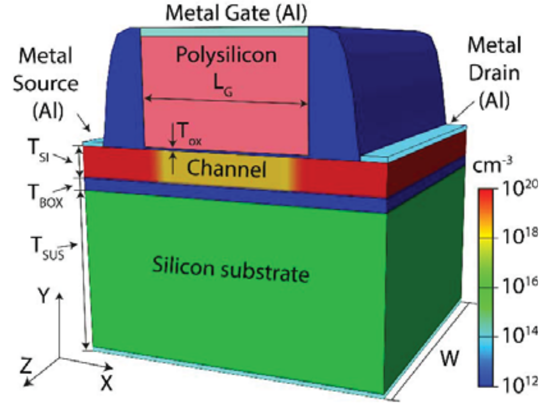

FIGURE 1. 3D TCAD structure of the simulated device showing the doping profile (not at scale).

Fig. 2a shows different I_DV_G curves for a nMOS device (T_{SI} =15 nm, T_{BOX} = 15 nm and V_{DS} = 0.1 V), for several V_{BB} from 0 to −4 V. Current values obtained are compatible with other works [17], [18], where devices of the same technology are studied. As it can be seen, when the $|V_{BB}|$ increases, I_DV_G curves show less current through the device modifying the V_{TH}.

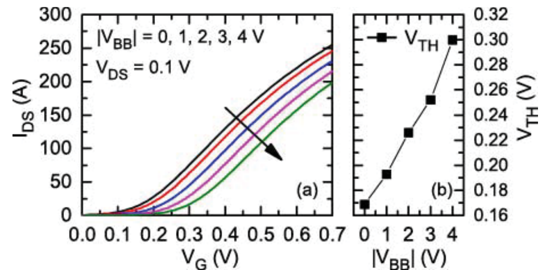

FIGURE 2. (a) I_DV_G curves simulated for several $|V_{BB}|$ for a nMOS device (T_{SI} = 15 nm, T_{BOX} = 15 nm and V_{DS} = 0.1 V). (b) The V_{TH} obtained from I_DV_G curves, as a function of $|V_{BB}|$.

Fig. 2b shows the V_{TH} variation as a function of V_{BB} where a linear relationship is found. Notice that the V_{TH} values range between 0.1 to 0.3 V, for the considered V_{BB}. The V_{TH} was calculated from I_DV_G curves applying the extrapolation in the linear region method [19]. Similar correlations of V_{BB} with V_{TH} were reported in [10].

III. SIMULATION RESULTS

To determine the energy consumption, two power dissipation mechanisms in an CMOS logic gate must be taken into account: the static power consumption (P_S), which is the result of the leakage current through the contacts of the devices in the circuit for the two logical states, and the dynamic power consumption (P_D), which is calculated by considering a capacitive load that is charged and discharged when the logic gate is switching. To evaluate this power

consumption, a circuit simulator such as SPICE can be used, considering a compact model to describe the electrical behavior of devices [11]. However, in this work, instead of a compact model, a TCAD simulator is used to evaluate the leakage currents at all contacts and the parasitic capacitances required to calculate the power consumption.

The key advantages of using TCAD simulation instead of compact models are that all device parameters can be changed easily, what allows parametric studies, and the parameters introduced in TCAD have a physical meaning. For instance, variability sources such as bias temperature instabilities (BTI) or random telegraph noise (RTN) can be introduced in the simulation, changing the physical parameters (trap parameters) which describe these phenomena [20]. As main drawback, the TCAD simulations consume more computational resources than compact models and therefore complex circuits cannot be easily simulated.

A. STATIC ENERGY CONSUMPTION

The static power consumption is a function of supply voltage (V_{DD}) and leakage current ($I_{leakage}$) flowing through the devices. In this work, the gate current and the drain–source current are considered as main contributions to the leakage current. Other leakage current contributions, such as bulk leakage current, are neglected, because the applied voltages are close to the threshold voltage. Actually, depending mainly on the gate oxide thickness and the applied voltages, the gate leakage current could be also neglected.

TABLE 2. nMOS voltages applied in TCAD simulations and corresponding voltages of the equivalent pMOS in an inverter.

Bias (V)	nMOS (on/off)	pMOS (on/off)
V_{gate_source}	V_{DD} / 0	V_{DD} / 0
V_{drain_source}	V_{OUT}	V_{DD} - V_{OUT}
V_{bulk_source}	-BB	-BB
V_{source}	0	0

Fig. 3a shows the $I_{leakage}$ simulated for the n-type device as a function of output voltage of the inverter (V_{OUT}), for different V_{DD}. These curves were estimated when the output of the logic gate was logic '0', i.e., the nMOS device was ON and pMOS OFF. Notice that pMOS device was considered electrically equivalent to the nMOS and therefore it was not simulated, saving computational time. The pMOS curves were derived from those of the nMOS, taking into account the voltages at device terminals when included in a CMOS inverter, which are shown in Table 2.

From the circuit analysis, (Fig 3.b) the crossing points of the curves in Fig 3.a represent the circuit solution where the $I_{leakage}$ flowing through both transistors is the same, for V_{OUT}. Note that in the case of evaluating the configuration of a logic "1", the voltages applied to devices would change, being nMOS in the OFF state and pMOS in the ON state.

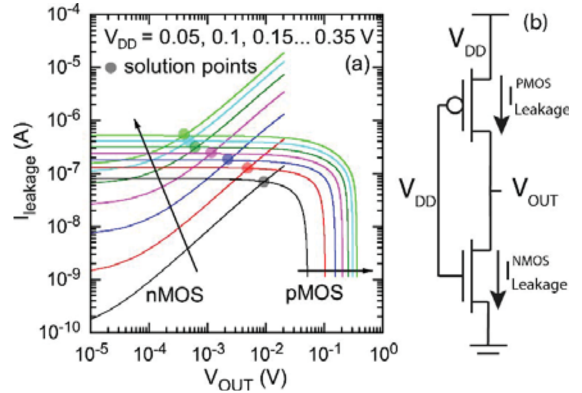

FIGURE 3. (a) $I_{leakage}$ as a function of V_{out} for different V_{DD} in an inverter logic gate. (b) Scheme of the inverter gate, highlighting $I_{leakage}$ for each transistor and V_{out}. The crossing points for the nMOS and pMOS curves represent the solution points of the circuit, where $I_{leakage}$ of both devices are equal.

The equation used to calculate the power consumption is;

$$P_s = I_{PMOS} \cdot (V_{dd} - V_{OUT}) + I_{NMOS} \cdot (V_{OUT} - 0) \quad (1)$$

where I_{PMOS} and I_{NMOS} are the currents flowing through the devices. To calculate the energy consumed per cycle, the power consumption is multiplied by the propagation delay (t_p) of one cycle, which can be calculated from the dynamic analysis in the next described section.

B. DYNAMIC ENERGY CONSUMPTION

CMOS dynamic power consumption is due to the current that flows when the inverter is switching from one logic state to the other. In order to estimate this energy consumption, the t_p is evaluated using a lumped load capacitance to ground (C_L). This load capacitance is the sum of all interconnect capacitances (including gate-drain capacitance (C_{GD}), drain-bulk capacitance (C_{DB}) and fan-out gates (C_G), (see Fig. 4a) connected to the output of the CMOS circuit [6]. Fig. 4b shows an example of gate parasitic capacitance as a function of gate voltage calculated by TCAD simulator. The other capacitances were also simulated and C_L calculated. The fan-out of the logic gate was considered equal to 1.

The equation that allows to calculate the dynamic energy consumption is;

$$E_d = C_L \cdot V_{DD}^2 \quad (2)$$

To evaluate the energy consumption, from eq. (1), the propagation delay, t_p is estimated by integrating the capacitor discharge/charge current. Equation (3) is a good approximation to calculate t_p from TCAD data [21];

$$t_p = 0.69 \cdot C_L \cdot \left(\frac{R_{eqn} + R_{eqp}}{2}\right) \quad (3)$$

where R_{eqn} and R_{eqp} are the equivalent resistance of nMOS and pMOS devices respectively. This propagation delay represents the minimum time needed to switch from one state

to the other. However in real circuits the logic gates are not switching as faster as possible, since their switching depends on the input signals. This is considered by adding an activity factor, whose value in this work is kept constant, to 0.001.

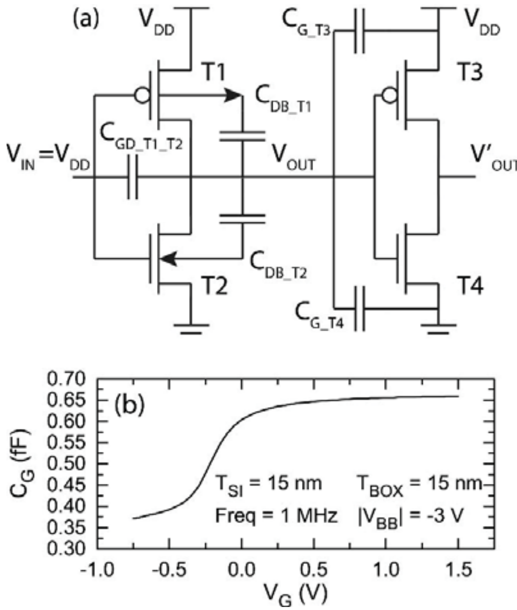

FIGURE 4. (a) Parasitic capacitances impact the transient behavior of the inverter, with fan-out equal to one. (b) An example of one gate parasitic capacitance.

Fig. 5 shows the total power consumption and maximum operating frequency (a) and the energy consumption per cycle (including the static and dynamic contributions) (b) as a function of V_{DD}. The considered parameters for those simulations were $T_{SI} = 15$ nm and $T_{BOX} = 15$ nm and the V_{BB} was equal to $-3/3$ V for n/p type. As it can be seen, when V_{DD} is scaled down (from 0.7 V to 0.4 V) the performance is reduced 1.7X, however, the energy consumption is improved 3.2X. This indicates that operating near the threshold voltage (see fig. 2b) reduces significantly the energy consumption [6]. Similar results have been obtained in circuits for other device technologies in [5] or for the same technology [11], [22] validating the methodology used in this work.

IV. PARAMETRIC STUDY

$|V_{BB}|$ and device structural parameters (such as T_{SI} and T_{BOX}) can impact the performance of UTBB FDSOI devices, and consequently, that of the inverter. Then, a detailed parametric study has been carried out, to evaluate the dependence of the energy consumption and I_{on}/I_{off} ratio of the inverter on those magnitudes.

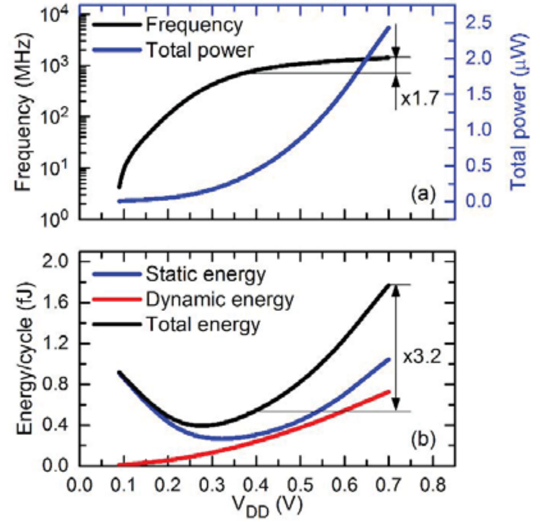

FIGURE 5. Simulated power, frequency and energy per cycle in a CMOS inverter implemented with UTBB FDSOI devices ($T_{BOX} = 15$ nm, $T_{SI} = 15$ nm) and the $|V_{BB}| = 3$ V.

A. DEVICE OPERATION STUDY (BB)

Firstly, the impact on the energy consumption and I_{on}/I_{off} ratio of the $|V_{BB}|$ applied to the devices in the inverter is analyzed. This current ratio is also included in the study, because in digital applications values around 1000 are required for this ratio (International Roadmap for Devices and Systems (IRDS 2016) [23]) in order to distinguish the logic states. The simulations were performed in 2D because device properties were assumed to be completely homogeneous in the Z-axis direction. This assumption reduces the computational time (minutes) compared to 3D simulations (hours).

Fig. 6a and 6b show the energy consumption and the I_{on}/I_{off} ratio as a function of V_{DD}, respectively, for different V_{BB} ranging (from 0 to $-4/4$ V in n/p type devices). Structure parameters are kept constant with values $T_{SI} =$ 15 nm and $T_{BOX} = 15$ nm. As it can be observed, when the $|V_{BB}|$is increased (negative values in nMOS and positive values in pMOS) the performance and consumption of the circuit improves. In fact, when $|V_{BB}| = 0$, V_{DD} for minimum energy is less than zero. These results can be explained through TCAD simulations. Higher $|V_{BB}|$ prevents the creation of the inversion layer under the gate. Therefore, the carrier concentration decreases (not shown), what rises the V_{TH} of devices and consequently reduces the current. Regarding the increase of the I_{on}/I_{off} ratio with $|V_{BB}|$ rises, it can be explained because Ion is only slightly reduced but I_{off} is diminished 2 orders of magnitude approximately.

As it can be seen, the V_{DD} that minimizes the energy consumption (yellow points Fig. 6a) and maximize the I_{on}/I_{off} ratio (yellow points Fig. 6b) are not coincident. Therefore an operation point that correspond to the best trade-off between

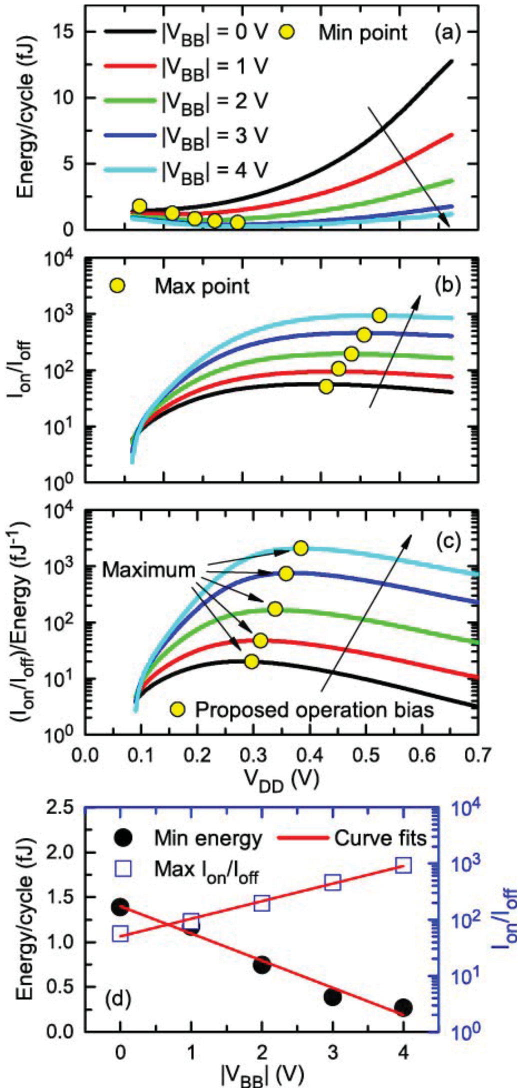

FIGURE 6. (a) Total energy consumption, (b) I_{on}/I_{off} ratio and (c) I_{on}/I_{off} and energy consumption ratio as a function of V_{DD}, for different $|V_{BB}|$ values. (d) Minimum energy consumption (black solid circles) and maximum I_{on}/I_{off} ratio (blue empty squares) as a function of $|V_{BB}|$. Red lines represent the data fitting. T_{SI} = 15 nm and T_{BOX} = 15 nm.

the two parameters has been proposed, as $\frac{I_{on}/I_{off}}{Energy\ consumption}$ which is shown in Fig. 6c. Note that this figure of merit has a maximum for a determined V_{DD} (yellow points Fig. 6c) whose value, V_{OP}, is proposed as an operation point of the inverter.

Fig. 6d shows the minimum energy consumption and the maximum I_{on}/I_{off}, as a function of $|V_{BB}|$. The studied devices show a linear dependence of the minimum energy consumption on $|V_{BB}|$. It is worth highlighting that this linear dependence is not accurate at the extreme values of $|V_{BB}|$ (0 and 4 V) indicating a possible saturation of the tendency. On the other hand, a logarithmic dependence is found for the maximum I_{on}/I_{off} as a function of $|V_{BB}|$. This kind of relationships could be useful in order to optimize the $|V_{BB}|$ voltage because they allow to predict the minimum $|V_{BB}|$ required to reach a target parameter.

B. DEVICE STRUCTURE STUDY (T_{BOX}, T_{SI})

A similar study to that shown in the previous section has been performed, but now, sweeping T_{BOX} between 10 and 25 nm, while the other parameters are kept constant T_{SI} = 15 nm and $|V_{BB}|$ = 3 V. Minimum energy consumption and maximum I_{on}/I_{off} ratio as a function of T_{BOX} is represented in Fig. 7a. Moreover similar dependences of the minimum energy (linear) or maximum I_{on}/I_{off} (logarithmic) on T_{BOX} is observed as for the case of $|V_{BB}|$ Fig. 6d. The results indicate that a thinner BOX improves the electrical characteristics of the devices, reducing the energy consumption and rising the I_{on}/I_{off} ratio Fig. 7a. Fig. 7b represents the ratio I_{on}/I_{off} - energy as a function of V_{DD} showing that the V_{OP} increases when the T_{BOX} decreases, but it is still kept near to the threshold voltage. This dependence can be explained because smaller T_{BOX} leads to a higher influence on the carriers of the channel, increasing the device currents.

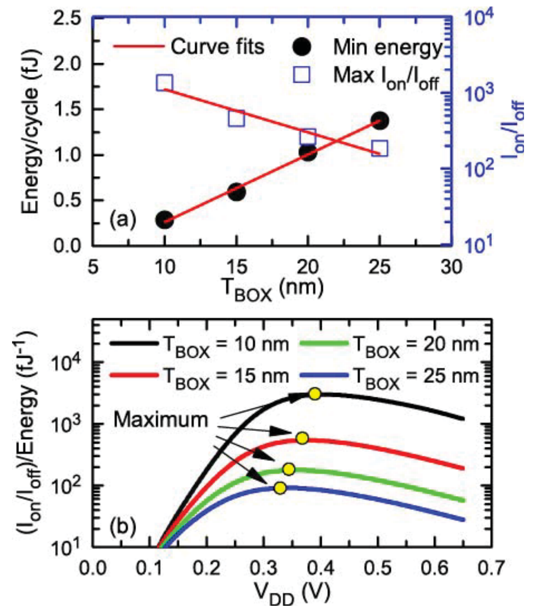

FIGURE 7. (a) I_{on}/I_{off} and energy consumption ratio as a function of V_{DD}, for different T_{BOX}. (b) Minimum energy consumption (black solid circles) and maximum I_{on}/I_{off} ratio (blue empty squares) as a function of T_{BOX} (b). Red lines represent the data fitting. T_{SI} =15 nm and $|BB|$ = 3 V.

Finally, the impact of T_{SI} is analyzed in Fig. 8 (T_{BOX} =15 nm and $|BB|$ = 3 V). Minimum energy consumption and maximum I_{on}/I_{off} ratio as a function of T_{SI} are

represented in Fig. 8a. When T_{SI} is diminished, the energy consumption and I_{on}/I_{off} improve significantly. This improvement in the energy consumption can be explained because the current flowing through the channel is smaller for thinner T_{SI}. On the other hand, the improvement of I_{on}/I_{off} ratio can be explained because the gate exerts more control over the channel. Besides, similar dependences are observed when T_{SI} is changed than when T_{BOX} is varied. Nevertheless, in our structure, in the case of energy consumption, a higher dependence on T_{BOX} than on T_{SI} is observed, whereas the opposite is observed for the case of the I_{on}/I_{off} ratio. These relations indicate that a trade-off between both device parameters could be considered in order to optimize circuits for a particular propose. Fig. 8b shows V_{OP} (yellow points) for the different values of T_{SI}, obtaining similar values than those when T_{BOX} is swept.

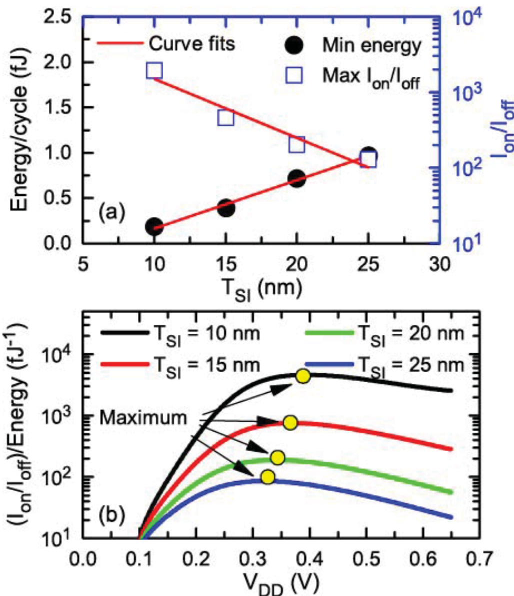

FIGURE 8. (a) I_{on}/I_{off} and energy consumption ratio as a function of V_{DD} for different T_{SI}. (b) Minimum energy consumption (black full circles) and maximum I_{on}/I_{off} ratio (blue empty squares) as a function of T_{SI}. Red lines represent the fitting performed. T_{BOX} = 15 nm and |BB|= 3 V.

In order to contextualize our results, the requirements for future technologies, the energy consumption per cycle and I_{on}/I_{off} ratios obtained for each V_{OP} estimated previously (see Fig. 6c, 7b and 8b) are compared to those given by [23]. To do this, in Fig. 9 the I_{on}/I_{off} ratio as a function of the energy consumption per cycle is represented. In solid black squares, the IRDS projected electrical specifications of logic core devices for each year are shown. The empty symbols represent our best result obtained for each of our studies ($|V_{BB}|$ = 4 V red circle, T_{BOX} = 10 nm green triangle and T_{SI} = 10 nm blue diamond), for the corresponding V_{OP}. Our results show lower energy consumption than projections beyond 2027 for all the studied cases, pointing out that UTBB-FD-SOI operating at NTV, with suitable $|V_{BB}|$, is an attractive candidate for low power applications. [3], [11]. However, the I_{on}/I_{off} ratio for $|V_{BB}|$ = 4 V and T_{BOX} = 10 nm are 46 % and 22% smaller than prediction respectively. Only when T_{SI} = 10 nm, the I_{on}/I_{off} ratio is comparable to the projections. This result indicates that T_{SI} parameter can play an important role to optimize this kind of devices.

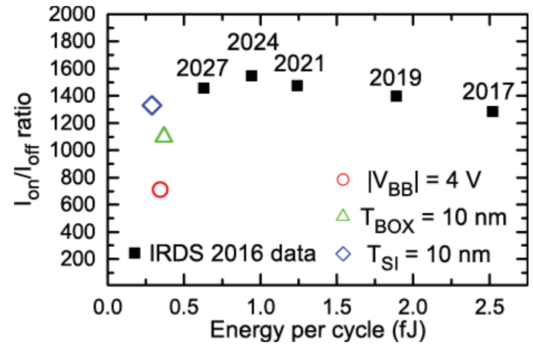

FIGURE 9. Comparison of energy consumption per cycle and I_{on}/I_{off} ratio of IRDS 2016 predictions from 2017 to 2027 (black solid squares) and our results (empty symbols).

C. IMPACT OF OXIDE TRAPPED CHARGE

Until now, simulated devices have not been considered to be affected by any variability source. In this section, the impact of interfacial traps charged with 1e$^-$ on the frequency and energy consumption per cycle is analyzed. In particular, as a preliminary analysis, the study is focused on the comparison of these parameters in the pristine device to these devices where one trap is present in the gate oxide-channel (see Fig. 10a and 10b), in the BOX oxide-channel interface (see Fig. 10c and 10d) or both traps are simultaneously present. Since the presence of discrete charges in the devices breaks their homogeneity, the simulations were performed in 3D, with W = 100 nm. In the simulations T_{SI} = 15 nm, T_{BOX} = 15 nm and the $|V_{BB}|$ = 3 V were considered.

Fig. 10 shows the impact of one trap on the potential contour map in a n-type device, top (a) and sectional (b) view when it is introduced in the interface gate oxide–channel, and top (c) and sectional (d) view of the potential contour when the trap is located in the interface channel–BOX oxide. The bias applied to gate and drain contact was 0.35 V. As it can be observed, the trap modifies the device potential, hindering the carriers flow in the channel and consequently increasing the V_{TH} [20].

The change in the electrical behavior of devices because of the introduction of interfacial traps can provoke variations in the performance of logic gates. To show this point, frequency and energy consumption per cycle are analyzed, because large variations of these parameters in logic gates could be critical for design circuit [7].

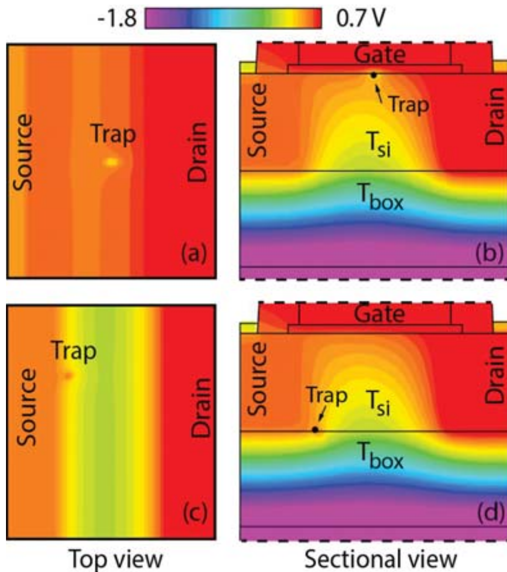

FIGURE 10. (a, c) Potential maps of top and (b, d) sectional view of the device (T_{SI} = T_{BOX} = 15 nm and Vbulk = -3 V) when the trap is at the gate oxide (a,b) and at the BOX (c, d) interface. Gate and drain contacts are biased V_{GS} =V_{DS} = 0.35 V.

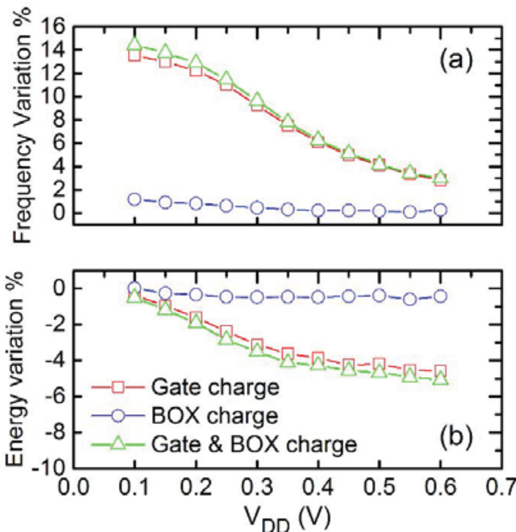

FIGURE 11. (a) Frequency and (b) energy consumption shift when traps are present at gate (red squares), BOX (blue circles) and both simultaneously (green triangles) as a function of power supply (V_{DD}).

Fig. 11a shows the frequency variation when charges are present compared to pristine devices. The impact of trap location was studied simulating three different scenarios; trap located at gate (G) interface, BOX interface (B) or both simultaneously (G & B). As it can be seen, traps located at the gate (red) have more impact than traps located at the BOX (blue) interface. Besides, the impact of both traps (simultaneously in the device) almost correspond to the sum of each trap separately, pointing out that the simulated traps, in our case, are independent. Also, the frequency variation depends on V_{DD}, being higher than 10% when V_{DD} is smaller than 0.30 V.

Fig. 11b shows the variation of energy consumption per cycle. Note that the variations are negative indicating that introducing traps in the device improves slightly the power consumption, around 4%. The cause of this improvement could be attributed to the reduction of leakage currents through the channel.

V. CONCLUSION

New strategies must be developed in order to reduce the power consumption of devices used in IoT. In this paper, UTBB-FD-SOI devices, which have been demonstrated to be good candidates for low power applications, have been considered operated at NTV for digital applications. The electrical characteristics of the devices have been simulated using Silvaco TCAD tool. The TCAD results were used to calculate the energy consumption and operation frequency of an inverter logic gate. The dependence of these parameters on two structural properties of devices (T_{BOX} and T_{SI}) and operation conditions (V_{BB}) has been studied. Our results indicate that higher |BB| and thinner T_{SI} and T_{BOX} improve significantly the energy consumption and I_{on}/I_{off} ratio of the logic gate. However, their impacts are different, and therefore an optimization criterion, which will depend on the application, must be considered. Besides, an operation point (V_{OP}) has been selected which could be useful on digital applications because it provides a good trade-off between the I_{on}/I_{off} ratio and the energy consumption. These results were compared to IRDS projections pointing out FD-SOI devices with thin T_{SI} and T_{BOX} operating at NTV as a promising technology in low power applications. Finally, the impact of interfacial traps on the frequency and energy consumption of the logic gate was studied obtaining variations in the frequency larger than 10%. Therefore, the variability related to the presence of charges in the gate and BOX oxide interfaces can be critical for the performance of circuits based on these devices operating in NTV.

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Appendix II

Paper: IEEE EDL (May 2016)

Conductance of Threading Dislocations in InGaAs/Si Stacks by Temperature-CAFM Measurements

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Abstract— **The stacks of III–V materials, grown on the Si substrate, that are considered for the fabrication of highly scaled devices tend to develop structural defects, in particular threading dislocations (TDs), which affect device electrical properties. We demonstrate that the characteristics of the TD sites can be analyzed by using the conductive atomic force microscopy technique with nanoscale spatial resolution within a wide temperature range. In the studied InGaAs/Si stacks, electrical conductance through the TD sites was found to be governed by the Poole–Frenkel emission, while the off-TDs conductivity is dominated by the thermionic emission process.**

Index Terms— **CAFM, semiconductor defects, threading dislocation, thermionic emission, Poole Frenkel emission.**

I. Introduction

HIGH MOBILITY channel transistors for complex multi-device circuitries are considered to be fabricated using III-V materials locally grown over the Si substrate. Due to the lattice mismatch between these materials, the III-V films tend to form structural defects [1], in particular Threading Dislocations (TDs), which may contribute to charge carriers transport thus degrading device performance [2], [3]. In particular, TDs enhance current conduction in forward and reverse biased diodes [4] and increase device-to-device variability due to the formation of multiple parallel paths with different conductivity (on- and off-TD sites) [5]. In HEMTs, TDs increase reverse gate leakage current and frequency related noise (affecting, for example, low-noise amplifiers [3]) and reduce drain saturation current, peak transconductance, off-state breakdown voltage and cutoff frequency [3]. In InGaAs nMOSFETs, TDs severely reduce carrier mobility [6], [7], affecting I_{ON} and V_{TH} and limiting drive current. Therefore, monitoring the TDs' contribution/effect to the charge transport through the III-V channels is critical for controlling/improving device characteristics [3], [7].

Electrical conduction through III-V films has been previously studied on fully processed devices by measuring I-V characteristics [1], [8], [9]. However, these device level measurements register the overall current through the entire device area that may mask the current component associated with TDs. Therefore, since TDs cross-section dimensions can be in the nanometer range, employing techniques with the nanoscale spatial resolution capability, such as the Conductive Atomic Force Microscopy (CAFM), is expected to provide TD-specific conductivity data. Indeed, the CAFM technique has been widely used for nanoscale electrical characterization of the defects in gate dielectrics, either grown or generated under the applied electrical stress and irradiation [10]–[17], as well as TDs in III-V based stacks. In the latter, the I-V measurements were performed on the TD sites attributed to the surface pits (as was observed in the CAFM topographical images). These sites exhibited lower turn-on voltages and higher leakage currents under the forward and reverse biases [4], [5], [18]–[20]. Higher forward currents through TDs was attributed to Poole-Frenkel (PF) conduction [19], [20] and described as caused by lowered barrier heights of the Schottky contacts between the tip and samples [5].

In the above studies, CAFM measurements were performed at ambient temperatures, and, in some instances, were combined with the device level I-V characteristics collected at different temperatures, which allowed attributing the reverse current to the PF emission [9], [21]. However, the device-level I-V data could not be linked exclusively to the TDs electrical properties because they were also affected by contributions from the electrically active non-TD device area. The present study extends the analysis by performing CAFM measurements of the localized (contact site specific) current-voltage characteristics, on both on-TD and off-TD sites in the III-V/Si stack, at different temperatures.

II. Sample Preparation and Characterization

The CAFM measurements were performed with an Asylum MFP3D System, using ORCA module with a Polyheater sample stage. This configuration allows for conductivity measurements (from 100 pA to 10 μA) while keeping the tip grounded and in a temperature range up to 300 °C. The sample investigated with CAFM consists of a Te:InGaAs 30 nm/InGaAs 120 nm/InP 600 nm/GaAs 500 nm/Si stack. Fig. 1 (a) shows a cross section TEM image of a studied stack. In Fig. 1 (a), structural defects (TDs) can be observed

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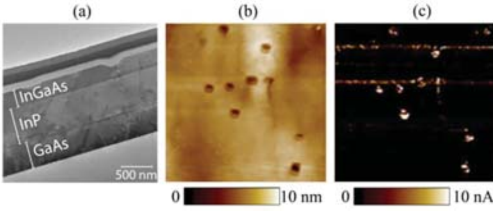

Fig. 1. (a) TEM cross section image. (b) Topographical and (c) reverse current (measured at 2 V) CAFM images collected on 7.5 × 7.5 μm^2 area. Two bright lines in the upper region of a current map (c) correspond to AFM artifacts.

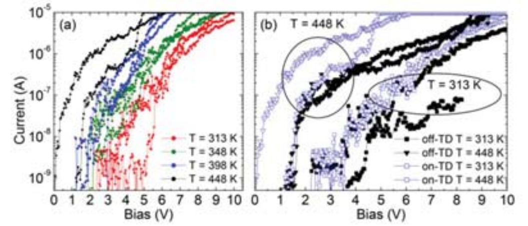

Fig. 2. (a) Set of I-V curves measured on different TDs sites (same temperature color). (b) Example of I-V curves measured on-TDs (open symbols) and off-TDs (solid symbols) at 313 K and 448 K.

propagating from the interface with a Si substrate and may extend significantly through the III-V material thickness, in some instances reaching the film surface.

To identify the TDs locations on the surface, topographical and current maps were measured simultaneously by scanning the CAFM tip on randomly selected surface areas of the stack. Fig. 1 shows (b) topographical and (c) current maps at 2 V, injection from the tip. Detected surface pits in Fig. 1 (b) (attributed to TDs) match those of the high conduction sites in the current map. I-V curves on the targeted defect sites were then collected using ramped voltage measurements. The tip-sample contact was characterized as being of the Schottky type [22], although currents under the reverse bias condition partially cover the rectifying features.

To compare temperature dependencies of the conduction through on-TDs and off-TDs sites, CAFM I-V measurements were performed at several temperatures (313, 348, 398 and 448 K) at both sites. It is important to note that the CAFM-based I-V measurements at different temperatures are technically rather complex to execute. To change temperature, the tip must be withdrawn from the sample surface, and then it has to be repositioned on the same site, which is a challenging task in the case of the required highly scaled area range. On the other hand, the measurement itself could modify the TD electrical properties: changes in electrical conductivity, observed after the site was re-measured at different temperatures, might be dominated by structural changes (charge trapping) induced by previous measurements on this site [23]. To mitigate such uncertainty, a statistical analysis of the electrical conductivity data collected at each temperature on different TD sites was carried out (I-V curves were not measured repeatedly on the same site). This method was found to be more accurate than measuring a fixed TD site at different temperatures. In order to ensure the stability of tip properties during the experiments, the Pt bulk tips were used.

III. Results and Discussion

Fig. 2 (a) shows examples of I-V curves measured over the TDs (on-TDs sites) at 4 different temperatures within the 313 K-448 K range. Similar measurements have been performed over the regular (off-TDs) surface sites. Comparisons of the I-V curves measured on-TDs (open symbols) and off-TDs (solid symbols) at 313 and 448K, Fig. 2(b), demonstrates that the on-TD currents are higher than those of the off-TDs, consistent with the data in the images in Fig. 1. Moreover, currents through the sites and, subsequently, their conductivities, increase with temperature, more pronouncedly in the on-TD sites. Assuming that higher current values over the on-TD sites (compared to the off-TDs) are associated with their structural defects, the measured I-V dependencies were modeled using the Poole-Frenkel (PF) emission process [19]:

$$J = C \times E \times exp\left\{-q/KT\left(\phi_t - \sqrt{qE_b}/\pi\varepsilon_0\varepsilon_s\right)\right\} \quad (1)$$

where J is the current density, E the electric field over the energy barrier at the tip-semiconductor interface, q is the electron charge, K is the Boltzmann constant, ε_0 and ε_s are the vacuum and relative dielectric permittivity (at high frequency) of the semiconductor, respectively, T is the temperature, Φ_t is the barrier height for electron emission from the trapped state and C is a constant. The electric field dependency in the PF process can be linearized when plotting (1) as:

$$ln(J/E) = R(T) \times \sqrt{E} + S(T) \quad (2)$$

$$R(T) = q/KT\left(\sqrt{qE/\pi\varepsilon_0\varepsilon_s}\right) \quad (3)$$

$$S(T) = -q\phi_t/KT + \ln(C) \quad (4)$$

where $R(T)$ and $S(T)$ are the slope and y-intercept, respectively.

The I-V curves in Fig. 2 (a) are re-plotted following the expressions of (2-4) (see Fig. 3 (a), a single I-V curve is shown for each temperature). At each temperature, the measured (re-plotted) I-V dependencies generally follow (although they fluctuate) a trend of (2) (shown by the linear lines in Fig. 3 (a) suggesting that the conduction through the TDs is consistent with the PF mechanism (1).

The average values of S(T), the y-intercept values of the fit (solid) lines in Fig. 3 (a), are plotted as a function of 1/T (triangles) in Fig. 3 (b). The S(T) linear dependency on 1/T is reflected by a solid line. The S(T) slope is proportional to the emission barrier height Φ_t (4), which calculated value of 0.51 eV is compatible to the reported ones [24]. Similarly, the slopes of the fit lines in Fig. 3 (a), R(T), also show a linear dependency on 1/T (squares) in Fig. 3 (b). Using (3), ε_s is estimated to be about 4.52. It must be noted that the calculated values of Φ_t and ε_s have been obtained from a linear fitting of the S(T) and R(T) average values at different temperatures. The S(T) and R(T) average values (at a given T)

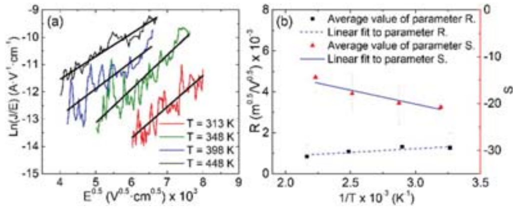

Fig. 3. (a) Measured I-V curves in Fig. 2 (a) are plotted (one curve per each T) following the expressions (2-4). The linear lines represent the fittings using (2-4). (b) R(T) (squares) and S(T) (triangles) mean values in the y-axis, which are the slope and the y-intercept values of the entire set of measured I-V curves respectively, as a function 1/T. Continuous lines show the linear dependency of R(T) and S(T) versus 1/T in (3 and 4).

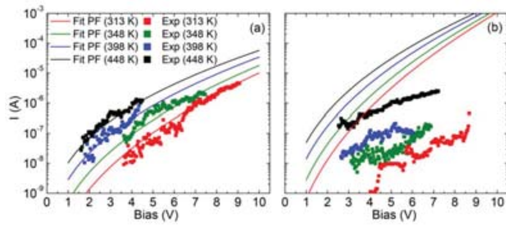

Fig. 4. I-V curves (symbols) measured on-TD (a) and off-TD (b) sites at different temperatures. Solid lines correspond to the calculated PF current using the parameters obtained by the fitting of S(T) and R(T).

used in the linear fitting correspond to the average values of S and R obtained from the data collected on different TDs sites. Therefore, the calculated values of Φ_t and ε_s correspond to an average value of the analyzed sites.

To verify the validity of the PF-based mechanism in TDs, the current in (1) was calculated using the average value of the physical parameters in (3 and 4). Fig. 4 (a) shows the experimental I-V curves measured at different temperatures (symbols) and I-V dependencies calculated using the PF equation (solid lines) with the experimentally determined parameters, which includes only one I-V curve for each T of Fig. 2. The data at low biases (noise level of the setup) and very high biases (possible parasitic), is not shown. I-V trends based on the PF emission mechanism fit well the measured ones.

Although the on-TDs conduction is generally higher than that of the background areas, the off-TD conductivity is not negligible (see Fig. 2 (b)) and, therefore, needs to be evaluated. The above presented procedure was applied to the data in Fig. 2 (b), yielding $\Phi_t = 0.53$ eV and $\varepsilon_s = 2.56$ values. However, the I-V curves calculated by using these parameters do not match the experimental data (see Fig. 4 (b)). Hence, the above analysis demonstrates that the PF emission is dominant process exclusively in the TD sites.

I-V curves measured under the reverse-bias on the off-TD sites were fitted by the Thermionic / Schottky Emission (TE) mechanism:

$$J = A^* \times T^2 \times exp\left\{-q/KT\left(\phi_b - \sqrt{qE/4\pi\varepsilon_0\varepsilon_s}\right)\right\} \quad (5)$$

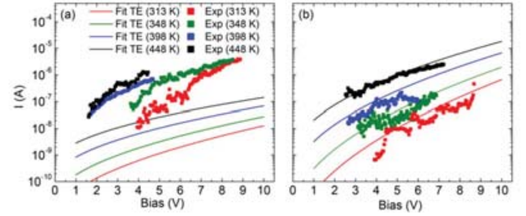

Fig. 5. I-V curves (symbols) measured on the on-TDs (a) and off-TD (b) sites at different temperatures. Solid lines correspond to the calculated TE current using the parameters obtained by the fittings of S'(T) and R'(T).

Here A^* is the effective Richardson constant, Φb is the Schottky barrier height and E the electric field over the energy barrier at the tip-semiconductor interface (related to the bias applied to the structure); remaining parameters are defined previously. Thus, using a procedure similar to that used in the on-TDs case can be followed to estimate Φb in S'(T). Since TE process is effective predominantly at high temperatures, only the data measured at 348, 398 and 448 K were considered. The barrier height and permitivity for the off-TD sites were found to be Φb = 0.61 eV and $\varepsilon_s = 3.9$, respectively.

Fig. 5 (b) shows experimental off-TD I-V curves (symbols) and calculated TE current for each temperature (solid lines) using (5) and the values obtained from the experimental data ($\Phi_b = 0.61$ eV and $\varepsilon_s = 3.9$). Note that the experimental data matches very well to the TE-based calculations (especially at a higher temperature, when the TE process dominates). Therefore, off-TD current could be described by considering electrons tunneling over the barrier when the process of the defects assisted electron transport can be negligible. The observation of high off-TDs currents under the reverse bias conditions could be understood by considering a low barrier height for the electrons injected from the metal ($\Phi_b = 0.61$ eV), which depends, in our case, on the materials in a CAFM tip and top layer of the analyzed sample.

Following the procedure employed above in the case of the on-TDs I-V curves for the TE emission, $\Phi_b = 0.37$ eV and $\varepsilon_s = 11.7$ were obtained, respectively. However, the I-V curves calculated by using these parameters in (5) do not match the experimental data (Fig. 5 (a)). This result further supports the conclusion that the conduction through the on-TD sites can be described by considering the PF emission, but not the TE process, pointing-out that TDs are a major component of enhanced reverse-leakage current through III-V materials. Presented data demonstrate that, thanks to the nanoscale resolution, the employed methodology provides a valuable insight to the TDs conduction properties, critical for optimizing multi-level structures of scaled devices.

IV. Conclusion

Conduction through TDs sites in the III-V materials have been investigated using CAFM-based measurements at different temperatures. The conductivity of TDs, observed as the surface pits in topographical maps, is found to be higher

than that of the off-TD sites. In both on- and off-TD sites, the currents were observed to increase with temperature. The on-TD electrical conduction can be described by accounting for the Poole-Frenkel (PF) emission process suggesting that it can be the dominant conduction mechanism at these sites. Conductivity of the off-TD sites, in particular, at higher temperatures, seems to be controlled by the thermionic emission mechanism. In summary, the results demonstrate that the CAFM technique is well-suited for evaluating the TDs electrical properties with the nanoscale resolution, required to identify material structural features affecting device performance.

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Dependence of MOSFETs threshold voltage variability on channel dimensions

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***Abstract*— The dependence of the MOSFET threshold voltage variability on device geometry (width (W) and length (L)) has been studied from experimental data. Our results evidence, in agreement with other works, deviations from the Pelgrom's rule, especially in smaller technologies. TCAD simulations were also performed which further support the experimental data and provide physical information regarding the origin of such deviation. Finally, a new empirical model that assumes different impact of W and L in the device variability has been proposed, which reproduces the experimental results.**

Keywords-Pelgrom's law; charges; variability; MOSFET.

I. INTRODUCTION

Understanding the dependencies of the variability of the threshold voltage in MOS devices constitutes a challenge that must be faced in order to optimize the circuit design. According to Pelgrom's rule, MOSFET threshold voltage (V_{th}) variability is inversely proportional to the square root of the active transistor area [1]. However, significant deviations from this rule have been reported on experimental data, especially in 65 nm technologies and beyond [2], [3]. The origin of this deviation have been studied in previous works [4], [5], where several sources of variability such as Random Dopant Fluctuation (RDF), interfacial traps, etc., [4] were pointed out as the origin of this mismatch. Nevertheless, they have not been fully clarified yet.

In this work, it is experimentally shown that the dependences of V_{th} variability associated to W and L should be decoupled. TCAD simulations have been performed in order to elucidate the physical origin of the different dependences. Finally, an empirical model has been proposed and validated using the experimental and simulated data.

II. EXPERIMENTAL DATA

A large set of pMOS and nMOS devices of different W and L manufactured in a 65 nm CMOS technology has been characterized. Table I indicates the number of DUTs tested for each device geometry. Note that in some cases W and L are fixed (yellow and green cells in Table I), which allows to study the V_{th} variability when only one of the dimensions is changed. The studied geometries were chosen to cover the range of device areas allowed in this technology. The V_{th} of each device was obtained from the devices Id-Vg curves (V_D = 100 mV), by applying the constant current (CC) method, where the constant drain current of 10^{-7} A x W / L was chosen to determine Vth.

	Experimental device dimensions W/L (nm)							
DUTs	592	16	16	16	36	36	36	36
W	80	200	600	800	1000	1000	1000	1000
L	60	60	60	60	60	100	500	1000

Table I: Number of devices experimentally analyzed for each type (nMOS and pMOS) and W and L values used for the V_{th} variability study.

According to Pelgrom's rule, the V_{th} standard deviation, $\sigma(V_{th})$, depends inversely on the square root of the device area, equation (1), where A_{Vth} parameter is related to the device technology. For fixed values of L (L_{cte}) or W (W_{cte}), eq. (1) can be written as eq. (2) or eq. (3), respectively.

$$\sigma(V_{th}) = \frac{A_{Vth}}{\sqrt{W \cdot L}} \quad (1)$$

$$\sigma(V_{th}) \cdot \sqrt{L_{cte}} = \frac{A_{Vth|L_{cte}}}{\sqrt{W}} \quad (2)$$

$$\sigma(V_{th}) \cdot \sqrt{W_{cte}} = \frac{A_{Vth|W_cte}}{\sqrt{L}} \quad (3)$$

Fig 1 shows the $\sigma(V_{th})$ fitting (lines) of the experimental data (symbols) to eq (2) and eq (3), when only W (a) or L (b) is varied, for n- (black) and p- (red) MOSFETs. Note that different slopes, $\Delta V_{th}|L_{cte}$ and $\Delta V_{th}|W_{cte}$, are observed (Table II). These results point out that the coefficient AVth in eq(1) must be changed suggesting a deviation from the Pelgrom's rule [4]. This result is observed for both nMOS and pMOS devices, being the effects more important in nMOS transistors. Therefore, the different slopes indicate that to correctly take into account the variability dependence on device area, different dependences of $\sigma(V_{th})$ on W and L should be considered.

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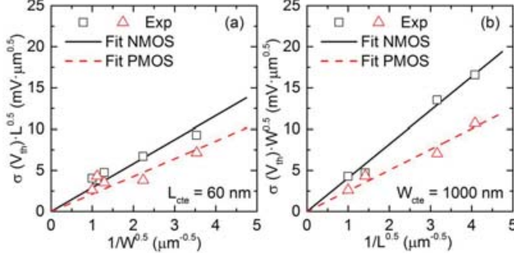

Fig. 1. Experimental σV_{th} (dots) as a function of $1/W^{0.5}$ (a) and $1/L^{0.5}$ (b). The lines correspond to linear fittings, with slopes in Table II.

	$A_{Vth\|L}$	$A_{Vth\|W}$
nMOS	$2.906 \cdot 10^6$ (mV · μm)	$4.088 \cdot 10^6$ (mV · μm)
pMOS	$2.138 \cdot 10^6$ (mV · μm)	$2.517 \cdot 10^6$ (mV · μm)

Table II: Slopes of the linear fittings of the data in Figure 1, to equations (2) and (3).

III. SIMULATION PROCEDURE

To elucidate the physical origin of the difference observed in the slopes of Fig. 1 and, therefore, the deviations of the Pelgrom's rule, TCAD simulations were performed with ATLAS Silvaco simulator.

First, a nMOSFET structure was defined in the TCAD tool using Gaussian and Exponential doping profiles [6] and an EOT = 2 nm. The models used in all simulations were: the Lombardi model (CVT) for carrier mobility, the Shockley-Read-Hall (SRH) model for recombination, and the Fermi-Dirac model for the carrier statistics. Fig. 2 shows the net doping profile and the dimensions of the simulated device. Several devices with different W and L were considered. Table III shows the 4 selected values of L and W, which were combined to simulate 16 different areas.

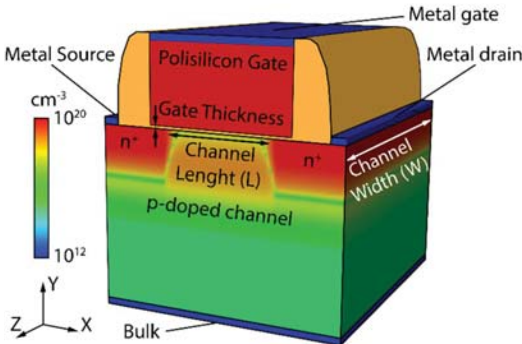

Fig.2 MOSFET simulated structure showing the net doping profiles. The main device dimensions have been plotted.

Once the I_DV_G device characteristics can be simulated, the V_{th} variability was introduced in the simulations. Since one of the main sources of device-to-device V_{th} variability is associated to the presence of Discrete Fixed Charges (DFC) in the oxide or at the interface [5], the impact on V_{th} of random distributions of these charges in the gate dielectric was evaluated. To do this, TCAD simulations were performed by locally introducing interfacial charges ($1e^-$) at the gate oxide/channel interface [7] of devices with different geometries. In order to reproduce the variability typically observed in the experimental data, the average of DFC (<N>) introduced in the smallest device (50x50 nm) was fixed to <N> = 9. The average DFC in larger devices was scaled with area. In this way, the average interfacial charge density (D_{it} = <N> / (W·L)) is kept constant in all the devices, with value $3.6 \cdot 10^{11}$ cm^{-2}. For devices with the same area, the number of defects per device (N) is also statistically distributed, the N associated to each particular device was obtained from the generation of random numbers that follow a Poisson distribution with mean value <N> [8]. Each of the fixed charges is randomly located at some position of the device interface.

	Simulated device dimensions W/L (nm)			
W	50	80	100	200
L	50	80	100	120

Table III: L and W values considered for the V_{th} variability study. A total of 16 areas was simulated.

Fig. 3 shows, as an example, a current density map calculated at the oxide/semiconductor interface of a device L/W=80/200 nm in which N = 58 fixed charges (black points) were introduced. The applied bias were V_D = 0.1 V and V_G = 0.50 V, being the last value close to the average V_{th} measured for this geometry. As it can be observed, the current density decreases near the DFCs. In some cases, the high population of traps located in small regions of the device interface blocks the current density in this area and originates percolative paths through the device [7]. The fact that for each device a different DFC random distribution (in number and localization) is considered, leads to a variability of V_{th}, which will be analyzed in the following.

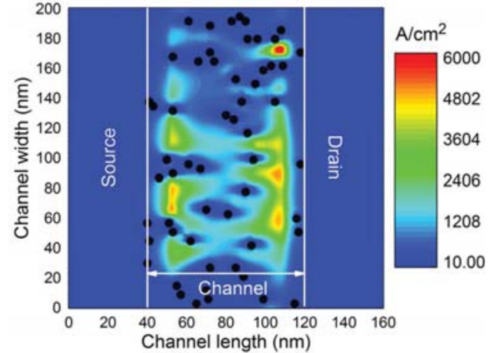

Fig. 3 Current density map at the oxide/semiconductor interface when 58 DFC were randomly located. The biases applied were; V_D = 0.1 V and V_G = 0.50 V.

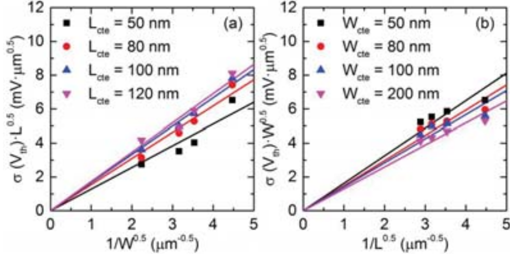

Fig. 4 Simulated $\sigma(V_{th})$ (symbols) as a function of $1/W^{0.5}$ (a) and $1/L^{0.5}$ (b). The lines correspond to linear fittings.

Fig. 4 shows the dependence of the V_{th} variability as a function of $1/W^{0.5}$ (a) and $1/L^{0.5}$ (b), for simulated devices with different L and W, respectively. As it can be seen, by changing the device dimensions, the slopes are modified with different dependences. These results suggest that the statistical distribution of charges in the device leads to the V_{th} variability and to deviations of Pelgrom's rule as those observed experimentally in Fig. 1. Of course other variability sources also contribute to this effect.

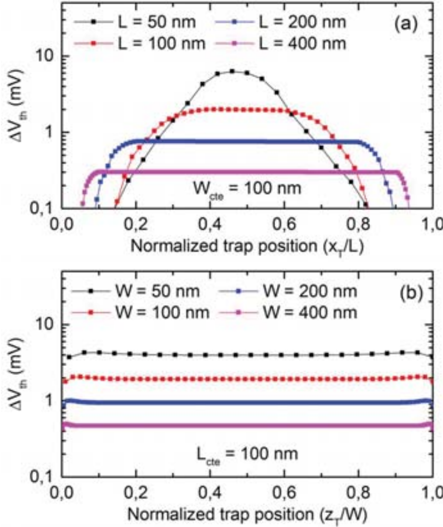

Fig. 5 TCAD simulation of the change in the device V_{th} (ΔV_{th}) when a DFC is swept along the channel length (a) and width (b) of the device. Devices with several dimensions are considered, so that the normalized trap location is plotted in the x-axis.

Once the random charge distribution in the oxide has been demonstrated to be a Vth variability source, which leads to deviations from the Pelgrom's rule, further simulations have been performed to elucidate the possible origin of such asymmetry in the L and W dependences. To do this, and for simplicity, one DFC was swept along the channel length and width of the device and its impact on the Vth was evaluated. Fig. 5 shows TCAD simulations of the change in the device V_{th} (ΔV_{th}) when a DFC is swept along L (a) and W (b) of the device.

Devices with several geometries are considered, so that the normalized trap location is plotted in the x-axis. It can be seen that the impact of the DFC on V_{th} depends on the charge position along the channel (especially for shorter devices, black and red curves in Fig.3a) while V_{th} has essentially a constant value when the DFC is swept along W. This asymmetry in the V_{th} impact, depending on the trap location along W or L, has been assumed to be the root of the differences observed in Fig 1.

IV EMPIRICAL MODEL

Since Vth variability for small enough devices seems not to follow Pelgrom's rule, for a better fitting of the data, the dependences of V_{th} variability on W and L have been decoupled, proposing equation (4) to describe the V_{th} variability. In this expression α and β are free fitting parameters that are used to take into account the different dependences of $\sigma(V_{th})$ on L and W.

$$\sigma(V_{th}) = \frac{B_{Vth}}{W^{\alpha} \cdot L^{\beta}} \quad (4)$$

With the aim of comparing the goodness of our model and Pelgrom's law, in Fig 6 the fittings of Vth variability obtained experimentally in nMOS (Fig. 6a/6b) and pMOS (Fig. 6c/6d) to Pelgrom's rule (a, c) and to our model (b, d) are shown. As it can be observed, for all devices, the proposed model reproduces better the data.

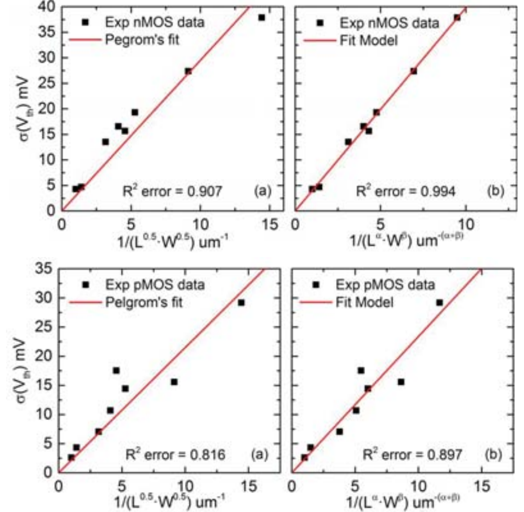

Fig. 6 Comparison between the fittings the Pelgrom's law (a, c) and the proposed equation (4).

To compare quantitatively the fittings, the α, β, A_{Vth}, B_{Vth} and R-square coefficients parameters were calculated (see Table IV). For both cases (nMOS and pMOS), the error obtained using the proposed model is lower than that obtained with the Pelgrom's law. Note that the new incorporated coefficients, α and β, could depend on the technology.

	Fit parameters				R-square	
	α	β	A_{Vth}	B_{Vth}	Eq (1)	Eq (4)
unit	-	-	mV·µm	mV·µm$^{(\alpha+\beta)}$	-	-
nMOS	0.342	0.493	$2.95 \cdot 10^{6}$	$4.03 \cdot 10^{5}$	0.907	0.994
pMOS	0.329	0.578	$2.15 \cdot 10^{6}$	$3.89 \cdot 10^{5}$	0.816	0.897

Table IV: Slopes of the fittings of the experimental data in Fig. 1 to equations (1) and (4).

IV. CONCLUSIONS

Our experimental results, as other works, point out a deviation from Pelgrom's scaling rule of V_{th} variability, especially in scaled technologies. In order to clarify the origin of this deviation, TCAD simulations have been performed to evaluate the impact of random distribution of DFC on the device V_{th}. The results show that this source of variability leads to deviations from Pelgrom's rule, which could be related to the different impact on V_{th} of charges depending on their location along W and L. Taking this into account, an empirical equation is proposed to fit the data, in which two parameters are introduced to separately account for the W and L dependences. With the proposed equation, better fits of the experimental data are obtained in the analyzed area range.

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