Universitat Autònoma de Barcelona

Implementation of unsupervised learning mechanisms on OxRAM devices for neuromorphic computing applications

Marta Pedró Puig

Universitat Autònoma de Barcelona

Escola d'Enginyeria

Electronic Engineering Department

Implementation of unsupervised learning mechanisms on OxRAM devices for neuromorphic computing applications

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Supervised by Dr. Javier Martín Martínez
and Dr. Montserrat Nafría Maqueda

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The undersigned,

Dr. Javier Martín Martínez, *Associate Professor*, and Dr. Montserrat Nafría Maqueda, *Full Professor*, of the *Electronic Engineering Department* of the *Universitat Autònoma de Barcelona*

CERTIFY

That the thesis entitled "*Implementation of unsupervised learning mechanisms on OxRAM devices for neuromorphic computing applications*" has been developed by the Ph. D. candidate **Marta Pedró Puig** under their supervision, in fulfillment of the requirements for the PhD degree of Electrical and Telecommunication Engineering.

And hereby to acknowledge the above, they sign the present:

Dr. Javier Martín Martínez

Dr. Montserrat Nafría Maqueda

Marta Pedró Puig

Bellaterra (Cerdanyola del Vallés), July 2019

"Look deep into nature,
and then you will understand everything better."

A. Einstein

Acknowledgments

"The flow of time is always cruel. Its speed seems different for each person, but no one can change it". It was a long time ago when I first read this quote, but never truly understood its meaning until I began researching. Three years ago, I officially started the work related to this thesis dissertation. I sometimes wanted time to flow faster, and sometimes I wanted it to stop. When deadlines are approaching, days are dark and full of terrors. However, we always end laughing at them. Indeed, I have learned so much from this thesis, but the most important things come from the people who have surrounded me during these years. The following lines are dedicated to all of you.

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To my Ph.D. and post-doc colleagues at UAB, specially to who I shared office and lunch-time with, together with so many happy and geeky moments. Thank you for always making my day, no matter how cloudy it was to me. To my closest friends I have shared these earlier researcher years with: Guille, Alba, Alex, Alicia and Julia. Despite I am submitting the present thesis dissertation, I am afraid I will never stop talking about neurons or electronics. I owe you so many coffees, beers and glasses of wine for that. Thank you for your understanding and for always believing in me.

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Contents

Preface

The exponential growth of electronics computing power over the past decades has brought about profound changes in almost every aspect of our society: from communications to data resource management, health and transport. This impact had been largely pushed forward by researchers from the solid-state physics field, focused on the improvement of the scalability of electronic devices, aiming to increase the power density per unit area of an integrated circuit. This interest does not only belong to the scientific community but also to the companies of the semiconductor industry, which provide financial support for the research and development of high performance computing platforms, concerning the maintenance of the exponential growth rate predicted by Moore's law [1, 2]. Moreover, these companies must guarantee the cost-effectiveness of their products while keeping them affordable for their target audience. This trade-off applies specially to smart mobile devices and multimedia platforms, since they have become a key part of the daily life of their users. Thus, there is an urgent demand for electronic systems that can achieve high-performance computing and handle large amounts of data with low power consumption [3].

The difficulty of overcoming the disparity between processor speeds and data access speeds leads to a limitation on throughput, caused by the standard Von Neumann computer architecture, which involves separate memory and processor units [4]. Therefore, maintaining the growth trend predicted by Moore's law implies facing significant challenges at the practical level, which are related to the non-idealities of electronic devices, power consumption limitations or parallel processing requirements [3]. The recent progress in the development of new classes of nanodevices enabled the re-emergence of alternative approaches to the von Neumann model, such as bio-inspired architectures, also referred to as neuromorphic systems. This field of research aims to build cognitive adaptive solid-state devices that emulate the computation performed by the brain, and because of their structure and physical properties, these devices have the ability to mimic its energy-efficient, parallel and fault-tolerant computation [5]. Specifically, two-terminal resistive switching devices (memristive devices) made it possible to prove such key properties, which are local adaptive learning and large connectivity, that turned them to be well suited for neuromorphic applications [6].

Neuromorphic engineering is a concept developed by Carver Mead in the late '80s [5]. It is a multidisciplinar field that takes inspiration from neuroscience, mathematics, computer science and electronic engineering to design artificial neural systems for high-performance computing applications, in which pattern recognition tasks play a major role, such as computer vision, auditory processors or autonomous robots. A broadened definition for neuromorphic engineering proposed by C. Diorio [7] is: "reverse engineering the information representation used by neurobiology, and developing artificial systems that employ these representations in their operation". Biological brains and digital computers are the only two successful computing machines that nowadays we know about. Both are physical machines that compute using physical processes, consuming energy to manipulate or destroy information. The first difference found between them is the material of origin: computers are built from semiconductors, oxides and metal, and brains are built from hydrocarbons and aqueous solutions. The second difference is the way they represent information, yet both use physical quantities: computers use electrical signals, which are transmitted on metallic wires (Figure 1) and avoid noise by using a digital representation; while brains use electrochemical signals transmitted on neural wires or via chemical solutions (Figure 2), which are limited by noise. However, the

significant variability found in the biological brain is considered as a potential basis for learning [8].

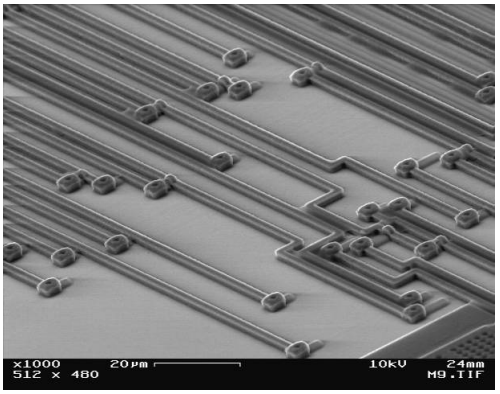

Figure 1: Wires ending in interconnects from an Intel Pentium processor, produced in 1992. Image credits: Alex Pisarski, The Institute of Optics, The University of Rochester [9].

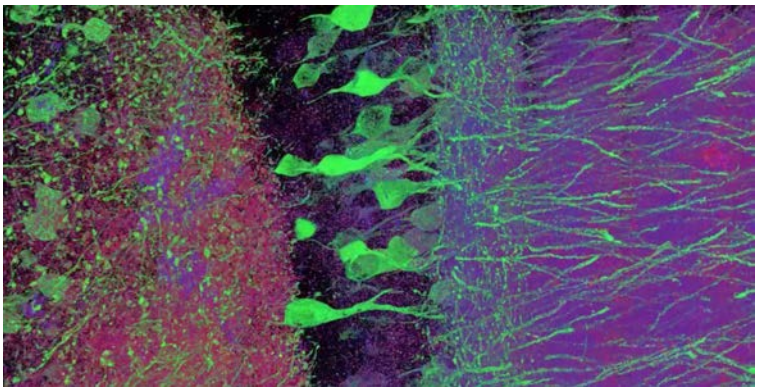

Figure 2: Neurons in the hippocampus expressing Yellow Fluorescent Protein, spanning a large volume relevant to neural circuitry. Image credits: Ed Boyden, Paul Tillberg, Fei Chen [10].

These differences do not completely explain the reason why brains can solve problems involving speech understanding, recognition, association and learning tasks with such low power consumption, efficiency, parallelism and fault-tolerance operation. Performing these tasks with a computer implies not only precisely specified inputs, which are not found in natural, real-time changing environments, but a energy and space trade-off: most attempts at replicating a biological brain for emulating neuronal computation involved simulating a very large number of neurons on a high-performance computer.

As an example of an artificial cognitive platform, IBM built a question answering (QA) computing system to apply advanced natural language processing, information retrieval, knowledge representation, automated reasoning, and machine learning technologies to the field of open domain question answering. This supercomputer had access to 200 million pages of structured and unstructured content consuming four terabytes of disk storage. The key difference between QA technology and document search is that document search takes a keyword query and returns a list of documents, ranked in order of relevance to the query (often based on popularity and page ranking), while QA technology takes a question expressed in natural language, seeks to understand it in much greater detail, and returns a precise answer to the question. According to IBM, more than 100 different techniques are used to analyze natural language, identify sources, find and generate hypotheses,

find and score evidence, and merge and rank hypotheses [11].

In 2011, a comparison between human brains perfomance and Watson was carried out for computational tasks involving mainly voice recognition, natural language processing, information retrieval and machine learning. The supercomputer won the contest with an advantage of almost 40-fold difference in reaction time. But the main points, which were missing in this comparison, were the energy consumption and physical sizes of the computational systems: Watson employed a cluster of ninety IBM Power 750 servers, each of which uses a 3.5 GHz eight core processor, with four threads per core. In total, the system had 2.880 processor threads and 16 terabytes of RAM, and required 80kW of power and 20 tones of air-conditioned cooling capacity, occupying a total volume worth 10 refrigerators [11], while human brain has a volume up to 1400cm^3 and a estimated power consumption of 10W [12]. Definitely, the conventional computing paradigm based on CMOS logic and the von Neumann architecture is ideal for solving structured problems and well-defined mathematical problems with precisely defined data sets, with such performance and speed that are not comparable to the achieved by a human brain. However, for real-time processing of unstructured sensory data the brain outperforms computers, considering the physical feasibility and cost of an artificial computing system with equivalent computing attributes.

Summarizing, both computers and brains are each efficient at computing in their respective domains but are not well suited for the other. Biology uses physical phenomena as primitives for adaptation and learning, and computers use multipliers and adders as primitives to perform mathematics. Both are efficient at computing in their respective domains, but are not well suited for the other domain: neurons are terrible at math, and multipliers and adders are poor choices for adaptation and learning, as a consequence of their underlying information representation [7]. The basis of the neuromorphic engineering (Figure 3) consists in this idea: an alternative approach for achieving a learning-based computing paradigm could consist in using semiconductor physics as a primitive, and use the model provided by neuroscience. Hence, there is a need to know how nerve tissue represents, communicates and processes information: a need to understand the biology primitives.

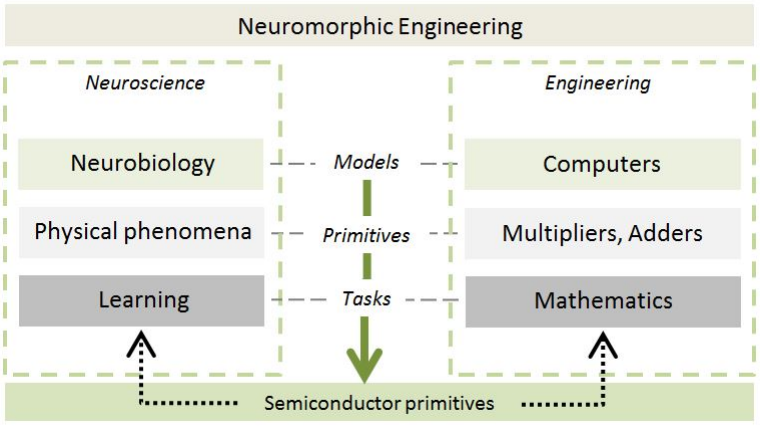

Figure 3: The neuromorphic engineering concept.

This is the reason why the neuromorphic computing term nowadays represents a wider concept that links computing systems and neural systems in both directions: the original concept was essentially concerned with the construction of electronic systems using existing technologies, in order to emulate the behavior of some regions of the brain and reproducing neurophysiological phenomena to increase our understanding of nervous systems, mostly for brain simulation purposes [13, 14, 15].

The objective of understanding the architecture of brain and mind is recognized as one of the grand challenges in computing research and is a long-term multi-disciplinary project pursued at many different levels of abstraction [16]. This traditional view of neuromorphic computing is still the most widely accepted one in the domain of neuroscience and neural computing [17]. From the engineering point of view, consists in an effort to overcome the limitations of current technologies (in terms of energy per operation and area), using a sub-set of neuronal properties to build neuron-like computing hardware, with the purpose of achieving the computational capabilities of such systems with similar volume and energy efficiency [12, 18].

According to [19], one of the challenges in neuromorphic engineering is to realize a connectivity of 10^4 synapses per neuron, which is the characteristic of the mammalian brain, in order to reach its level of computing performance. Unfortunately, even with the exponential transistor density growth nowadays, it is not sufficient to realize such massive connectivity in traditional CMOS processes. For the implementation of the connections between neurons, i.e. the synapses, the emerging non-volatile memory devices have been widely studied during the last years [20, 21, 22], popularly referred to as memristors [23]. The fine-tuning of the device resistance with memory effects is the key enabling factor of memristor-based neuromorphic circuits [18, 24, 21]. The conductance tuning in memristors can be thought as being *analogous* to the plastic synaptic weight changes in biological synapses, so memristors can be used to emulate biological learning mechanisms. Moreover, the large connectivity that can be offered by nano-scaled memristors make them well suited for physical implementation of synaptic functions in neuromorphic circuits [24, 20, 25, 26, 27].

Within the variety of memristive devices, oxide-based Resistive Random-Acces Memory (OxRAM) technology seems to suit best the requirements for the implementation of an electronic synapse, which are relatively lower energy consumption and compatibility with CMOS technology [28]. OxRAM technology offers the possibility to implement analog and binary electronic synapses, where the conductivity of the device is identified as the synaptic weight. In analog synapses, the synaptic weight can be set within a continuous range, and thus its electrical implementation requires the continuous control of the conductivity of the device. Moreover, the linearity and symmetry of the conductivity change, in both directions (to be increased or decreased), with respect to the control parameter (such as voltage or current), is desirable for optimizing the neuromorphic system performance [18]. These requirements suppose a challenge to be overcome, due to many properties of the OxRAM devices such as its intrinsic variability, non-linearity of the conductivity change with respect to the control parameter (voltage), the stochasticity of the conductivity change (specially when it is meant to be decreased) and the asymmetry in its typical I-V characteristics. On the other hand, binary synapses present only two states (e.g. the synapse is active or not), and are based on the comparison between the synaptic weight and a predefined threshold. Concerning its electronic implementation, binary synapses do not require the capability of fine-tuning the conductivity of the device and offer a greater tolerance to the intrinsic device variability. On the other hand, the performance of the neuromorphic system is diminished if compared with the one found in an analog-synapse-based system, assuming an equal number of neurons and synapses. Hence, for reaching a similar performance and accuracy, the area of the system and its power consumption has to be increased [29, 30]. The key challenge to be overcome in any of the two cases consists in developing an understanding of the physical mechanisms governing the switching of the OxRAM devices. There are two main near-term goals: the first is to decrease the power consumption required to program such devices, by means of progressing in the physical mechanisms understanding and the devices materials and manufacturing. The second is related to the development of new programming schemes oriented to mitigate the non-linearity, asymmetry and variability of the conductivity update process, whose effects increase when scaling-down such devices in terms of area, or when operated in low power consumption modes [31, 30, 29].

Because of the advantages that OxRAM offers, recent approaches to address the challenge have been to integrate CMOS with OxRAM nanotechnology to achieve the required synaptic densities. These solutions use **crossbar** architectures predominantly, but the connectivity challenge

still remains a daunting task for such solutions. According to [28], CMOS compatibility is desirable because the neurons can be easily implemented by CMOS circuits for emulating the action potential pulses. For example, in [19] a CMOS technology was adopted for emulating all neural and synaptic computations, and memristor (OxRAM) technology for high-density analog storage. Moreover, there is an analogy between a biological neural system and its artificial counterpart in a crossbar architecture: the cross-point array with a memristive-synaptic device at the junctions. Interestingly, the biological synapse changes its conductance by exchanging Ca_{2+} or Na_{+} ions between the membrane and the synaptic junction when the spike stimulus arrives, while the OxRAM synaptic device changes its conductance by migration of the oxygen ion/vacancies when the programming pulse is applied. In [28], it was experimentally reported an oxide-based resistive switching electronic synaptic device with sub-pJ energy per spike, having characteristics that are substantially improved over previously reported synaptic devices based on other technologies, in terms of energy consumption. Hundreds of resistance states were gradually modulated by using identical pulses, and the capability of using pulse number to control the resistance would greatly simplify the neuron circuit design. Furthermore, this gradual behavior was found to be useful for adaptive learning in the presence of device variability. With the rapid progress of oxide-based resistive switching memory technology (down to 10nm cell size [32], up to Mb array size [33], and 10^{12} endurance cycles [34][35]), the envision of a large-scale neuromorphic system using OxRAM devices as electronic synapses is conceived to be feasible in the near future [3].

Other challenges to be overcome by the neuromorphic engineering community are related to the development of the hardware-versions of learning algorithms to be implement in hardware neural networks (i.e. neuromorphic systems), in order to provide such systems with artificial intelligence. The artificial intelligence research is defined as the study of intelligent agents, which could be any device that perceives its environment and takes actions that maximize its chance of successfully achieving its goals. The learning algorithm is the method used in an intelligent system (such as an artificial neural network) as to *train* it to some input data, in order to extract patterns appropriate for application in a new situation, adapting the system to a specific input-output transformation task. Once *trained*, the system is able to perform a specific task without using explicit instructions, relying on the learned patterns and inference processes. The learning algorithms have been studied and implemented in software for many decades for artificial intelligence tasks, such as data classification and computer vision. Nowadays, their application has been extended to intelligent Internet-of-Things devices and Big Data analysis methods and systems [3], because artificial intelligence permits the execution of data mining and data prediction tasks in an efficient way. An intelligent system can learn on real-time (i.e. on-line learning capability) and adapt to the changes occurring in the actual input data set, being a promising solution for real-time decision-making tasks, such as self-driving vehicles (drones, cars, etc.).

Learning algorithms can be classified according to the type of data used as the input data set, the data that the system generates as an output, being their learning approach one of the following: *supervised* or *unsupervised*. On one hand, supervised learning algorithms build a mathematical model of a data set, which contains the inputs and the desired outputs of the system. This data set is referred to as the training data. Each training example is represented by an array, and through the iterative optimization of an objective function (e.g. cost function), the system learns a function that can be used to predict the output related to new inputs, never seen by the system before. In the case of a neural network, it must be able to compute the error performed in each of the training examples, and update its synaptic weights in order to diminish it over time. Examples of application of supervised learning algorithms are classification tasks such as visual identification, identity tracking or prediction of the evolution of financial data. On the other hand, unsupervised learning algorithms rely on a data set which only contains the inputs of the system. Hence, the data used for the training has not been labeled, classified or categorized. The learning algorithm permits the system to identify the similarities between the features of a training example, and to react based on the presence of absence of these similarities in each new training example. An example of application of unsupervised learning is the cluster analysis, which consists in the assignment of a set of observations into clusters, so that observations within the same cluster are

similar in terms of a predesignated criteria or feature, whereas observations from different clusters are dissimilar.

The present thesis is focused on the implementation of reliable neuromorphic systems, based on memristive devices, working as analog or digital synapses. In particular, the OxRAM technology is the object of study of this thesis, being one of the most promising candidates for the implementation of a reliable electronic synapse. Following a bottom-up approach, this thesis dissertation begins parting from the device-level perspective. The first chapter is dedicated to the memristor concept and to the resistive switching devices, as to provide the theoretical foundations for understanding the experimental results exposed in the thesis. After a brief introduction to the memristor, the to-date available memristive technologies are exposed and compared in terms of their figures of merit, focusing in the state-of-the-art electronic synapse implementation. The key research issues and challenges for these technologies are finally indicated according to the 2018 IRDS [3].

After the introductory chapter, the devices to be investigated are presented. The following two chapters are related to the electrical characterization and modeling of the tested samples, with the objective of verifying if they are suitable for analog synaptic applications. In particular, chapter 2 covers the static and dynamic electrical characterization methods, which were performed in order to evaluate the dependence of the conductance state of the devices under different electrical stimuli and test parameters. A time-independent model of the experimental G-V characteristics is finally exposed at the end of this chapter. The model has been widely used during the execution of this thesis. Parting from the results of chapter 2, two biorrealistic learning rules are demonstrated experimentally with the available OxRAM devices in chapter 3. The aim of this part of the research consists in studying the learning mechanisms that can be implemented in the tested devices, by means of playing with the conductance dependence of the devices on the voltage drop applied to them. The experimental results from this chapter are used to verify the goodness of the G-V characteristics model.

The two studied learning mechanisms in chapter 3 are the basis for adapting the software version of a popular bio-inspired unsupervised learning algorithm to a hardware architecture. The original learning algorithm to be adapted consists in achieving the specialization of regions of a neural network to different features of the data shown to the network, by means of obtaining a spatially-distributed, topographical representation of these features. In chapter 4, a hardware-friendly version of this learning algorithm, to be implemented in a feasible neuromorphic system based on the tested OxRAM devices, is presented. The G-V characteristics model of the tested technology is used to test the proposed learning algorithm in a OxRAM-based neuromorphic array through simulation. The objective of chapter 4 consists in checking if the proposed learning algorithm provides the neuromorphic system with the self-organizing property, permitting to spatially distribute the input data set features in a topographical manner. After the details of the learning algorithm are given, a fundamental application of the self-organizing algorithm is demonstrated by means of simulation. This application is also used for checking the impact of different levels of cycle-to-cycle variability on the performance of the neuromorphic system. This study pretends to verify if the proposed neuromorphic system is tolerant to noise and synaptic variability, as its software-version is. Finally, a multi-layer hierarchical computing system is proposed, as a new concept for achieving complex computing tasks related to associative learning mechanisms.

The last chapter of the present thesis dissertation, chapter 5, is dedicated to the results obtained during an internship of 3 months carried out at IMEC (Leuven, Belgium). Chapter 5 also follows a bottom-up approach, and compiles the OxRAM devices electrical characterization and modeling results when operating in low-current mode. In this case, the OxRAM devices application to binary stochastic synapses is studied. Concluding this chapter, a temporal-sequence learning algorithm is simulated, which is compared with the self-organizing algorithm proposed in chapter 4. Finally, the conclusions stating the main results of the research are included. The publications related to this research are also included at the end of the manuscript.

Chapter 1

Memristors as electronic synapses

1 Introduction

Advances in neuromorphic engineering during the last years have been possible due to the combination of progresses made in two different research fields: neuroscience, through experimental and modeling studies; and nanotechnology, involving the emergence of new classes of nanodevices [36]. Two major challenges have to be overcome concerning the implementation of a basic neuromorphic computing cell: neurons with extremely low energy consumption [12] and reliable electronic synapses. Although the neuron design still has to face important challenges to match the neurons density and functionality required for neuromorphic circuits, it is worth highlighting that the most abundant element in a neural network is the synapse [21]. In order to properly train the neural network by means of executing a learning algorithm, which has the objective of modifying the synapses characteristics, a reliable synaptic behavior is required.

The desired properties for an electronic synapse include non-volatile programmable conductance, low-power consumption, high endurance and high integration capability, being preferably a two-terminal nanoscaled device with CMOS process compatibility. Since 2008, the emerging nano-scaled devices which were initially investigated for non-volatile memory applications have been considered for this purpose, among other applications, such as logic or security. Hence, a better understanding of these devices has been achieved through extensive electrical and material characterizations and modeling [12]. These devices were then identified as memristive devices, since they electrical properties matched the ones of the fourth missing circuit element predicted by Leon Chua in the decade of the seventies, the memristor.

This chapter is dedicated to the memristive devices, as to provide the necessary details required for understanding their application as electronic synapses. First of all, the memristor concept and its origin are introduced. Next, the main resistive switching mechanisms, which provide the above mentioned emerging nano-scaled devices with the memristive behavior, are briefly described. The different technologies which have been proved to be good candidates for the implementation of electronic synapses are then compared in terms of reliability, including their variability, stability and drift, retention and durability. Lastly, the state-of-the-art of the memristor-based neuromorphic computing research is summarized, where a comparison of the main memristive technologies that are being currently investigated is provided.

2 The memristor concept

Memristor is a contraction of *memory resistor*, because that is exactly its function: to remember its history. Conceptually, a memristor is a two-terminal device whose conductivity depends on the magnitude and polarity of the voltage applied to it, and the length of time that voltage has been applied [20], and because of its ability to store its conductivity state, a memristor can be used as a non-volatile memory.

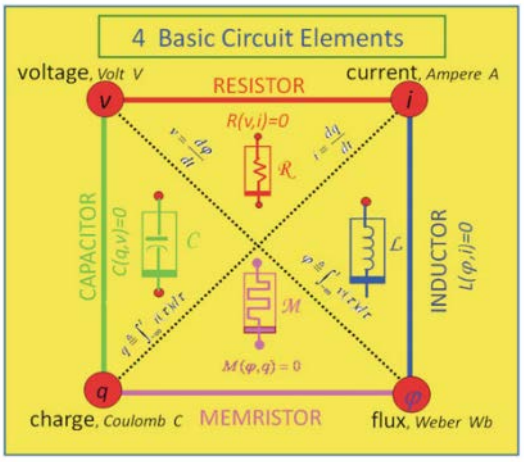

Figure 1.1: The four axiomatically defined passive circuit elements.

The origin of the memristor concept dates back to 1971, when Leon Chua demonstrated via axiomatic definition that an hypothetical passive device would provide the missing axiomatic relationship between flux and charge. Since its behavior could not be duplicated by any circuit built using only the other known three elements, Chua proved that this device would a truly fundamental passive circuit element [37]. The justification provided by Chua was based on the fact that the fundamental passive circuit elements were back then limited to the capacitor (1745), the resistor (1827), and the inductor (1831). According to Chua, these fundamental electrical elements can be thought as conceptual abstractions that are used in the analysis of electrical networks. Hence, the resistors, capacitors, and inductors can be defined axiomatically, via a constitutive relations between a pair of variables chosen from v,i,q,φ, which are identified as the voltage $v(t)$, current $i(t)$, flux $\varphi(t)$ and charge $q(t)$. The basic circuit elements, including the memristor, alongside their constitutive relationships are indicated in Figure 1.1. There are six different pairs that can be formed from these four state variables, namely: (v,φ), (i,q), (v,i), (v,q), (i,φ) and (φ, q).

The first two pairs (v,φ) and (i,q) are not considered constitutive relations because they cannot predict the corresponding current $i(t)$ and voltage $v(t)$, but are related via the equations (1.1) and (1.3), corresponding to the fourth and fifth pairs:

$$\varphi(t) = \int_{-\infty}^{t} v(\tau)d\tau = q_0 + \int_{t_0}^{t} v(\tau)d\tau \tag{1.1}$$

Which defines the capacitor, given the relationship between the charge $q(t)$ and $v(t)$, and the slope at any point Q is called the small-signal capacitance C at Q (equation 1.2):

$$q(t) = C(t)v(t) \tag{1.2}$$

and:

$$q(t) = \int_{-\infty}^{t} i(\tau)d\tau = q_0 + \int_{t_0}^{t} i(\tau)d\tau \tag{1.3}$$

Which defines the inductor, given the relationship between the flux φ and the current i, and the slope at any point Q is called the small-signal inductance L at Q (equation 1.4):

$$\varphi(t) = L(t)i(t) \tag{1.4}$$

The third pair defines the resistor, given the relationship between v and i and stated by Ohm's law, where the slope R is the resistance (equation 1.5):

$$v(t) = R(t)i(t) \tag{1.5}$$

The last pair (φ, q) defines yet another constitutive relation, since given any $(\varphi(t), q(t))$, one can recover the corresponding $(v(t), i(t))$ via equations (1.1) and (1.3). For symmetry considerations, it is then necessary to define a fourth circuit element via the constitutive relation between the variables φ and q (equation 1.6):

$$M(q(t)) = \frac{d\varphi(t)/dt}{dq/dt} = \frac{V(t)}{I(t)} \tag{1.6}$$

Where the slope at any point Q is called the small-signal *memristance* M at Q. This fourth circuit element only has any meaning as a time-dependent non-linear element, since as a time-independent linear element it reduces to a regular resistor. According to [20], a memristor is thus defined to be any dynamical electronic circuit element that obeys the following Chua memristor equations 1.7 and 1.8. In these equations, i is an independent input function, and often a function of time. The resistance R is a function of the physical state of the device, which imparts memory to the device, and also possibly the current i, resulting in a non-linear Ohm's law [20]:

$$v = R(x, i)i \tag{1.7}$$

and

$$\frac{dx}{dt} = f(x, i) \tag{1.8}$$

As stated by Chua, the current-voltage characteristic of a memristor displays always a *pinched hysteresis loop* as the one shown in Figure 1.2, if energized by a sinusoidal voltage or current source, with the hysteresis loops collapsing with increasing frequency of the excitation, being this current-voltage behavior the memristor's fingerprint [37]. Hence, all two-terminal non-volatile memory devices which exhibits a pinched hysteresis loop in the I-V plane, for any initial conditions, is a memristive devices. The electronic devices displaying the resistive switching phenomena can be identified as memristors, regardless of the device material and physical operating mechanisms [23].

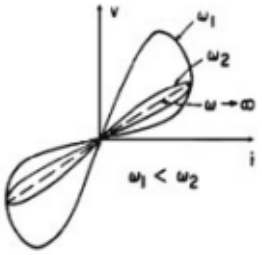

Figure 1.2: Chua's original graph representing the hypothetical memristive behavior.

3 Resistive switching devices for the implementation of electronic synapses

Resistive switching (RS) devices are based on a conductance-changeable material, whose structure often consists in this material, which is usually an insulator in its pristine state, being sandwiched by two metal electrodes. The switching behavior depends strongly on the materials of both insulating layer and electrodes. The RS operation is regarded as a toggling of conductivity states, as a result of electrical stimulus (i.e. the application of a voltage), which is usually thermally-assisted. The switching from a low to a high conductivity state is widely known as the SET process, whereas the reverse process is referred to as the RESET process. The conductivity state is detected by applying a low voltage to the electrodes of the device. Depending on the relationship of the electrical polarity between the SET and RESET voltages, the RS behavior can be classified into the unipolar (Figure 1.3.a) or bipolar (Figure 1.3.b) mode.

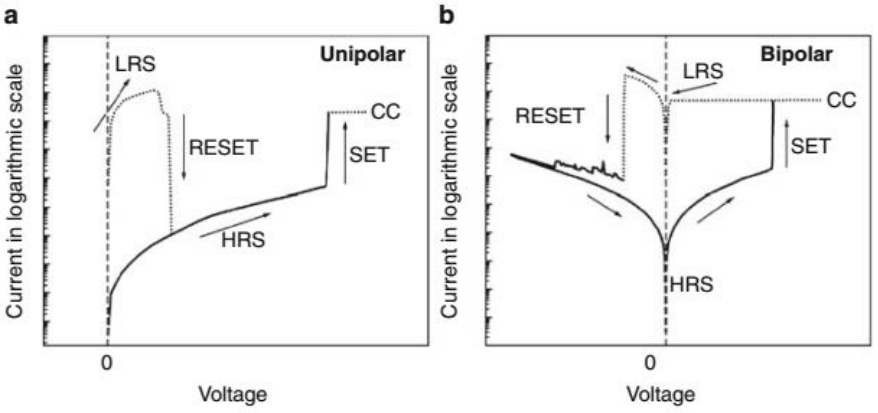

Figure 1.3: Examples of a typical I-V characteristic of an **(a)** unipolar and **(b)** bipolar binary metal oxide RS device.

The RS phenomena have been reported as early as in the 1960s. These devices, now identified as memristors, were extensively studied as the future non-volatile memory (NVM) devices, aiming to replace the Flash memory technology. This was motivated because RS devices can be realized at low cost while promising a low power consumption, and meet all the requirements of a NVM: non-destructive write/read operations at a speed comparable to current logic devices, large retention of its stored value, low power consumption, and integration capability with the current CMOS process [20]. In the neuromorphic computing context, CMOS-based implementations of electronic synapses were the first to be studied, as CMOS is a mature technology in comparison with emerging nano-scaled memristive devices, whose main drawback is their reliability. In the case of CMOS-based technologies, the synaptic weight is stored in analog or digital elements such

as a capacitor, 4-bit SRAM, 8T-SRAM, 1-bit SRAM or SRAM with multiple bits per synapse. However, if bio-realistic functions are meant to be implemented in the neuromorphic system, the size of each synapse circuit is increased, being the area of a single synapse in the order of $100\mu m^2$. Moreover, on one hand, both capacitors and DRAM cells require refresh process, whereas SRAM cells suppose high leakage power. Due to these disadvantages, the emerging memristive devices were considered as candidates for replacing the CMOS-based technology for synaptic applications, among other applications such as non-neuromorphic mem-computing (i.e. logic or security applications). The advantage that these technologies offer is related to the size reduction of the electronic synapse, being a single synapse represented by one or a few memristors, since a single device permits to store an analog synaptic weight. Hence, better scaling and power consumption are expected if a memristive NVM is considered for neuromorphic computing applications.

The various types of switching mechanisms that are responsible for RS phenomena can be broadly categorized into nanoionic effects (including valence change, electrochemical metallization and thermo-chemical), phase change, ferroelectronic or ferromagnetic properties of the materials and nanomechanical effects [20] (Figure 1.4). Devices that fall in the nanoionic cathegory, namely, valence change and thermo-chemical RS mechanisms, are the Resistive Random-Access Memory devices (RRAM), which include Oxide-based RAM (OxRAM) and Conductive-Bridge RAM (CBRAM) devices. The RRAM and the phase change memory (PCM) technologies have been widely studied for the implementation of analog synapses. On the other hand, those devices whose RS mechanism is based on electrochemical metallization (ECRAM), and ferroelectric and ferromagnetic (STT-MRAM) materials are also being investigated recently for synaptic applications. In order to compare all of the above mentioned technologies, first of all, the desired requirements for the implementation of an analog electronic synapse are stated. Then, in the following subsections, the principle of operation and characteristics of these devices are discussed, with special focus on the OxRAM technology. Lastly, a comparison is made in order to conclude this section.

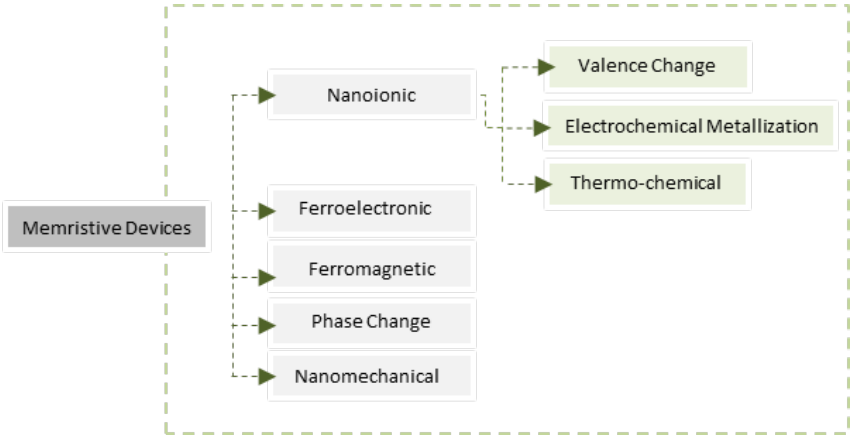

Figure 1.4: Classification of the RS mechanisms in memristive devices.

The electronic synapse operation relies on the possibility to tune the conductivity state of the device, which is identified as the synaptic weight, indicating the strength of the connection between two neurons. The reliability requirements of analog electronic synapses involve the cycle-to-cycle and device-to-device variability, which suppose an impact on the operation of the devices. The quantities of interest to be studied, as to verify if a technology accomplishes the analog synaptic requirements, are the following: the conductivity range (i.e. available window, usually defined as the g_{high}/g_{low} ratio), the number of possible conductivity state levels within this range and the distribution of the conductivity change in both switching directions. Moreover, retention and long-term stability are the properties to be prioritized when inference tasks are considered, once the system has been trained. On the other hand, endurance, short-term stability, a linear dependence of the synaptic weight change on the electrical stimuli and symmetric switching behavior properties

are preferred for the training stage of the neuromorphic network. The symmetric switching behavior refers to the possibility to switch and tune the conductivity state of the synaptic device in both directions (increase and decrease it, which are identified as the synaptic potentiation and depression processes, respectively), by the same amount for the same electrical stimulus (in absolute value). This property, together with the linear synaptic weight updating property, are specially highlighted in the present thesis, because they permit to simplify the design of the system while optimizing the performance of the neuromorphic neural network.

3.1 Resistive Random-Acces Memory (RRAM)

The RRAM technology encompasses CBRAM and OxRAM devices, in which the RS operating principle is based on the creation and destruction of a conducting filament (CF) between two electrodes. The typical RRAM device structure consists on a Metal-Insulator-Metal (MIM), or on a Metal-Insulator-Semiconductor (MIS) structure, in which the insulator is a metal-oxide film in the case of OxRAM devices. CBRAM devices structure consist on a thin solid-state electrolyte layer or a metal-oxide sandwiched between an oxidizable anode and an inert metal cathode.

The CBRAM operation is based on the electrochemical formation of conducting metallic filaments (Figure 1.5). This technology is a promising approach to NMV devices, because it permits high speed switching in the order of nanoseconds, scalability to the nanometer regime, CMOS compatibility and ultra-low power consumption ($\sim$ nW). These devices usually display bipolar switching phenomena (some unipolar cases have been reported), and present a conductivity window larger than the OxRAM window. The SET process is induced by means of applying a positive voltage to the sample. As a consequence, the top electrode is oxidized, the ions migrate to the bottom electrode where they are reduced, creating a metallic filament towards the top electrode. The CF formation is quite abrupt, but its size can be incremented gradually. If the voltage polarity is reversed, the electrochemical dissolution of the CF occurs. However, due to the combination of materials, the resulting states are quite conductive, leading to large currents flowing through the electronic synapses of a neuromorphic array. This implies the use of larger capacitors if integrate-and-fire neurons are meant to be employed. On the other hand, the precise control of the dissolution of the CF through pulsed voltages has still to be overcome. Hence, CBRAM devices are preferred to be employed for the implementation of binary synapses.

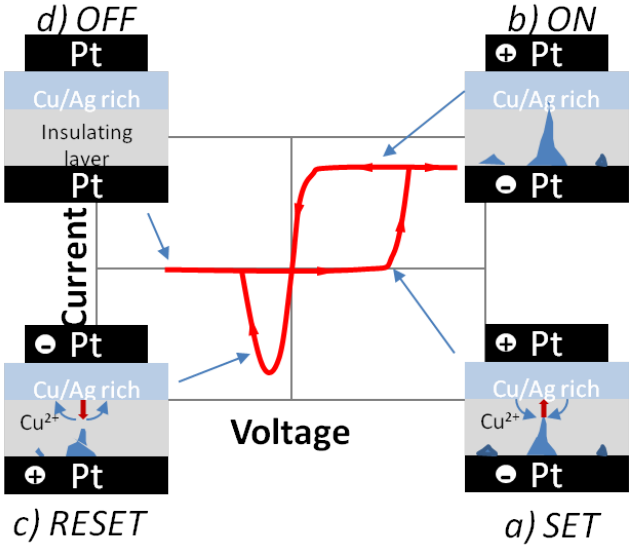

Figure 1.5: An example of the I-V characteristics of a CBRAM device. In each stage, a scheme of the cross-section is depicted, indicating the state of the CF.

On the other hand, OxRAM devices can operate in unipolar or bipolar mode, depending on the combination of materials of the electrodes and the insulating layer. In unipolar OxRAM, the CF formation and rupture processes are due to thermally-assisted redox reactions, where the defects which build the CF are recreated and diffused radially. On the other hand, on bipolar OxRAM devices, the CF modulation is related to ion migration and Joule heating, and it is suggested that the same defects migrate in one direction or the other, depending on the voltage polarity. The differences in the RS mechanism result in the fact that, in general, the bipolar OxRAM devices exhibit a higher endurance, and require less current as to be programmed. Some combinations of materials are more favorable for obtaining symmetrical weight updating, and less abrupt SET and RESET processes, such as the $TiN - Ti - HfO_2 - W$ operating in bipolar mode.

An electroforming stage is first required in order to induce a local redox reaction, which leaves an oxygen-deficient CF in the oxide layer, connecting the two metal electrodes. In these devices, one of the stack layers acts as an oxygen-exchange layer, and the valence-change process is a result of a local stoichiometric change caused by the oxygen ion/vacancies (VO) generation, and the oxygen ion migration to oxygen-exchange layer. By means of accumulating or depleting the oxide layer with VOs, an increase or decrease of the local conductance can be induced, resulting in the modulation of the overall device conductivity. The VOs modulation is achieved by means of applying positive and negative voltage drops to the device, corresponding to the SET and RESET processes. The positive voltage drop required for the induction of the forming process is usually larger than the ones required for inducing the SET and RESET processes respectively, in absolute value. In Figure 1.6.a and Figure 1.6.b, the OxRAM device structure and the CF state related to the high and low conductivity states are depicted, respectively. When RS cycles are induced to the device, the size and shape of the CF is modulated by means of varying the maximum voltage drop applied to the sample (valid for both of the SET and RESET processes), or the maximum current driven by the device during the SET process (the compliance current). These parameters have to be controlled in order to prevent the CF to be overheated, which could result in the irreversible breakdown of the device. The modulation of the CF size and shape permits to induce conductivity changes in both directions (potentiation and depression processes). In Figure 1.6, a scheme illustrating two different situations of the CF is depicted, for **(c)** a high conductivity state, and **(d)** a low conductivity state.

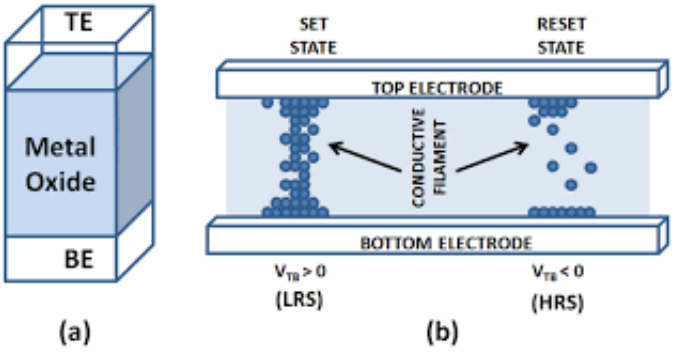

Figure 1.6: Illustration of the conductivity state of a OxRAM device and the state of the CF between its two electrodes, for **(c)** a high conductivity state, and **(d)** a low conductivity state.

The main issue encountered in OxRAM devices is the variability observed in the forming, SET and RESET processes. Literature reports inherent stochastic forming processes, meaning that different voltages have been observed in DC schemes, as well as a wide range of times needed to form the devices at a constant voltage. Large variability is observed also in the voltages related the SET and RESET processes, specially for the latter one. This variability complicates the choice of the operating conditions for OxRAM cells within a neuromorphic array. However, as stated above, neuromorphic systems show high resilience to device (synapse) variability. Since the switching behavior strongly depends on the combination of electrode and insulating layer materials, for a

particular case, the device-to-device and cycle-to-cycle variability impact on the system performance should be individually investigated.

On the other hand, symmetrical and/or linear synaptic weight updating can be achieved with the proper operating conditions, permitting the implementation of analog synapses with OxRAM devices. This is one of the advantages that OxRAM technology offers, in comparison with the other technologies. It has been demonstrated that a 1T-1R configuration, consisting on a transistor and a RRAM stacked, presents a more gradual switching in contrast with the 1R case. Moreover, in a 1T-1R structure, the current flowing through the RRAM device can be modulated by means of controlling the gate voltage of the transistor, so that the size of the CF can be modulated in an analog manner. The transistor also behaves as a device selector when an array is considered. However, a trade-off between symmetric weight updating and the signal-to-noise ratio (SNR) of RRAM devices has been reported, where the SNR indicates the impact of the inherent RRAM variability on the induced conductivity change (the larger the observed SNR, the less susceptible is the conductivity change to the inherent device variability). In general, RRAM technology presents better endurance and scalabity, the required reading voltage, programming energy and time are lower compared to the PCM and STT-MRAM technologies. However, the materials and operating conditions have still to be optimized for improving the RRAM switching characteristics.

3.2 Electrochemical Random-Access Memory (ECRAM)

The ECRAM category is in the early stage of development, and involves those devices in which purely ionic and purely electronic conduction occurs. These devices have three terminals, which are the gate, source and drain regions. On top of a substrate, there is the ion channel communicating the source and the drain terminals. The channel is in contact by a solid-state electrolyte, which is capped by the gate or reservoir terminal (Figure 1.7. The conductivity programming processes are performed by means of applying a voltage to the gate terminal. This voltage drives mobile ions through an electrolyte and into a channel. The current continuity between the ionic and electronic conduction regions is maintained through electrochemical reactions. The conductivity state is proportional to the number of ions transferred to the channel, and is read by applying a voltage across the source terminal.

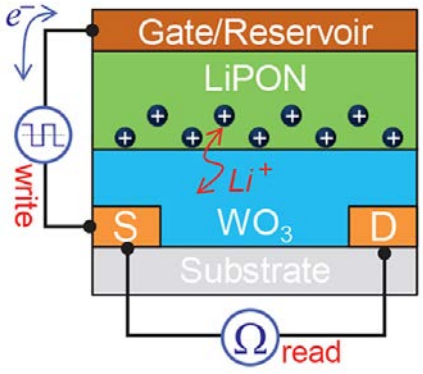

Figure 1.7: Scheme of the cross-section of an ECRAM device.

In these devices, the retention mechanism is based on charge balance. The electrolyte prevents the electrons flowing through the device, whereas an access device prevents them to leakage outside of the device, except for when an updating process is taking place. Therefore, the ions remain fixed. The most common combination of materials consists on $LiCoO_2$ and WO_3 with mobile Li ions, or on a polymer (PEDOT), for which the hydrogen is the mobile ion. In general, ECRAM devices can

contain reactive and mobile elements, such as Li and H ions, and special care with their design has to be taken, in order to avoid them to react with the environment, specially with oxygen. Hence, fabrication and integration of these devices suppose a challenge.

On the other hand, ECRAMs have been scaled down to 100x100nm for their active channel area. The $Li - Wo_3$ devices have been proved to have an endurance of > 1000 cycles and 10^5 pulses, without significant degradation. However, there is still a lack on studies testing their durability under pulse-programming schemes oriented to the implementation of analog synapses.

3.3 Phase Change Memories (PCM)

PCM devices are based on chalcogenide materials, being the most popular employed material the GeSbTe (GST). The switching principle of operation is based on the change of the morphology of such materials, from the amorphous (low conductivity state) to the crystalline (high conductivity state) phases, and viceversa. Since the transitions are thermally assisted, a heater element is required. Typically, the chalcogenide layers are in series with a low resistive contact material (Figure 1.8), which supplies a high current density in order to provide the sufficient energy for inducing the phase transition. These devices show a gradual change of the resistance state in one direction, by means of applying positive voltages. The material starts in an amorphous phase, and can crystallize gradually, increasing its conductivity state (SET process) by means of applying repetitive pulses. In order to perform the reverse process (RESET), a high current pulse is required, as to melt the material and then, reduce quickly the temperature, so that the material quenches, transitioning to a metastable amorphous state. Hence, one of the main drawbacks of this technology is related to the asymmetry of the conductivity change, being the RESET process much more abrupt than the SET process, which is usually gradual.

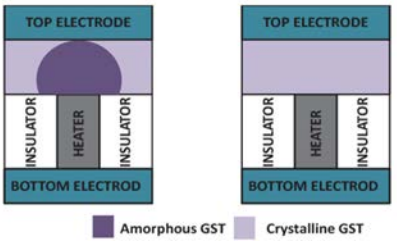

Figure 1.8: Scheme of a PCM device, displaying **(a)** the amorphous and **(b)** crystalline phases.

In order to provide the synapse with both potentiation and depression processes, usually, two PCM samples are employed for implementing a single synapse. The net conductance is then computed as the difference between the conductance of the individual devices. The symmetry of the weight updating process can be achieved if the device presents a gradual linear SET process. Because two devices are involved, their linearity has to match (their SET processes have to present similar slopes), which supposes a challenge, since these devices show significant device-to-device variability. Because the switching process of the PCM technology relies on the crystallization process, this technology displays a stochastic switching behavior.

Relaxation of the programmed resistive state has also been observed. Another disadvantage of the PCM devices for their application as electronic synapses is the resistance drift towards higher values, meaning that the synaptic weight changes over time. This issue only affects to the amorphous phase of the material, whereas its crystalline state is stable, meaning that the PCM could be a good candidate for the implementation of binary synapses. More investigation on the synaptic circuit design based on multiple PCM devices, and on its materials, has to be carried out for implementing reliable analog synapses.

3.4 Ferroelectric and ferromagnetic materials (FeFET, Fe-FTJ and STT-MRAM)

Ferroelectric transistors, FeFETs, had been considered for synaptic applications as early as in the nineties, mainly because in contrast with regular logic transistors, they present the NVM property. In these transistors, until recently based on $Pb(Zr, Ti)O_3$ (PZT) films, the threshold voltage and the drain current is controlled by the ferroelectric polarization state of the dielectric, and can be tuned by applying positive and negative voltages. In Figure 1.9, a scheme of the cross-section of a metal/PZT/MgO/SiO_2/Si FeFET is depicted.

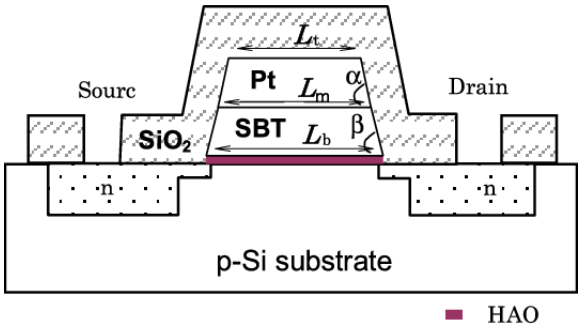

Figure 1.9: Scheme of the cross-section of a metal/PZT/MgO/SiO_2/Si FeFET.

The advantage of FeFETs with respect to similar floating-gate transistors relies on the fact that FeFETs allow faster programming processes at lower voltages. On the other hand, their integration with CMOS technology remains a challenge due to material issues. The employment of ferroelectric films for synaptic applications require also a minimum thickness of $\sim$ 100nm in order to provide a significantly large conductivity state window, which limits the scalability of these devices. Stability of the synaptic weight is also compromised because of the charge trapping/detrapping in the regions near the interface of the gate stack. Due to all of the mentioned limitations which lead to unstable synaptic weights with poor scalability and integration capabilities, the interest in employing FeFETs for analog neuromorphic computing applications decayed during the last years.

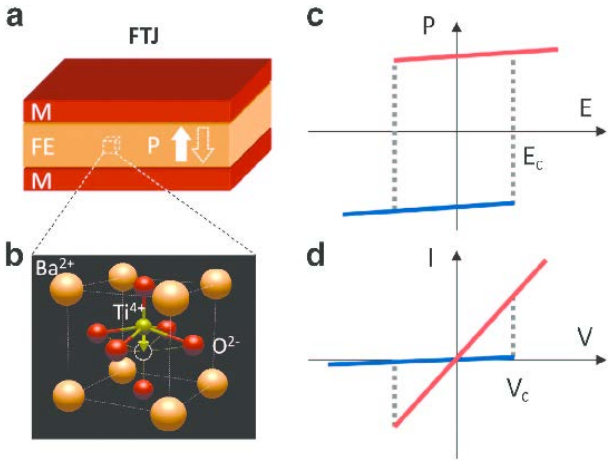

Figure 1.10: Scheme of the cross-section of ferroelectric FTJ and its typical electrical characteristics.

However, the recent discovery of a ferroelectric phase of HfO_2 maintained the interest in investigating ferroelectric devices for electronic synapse applications. The ferroelectric phase of HfO_2

leads to an improvement of the thickness scalability of the device, and provides longer retention times. Devices with analog conductivity state tuning capabilities and CMOS compatibility have been recently reported in [**?**]. In this case, the structure is no longer the one of a FET, but of a ferroelectric tunnel junction (FTJ) (Figure 1.10). Such FTJ devices are in an earlier stage of development and more research has to be conducted, in contrast with PCM and RRAM devices.

Spin-Transfer-Torque Magnetic RAM (STT-MRAM) technology is based on ferromagnetic materials, displaying the bipolar resistive switching phenomena. The main component of the STT-MRAM is the magnetic tunnel junction, consisting of two magnetic layers, referred to as the free and the reference layers, separated by a tunneling barrier (Figure 1.11). The magnetization of the reference layer is fixed and provides a reference to the magnetic orientation of the free layer, which can be switched between two states. It is the Spin-Transfer-Torque (STT) effect permits to switch the magnetic orientation of the free layer. Then, if the two layers share the same orientation, the device is considered to be in the parallel state, whereas if the orientation is the opposite, then the device is in an anti-parallel state. The Tunneling Magneto-Resistance (TMR) effect permits to distinguish between the resistance states related to the parallel and antiparallel states, so the stored information can be retrieved. Compared to the other technologies, the STT-MRAM presents very high endurance, because any magnetic degradation is associated to the switching of the magnetic orientation. Due to its stochastic switching nature, currently only binary stochastic synapses can be implemented with STT-MRAM technology.

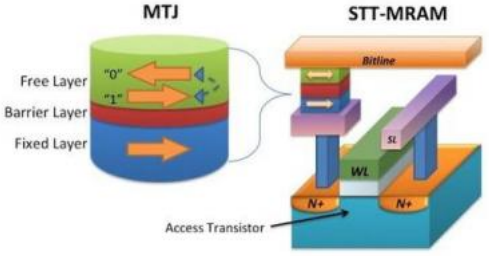

Figure 1.11: Scheme of the cross-section of a STT-MRAM.

3.5 Comparison between resistive switching technologies for synaptic applications

In this subsection, a comparison between the different NVM devices is presented. Table 1.1 summarizes the benchmark for the above mentioned technologies, according to the demonstrated Figures of Merit (FoM) indicated at the 2013 International Technology Roadmap for Semiconductor (ITRS):

FoM	**PCM**	**STT-MRAM**	**CBRAM**	**OxRAM**
Programming Voltage (V)	3	1.8	0.6	1
Programming Time (ns)	100	35	< 1	< 1
Programming Energy (J/bit)	$6 \cdot 10^{-12}$	$2.5 \cdot 10^{-12}$	$8 \cdot 10^{-12}$	$< 1 \cdot 10^{-12}$
Read Voltage (V)	1.2	1.8	0.2	0.1
Retention Time (yr)	> 10	> 10	> 10	> 10
Endurance # Cycles	10^9	$> 10^{12}$	$> 10^{10}$	$> 10^{12}$

Table 1.1: Comparison between the different NVM memories performance according to the 2013 International Technology Roadmap for Semiconductor (ITRS). The demonstrated characteristics values are indicated.

The key research questions and issues are now discussed according to the 2019 Nereid. In the case of OxRAM, the interest is focused on reducing the forming voltage and the operation energy. In order to do so, new materials and programming schemes need to be investigated. CBRAM presents similar issues, including also the need to increase its endurance up to 10^5, and improve the data retention. Both technologies are good candidates to be used in neuromorphic computing applications, being the OxRAM suitable for both analog and stochastic binary synapse implementations, and the CBRAM for the latter case. RRAM technology has been demonstrated to have the lowest programming voltage, time and energy and reading voltage, while showing great endurance. However, the impact of their intrinsic variability should be evaluated for each application. PCM technology is suggested to be the most mature NVM solution, with some specimens existing on the market. This technology still needs to improve its programming time, integration capabilities and data retention for scaled nodes. However, it is not the most attractive option for synaptic applications if compared to OxRAM or CBRAM, which offer better synaptic weight updating behavior, and the synapse implementation can be carried out with a single device. For the MRAM, the issues are related to integration, consumption and scaling. It must be taken into account that the high current consumption can suppose a serious drawback for some applications such as Internet-of-Things (IoT) and neuromorphic computing. In any case, despite these technologies are very promising for neuromorphic applications, they have to still face important challenges in order to become a reliable solution. Nowadays, researches agree that if application-driven design is considered, different specifications may arise, where trade-offs in the device characteristics will be hard to be overcome.

4 Memristor-based neuromorphic computing: State-of-the-Art

Neuromorphic computing hardware has undergone rapid development in the last two decades, with the introduction of a large variety of designs, implementation methodologies and prototype chips. All shared a common objective: to mimic the functional behavior of the human brain within the same budget of energy. The key-finding for today's research in the neuromorphic engineering field was in 2008, when R. Stanley Williams from Hewlett Packard Laboratories (HP) reported Chua's postulated electronic device, the memristor [38], and explored their use as a synaptic device [39]. Many electronic devices with memristive properties were already reported by this time, but they were not described as memristors. In the same year, Hylton and Nugent launched a DARPA program (DARPA is the Defense Advanced Research Projects Agency, an agency of the U.S. Department of Defense), the Systems of Neuromorphic Adaptive Plastic Scalable Electronics (SyNAPSE) program, with the goal of demonstrating large scale adaptive learning in integrated memristive electronics at biological scale and power. This program was undertaken by Hughes Resarch Laboratories, HP and IBM Research.

In late 2014, IBM announced a spiking-neuron integrated circuit called TrueNorth [40], evading the von-Neumann architecture bottleneck, boasting a power consumption of 70 mW, about 1/10,000th the power density of conventional microprocessors. It is however not currently capable of on-chip learning or adaptation. Other neuromorphic computing projections included: SpiNNAker [15] at Manchester University in the United Kingdom; BrainScale [41], another European project headed by Heidelberg University; CogniMem [42], a California-based chip manufacturer; Neurogrid [14], located at Stanford University; BioRC [43], building carbon nanotube transistors at University of Southern California; MIT Silicon Synapse [44], from Massachusetts and Cog Ex Machina [45], a project out of Boston University and HP.

Within the different proposed approaches, there are substantial differences in the way in which the

goal is pursued. According to [17], they can be group in two main classes, namely emulative and simulative solutions (Figure 1.12).

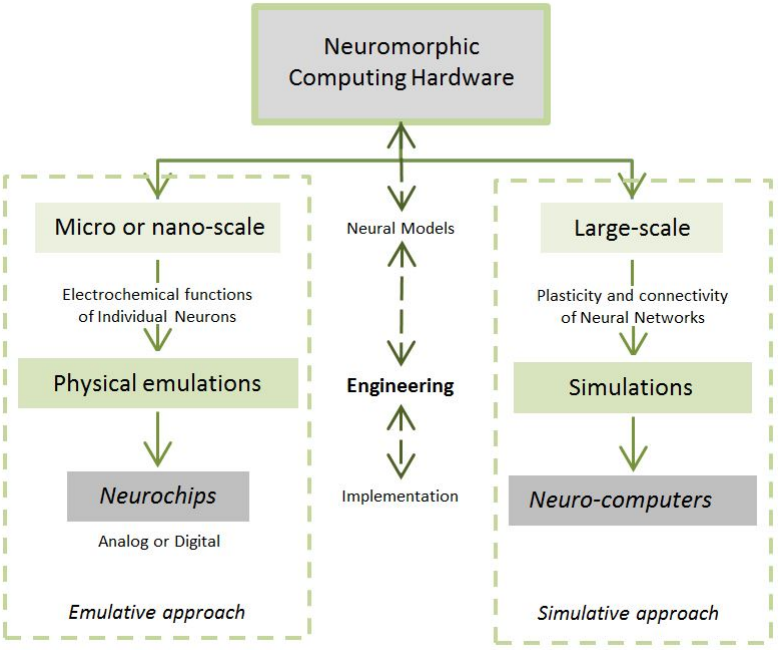

Figure 1.12: Neuromorphic hardware implementations: emulative and simulative solutions

The emulative approach focuses on physical emulations of neural models using inherently noisy and unreliable micro or nanoscale electronic components, with feature sizes approaching the atomic structure of matter. Circuits resulting from this approach are typically referred to as neurochips. These solutions have the potential to exploit the non-linear current characteristics of silicon-based transistors to naturally replicate the electrochemical functions of neurons. The choice of analog or digital neural primitives constitutes the main factor distinguishing between different neurochips [17]: the work conducted by Carver Mead [46] belongs to the class of analog neurochips, as it integrates biologically inspired electronic sensors with analog circuits. Analog circuits are very compact and offer high speed at low energy dissipation as they inherently perform neuron-like functions, such as integration and summation of currents and charges, but are less tolerant to noise. On the other hand, digital circuits offer high computational power, high reliability and faster prototyping due to the availability of powerful computer-aided design tools, but compared to analog implementations, they have a relatively large size, and also many elementary functions (like integration) are not available. Pioneering works on digital circuits during the 90s were for example Ramacher et al. (1993) [47] or Jahnke et al. (1996) [48].

Simulative approaches are those that focus on simulation of neural models rather than precise emulation of neural signals. Such methods referred to as neuro-computers, exploit the large availability of low-price, reliable integrated circuits to speed up the execution of neural models. They aim to reproduce large systems that abstract away the concrete biological details of the brain and focus on the brainâĂŹs larger-scale architecture, concretely in the plasticity of structures and connectivity. The largest-scale project aimed at building computer simulations of sections of the brain is the Blue Brain project at École Polytechnique Fédérale de Lausanne (EPFL) in Switzerland [49] and it is based upon one of the world's most powerful supercomputers, the IBM Blue Gene/L. This machine delivers up to $360 teraFLOPS$ of computing power from 8192 PowerPC CPUs, each running at 700âĂŁMHz and arranged in a toroidal mesh. Alongside the IBM supercomputer there

is a sophisticated stereo visualization system. The Blue Brain Project is an attempt to create a synthetic brain by reverse-engineering the mammalian brain circuitry, in order to study the brain's architectural and functional principles by simulating biological neural networks using detailed compartmental neuron models, and aims to deliver biologically accurate models of neural microcircuits such as the neocortical microcolumn. In addition to exploiting their computational resources, the Blue Brain team is also assembling a major database of biological neural data upon which to base their computer models. The emphasis is on maximally accurate models of biological neural systems.

A more recent, large-scale project in which neuromorphic computing is involved is the Human Brain Project (HBP). The HBP is a large ten-year scientific research project that aims to build a collaborative information and communication technologies (ICT)-based scientific research infrastructure to allow researchers across the globe to advance knowledge in the fields of neuroscience, computing, and brain-related medicine. HBP started on 1 October 2013, is coordinated by the EPFL, and is largely funded by the European Union. The project is based in Geneva, Switzerland. Neuromorphic computing is a fundamental pillar of the HBP and one of the six platforms implemented within it (the Neuromorphic Computing Platform, NCP). The NCP is closely linked with two other HBP platforms: the Brain Simulation Platform and the High-Performance Computing Platform. The former feeds the NCP with brain models, whereas the latter provides supercomputing, and cloud capabilities as well as the system software, middleware, and visualization support necessary to create, simulate and analyze multiscale brain models. HBP is also developing neurochip-like computing systems (NCS), particularly one termed NM-PM in the project, where PM stands for physical model. It is based on the European Fast Analog Computing with Emergent Transient States project (FACETS) [50], which has pioneered an approach combining local analog computation in neurons and synapses with binary, asynchronous, continuous time spike communication. FACETS aimed to research the properties of the human brain. Established and funded by the European Union in September 2005, the five-year project involved approximately 80 scientists from Austria, France, Germany, Hungary, Sweden, Switzerland and the United Kingdom. The main project goal was to address questions about how the brain computes.

Another objective of the HBP was to create microchip hardware equaling approximately 200,000 neurons with 50 million synapses on a single silicon wafer. Last prototypes were running 100,000 times faster than their biological counterparts, which would make them the fastest analog computing devices ever built for neuronal computations. The institutions involved were the University of Heidelberg, the French National Centre for Scientific Research (CNRS) of Gif sur Yvette, the CNRS of Marseille, the Institut National de Recherche en Informatique et en Automatique, the University of Freiburg, the University of Graz, the EPFL, the Swedish Royal Institute of Technology, the University of London, the University of Plymouth, the University of Bordeaux, the University of Debrecen, the University of Dresden and the Institute for Theoretical Computer Science at Technische Universitat Graz.

Current versions of the HBP FACETS-based NM-PM system incorporate 5ÃŮ107 plastic synapses and 200,000 biologically realistic neuron models on a single 8-inch silicon wafer. In terms of technology, the large-scale FACETS system is based on a mixed analog/digital VLSI implementation in a standard $180nm$ CMOS process. Local computation in neurons and synapses is mostly performed by compact custom-designed analog circuits, which communicate by exchanging spikes in an asynchronous fashion. The neuron and synapse models implement state-of-the-art results from neuroscience; the models include features such as plasticity mechanisms and a complex neuron model with up to 16,000 synaptic inputs per neuron, spike frequency adaptation and various firing modes as observed in biology. As the substrate represents a typical non-von Neumann system architecture, the memory required for synaptic weights and cell parameters is distributed in the computing fabric and employs technologies like small SRAM memory cells as well as analog units. According to [17], a key characteristic of the NM-PM computing system is that it does not execute a programmed code, but evolves according to the physical properties of the electronic devices. In this sense, NM-PM truly implements the neuromorphic hardware paradigm, in which a specific

hardware architecture is used to implement a brain model.

Currently, several fundamental learning rules for neuromorphic computation have been reported in OxRAM-based neuromorphic systems, and believed to be critical for the efficient operation of biological systems, including rate-dependent synaptic plasticity (SRDP) [51][52], timing-dependent synaptic plasticity (STDP) [51][6] [53].

Chapter 2

Electrical characterization and modeling of OxRAM devices as analog synapses

The possibility to tune the conductivity state of the electronic synapses is essential for a neuromorphic system implementation. It is referred to as their plasticity property if the induced changes are dependent on the previous history of the devices. The implementation of analog synapses demands an electronic device displaying multiple, continuous and reconfigurable conductivity states within a limited range [54, 26, 55, 56, 57, 58]. It is specially desirable to induce similar increments (potentiating) and decrements (depressing) in the conductivity state for similar voltage increments/decrements [18, 59, 60, 61], since the symmetry between these two procedures increases the performance of the neural network. Furthermore, the control of the conductivity state is preferred to be done by means of the application of pulsed voltage waveforms for two reasons: first of all, pulse-programming schemes permit a simple codification of the input data to be fed to a neural system, by means of modulating the pulse parameters, such as the pulse-width, amplitude or number of consecutive applied pulses. Lastly, the shorter the application of the voltage or current required to modify the conductivity state of the electronic synapses, the lower is the power dissipation [62, 63, 64, 65].

Therefore, an initial study focused on verifying the tuning conductivity state property of the devices which will form the neural network is required. In this chapter, OxRAM devices are investigated (i.e. electrically characterized) to evaluate their potential capabilities as analog synaptic elements in neuromorphic circuits. The objective of this part of the thesis consisted in proving if and how the conductivity state of the tested samples can be controlled electrically. This parameter is identified as the synaptic weight, which determines the strength of the connection between two neural elements within neuromorphic architectures. This verification is performed under a DC characterization scheme. It is followed by a pulsed-characterization, as to investigate the dependences of the candidates' conductivity state on the pulse parameters, such as the pulse-width or amplitude. An automatic characterization setup involving the smart control of the employed equipment is proposed for this purpose and for extracting the pulsed G-V characteristics of the devices. These characteristics summarize how the conductivity state can be repetitively tuned in an analog fashion by means of modulating the voltage applied to the device, successfully providing multiple and controllable conductivity levels within a specific range.

Lastly, the obtained G-V characteristics are modeled, allowing the simulation of the tested devices behavior under a neuromorphic context. Because the OxRAM technology presents significant variability, the cycle-to-cycle variability is also studied in terms of the model parameters statistics, so

that its impact in the learning performance of a neuromorphic system can be further analyzed in the third chapter of this thesis.

1 Tested samples description

The tested samples, provided by the IMB-CNM (CSIC), consist in $TiN - Ti - HfO_2 - W$ Metal-Insulator-Metal (MIM) structures with 10nm oxide thickness and an area of $5x5\mu m^2$. The devices were fabricated on Si wafers with a thermally grown 200nm-thick SiO_2 layer. The 10nm-thick HfO_2 layer was deposited by atomic layer deposition (ALD) at 225°C using TDMAH and H_2O as precursors, and N_2 as carrier and purge gas. The bottom electrode consists of a $200nm - W$ layer and the top electrode of a $200nm - TiN$ on top of a $10nm - Ti$ layer acting as oxygen getter material. The resulting device structures are square cells with an area of $5x5\mu m^2$. A cross-sectional view is shown in Figure 2.1. Further details of their fabrication process can be found in [66].

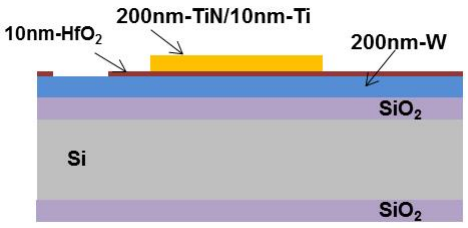

Figure 2.1: Schematic of the tested MIM structures.

The samples present the bipolar resistive switching phenomena. Examples of (1) the forming process, occurring at 2V, and of some resistive switching cycles consisting on the consecutive induction of (2) SET and (3) RESET processes are depicted in Figure 2.2. Under the framework of this thesis, these devices were electrically characterized using both DC and pulsed test schemes, in order to verify if they are able to play the electronic synapse role.

2 DC characterization

For the DC characterization, two different electrical test schemes were used, involving the smart control of the applied negative voltage limit (V_{lim}) and varying the maximum current driving the devices during the SET process, also referred to as the compliance current (I_c). A MATLAB script was specifically developed for controlling the semiconductor parameter analyzer Agilent4156C (SPA) via GPIB communication and for automatizing the characterization tests.

The performed experiments consisted in the application of consecutive, positive and negative voltage ramps in order to induce the SET and RESET processes, respectively. Two different devices were tested: one device for each of the two test schemes. For both test schemes, the I_c parameter was controlled and varied gradually from cycle to cycle from $10\mu A$ up to 5mA for the SET process. On the other hand, two cases were considered for the RESET process, which was compliance free:

(1) V_{lim} as the voltage measured when the RESET process was detected as a current drop, and the applied negative voltage ramp was immediately interrupted (Figure 2.3, bottom). This second case is referred to as the **free** V_{lim} **test**, since any imposition was made over this parameter. For this test, the I_c parameter was swept sequentially from $10\mu A$ up to 1mA during 100 resistive switching

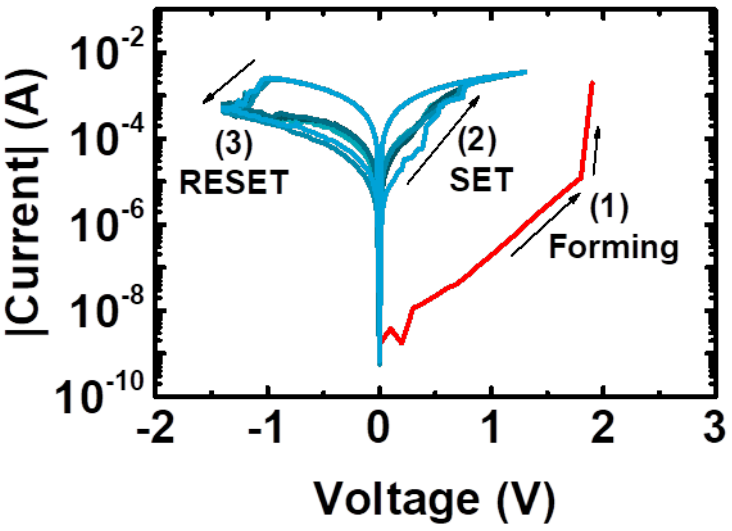

Figure 2.2: Examples of I-V characteristics of a MIM device from the described technology, displaying bipolar resistive switching phenomena. **(1)** The forming process occurs at 2V, and is followed by a few **(2)** SET and **(3)** RESET processes.

cycles. Given the results of this test, the I_c parameter range was increases for the second case, in order to verify the dependence of the reached conductivity on I_c.

(2) V_{lim} as a fixed voltage, set at V_{lim}=-1.6V (Figure 2.3, top). This case is further referred to as the **fixed** V_{lim} **test**, and is the common procedure. In here, 890 resistive switching cycles were performed, during which the I_c parameter was swept sequentially from 10μA up to 5mA.

Examples of the I-V characteristics of the tested samples for the two considered test cases are depicted in Figure 2.3 (top, fixed V_{lim} case; bottom, free V_{lim} case).

With the free V_{lim} case, the conductivity state of the device right after the RESET had occurred could be studied and further compared with the results obtained via case (1). The method for the smart control of the interruption in case (2) consisted in performing a linear fitting of the I-V curve at low voltages during the measurement, which was extrapolated at high voltages giving rise to the control parameter I_{fit}. Values of I_{fit} were then compared to the experimentally measured current values, I_{exp}. Then, a criteria for stopping the application of the negative voltage ramp was defined as a particular value of the ratio between I_{exp} and I_{fit}, I_{exp}/I_{fit}=0.9. If the measured ratio I_{exp}/I_{fit} was equal or below 0.9, the negative voltage ramp was interrupted. In Figure 2.3 (bottom), the I_{fit} and I_{exp} values are identified for two different cycles.

In Figure 2.4, the employed I_c values (top) and the obtained conductivity state G (bottom), expressed in G_o units ($G_o = 7.75 \cdot 10^{-5}$S, the conductance quantum unit) after the SET for the fixed V_{lim} case (measured at 0.1V) are plotted against the number of performed cycles, showing that the control of the conductivity state of these devices is repetitive, and also symmetric in terms of synaptic potentiation and depression, being independent of the direction of the change of I_c in between consecutive cycles.

The conductivity state of the device G after the SET (G after SET) and RESET (G after RESET) was calculated as the V-I ratio measured at | 0.2 |V. The G values (normalized to G_o) measured for the two test cases after the RESET and SET processes are plotted versus I_c in Figure 2.5 top and

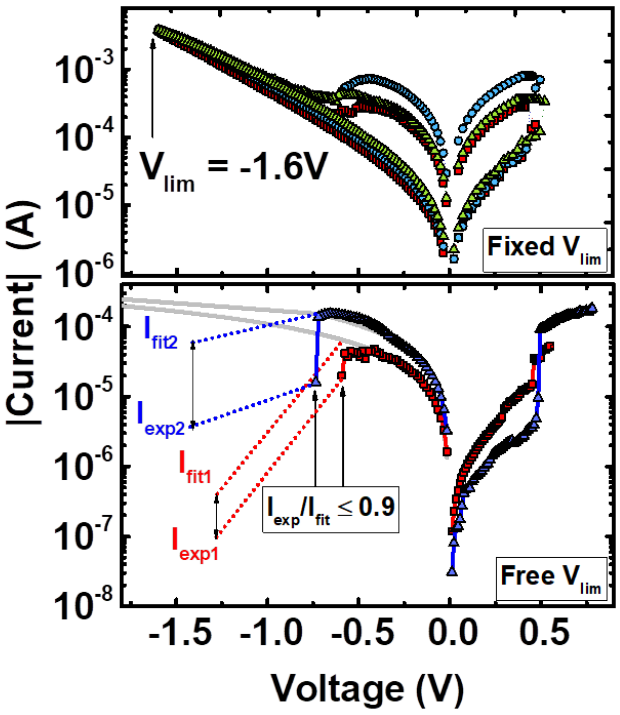

Figure 2.3: **(Top)** Fixed V_{lim} case: example of I-V curves measured when V_{lim} was fixed to -1.6V. **(Bottom)** Free V_{lim} case: example of I-V curves for the interrupted measurement procedure. The gray line corresponds to the linear fitting of the I-V curve for negative voltages. I_{fit}, I_{exp} and V_{lim} for two different curves are indicated.

bottom, respectively. It can be observed that for $I_c > 0.1$mA, the G after the SET values increase with increasing I_c. Below this value, no dependence is observed. On the other hand, the obtained G values after the RESET show no dependence on I_c. Larger cycle-to-cycle variability is observed for G after the RESET process in the free V_{lim} measurement case, in contrast with the values of the fixed V_{lim} configuration.

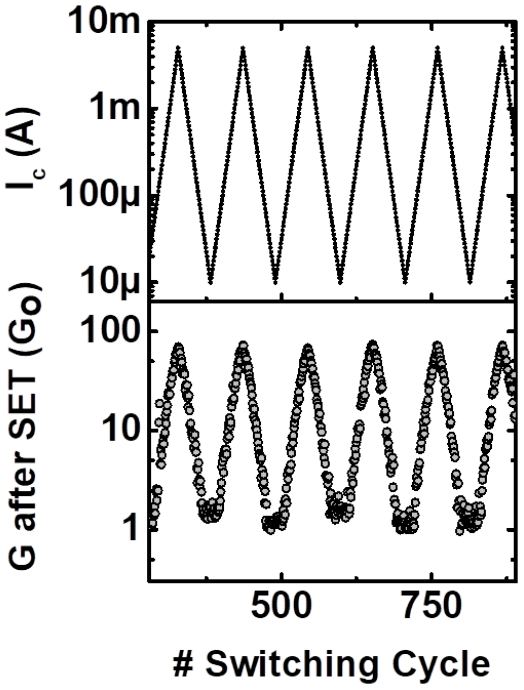

Figure 2.4: The conductivity state after the SET was evaluated when I_c was sequentially increased and decreased. **(Top)** I_c employed during each SET process **(Bottom)** conductivity state, G, measured indirectly at 0.2V after each SET process, plotted vs. the number of performed cycles for the fixed V_{lim} case, from the 280th to the 890th (final) cycle.

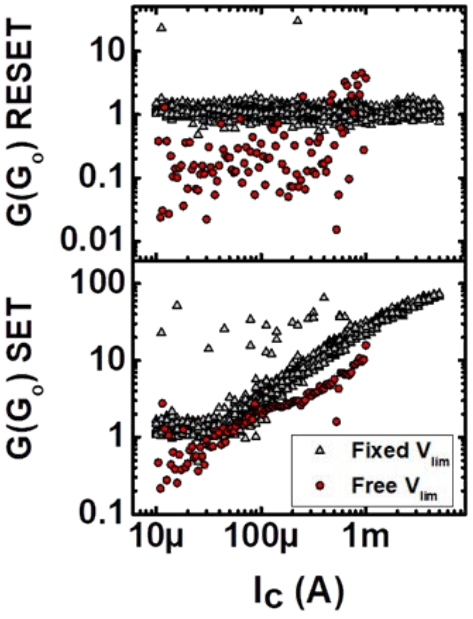

Figure 2.5: Normalized G values after **(Top)** the RESET process and **(Bottom)** the SET process, measured at -0.2V, plotted versus the current compliance used for the SET process. Results for the two measurement schemes are shown.

Results of Figure 2.5 support that the conductivity state of the device can be tuned by means of varying the I_c employed during the SET process, suggesting the capability of these devices to be

used as a synaptic element in neuromorphic circuits. Despite no correlation between I_c and G after the RESET is observed, it appears being controlled by the V_{lim} variable, as seen in other studies [66].

To further investigate the conductivity of the devices, the I-V characteristics for each cycle were fitted to $I = A \cdot V^b$ within the range 0V-0.2V [67]. In Figure 2.6, the obtained A/G_o versus b coefficients after the RESET (Figure 2.6.a) and the SET (Figure 2.6.b) processes are plotted respectively, where A is identified as the conductance of the device if b=1. Results displayed in Figure 2.6.a, corresponding to the A parameter after the RESET, show that A can be identified as the conductance of the device when $A/G_o \geq G_o$ and b=1, for some of the cycles of the fixed V_{lim} case, and for a minority of the cycles of the free V_{lim} case. According to the Quantum Point Contact (QPC) model [[68]], if the conductive filament (CF) between the two electrodes is completely formed, I-V displays a linear relationship (b=1 and $A/G_o \geq 1$). For the free V_{lim} case, most of the A values are below $1G_o$ ($A/G_o < 1$), highlighting the partial disruption of the CF, which results in a spatial gap. This is corroborated by the observed I-V potential dependence ($b \neq 1$). For some cycles of the fixed V_{lim} case, $A/G_o > 1$ with $b \sim 1$, so under this test configuration, the CF appears to be fully-formed after a RESET process, being the linear I-V characteristics maintained. It is suggested that the continuous application of a negative voltage once a RESET process has been induced is fundamental for keeping the CF formed.

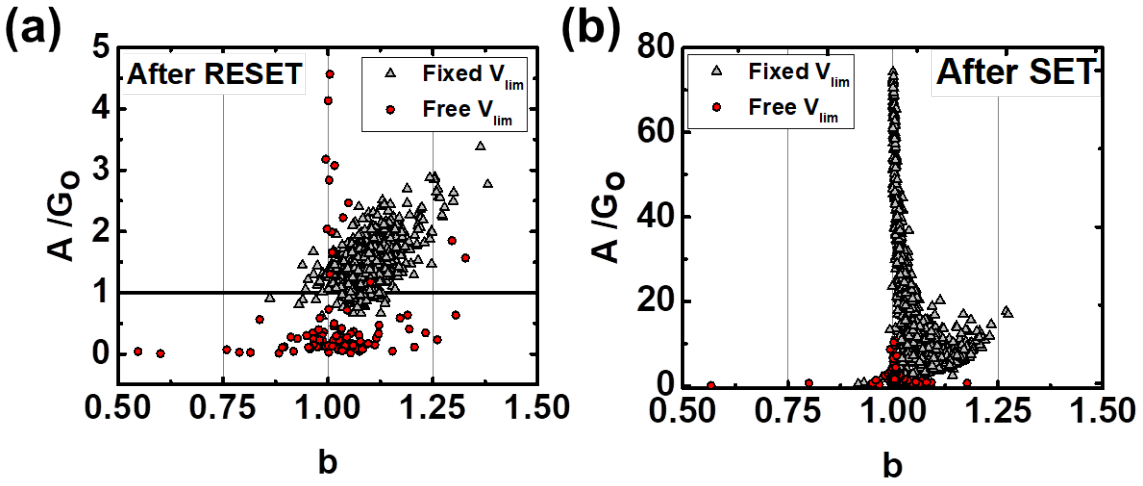

Figure 2.6: **(a)** A/G_o versus b parameter obtained by fitting the I-V characteristics to $I = A \cdot V^b$ at 0.2V after the RESET process. **(b)** A/G_o versus b parameter obtained by fitting the I-V characteristics to $I = A \cdot V^b$ at 0.2V after the SET process.

The A/G_o values after the SET process are shown in Figure 2.6.b, being larger than the ones obtained after a RESET process, as expected. Lower A/G_o values appear to be much more scattered than larger A/G_o in terms of their corresponding b values. Larger A/G_o values show a linear relationship between I and V ($b \sim 1$). Specifically, when $A/G_o > 10$ and b is approximately 1, the conductivity can be tuned in coherence with the results of Figure 2.4 and Figure 2.5. The conductivity control is supported by the results shown in Figure 2.7, where the b (top) and A/G_o) (bottom) coefficients for the I-V characteristics after SET are plotted versus I_c. In here, the tunable conductivity region is identified. In this region, starting from $I_c = 0.5$mA, the range of A/G_o between 10 and 80 corresponds to $b \approx 1$, indicating that the A parameter corresponds to the G state of the tested device, as seen in Figure 2.5. According to [69], these results suggest that the G state of the tested devices under the configuration of the fixed voltage limit can be tuned by means of modulating I_c parameter as long as $I_c \geq 0.5$mA. It is suggested that the variation of this parameter allows to modulate the size of the CF in a reversible and repetitive way. It is also suggested that,

if the same CF remains as the principal conducting path during the performed resistive switching cycles, the conductivity of the device beyond a certain threshold value ($\approx 10G_o$) behaves linearly with the current compliance, fulfilling the main requirement for the implementation of an analog electronic synapse.

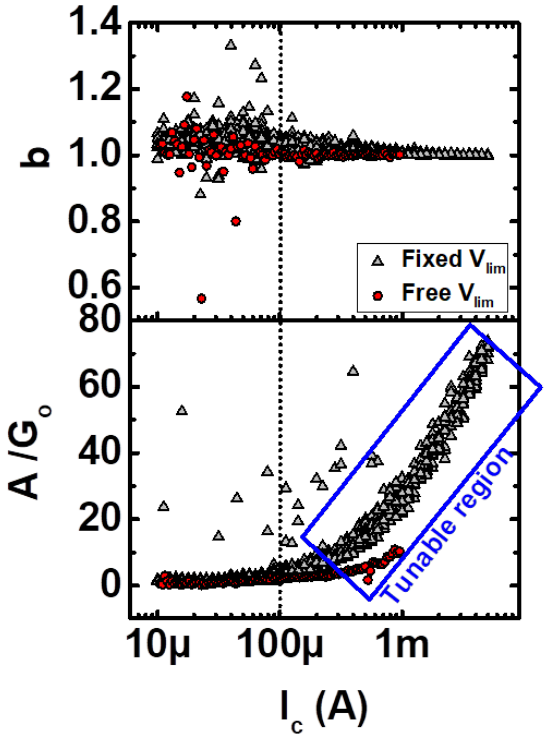

Figure 2.7: (Top) b and **(Bottom)** A/G_o versus I_c after the SET process. The tunable region starting from $I_c = 0.5$mA is marked for the two test schemes, corresponding to $b \sim 1$ and $A/G_o > 10$.

The highlights of this subsection results can be summarized with the following concepts: a continuous tuneable region of the I-V characteristics in which the tested devices behave linearly ($b \approx 1$) has been found. In here, the G state is controllable in a reversible fashion, being dependent on the I_c parameter. It is suggested that the analog control of G in the mentioned region is possible and repetitive because the main CF remains formed ($A > G_o$) after the induction of a RESET process. Hence, the performed DC characterization support that these samples are potentially good candidates for the implementation of analog electronic synapses, where their G is identified as the analog synaptic weight, since it presents a continuous and controllable range of possible values [Conf1, Conf2, Art1, Art3].

3 Single-pulse characterization

Applications within neuromorphic engineering involve pulse programing schemes, where the control of the OxRAM electrical characteristics with the suitable pulse parameters becomes mandatory. The objective of the work described in this section consists in achieving using such program scheme an analog change of the device conductivity state, which is related to a synaptic weight update. In particular, this section is focused on the characterization of the OxRAM devices by the application of single pulses, as a necessary previous step for the understanding of the effects of pulse

trains on the device conductivity state for neuromorphic applications. For this purpose, a flexible automatized characterization setup is proposed, in which the application of voltage pulses can be combined with conductivity measurements. With this setup, the G-V characteristics of the tested samples were obtained, which were widely used during the rest of this thesis. The results are of great importance, since they outline how the conductivity state of the OxRAM can be tuned in an analog fashion under a pulse-programming scheme.

3.1 Measurement setup description

The pulsed characterization consisted in the study of the single-pulse parameters effects on the conductivity state of the devices, such as the pulse amplitude and the pulse-width. The proposed measurement setup involves the smart control of the employed equipment via GPIB communication, so that multiple test schemes can be automatized. In here, the semiconductor parameter analyzer Agilent4156C (SPA) employed for the DC characterization was combined with the pulse generator Keysight 81101A (PG). The samples were tested with the setup depicted in Figure 2.8, consisting in the alternated use of the SPA and the PG, where the functions of each instrument are summarized in Figure 2.8.b) and 2.8.c), respectively. Both SPA and PG were connected simultaneously to the device (Figure 2.8.a), each of them to one of its terminals (SPA, top electrode, and PG, bottom electrode).

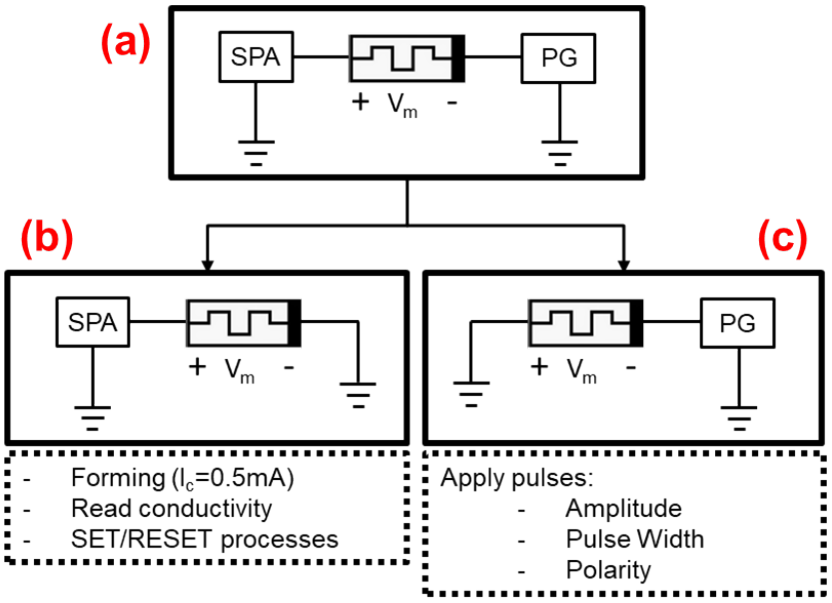

Figure 2.8: Pulsed-characterization setup. **(a)** The SPA and the PG are connected to the top and bottom electrodes of the tested sample, respectively. However, only one of these instruments is active during each stage of the characterization tests, being the other one grounded. **(b)** The SPA is activated when the forming, reading or SET/RESET processes are performed on the sample, whereas the PG is kept grounded. **(c)** The PG is activated when pulses are applied to the sample, keeping the SPA grounded.

The PG can be flexibly configured, to apply single pulses or pulse trains, with amplitude, pulse width (PW) and polarity defined by the user. However, it is not possible to acquire the applied voltage or current with it. The PG was in charge of applying voltage pulses, whereas the SPA was employed for the forming stage (with $I_c = 0.5$mA), switching the device state by inducing controlled SET or RESET processes, and reading the current driven by the device as to indirectly measure its conductivity state. It must be emphasized that the SPA and PG cannot be simultaneously active:

when the SPA applies signals, the PG is grounded, and vice versa. A MATLAB script, which was specially developed for the automatization of the characterization setup used during this thesis, permitted to ground the electrode of the equipment which was not being used at a particular time (Figure 2.8.b and 2.8.c). With this configuration, a switch to alternate the connection of the sample between the SPA and PG is not needed. Then the parasitic effects derived from the circuitry used to implement the switch are mitigated, which might affect the measurements when low width pulses ($\sim$ 100ns) are applied and the device presents a very low conductivity state ($G < G_o$).

In Figure 2.9, a flow diagram of the adopted measurement scheme is shown. The characterization procedure consisted in **(a)** performing a current-controlled forming cycle with the SPA (Figure 2.9.a) using a voltage ramp as to enable the resistive switching behavior of the samples. When I_c is reached during the forming cycle, the application of the voltage ramp is automatically ceased. Then, **(b)** the SPA is used to tune the device conductivity (g_{set} in Figure 2.9.b) by means of applying a few DC resistive switching cycles (RS), consecutively inducing SET and RESET processes, in order to stabilize the main CF. In here, the minimum negative voltage reached during the RESET stage is kept at V_{lim}=-1.6V. For the current-controlled SET, I_c can be set by the user so a desired conductivity state can be reached, taking into account the results obtained in the DC characterization. In this case, $5G_o \leq G \leq 10G_o$ was chosen as the target g_{set}, according to the results of the previous DC characterization (see Figure 2.4). The number of cycles dedicated to set the conductivity state of the devices within a determined range depends on each device and its initial conductivity, given by the forming cycle. For the tested technology, three RS cycles were enough to set the device conductivity within the above mentioned range, using a current compliance of 0.5mA. Once this conductivity tuning stage is performed, **(c)** the pulsed-voltage test begins (Figure 2.9.c-d). The user defines a sequence of pulsed voltages (Figure 2.9.c), which are applied by the PG. This sequence may consist in single pulses, a pair, or a pulse-train, taking into account that pulses within a pair or a pulse-train are identical.

The key of the proposed characterization setup is that the user can program a large sequence of n pulsed voltages, where the conductivity of the device after every programmed voltage, g_{fin}, can be calculated from an SPA measurement (Figure 2.9.d). The pulse parameters, such as amplitude, pulse width or polarity of each of the pulses can be modified during the sequence. The programmed sequence can be repeated automatically N times, with the possibility of performing a new RS stage (Figure 2.9.b) for setting the conductivity of the device. With this pulsed characterization test scheme, the dependence of the changing conductivity state of the devices on the pulse amplitude was analyzed. Lastly, an extension was made in order to extract the G-V characteristics of the tested devices.

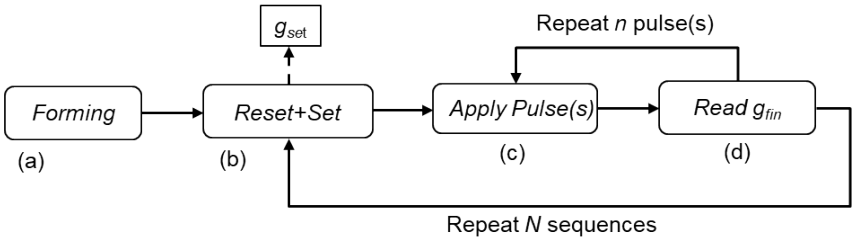

Figure 2.9: Flow diagram of the pulsed characterization measurements.

3.2 Dependence of DUT conductivity state on pulse amplitude and width

Using the characterization setup of Figure 2.8, the dependence of the OxRAM conductivity state on the pulse amplitude was studied in three different samples. More than N=100 iterations were

applied to each sample, consisting on 14 repetitions of the subsequence **(c)**-**(d)** (n=14 single pulses). The pulse amplitude was increased by | 0.1 |V in each **(c)**-**(d)** iteration, starting from | 0.1 |V up to | 1.4 |V , with a different PW for each tested sample (1ms, 10μs and 100ns). Both pulse polarities were studied in order to verify the ability to increase (potentiate) and decrease (depress) the conductivity state (synaptic weight) of the devices. A picture of the test scheme can be found in Figure 2.10. In between the application of increasing amplitude pulses, the conductivity state g_{fin} was measured by the SPA. When the pulse amplitude reached | 1.4 |V, three RS cycles with $I_c = 0.5$mAwere performed in order to set the conductivity state of the tested device to $5G_o \leq g_{set} \leq 10G_o$.

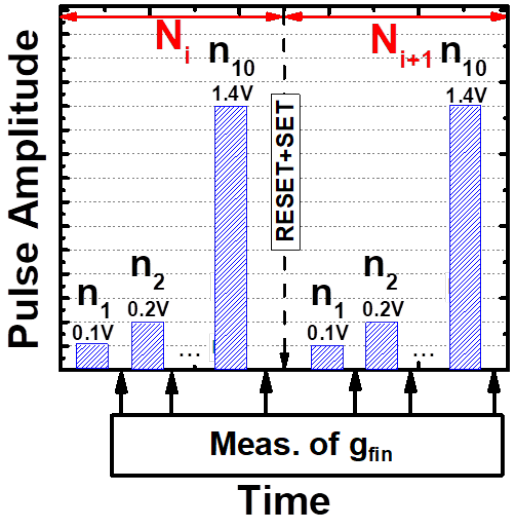

Figure 2.10: Test scheme used for studying the effects of the pulse amplitude on the conductivity state of the device. The sequence starts with the conductivity state given by the SET+RESET processes. Then, increasing amplitude voltage pulses are applied. In between every voltage pulse, the conductivity state g_{fin} is measured with the SPA. When the pulse amplitude reaches | 1.4 |V, three SET+RESET processes are induced again, and the increasing amplitude sequence restarts. This test was performed for both pulse polarities (negative not shown).

Results for the negative polarity are shown in Figure 2.11, where the conductivity state after the application of every single pulse is shown: **(a)** the data corresponding to a PW of 100ns; **(b)** 10μs and in **(c)** 1ms. The average is depicted in black. The first data point of every curve is given by the resistive switching cycles from step **(b)**, which set the average initial conductivity state to $g_{set} \approx 7.5G_o$. In here, the cycle-to-cycle variability can be observed, in accordance to the results obtained in the DC characterization. In average, the first data point for each sample is similar, being $g_{set} \approx 7.5G_o$. The next data points correspond to the conductivity state read after each pulse.

The following trend is observed in all cases: the first pulses do not change the conductivity state of the device until a particular pulse amplitude is reached (V_{thr}^{-}), being of 0.75V, 0.55V and 0.5V for each tested sample, respectively, showing a dependence of the V_{thr}^{-} average values with the PW parameter. Pulse amplitudes above (V_{thr}^{-}) do actually change the conductivity state of the device, which decreases non-linearly and finally saturates around $1G_o$ for pulse amplitudes larger than 1V, meaning that probably it is the minimum conductivity that can be reached through this method. Because all of the tested devices follow the same trend despite using different PW, it is concluded that in order to induce a depression in their conductivity state, negative polarity pulses with a pulse amplitude ranging from (V_{thr}^{-}) up to | 1V |V are required. It is also suggested as a general fact that, if the initial conductivity state of the device is smaller than $5G_o$, the probability of efficiently tune the device conductivity state is very low: in all cases, the curves which present these initial values due to the cycle-to-cycle variability effects on the resistive switching stage (Figure 2.9.b) do

not seem to respond to the cumulative effects of the pulse amplitude.

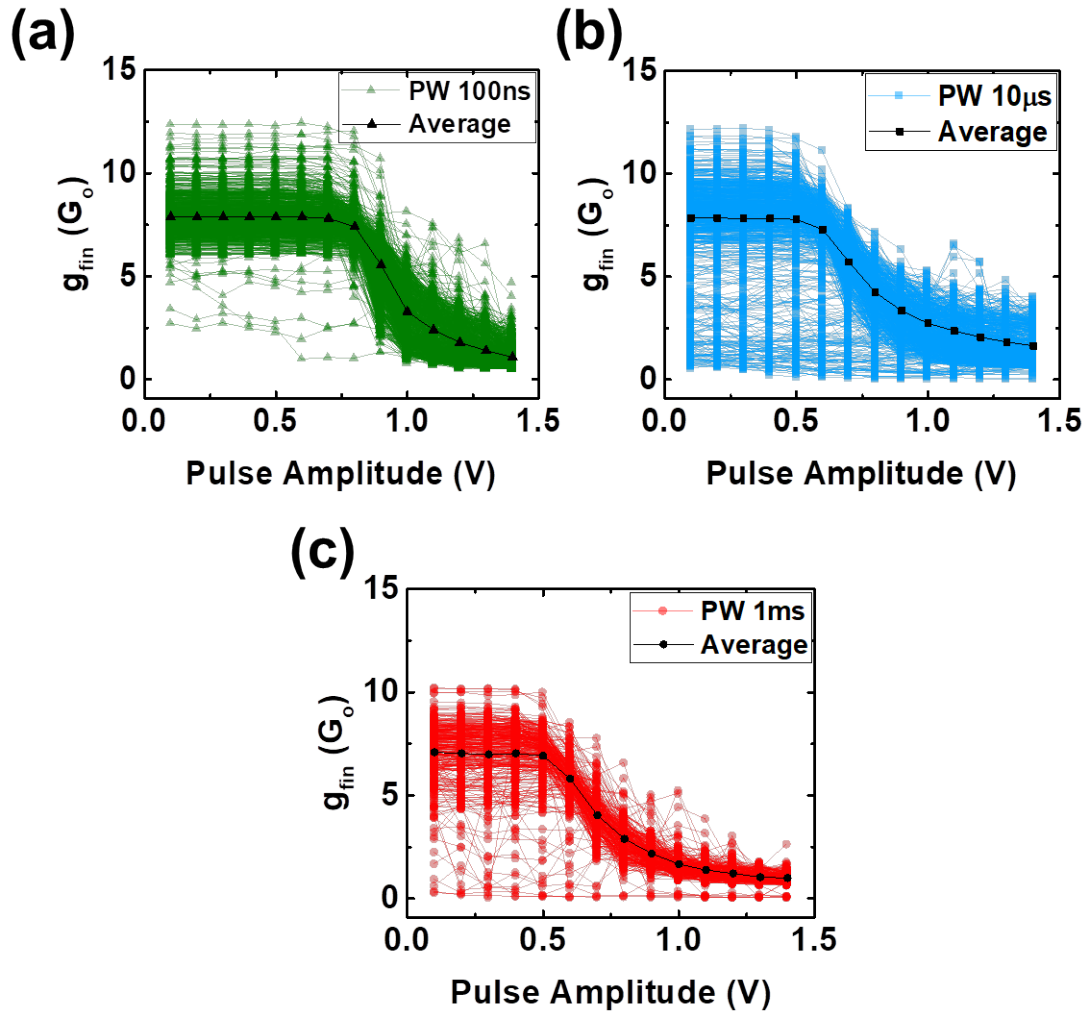

Figure 2.11: Cumulative effects on g_{fin} of increasing the pulse amplitude with a fixed pulse-width and negative polarity: **(a)** 100ns (green triangles), **(b)** 10μs (blue squares, **(c)** 1ms (red circles). The average is depicted in black.

In Figure 2.12, the resulting data for the case of positive polarity pulses are shown. The obtained g_{set} values of the three tested devices after the resistive switching cycles are $6G_o$, $8G_o$ and $12.5G_o$ in average. This deviation in g_{set} is attributed to the device-to-device variability. In a similar way to the negative polarity pulses case, the first low amplitude pulses do not affect the conductivity state of the devices. The observed threshold voltages V^+_{thr} are the following: 0.8V, 0.5V and 0.5V, again suggesting a dependence of the average V^+_{thr} with the PW, being in this case not as clear as in the negative polarity case. Beyond V^+_{thr}, the conductivity starts increasing with increasing pulse amplitude. In this case, any saturation of the conductivity state is observed in the studied pulse amplitude range, and the reached conductivity state after each iteration of the tests shows both cycle-to-cycle and device-to-device variability. Some of the curves of the PW = 10μs case show initial conductivity state values smaller than $5G_o$ due to cycle-to-cycle variability, and, as seen before for the negative polarity test, it is not possible to control the conductivity state of the device via varying the pulse amplitude with this initial condition.

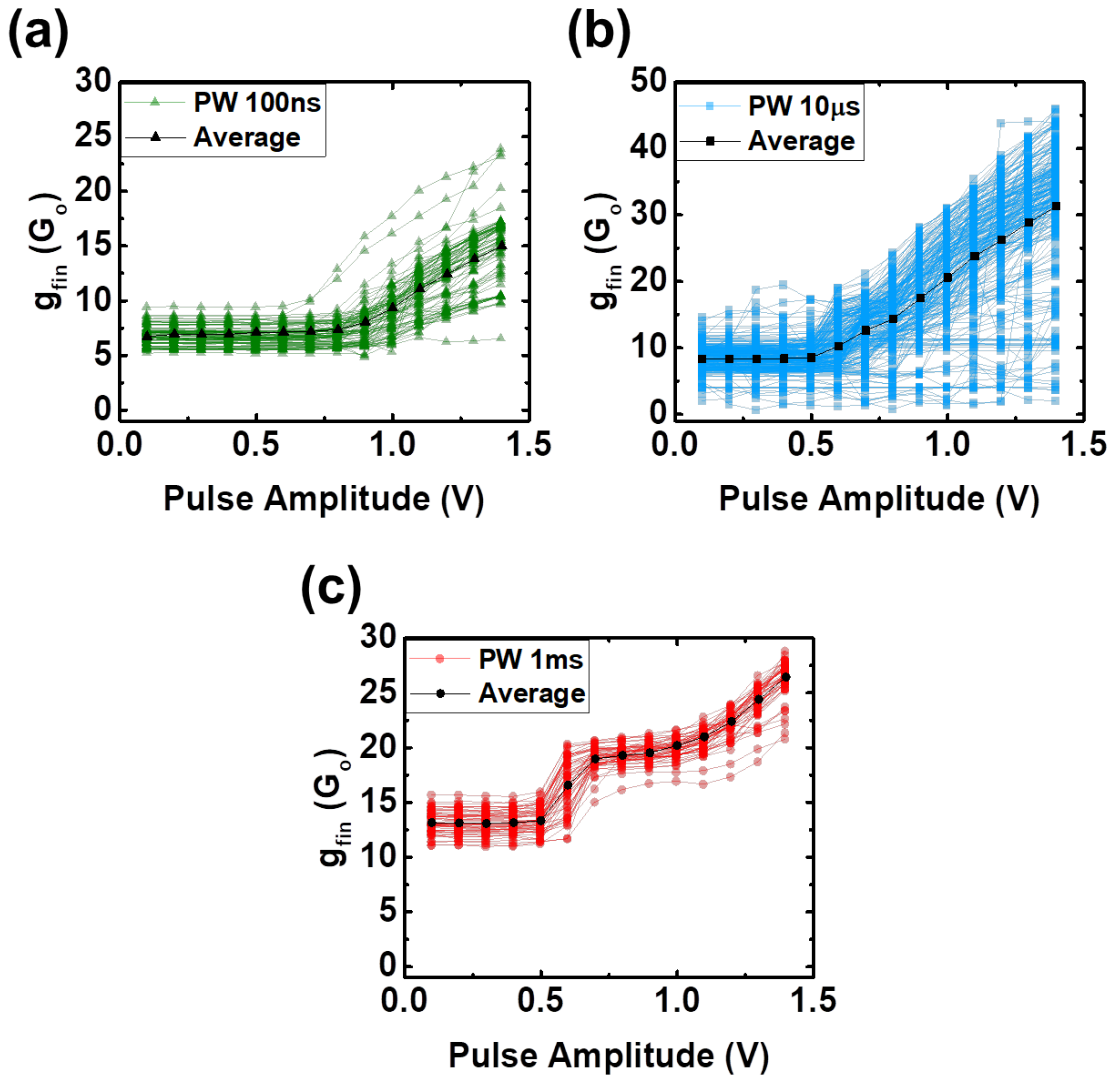

Figure 2.12: Cumulative effects on g_{fin} of increasing the pulse amplitude with a fixed pulse-width and positive polarity: **(a)** 100ns (green triangles), **(b)** 10μs (blue squares, **(c)** 1ms (red circles). The average is depicted in black.

The obtained results match the findings from [70, 66]. In the former, OxRAM-based 1T1R structures with the same resistive switching stack composition has been studied for neuromorphic applications. It is observed that, on one hand, the potentiation process related to a SET process depends mainly on the pulse amplitude and on the I_c parameters, and not on the pulse width. On the other hand, for the synaptic depression, related to a RESET process, a dependence of the conductivity on the total energy of the applied pulse is suggested, being this process dependent on both pulse amplitude and width. In the case of [66], the tested devices are the same as the ones tested in the present thesis. In [66], it is seen that the synaptic potentiation and depression can be induced by means of modulating the I_c and the pulse amplitude parameters, respectively. It is finally concluded from the results of these tests, that these devices allow the analog potentiation and depression of their conductivity state by means of modulating the pulse amplitude, which has to be at least of 0.5-0.8V, as long as the initial conductivity state is above $\approx 5G_o$, which is in accordance with the results of the DC characterization subsection. It has been seen that the evolution of the conductivity when the pulse amplitude is varied is similar for the different tested pulse-widths. Therefore, the pulse amplitude is chosen as the main pulse parameter to be varied in order to induce a conductivity change in the tested devices. However, significant cycle-to-cycle

variability is observed under single-pulse schemes, which has to be taken into account for the implementation of reliable synaptic devices, as seen in the following sections of the thesis.

3.3 G-V characteristics

Given the results from the previous subsection, where the device conductivity can be controlled by means of the applied voltage, another test scheme oriented to the characterization of the tested devices as synaptic elements is proposed. The goal was to obtain the G-V characteristics of the tested device. In order to do that, the flow diagram of the test from Figure 2.9 was slightly modified (Figure 2.13), in order to control the minimum and maximum conductivity states of the tested device within a range. The forming and initial resistive switching cycles (steps **(a)** and **(b)**) were kept the same as in Figure 2.9. The difference between the two test schemes relies on the fact that step **(b)** was applied only once. As in the previous flow diagram (Figure 2.9), a single pulse was applied (Figure 2.9.c) and the reached conductivity state g_{fin} was measured (Figure 2.9.d). Then, according to the measured g_{fin} value, the pulse amplitude of the following pulse was increased or decreased. The objective was to sweep the conductivity state of the device while keeping it confined within a certain range, between $18G_o$ and $30G_o$. The following criterion was automatized: pulses with increased amplitude by $|\ \Delta V\ | = 0.01V$ were sequentially applied until a maximum conductivity $g_{fin} = 30G_o$ was reached. At this point, the pulse amplitude was decreased by the same step, until the conductivity reached the minimum set by the user, $g_{fin} = 18G_o$. A voltage limit condition was also defined to avoid the total rupture of the DUT, being the maximum applied voltage of | 1.2 | V. However, these voltage limits were never reached during the test.

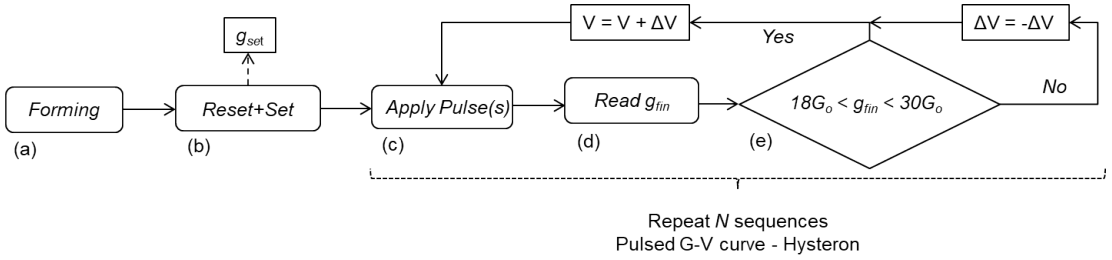

Figure 2.13: Modified flow diagram of the performed test scheme.

The envelope of the amplitude of the applied voltage waveform is depicted in Figure 2.14.a (inset). In here, the pulse amplitude values between -0.1V and 0.1V are not shown, because the corresponding pulses were not actually applied due to equipment limitation. More than 50000 pulses were applied to the DUT, corresponding to N=178 loops (at this point, the sample broke down). In Figure 2.14.b, the conductivity measured after each applied pulse is represented over the number of applied pulses (# pulse). As expected, the conductivity state can be controlled with the applied voltage, being a repetitive process. A zoom of the first 2000 pulses is shown as an inset, where the saturation of the conductivity state at $\approx 10G_o$ (minimum value) and at $\approx 33G_o$ can be seen. The minimum conductivity value presents a transient during the first 20000 pulses, in which it starts increasing from $5G_o$ up to $15G_o$, where it saturates.

In Figure 2.15, the conductivity is plotted over the voltage drop at the DUT, giving rise to the G-V characteristics consisting of 178 curves (one for each of the N=178 iterations). The G-V obtained during the first pulses are plotted in dark blue, and in a lighter color as time evolves. The transient of the minimum can be observed, whereas the maximum conductivity value remains constant over time. The increment of the conductivity G, which corresponds to the potentiation of the electronic synapse, occurs in average when the pulse amplitude V is above 0.3V, whereas its decrement, representing the synaptic depression, occurs for $V = -0.9V$. The synaptic depression

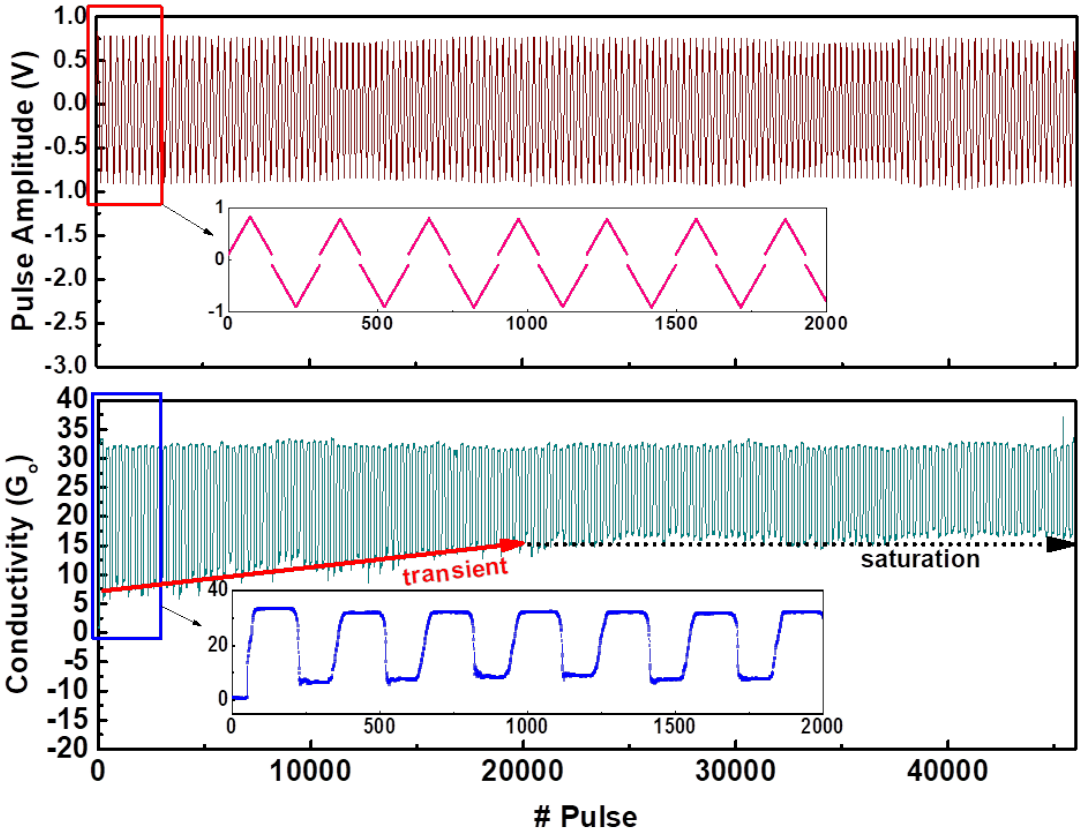

Figure 2.14: **(Top)** Envelope of the employed pulse amplitude and **(Bottom)** measured conductivity (in G_o units) after the application of each pulse, represented over the number of applied pulses. The minimum conductivity shows a transient during the first 20000 pulses in which it increases (indicated with a red arrow), and then saturates (black dotted arrow).

appears to be more abrupt in contrast with the potentiation, resulting in an asymmetry between the synaptic updating processes of potentiation and depression.

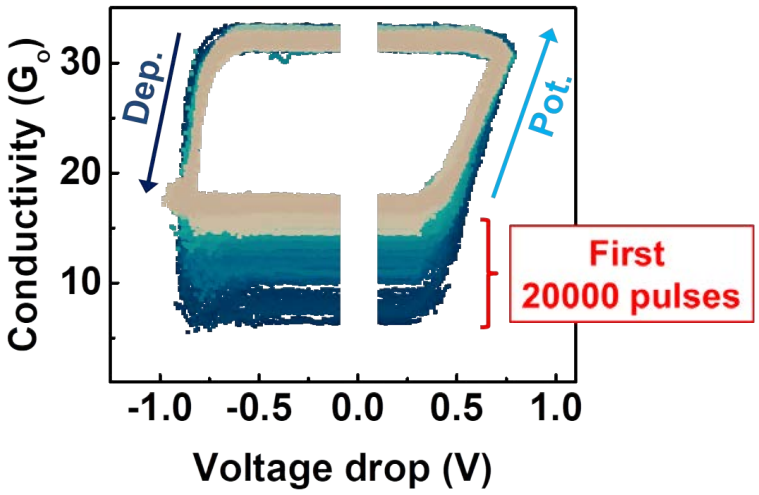

Figure 2.15: G-V characteristics of the tested device. The minimum value of the conductivity transient observed in the first 20000 pulses is indicated. The potentiation (Pot.) and depression (Dep.) processes occur as increments and decrements of the conductivity state, for increasing and decreasing pulse amplitude, respectively.

Concluding this sub-section, it has been proved that the conductivity state of the tested device can be tuned by means of modulating the amplitude of an applied pulse, being possible to potentiate (increase) and depress (decrease) the synaptic strength that the DUT would represent. Depending on the previous conductivity state, more or less voltage is required in order to induce a change in it. As observed in the G-V characteristics, it is possible to constraint the maximum and minimum values of the synaptic weight and to define a range of possible synaptic weight values. It is concluded that the tested devices are good candidates for the electronic implementation of an analog electronic synapse under a pulse-programming scheme [Conf5, Conf7, Art2], which is preferred in neuromorphic applications over the use of DC voltages.

4 G-V characteristics modeling

The G-V characteristics obtained by single-pulse characterization in the previous section provide a voltage-related conductivity state map of the DUT. It compiles graphically the information about how the conductivity state of the OxRAM device can be fine-tuned by means of modulating the voltage applied to it, when a pulse-programming scheme is considered. For neuromorphic applications, this conductivity state map represents the voltage-related synaptic weight updating rule of an analog synaptic device. Thus, its modeling supplies a simple methodology for calculating voltage-based analog conductivity state changes. Moreover, the experimental G-V characteristics also provide data related to the significant cycle-to-cycle variability observed in the previous characterizations, typical of the tested technology and often considered a drawback for its application. Therefore, it has to be taken into account when modeling the OxRAM behavior in both device and system-level simulations.

In this sub-section, the G-V characteristics are interpreted and modeled according to the time-independent compact model for non-linear memristive devices proposed in [71], where the G-V characteristics are referred to as hysteretic loops, or alternatively, hysterons. Statistical information from the model parameters is used to describe the observed cycle-to-cycle variability, so that its effects could be included in the device and system-level simulations described in the next sections of the thesis.

4.1 The hysteron model

According to the model of [71], the hysteron function (Figure 2.16) can be obtained from two logistic ridge functions, Γ^+ and Γ^-, identified as the SET and RESET ridge functions, respectively ($\Gamma^+(V) > \Gamma^-(V)$). These functions relate the conductivity state variable, λ, with the voltage drop, V, applied to the non-linear memristive device. The logistic ridge functions $\Gamma^\pm$ define the boundaries of the space Ω of possible conductivity states of the device, within a range limited by the minimum and maximum conductivity states, g_{min} and g_{max}, respectively. Moreover, $\Gamma^\pm$ represents the creation (+) or dissolution (-) of CFs. Summarizing, the principal concepts that this model leads to are the following: on one hand no conductive channel can be generated or destroyed if the applied voltage is insufficient to meet the required condition. On the other hand, if $\Delta V = 0$, nothing changes over time, since it is a conductance static model. In Figure 2.16, the state variable λ is depicted over the voltage drop V applied to the device. Assuming that λ_o is the initial conductivity state of the DUT, a minimum voltage is required in order to increase λ. In the example of Figure 2.16, this voltage corresponds to $V \approx 2V$. Voltage drops lower than this value imply a horizontal displacement of λ. Once the required condition is met, λ increases following the trajectory described by the ridge function $\Gamma^+(V)$ with increasing V ($dV/dt > 0$), eventually up to the g_{max} value. If one starts decreasing the applied voltage, an horizontal displacement within the Ω space towards $\Gamma^-(V)$ occurs. The required applied voltage as to decrease λ is the value corresponding to the intersection between the actual λ state and the $\Gamma^-(V)$ ridge function. At this point, λ decreases with decreasing V ($dV/dt < 0$), eventually reaching g_{min}.

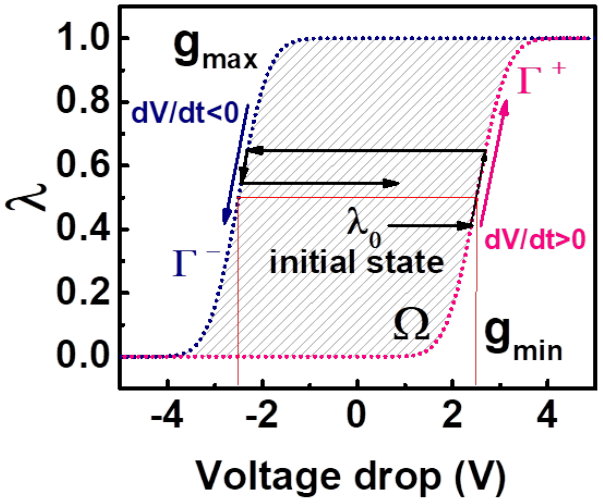

Figure 2.16: Hysteron model with logistic ridge functions Γ^+ and Γ^-. Ω is the space of feasible states S. Arrows indicate the typical piecewise evolution of the variable state λ inside Ω. λ_o is the initial state of the system.

In order to fit the experimental G-V characteristics in Figure 2.15 to the hysteron model, each of the 178 G-V curves were divided in two curves to be fitted to Γ^+ and Γ^-, for ($dV/dt > 0$) and ($dV/dt < 0$), respectively. The resulting 356 G-V characteristics were fitted to equation (2.1):

$$\Gamma^{\pm}(V) = g_{min} + \Big(g_{max} - g_{min}\Big)\left\{\frac{1}{2}\left[1 + erf\left(\frac{V - V^{\pm}}{\sigma_v^{\pm}\sqrt{2}}\right)\right]\right\} \tag{2.1}$$

Where erf(V) is the error function given in equation (2.2):

$$erf(V) = \frac{2}{\sqrt{\pi}} \int_0^V e^{-t^2} dt \tag{2.2}$$

The parameters involved in these equations are identified as the following: V is the voltage drop at the DUT, the average voltage values for the SET and RESET processes are V^+ and V^- respectively, their standard deviations are σ_V^+ and σ_V^-, respectively, and the conductivity extreme values for each G-V characteristic are g_{min} and g_{max}. The parameters V^+ and σ_V^+ are used when $dV/dt > 0$, while V^- and σ_V^- when $dV/dt < 0$. It is assumed that $d\lambda/dt = 0$ for $dV/dt = 0$.

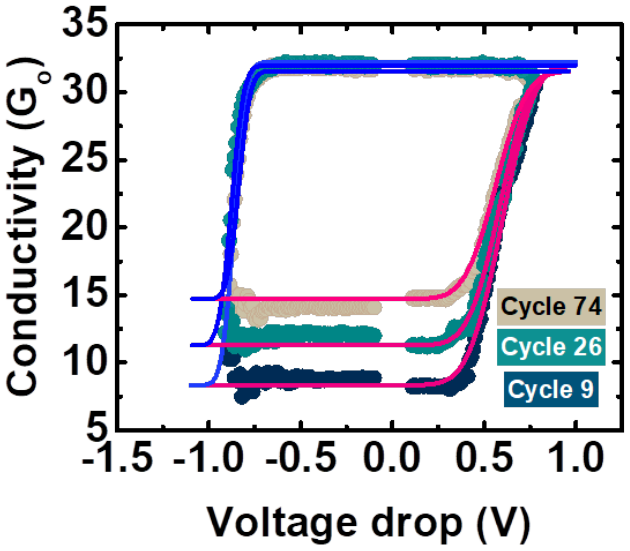

Figure 2.17: Examples of G-V curves fitted to the hysteron model, corresponding to cycle 9 (dark blue dots), 26 (green dots) and 74 (beige dots).

A total of 178 sets of the six fitting parameters V^+, V^-, σ_V^+, σ_V^-, g_{min} and g_{max} were obtained. Figure 2.17 shows a few of the fitted curves as examples, where the fitted $\Gamma^+(V)$ and $\Gamma^-(V)$ functions are depicted as magenta and blue lines, respectively, over the experimental data, for cycles 9 (dark blue dots), 26 (green dots) and 74 (beige dots). Note the good fitting of the experimental data to the hysteron model.

4.2 Analysis of the cycle-to-cycle variability

Since the OxRAM technology presents significant cycle-to-cycle and device-to-device variability, it is mandatory to investigate how it would affect the performance of a neuromorphic system. Whereas in biological neural systems, in which the neuromorphic community takes inspiration from, the variability is considered a sign of healthy neural and synaptic tissues, its impact on their learning execution is still a topic under research nowadays. There is not any hint about how the electronic devices variability could be beneficial or harmless for the hardware implementation of a neural network. In order to analyze and predict its effects, a statistical analysis of the model parameters is described in this subsection, which permits to model the electrical behavior of the tested samples considering the cycle-to-cycle variability. By means of simulation, it will be then possible to determine the neuromorphic system behavior when the intrinsic variability of memristive devices such as the tested ones is considered.

Fitting parameter	Average (without / with)	Standard dev. (without / with)
V^+	0.51996 / 0.54333	0.02424 / 0.03526
V^-	0.8326 / 0.84596	0.02478 / 0.02188
σ_V^+	0.14318 / 0.14272	0.00744 / 0.01064
σ_V^-	0.05857 / 0.05672	0.00935 / 0.00783
g_{min}	16.5754 / 14.3027	0.68417 / 2.93082
g_{max}	32.3396 / 32.3505	0.36068 / 0.363

Table 2.1: Average and standard deviation values of the fitting parameters of the hysteron model, considering all the data including the transient (right value), and the data after the 20000th pulse (without transient, left value).

The starting point is the data depicted in Figure 2.15, which was fitted to the hysteron model. The cumulative distribution functions (cdf) of each of the fitting parameters were obtained and are shown in Figure 2.18: **(a)** $V^{\pm}$, **(b)** $\sigma_V^{\pm}$, and **(c)** g_{min} and g_{max}. The cdfs of the data including the observed transient are depicted as white triangles, alongside the cdfs obtained when considering only the experimental data after the 20000th pulse (coloured circles), after the transient of the minimum conductivity value had occurred. In Table 2.1, the average and the standard deviation of each of these parameters are shown with the following format: "*not including data from the transient / including transient*".

This transient seems to affect mainly to two of the fitting parameters: the V^+ and the g_{min}. The upper tail of the V^+ distribution shifts towards the left if the data during the transient is not considered. In particular, most of the V^+ values are below 0.5V when considering the transient (gray triangles), instead of 0.6V. In the case of g_{min}, the lowest normalized values ($g_{min} < 0.3$) show significant dispersion if the data related to the transient is considered (gray triangles), in

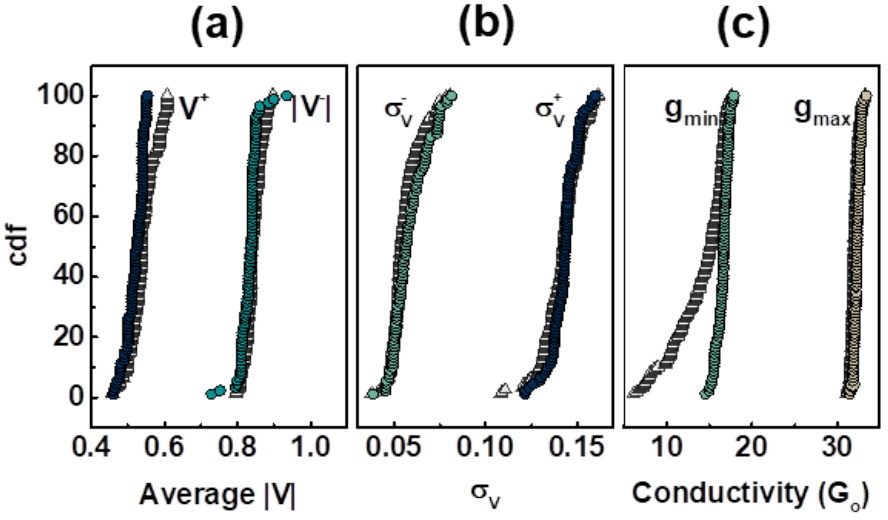

Figure 2.18: Cumulative distribution functions of the fitting parameters of the hysteron model, **(a)** the average voltage $V^{\pm}$ for the SET (V^+) and RESET (V^-) processes, **(b)** the standard deviation $\sigma_V^{\pm}$, **(c)** the normalized g_{min} and the normalized g_{max} values, considering all the data (white triangles), and the data after the 20000th pulse (colored symbols). The g_{min} values suffer a saturation around 0.3 (colored circles). The V^+ and the g_{min} parameters are displaying a significant change in its cdf if the transient is considered.

contrast with the data after the transient (green circles). This transient does not seem to affect to the rest of the fitting parameters, which do not present significant dispersion.

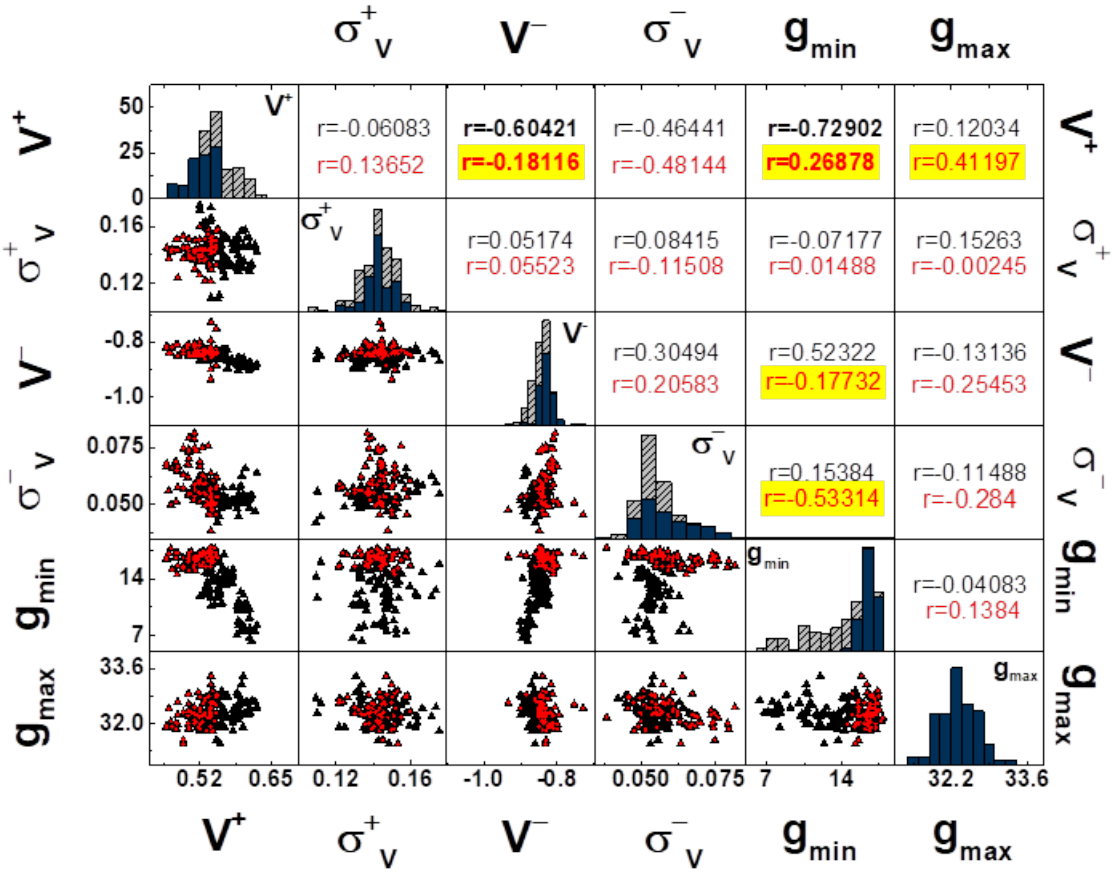

Figure 2.19: Correlation matrix of the fitting parameters. The elements under the diagonal are the obtained scatter plots, in black for the whole experimental data set, and in red for the reduced dataset. Within the matrix diagonal, histograms of the fitting parameters are depicted, in black and white bars (whole data set) and in colored bars (reduced set). Above the matrix diagonal, the Pearson correlation coefficients r are shown. The greatest correlation coefficients are written with a bold font (top value for the whole data set in black, and bottom value for the reduced one in red). The coefficients that suffered a significant change between both reduced and complete experimental data sets are highlighted in yellow.

Correlation between the used parameters was also analyzed for both experimental data sets. In Figure 2.19, the scatter plots are depicted below the matrix diagonal, and the Pearson r correlation coefficients are indicated above the diagonal (when considering all of the data, in black, and only data after the 20000th pulse, in red, respectively). Significant correlation indexes were observed between the average value of V^+ and V^- (Pearson r = âĹŠ0.604), and V^+ and g_{min} (Pearson r = âĹŠ0.729) if the whole set of experimental data is considered. However, the greatest observed correlation coefficients drop when the reduced data set is taken into account. On the other hand, an increase of the r coefficients between the average SET voltage V^+ and the g_{max} values, and between g_{min} and the standard deviation of the RESET voltage, σ_V^-, is also observed.

Histograms of all the calculated model parameters are located within the matrix diagonal (black and white dashed bars for the whole data set, and color-filled bars for the reduced data set), all of them sharing the same y-axis scale (from 0 to 50 counts). A decrease of the variability of V^+ and

g_{min} values can be noticed when the reduced data set is considered.

The greatest correlation coefficients observed after the transient are $| r | \approx 0.5$, suggesting a moderate linear relationship between these model parameters in the case of this DUT. Only the data of a DUT was analyzed in terms of correlation and further experiments oriented to study the relationship between the model parameters were not carried out during this thesis. Due to the lack of statistical data related to the correlations between model parameters, for simplicity, the obtained correlation data are not taken into account in the simulations performed during this research. This is mainly because the objective of these simulations does not consist on describing accurately the tested device's behavior, but to demonstrate and validate learning rules and algorithms on systems based on them, as a first step towards the implementation of neuromorphic architectures.

The performed cycle-to-cycle variability modeling of the DUT allows to investigate its impact on a neuromorphic system through simulation, without the need of manufacturing it [Conf5, Conf7, Art2]. An example is provided in chapter 5, where the cycle-to-cycle variability impact on the performance of an electronic self-organizing neural network performing a color classification task was evaluated by system-level simulations [Conf4, Conf6].

Chapter 3

Bio-inspired device-level learning processes

1 Introduction

A local learning process rule has the objective of adjusting the synaptic weights, which represent the strength of a connection between two neurons, according to some features of the input data set to be learned in an iterative manner. It is used as a method, usually repeated all over the neural network. In the frame of neuromorphic computing, the local learning process can be thought as a way to change the electrical parameter of the employed synaptic device, identified as its synaptic weight. In the case of the present thesis, it corresponds to the conductivity state of the tested OxRAM devices. This chapter is focused on bio-inspired device-level learning processes for analog synapses. Bio-inspired stands for the following fact: the studied learning methods show some similarity or analogy with actual biological processes, regardless if the original mechanisms affect at the local neural circuitry level, or in a systemic way, thus affecting simultaneously large areas. In particular, inspiration is taken from the Spike-Timing Dependent Plasticity (STDP) [72], and from the classical Pavlovian conditioning from psychology [73]. The studies exposed in this chapter are based on experimental measurements performed on the OxRAM devices tested in chapter 3, where the fulfillment of the analog synaptic device requirements was demonstrated.

The first section of the present chapter is related to the STDP rule, consisting in the time-dependent adjustment of the synaptic weight of an individual synaptic device. An introduction explaining its concept and a brief review from other works within the neuromorphic engineering community is provided. The objective of this section consisted in demonstrating the STDP induction in the tested devices. The experimental STDP measurements are detailed, and the data is modeled according to the hysteron model of the tested technology, which was exposed in the previous chapter.

The second section provides a basis for the implementation of associative learning in neuromorphic architectures, thus requiring at least two synaptic devices for its investigation. An introduction to associative learning is first given, with the aim of highlighting the impact of its application on neuromorphic computing systems. In this case, the following experimental measurements are made simultaneously in two dependent OxRAM devices, in which a classical conditioning test is carried out, emulating the Pavlov's dog experiment from psychology.

2 Spike-Timing Dependent Plasticity (STDP)

2.1 Introduction

In this section, the STDP property of the tested OxRAM devices is studied. The STDP is a bio-inspired local learning rule widely employed in the artificial neural networks training, especially when unsupervised learning schemes are considered, which has been transferred to the neuromorphic engineering research field. It takes inspiration from the actual biological STDP, which is a physiological mechanism for synaptic strength adjustment observed in biological in vitro [74] [75] [76] and in vivo [77], [78] and [79] neural tissues. Summarizing, the STDP rule relates the increment and decrement of the synaptic weight or strength, referred to as synaptic potentiation and depression respectively, with the temporal correlation found between the pre and post-synaptic neuronal activities, which usually corresponds to the order and temporal interval between spiking events of the involved pre and post-synaptic neurons.

In cognitive neuroscience, the spike timing is nowadays considered as one of the main several factors contributing to synaptic plasticity induction [72], in the sense that the strength of a synaptic link between two neighboring neurons depends on its history, concretely by the overall amount of neurotransmitters that has been propagated through it after a relevant neural spike [51] (Figure 3.1.a). The biological STDP mechanism does not rely only on the spike timing, but also on the firing rate, synaptic cooperativity and the neuron depolarization process [72]. Meanwhile, in the neuromorphic computing context, the STDP is simplified to the property of artificial synapses to change their strength according to the precise timing of individual pre and post-synaptic spikes. The benchmark consists in reproducing the experimental STDP results reported in biology, for which an example from [75] is depicted in Figure 3.1.b. In here, the canonical STDP function is displayed, where the relative change of the synaptic strength measured experimentally from biological tissues is plotted over the relative timing $\Delta t = t_{post} - t_{pre}$, indicating the difference between the arrival time t_{pre} of a pre-synaptic spike in the synaptic cleft found between two neurons, and the time t_{post} where the post-synaptic neuron has generated a post-synaptic spike (Figure 3.1.a). Basically, the canonical STDP function of Figure 3.1.b indicates that for the induction of a positive synaptic change (potentiation), a positive Δt is required, whereas a decrease of the synaptic strength (depression) occurs for negative Δt.

This STDP function actually follows the causality principle: if the post-synaptic neuron spikes after the arrival of a pre-synaptic spike, then the connection between the post-synaptic neuron and the recently-activated pre-synaptic neurons is strengthened. On the other hand, if the post-synaptic spike precedes a pre-synaptic spike, then that particular pre-synaptic neuron has not presumably contributed to the post-synaptic neuron generation of the post-synaptic spike, hence their connection is weakened. Moreover, the magnitude of the change increases for shorter Δt, i.e. for higher time-correlation between the pre and post-synaptic events. If the induced change lasts over time, then the updating process is referred to as long-term potentiation (LTP) or depression (LTD), whereas if the synaptic update consists on a transient modification, then it is called short-term potentiation (STP) or depression (STD).

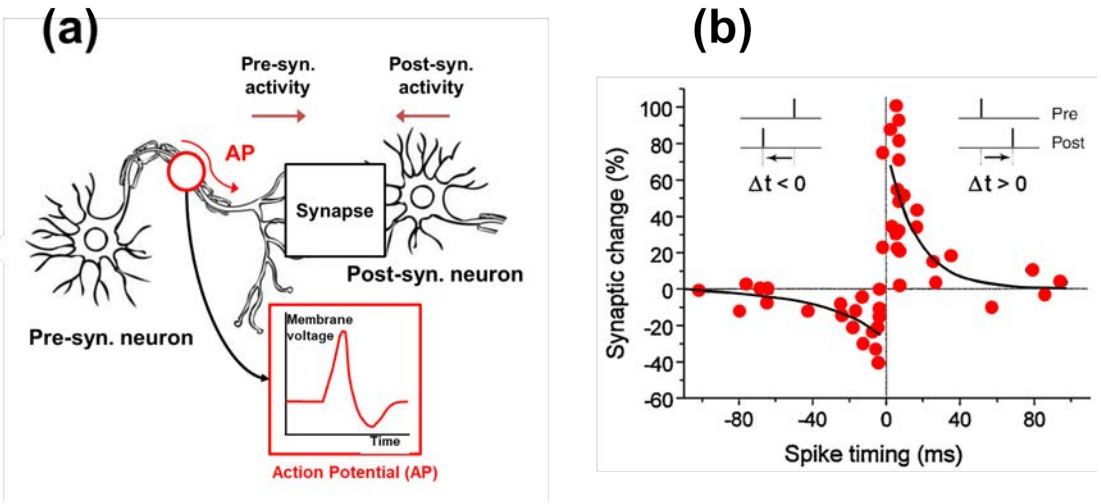

Figure 3.1: **(a)** Representation of two neurons and its synapse. The pre-synaptic neuron initiates a synaptic event by generating an action potential, which stimulates the release of chemical substances (neurotransmitters) in the synapse region (synaptic cleft). The post-synaptic neuron can be depolarized if it is sensible to this neurotransmitters. If the depolarization is large enough, the post-synaptic neuron will also fire an action potential. According to the STDP property, if there is some temporal correlation between the pre and post-synaptic neuron activities, then its connection (synaptic weight) will be modified. **(b)** Canonical STDP function reported in biological studies (adapted from Bi and Poo , 1992, [75]). For $\Delta t < 0$, synaptic depression (relative decrement of the synaptic weight) is induced, whereas for $\Delta t > 0$, potentiation occurs (relative increment of the synaptic weight).

The interest in implementing the STDP rule in electronic synaptic devices has grown exponentially over the last years, mainly because it is one of the most popular learning rules employed in unsupervised learning schemes, which are discussed in chapter 5. The first electronic implementations of STDP were purely based in CMOS technology, being very expensive in terms of the number of required devices and power consumption, in contrast with the employment of memristive devices, with just one memristor per synapse, often combined with CMOS neurons [51] [80] [81], [15] [81] [55] and [82]. Nowadays, the implementation of the electronic neuron still relies on CMOS chips [83][84] [85] and [86], yet the proposals of memristor-based neurons are arising due to the memristive devices dynamics resemblance to neuron dynamics, their inherent stochasticity and better size and scalability [87] [88] [89] and [90]. In any case, as discussed in chapter 2, the memristor is extensively studied as a synaptic device, whose conductivity state is identified as the synaptic strength between two electronic neurons. The neurons are meant to be able to trigger the proper electrical signals towards the electrodes of the memristive device, in order to induce a change in its conductivity state, according to the codification of the input data set to be processed by the neural network. In the case of STDP, the electronic synapse weight update is expected to be dependent on the time-delay, Δt, between the pre and post-synaptic spikes.

The canonical STDP function of Figure 3.1.b has been reproduced mostly in PCM and OxRAM technologies by means of modulating the pulse amplitude according to a certain Δt [91] [54] and [26]. It is worth highlighting that the variation of Δt actually implicates the modification of the voltage waveform to be applied to the memristor, so it is the actual voltage drop waveform at the electronic synaptic device which induces a certain conductivity change [18-20]. As stated above, if the STDP property is demonstrated in an electronic synaptic device, an unsupervised learning algorithm can be further applied to a neuromorphic system based on such devices, as detailed in chapter 5. In order to do so, the STDP property of the devices which were tested and modeled in the previous chapter is experimentally verified and analyzed in the following subsection.

2.2 STDP experimental measurements

In this subsection, the experimental measurement procedure focused on demonstrating the STDP property in the tested OxRAM devices is detailed. The performed tests shared the same scheme, depicted as a flow diagram in Figure 3.2, involving the use of an individual OxRAM sample and a semiconductor parameter analyzer Agilent4156C (SPA). First of all, a forming stage was carried out, employing an I_c=0.5mA (Figure 3.2.a). Then, a resistive switching cycle consisting on the induction of a RESET, followed by a SET process, was performed (Figure 3.2.b). As explained in chapter 3, the resistive switching cycle permits to set the conductivity state of the tested device within a particular narrow range of conductivities. The obtained conductivity state was indirectly measured by means of applying a voltage ramp up to 0.1V (Figure 3.2.c), and is referred to as the initial conductivity of the experiments, g_{init}. Then, a voltage waveform, corresponding to a particular Δt, was applied (Figure 3.2.d). Lastly, the conductivity state of the device after the application of the voltage waveform, g_{fin}, was measured (Figure 3.2.e), and the test restarted at the resistive-switching cycle test (Figure 3.2.b). This test scheme ensured that, for each of the obtained points of the experimental STDP function, the previous history of the tested device was removed by the RESET process, and that the g_{init} value prior to obtaining a STDP function data point was similar, so that the impact on the relative synaptic weight change (i.e. the relative conductivity change) was mainly due to the applied voltage waveform, hence to the variation of Δt.

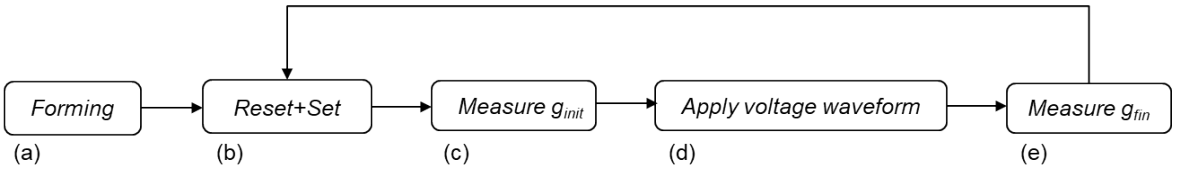

Figure 3.2: Flow diagram of the performed test.

The applied voltage waveform related to Δt consisted in an equivalent voltage drop waveform (referred to as V_{drop}), which was applied to the top electrode of the tested device, whereas its bottom electrode was grounded (Figure 3.3.b). The V_{drop} waveform is the actual voltage drop caused by the overlap of the pre (V_{pre}) and post-synaptic (V_{post}) spike waveforms meeting at the terminals of the electronic synapse (Figure 3.3.a). The resulting voltage drop is defined as $V_{drop}=V_{post}-V_{pre}$, whereas $\Delta t=t_{post}-t_{pre}$, where t_{pre} and t_{post} are the times in which the maximum values of the pre and post-synaptic spikes occur, respectively. The shape of the employed pre and post-synaptic pulses resemble the action potential generated by biological neurons (Figure 3.3.c), which is the signal travelling through the neuron axon finally triggering the release of neurotransmitters to the synaptic juncture, enabling the information transmission between the involved neurons. The time-scale of V_{post} and V_{pre} is set to be in the order of seconds, as to acquire precisely the current evolution when the voltage drop waveform V_{drop} was being applied, so that a first experimental approach for understanding the STDP rule induction on the tested devices could be performed. According to the set time-scale of V_{drop}, the induced STDP will present a spike-timing scale in the order of seconds, whereas in biology, it is in the order of tenths of milliseconds (Figure 3.1.b).

Then, the pre and post-synaptic spikes consist in identical bipolar triangular waveforms in terms of spike amplitude and spike-width. The triangular waveform allows naturally increasing (decreasing) the pulse amplitude of the resulting voltage drop at the electronic synapse, according to the previously defined Δt, with the cost of also modifying its duration. However, as seen in the third chapter, the pulse amplitude dominates over the pulse-width as the main pulse parameter allowing the control of the conductivity state of the tested devices, regardless of the pulse polarity. Therefore, in order to induce a change in the conductivity state of the device as to implement the STDP rule, the maximum and minimum voltages of the synaptic spikes have to be chosen according to the voltages required for inducing a SET and a RESET process, which in the case of the tested samples range between |0.36|V and |0.68|V. An example of the I-V characteristics of the tested devices is

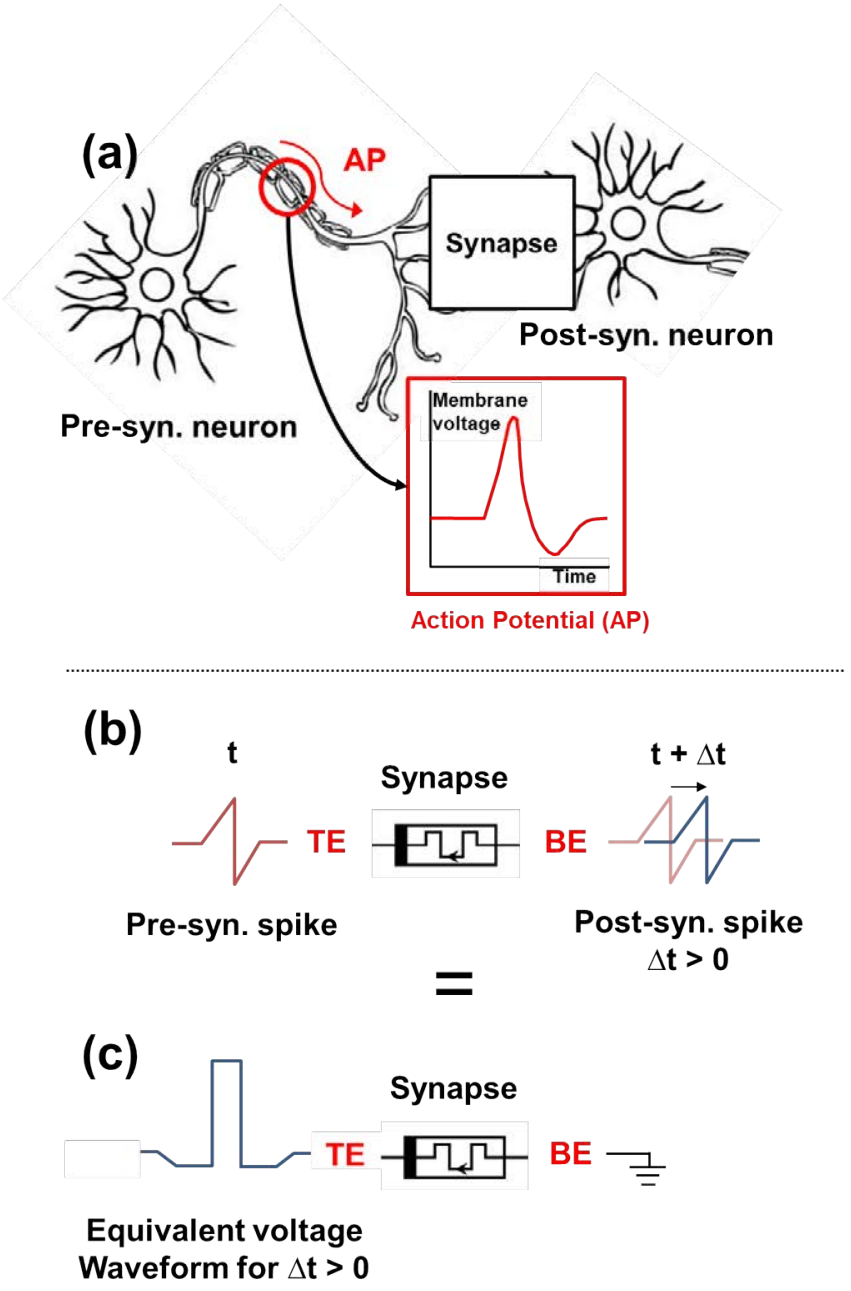

Figure 3.3: (a) Schematic of a biological synapse between two spiking neurons. The synaptic role is played by the DUT, whereas the pre and post-synaptic neurons spikes are not applied to the top and bottom electrodes of the sample. Instead, the resulting V_{drop} for a certain Δt is applied to the top electrode of the DUT, whereas the bottom electrode is kept grounded. (b) Schematic of the electronic synapse, in which the pre and post-synaptic spikes resembling the biological action potential meet with a certain delay, causing a voltage drop waveform whose shape depends on Δt. (c) Schematic of the actual performed measurement, where the equivalent voltage waveform is applied to the top electrode of the tested sample, whereas the bottom electrode is grounded.

shown in Figure 3.4. In Figure 3.5, the considered V_{pre} and V_{post} and the resulting voltage drop V_{drop} waveforms are depicted, for $\Delta t > 0$ (Figure 3.5.a) and for $\Delta t < 0$ (Figure 3.5.b). As seen there, a positive Δt implies that the maximum voltage in absolute value applied to the sample, $| V_{max} |$, has a positive polarity, for which an increase of the conductivity state is expected (i.e. potentiation of the synaptic weight, LTP), whereas for a negative Δt, it has negative polarity, for which the conductivity state of the device should decrease (depression of the synaptic weight, LTD).

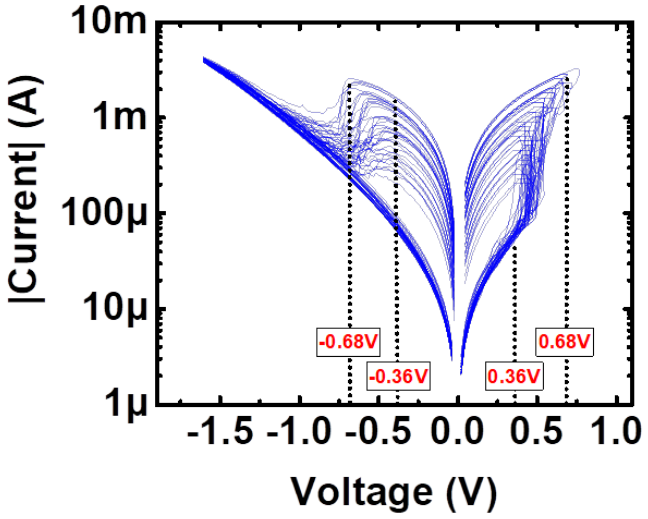

Figure 3.4: Examples of experimental I-V characteristics of the tested devices. The range of voltages required for the induction of the SET and RESET processes are indicated.

The evolution of the current flowing through the tested device during the application of the equivalent voltage drop waveform is depicted in Figure 3.6, where one example for LTP (Figure 3.6.a) and one for LTD (Figure 3.6.b) are shown for two particular time delay values: Δt=65s and Δt=-31s, respectively. The voltage waveforms (V_{drop} are also plotted. The applications of the reading voltage for the calculation of g_{init} and g_{fin}, corresponding to the stages (c) and (e) of the flow diagram of Figure 3.2, at the beginning and ending of each test are also represented. In the case of LTP, $g_{init} = 17.43G_o$ and $g_{fin} = 18.23G_o$. In the case of LTD, $g_{init} = 13.74G_o$, and $g_{fin} = 11.08G_o$. These changes in the conductivity of the device related to the STDP are further indicated as the relative conductivity changes, $\Delta g/g_{init} = (g_{fin} - g_{init})/g_{init}$, and are of $\Delta g/g_{init} = 4.5\%$ for LTP, and of $\Delta g/g_{init} = -19.36\%$ for LTD. It can be observed that for shorter $|\Delta t|$, the magnitude of the maximum voltage applied to the sample increases in absolute value ($| V_{max} |$), being in the case of the LTP, V_{max}=0.5V, corresponding to Δt=65s, and in the case of LTD, $| V_{max} |$=0.576V, corresponding to a time delay of Δt=-31s. On the other hand, the current increases and decreases potentially during the application of $| V_{max} |$.

In order to study the STDP function of the tested device, the test scheme of Figure 3.2 was performed for different Δt values, giving rise to different $| V_{max} |$ values. The Δt value was varied randomly over the tests. Each of the obtained data points corresponds to a different test performed on the same sample, with a similar g_{init} value obtained by means of employing I_c=1mA during the stage (b) of the tests. The distribution of the obtained g_{init} values is depicted as a histogram in Figure 3.7.a, in G_o units, where the average value is also indicated. In Figure 3.7.b, the induced STDP function is depicted. In here, the relative conductivity change over the value of g_{init} is plotted against Δt, where the average of the data is also included as a dotted line, revealing a shape similar to the canonical STDP function's one (Figure 3.1.b).

The same test was carried out for four different g_{init} values, in order to study the impact of this

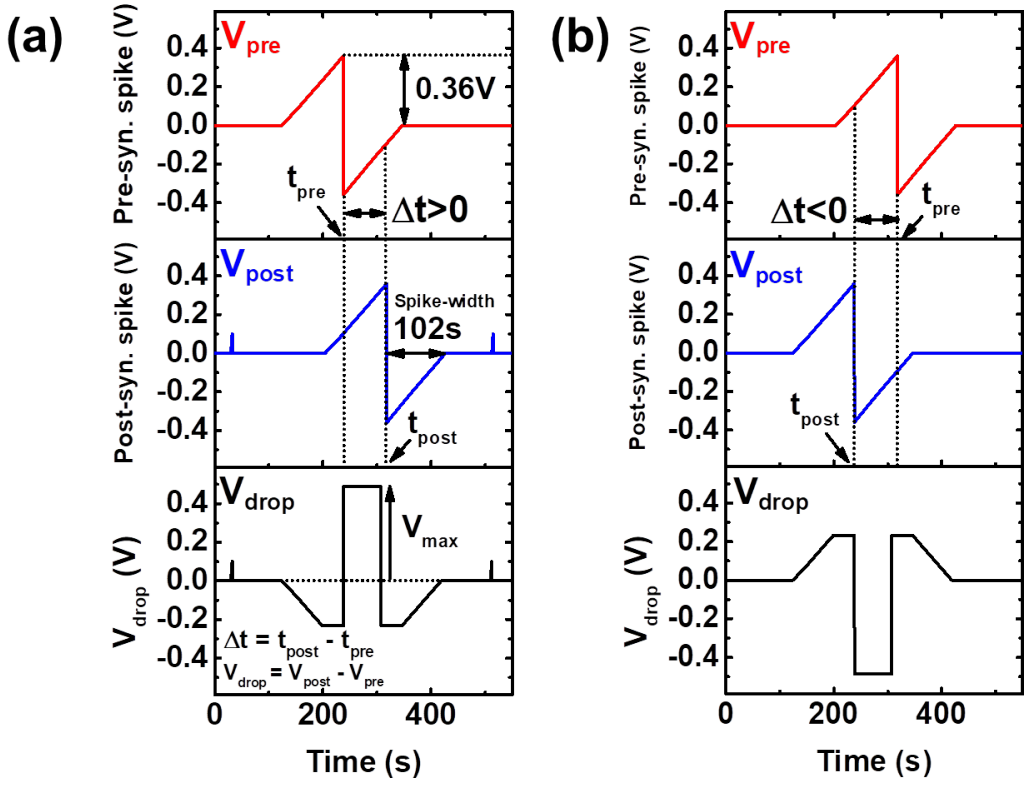

Figure 3.5: Pre-synaptic (V_{pre}), post-synaptic (V_{post} pulses and resulting voltage drop ($V_{drop} = V_{post} - V_{pre}$)plottedfordifferent$\Delta t$: **(a)**$\Delta t > 0$.**(b)**$\Delta t < 0$.Thevaluesofthespikeamplitudeandspikewidthen

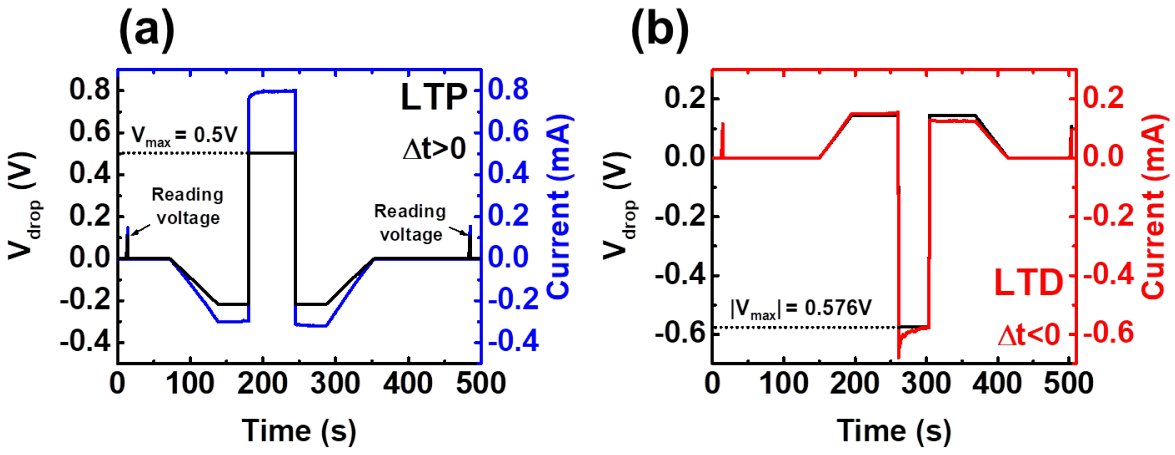

Figure 3.6: Evolution of the current through the tested devices during the application of the voltages corresponding to steps **(c)-(d)-(e)** of the test (reading-equivalent synaptic voltage drop-reading), for the **(a)** LTP and **(b)** LTD processes.

parameter on the STDP function shape. The g_{init} parameter was changed by means of setting the I_c current to: I_{c1}= 0.75mA, I_{c2}= 1mA and I_{c3}= 1.25mA. The histograms of the g_{init} values (in G_o units) for all of the cases can be found in Figure 3.8.a, whereas in Figure 3.8.b, the experimental STDP functions are presented.

As seen in Figure 3.8.a, for increasing I_c, the g_{init} values increase, in accordance with the results of

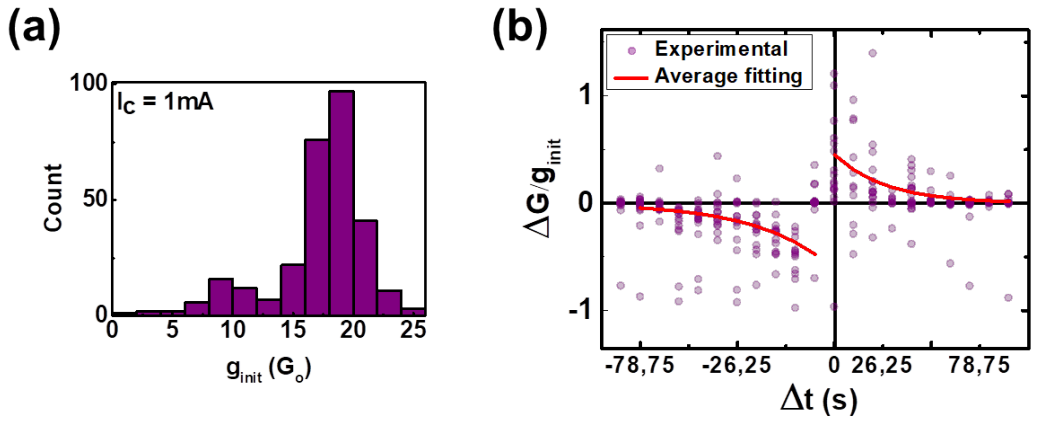

Figure 3.7: **(a)** Histogram of g_{init}, obtained when I_c=1mA was set during the initialization process from Figure 3.2.b. **(b)** STDP function of the tested device, where the relative conductivity change over the g_{init} value is plotted against Δt. The experimental data are represented as purple dots, whereas the average value is depicted with a dotted line.

chapter 3. The STDP functions shown in Figure 3.8.b show similarity with the biological STDP function (Figure 3.1.b) in terms of shape and cycle-to-cycle variability. For I_c=0.75mA, the greatest relative synaptic update is in average of $|\Delta G/g_{init}| \approx 0.25$ for $\Delta t > 0$, whereas for $\Delta t < 0$ is of $|\Delta G/g_{init}| \approx -0.4$. In the case of I_c=1.25mA, the highest magnitude of the relative conductivity change is in average of $|\Delta G/g_{init}| \approx 0.25$, corresponding to the smallest $|\Delta t|$, which is still a significant synaptic update. The impact of g_{init} on the STDP function of the tested device consists in the following: for higher values of g_{init}, the magnitude of the relative change is smaller, suggesting that the employed voltages should also be scaled up in magnitude with g_{init}, as observed in the G-V characteristics of the tested samples. The obtained relative conductivity changes indicate that the final conductivity values can double their previous g_{init} values for the smallest $|\Delta t|$ when also considering the smallest tested I_c, i.e. when g_{init} is smaller.

The different tested initial conductivity state values, ranging from $10G_o$ up to $20.7G_o$, affect to the STDP function shape in the sense that, for increasing g_{init}, a smaller relative change of the conductivity is observed. An interpretation with the hysteron model is given in Figure 3.9, where the impact of g_{init} on the LTP part of the STDP function is explained for two different values of g_{init}, being higher in the case of 3.9.b. In both Figures, an example of the G-V characteristics of a tested device are depicted. Two different Δt are considered, being $\Delta t_1 > 0$ and $\Delta t_2 \sim 0^+$. These time delays correspond to the application of different voltage drops to the device, being higher in the case of Δt_2, since it is a shorter delay. Assuming that the applied pre and post-synaptic waveforms are the same in Figure 3.9.a and 3.9.b (that is, the same voltages are employed in both cases), in both cases, a larger voltage drop implies a higher conductivity change ΔG (if $\Delta t_1 > \Delta t_2$, then $\Delta G_1 < \Delta G_2$). Finally, if a larger g_{init} is considered (3.9.b), then the obtained ΔG is smaller for any of the Δt values, being finally reflected in the $\Delta G/g_{init}$ values. Concluding, higher voltages should be employed for higher initial conductivity values in order to induce the same change in the conductivity state, as the G-V characteristics suggest. The results demonstrate that the canonical STDP rule can be induced in the tested devices by playing with the temporal delay between the pre and post-synaptic spikes, since it implies a modulation of the magnitude of the voltage drop seen by the tested device, being inversely proportional to $|\Delta t|$. Any of the tested initial conductivity values allow implementing an STDP function similar to the one reported in neuroscience, in terms of magnitude of the relative synaptic weight change and variability.

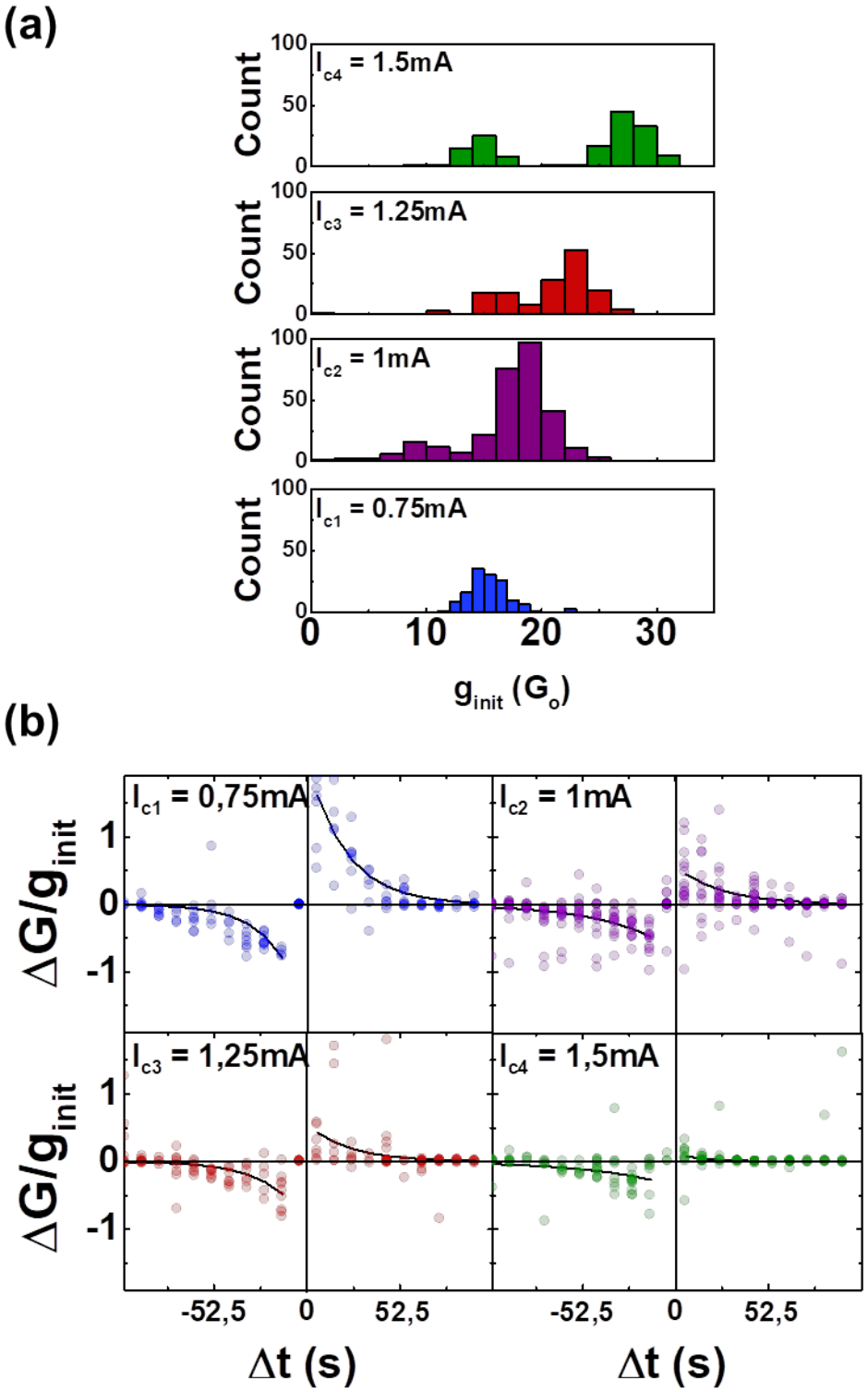

Figure 3.8: **(a)** Histograms of the tested g_{init} values, where the average value is also indicated, for I_{c1}=75mA, I_{c2}= 1mA and I_{c3}= 1.25mA. **(b)** STDP functions of the tested device for different g_{init} values (in G_o units), corresponding to I_{c1}=75mA, I_{c2}= 1mA and I_{c3}= 1.25mA. The averages are depicted as dotted lines.

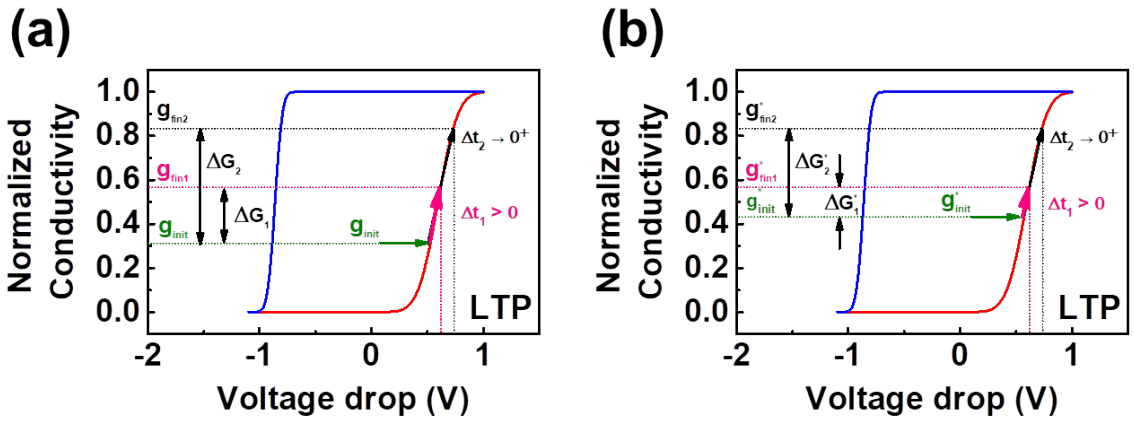

Figure 3.9: Impact of g_{init} on the STDP function for two cases of Δt. **(a)** In the first case, taken as the reference, Δt_1 is larger than Δt_2, which results in a larger ΔG_2 since the corresponding applied voltage drop is larger. **(b)** If g_{init} is larger, then for the same Δt values, the induced changes in the conductivity state are smaller in magnitude.

The performed experiments in this section provided the basis for studying this local learning rule in the tested devices. A reproduction of the test presented in this section and carried out with the same devices can be found in [92], where the STDP functions were obtained for different time scales of the spike-width, ranging from hundreds of nanoseconds up to milliseconds. The experimental STDP measurements were obtained by means of applying identical pre and post-synaptic waveforms with a determined spike-width and a spike amplitude of $\mid 0.7V_{peak} \mid$, which are shown in Figure 3.10.a. Figure 3.10.b shows three examples of experimental STDP induced to the same device, with pre and post-synaptic spikes with different spike-width time-scales: for 1ms, 1μs and 10μs.

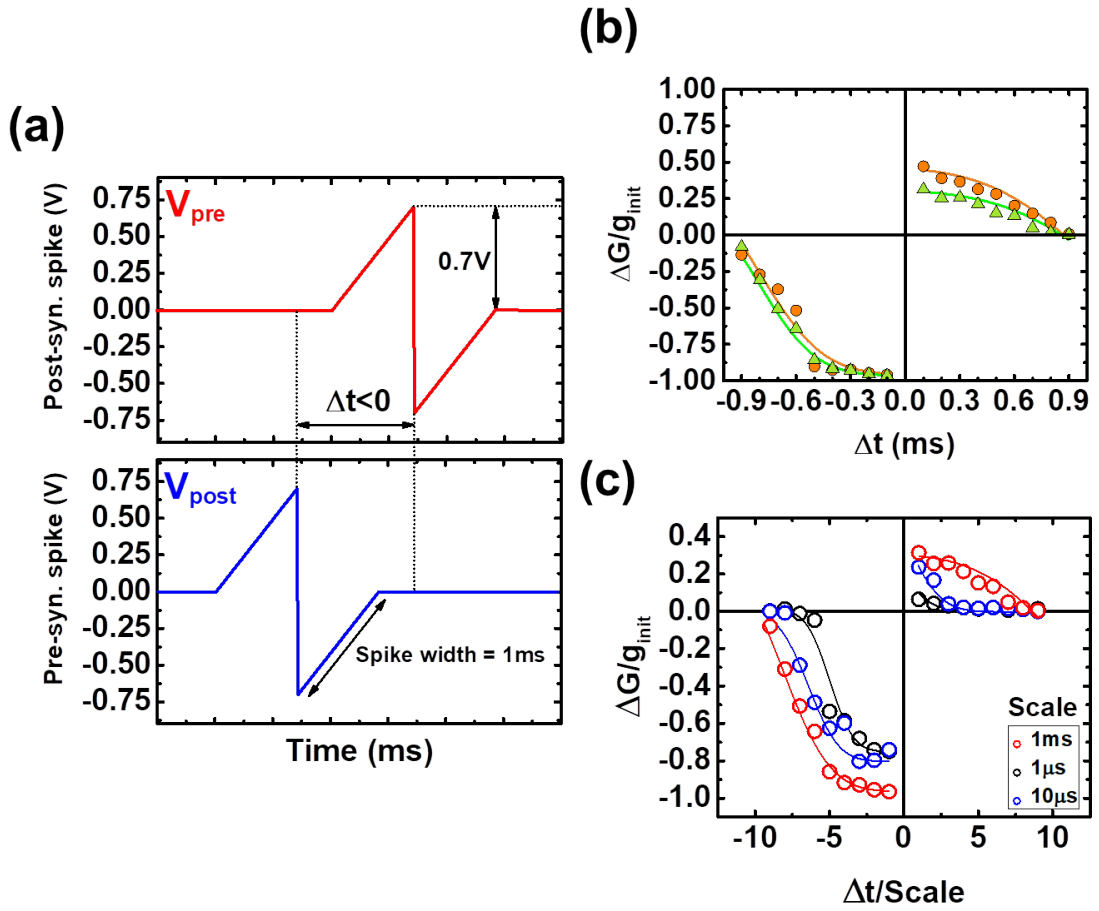

Figure 3.10: **(a)** Pre and post-synaptic waveforms used in [92]. Experimental data from [92]. In particular, **(b)** two examples of STDP functions induced to the same device with a spike-width of 1ms are shown. **(c)** three examples of STDP functions from the same device for different spike-widths are shown: 1ms (red), 1μs (black) and 10μs (blue). The fittings using the G-V characteristics model are depicted as lines.

In here, a bias towards synaptic depression is observed: a higher relative conductivity change is observed for the LTD and for similar $\mid \Delta t \mid$. This biasing is related to the asymmetry in the G-V characteristics, as the one that can be observed in Figure 3.9, where it can be seen that the RESET process is more abrupt than the SET process, and requires a higher voltage drop. It can also be seen in Figure 3.10.b that the STDP functions overlap for $\Delta t < 0$. In general, this overlapping occurs for all of the tested time-scales [92]. Also, saturation of the synaptic weight update is observed for small and negative Δt. It is suggested that both overlapping and saturation of the relative synaptic weight change functions are due to the RESET process being more abrupt than the SET process, so that the dependence of ΔG with Δt is lost for $-0.5\text{ms} < \Delta t < 0\text{ms}$. Because the overlapping is not observed for positive Δt, it is suggested that the tested device G-V characteristics are asymmetric, being the RESET process more abrupt than the SET process, as shown in Figure 3.9. The implication of this asymmetry of the STDP curves in a neuromorphic system is further discussed in chapter 5. Lastly, in [92], it is concluded that in the tested devices, the time-scale of the spike-width does not significantly affect the shape of the obtained STDP functions, in terms of the relative conductivity change, nor variability.

Finally, the STDP curves shown in Figure 3.10.b were fitted using the G-V characteristics model provided in chapter 3 (shown in Figure 3.10.b as lines). In order to do so, the employed voltage waveform from [92] is used as the input of a device simulator, which computes the conductivity

change of the simulated device, according to the model parameters of the G-V characteristics of the device. The goodness of the fittings validates the hysteron model, proving that it is suitable for describing the learning rules in the devices under study. In the following chapter, the G-V characteristics model is used within a simulation in which the STDP is considered as the local learning rule in an unsupervised learning algorithm, which is applied to a neuromorphic system based on the tested devices.

Summarizing the results of this section as to conclude, the STDP canonical function has been reproduced in the tested OxRAM devices, by means of applying identical triangular waveforms as the pre and post-synaptic spike. It has been shown that the initial conductivity state of the devices affects the magnitude of the relative change of the synaptic weight. It is suggested that the asymmetry, saturation and overlapping of the STDP functions for $\Delta t < 0$ is due to asymmetry in the G-V characteristics of the synaptic devices, being the RESET process more abrupt than the SET process. Results from [92] suggest that the relative conductivity change does not depend on the employed time-scale. This time-independence permits to use the hysteron model to fit the STDP data. The goodness of the fittings validates the model, in the sense that it can be used to simulate the device behavior when a local learning rule such as the STDP is considered. The tested devices are then suitable to be used as synapses in a neuromorphic system in which an unsupervised learning scheme is meant to be applied.

3 Associative learning

3.1 Introduction

As stated in the previous section, unsupervised learning rules such as the STDP, which rely on the dependences of plasticity on time or frequency correlations between the pre and post-synaptic activities, have been already proven in single electronic devices in a variety of memristive technologies [6] [51] [24] and [25]. However, there is still a lack of understanding on how bio-inspired local learning rules should be designed when the interaction between two or more memristors is considered. In the biological brain, complex cognitive processes arise from associative learning mechanisms, involving the causal interaction between multiple neuronal layers, and thus, of a large amount of synapses. Therefore, the study of associative learning between electronic synapses would suppose a step towards the implementation of neuromorphic associative memories and hierarchical computing networks, able to store and recall symbolic knowledge, as occurs in the mammalian neural system.

A simple case of associative learning can be found in the classical conditioning experiments initially conducted by I. Pavlov [73]. In classical conditioning, two stimuli are considered: one is the so-called unconditioned stimulus (US), and the second is the neutral stimulus (NS). The US triggers a response of the system, labeled as the unconditioned response (UR). On the other hand, the NS does not provoke the UR. It is through a stage of conditioning in which the NS is associated to US, so that the NS becomes a conditioned stimulus (CS), generating a system response similar to the UR. The experiment that Pavlov carried out was actually with dogs: the US was the sight of food, which made the dogs salivate (UR). The NS that Pavlov employed was the ringing of a bell, which was neutral to the dogs in the sense that, only with its presence no salivation was induced. Pavlov discovered that, by consecutively ringing the bell when feeding the dogs, they would start responding similarly to both US (food) and NS (ringing of the bell), the latter becoming a CS. That is, they would salivate when hearing the bell without the presence of food, because the dogs associated it with their feeding time. This finding had great implications, being today the basis of the associative learning theory.

In this section, a potential basis for implementing unsupervised associative learning in two or more memristors within neuromorphic architectures is presented. The experimental demonstration is carried out by means of emulating the Pavlov's dog classical conditioning experiment with two OxRAM devices, in which the dependence of the probability of association on test parameters, such as the pulse amplitude, is studied.

Electronic emulations of classical conditioning and Pavlov's dog test have actually been carried out with memristive devices, either using a single partially-volatile device [93], a single non-volatile device [94] [95], or a pair of volatile organic transistors with discrete CMOS neurons, being the latter focused on the implementation of a short-term associative memory [96]. In this thesis, an unsupervised electronic setup for studying a basic process of associative learning is proposed, involving the use of a pair of non-volatile OxRAM devices, and being the test scheme analogous to the original Pavlov's dog experiment. The results are analyzed by establishing a probabilistic association criterion. This is motivated by, on the one hand, taking into account the variability found in memristive technologies such as OxRAM, which is often considered as an issue, and was already observed in chapter 3 in the case of the tested devices. On the other hand, significant variability is also found in biological neural and synaptic populations, as well as in their plasticity property, yet this variability is thought to be a typical (and maybe necessary) feature for a healthy nervous system [97] [98] and [99]. This is the main reason for which statistical methods and models have been successfully incorporated to the computational neuroscience research during the last decades [100]. Therefore, it is plausible to design probabilistic learning rules for their application in neuromorphic architectures considering the variability observed in the devices to be employed.

3.2 Emulating Pavlovian conditioning with OxRAM devices

A scheme of the employed characterization setup for implementing associative learning is shown in Figure 3.11.a. In here, two OxRAM devices with 5x5μm^2 area represent the synaptic connection (S1, S2) between two pre-synaptic sensors and a post-synaptic neuron (POST), which S1 and S2 have in common. The signals coming from the sensors are identified as V_1 and V_2, which are the inputs of the system, and share the same amplitude value, V_d. On the other hand, V_3 represents the feedback signal triggered by the POST, and provides also a way to measure the response of the POST. All of the employed signals were applied with a semiconductor parameter analyzer (SPA) Agilent4156C. In Figure 3.11.b, pictures of the probe-station setup are shown.

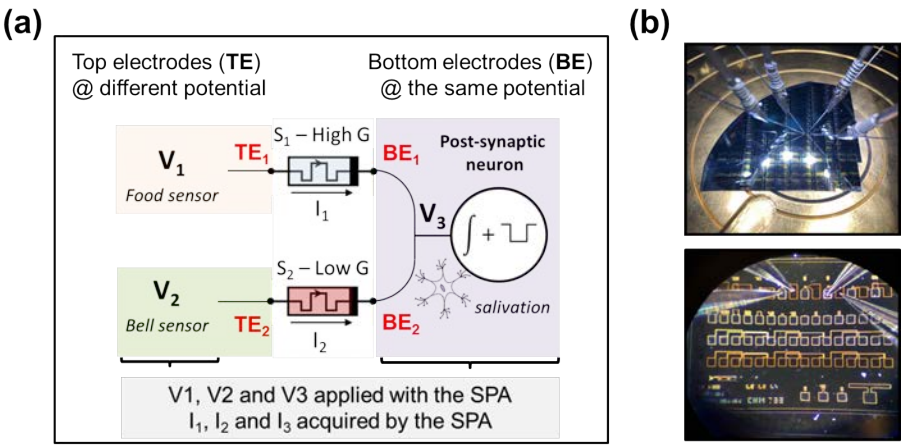

Figure 3.11: **(a)** Scheme of the experimental setup for the electronic Pavlov's dog experiment. V1 and V2 are the input signals of the system, connected to the post-synaptic neuron via two OxRAM devices, S1 and S2. Initial conditions for the two samples are also displayed, being S1 at a high conductivity state, whereas S2 has a low conductivity state. **(b)** Pictures of the probe-station setup.

The smart control of the SPA was employed for emulating the POST as an integrate-and-fire neuron, whose behavior consists on the following processes: the neuron starts accumulating the charge it is receiving from multiple synaptic transmissions. The accumulation of charge depolarizes the neuron, increasing its membrane potential, which is related to the difference between the charges located in the interior and exterior of a biological neuron. This depolarization process is often modeled as a capacitor charging. When the membrane potential reaches a certain threshold, the neuron fires an action potential and a synaptic transmission is initiated. In order to emulate the described behavior, the current flowing through S1 and S2 is collected by the SPA, and the amount of charge that the POST is receiving is computed and accumulated virtually over time. When the accumulated charge reached a defined threshold Q_{thr}, the virtually stored charge is cleared and the POST neuron fires a voltage pulse towards S1 and S2. In this case, the post-synaptic spike has an amplitude V_3=âĹŠV_d and a determined spike width PW. Since this post-synaptic spike represents a response to the pre-synaptic activity, two different situations can occur for each of the synapses: a voltage drop of $2V_d$ if there is some pre-synaptic activity coming from the sensor, or a voltage drop of âĹŠV_d if there is no pre-synaptic signal. The electrical classical conditioning scheme that we propose consists in emulating the PavlovâĂŹs dog test. The goal is to associate the V1 and V2 inputs through experience, so that the activation of the POST (salivation) is achieved not only with the presence of V1 (food), but also with the single application of V2 (bell ringing). This is because during the trials V2 appears paired with V1, so an associative process between the inputs takes place.

Initially, S1 has a high conductivity level, since the dog salivation is related to the sight of food, whereas S2 has a low conductivity, because the ringing of the bell is assumed to not cause salivation. First of all, a current-controlled forming process is performed on the S1 and S2 devices, which are located within the same dice. Examples of their I-V characteristics are depicted in Figure 3.12, where it can be seen that the devices present a similar electrical behavior. Next, five compliance-free RESET and SET processes are induced to each of the samples, in order to set their conductivity states within a certain range, following the procedure of the previous works [101] and [102]. The maximum voltage applied to the sample with the S1 role was of $V_{set} = 2V_d$, whereas in the case of S2, it was of $V_{set} = V_d$. In this way, the conductivity state of S1 was set to a high value ($G > 30G_o$), whereas S2 was set to a low value ($G \leq 5G_o$). The whole learning sequence is represented in Figure 3.13. The voltage drops at S1 (V_{S1} in Figure 3.13.a) and S2 (V_{S2} in Figure 3.13.b), which are defined as $V_{S1} = V1 - V3$ and $V_{S2} = V2 - V3$, are plotted over time. Next, the V1 (US) and V2 (NS $\rightarrow$ CS) waveforms (Figure 3.13.c and Figure 3.13.e, respectively) are plotted

over time. The neuron response | V3 | is also depicted in Figure 3.13.g, symbolizing the dogs' salivation. The currents through S1 (I1 in Figure 3.13.d) and S2 (I2 in Figure 3.13.f) which were measured during one of the tests are also shown as an example, which were recorded only when the POST was firing a pulse, in order to speed the performance of the tests.

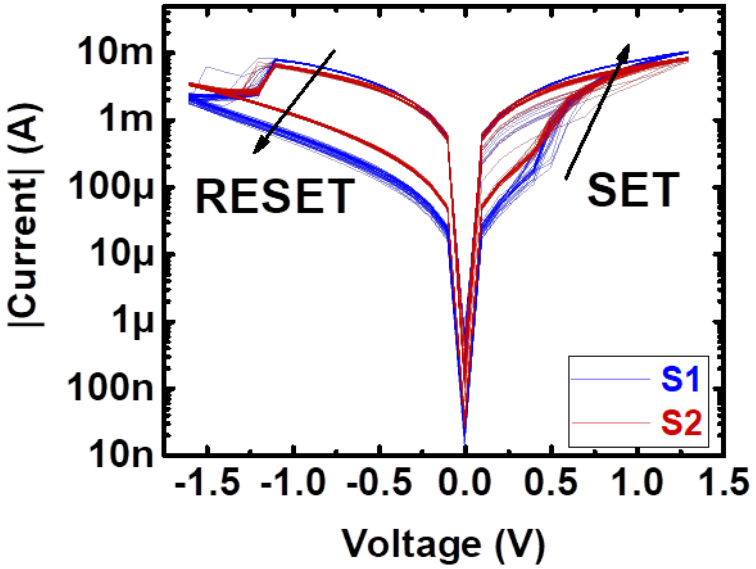

Figure 3.12: I-V characteristics of the two tested OxRAM devices, S1 as blue lines and S2 as red lines. The two devices show a similar electrical behavior.

The learning sequence starts with the single application of V_1=V_d($-20s < t < -15s$), and then of V_2=V_d($-10s < t < -5s$). The POST responds to V_1 because S1 presents a high conductivity state from the beginning of the test. On the other hand, no firing of the POST is expected to occur when only V_2=V_d is applied, since it represents the NS, and S2 has a very low conductivity. Next, both V_1 and V_2 are activated together during a training time of 50s. Because of the current through S1 is high, eventually, the accumulated charge in POST reaches Q_{thr}, so that it fires a voltage pulse as a response. The voltage drop at S2 (Figure 3.3.b), which has a magnitude of $2V_d$, causes S2 to eventually increase its conductivity. This event may occur multiple times during this phase since it depends on the POST spiking, as shown in Figure 3.3, which is affected by the conductivity change evolution of S2 during the conditioning stage, which might differ from test to test due to the intrinsic cycle-to-cycle variability of the tested devices. Finally, V_2=V_d is applied as a single input ($55s < t < 60s$), and the current through S2 is high enough to trigger the POST response, which is similar to the response evoked by single V_1 application, so V_2 has been effectively associated to V_1. The conductivity state of S2 reached after the conditioning stage is referred to as the conditioned conductivity, g_{CC}.

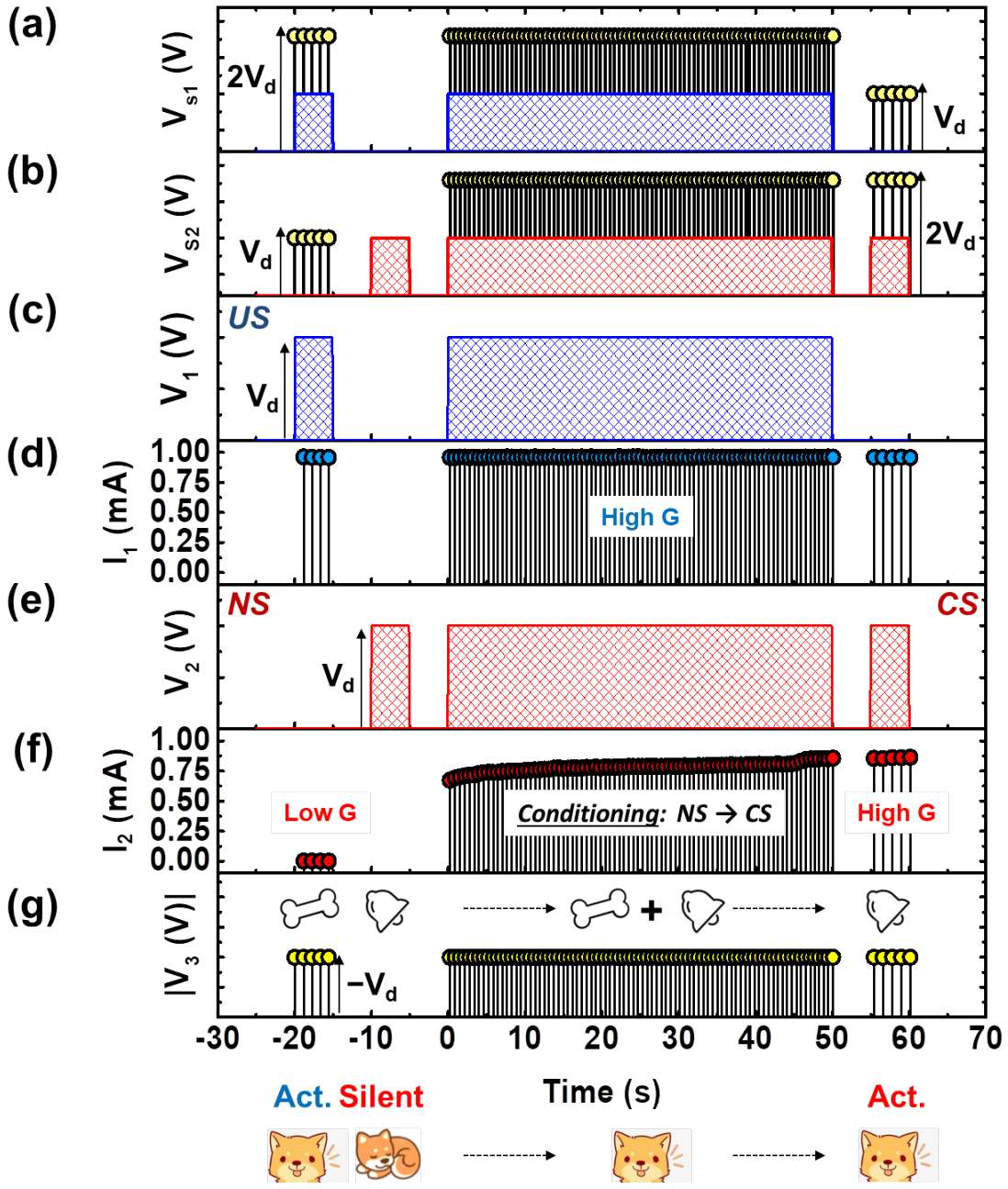

Figure 3.13: Electrical classical conditioning test scheme. An analogy of the POST state (active (act.) or silent) to the Pavlov's dog behavior is shown at the bottom of the plot. **(a)** Voltage drop at S1 over time, defined as $V_{s1} = V1 - V3$. **(b)** Voltage drop at S2 over time, $V_{s2} = V2 - V3$. **(c)** V1 waveform, being its high level of V_d V. **(d)** Intensity level flowing through S1 when the POST is firing a spike. The effect seen at t=55s is due to a lower voltage drop at S1. However, the conductivity state of S1 remains constant during the whole test, being $G_1 \approx 35G_o$. **(e)** V2 waveform, being its high level of V_d V. **(f)** Intensity level flowing through S2 when the POST is firing a spike. During the conditioning stage ($0s < t < 50s$) increases, being the most significant change at the instant when the voltage drop at S2 is of $2V_d$. As for its conductivity level, it increases from $G_2 < 1G_o$ up to $G_2 = 31.89G_o$, being similar to the one of S1. **(g)** POST firings over time. Its high level is also of $|V3| = V_d$, being its polarity reversed.

The stage with paired V_1 and V_2 is the core of the classical conditioning experiment, because

it is when associative learning, which implies that a change in S2 conductivity when V_1 and V_2 are activated simultaneously occurs. The value of V_d has to be carefully chosen as to induce a positive change in S2 conductivity only when V_2 and the POST spikes are overlapping. That is, the voltage drop at S2 of $2V_d$ has to be large enough to induce a SET process, but a voltage drop of magnitude V_d in device S2 should not. On the other hand, the conductivity state of S1 remains constant during the whole test, since a voltage drop of $2V_d$ is not large enough as to increase its conductivity state above its initial value, which is already large. In Figure 3.14, the impact of the above mentioned voltage drops at S1 (Figure 3.14.a) and S2 (Figure 3.14.b-d) is depicted within G-V characteristics plots.

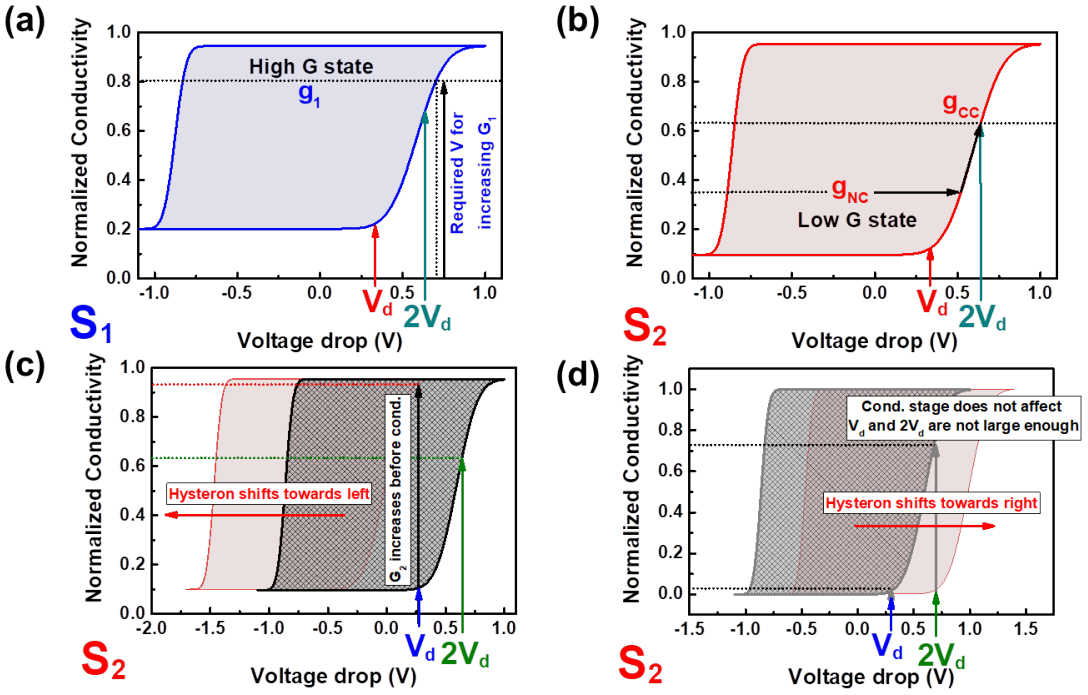

Figure 3.14: Normalized G-V characteristics of the tested devices explaining the behavior of S1 and S2 during the electrical classical conditioning test. **(a)** S1 G-V characteristics. In this case, the initial conductivity state is so high that voltages drops with values of V_d (red arrow) and $2V_d$ (green arrow) are not enough to update it. The required voltage drop is indicated with a black arrow. **(b)** S2 G-V characteristics. Initially, S2 presents a low conductivity state, corresponding to a non-conditioned value, g_{NC}. This state is large enough in order to not be affected by a voltage drop of V_d. However, a voltage drop of $2V_d$ is large enough in order to update the conductivity state to g_{CC} during the conditioning stage, so that S2 is conditioned through association. **(c)** Interpretation of the cycle-to-cycle variability effects on the G-V characteristics of S2. In some tests, the S2 hysteron is shifted towards left (red hysteron). In this case, a voltage drop of V_d is large enough to update its initial conductivity value. Any association process can occur since g_{NC} is already high before the conditioning stage begins. **(d)** The hysteron can also shift towards right due to the cycle-to-cycle variability. In this case, neither voltage drops of V_d or $2V_d$ are large enough to change its initial conductivity state g_{NC}. Hence, any association process cannot occur.

In order to study the effects of the V_d value on the conductivity state evolution of S2, the relative conductivity change $\Delta g_2(t)$ of S2 during the conditioning stage was studied. $\Delta g_2(t)$ is defined as the difference between the measured conductivity state of $g_2(t)$) (in G_o units), and the conductivity before the conditioning stage, g_{NC}. The test was performed for different values of V_d, ranging from 0.2V up to 0.4V, while keeping the rest of test parameters fixed: Q_{thr}=0.1mC and a POST spike width of PW=0.1ms. In Figure 3.15, a few examples of the evolution over time of

the relative conductivity change normalized to g_{NC}($\Delta g_2(t)/g_{NC}$) measured on the same device are depicted. Each color represents a different value of the employed V_d. Despite of using the same test parameters, different $\Delta g_2(t)/g_{NC}$ waveforms are observed during the trials. This is attributed to the cycle-to-cycle variability of the tested technology, observed in the previous chapter. An interpretation of its effects on the G-V characteristics of S2 is provided in Figure 3.14. It is suggested that the cycle-to-cycle variability can cause a horizontal displacement of the S2 hysteron, shifting it towards the left (Figure 3.14.c) or towards the right (Figure 3.14.d). If the hysteron is shifted towards the left, a voltage drop of V_d is large enough to provoke an increment of the initial conductivity state S2, occurring before the conditioning stage ($-10s < t < -5s$ in Figure 3.3.e). In the latter case, the shift towards right causes S2 to be immune to voltage drops of V_d or $2V_d$ despite of S2 having a low conductivity state. In any of the cases, any association process can occur.

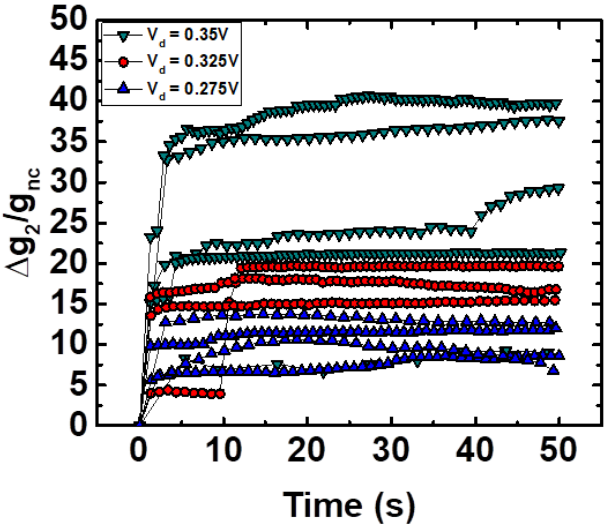

Figure 3.15: $\Delta g_2(t)/g_{NC}$ examples for different V_d levels during the conditioning stage. Each curve is related to the I_2 values measured when POST was firing a pulse for different V_d values, performed on the same device.

As to analyze the cycle-to-cycle variability effects on the association process, the cumulative distribution functions (cdf) of the conductivity values observed after conditioning, $g_{CC} = \Delta g_2(t=55s)$ were analyzed. The cdfs are shown in Figure 3.16.a, where each curve corresponds to a different V_d value. Results of Figure 3.15 and 3.16.a show that the associative process has a dependence with the employed V_d. As to provide a probabilistic interpretation, an association criterion in terms of a conductivity ratio threshold ($CCR_t h$) is defined, assuming that if the conditioning conductivity ratio $CCR=g_{CC}/g_{NC}$ is larger or equal than the CCR_{th}, ($CCR \geq CCR_{th}$), the conditioning stage has been effective. In Figure 3.16.a, three criteria are marked: $CCR_{th}=0.1$, $CCR_{th}=1$ and $CCR_{th}=10$. The probability of association ($Prob_{acc}$) is computed as the number of trials where a particular association criterion CCR_{th} is met, corresponding to the number of trials in which the CCR is above CCR_{th}, and corresponds to:

$$Prob_{acc} = 1 - P(CCR \geq CCR_{th})$$

The probabilities of association as a function of the tested V_d values are depicted in Figure 3.16.b. It can be observed that the probability of association increases with increasing V_d, up to the maxima $V_d=0.325V$. Above this value, any association process can take place: the voltage drop of V_d, originated when V_2 is active before the training stage (âĹŠ10s $< t <$ âĹŠ5s) is large enough to evoke a SET process to S2 on its own (Figure 3.14.d), being its conductivity state increased in the

wrong scenario.

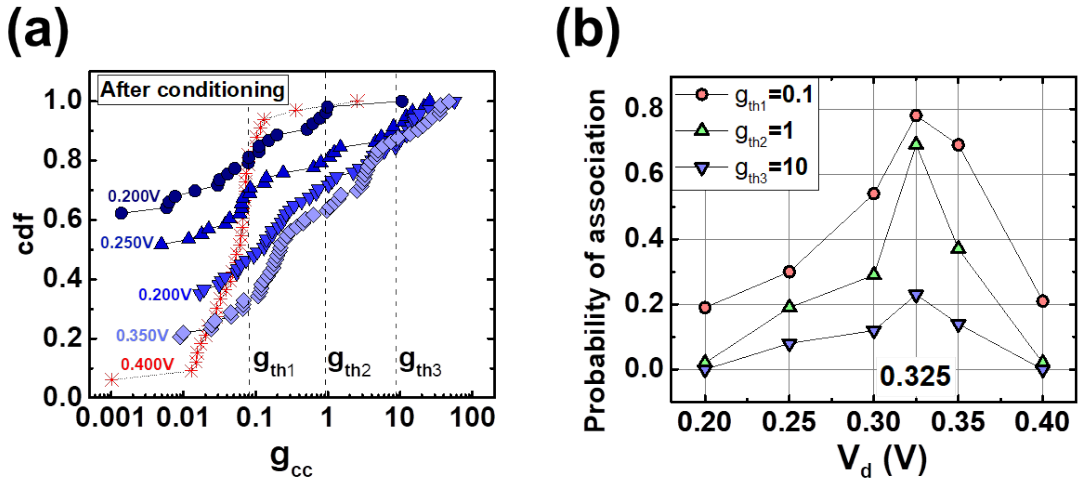

Figure 3.16: **(a)** Cdfs of the relative conductivity change achieved after the conditioning stage, CCR=g_{CC}/g_{NC}, for differents V_d. The associative process requires a proper choice of V_d. Three association criteria examples are depicted: $CCR_{th1} = 0.1$, $CCR_{th2} = 1$ and $CCR_{th3} = 10$. **(b)** The association probability for three different criteria of association (CCR_{th} = 0.1,1 and 10) is represented as a function of V_d. Probability increases with increasing V_d up to a limit were no association process takes place, since S2 conductivity changes before any pairing between V1 and V2 is made. Maxima are found at $V_d = 0.325$V.

Concluding this subsection, the experiments show that the probability of having the post-synaptic neuron responding to the neutral stimulus when it is the only active input is highly increased after the conditioning stage, in analogy to Pavlov's dog behavior. Because of the intrinsic cycle-to-cycle variability of the tested devices, a probability of association criterion is defined. The association level reached during conditioning increases with increasing voltage drop applied to the synaptic devices, up to a certain value, for which any association learning process cannot occur. The results of this subsection suppose a step towards the study of fundamental associative learning rules, which would permit the implementation of neuromorphic associative memories and hierarchical computing networks.

Chapter 4

A bio-inspired unsupervised learning algorithm for an OxRAM-based neuromorphic systems

1 Introduction to self-organizing neural networks

Unsupervised learning involves a methodology where the training stage does not require the calculation of any error made by the system for a certain input data set, in order to improve its performance. That is, both user and system are not meant to know the actual solution of the problem to be faced by the neural network, nor detailed information about the input dataset properties, in contrast with supervised learning techniques. Unsupervised learning implementation would be beneficial for neuromorphic architectures, since in one hand it does not rely on the error computation and correction as the supervised learning techniques do, so extra-circuitry could be avoided. The applications of unsupervised learning algorithms are related to classification, symbolic representation and associative tasks in which the relevant features of the input data set are learned in an autonomous way. Examples of bio-inspired unsupervised learning implementations based on memristive devices for image recognition tasks can be found in [91] [103] [104] [105] and [57]. In these works, the MNIST data set (consisting on handwritten letters) or a few 25-bit vowel characters are used to train simulated neural networks. The neural networks consist on two neuron layers, where the training relies on the Spike Timing-Dependent Plasticity (STDP) as the learning rule, and includes a winner-takes-it-all mechanism (WTA). After the training, each of the output neurons is specialized to the recognition of particular character. These works demonstrate that unsupervised learning can be implemented in a neuromorphic system based on memristors, with significant accuracy when character recognition tasks involving a certain level of noise are considered. However, there is still a lack of knowledge on how to adapt more complex unsupervised learning algorithms to be implemented in a neuromorphic hardware, in which the features of the input data set appear represented with a certain spatial order within the output neuron layer, resembling the topographical organization found in the biological brain.

A particular example of bio-inspired unsupervised learning is the self-organizing map (SOM), also called Kohonen network [106]. Applications of SOM extend to financial predictions, medical diagnosis or data mining, among others [106] [107] [108]. The aim of this learning algorithm consists in mapping the input data set onto a regular and usually two-dimensional grid, which corresponds to the output layer, under an unsupervised and competitive learning scheme. A diagram of a Kohonen network is depicted in Figure 4.1.a. In here, the synaptic weights represent the connections

between one element within the output layer, and each of the members of the input layer. The key of this algorithm consists in evaluating the similarity between the set of weights of an output neuron, and the input data, which fed to the system as a vector. The original algorithm consists in the sequential execution of the following steps, parting from a network with randomly initialized weights. For randomly chosen input from a particular data set, the Euclidean distance between the input and the weights of every output neuron must be computed, in order to determine which is the output neuron whose weights are closer to the input. This element is identified as the best matching unit (BMU), and its weights are updated in order to slightly reduce its distance with the input data. The magnitude of the weights change depends on the learning rate parameter, which is set by the user.

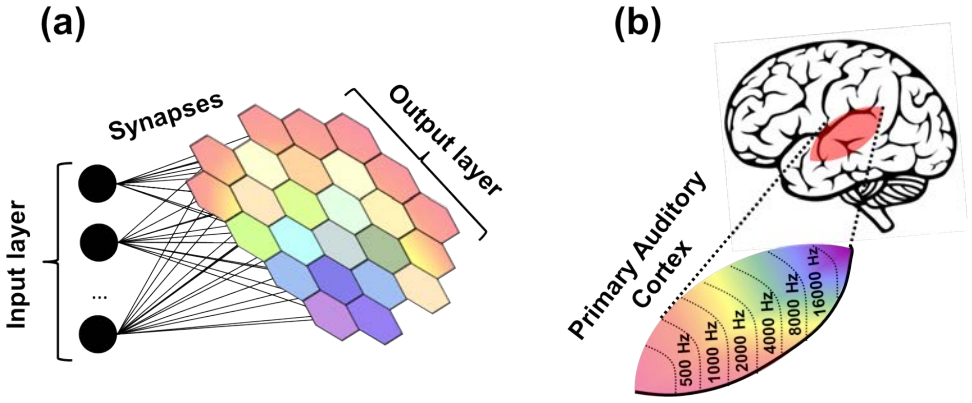

Figure 4.1: **(a)** Example of a self-organizing map. The input layer is unidimensional and consists of three nodes (input neurons). The output layer is bidimensional, and each node corresponds to an output neuron. Output neurons can communicate to their immediate neighbors. All of the input nodes have a weighted connection (synapse) with every output node. The weight of the synapse determines how strong an output neuron responds to the activation of a particular input. These neural networks are inspired in the topological maps found in the sensory-processing areas of the brain, where neurons that respond to similar inputs are spatially located very close. **(b)** An example of a topological map in the human brain, corresponding to the tonotopic map of the primary auditory cortex, in charge of processing sound. Neurons that respond to similar sound frequencies are grouped in clusters, which appear in a frequency-ordered fashion.

Once trained, these networks present topographical organization such as the one found in sensory processing areas of the brain (Figure 4.1.b) [106] [107] [108] [109] [110] and [111]. In this way, similar inputs will activate neurons in the output layer which are found close to each other, whereas dissimilar ones will affect distant regions. The output layer appears organized in clusters, whose relative size and location provides statistical information of its corresponding input data item characteristics. It is actually the presence or absence of an active response of an output neuron cluster, and not so much the exact input-output signal transformation or magnitude of the response, that provides an interpretation of the input information [106] [107] [108]. Many methods are derived from the SOM algorithm, where the neural system is built with SOMs as basic blocks or layers, such as the multi-layer or hierarchical SOM (HSOM) [106]. In the latter case, the network is constituted by concatenating SOMs in a feed-forward way (cascade), where one SOM layer is trained by receiving as input the outputs of another previous SOM. The advantage of HSOMs is that they require less computational effort than a standard SOM to perform certain tasks or problems that present a hierarchical or thematic structure, and moreover, HSOMs provide a simplest representation of the results, which leads to an easier interpretation because they allow the user to check what clustering has been performed at each level of the hierarchy.

In this chapter, a fully-unsupervised learning algorithm for reaching self-organization in neuromorphic architectures is proposed. Parting from the demonstrated spike-timing dependent plasticity

(STDP) function in the tested OxRAM devices in chapter 4, an alternative set of pre and post-synaptic waveforms is proposed, in order to induce symmetric conductivity changes. The modeled G-V characteristics from chapter 3 and chapter 4 are used to simulate a neuromorphic system in which the OxRAM devices act as electronic synapses. A fully-unsupervised learning algorithm, adapted from the original self-organizing maps algorithm is tested, involving the STDP as the local learning rule. The design of the system and learning scheme permits to concatenate multiple neuromorphic layers, where autonomous hierarchical computing can be performed.

2 System structure and neuron specifications

In this section, the simulated neuromorphic system structure is detailed. The simulated system consists in a single memristive synaptic, which is implemented by a RRAM-based crossbar array (Figure 4.2.a), and two neuronal layers, namely, the input and output layers (Figure 4.2.a). With this architecture, a voltage can be applied to one of the rows from the input layer. This potential affects to the memristive devices within the same row, each of them having a particular conductivity state. Then, the output layer can collect the sum of the weighted intensities flowing through the memristors within the same column. The conductivity state of the synaptic devices can be updated by means of applying the proper pre and post-synaptic voltage waveforms (Figure 4.2.b) according to some learning rule, such as the above mentioned STDP (Figure 4.2.c).

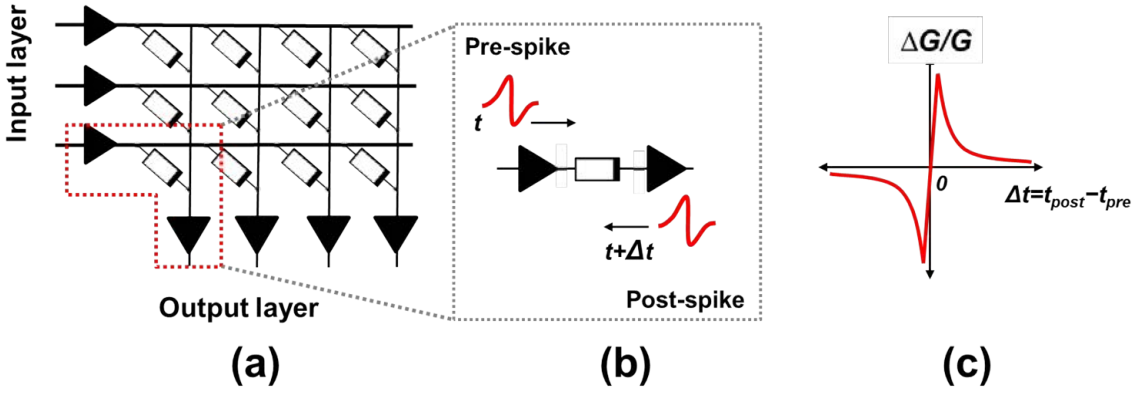

Figure 4.2: **(a)** Neuromorphic memristive array. Each node within the crossbar corresponds to the weighted connection (synapse) between two neurons, implemented with a memristor. **(b)** The conductivity state of the device can be changed according to the activity of the neurons it connects, by means of applying voltage-waveforms to its two terminals, being the pre and post-synaptic spikes. **(c)** According to the STDP property, synaptic weight changes (ΔG) can be induced by means of delaying one of the spikes with respect to the other, so that the shape of the resulting voltage drop at the memristor shows dependence on the time delay Δt.

The input and output neurons share the same structure and functionality, so that the neuron layer roles can be interchanged, and multiple synaptic layers can be concatenated without adding extra-circuitry. The neurons are considered to be integrate-and-fire neurons:the received charge is accumulated, which causes the neuron to depolarize along its membrane (membrane potential), until a certain threshold potential is reached (this process is analogous to a capacitor being charged). A schematic of the proposed electronic neuron is shown in Figure 4.3. It has six input/output terminals: terminals In1 and In4 receive current signals from the synaptic arrays, which polarize the neuron and update its membrane potential. This membrane potential is compared constantly to a voltage threshold. When this threshold is reached, the neuron is discharged (its membrane potential is reset to 0). Then, it triggers a voltage pulse backwards through Out1 and forward via

terminal Out4, towards its synapses. I/O2 and I/O3 are for neighbor activity signaling, providing communication with the neuron immediate neighbors. For instance, if a neuron fires a pulse, its terminals I/O2 and I/O3 flags will be activated, so its neighbors are warned and will consequently trigger a pulse, which is independent of its membrane potential. When this event occurs, the membrane potential of the neighbors is also reset.

As to provide a simple example, only one self-organizing layer is considered in Figure 4.3.a. The input neurons of the system are in charge of triggering voltage pulses according to the input data set through terminal Out4, sourcing or draining current from/to the synaptic layer, whereas output neurons integrate the received current through terminal Out1, which corresponds to the summation of each of the input neurons voltage pulse, weighted by its connection weight or device conductivity, and have the integrate function disabled, as well as the neighbor interaction. These output neurons fire a post-synaptic pulse backwards, as a response to the input neurons activity, and also communicate with their immediate neuronal neighbors within the output layer via terminals I/O2 and I/O3. Its activity is measured through Out4. Finally, the terminal In4 is left unconnected. An example of a 2x2 crossbar where all of these signals are shown in Figure 4.4.

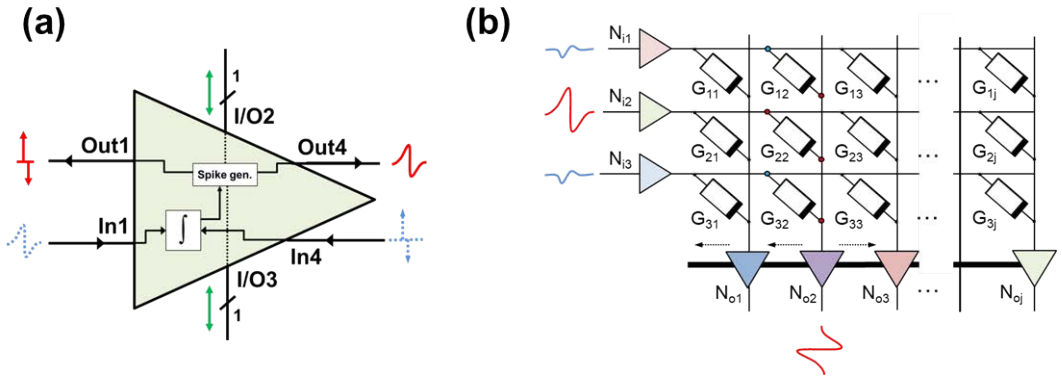

Figure 4.3: **(a)** Schematic of the proposed electronic neuron. **(b)** A simplified scheme of the proposed self-organizing neuromorphic network (not showing all the connections). The system consists in two neural layers behaving as the input and output layers. The output neurons integrate the signals coming from the input layer, and trigger pulses backwards when their potential reaches a threshold. Adjacent neurons within the output layer are connected (black wide line) in order to provide lateral interaction, which is one of the key aspects of the proposed algorithm. The input and output layer are connected through a memristive crossbar array, where every intersection corresponds to a weighted connection between an input and an output neuron, provided by a RRAM device.

In the simulations performed during this thesis, the output neurons behavior was included mathematically. Implementations of the designs of electronic neurons with the same functionality, based in CMOS technology, can be found in [112] [113].

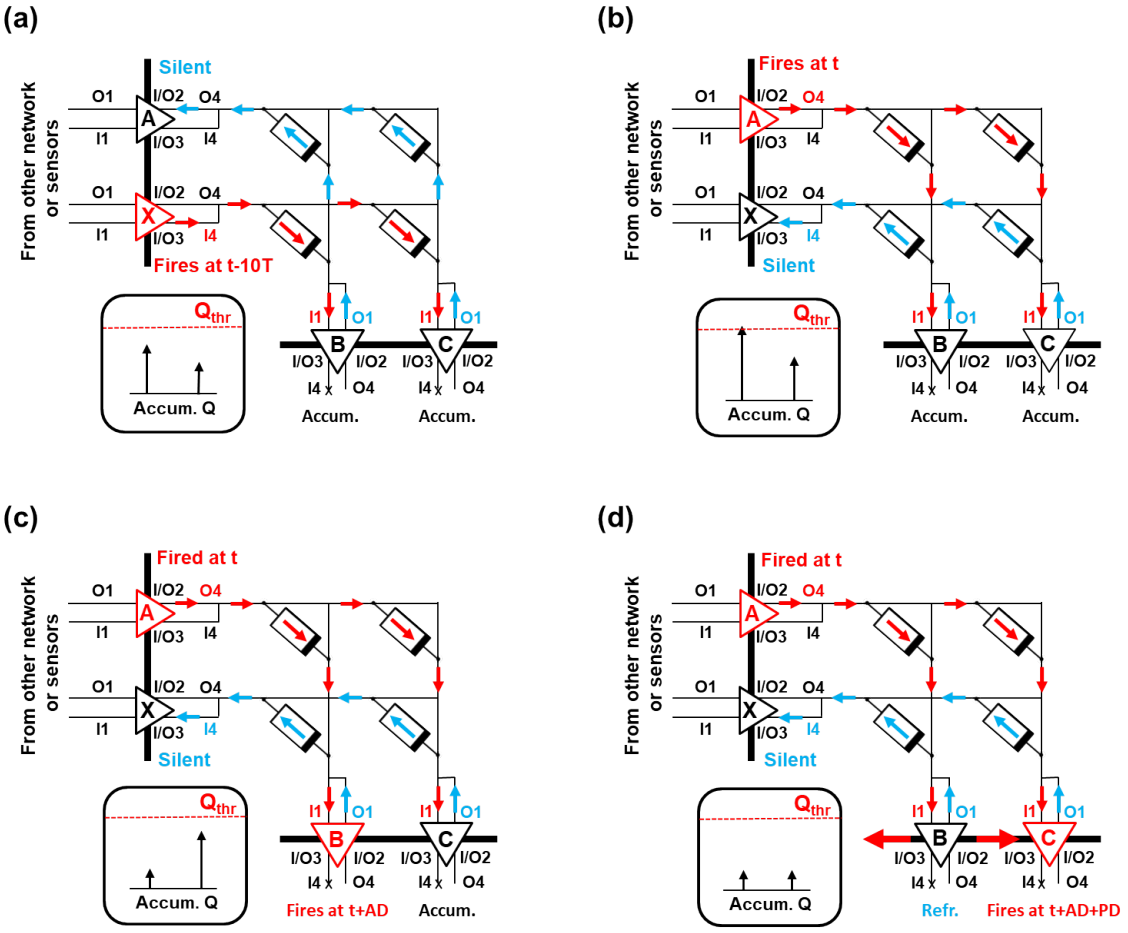

Figure 4.4: Example of a 2x2 crossbar array in which all the neuron connections are shown. The input neurons can be driven by sensors, or by signals coming from another network. The accumulated charge of the output neurons is also depicted. **(a)** Input neuron X fires a pulse, and input neuron A remains silent. These signals update the accumulated charge of the output neurons B and C. **(b)** Input A fires a pulse, and output neuron B accumulated charge reaches the charge threshold, $Q_t$hr. **(c)** The accumulated charge of B is reset, and B fires a pulse delayed by AD with respect to the firing time of A. The voltage drop at the synapses within the B column causes a change in their weights. **(d)** Neuron B communicates with its neighbors (only C is depicted), and enters its refractory period. Neuron C triggers a pulse delayed AD+PD with respect to the firing time of A, and its accumulated charge is reset. Because its pulse presents a larger time delay, the magnitude of the change of its synapses will be smaller, according to the induced STDP function.

3 STDP-based symmetrical synaptic weight updating

The proposed unsupervised learning algorithm relies on the STDP property of the tested devices. This subsection parts from the results of [21], where STDP functions were experimentally obtained for different time scales. In the previous chapter, two examples of the experimental and modeled STDP functions for a spike-width of 1ms were shown (Figure 4.9.b). In general, a bias towards synaptic depression is observed, regardless of the time-scale. It is suggested that this biasing is related to an asymmetry of the G-V characteristics, being the RESET process more abrupt in contrast with the SET process. Due to this asymmetry, saturation of the synaptic relative weight update is observed for small and negative Δt. Summarizing, the induced STDP functions present asymmetry and the relative weight change is not linear. With such characteristics, these functions are not optimal choice for increasing the performance of the learning algorithm [114].

In order to get symmetrical STDP functions, instead of using identical pre and post-synaptic waveforms, we propose using the pair of pulse shapes shown in Figure 4.5.a, so the STDP function can be easily tuned in terms of biasing, according to the desired working regime of the employed devices. In here, the maximum and minimum voltage drops at the synaptic device are defined as the $V^{\pm}_{max}$ and $V^{\pm}_{min}$ parameters, respectively (see Figure 4.6.b). By using the proper $V^{\pm}_{max}$ and $V^{\pm}_{min}$ values, a linear operation regime can be achieved (gray area identified as a sub-hysteron in Figure 4.6.b), where the conductivity state can be finely updated according to the STDP rule, and the saturation of ΔG is withdrawn. Moreover, the stochasticity related to the RESET process is avoided. In our case, we employed the following parameters: $V^{+}_{pre} = 0.5V$, $V^{-}_{pre} =$ âĹŠ$0.4V$, $V^{+}_{post} = 0.875V$ and $V^{-}_{post} =$ âĹŠ$0.4V$. With these voltages, the conductivity state is kept within the sub-hysteron region depicted in Figure 4.6.b, ranging from $g_{SHmin} = 0.33$ ($10G_o$) to $g_{SHmax} = 0.8$ ($25G_o$).

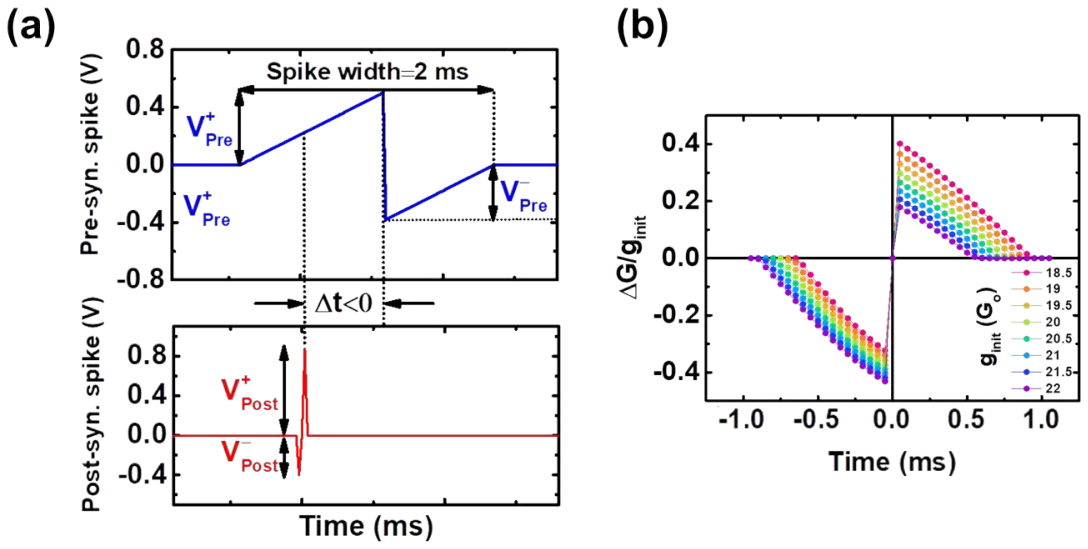

Figure 4.5: **(a)** Pair of proposed pre and post-synaptic waveforms.**(b)** Tuned STDP function. Each curve corresponds to a different initial conductivity state of the same devices. Symmetrical conductivity changes are observed in the normalized initial conductivity state of g=0.5, corresponding to $g_{init} = 19G_o$.

This procedure allows implementing the balanced STDP functions shown in Figure 4.5.b, where multiple cases involving different initial conductivity values (g_{init}) within the sub-hysteron region are shown. Since there is a dependence on the conductivity change and g_{init}, the symmetry in the induced conductivity changes is checked at the normalized conductivity state of g_{init}=0.5 within the sub-hysteron region, corresponding to g_{init}=$19G_o$ in our case. These results support that symmetrical conductivity changes can be induced by using the proposed pre and post-synaptic waveforms, being this symmetry a key factor for increasing the neural network performance [106].

4 Self-organizing neural networks based on OxRAM with fully-unsupervised learning training

In this subsection, the details of the proposed learning algorithm are exposed. This learning algorithm is a neuromorphic hardware-adapted version of the self-organizing maps algorithm by T. Kohonen [106]. Bio-inspired mechanisms have been added in order to provide with a fully-

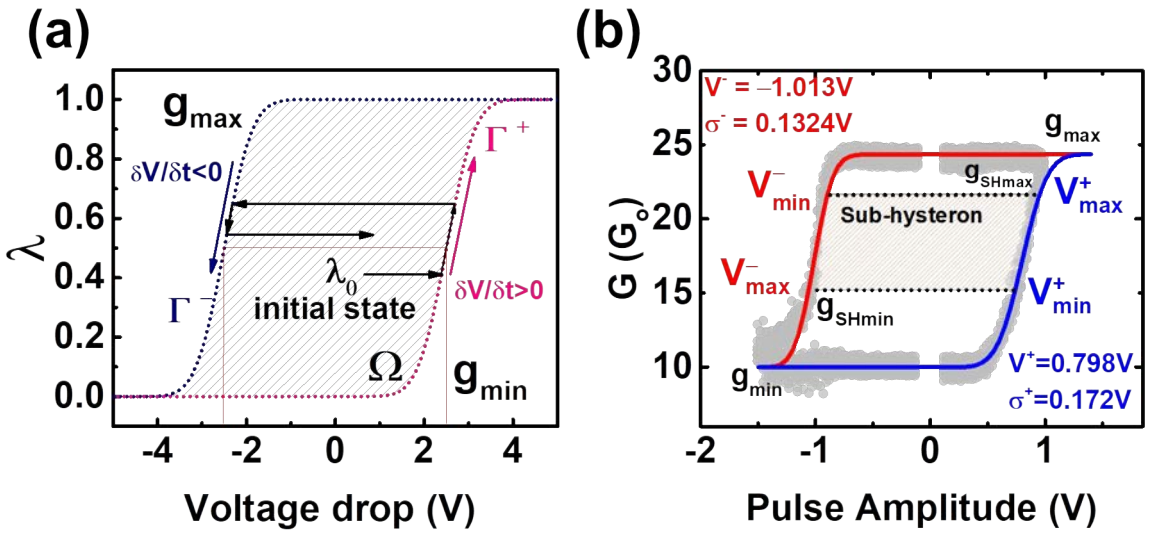

Figure 4.6: **(a)** Ideal hysteron function of a non-linear memristive device [71]. The normalized internal state λ is represented as a function of voltage drop at the memristor. Top and bottom boundaries are identified as the maximum (g_{max}) and minimum (g_{min}) conductivity states. In order to increase (decrease) the conductivity state of the device, a positive (negative) voltage has to be applied so that λ shifts towards g_{max} (g_{min}), describing the Γ^+ (Γ^-) trajectories. **(b)** An example of experimental (black dots) and fitted (blue and red lines) G-V characteristics. The fitting parameters are also indicated at the top part of the figure. A conductivity state sub-space is identified as a sub-hysteron. The main parameters which allow confining the conductivity state of a device within the g_{SHmax} and g_{SHmin} conductivity state values as the top and bottom limits of the identified sub-hysteron are $V^{\pm}_{max}$ and $V^{\pm}_{min}$. These are the main parameters used to design the pre and post-synaptic waveforms required to tune the STDP function of a device.

unsupervised version of the learning algorithm, meaning that any extra-circuitry for the calculation of the Euclidean distance required in the original Kohonen's algorithm is needed. The single-layer system from subsection 5.3 is trained on-line with this algorithm, meaning that the synaptic weights are being updated according to the input data set features. On-line training presents the following advantage against off-line training: if some of the input data set feature changes over time, the system is expected to re-organize and adapt to that particular change.

The main mechanisms regarding the proposed algorithm are summarized in Figure 4.7. In here, the electronic components of the proposed neuromorphic system (integrate and fire neurons and OxRAM devices as analog synapses) are indicated. A part from the use of the STDP property of the tested devices as a local learning rule, two more bio-inspired learning rules are considered in the learning algorithm: the so-called lateral neural neighbor interaction and vertical inhibition within a synaptic column. Lastly, the features of the system once trained are indicated, indicating that a self-organizing map has been properly achieved on hardware.

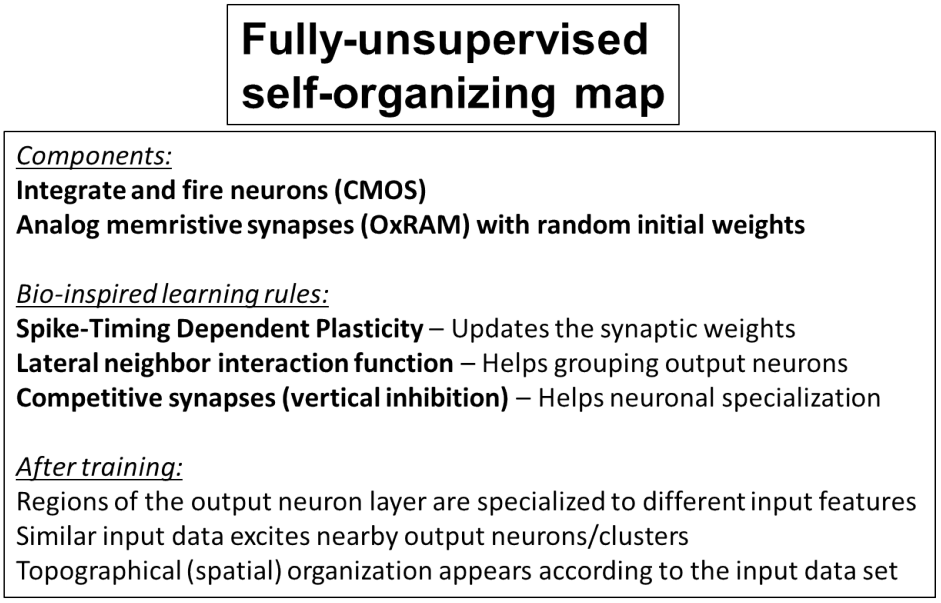

Figure 4.7: Main concepts of the proposed fully-unsupervised self-organizing maps learning algorithm, adapted to a neuromorphic architecture based on integrate and fire neurons and analog memristive synapses (such as the tested OxRAM devices). The synapses must have an initial random weight (i.e. conductivity state) within a certain range in order to trigger the self-organization process. The bio-inspired learning rules are the STDP, the lateral neighbor interaction function and competitive synapses, also referred to as vertical inhibition within a synaptic column. After the training, the system behaves as a self-organizing map: regions of the output neuron layer specialized to different input features appear, and a topographical organization is reached. In this way, the system maps the input data according to its similarity with the inputs it has been trained with. In order to do so, it parts from the fact that similar input data excites nearby output neurons/clusters.

Lateral neighborhood interaction is one of keys regarding the self-organizing property of the network. According to T. Kohonen in [106], "it is crucial to the formation of ordered maps that the cells doing the learning are not affected independently of each other but as topologically related subsets, on each of which a similar kind of correction is imposed". This means that when one output neuron receives a signal from a neighbor, which has recently fired a voltage pulse, it is also meant to trigger an identical pulse, both to its own connections with the input layer, and also to its other output neuron neighbor. In other words, the output activity of a particular output neuron propagates through the output neuron layer, leading to the activation of its neighbors. The number of affected neighbors can be defined externally, as well as the shape of the neighborhood interaction function. The implementation of a neighborhood interaction function whose amplitude decays laterally is often used in the software versions of the self-organizing networks (Figure 4.8). This is motivated by both anatomical and physiological evidence of the way neurons in nervous system interact laterally. The most popular choices for this function include a rectangular (abrupt) interaction function, Gaussian (a soft transition) or the so-called Mexican hat function, which consists in a soft transition involving the inhibition of the outermost neurons within the neighborhood. In our case, the decaying amplitude of the neighborhood interaction function is inherent to our system, because of the implementation of the above described STDP function as a local learning rule. Despite the neighbors of the maximally responding output neuron are intended to fire an identical pulse, this pulse will be delayed in comparison with the response of the main responding neuron (center of the neighborhood). With increasing Δt, the induced ΔG/G will also decay with increasing lateral distance, as shown in Figure (Figure 4.8).

The radius or number of affected neighbors can be set externally by controlling the time delay: the

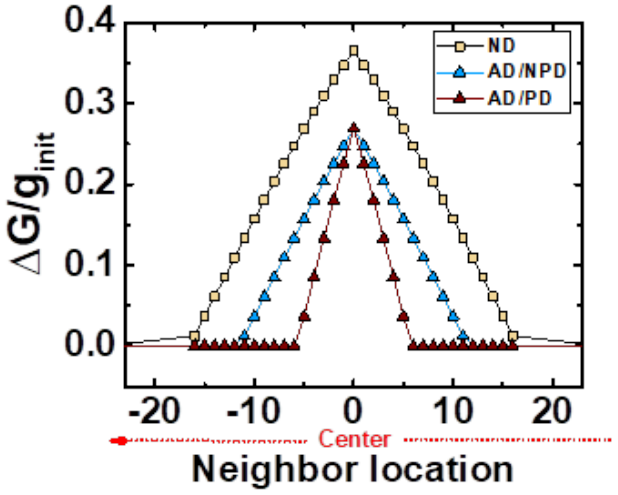

Figure 4.8: Neighborhood interaction functions based on the STDP rule. The neighbors are intended to fire a spike which is delayed in comparison with the main spiking neuron. According to the STDP rule described above, the magnitude of the change in conductivity $\Delta G/g_{init}$ decreases with increasing time delay. Two types of delay are considered: the first is the delay affecting to all of the neighborhood: the main spiking neuron response is delayed with respect to its pre-synaptic pulse. Then, all the induced conductivity changes are reduced. The second is the propagation delay (PD) between immediate neighbors. The ND curve (yellow squares) shows an example where any delay is considered. AD/NPD curve (blue triangles) consists in a delayed response from the main spiking neuron, but minimum propagation delay. The AD/PD curve is an example of the presence of both delays.

whole neighborhood activity can be delayed (all delayed, AD), and the propagation delay (PD) between immediate neighbors. In Figure 4.8, different neighbor interaction functions are depicted as examples, assuming that the affected synapses have the same initial conductivity state and received the same pre-synaptic pulse. The ND curve corresponds to a function where minimum delays are considered: the main firing output neuron B is firing with a delay AD of 1 time unit with respect to the last pre-synaptic pulse sent by neuron A, and the PD is also of 1 time unit. Therefore, the time delay in which a neuron C within the neighborhood fires a pulse after the main responding neuron A has triggered one, as an answer to an input neuron, corresponds to $AD + PD \cdot N$, being N the number of neurons which separate neurons B and C. In Figure 4.8, the distance between neurons B and C is none, thus N=1. The AD/NPD and AD/PD curves present a delay of AD=5 time units, so that all the conductivity changes in the neighborhood are diminished equally. The difference between these two functions relies on the propagation delay: AD/NPD has the minimum PD, whereas AD/PD has a PD of 2 time units. As seen in Figure 4.8, increasing PD results in a narrower function, reducing the number of affected neurons.

Another important aspect is the inhibition of the synapses within the synaptic column of an active neuron. The synaptic column comprises all its synapses, some of them connecting the neuron with inactive input neurons. For our system, both potentiation of the synapse, relating the firing neuron with the active inputs, and the depression of its synaptic weights which connect it with the inactive inputs, are mandatory to efficiently group or cluster the output neurons, so that a complete correction of the synaptic weights (and thus, of its neighborhood) is performed. This means that if a particular RRAM conductivity is increased as a result of applying the STDP rule, the other RRAMs in that synaptic column, connecting the same output neuron with the inactive input neurons, shall be depressed (i.e. their conductivity is decreased) (Figure 4.4.c and 4.4.d). In our case, the inclusion of inhibitory synapses leads to an increase of the sensitization of an output neuron to a single input neuron, facilitating clusters specialization to a specific input property. In order to implement this feature electronically, the silent input neurons at a particular time are

not actually silent, but rather applying a small and negative DC voltage through terminal Out4 to their synapses (Figure 4.4), in analogy with the biological neurons resting potential. When an output neuron is firing a pulse backwards, the induced voltage drop at the synapses connecting to a silent input neuron will cause a decrease in their conductivity states. In this case, there is no direct relationship with the STDP rule, since the induced voltage drop at the synapses is not related to any time correlation between the pre and post-synaptic activities.

Lastly, the methodology suggested for the unsupervised self-organization process to arise is discussed. The synaptic layer is randomly initialized, that is, the conductivity state of each RRAM device is set randomly between the g_{SHmin} and g_{SHmax} values defined previously in Figure 4.6.b. In order to amplify the initial differences between each output neuron synaptic weight values, the threshold potential has to be set large enough, so that the first post-synaptic firing occurs after the presentation at least 100 pre-synaptic pulses in the case of our electronic synapses. This value takes into account the initial conductivity state values of the employed synaptic devices, and the voltages required to induce the conductivity change according to the STDP function (Figure 4.5.b). The active input neurons provide current to the output neuron layer, whereas silent input neurons drain current from the system because of the polarity of its resting potential. In this way, active inputs depolarize the neurons increasing their membrane potential, whereas silent inputs decrease it (Figure 4.4.b). The identification of the best matching neuron by means of calculating the Euclidean distance of the whole set of synaptic columns is avoided, which simplifies the electronic implementation of the learning algorithm compared to the original Kohonen's self-organizing learning algorithm, despite a larger number of iterations are required in order to execute this step. On the other hand, if a neuron has recently fired a spike, it will present a refractory period, meaning that it will not be able to fire again after some time. By doing this, the output neurons which have not fired recently are encouraged to do it. We do not explore the effects of dynamically changing the threshold potential of the output layer. However, a dynamic threshold could improve the performance in terms of convergence time of learning algorithms [113].

The whole training stage is summarized in the flux diagram depicted in Figure 4.9. Initially, all of the devices are assumed to have a random normalized conductivity around 0.3-0.4, corresponding to $18G_o$-$20G_o$ in our case. The output neurons membrane potentials are also initialized to zero. The input dataset is then fed to the system through the input neurons, which are triggering the pre-synaptic voltage waveform depicted in Figure 4.5.a if active, or applying their resting potential to the synaptic array, if silent (Figure 4.5.a and Figure 4.5.b). The output neurons potentials increase as the output neurons integrate the pulses of the input neurons that they receive, which are weighted by the conductivity of the synaptic devices. That is, the output neurons are receiving a charge whose magnitude is related to the input activity and the weight of the connections between each of them and the input layer.

Eventually, one of the output neurons potential will reach the defined threshold potential. At this point, the weight updating process occurs: the output neuron resets its accumulated potential to zero, and triggers the post-synaptic voltage waveform from Figure 4.5.a backwards, affecting its synapses (Figure 4.4.c). The maximum voltage drop given by this post-synaptic voltage pulse and the active input neuron corresponds to the sum of V^+_{pre} and V-post (positive Δt), so this particular synapse is strengthened. On the other hand, the synapses with silent input neurons are depressed, being their voltage drop equal to the sum of V^+_{pre} and the input neurons resting potential, which is a DC voltage of $0.2 \cdot V^+_{pre}$V. Therefore, the induced conductivity change in these synapses has a smaller magnitude in comparison with the one induced to the synapse that connects the winner output neuron with the active input neurons. After the weight updating of the main neuron has been executed, its activity is propagated through the output layer, affecting its immediate neighbors. These other output neurons trigger a voltage pulse with the same amplitude, but with a certain accumulated delay (Figure 4.4.d). That is, the magnitude of the change in the strengthened synapses will be decreasing as the output signal propagates through the output layer, until reaching a non-significant synaptic change, following the neighbor interaction function of Figure

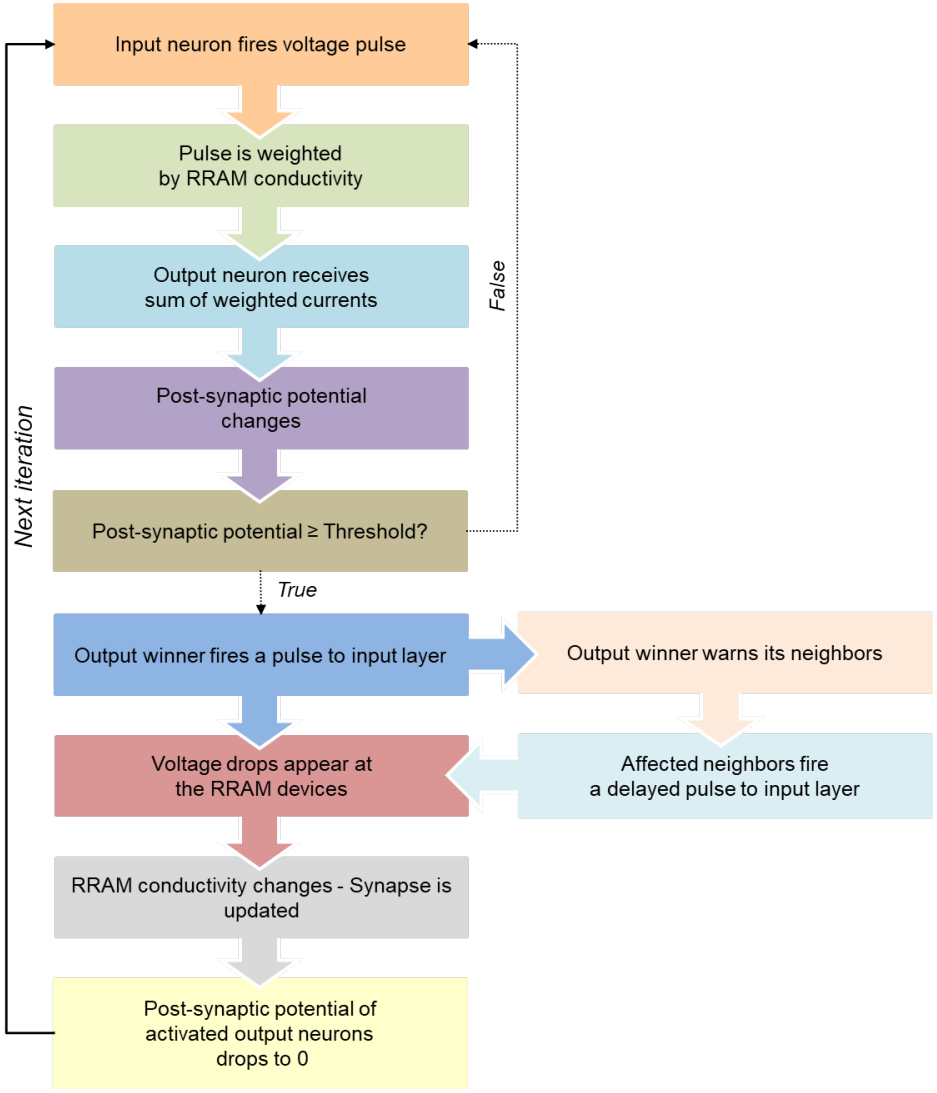

Figure 4.9: Flux diagram of the self-organizing algorithm based on STDP.

4.8. The affected neighbors will also reset their output potential to zero. In order to reach a convergence state of the map, the maximum synaptic change is diminished by increasing the firing neuron time delay over the iterations. Also, the size of the neighborhood is naturally decreasing over time, since the neighbor firings are also delayed. At the end of this training stage, the crossbar weights are organized in clusters, which present overlapped areas. In this way, nearby output neurons will be prompt to react to the same input, whereas distant output neurons will be sensitized to other inputs, as occurs in the software version of the Kohonen map.

5 Example of application: color mapping

A fundamental application of the proposed autonomous SOM is shown as an example. In here, a single synaptic layer system of 150 OxRAM synapses is simulated. The synapses are distributed in a 3x50 array, being 3 the size of the neuron input layer, and 50 the length of the output neuron layer. The input of the system are the red (R), green (G) and blue (B) color components of a pixel of an image.

During the training stage, only one of these components is shown at each time, that is, only one input neuron is firing a pre-synaptic pulse (Figure 4.4.a) at each time, with the V^+_{pre} value as the one shown above (V^+_{pre}=0.7V). The silent input neurons resting potential is set to a DC voltage of $-0.2 \cdot V^+_{pre} = -0.14$V. These voltage waveforms are weighted by the synaptic devices conductivities, which are randomly initialized between $15G_o$ and $18G_o$ (Figure 4.5.b). The voltage threshold of the output neurons is set to V_{thr}=$1000G_o$, that is, initially it takes approximately 200 pre-synaptic pulses before the first output neuron fires a post-synaptic spike. This firing is delayed initially 7 time units (being in our case a time unit t=0.05ms, so that initially, AD=0.35ms) with respect to the pre-synaptic pulse, so that the maximum relative conductivity change magnitude of a 10% according to the STDP function depicted in Figure 4.4.b. This delay is increased by one time unit with increasing learning iterations, every $1 \cdot 10^6$ input pulses (a learning iteration corresponds to the presentation of the whole input dataset). The propagation delay is kept constant at five time units, PD = 0.0275ms. Through the iterations, the system is able to self-organize in an autonomous way, without any intervention, being a fully-unsupervised training scheme. The training stage time can be computed in terms of the number of applied pulses and the time scale of the implemented STDP function. The map shown in Figure 4.10(a) was developed within two iterations, consisting in the application of single pulses of a defined spike width T (Figure 4.10.a) , being the time between pulses of 10T, which corresponds to a total training time $t_T = 2400s \approx 40$ minutes, assuming T = 1ms.

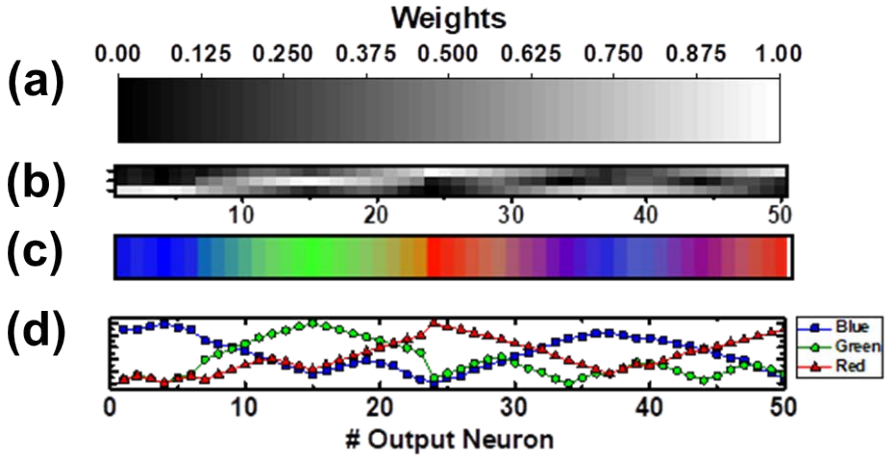

Figure 4.10: **(a)** 3x50 crossbar array displaying the normalized conductivity states of the simulated RRAM devices after the learning stage, which are represented in gray-scale. The highest conductivity states in white correspond to $21.1G_o$, whereas the lowest ones in black correspond to $15.6G_o$, being within the defined range of $g_{SH}(15G_o - 25G_o)$ (Figure 7.b) **(b)** The synaptic weights from every output neuron are related to a RGB coded color. The cluster in the left part of the output layer is specialized in red, and is followed by green, blue, red and green-sensitive clusters of neurons. The size of the obtained clusters is similar and is of approximately 15 neurons. **(c)** Normalized activation response of the output neurons when a red (red line with diamonds), green (green dotted line) or blue (blue line with triangles) is presented as an input. **(d)** Normalized activation response of the output neurons when combinations of red, green and blue are used as input. Clusters responding to yellow, cyan and magenta are the ones which are sensitive to red and green, green and blue, and red and blue colors, respectively.

After the training stage, every neuron within the output layer had a different synaptic weights combination according to the conductivity states found in the memristor's column of the output neuron, so a color could be assigned to it. Nearby neurons had similar colors assigned, as expected. Clusters of output neurons sensitive to one of the primary colors used during the training stage could be identified. An example of the obtained topographical pattern is depicted in Figure 4.10.b. The obtained pattern reappears in the crossbar if the ratio between the number of affected neighbors and the size of the output neuron layer is small enough. By changing this ratio, as stated

above, one can rather add redundancy to the system, or obtain larger clusters with the corresponding improvement in the resolution of the system performance. The specialization of the obtained output neuron clusters with a certain input neuron or a combination of them can be checked by plotting their activation, that is, the change in their output potential due to a certain input. The activation patterns of the simulated crossbar caused by single input activity, meaning that only one input neuron is active at a certain time, are shown in Figure 4.10.c. By means of comparing the output neurons activation as a response of the input data, the system is able to map and classify any combination of the presented colors to the most similar color cluster, behaving as a simple self-organizing neural network, such as a Kohonen neural network.

5.1 Variability impact on the self-organization performance

In order to test the robustness of the proposed OxRAM-based self-organizing map to the intrinsic cycle-to-cycle variability, the system was trained again for the color-mapping application considering different levels of the synaptic device cycle-to-cycle variability. To simulate the variability, the model parameters from chapter 3 have been calculated by performing Montecarlo simulations for different variability levels. The experimental G-V characteristics are shown with red lines in Figure 4.11, being the observed variability level referred to as low variability (LV), since the impact of larger variability levels is studied. G-V characteristics examples of simulated devices with a cycle-to-cycle variability larger than to the one observed experimentally, referred to medium variability (MV), are also depicted in Figure 4.11 (blue lines). Another example for device with an extreme large variability level (HV) is represented with gray lines in Figure 4.11.

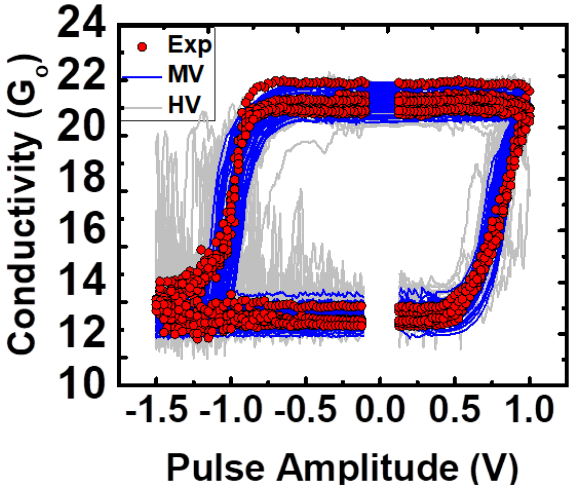

Figure 4.11: Experimental G-V characteristics (red dots). Simulation assuming MV (blue lines), similar to the one experimentally observed, and HV (gray lines).

Following the above described training algorithm, 3x100 crossbar arrays with the same initial weights were trained during 5000 iterations, with a random input data set and for the following cases: the modeled G-V characteristics, MV and HV. The distribution of the normalized initial weights is depicted in Figure 4.12.b. The gray-scale legend is shown in Figure 4.12.a. The normalized synaptic weights of the obtained self-organized crossbars obtained assuming any variability (as in the previous subsection), MV and HV are shown in Figure 4.12.c, 4.12.d and 4.12.e, respectively.

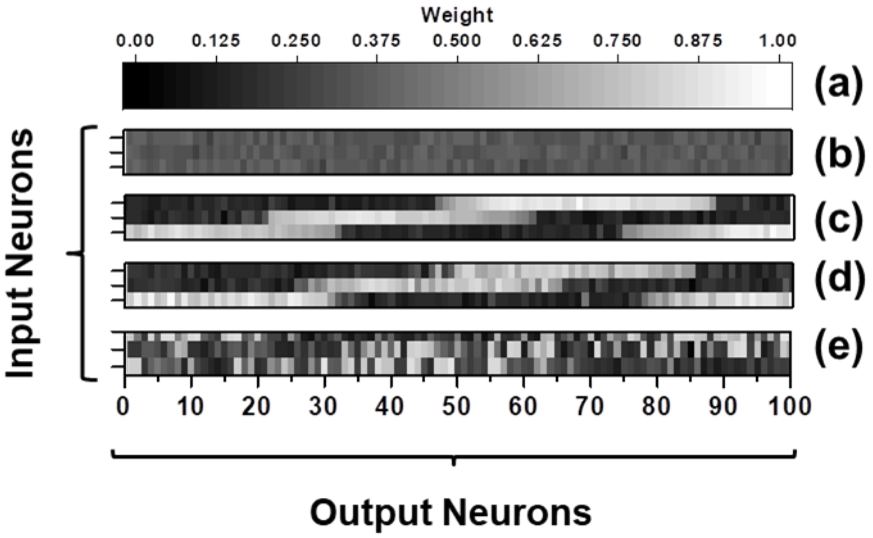

Figure 4.12: **(a)** The normalized conductivity state of the devices is identified as the synaptic weight, represented in a gray scale. **(b)** Randomly initialized 3x100 RRAM crossbar, with initial weights between 0.3 and 0.4. Synaptic weight distributions after the training, for the **(c)** LV, **(d)** MV, and **(e)** HV cases.

According to the final synaptic weights within a synaptic column, each of the output neurons represents a linear combination of the three primary colors, which could result in any possible color (except black). Representations of the color that each output neuron has assigned are shown in Figure 4.13, for the ideal (4.13.a), MV (4.13.b) and HV (4.13.c) cases. The LV crossbar shows spatial (topographical) organization of color, where seven color clusters are observed. In here, nearby neurons represent similar colors, meaning that they respond to a similar input (e.g. a red color), whereas distant neurons tend to be sensitive to opposite primary colors (green and blue), as observed in the previous simulation. The overlapping between the clusters of neurons sensitive to the stated primary colors gives rise to the ability to identify the so-called substractive colors, such as cyan (combination of green and blue); magenta (red and blue) and yellow (red and green). Each of the clusters was then labeled according to the color for which its neurons react: the cluster located at the left of the crossbar corresponds to blue, next to it, cyan, then green, yellow, red, magenta and lastly, blue again. This topographic organization can be observed in the synaptic weights and the output neuron color distribution for the LV (Figure 4.12.c and Figure 4.13.a) and MV (Figure 4.12.d and Figure 4.13.b) cases, whereas the clustering capability is lost when HV is considered (Figure 4.12.e and 4.13.c).

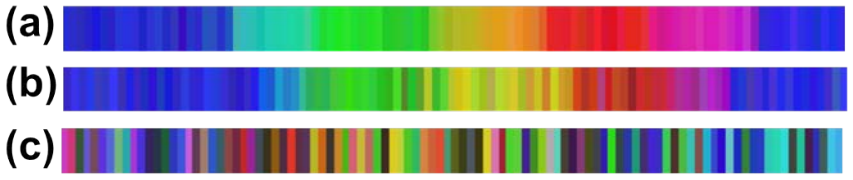

Figure 4.13: Each neuron within the output layer has a color assigned which results from the linear combination of the red, green and blue components. These primary colors are the inputs of the crossbar array, and are weighted by each of the synapses of every output neuron. The output neuron layer is represented as a color spectra for the **(a)** LV, **(b)** MV and **(c)** HV cases.

For the above mentioned image color clustering application, extra circuitry (not necessarily neu-

romorphic) would be required to decode the activation of a color cluster (i.e. the activation of a particular region within the output neuron layer) to a system output, providing the system answer to the following question: which is the predominant color of this pixel? The input of this decoder was considered to be the activity of the output neurons, which was measured in terms of the accumulated charge for a particular input color. The accumulated charge within a color cluster can be summed up in order to determine which color cluster reacts most to a particular input.

In Figure 4.14, the accumulated charge level within the output neuron layer of the simulated maps (output neuron response profile) is depicted for the following inputs: pure green, red and blue, and a mix of green and blue (cyan). In Figure 4.14.a, the output neuron response profile is shown for the LV case, Figure 4.14.b for MV, and Figure 4.14.c for the HV system. When LV is considered, the primary colors lead to a higher number of recruited neurons, displaying constant amplitude profiles (the whole cluster of neurons reacts); while a substractive color such as cyan leads to a three-level amplitude response, meaning that the neurons located in the overlapping region of two color react best, as expected. On the other hand, when HV was tested, the output neuron profiles for different colors were indistinguishable. Hence, the system capability of identifying colors according to the spatial location of the activated neuron cluster is lost.

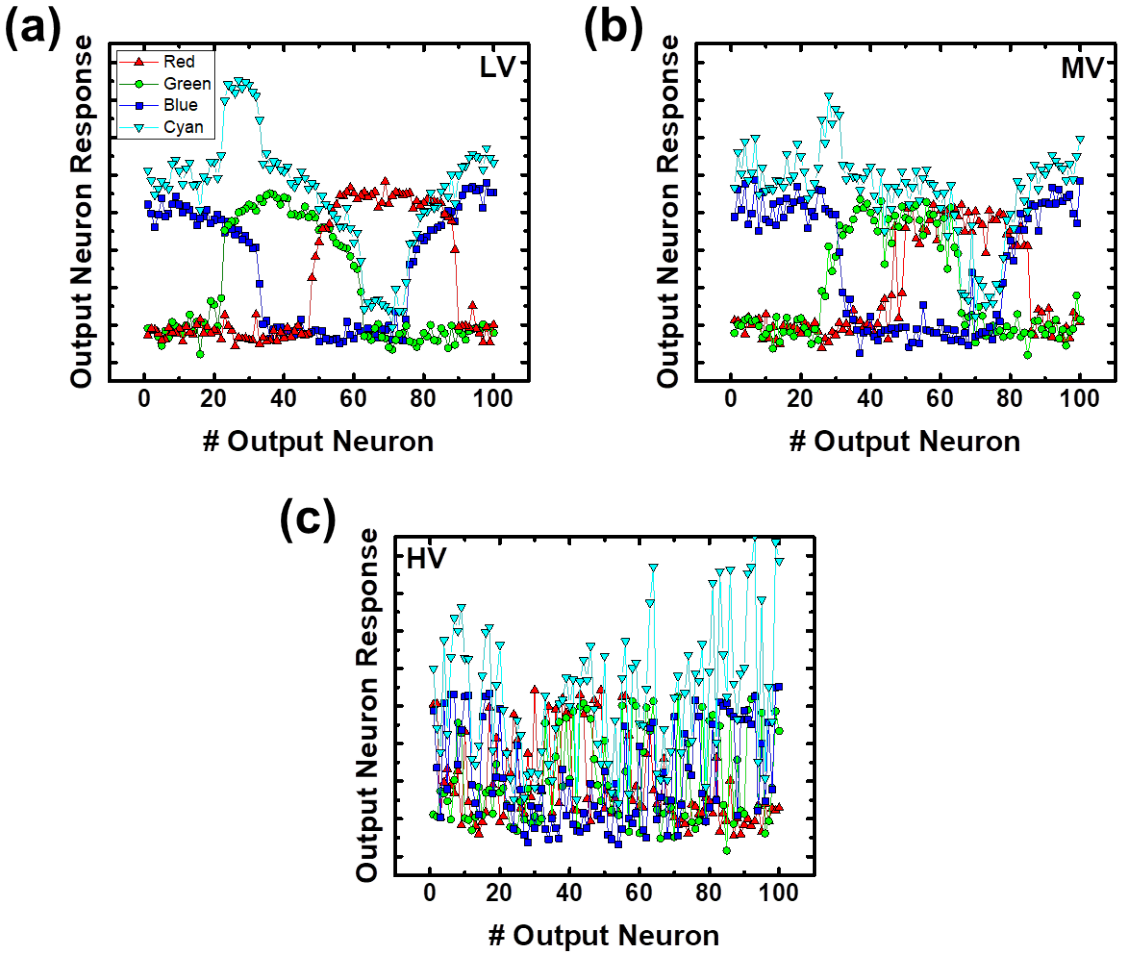

Figure 4.14: Output neuron response profiles to pure green, blue, red and cyan colors assuming **(a)** LV, **(b)** MV and **(c)** HV.

As to provide a visual example of application to illustrate the cycle-to-cycle variability impact,

a simple image compression task was performed. The task consisted in the identification of the predominant color of every pixel within an image, which can be used for color-pattern recognition tasks, or image compression, also referred to as image clustering [108] [109]. For this application, each of the pixels of the image depicted in Figure 4.15.a is entered to the crossbar as an input. The pixel has previously been decomposed in its red, green and blue (RGB) components. The image is first processed by assigning the color related to the output neuron cluster which shows a higher response profile (Figure 4.15). The image of Figure 4.15.a is then reconstructed displaying only the additive and substractive primary colors (red, green, blue, magenta, yellow and cyan). The image processed by the ideal system is shown in Figure 4.15.b. An example of application could consist in identifying which areas of the image present the combination of the green and blue components, which equals to the signalization of a cyan-colored area.

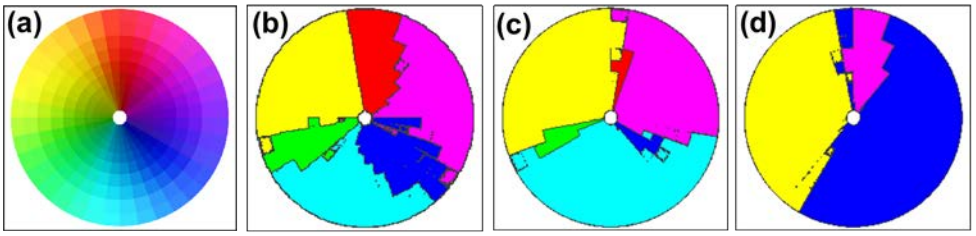

Figure 4.15: **(a)** Original image to be processed. Next, image processed by the **(b)** LV, **(c)** MV and **(d)** HV systems.

Regardless of the variability of the synaptic devices, due to the obtained topographical organization with overlapping output neuron clusters, the simulated LV and MV system can distinguish the cyan color despite of never have been introduced to it: the cyan, magenta or yellow colors were never used as input data during the training of the network. Hence, the proposed learning algorithm provides the system with resilience against the synaptic devices variability. On the other hand, its tolerance has a certain limit: as seen for the extreme HV case, there is no clustering in the output neuron layer, thus the system is not able to identify and map the input data set features according to its spatial location within the output neuron layer.

6 Hierarchical self-organizing neural networks

The design of the proposed self-organizing map is based on the fact that there is no difference in the electronic design and behavior between the input and output neurons. Because the training scheme is based on hardware-adapted unsupervised learning techniques, it is possible to concatenate multiple crossbar arrays, where information can flow in a bidirectional manner. By means of adding computing layers to a self-organizing neural network, hierarchical computation can be achieved. A simplified analogy of multisensory integration is exposed below, in order to illustrate a hierarchical computing application to be implemented with three layers of the proposed neuromorphic system. Multisensory integration encompasses primary sensory processing areas, such as the visual and auditory primary cortices of the mammalian brain, which present topographical organization, and a higher-order processing region such as the association areas, which constitute the largest area of the cortex in primates, where the pre-processed information is combined to form complex knowledge or perceptions.

Three self-organizing hardware networks are considered for providing an example of application, as shown in Figure 4.16.b. Two of the systems constitute the layers of the first level of hierarchy, and are able to process input information coming from different sources in parallel. One system is in charge of processing visual (colors) data, such as shown in the previous subsection (Figure

4.16.a left), where the colors are mapped according to their RGB components. The other one is specialized in processing audio (sound frequencies) signals, being the classification of the frequency of English vowels a simple case, by means of mapping their first and second formant frequencies (Figure 4.16.a right part). The response of the output neurons of this first level of the hierarchy is in turn fed to the layers of the next hierarchy level, where the pre-processed information is clustered again. At this level, association processes can take place, giving rise to symbolic learning. Relationships between colors and sounds can be learned: the blue component of an image and a low-pitch sound (such as the 'blue' word in English [ˈblu], the red color component and the frequency components of the vowel 'e' in the word 'red' [ˈrɛd], and the green component paired with the sound of the 'i' phoneme within the word [ˈÉąriËŘn]. This higher level of the hierarchy would compute the symbols of 'blue', 'green' and 'red', which relate the colors with the sound of its names in a particular language.

In this way, the system is not only able to classify information into a higher level of abstraction, identifying both blue-colored pixels of an image and low-pitch sounds as the 'blue' symbol, but also knows that there is an association between a particular pair of color component and sound frequency, which is made through this higher level layer. Because the information can flow in a bidirectional manner through the synaptic layers, a spiking neuron from the auditory layer can provoke the activation of a neuron related to the color-processing area, if both of them are related to the same symbol. If a neuron corresponding to the blue symbol within this higher level of hierarchy is activated, the system can track backwards its knowledge, and remember which color corresponds to blue, or how does the vowel within "blue" sounds, by means of activating its relative neurons from the lower hierarchy levels.

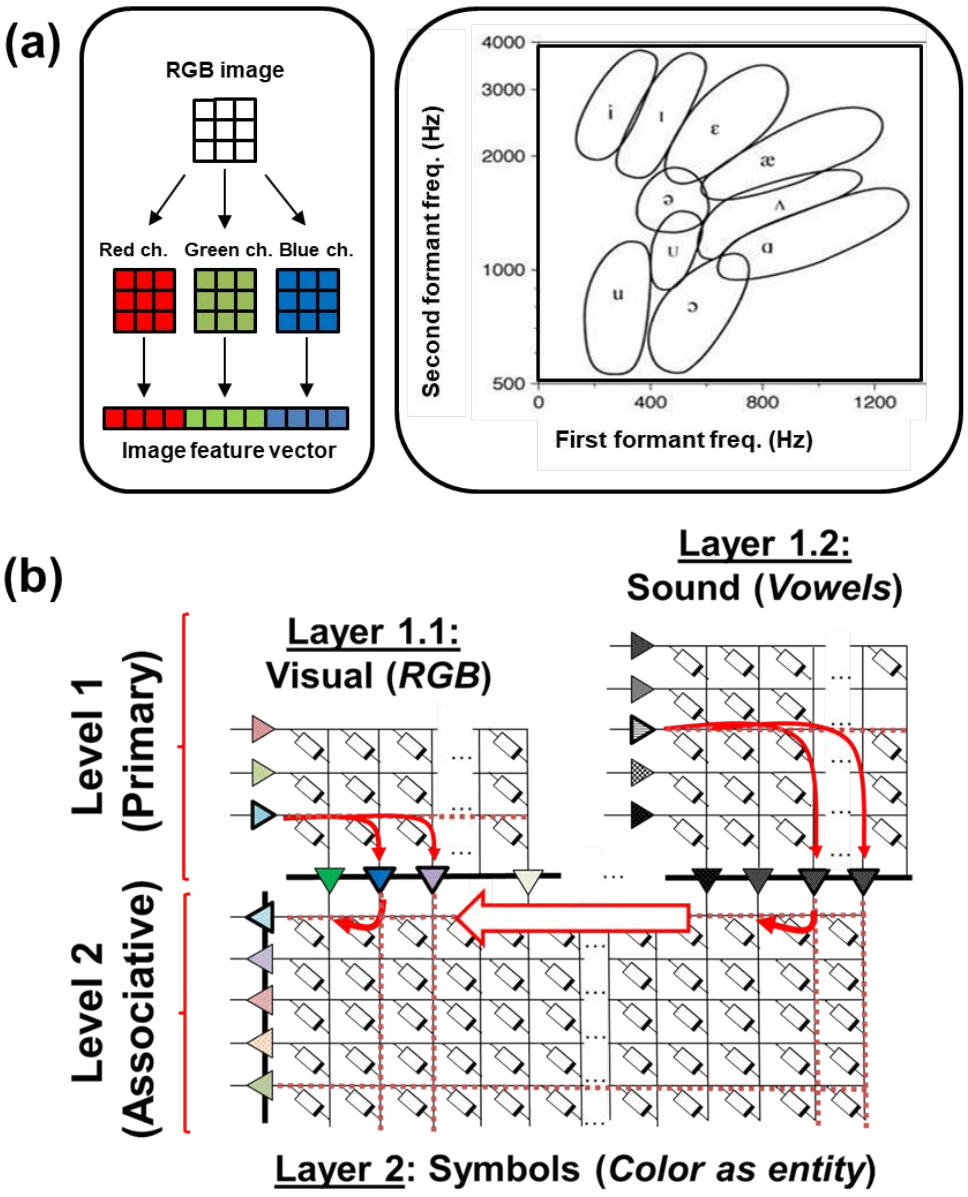

Figure 4.16: **(a)** Diagrams of the input data features to be processed by the systems within level 1. (Left) The task of the visual system (layer 1.1) corresponds to mapping color shades according to their RGB components. (Right) The system from layer 1.2 is in charge of mapping audio signals, in particular the English vowels sounds, according to their formant frequencies. **(b)** Scheme of the hierarchical system consisting in two levels of hierarchy. In level 1 (primary level), there are the two layers in charge of the processing individually the visual (layer 1.1) and the audio (layer 1.2) features of the input data set. Level 2 consists in a single associative layer, in which the association between the visual and audio data is made.

7 Summary

In this chapter, a fully-unsupervised learning algorithm is proposed. The algorithm has the objective to provide the self-organizing feature to a neuromorphic system, to be learned on-line and without requiring the calculation and propagation of the error, as occurs with supervised learning techniques. It is the first self-organizing algorithm adapted to a hardware system, in which

the topographical organization of the output neurons' specialization is aimed. Applications of the self-organizing map (SOM) include any related to data classification through mapping (hence the name of the network), to be used specially in cases where there is not any model describing the relationship between the input data set features.

The proposed SOM algorithm is tested by simulation on a neuromorphic system with integrate and fire neurons and analog memristive synapses. No electrical model is used for the neurons, being its electronic design out of the scope of this thesis. Their behavior is included mathematically. On the other hand, experimental G-V characteristics fitted to the hysteron model are used to simulate the synaptic devices. The initial conductivity states have to be randomized within an intermediate conductivity state range, in order to trigger the self-organization process of the neuromorphic neuron. This requirement is naturally full-filled with the intrinsic variability of the devices, as seen in previous chapters.

Three bio-inspired learning rules are considered, being the first one the STDP property of the electronic synapses. In order to provide a symmetrical and linear weight updating, a pair of pre and post-synaptic waveforms is proposed and tested with the G-V characteristics model. The other learning rules are the lateral neighbor interaction, and the competition between synapses within the same synaptic column (related to the same output neuron).

A color-mapping map is shown as an example of application. The input data set is chosen to be as simple as possible, in order to (1) test the first version of the learning algorithm, (2) study the variability impact on the system performance. It has been demonstrated that the algorithm supplies the system with resilience against the variability or noise, as expected in a neural network.

The proposed network design and algorithm allow to concatenate maps in order to build a multilayer hierarchic neural network (HSOM), in which more complex computation tasks can be achieved through an associative learning process, such as the one proposed in the previous chapter. Association between input data sets coming from different sensors or other networks can be established, so the output neurons of the top-level of the hierarchy would be specialized to concepts, instead of to simple features or variables. In this way, an associative in memory-computing system could be achieved parting from simple crossbar arrays.

Chapter 5

OxRAM devices as binary stochastic synapses

1 Introduction

In contrast with analog synapses, binary stochastic synapses do not actually rely on small reliable changes on their conductivity state within a specific range, thus relaxing the constraint of avoiding abrupt or probabilistic transitions between the available levels. In here, a conductivity threshold is defined, and the electronic synapse is rather active or not, if their conductivity state is above or below this threshold, respectively. Binary synapses are meant to provide a solution to the intrinsic device variability of analog synapses, which increases when scaled-down in terms of area [31], or when weak programming schemes are considered [31] [29], and affects to the linearity and reproducibility of the weight updating of analog synapses [31] [30]. However, the trade-offs of employing binary synapses in contrast with analog synapses are that a higher number of synaptic devices are required for online training, therefore increasing the system area and its power consumption [29, 30].

Usually, binary synapses are employed in artificial deep learning neural networks, such as the convolutional neural networks (CCN) where multiple synaptic layers are considered, under supervised learning training schemes. Implementations with memristive devices include STT-MRAM [115] [116], CBRAM [31] and OxRAM [29] [30] [56] [116]. In [30], a 16Mb OxRAM-CMOS macro-chip consisting of three neuronal layers was proved to present a high learning accuracy ($\sim 96.5\%$) for the MNIST database benchmark [117], being the proposed implementation also applicable to SRAM, PCM or MRAM technologies. In [56], a CNN achieving high learning performances was demonstrated through simulation, where the implementation of a synapse involved the use of multiple (from one to twenty) OxRAM devices as to provide an analog behavior of the synapse. In here, a stochastic STDP rule (unsupervised learning) was combined with a back-propagation algorithm, which is a supervised deep learning technique, in order to train the system.

Binary synapses can also be used in smaller neural networks with only one synaptic layer, being the manufacturing of the corresponding neuromorphic architecture more simple and feasible. Moreover, neuromorphic systems are attracting a lot of interest towards implementing real-time adaptive systems for a variety of applications. Real-time learning requires the system to continuously adapt to time-varying inputs in an autonomous way. Hence on-line learning without external supervision is preferred in this case, so that unsupervised learning rules to be implemented uniformly across the whole network are of great interest. An example of this concept can be found in [29], where a unsupervised learning scheme was implemented in a simulated winner-takes-it-all two-layer neural network. In here, the SET probability of the OxRAM-based binary synaptic devices provided an electrical history-dependence, enabling its use as a learning rule for an orientation classification

task. According to [29], the use of the tested OxRAM devices as binary synapses improved the orientation selectivity of the network, compared to a system in which the same OxRAM devices were employed as analog synapses, with the same network storage capacity. However, the total energy consumption of the system resulted to be higher in the binary-synapse system. A similar learning rule is presented in [118], where the RESET probability of OxRAM devices under low-current programming was studied as the main local learning rule, to be employed in a bio-inspired fully-unsupervised training algorithm, involving the learning and prediction of temporal sequences.

In this chapter, the results of a study similar to the one found in [118] concerning binary synaptic devices are exposed. The study was carried out during a three months internship (July 2018 - September 2018) at imec (Leuven, Belgium) within their machine learning program. Binary synaptic devices were electrically characterized and modelled with the objective of testing the bio-inspired temporal-sequence learning algorithm on a hardware neuromorphic system. Concretely, an OxRAM and CMOS-based chip supported by an FPGA board was first electrically characterized, and the individual device behavior was modelled. The possibility to simultaneously testing a large amount of devices allowed extracting the required statistical data as to verify a history-dependent probabilistic learning rule. The model was used to find the electrical parameters required to implement the learning algorithm on the chip. Next, the FPGA was programmed with Python in order to test the learning algorithm performance for a temporal-sequence prediction application, still being under testing. An introduction to the bio-inspired learning algorithm is also given, in order to provide a link between the RESET probability learning rule and the temporal sequence learning capability of the chip.

2 Tested samples and characterization setup description

The tested OxRAM samples were provided by imec, and consist of a 3nm-thick $TaOx-$ based layer and 5nm-thick Ta capping between the TiN bottom and top electrode (BE and TE respectively). Data was collected from a 1Mb $TaOx-$ based-based RRAM array fabricated with 65nm CMOS, packaged and placed on a board alongside off-chip DACs and ADCs, all driven by a XilinX FPGA. Figure 5.1.a shows a TEM cross section of part of the array, showing the 60nm active memory element, and the electrically inactive dummies at 200nm pitch. Figure 5.1.b depicts a scheme of OxRAM stack. Figure 5.1.c shows a picture of the FPGA supporting the tested chip.

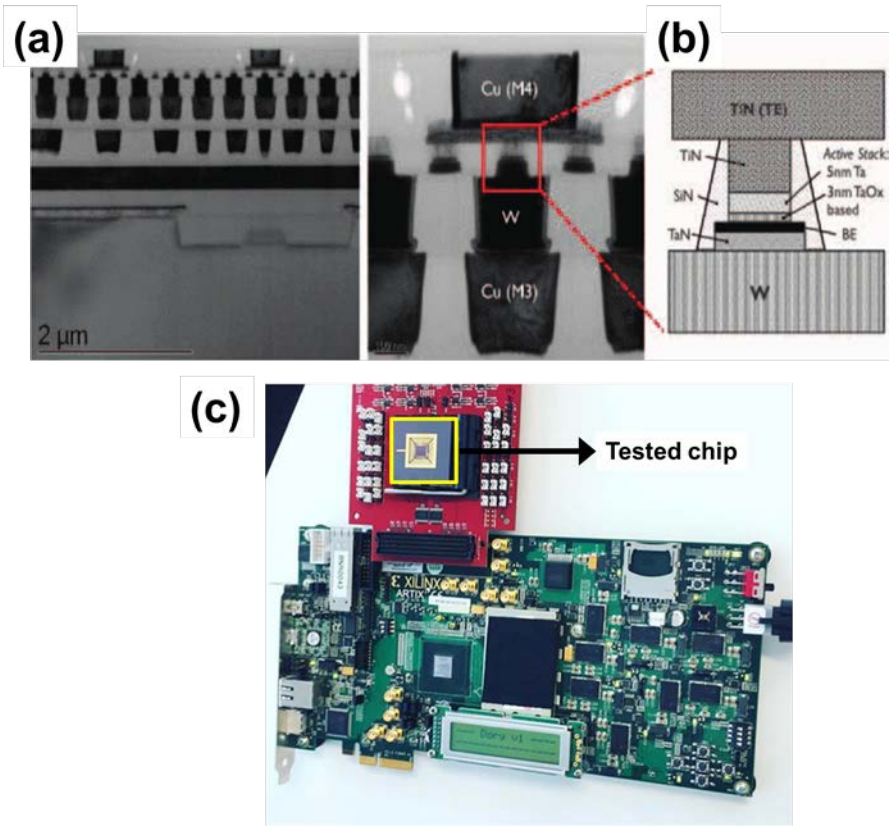

Figure 5.1: **(a)** TEM cross section of part of the 1Mbit TaOx-based OxRRAM array, showing the 60nm active memory element and the electrically inactive dummies at 200nm pitch. Extracted with permission from [118]. **(b)** Composition of the TaOx-based memory stack. **(c)** FPGA supporting the tested chip.

3 Low compliance current pulsed characterization

3.1 Test scheme

The OxRAM devices were characterized by means of applying multiple pulses while controlling the compliance current I_c, with the aim of verifying how multiple potentiating pulses (referred to as SET pulses) drastically lower the RESET probability at low-voltage, following the same procedure found in [118], in which the measurements were done at wafer-level. In here, the SET pulses are positive polarity pulses, and on the other hand, the RESET pulses are pulses with negative polarity. All of the applied pulses have a pulse-width of 100ns.

A diagram of the test scheme is shown in Figure 2, consisting of first performing **(a)** a forming stage, where all the tested devices were formed at the same I_c by means of applying a SET pulse with amplitude 3.25V. Then, **(b)** a hard RESET pulse was applied to all of the devices (-1.5V). The test followed with **(c)** the application of multiple consecutive current-controlled hard SET pulses (1.5V) using the same I_c as in the forming stage, and lastly, **(d)** 1000 soft RESET pulses with different V_{reset} values. The resistance states of the devices were read after each event by means of applying a voltage of 0.1V. This test scheme was executed for different values of I_c on different groups of samples. The number of applied hard SET pulses and their effects on the RESET probability was also studied. The employed test parameters are summarized in Table 5.1.

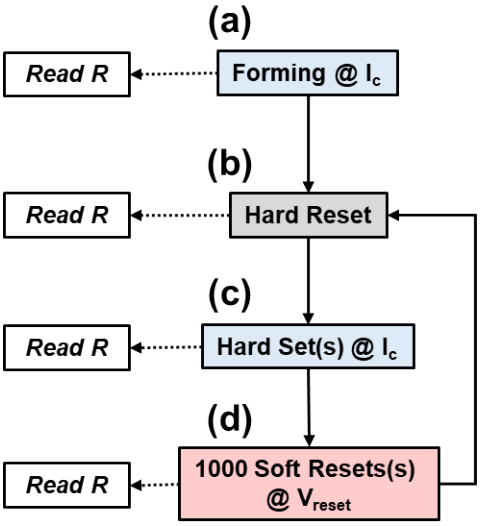

Figure 5.2: Flux diagram of the performed test.

Test parameters		
$I_c(\mu A)$	Soft RESET @ V_{reset} (V)	# Hard SETs
25	−0.6	1
50	−0.7	10
106	−0.8	50
200	−0.9	

Table 5.1: Employed measurement parameters. All the possible combinations of test parameters were tested.

3.2 Results

A total of 4 groups of 128 devices were tested using the different I_c values shown in Table 5.1. Table 5.2 displays the coordinates of the devices (where R W:X and C Y-Z denote that the group of devices is located within the W and X rows, and the Y and Z columns of the 1Mb chip), the I_c parameter, the gate voltage V_g applied to the transistor in order to control the I_c, the median of the measured resistance states and their standard deviation. In Figure 5.3, the cumulative distribution functions of the resistance states after the forming stage are depicted for all of the employed I_c values. It can be seen that the distributions shift to the right for decreasing I_c, being the median values between 3.62KΩ and 14.81KΩ. The standard deviation also increases potentially for decreasing I_c.

Coordinates	$I_c(\mu A)$	Soft RESET @ V_g (V)	MedianR(KΩ)	Standard Deviation KΩ
R 0:1 C 0:63	25	0.85	14.8123	10.5147
R 2:3 C 0:63	50	0.95	8.6106	2.1311
R 4:5 C 0:63	106	1.00	6.8808	0.9788
R 6:7 C 0:63	150	1.15	4.0730	0.3090
R 8:9 C 0:63	200	1.20	3.6201	0.2626

Table 5.2: Coordinates of the devices tested under the same test conditions, employed I_c and corresponding V_g values, median and standard deviation of the resistance states measured after the forming stage.

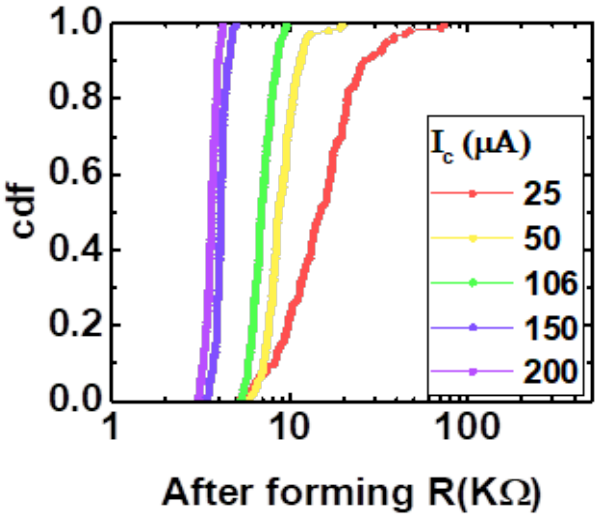

Figure 5.3: Cdfs of the resistance states after the forming stage.

In Figure 5.4, the cdf plots of the resistance states corresponding to each of the following test hard RESET (Figure 5.4.a) and hard SET (Figure 5.4.b) stages are grouped. For both events and for increasing I_c, the median and the standard deviation values decrease.

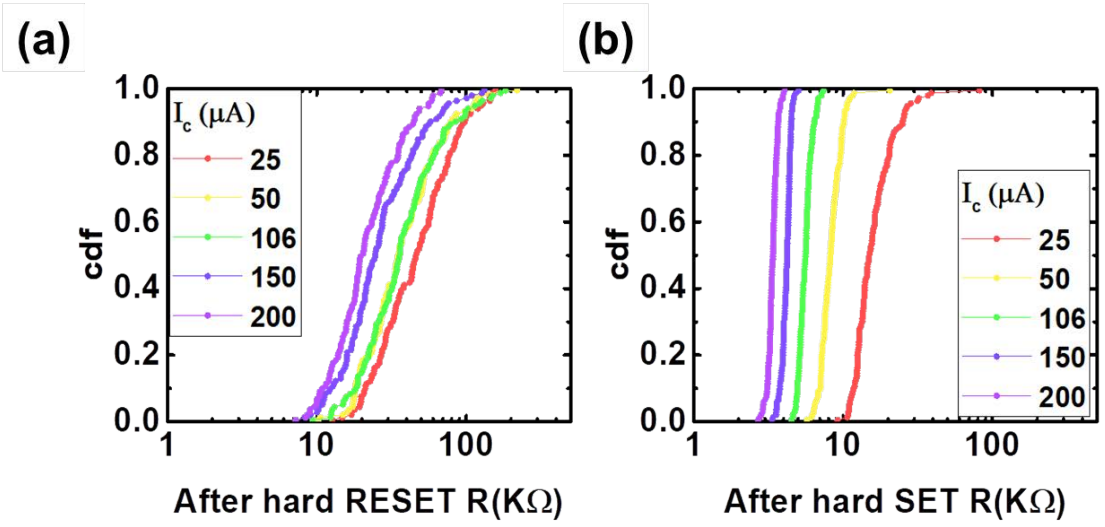

Figure 5.4: Cdf plots of the resistance states after the hard RESET **(a)** and hard SET **(b)** events.

The resistance state medians after 0 (none), 1, 10, 100 and 1000 soft RESET pulses applied after a single hard SET pulse are depicted in Figure 5.5, as a function of the employed I_c. In here, each subplot corresponds to a different V_{reset} value. These results show that for increasing number of consecutive applied soft RESET events, the resistance state median increases, being dependent of the I_c used during the forming and hard SET stages. For higher I_c values, larger V_{reset} values are required in order to increase the resistance state of the devices.

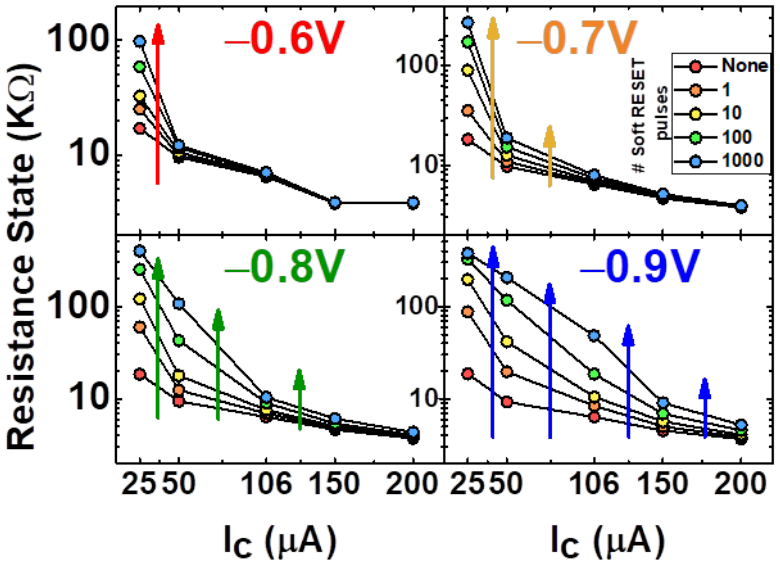

Figure 5.5: Resistance state median after the soft RESET events over the employed I_c during the forming and hard SET stages. Each plot corresponds to different soft RESET pulse amplitude V_{reset} values. The curves within the subplots indicate the number of applied soft RESET pulses.

Figure 5.6 shows the resistance states of two particular examples of I_c: 25μA (Figure 6.a) and 106μA (Figure 5.6.b) for V_{reset} values of âĹŠ0.6V and âĹŠ0.7V respectively, represented over the number of applied soft RESET pulses. The curves depicted in each subplot are related to a different number of applied hard SET pulses (1, 10 and 50). The resistance states median values within each subplot are similar after a single soft RESET process, being around 25kΩ and 6.25kΩ for the

25μA and 106μA cases, respectively. However, for increasing number of soft RESET pulses, the dependence on the previous number of applied SET pulses is stronger, especially for the lower I_c value.

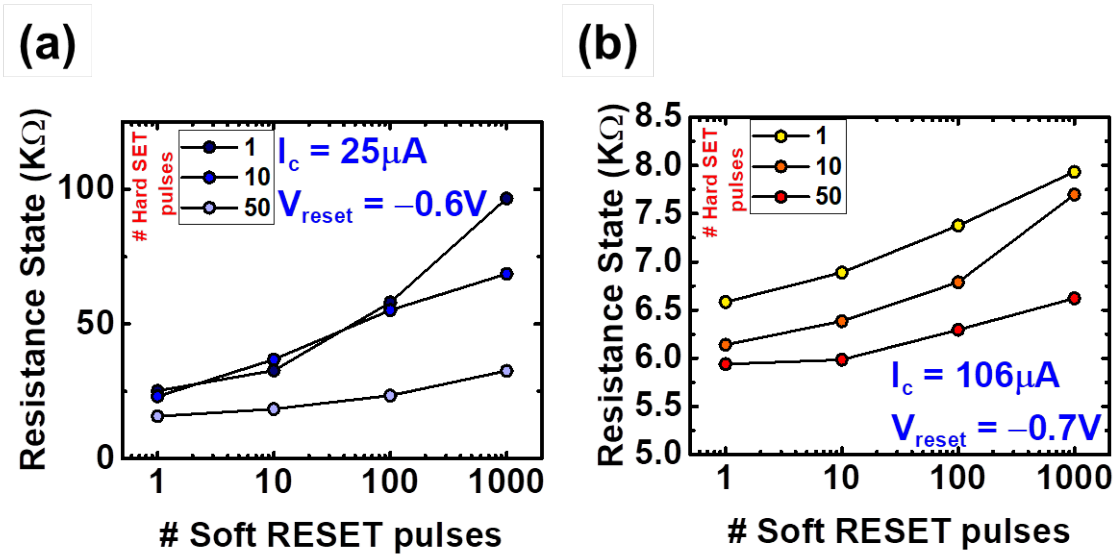

Figure 5.6: Resistance state median values over the soft RESET pulses, for two particular cases of I_c and V_{reset}. The curves within the subplots indicate the number of applied hard SET pulses. **(a)** I_c=25μA and V_{reset}=âĹŠ0.6V. **(b)** I_c=106μA and V_{reset}=âĹŠ0.7V.

Lastly, Figure 5.7 shows the devices resistance states evolution (gray lines) through the number of consecutive applied soft RESET pulses, for the particular case of 1 hard SET event using I_c = 50μA. It can be seen that individual devices present a stochastic behavior in terms of unpredictable increasing and decreasing resistance shifts. A few examples are highlighted as black lines. Despite of the observed stochastic RESET trend, the median resistance (red line) increases gradually with increasing number of soft RESET pulses. It is concluded that the RESET process in these devices under the employed test conditions should be interpreted as a probabilistic event. Therefore, the tested devices are not able to be employed as analog electronic synapses, because their resistance state cannot be finely tuned with a fixed range, but rather as binary stochastic synaptic devices, for which a resistance threshold should be defined in order to determine if the synapse is active or not.

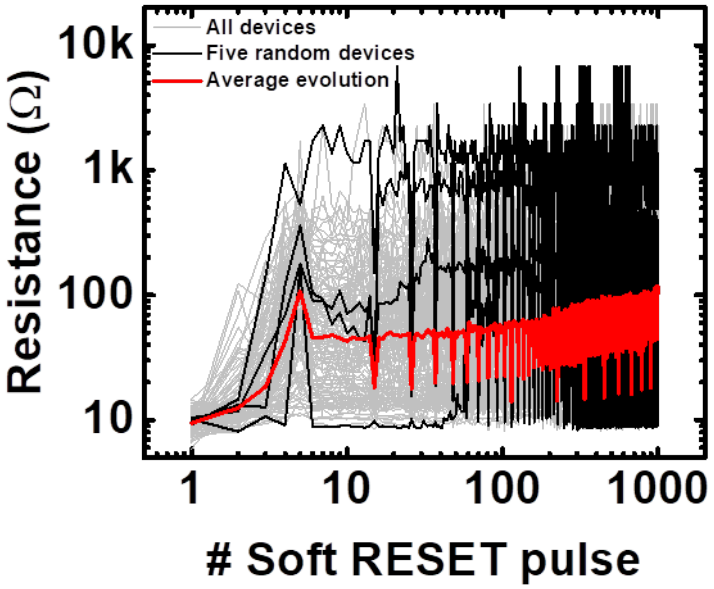

Figure 5.7: Resistance state evolution of all of the tested devices (gray lines) over the soft RESET pulses. A few examples are highlighted in black, showing that the resistance state shifts unpredictably. The median, which is depicted in red, increases gradually with the number of applied soft RESET pulses.

These results of the performed electrical characterization are in accordance with the ones obtained in [118], being the only difference between the characterization procedures, the test setup: wafer-level with probe-station versus packaged chip supported by FPGA. As to summarize, the more SET events are applied, the more resilient becomes the device resistance state to soft RESET pulses. This SET-history dependence can be tuned by modulating the V_{reset} and the I_c parameters, leading to a history-sensitive probabilistic RESET behavior of the samples, to be used as binary synaptic devices.

4 Resistance threshold and conditional probabilistic RESET modelling

The results of the electrical characterization detailed in the above section suggest that the tested devices can be employed to implement binary stochastic synapses. In order to do that, a resistance threshold has to be defined, indicating the boundary between the activation and deactivation of a particular electronic binary synapse. In this section, a thresholding process is performed in each of the experimental datasets. Then, the probability of efficiently inducing a RESET process in a device, meaning that its resistance state is above the threshold, can be studied. Finally, a RESET probability model is used to fit the obtained probability distributions, providing a model of the conditional RESET probability, used to simulate the tested devices behavior as binary stochastic synapses.

The thresholding process consisted in setting a resistance threshold R_{thr} for a given dataset test conditions, meaning that for all of the devices sharing the same I_c and V_{reset} employed during the previous electrical characterization, the same thresholding value was employed. The resistance states of the devices after each consecutive soft RESET pulse were evaluated in terms of this threshold, and only the devices whose resistance states were above the defined threshold were taken into account for the RESET probability calculation. By means of doing this process, the

cdfs of the RESET probability as a function of the applied hard SET pulses (being 1, 10 or 50 SET pulses) and of the applied soft RESET pulses (up to 1000) were obtained for different resistance thresholds. An example is shown in Figure 8, for the particular case with the following conditions: I_c=106μA, V_{reset}=0.8V and R_{thr}=8KΩ. In general, an increasing number of preceding hard SET events decreases the cumulative RESET probability.

The obtained cdfs of the RESET probability Pr were fitted to expression 5.1 (black curves in Figure 5.8):

$$P_r = low + \frac{up - low}{1 + exp\Big(- \frac{ln(N_r) - loc}{scale}\Big)} \tag{5.1}$$

Where up and low define the vertical boundaries of the cdf, Nr is the number of applied soft RESET pulses and loc refers to the location parameter of a probability distribution function. The scale parameter is also characteristic of a probability distribution function, and was fixed for datasets obtained with the same test conditions, except for the number of applied hard SET pulses value.

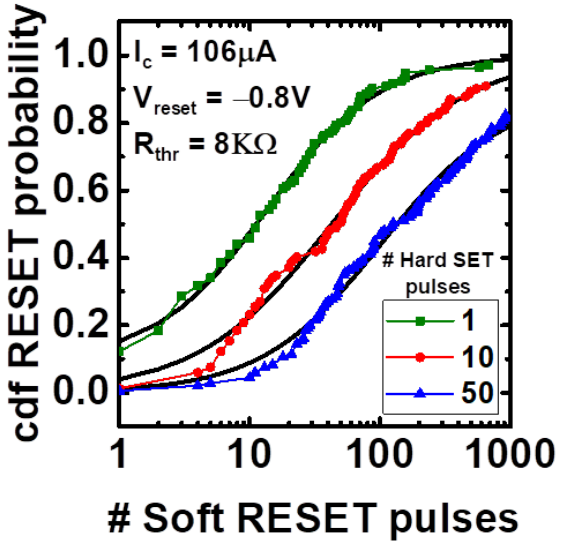

Figure 5.8: Cdfs of the RESET probability after the application of 1 (green squares), 10 (red circles) and 50 (blue triangles) hard SET pulses, as a function of the number of applied soft RESET pulses, for the particular case with I_c=106μA, V_{reset}=âĹŠ0.8V and R_{thr}=8KΩ.

An example of the obtained location parameters for different V_{reset} values is shown in Figure 5.9 (I_c=106μA and R_{thr}=8KΩ), where it is represented as a function of the number of applied hard SET pulses. A linear fitting (black lines in Figure 9) was performed, so that the location parameter for a particular number of hard SET pulses could be interpolated. It can be seen that, for lower voltages, the location parameter shift is more pronounced.

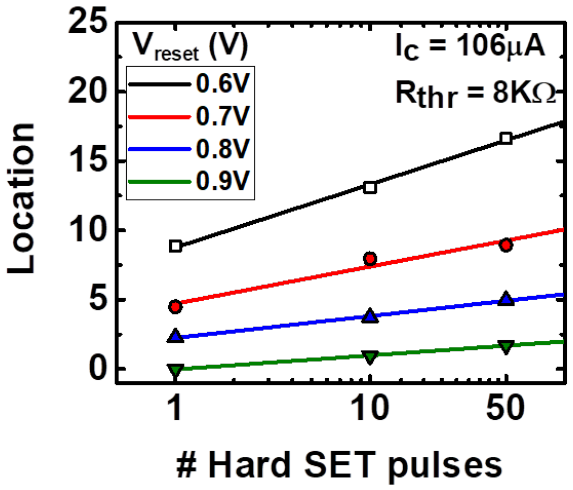

Figure 5.9: Location parameter as a function of the number of applied hard SET pulses, for different V_{reset} values.

Finally, the conditional RESET probability function was obtained by means of taking the derivative of the RESET probability Pr over the number of applied soft RESET pulses, computed according to equation 5.2:

$$\frac{dP_r}{dN_r} = \frac{up \cdot exp\left(\frac{loc}{scale}\right) \cdot N_r^{\frac{1}{scale}-1}}{scale\left(exp\left(\frac{loc}{scale}\right) + N_r^{\frac{1}{scale}}\right)^2} \tag{5.2}$$

Examples of conditional RESET probabilities are shown in Figure 5.10, for two different test conditions and different values of R_{thr}. In both cases, for increasing number of preceding applied hard SET pulses, the conditional RESET probability decreases.

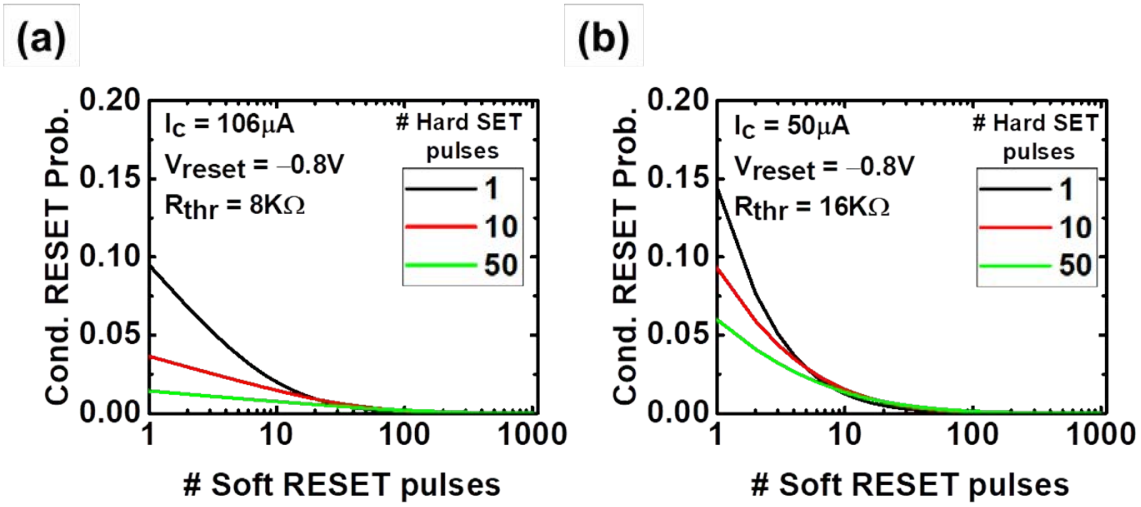

Figure 5.10: Conditional RESET probability for different number of applied hard SET pulses (1, 10 and 50) as a function of the number of applied soft RESET pulses for different test conditions. **(a)** I_c=106μA, R_{thr}=8KΩ and V_{reset}=-0.8V. **(b)** I_c=50μA, R_{thr}=16KΩ and V_{reset}=-0.8V. For increasing number of preceding applied hard SET pulses, the conditional RESET probability decreases.

The obtained model parameters were used as the input file of a simulator, where the conditional RESET probability was computed and used as the local learning rule within a learning algorithm, which is detailed in the last part of the this section.

Summarizing this section, the intrinsic history-sensitive probabilistic RESET property of these OxRAM devices, observed for these particular test conditions involving low current compliance, is exploited. The tested devices are considered as active computational synaptic elements, where the learning capability relies on the probability of a successful RESET operation at low RESET voltage and its large sensitivity to the programming history.

5 A bio-inspired temporal sequence learning algorithm

5.1 Introduction to the Hierarchical Temporal Memory model

In this section, a brief introduction to the Hierchical Temporal Memory (HTM) theory [119] is provided. The bio-inspired temporal sequence learning algorithm to be implemented in a neuromorphic system based on the tested binary synapses, which is inspired in HTM framework, is also detailed and compared to the adapted SOM algorithm proposed in the previous chapter.

The HTM is a bio-inspired computational neuroscience theoretical framework describing some learning mechanisms of the biological brain neo-cortex. In essence, it is considered as a learning model based on unsupervised learning mechanisms. The objective of the algorithm is to provide a neural system with the ability to recognize and predict temporal sequences of sensory inputs, being vital for survival in natural environments. The model is able to continuously learn a large number of variable order temporal sequences using an unsupervised Hebbian-like learning rule. It also exhibits properties that are critical for sequence learning, including continuous on-line learning, the ability to handle multiple predictions and branching sequences with high-order statistics, robustness to sensor noise and fault tolerance [119]. Applications of the HTM model and derived learning algorithms include temporal sequence learning for data generation, prediction and filtering, pattern recognition of real-time data, as well as for anomaly detection.

Hardware-adapted versions of the learning algorithm proposed in [119] are currently under study, in order to exploit and use the history-dependent probabilistic RESET learning rule demonstrated in the tested binary synaptic devices. A first adaptation is demonstrated in [118], where a simulated system shows the ability to generate periodic data sequences according to some rules learned during the training stage. In [118], two applications were tested. The first application was related to music: the system could compose minuets parting from the information retrieved from actual minuets, used as the input data set during its training. The latter application consisted in filtering the noise from a periodic signal, used as the input data set. The system could regenerate the periodic signal parting from an input signal with up to a 25% noise.

The main HTM model concepts are now summarized, since they are the basis of the temporal sequence learning algorithm to be used in the tested binary synapses. First of all, the HTM systems require data input in the form of Sparse Distributed Representations (SDRs) [120]. An SDR consists of a large array of bits of which most are zeros and a few are ones. Each bit carries some semantic meaning, so if two SDRs have more than a few overlapping one-bits, then those two SDRs have similar meanings. In Figure 5.11, three examples of SDRs are depicted. In here, SDR A and B show some similarity because the location of many of the '1' bits match. In contrast, SDR C does not share any '1' location with SDRs A and B. Then, SDRs A and B represent similar meanings, whereas SDR C does not.

The SDRs of an input data set can be obtained through a process called encoding. The encoding process is analogous to the functions of sensory organs of humans and other animals. The cochlea, for instance, is a specialized structure that converts the frequencies and amplitudes of sounds into a sparse set of active neurons [121] [122]. One important aspect of the cochlear encoding process is that each hair cell responds to a range of frequencies, and the ranges overlap with other nearby hair cells (Figure 5.12), so that a topographical organization can be observed in the cochlea and the primary auditive cortex (and as well in other sensory processing areas of the brain, as stated in the previous chapter). Having multiple neurons responding to the same feature of the input data, being a specific frequency in the case of the auditory system, provides redundancy: in case some hair cells specialized to a certain frequency are damaged, the system will still have the ability to process the input, since the same frequency excites multiple neurons. The topographical organization implies that two sounds with similar frequencies will have some overlap in the cells that are stimulated, providing the system with the following benefits: since the overlapping between representations is how the semantic similarity of the data is captured in the representation and it is distributed across a set of active cells, the representation of a certain input feature is tolerant to noise or sub-sampling. In this sense, the HTM model states that an encoder system task consists in providing a spatially-organized representation of the input data set features. Hence, the proposed SOM in the previous chapter could be used as a neuromorphic data encoder.

The HTM system the input data set to be encoded as SDRs. Next, the characteristics of a HTM algorithm are described. A HTM system consists in groups of neurons, which in contrast with a SOM, the groups or neuron clusters are already defined before the training stage starts. That is, the amount of available input and output neurons are previously divided in groups or neuron clusters, being each of them related to a target input feature. Depending on which of the neurons within the cluster is activated, the same input feature is represented in a different context. For instance, the activation of different neurons within a cluster can be related to the same input feature, being represented in different temporal contexts. During the training stage, relationships (i.e. connections) between the input features represented in different time contexts are grown. In this way, a prediction of a periodic sequence or anomaly detection can be performed by checking which neurons from different clusters (related to different input features) are connected, corresponding to different timings of the sequence. In order to provide an example, a digital sine signal S(t) with an amplitude of 50 (arbitrary units) to be used as an input data set, is shown in Figure 5.13. The samples of this signal can have one of the five possibles values (0, $\pm$29, $\pm$48). In this case, each of the neuron clusters has one of these values assigned. The activation of a particular neuron within a cluster indicates that a sample presents that value (for example, 29) in a particular temporal context. That is, different neurons within the cluster represent the 29 value when $dS(t)/dt > 0$, and others when $dS(t)/dt < 0$.

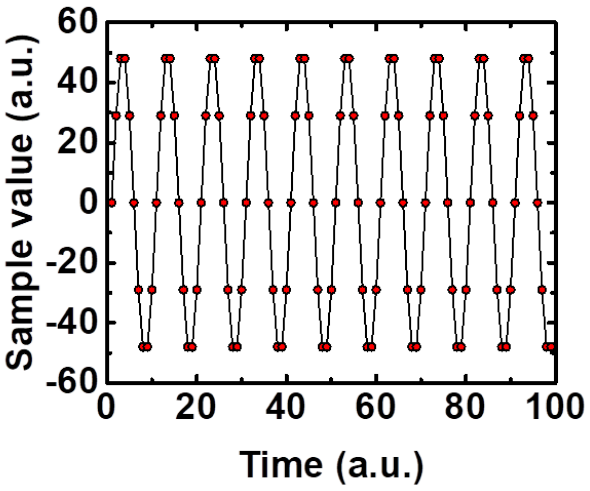

Figure 5.13: Digital sine signal, consisting on samples with five possible values.

A scheme of the HTM model implementation on a 2D neuromorphic array is shown in Figure 5.14, being the input and output neuron layers arrangement identical to the SOM of the previous chapter. In this case, the input and output layer present the same number of neurons, with the size and location of the clusters defined before the training stage begins. The input neuron layer provides a representation of the temporal sequence at a time t, whereas the output neuron layer represents the values of the temporal sequence at a time $t + 1$. In the case of 5.14, the clusters are of 64 neurons. Hence, there are 64x64 synaptic devices representing the relationships between the sequence value at t and at $t + 1$.

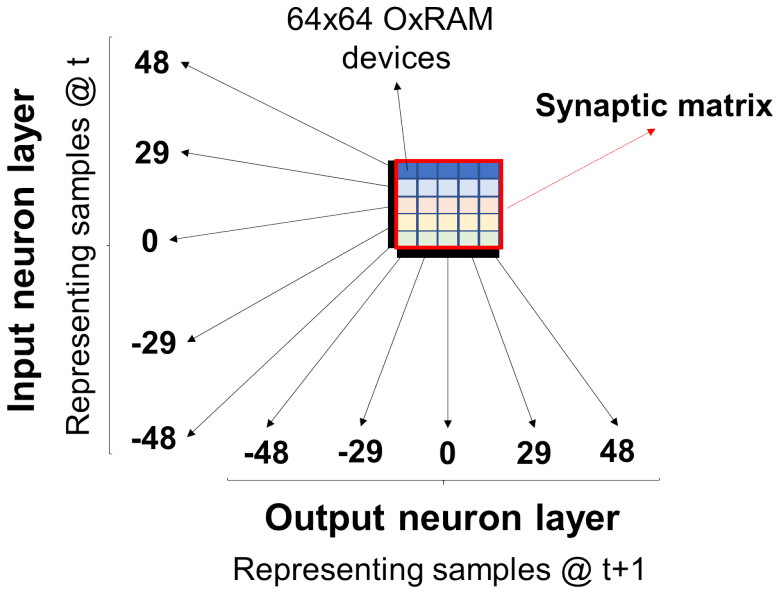

Figure 5.14: Implementation of the HTM model on a 2D square crossbar array. The input neuron layer represents the samples values at a time t, whereas the output layer indicates the values at a time $t + 1$. The input features are represented by groups of 64 neurons in each of the layers.

In contrast with the SOM algorithm, the synapses connecting neuron groups are considered to be binary. In particular, the analog synaptic weight is defined as the permanence of the synapse. The

permanence is always compared to a certain threshold, which determines if the connection (i.e. the synapse) is active or unconnected. In terms of the resistance state of an electronic synaptic device, if the permanence is above the threshold, given in Ω units, the synapse is considered to be unconnected, whereas if below, it is then an active synapse. This binary synapse state evaluation is related to the conditional RESET probability model of the tested binary synapses, for which a resistance threshold had to be defined.

5.2 Temporal sequence learning algorithm

As stated above, the learning algorithm to be employed on the system based on the tested binary synapses is based upon but modified from the HTM model. The steps of the temporal sequence learning algorithm are now described (a flux diagram is shown in Figure 5.15, using the simulation performed for training the system with the sine wave depicted in Figure 5.12 as an example. A particular set of V_{reset}, I_c and R_{thr} is chosen for testing the performance of the system, being of $V_{reset} = -0.7V$, $I_c = 106\mu A$ and $R_{thr} = 7K\Omega$. It is assumed that the representation of a sample at a particular time (its SDR for a particular temporal context) is complete if 8/64 neurons are specialized to that representation.

The training begins with **(a)** an initialization, where the OxRAM devices are formed with a particular low I_c value ($I_c = 106\mu A$). Due to device-level variability, the OxRAM devices present resistance state values within a range, following the probability distribution of Figure 5.3. Next, **(b)** the first sample of the sine wave sequence is applied to the system (e.g. the sample value is '0'), corresponding to the sequence value at t. Initially, a portion of the 64 neurons located in the input layer cluster representing the '0' is activated, and each of the active input neurons applies the reading voltage to the synaptic matrix. By means of this voltage, the state of the involved synapses is determined (being active or not, if its resistance state is below or above the threshold R_{thr}, respectively). A prediction by the system is then made, by means of checking to which neuron and cluster of the output layer are the active synapses connected. For the first training iterations, it does not matter which output neuron is activated, as long as it belongs to the correct cluster, corresponding to the sample value at $t + 1$. In this case, it corresponds to the output neurons representation of '29'. Next, **(c)** the actual value of the sequence at $t + 1$ is checked, and a synaptic weight updating takes place. If the active synapses do actually relate the sample value at t (input neurons within the '0' cluster) with the next value at $t + 1$ (output neurons within the '29' cluster), a SET pulse (1.5V) is applied to that synapses. If there are connections not supposed to be, such as those leading to the output neuron cluster corresponding to '48', these connections are weakened by means of applying a soft RESET pulse (with $V_{reset} = -0.7V$. It is in this step of the simulation where the conditional RESET probability is computed, as to determine if a particular connection has been effectively removed or not. The RESET pulse has been successful if the resistance state of a synapse is above R_{thr} after the pulse. Lastly, **(d)**, some random connections between the input and output neurons corresponding to clusters representing '0' at t and '29' at $t + 1$ respectively are grown. This step is performed by choosing at random neurons from both clusters, and applying a SET pulse to the corresponding synapses, until the representation of that transition ($'0' \rightarrow' 29'$) is completed. Then, the sample value at $t + 1$ is pushed to t, and steps **(b)-(c)-(d)** are repeated, being now the input neuron cluster corresponding to '29' virtually activated. Active synapses connecting some input neurons representing '29' at t to some output neurons representing '48' at $t + 1$ are expected.

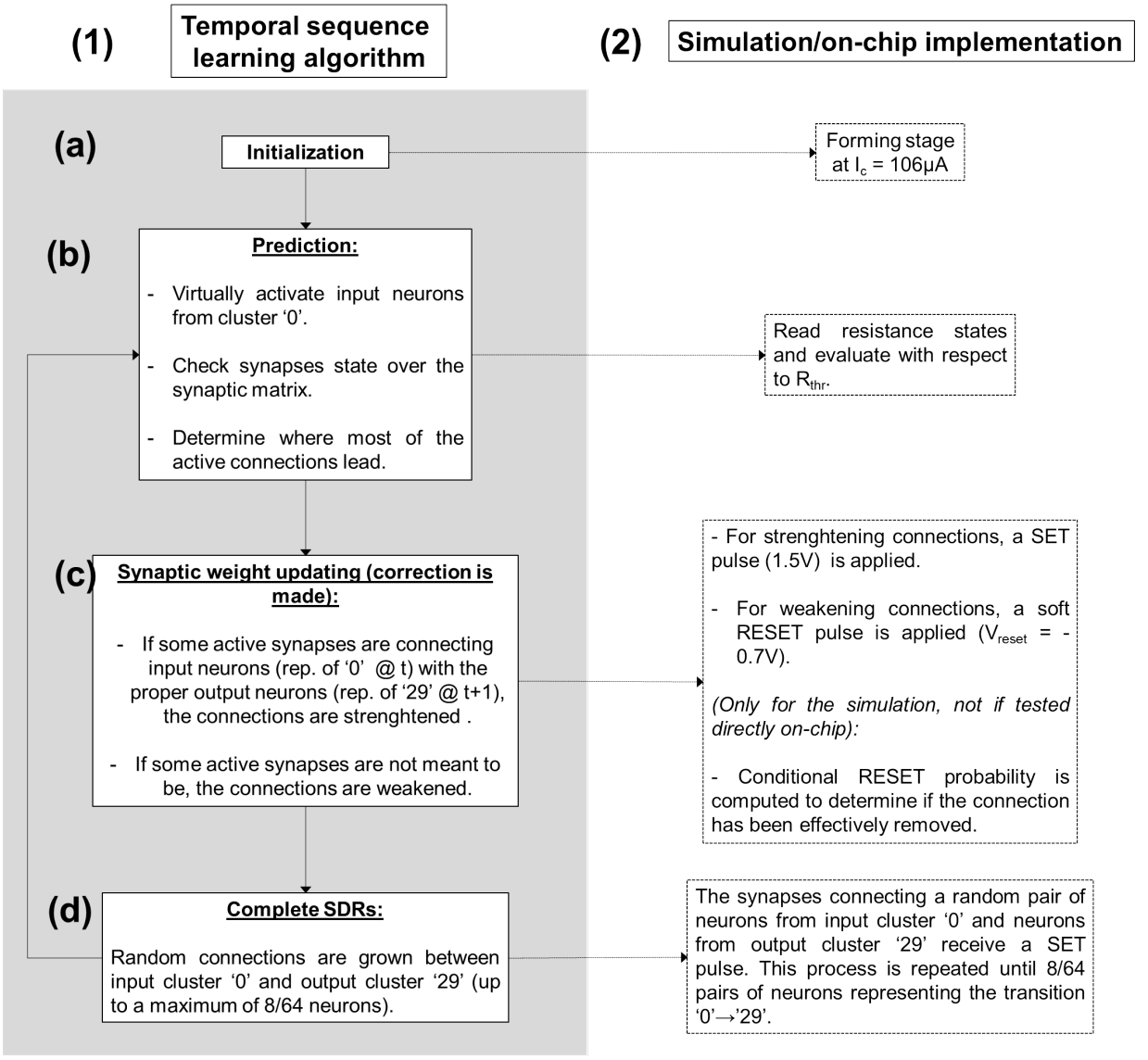

Figure 5.15: Flux diagram of the temporal sequence learning algorithm. **(1)** Qualitative description **(2)** Corresponding steps for the simulation and on-chip implementation of the algorithm.

The training is concluded when 5000 periods of the periodic sequence have been fed to the system. Figure 5.16 shows a representation of the connected input and output neuron clusters after the training with the sine wave from Figure 5.13 as the input data set. In here, for simplicity, the sum of the active synapses is represented in a gray scale, being a portion of the synaptic matrix black if any synapse is connected (none active), and ligher with increasing number of synapses being active, having a maximum of 8 synapses in this case (an SDR was complete if 8/64 neurons represented it).

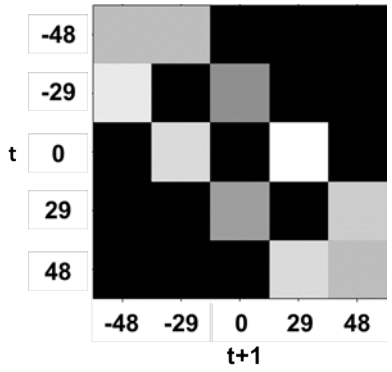

Figure 5.16: Scheme of the simulated crossbar array after the training, where the number of active connections between input and output clusters is represented in a gray-scale: if the portion of the synaptic matrix is black, then any synapse is active, whereas if it is white, all of the 8/64 neurons representing that temporal context are properly connected.

The same simulation was carried using the sine wave with a certain degree of noise, from a 5% up to a 25%. Figure 5.17.a shows an example of a sine wave with a 25%, whereas the representation of the resulting crossbar array is depicted in Figure 5.17.b.

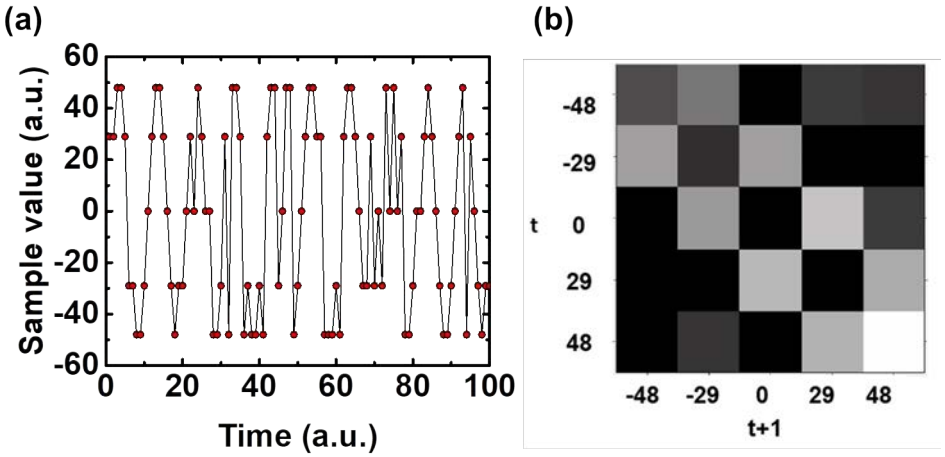

Figure 5.17: **(a)** Digital sine signal, consisting on samples with five possible values, with a 25% noise. **(b)** Scheme of the simulated crossbar array after a training stage where the input data set had a 25% noise. The number of active connections between input and output clusters is represented in a gray-scale.

As it can be seen, there are some unwanted connections when the system is trained with a noisy signal (being between $'-48' \rightarrow' 29'$, $'-48' \rightarrow' 48'$, $'0' \rightarrow' 48'$, $'-29' \rightarrow' -29'$ and $'48' \rightarrow' -48'$). As occurred with the SOM algorithm, the system presents with resilience against variability or noise. In this case, despite some undesired connections can not be effectively removed, the system is still able to learn the most significant relationships of the input data set features, and is able to generate noise-free sequences based upon what has been learned.

Another example of application tested by means of simulation consists in the generation of a temporal sequence, for instance a string of characters following some pre-defined rules. This type of learning is referred to as artificial grammar learning, and is both a popular learning benchmark and a paradigm of study within cognitive psychology and linguistics [123]. It is related to statistical

or Bayesian learning, in which the system predicts by making inferences in the form of probability distributions, which could be used to estimate unknown Markov chains from its samples. In particular, the following grammar was used to generate random strings of characters (Figure 5.18.a). As seen here, when the string character at time t is '2', the system is required to learn and remember if the character after the 'S' was 'A' or 'C', in order to properly predict 'B' or 'D', respectively, so the rules of the grammar are accomplished. In Figure 5.18.b, the active synapses are represented individually over the crossbar array (gray scale indicates its permanence value, being black above the threshold, and as lighter the color is, the lower is the resistance value with respect to the R_{thr}), showing that the system has properly inferred the grammar rules parting from correct random strings used as the input data set.

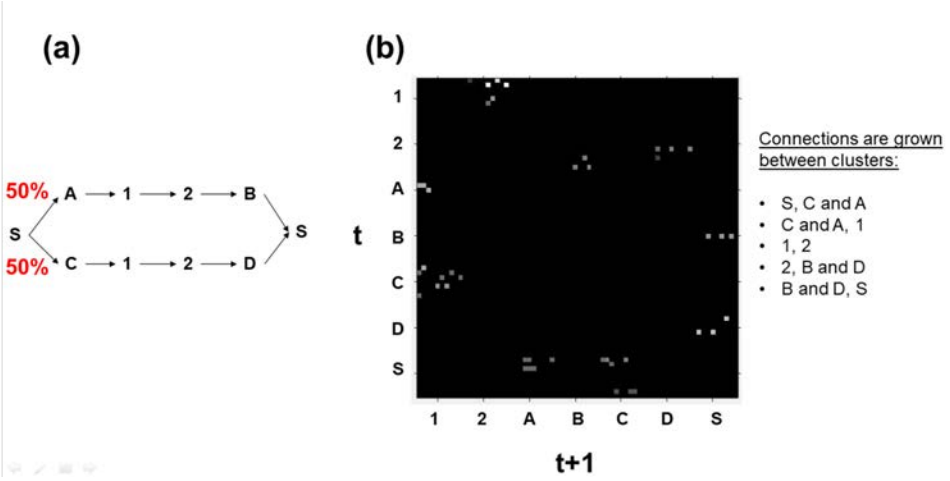

Figure 5.18: **(a)** Artificial grammar rule **(b)** Scheme of the simulated crossbar array after a training stage. Individual active synapses are represented in gray-scale according to its permanence value.

In order to test the accuracy of the system once trained, the system has to be able to generate strings according to the probability inferred from the input data set. In this case, the probability of each of the possibilities (S-A-1-2-B-S and S-C-1-2-D-S) was of a 50%. The test consists in generating 1000 strings according to the learned grammar. Then, the probability of each of the strings to appear is verified, which should match the 50% according to the employed input data set. Multiple-step predictions have to be performed by the system in order to properly evaluate its accuracy. In order to do so, the system first makes a prediction parting from 'S', and a random neuron within that input cluster is activated. Then, the active synapses are checked, and a prediction for $t + 1$ is made by choosing the output cluster which has more active synapses relating it with the activated input neuron from 'S'. The system has to keep track of all of the possible characters predicted for $t + 1$ and of the output neurons (that is, of the predicted SDR). For each of the predictions, the SDRs are pushed at t, meaning that now, the predicted output neurons appear activated at the input layer (the location within the cluster is maintained, since the location was the main parameter distinguishing different SDRs related to the same input feature or cluster). The active synapses are checked, and a prediction for $t + 2$ is made. The process is repeated for $t + 3$. In order to make a decision, the system has to check which is the final cluster with more active synapses leading to it.

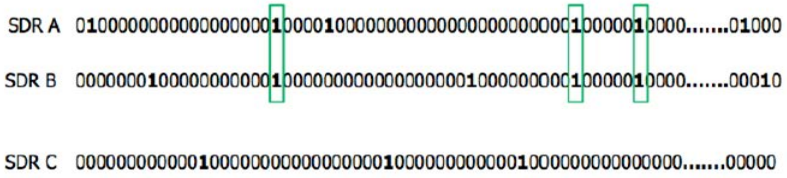

Figure 5.11: SDRs A and B have matching 1 bits. Therefore, they share semantic meaning. SDR C has no matching bits, so it does not share its semantinc meaning with A and B.

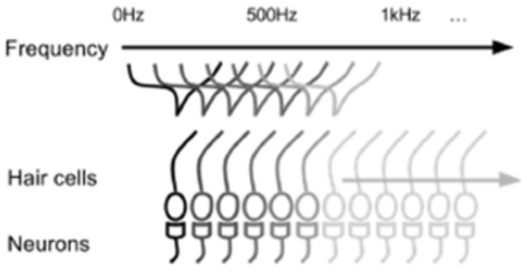

Figure 5.12: The hair cells in the cochlea act as transducers, stimulating a set of neurons based on the frequency of the sound.

Conclusions

Bio-inspired neuromorphic computing encompasses the design paradigms inspired by biological systems, where a balance between power consumption and performance is pursued. The objective is to provide a reliable hardware implementation of neural networks, which can be based on analog or digital mem-computing. Its applications are focused in such tasks in which the biological brain surpasses the performance of artificial intelligence, in terms of fast response, accuracy and power consumption. Such tasks are related to pattern recognition, classification and statistical inference, which are the basis of the learning mechanisms, which are fundamental for the adaptation of life-beings according to their experiences and environment.

During the last years, the emerging nano-scaled non-volatile memory devices have been studied for its implementation as synaptic elements within a neuromorphic hardware system. These technologies have in common its memristive behavior, which is related to the resistive switching phenomena. Initially focused on replacing the CMOS-based technology for memory applications, memristors have been proved that are more suitable than CMOS-based devices for the implementation of electronic synapses, because they permit a multi-bit non-volatile storage with better scaling capabilites and lower power consumption. However, the neuromorphic community has still to face important drawbacks of the memristive technologies, related to reliability issues, such as the retention time or endurance. Research should be conducted towards improving the switching behavior of the different memristive technologies, in order to optimize the neuromorphic systems performance. Among all of the memristive technologies, the oxide-based resistive random access memory (OxRAM) devices have been demonstrated to be the most suitable for the implementation of analog electronic synapses, because such devices can present symmetric and linear synaptic weight updating, if manufactured with the proper combination of materials and under the proper programming conditions. This technology is well-known for having intrinsic variability issues, for which each particular case and application should be analyzed.

The present thesis begins with an electrical characterization carried out on OxRAM devices, with the aim of demonstrating if they are good candidates for the implementation of analog electronic synapses within a neuromorphic system. The requirements for an electronic synapse include a two-terminal nanoscale device, compatible with CMOS technology, with non-volatile storage and programmable conductance properties, being the conductivity state of the devices identified with the synaptic weight of an electronic synapse. Such requirements are already fulfilled since the tested samples consist in OxRAM devices, where a filamentary conduction mechanism is considered. Moreover, an analog electronic synapse demands a wide range of possible conductivity state values, with the capability of inducing small changes to the actual conductivity state. Their resistive switching property was verified in the DC characterization section, where the control of the conductivity state in an analog fashion was verified by means of modulating the current compliance and fixing the minimum voltage applied to the samples, being both parameters set externally during the tests. It has been found that the tuning of the conductivity state is a reliable and repetitive process, if the main conductive path remains the same filament during consecutive resistive switching cycles. A good indicator for that is the conductivity state G measured at low voltages, which should be at least of $G = 1G_o$. Moreover, if the conductivity state is $G \approx 10G_o$, then it behaves linearly with the employed current compliance. Since in neuromorphic applica-

tions, pulse-programming is preferred over DC signals because it provides a way of modulating the input data to be fed to the system, a pulsed-characterization was performed. With this purpose, an automatic and flexible characterization setup was proposed in section, where the effects of the pulse parameters on the conductivity state of the devices when single pulses are applied was investigated, as a previous step for properly understanding the effects of pulse-trains. It is concluded that the conductivity state of the tested devices can be controlled by means of modulating the pulse amplitude, regardless of the employed pulse-width. Then, the G-V characteristics of the samples were extracted, providing a simple representation of how the conductivity state behaves with the applied voltage. In the neuromorphic context, these data indicates in a compact way how the synaptic weight can be updated by an external electrical parameter. The G-V characteristics, which were assumed to be time-independent, were modeled, and the cycle-to-cycle variability was studied. The proposed model is the basis of the simulations performed during the thesis.

Once the available devices were proved to be suitable for playing the analog synaptic role, experimental studies focused on demonstrating local learning rules were carried out. In chapter 4, two fundamental learning rules related to the plasticity property of the tested devices were tested: the STDP and the association between two synapses. Results of this part of the research demonstrate that biological learning mechanisms can be mimicked, which is key for the further development of unsupervised on-line learning algorithms to be implemented in currently state-of-the-art memristive crossbar arrays, being one of the main challenges of neuromorphic computing addressed the design of architectures supporting supervised techniques such as back-propagation of the error made by the system, among others. In particular, the STDP experiments verified that the synaptic weight updating process is not time-scale dependent, meaning that pulse-widths ranging from 100ns up to seconds with identical voltages can induce the same effects on the conductivity state of the devices. It is suggested that the STDP functions shapes are rather affected by the asymmetry of the G-V characteristics. On the other hand, the basis for implementing associative learning in a OxRAM-based crossbar array was also demonstrated. It was shown that the association process has to be though as a probabilistic event, such as in the biological neural systems case. There is an optimal choice of voltage waveforms in order to increase the probability of association between two OxRAM analog synapses.

The tested local learning rules were the foundations of a proposed bio-inspired on-line unsupervised learning scheme. Inspiration was taken from the software version of the self-organizing maps learning algorithm, which implementation is still not feasible on the current state-of-the-art crossbar arrays without requiring extra-circuitry and a complementary supervised learning scheme. The proposed learning algorithm is a fully-unsupervised learning algorithm, which relies on the time-dependent plasticity property of the tested OxRAM devices. The proposed algorithm has been proved to generate a spatially-distributed representation of the input data set features in a 2D simulated crossbar array, where topographical organization appears, as occurs in the sensory-processing areas of the brain. Moreover, its resilience against the intrinsic OxRAM variability has been tested, demonstrating that the system performance is immune to this issue. Lastly, a multi-layer system consisting on concatenated neuromorphic self-organizing maps and no extra circutry is proposed, for which unsupervised on-line hierarchical computation capabilities are expected, being the system able to process complex data sets without increasing the complexity of the system architecture.

These chapters conclude with the idea that reliable bio-inspired unsupervised on-line learning computing tasks can be achieved in a neuromorphic system, with OxRAM devices behaving as analog synapses.

The last chapter of the thesis is dedicated to the application of OxRAM devices to binary stochastic synapses. It has been proved that the history-sensitive RESET probability of OxRAM devices operating in low-current mode can be employed as a local learning rule in a neuromorphic crossbar array. Another unsupervised on-line learning algorithm related to the learning of temporal sequences was tested. In this case, the algorithm provides the neuromorphic system with the abil-

ity to learn and predict periodic sequences on real-time, detect anomalies and generate sequences according to the inferred features of the input data set, despite of the OxRAM intrinsic variability.

Overall, the work developed in this thesis provide new characterization schemes focused on verifying the fullfilment of the electronic synapse requirements of memristive devices, as well as a methodology to simulate the synaptic device behavior by means of modeling the tested devices G-V characteristics. Local learning rules have been experimentally demonstrated in OxRAM device for both analog and digital synaptic applications. Bio-inspired fully-unsupervised on-line learning algorithms have been proposed and tested, and it has been demonstrated that they provide the neuromorphic systems with high resilience against the intrinsic variability of the OxRAM technology, being its impact on the system's performance mitigated.

Publications related to this thesis

[Art5] M. Pedro, J. Martin-Martinez et al. An unsupervised and probabilistic approach to Pavlov's dog experiment with OxRAM devices. Article accepted for publication in Microelectronic Engineering, 215 (July 2019).

[Conf11] N. A. Jimenez, M. Pedro et al. Influence of the initial conductivity in the synaptic plasticity of $TiN - Ti - HfO_2 - W$ structures. Conference paper accepted in the 2019 Memristive Materials, Devices and Systems (MEMRISYS). July 2019, Dresden, Germany.

[Conf10] M. Pedro, J. Martin-Martinez et al. A probabilistic approach to associative learning for neuromorphic applications. Conference paper accepted in the 2019 Memristive Materials, Devices and Systems (MEMRISYS). July 2019, Dresden, Germany.

[Conf9] M. Pedro, J. Martin-Martinez et al. An unsupervised and probabilistic approach to Pavlov's dog experiment with OxRAM devices. Conference paper accepted in the 2019 Insulating Films on Semiconductors (INFOS). July 2019, Cambridge, United Kingdom.

[Art4] M. Pedro, J. Martin-Martinez et al. Self-organizing neural networks based on OxRAM devices under a fully unsupervised training scheme. Submitted to the Materials Special Issue "Memristors for Neuromorphic Circuits and Artificial Intelligence Applications", June 2019.

[Art3] G. Gonzalez-Cordero, M. Pedro et al. Analysis of resistive switching processes in $TiN - Ti - HfO_2 - W$ devices to mimic electronic synapses in neuromorphic circuits. Article in Solid-State Electronics, April 2019. Accepted for publication.

[Art2] M. Pedro, J. Martin-Martinez et al. A Flexible Characterization Methodology of RRAM: Application to the Modeling of the Conductivity Changes as Synaptic Weight Updates. Article in Solid-State Electronics, March 2019. Accepted for publication.

[Conf8] M. Pedro, J. Martin-Martinez et al. Investigation of Conductivity Changes in Memristors under Massive Pulsed Characterization. Conference paper in 2018 Conference on Design of Circuits and Integrated Systems (DCIS), pp. 1-4. November 2018, Lyon, France.

[Conf7] M. Pedro, J. Martin-Martinez et al. Characterization and modelling of G-V characteristics of RRAM devices for synaptic applications. Conference paper in the 12th Spanish Conference on Electron Devices (CDE 2018), November 2018, Salamanca, Spain.

[Conf6] M. Pedro, J. Martin-Martinez et al. A RRAM-based self-organizing neural network. Conference paper in the 8th Forum on New Materials within the 14th International Ceramics Congress

(CIMTEC 2018), June 2018, Perugia, Italy.

[Conf5] M. Pedro, J. Martin-Martinez et al. A flexible characterization methodology of RRAM: Application to the modelling of the conductivity changes and their variability. Conference paper in 2018 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS) (pp. 1-4). March 2018, Granada, Spain.

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[Conf3] J. Martin-Martinez, N. A. Jimenez et al. Synaptic Plasticity implemented in $TiN - Ti - HfO_2 - W$ structures. Conference paper in the 2017 Memristive Materials, Devices and Systems (MEMRISYS) (April 2017), Athens, Greece.

[Art1] M. Pedro, J. Martin-Martinez et al. Tuning the conductivity of resistive switching devices for electronic synapses. Article published in Microelectronic Engineering (2017), 178, pp. 89-92.

[Conf2] M. Pedro, J. Martin-Martinez et al. Tuning the Conductivity of Resistive Switching Devices for Electronic Synapses. Conference paper in the Conference on Insulating Films on Semiconductors (INFOS 2017), June 2017, Potsdam, Germany.

[Conf1] M. Pedro, J. Martin-Martinez et al. Control of the Bipolar Resistive Switching Conductivity for Neuromorphic Computing Applications. Conference paper in the 11th Spanish Conference on Electron Devices (CDE 2017), February 2017, Barcelona, Spain.

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