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Muthupandian Cheralathan

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DOCTORAL THESIS

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COMPACT MODELING FOR MULTI-GATE MOSFETs USING ADVANCED TRANSPORT MODELS

UNIVERSITAT ROVIRA I VIRGILI

Department of Electronic, Electric and Automatic Engineering

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DOCTORAL THESIS

Supervised by Prof. Benjamin Iñiguez

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I STATE that the present study, entitled “Compact Modeling for Multi-Gate MOSFETs using Advanced Transport models”, presented by Muthupandian Cheralathan for the award of the degree of doctor, has been carried out under my supervision at the Department of Electronic, Electric and Automatic Engineering of this university, and that it fulfills all the requirements to be eligible for the European Doctorate Award.

Tarragona, 25th February 2013

Doctoral Thesis Supervisor

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Prologue

The continuous scaling-down process of the channel length over the last four decades is reaching its limits in terms of gate oxide thickness, short channel effects and power consumptions, increased leakage currents. The multiple-gate SOI CMOSFET devices are expected to replace the bulk CMOSFET transistors for a better control of the entire device electrostatics. In today's extremely scaled MOSFETs the channel length is in the order of the carrier mean-free-path (λ).This means that carriers, when travelling from source towards the drain, experience only few scattering events. This regime is commonly referred to as quasi-ballistic transport. Quasi-ballistic (QB) effects are expected to occur in bulk MOSFETs as well. It is, however, the multiple gate structure that increases the device's immunity to short-channel effects, thus allowing a further reduction of the channel length into the order of the carrier mean-free-path, making quasi ballistic transport phenomena even more likely. QB transport is an active area of research since a good understanding of the physics of carrier scattering and the main feature which impact carrier transport, can help improve and optimize the device performance. QB transport models are benchmarked against Monte-Carlo (MC) simulations. The MC approach provides a statistical solution to the Boltzmann Transport equation (BTE). The BTE is a general formulation of the semi-classical carrier

transport problem from which approximate transport models such as the Drift-Diffusion (DD) and hydrodynamic equations are derived.

In this thesis we have developed compact models including hydrodynamic transport model adapted for double-gate (DG) and surrounding-gate (SRG) MOSFETs from a unified charge control and surface potential models respectively which are derived from Poisson's equation. Similar modelling scheme have been used in all these devices. The current and total charges are written in terms of the mobile charge sheet densities at the source and drain ends of the channel. The model show good agreement with the 2D and 3D (SRG) numerical simulations, in all operating regimes. Due to the limitation of available optimized devices for analysis, numerical simulation was used as the main analysis tool. The model developed is very promising to be easily adapted in circuit simulators.
The thesis is outlined as follows: **Chapter 1** presents the state of the art, we dedicate **chapter 2** for the compact modelling of undoped and doped surrounding-gate (SRG) MOSFETs and its adaptation to reproduce advanced transport models. An analytical and continuous compact model for a long-channel cylindrical SRG MOSFETs is developed. The analytical expression for the surface potentials are continuous and explicit function of the applied voltages. The expression obtained for the potentials are used to derive an analytical compact model for the

drain current which is valid from low to high doping. The results are compared with 3D ATLAS device simulator. Further, the compact model is then extended to include the hydrodynamic transport and quantum mechanical effects, and we show that it can reproduce results of 3D numerical simulations using advanced transport models. The final compact model includes mobility degradation, drain-induced barrier lowering, velocity overshoot and quantum effects.

In **chapter 3** extension of the compact double-gate (DG) MOSFET model to reproduce advanced transport models, first our compact drain current model for DG MOSFET has been extended to include the hydrodynamic transport and quantum mechanical effects. The final compact model can accurately reproduce simulation results of some of the most advanced transport simulators. The model is based on a compact model for charge quantization within the channel and it includes mobility degradation, channel length modulation, drain-induced barrier lowering, overshoot velocity effects and quantum mechanical effects. The temperature dependency is also accounted in the compact model.

In **chapter 4** implementation of compact model of DG and SRG MOSFETs in circuit simulator specifically in SMASH has been presented. First, the results of the implementation of a nanoscale DG MOSFETs compact model, which includes hydrodynamic transport model, in Verilog-A in order to carry out circuit

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simulation are presented. The model is used with SMASH circuit simulator for the analysis of the DC and transient behaviour. A DG CMOS inverter circuit and a five stage ring oscillator circuit have been analysed. Second, compact model of a nanoscale cylindrical surrounding-gate (SRG) MOSFETs which includes hydrodynamic transport model, in Verilog-A implemented in circuit simulation are presented.

Finally in **chapter 5**, we will summarize the main findings of this work and conclude with some directions for future extension of the work addressed in this thesis.

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List of Symbols

ϕ - Electrostatic potential
N_a - Doping concentration
ε_{si} - Permittivity of silicon
q - Electric charge
Φ_f - Fermi level
Φ_t - Thermal voltage
C_{ox} - Gate capacitance per unit area
C_{si} - Silicon capacitance per unit gate area
t_{ox} - Oxide thickness
ε_{ox} - Permittivity of oxide
R - Radius of the cylindrical silicon body
V_{fb} - Flat band voltage
V_{ch} - Channel voltage
V_{gs} - Applied to the gate voltage
Q_{dep} - Fixed charge density per unit gate area
Q_{in} - Inversion charge density per unit gate area
E_s - Electric field at the silicon-oxide interface
ϕ_{sBT} - Surface potential at subthreshold
ϕ_{oBT} - Center potential at subthreshold
LW - Lambert function
ϕ_{sT} - Surface potential at threshold
ϕ_{oT} - Center potential at threshold
ϕ_s - Overall surface potential

α_T - Normalized difference between the surface and the center potential at threshold

V_{GM} - Maximum applicable gate voltage

Q_{sem} - Semiconductor charge per unit gate area

W - Channel width

L - Channel length

μ - Electron mobility

V_S - Source voltage

V_D - Drain voltage

V_{dss} - Effective drain-source voltage

C_{ox}^* - Corrected oxide capacitance

V_T - Threshold voltage

ΔV_T - Corrected threshold voltage

σ - Fitting parameter

L_m - Reference length

L_C - Characteristics length

v_{sat} - Saturation velocity

V_{sat} - Saturation potential

τ_w - Energy relaxation time constant

λ_w - Energy-relaxation length

T - Temperature

μ_o - Low-field mobility

μ_{eff} - Effective mobility

E_{sat} - Saturation field

L_e - Effective length

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ΔL - Saturated channel length

θ_1 - Mobility attenuation coefficients of the first order

θ_2 - Mobility attenuation coefficients of the second order

q_s - Normalized induced charge at the source

q_d - Normalized induced charge at the drain

V_{bi} - Source and drain junction built-in voltage

Q_s -Mobile charge densities at the source

Q_d - Mobile charge densities at the drain

$\Delta\phi$ - Work-function difference between the gate electrode and the intrinsic silicon

n_i - Intrinsic concentration

C_g - Effective oxide capacitance

C_{gs} - Gate-source capacitance

C_{gd} - Gate-drain capacitance

$\hbar$ - Reduced Planck constant

m_{eff} - Electron effective mass

γ - Fitting parameter

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Chapter 1

State of the Art and Trends for Multiple-gate MOS devices

1.1 Introduction

The phenomenal growth of the semiconductor industry is characterised by the remarkable increase of transistor count in integrated circuits (IC), as represented by the well-known Moore's Law [1]. However, this law is a rough prediction of the future of IC expansion. The semiconductor industry has made considerable progress, especially regarding the Metal Oxide Semiconductor Field Effect Transistor (MOSFET). MOSFETs have the remarkable feature that as they become smaller they also become cheaper, consume less power, become faster, and enable more functions per unit area of silicon. As a result, denser silicon integrated circuits can be realized, offering superior performance at reduced cost per function. Figure 1.1 shows the latest update of Moore's law, which sees the introduction of the world's first processor with 2 billion transistors.

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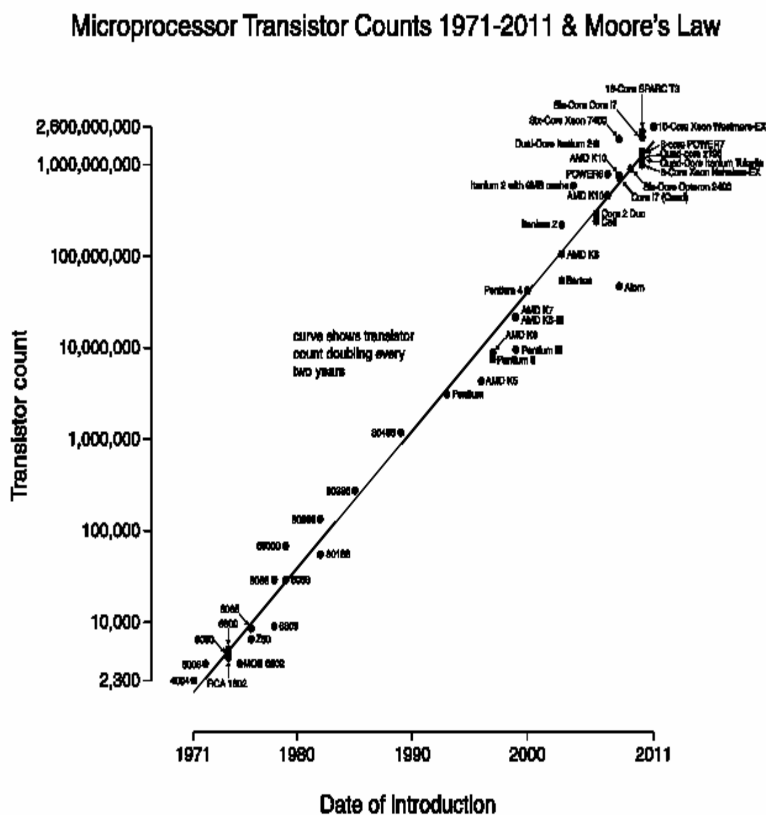

Figure 1.1 Plot of transistor count against dates of introduction – following Moore's law.

The need of a more accurate estimate defined by the International Technology Roadmap for Semiconductors (ITRS) [2], which has been forecasting and driving the pace of semiconductor technology at the same time. Figure 1.2 shows the evolution of the transistors gate length for the last decades, as well as the ITRS Roadmap predictions made for the next 15 years.

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Over the past several decades, the extraordinary evolution of microelectronics has thus been made possible together by continuously shrinking the size of the transistors and also materials used for fabrication that has changed from bulk silicon wafers to Silicon-on-Insulator (SOI) wafers. Within the SOI planar technology, two distinct families of devices are classically considered as shown in Figure 1.3, namely partially-depleted (PD) and fully depleted (FD) MOSFETs. One of the main advantages of this wafer is the drastic reduction of all the parasitic effects from the silicon substrate [3]. In FD MOSFETs, the thickness of the silicon film is reduced in such a way that the depletion region below the inversion channel extends down to the buried oxide. In this case the entire Si film is depleted from free carriers.

When the film is made thicker the depletion region can stop at a certain depth within the silicon film, leaving an un-depleted region above the buried oxide called the body. For this reason such devices are referred to as partially-depleted MOSFETs. The floating potential of the body region in PD MOSFETs is responsible for the floating body effects, which affect the device's electrical behavior. The remarkable feature of the FD MOSFET is that the current drive is higher than in bulk MOSFET and its subthreshold slope is sharper, due to a much smaller body factor [4].

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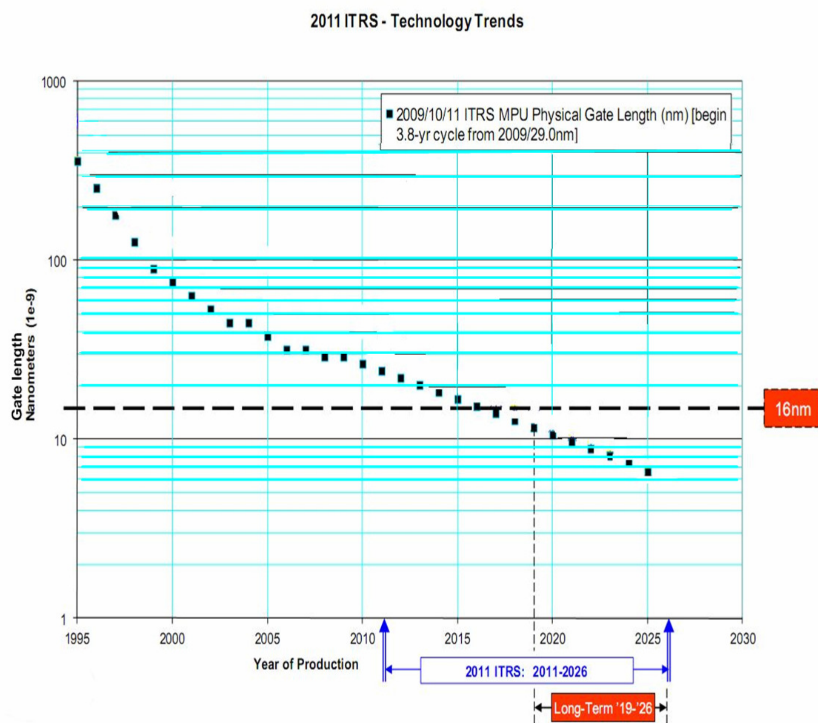
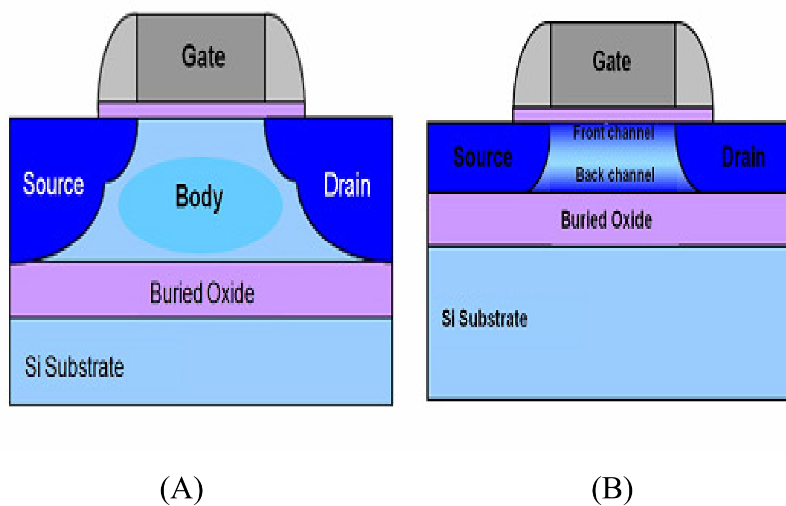


Figure 1.2 Predicted ITRS Roadmap for the next decade.



(A) (B)

Figure 1.3 (A) Partially depleted and (B) Fully depleted SOI MOSFETs.

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FD MOSFETs presents nearly an ideal subthreshold slope, lower junction capacitances, enabling the reduction of the threshold voltage and power consumption. For low power analog applications FD technology are much suited [5-6].

In the last decade, we have seen some remarkable technology at work, from just a few devices on a single silicon wafer, to Very-Large-Scale-Integration (VLSI) and in the last few years, this has moved to what is known as Ultra-Large-Scale-Integration (ULSI), in keeping with Moore's Law. The trend in device scaling has almost faithfully followed a universal scaling rule [7] that is derived from the assumption of simple electrostatics and the classical physics of ideal gases for transport. However, with device sizes entering the deep sub-micron (< 0.1 mm gate length) regime, several additional elements of the detailed transport physics have required attention to understand device behavior adequately.

These range from purely classical effects caused by the onset of ballisticity in the transport, such as hot-carrier effects [8], velocity overshoot [9], and impact ionization [10], to purely quantum mechanical effects due to the wave nature of the charge carriers in semiconductors. This constant shrinking, however, has its limits, and we have reached the point where materials and device issues are starting to arise, opening the door for alternative device structures. The most promising SOI devices for the nanoscale range are based on multiple gate structures, such as the double-gate (DG), the triple gate or fin-

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shaped field-effect transistor (FinFET), and the surrounding gate (SGT) or gate-all-around (GAA) [11-17. The definition of the various multiple-gate structures can be easily mistaken if not defined properly based on their physical gate dimensions. Figure 1.4 shows some of the multi-gate MOSFETs. The multiple-gate architecture has some interesting characteristics that are presented in the next section.

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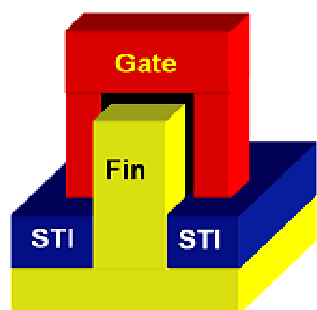
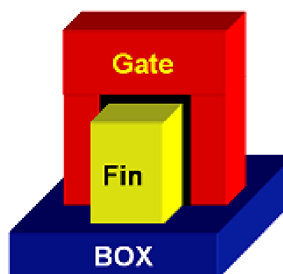
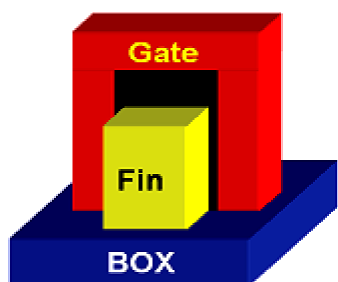


(a) Triple-gate FinFET on Bulk Si

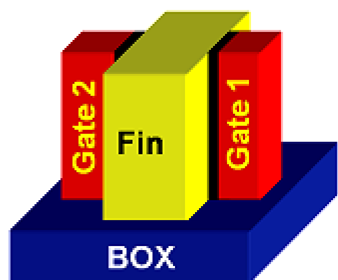


(b) Triple-gate FinFET on SOI



(c) Double-gate FinFET on SOI

(d) Gate-all-around



(e) Independent Double-gate FinFET on SOI

(f) Planar Double-gate on SOI

Figure 1.4 Various structures of multi-gate MOSFETs. (BOX: buried oxide; SOI: silicon-on-insulator).

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1.2 Advantages of Multi-gate MOSFETs

One of the most important ones is the gate control over the electrostatic charges. This increased charge control in the channel translates into improved short channel effects [18]. Since the channel (body) is controlled electrostatically by the gate from multiple sides, the channel is better-controlled by the gate than in the conventional transistor structure. Unwanted leakage components are reduced and a small transistor can be used to continue the cost reduction through miniaturization. Improved gate control also provides lower output conductance. This provides greater voltage gain, which is beneficial to analog circuits as well as to the noise tolerance of digital circuits.

Another distinct characteristic of multiple-gate devices is the increased current and therefore faster circuit speed [19]. One of the main advantages of using multiple-gate devices is the highly improved electrical characteristic in the subthreshold regime [20]. The drain induced barrier lowering (DIBL) characteristic of a FD multiple-gate transistor is much improved over a normal SG MOS transistor [4]. The volume inversion is a phenomenon found only in multiple-gate architectures. A device is said to be operating in volume inversion if there is a strong coupling between two conducting channels [21]. In multiple gate devices, the use of a very thin film allows to downscale the devices without the need of using high channel doping densities and

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gradients [22-24]. In fact, undoped films can be used: the full depletion of the thin film prevents punch-through from happening. Besides, the absence of dopant atoms in the channel increases the mobility by suppressing impurity scattering [23]. Multiple gate nanoscale devices have many advantages in circuit performance. A very high packaging density is possible because of the small size of these devices, caused by the short channel and the thin film. Because of the higher mobility, transconductance can be higher, which gives more current gain and allows a higher operating frequency. Therefore, multiple gate nanoscale devices have a big potential for RF and microwave applications [25-26]. The analog performance is also very good. Voltage gain is much higher than in conventional bulk MOSFETs, and especially in moderate inversion.

1.3 Compact modeling

Compact Models (CMs) for circuit simulation have been at the heart of CAD tools for circuit design over the past decades, and are playing an ever increasingly important role in the nanometer system-on-chip (SOC) era. Although not highly "visible" to circuit designers and technology developers, a compact model plays the key role in accuracy and efficiency of the circuit simulator being used by designers as well as a bridge to the technology in which the design is to be fabricated. As the mainstream MOS technology is scaled into the nanometer

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regime, development of a truly physical and predictive compact model for circuit simulation that covers geometry, bias, temperature, DC, AC, RF, and noise characteristics becomes a major challenge. A physics based device model is understood to be a description of device behavior in terms of analytical, algebraic expressions. This is contrary to device simulations, which are numerical derivations behavior based on complex equations, such as partial differential equations. Furthermore, device models may be characterized as being compact if they are described in terms of analytical, explicit expressions. Compact models can also cover models which involves preprocessing of model expressions by iterative routines that result in parameter lookup-tables for fast retrieval for use in simplified parameterized models. Compact models have the characteristic of being computational efficient in the context of circuit simulations. The demands for advanced models, which can describe nanoscale silicon devices in analog and mixed-signal applications and can account for the physical effects on small geometry devices, have led to enormous research & development (R&D) efforts in the development of advanced physics-based compact models.

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1.4 Numerical simulations

Numerical device simulation mostly involves iteration over Poisson's equation in combination with a transport model for a given set of boundary conditions. A common way to solve this problem is to discretise the 2D surface or 3D volume with a grid and iterate over this with a PDE solver. Convergence and accuracy of the solutions depends strongly on the grid distribution and size. In addition, convergence time depends strongly on the solver type, models for carrier statistics, and current continuity. Typically, numerical solvers are not applicable for simulating integrated circuits due to the high computational overhead. In the present work, we have used the device simulator Atlas from Silvaco [27]. Central in this tool is a range of models for physical phenomena behavior such as charge carrier transport models, classical and quantum carrier statistics, material properties, etc. These can be combined in the simulation of specific transistor configurations.

1.5 Circuit simulations

Tools for simulating the behavior of simple circuits began emerging in parallel with the development of integrated circuits. Central elements in circuit simulators are the device models. Different research groups have steadily provided models and modeling approaches to SPICE, adding a wide range of

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functionality to the simulator engine. The MOSFET model BSIM by the Berkeley group has been highly successful and was an industry standard for many years. In 2005, for the first time since the seventies, the Compact Model Council, which works for a standardization of compact models and model interfaces, has decided to make the PSP [28] model developed by Philips semiconductors and Pennsylvania State University the industry standard, succeeding the Berkeley groups BSIM3 and BSIM4 [29]. SPICE simulators come with a selection of models for different semiconductors. Choosing the most effective and exact model for the circuit simulation is a difficult task and often leaves the circuit designer with a dilemma, whether to choose a time-consuming precise model or a more simplified and quick model for simulation and parameter extraction. Precise models are often characterized by many parameters that have to be identified empirically by analyzing measurements or TCAD simulations. This may be a quite difficult task considering that some models use several hundred parameters. These parameters cannot always be associated directly with physical mechanisms. However, for a specified technology, this task only has to be performed once by the transistor manufacturer. The numerical tools sometimes come with additional parameter extractors which aid the designer in the process.

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Chapter 2

Current and Charge model for Surrounding-gate (SRG) MOSFETs

This chapter is aimed to study the electrostatic potentials and current characteristics of the cylindrical surrounding-gate (SRG) MOSFET.

The chapter is divided into two sections as follows:

In section 2A, an analytical and continuous compact model for a long-channel cylindrical SRG MOSFETs is developed. The analytical expression for the surface potentials are continuous and explicit function of the applied voltages. The expression obtained for the potentials are used to derive an analytical compact model for the drain current which is valid from low to high doping concentrations. The results are compared with 3D ATLAS device simulator.

In section 2B, the compact model is then extended to include the hydrodynamic transport and quantum mechanical effects, and we show that it can reproduce results of 3D numerical simulations using advanced transport models. The final compact model includes mobility degradation, drain-induced barrier lowering, velocity overshoot and quantum effects.

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2A. Compact model for long-channel cylindrical surrounding-gate (SRG) MOSFETs valid from low to high doping concentration

2A.1. Introduction

The advantages of silicon-on-insulator (SOI) MOSFETs over bulk transistors, such as reduced short channel effects, lower parasitic capacitances and increased circuit speed have made them very attractive for applications in low power and low voltage digital and analog integrated circuits [1]. Among SOI devices, cylindrical surrounding-gate (SRG) MOSFET has become one of the most promising device structures in the technology scaling roadmap [2]. By completely surrounding the channel by the gate, excellent gate control is achieved to reduce short-channel effects. These devices are especially interesting for analog and mixed circuit applications, making the demand of an accurate and CAD compatible compact model for the SRG MOSFETs a really urgent task. To use SRG MOSFETs in circuit design, an analytical model is required [3, 4]. Most of the developed SRG MOSFETs models are only valid for intrinsic channels [5 - 7]. However, doping in SRG MOSFET has been used to adjust the threshold voltage of the device [8]. Besides,

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there is a growing interest in highly doped nanowires working as junctionless transistors [9]. A few models have been presented for the particular case of heavy doping [8]. An compact model valid from low to high doping concentrations is been presented [10], nevertheless it requires iterations to solve for the mobile charge densities. But an explicit compact model for SRG MOSFETs, valid for a broad range of dopings, is needed for the design of circuits using SRG MOSFETs.

In this section, first of all, we present an analytical expression for the electrostatic potentials at the surface and center in the long-channel cylindrical SRG MOSFETs, valid for the practical range of doping concentrations. The expression obtained for the potentials is used to derive an analytical compact model for the drain current of doped long-channel cylindrical SRG MOSFETs. We have considered a long-channel device in order to focus on doping effects and to get rid of short-channel effects. Additionally the quantum effects are not considered for the radial geometry of the device if it is 10nm and above. However, this model can be used as a basis to introduce short-channel effects, like in [11] for double-gate (DG) MOSFETs.

In order to validate our model, calculated potentials and currents are compared with 3D simulations obtained using ATLAS device simulator [12].

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2A.2. SRG Model

The schematic cross-section and coordinate system of an N-channel SRG MOSFET being studied is shown in Figure. 2A.1. R is the radius of the cylindrical silicon body and V_{gs} is applied to the gate voltage [3].

Following the gradual channel approximation (GCA), the electrostatic potential distribution in the silicon channel can be described by Poisson's equation as follows [3]:

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{d\phi}{dr}\right)=\frac{qN_a}{\varepsilon_{si}}\left[e^{\beta}\left(\phi-V_{ch}-2\phi_F\right)+1\right] \qquad (2A.1)$$

where ϕ is the electrostatic potential, N_a is the doping concentration, ε_{si} is the permittivity of silicon, q is the electric charge, $\beta=q/(kT)$ represents the reciprocal of thermal voltage $\phi_t=\frac{1}{\beta}$, $\phi_F=\beta^{-1}\ln(N_a/n_i)$ is the Fermi potential, and V_{ch} is the quasi-Fermi potential along the channel.

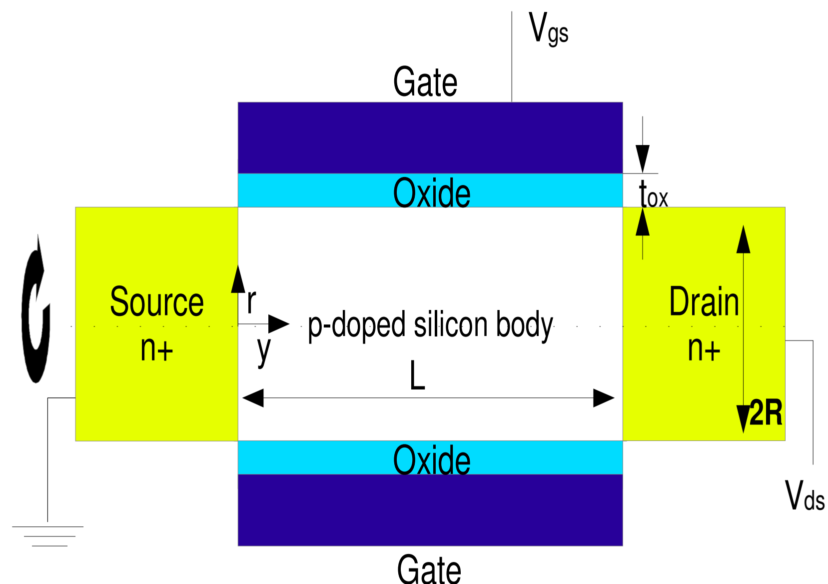

Figure 2A.1 Schematic cross-section of an N-channel SRG MOSFET showing the coordinate system and related variables.

The boundary conditions of (2A.1) are:

$$C_{ox}(V_{gs} - V_{fb} - \phi_s) = Q_{in} + Q_{dep} = -\varepsilon_{si} E_s \qquad \text{(2A.2a)}$$

$$\frac{d\phi}{dr} = 0 \;\text{ as }\; r = 0 \qquad \text{(2A.2b)}$$

where $C_{ox} = \varepsilon_{ox} / (R \ln(1 + t_{ox} / R))$ is the oxide capacitance per unit gate area in a SRG MOSFET [5], t_{ox} is the oxide thickness, ε_{ox} is the permittivity of oxide, V_{fb} is the flat band voltage, Q_{in} is the inversion charge density per unit gate area,

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$Q_{dep} = qN_a R/2$ is the fixed charge density per unit gate area, and E_s is the electric field at the silicon-oxide interface.

For the doped case, the full-depletion approximation can be obtained by neglecting the exponential term on the right hand side (RHS) of (2A.1) [3, 4]:

$$\phi(R) = \phi_o + \frac{qN_a R^2}{4\varepsilon_{si}} \tag{2A.3}$$

Following [3] an expression for the surface electric field E_s is obtained:

$$E_s = -\sqrt{\left[\frac{Q_{dep}}{\varepsilon_{si}} - \frac{2}{\beta R}\left[1 - e^{\beta(\phi_o - \phi_s)}\right]\right]\frac{4}{\beta R} e^{\beta(\phi_s - V_{ch} - 2\phi_F)} + \left(\frac{Q_{dep}}{\varepsilon_{si}}\right)^2} \tag{2A.4}$$

From (2A.4), we get E_s as a function of the potential at the surface ϕ_s, and at the center of the layer ϕ_o:

$$E_s = -\sqrt{\frac{2qN_a\phi_t}{\varepsilon_{si}}}\sqrt{\frac{\phi_s - \phi_o}{2\phi_t} + \left[1 - \frac{\phi_t}{\phi_s - \phi_o} + \frac{\phi_t}{\phi_s - \phi_o} e^{-\left(\frac{\phi_s - \phi_o}{\phi_t}\right)}\right] e^{\left(\frac{\phi_s - V_{ch} - 2\phi_F}{\phi_t}\right)}} \tag{2A.5}$$

We can rewrite (2A.5) as:

$$E_s = -\sqrt{\frac{4Q_{dep}\phi_t}{R\varepsilon_{si}}}\sqrt{\alpha}\sqrt{\frac{1}{2} + \left[\frac{1 - \frac{1}{\alpha} + \frac{1}{\alpha}e^{-\alpha}}{\alpha}\right] e^{\left(\frac{\phi_s - V_{ch} - 2\phi_F}{\phi_t}\right)}} \tag{2A.6}$$

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where $\alpha = (\phi_s - \phi_o)/\phi_t$ is the normalized difference of potentials [13].

Substituting (2A.6), in the expression $V_{gs} - V_{fb} = \phi_s - \varepsilon_{si} E_s / C_{ox}$ (coming from (2A.2a)), the surface potential ϕ_s is implicitly defined as:

$$V_{gs} = V_{fb} + \phi_s + \frac{1}{C_{ox}} \sqrt{\frac{4Q_{dep}\varepsilon_{si}\phi_t}{R}} \sqrt{\alpha} \sqrt{\frac{1}{2} + \left[\frac{1 - \frac{1}{\alpha} + \frac{1}{\alpha} e^{-\alpha}}{\alpha} \right] e^{\left(\frac{\phi_s - V_{ch} - 2\phi_F}{\phi_t} \right)}} \tag{2A.7}$$

2A.3 Calculation of the potentials

2A.3.1 Subthreshold regime

In the subthreshold regime, the difference between the surface potential and the potential at the center of the Si layer is calculated using the full-depletion approximation which is valid in this regime [3], (2A.3) as:

$$\phi_{dBT} = \phi_{sBT} - \phi_{oBT} = \frac{qN_a R^2}{4\varepsilon_{si}} = \frac{Q_{dep} R}{2\varepsilon_{si}} \tag{2A.8}$$

where ϕ_{sBT} and ϕ_{oBT} are the values of the surface potential and potential at the center of the Si layer corresponding to the

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subthreshold condition. As can be seen, ϕ_{dBT} depends only on the doping concentration N_a and on the silicon body radius R.

ϕ_{sBT} is calculated by solving the (2A.7). For the subthreshold regime, the term $\left[\frac{1-\frac{1}{\alpha_{BT}}+\frac{1}{\alpha_{BT}}e^{-\alpha_{BT}}}{\alpha_{BT}}\right]<1$ and (2A.7) can be simplified expanding the square root.

After some rearrangements we can obtain:

$$V_{gs}-V_{fb}=\phi_{sBT}+\frac{Q_{dep}}{C_{ox}}\left(1+e^{\left(\frac{\phi_{sBT}-V_{ch}-2\phi_F}{\phi_t}\right)}\right) \tag{2A.9}$$

Using the principal branch of the Lambert function LW. ϕ_{sBT} is calculated from (2A.9) as:

$$\phi_{sBT}=V_{gs}-V_{fb}-\frac{Q_{dep}}{C_{ox}}-\phi_t LW\left[\frac{Q_{dep}}{C_{ox}\phi_t}e^{\left(\frac{V_{gs}-V_{fb}-\frac{Q_{dep}}{C_{ox}}-V_{ch}-2\phi_F}{\phi_t}\right)}\right] \tag{2A.10}$$

ϕ_{oBT} is calculated substituting (2A.10) in (2A.8) as:

$$\phi_{oBT} = \phi_{sBT} - \phi_{dBT} \tag{2A.11}$$

Figure 2A.2 shows the behavior of ϕ_{sBT} (subthreshold) as a function of the doping concentration in the Si layer. Comparison is made between the results obtained by solving (2A.10) and numerical 3D ATLAS simulation. As can be seen, our analytical expression provides a good agreement in all the doping concentrations from 10^{16} to 5 x 10^{18} cm^{-3} for t_{ox} = 3 nm and R = 5 nm. A gate with a mid-gap work function was considered. The source and drain doping concentration of 10^{20} cm^{-3} was considered. From the plot, it can be seen that the potential increases as doping concentration increases. When $N_a = 10^{18}$ cm^{-3} the potential has a maximum value, and for further increase of the doping concentration in the Si layer the potential decreases, which is clearly seen from the plot.

From (2A.10) for the surface potential in the deep subthreshold regime (where the Lambert function term is negligible), we observe that the flatband voltage term dominates at low channel dopings over the other terms, leading to an increase of the surface potential with increasing doping. At high channel dopings the term Q_{dep}/C_{ox} term dominates over the other terms in the expression and hence the surface potential starts to decrease after reaching a peak value as the doping concentration is increased.

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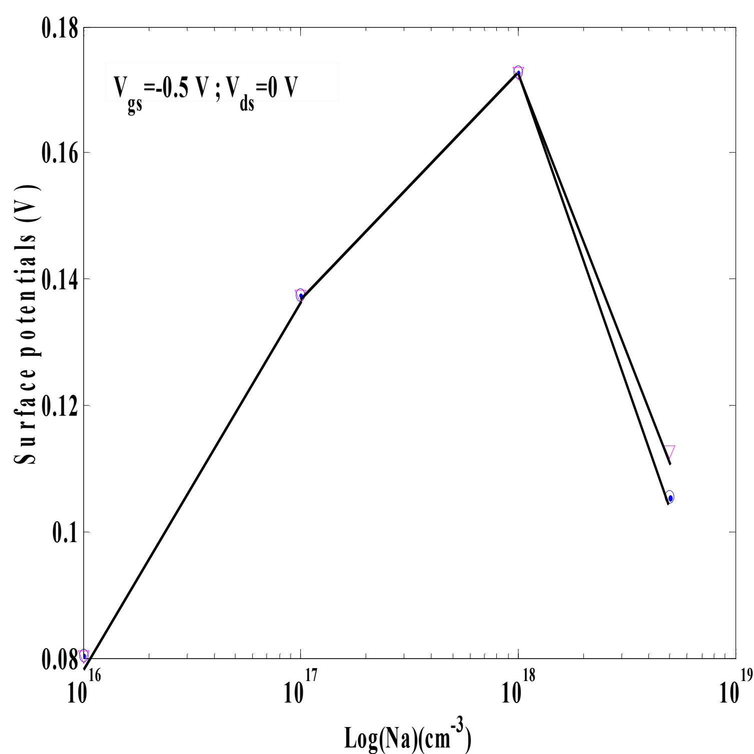

Figure 2A.2 Modeled (circles) and Simulated (triangles) potential at the surface of the Si layer as a function of N_a in the subthreshold regime for $t_{ox} = 3$ nm and $R = 5$ nm.

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2A.3.2 Threshold condition

From numerical calculation using 3D ATLAS simulation, the expression of the difference of potentials at the threshold voltage is found as:

$$\phi_{dT} = \phi_{dBT} + \Delta\phi_{dT} = \frac{Q_{dep} R}{2\varepsilon_{si}} + \frac{5}{8}\phi_t \qquad (2A.12)$$

Extending the threshold voltage expression given in [13] for double-gate (DG) MOSFETs to SRG MOSFETs, the surface potential at threshold condition is given by:

$$\phi_{sT} = 2\phi_F + \phi_t \ln\left[\frac{C_{ox}}{4C_{si}}\left(1 + \frac{\phi_t C_{ox}}{Q_{dep}}\right)\right] \qquad (2A.13)$$

where C_{ox} is the oxide capacitance of the cylindrical SRG MOSFET, and $C_{si} = \frac{\varepsilon_{si}}{2R}$ is the silicon capacitance per unit gate area.

while

$$\phi_{oT} = \phi_{sT} - \phi_{dT} \qquad (2A.14)$$

The potential at the center of the layer ϕ_{oT}, as a function of the layer concentration N_a has a maximum value for a doping

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concentration of $N_{a\max}$. The expression of $N_{a\max}$ is obtained by differentiating (2A.14) with respect to doping and making this derivative equal to zero.

The threshold voltage is calculated substituting (2A.13) in (2A.7):

$$V_T = V_{fb} + 2\phi_F + \phi_t \ln\left[\frac{C_{ox}}{4C_{si}}\left(1+\frac{\phi_t C_{ox}}{Q_{dep}}\right)\right] + \frac{1}{C_{ox}}\sqrt{\frac{4Q_{dep}\varepsilon_{si}\phi_t}{R}}\sqrt{\alpha_T}\sqrt{\frac{1}{2}+\left[\frac{1-\frac{1}{\alpha_T}+\frac{1}{\alpha_T}e^{-\alpha_T}}{\alpha_T}\right]\left[\frac{C_{ox}}{4C_{si}}\left(1+\frac{\phi_t C_{ox}}{Q_{dep}}\right)\right]} \quad (2A.15)$$

where α_T is the normalized difference between the surface and the center potential at threshold.

2A.3.3 Modeling of potentials in all regimes

Using the numerical calculation obtained from (2A.8) and (2A.12) we found that the difference between the surface and center potential can be expressed by empirical analytical expressions in the different conditions, in a similar way as for DG MOSFETs [13].

(a) Subthreshold

$$\phi_{d1} = \phi_{dBT} + \frac{19}{16}\phi_t \left[\frac{e^{\frac{V_{gs}-V_T-V_{ch}}{\phi_t}}}{1+e^{\frac{V_{gs}-V_T-V_{ch}}{\phi_t}}} \right] \qquad (2A.16)$$

(b) Above threshold for $N_a < N_{a\max}$

$$\phi_{d2a} = \left(\frac{\phi_{dBT}}{3} + \phi_{dM} - 0.028V\right) - \left(\frac{\phi_{dBT}}{3} + \phi_{dM} - 0.028V - \phi_{dT}\right)\left(\frac{1-\frac{V_{gs}-V_T-V_{ch}}{V_{GM}-V_T-V_{ch}}}{1+1.35(V_{gs}-V_T-V_{ch})}\right) \qquad (2A.17)$$

(c) Above threshold for $N_a > N_{a\max}$

$$\phi_{d2b} = \left(\frac{\phi_{dBT}}{2} + \phi_{dM} - 0.028V\right) - \left(\frac{\phi_{dBT}}{2} + \phi_{dM} - 0.028V - \phi_{dT}\right)\left(\frac{1-\frac{V_{gs}-V_T-V_{ch}}{V_{GM}-V_T-V_{ch}}}{1+1.35(V_{gs}-V_T-V_{ch})}\right) \qquad (2A.18)$$

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where V_{GM} is the maximum applicable gate voltage for the device (in our case $V_{GM} = 2\,\mathrm{V}$).

The complete expression for the difference of potentials ϕ_d valid from subthreshold to above threshold can be expressed using an interpolation function as in [13] for DG MOSFETs:

$$\phi_d = \phi_{d1}\frac{1}{2}\{1-\tanh[50(V_{gs}-V_T-V_{ch})]\}+\phi_{d2}\frac{1}{2}\{1+\tanh[50(V_{gs}-V_T-V_{ch})]\} \tag{2A.19}$$

where

$$\phi_{d2} = \phi_{d2a}\frac{1}{2}\{1-\tanh[10(\log(N_a)-\log(N_{a\max})-0.5)]\} + \phi_{d2b}\frac{1}{2}\{1+\tanh[10(\log(N_a)-\log(N_{a\max})-0.5)]\} \tag{2A.20}$$

As in [11] an empirical expression was found to describe the behavior of ϕ_{dM} up to $V_{GM} = 2\,\mathrm{V}$ as a function of gate dielectric and silicon layer thickness.

$$\phi_{dM} = 0.162 - 0.047t_{ox} + 0.0045t_{ox}^2 + 0.00836R - 12\times10^{-5}(R)^2 \tag{2A.21}$$

where t_{ox} and R are written in nm.

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The two empirical parameters have been adjusted to the best possible fit with the TCAD simulations regarding the difference between the surface and center potentials.

Figures 2A.3 (a, b and c), show a good agreement between the potential difference calculated by the model in expression (2A.19) and the 3D ATLAS simulations measured at the center of the channel (Figure 2A.3a) for V_{ds}= 0, and for V_{ds}> 0 at a position near the drain end (Figures 2A.3b and 2A.3c) for different doping concentrations and channel voltages.

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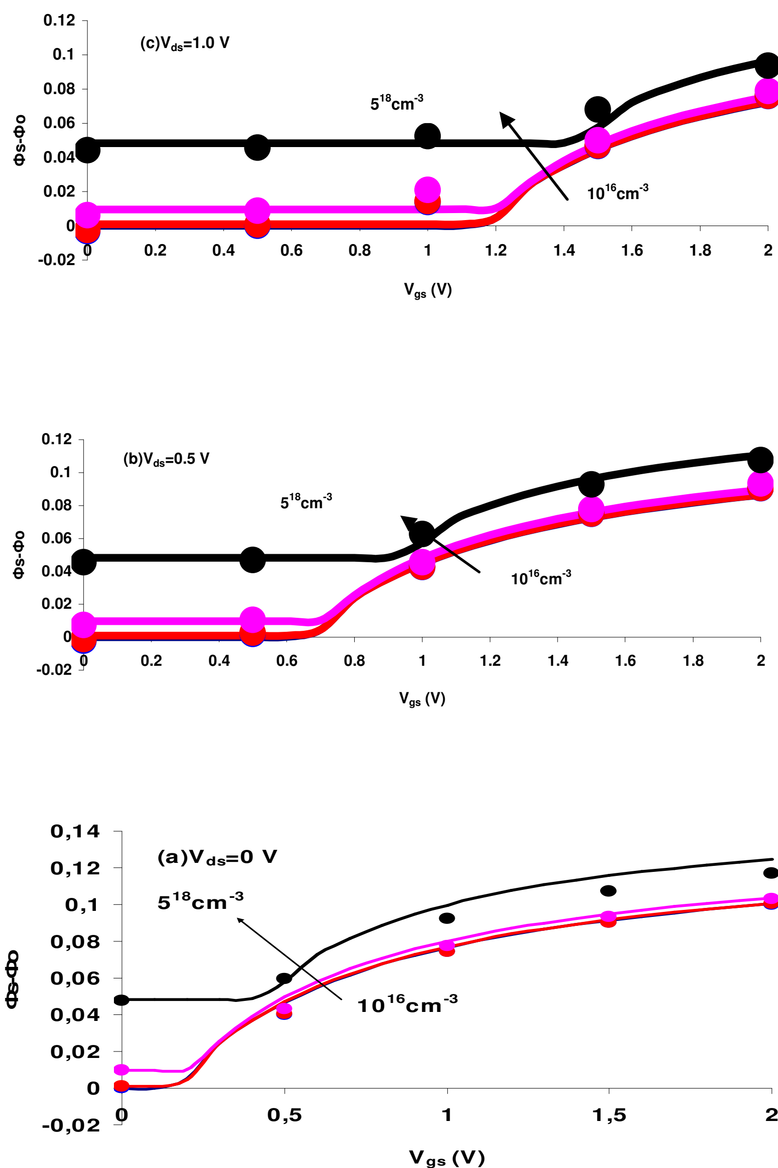

Figure 2A.3a, b and c. Modeled (solid lines) and numerically simulated (symbols) potential difference $\phi_s - \phi_o$ as a function of gate voltage for different Si layer concentration and V_{ds}= 0, 0.5 and 1 V, t_{ox}=3nm and R=5nm.

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The surface potential above threshold can be calculated from (2A.7) after substituting (2A.19) in α . The simplified expression for the surface potential above threshold is:

$$\phi_{sAT} = V_{gs} - V_{fb} - 2\phi_t LW\left[\frac{1}{2C_{ox}\phi_t}\sqrt{\frac{4Q_{dep}\varepsilon_{si}\phi_t}{R}}\sqrt{1-\frac{1}{\alpha}+\frac{1}{\alpha}e^{-\alpha}e^{\left(\frac{V_{gs}-V_{fb}-V_{ch}-2\phi_F}{2\phi_t}\right)}}\right] \quad (2A.22)$$

A complete expression for the surface potential valid from subthreshold to above threshold is obtained using an interpolation function as in [13] for DG MOSFETs:

$$\phi_s = \phi_{sBT}\frac{1}{2}\{1-\tanh[10(V_{gs}-V_T-V_{ch})]\} + \phi_{sAT}\frac{1}{2}\{1+\tanh[10(V_{gs}-V_T-V_{ch})]\} \quad (2A.23)$$

The potential at the center of the Si layer is calculated as:

$$\phi_o = \phi_s - \phi_d \quad (2A.24)$$

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Figure 2A.4 shows a good agreement between the overall surface potential calculated by the model and the one calculated by 3D ATLAS simulations in the subthreshold and near threshold regimes for the different doping concentrations considered. At higher gate voltages, the model potential is slightly higher than the simulation for all the doping concentration considered, but the agreement is acceptable, and as it will be shown, does not cause lack of accuracy in the modeled I-V characteristics.

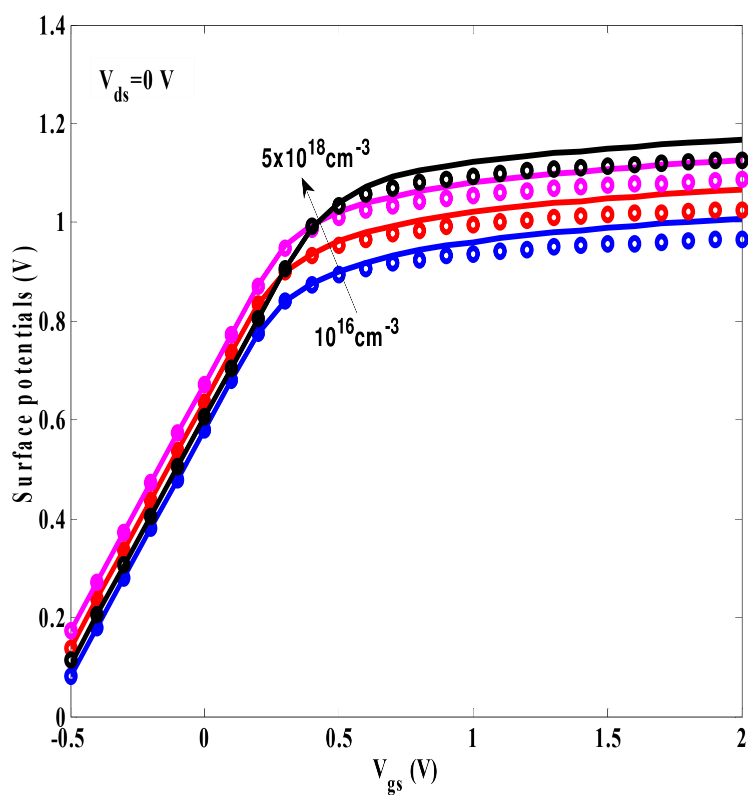

Figure 2A.4 Modeled (solid lines) and numerically simulated (symbols) surface potential as a function of gate voltage for different Si layer concentrations.

2A.4 Modeling charge carrier and current

2A.4.1 Charge carrier model

The charge carrier concentration at a certain position in the channel is determined by the following relation as governed by the Gauss's law at the silicon-oxide interface [10]:

$$-E_s = \frac{Q_{sem}}{\varepsilon_{si}} = \frac{C_{ox}\phi_t}{\varepsilon_{si}}\left(q_{in} + q_{dep}\right) \tag{2A.25}$$

where Q_{sem} is the semiconductor charge per unit gate area , $q_{in} = \frac{Q_{in}}{C_{ox}\phi_t}$ is the normalized inversion charges per unit gate area, and $q_{dep} = \frac{Q_{dep}}{C_{ox}\phi_t}$ is the normalized fixed charge density per unit gate area.

Substituting the expression of the electric field from (2A.6) in (2A.25), the normalized charge carrier concentration becomes equal to,

$$q_{in} = \sqrt{\frac{4q_{dep}\varepsilon_{si}}{C_{ox}R}}\sqrt{\alpha}\sqrt{\frac{1}{2} + \left[\frac{1 - \frac{1}{\alpha} + \frac{1}{\alpha}e^{-\alpha}}{\alpha}\right]e^{\frac{\phi_s - V_{ch} - 2\phi_F}{\phi_t}}} - q_{dep} \tag{2A.26}$$

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2A.4.2 Current model

Considering a drift-diffusion transport, the transistor current is calculated as [11]:

$$I_{DS} = \frac{W}{L} \mu C_{ox} \phi_t \int_{V_s}^{V_D} q_{in}(V) dV \tag{2A.27}$$

where W is the channel width (which for SRG MOSFETs is $W = 2\pi R$), L is the channel length (in our case $L = 1\mu m$), V_S and V_D are the channel potential at the source and drain respectively, and μ is the electron mobility.

Using (2A.26), the gate voltage V_{gs} in (2A.7) can be rewritten as

$$V_{gs} = V_{fb} + \phi_s + \phi_t (q_{in} + q_{dep}) \tag{2A.28}$$

Substituting ϕ_s from (2A.23) in (2A.26) and solving for V_{gs} the following general solution is obtained after neglecting few terms as:

$$V_{gs} - V_{fb} - \phi_t q_{dep} - V_{ch} - 2\phi_F + \phi_t \ln\left[\frac{1 - \frac{1}{\alpha} + \frac{1}{\alpha} e^{-\alpha}}{\alpha}\right]$$
$$= \phi_t q_{in} + \phi_t \ln\left[\left(\frac{2\alpha_{BT}}{\alpha}\right)\left(\frac{q_{in}}{q_{dep}}\left(\frac{q_{in}}{q_{dep}} + 2\right)\right)\right]$$
(2A.29)

The derivative of (2A.29) with respect to V_{ch} gives

$$-1 + \frac{d}{dV}\left[\phi_t \ln\left[\frac{1 - \frac{1}{\alpha} + \frac{1}{\alpha} e^{-\alpha}}{\alpha}\right]\right] = \phi_t\left[1 + \frac{1}{q_{in}} + \frac{1}{q_{in} + 2q_{dep}}\right]\frac{dq_{in}}{dV} + \phi_t \frac{d}{dV}\ln\left(\frac{2\alpha_{BT}}{\alpha}\right)$$
(2A.30)

Neglecting the logarithm terms on both sides, the following expression is obtained:

$$-1 = \phi_t\left[1 + \frac{1}{q_{in}} + \frac{1}{q_{in} + 2q_{dep}}\right]\frac{dq_{in}}{dV} \qquad (2A.31)$$

Substituting (2A.31) in (2A.27) and integrating q_{in} from its value at the source, q_s, to its value at drain, q_d, the current is expressed as:

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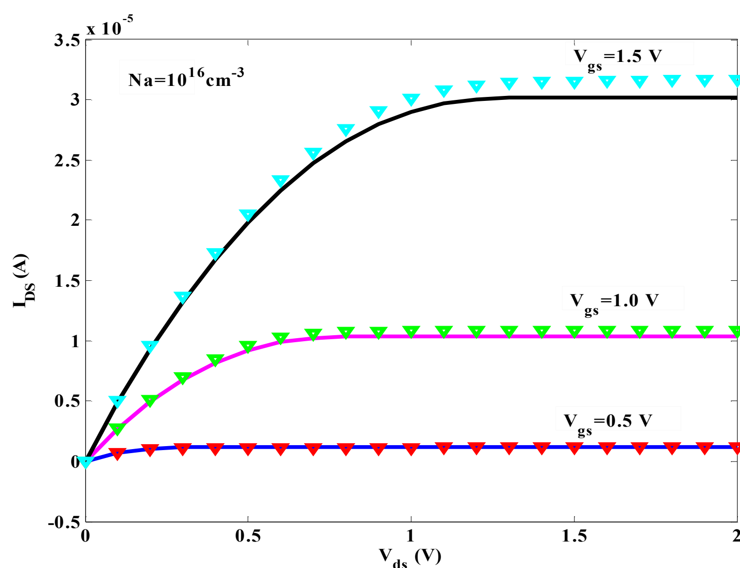
$$I_{DS} = I_o \left[2(q_s - q_d) + \frac{q_s^2 - q_d^2}{2} + 2q_{dep} \ln\left[\frac{q_d + 2q_{dep}}{q_s + 2q_{dep}} \right] \right], \tag{2A.32}$$

where $I_o = \frac{W}{L} \mu C_{ox} \phi_t^2$.

Figure 2A.5 (a1-a4) show a good agreement between output characteristics by the model and the 3D ATLAS simulations by considering constant mobility (1000 cm^2/Vsec) for doping concentrations from 10^{16} cm^{-3} to 5 x 10^{18} cm^{-3} at different gate voltages. In Figure 2A.5 (b1-b4) the transfer characteristics calculated between the model and the 3D ATLAS simulation show a good agreement for the doping concentrations from 10^{16} cm^{-3} to 5 x 10^{18} cm^{-3}.

a-1



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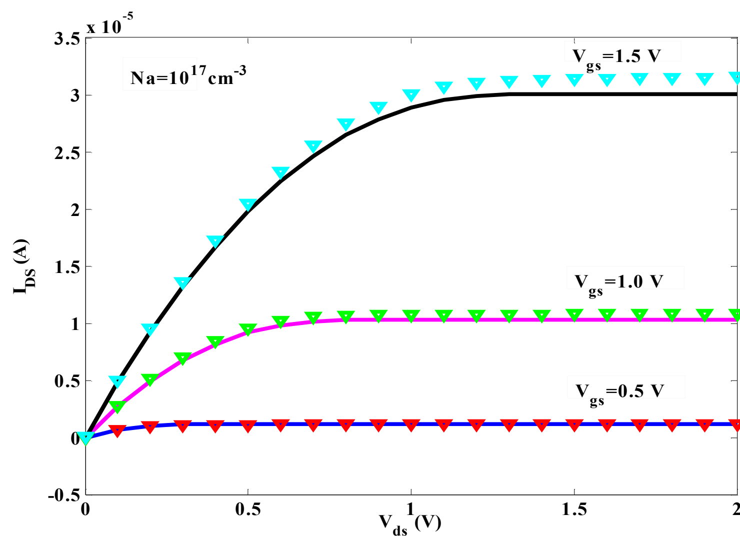
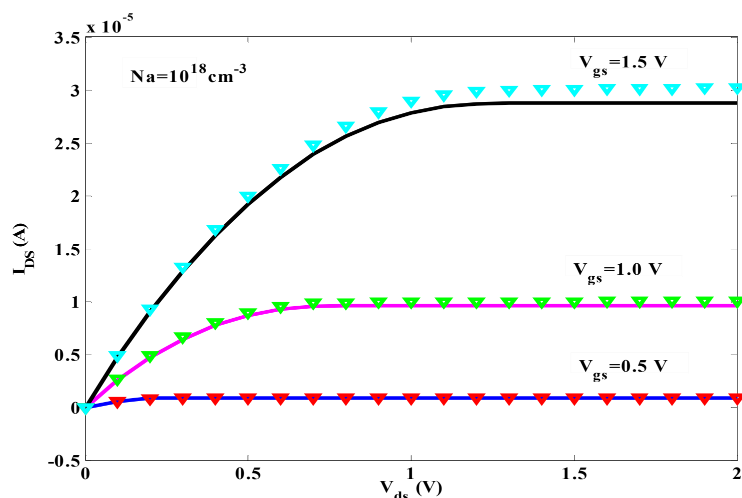


Figure 2A.5 Output (a1-a2) characteristics. Solid lines: compact model. Symbols: 3D numerical simulations with ATLAS. The doping concentration as indicated in the plot.

a-3



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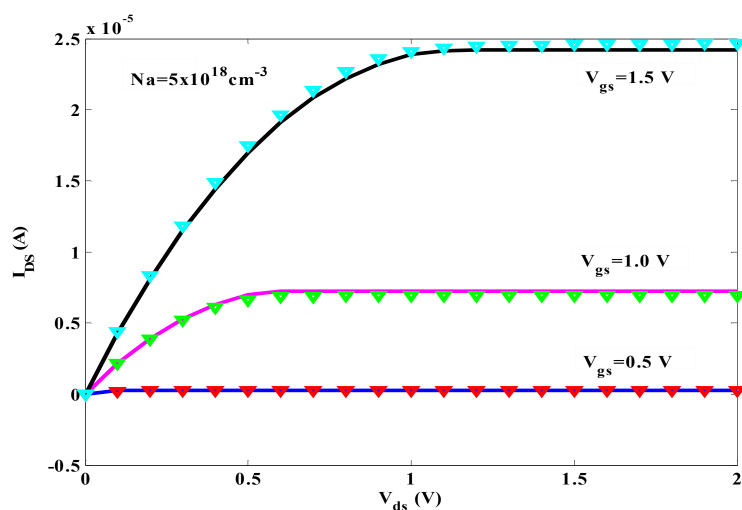

Figure 2A.5 Output (a3-a4) characteristics. Solid lines: compact model. Symbols: 3D numerical simulations with ATLAS. The doping concentration as indicated in the plot.

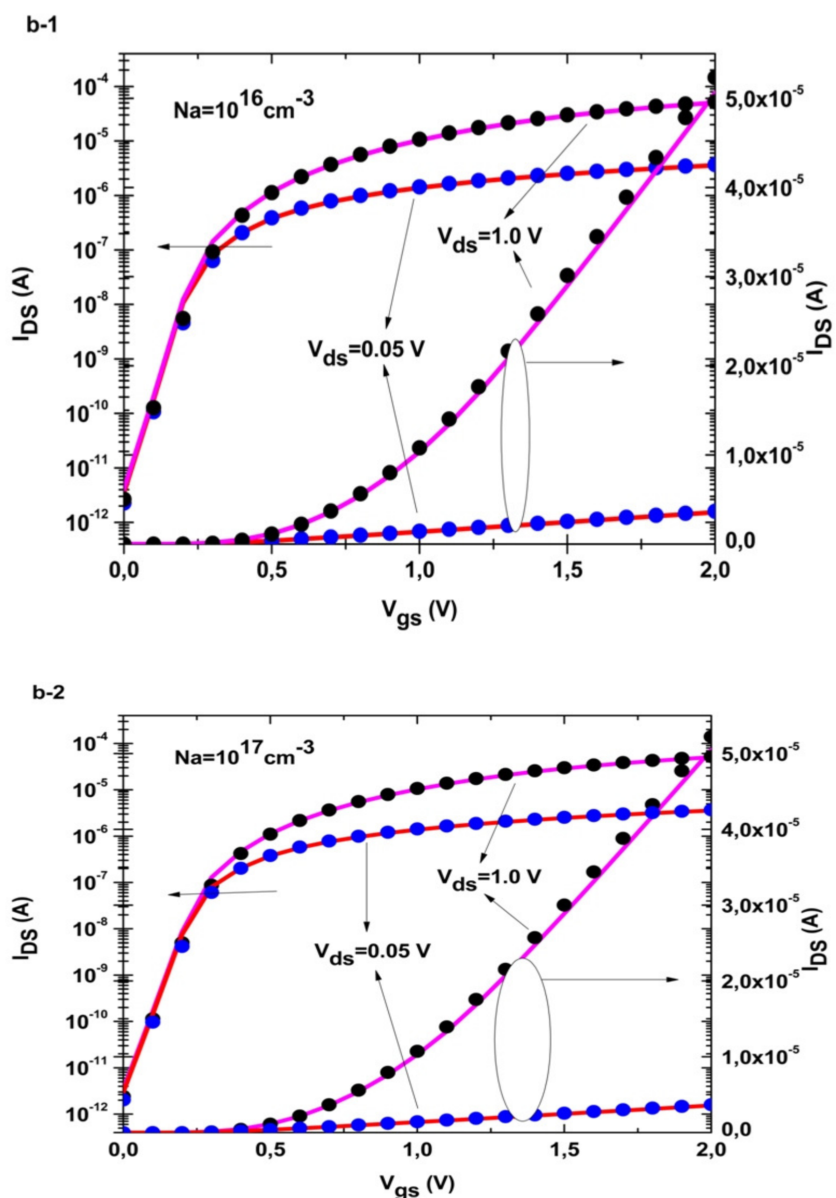

Figure 2A.5 Transfer (b1-b2) characteristics in logarithmic and linear scale. Solid lines: compact model. Symbols: 3D numerical simulations with ATLAS. The doping concentration as indicated in the plot.

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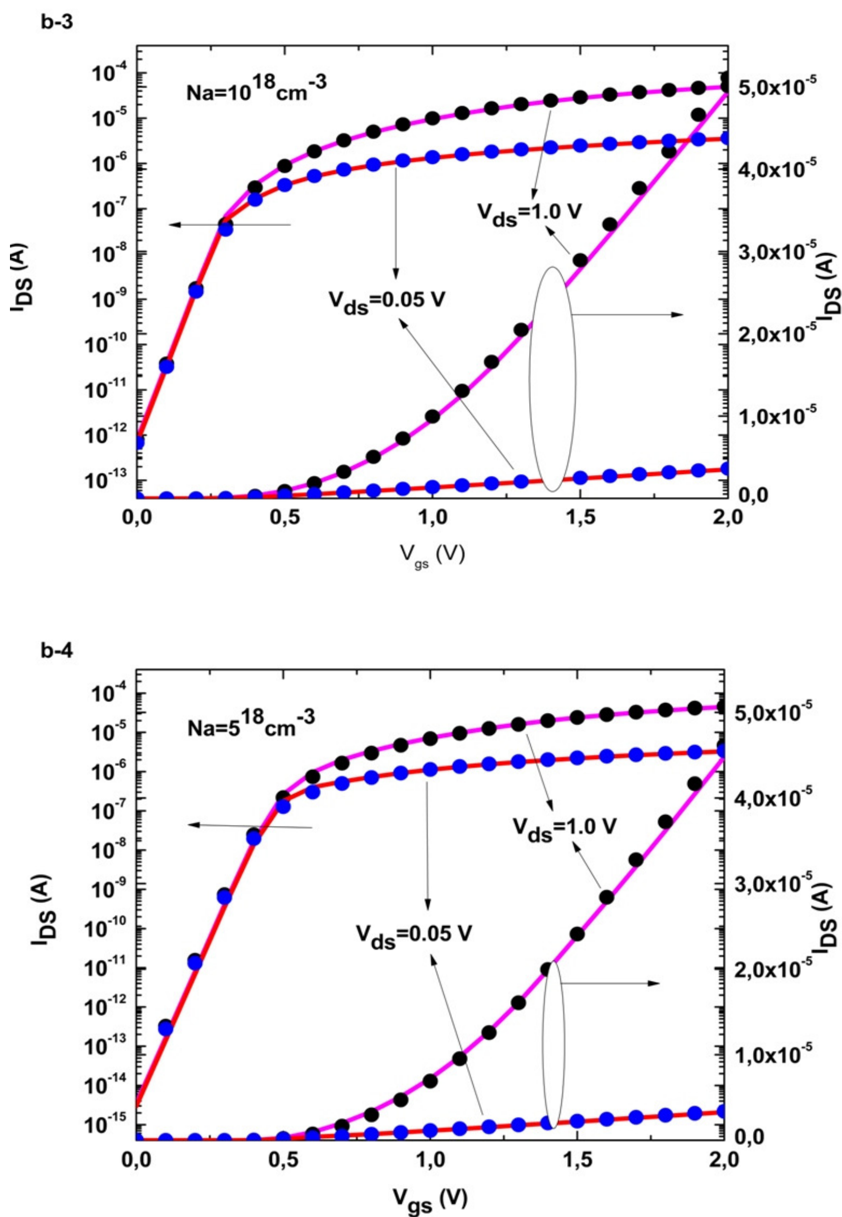

Figure 2A.5 Transfer (b3-b4) characteristics in logarithmic and linear scale. Solid lines: compact model. Symbols: 3D numerical simulations with ATLAS. The doping concentration as indicated in the plot.

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2B. Compact drain current model reproducing advanced transport models in nanoscale cylindrical surrounding-gate (SRG) MOSFETs

2B.1 Introduction

The surrounding-gate (SGT) MOSFET is one of the most promising candidates for the downscale of CMOS technology toward the nanometer-channel-length range since the SGT architecture allows excellent control of the channel charge in the silicon film, reducing short-channel effects (SCE) [14-17]. These devices include important features that permit more aggressive channel length scaling than to their conventional bulk counterparts. In this context, it is important to highlight the efforts currently under way in relation to multigate MOSFETs compact modeling [18-20]. The continuous scaling in the IC industry makes the reduction in the active silicon area in multigate MOSFETs essential in order to keep the short channel

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effects (SCE) under control [4]. Therefore, the influence of structural confinement is increasing, which makes the charge distribution in these devices completely different to that found in conventional bulk. Hence, there is a great need for new compact models that accurately describe the physics of these devices [21]. Our starting point, in this section is an analytical expression that models the variation of surface potential as well as the difference of potential at the surface and at the middle of the silicon layer [22]. The expression obtained for the potentials is used to derive an analytical compact model for the drain current of a cylindrical surrounding-gate MOSFETs. This model was derived for doped devices, but it has been demonstrated to be valid in lightly doped devices. We extend the model to include hydrodynamic transport and quantum mechanical effects. As the channel length is reduced 3D effects appear near the source and drain producing the so-called SCE such as drain-induced barrier lowering (DIBL). The DIBL effect is considered through a threshold voltage correction in the compact model. Using the concept of inversion layer centroid, we have introduced a

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correction in the oxide capacitance to improve the accuracy in the strong inversion region [21]. Velocity overshoot is modeled through the hydrodynamic transport [23] which is also included in the model. The model takes into account the mobility degradation [24] due to scattering effects. The final compact model for the drain current includes hydrodynamic transport, mobility degradation, short channel effects such as DIBL and quantum effects. Comparisons between the compact model and 3D advanced numerical transport models are shown.

2B.2 DC model

2B.2.1 Expression for potentials

The potentials at the surface, ϕ_s, and in the center, ϕ_o, of the silicon layer are calculated analytically. The surface potential in the subthreshold ϕ_{sBT} regime are calculated analytically using the Lambert function as [22]:

$$\phi_{sBT} = V_{GS} - V_{fb} - \frac{Q_{dep}}{C_{ox}^{*}} - \phi_t LW\left[\frac{Q_{dep}}{C_{ox}^{*}\phi_t} e^{\left(\frac{V_{GS}-V_{fb}-\frac{Q_{dep}}{C_{ox}^{*}}-V_{ch}-2\phi_F}{\phi_t}\right)}\right] \tag{2B.1}$$

and in the above threshold regime as:

$$\phi_{sAT} = V_{GS} - V_{fb} - 2\phi_t LW\left[\frac{1}{2C_{ox}^{*}\phi_t}\sqrt{\frac{4Q_{dep}\varepsilon_{si}\phi_t}{R}}\sqrt{1-\frac{1}{\alpha}+\frac{1}{\alpha}e^{-\alpha}}\, e^{\left(\frac{V_{GS}-V_{fb}-V_{ch}-2\phi_F}{2\phi_t}\right)}\right] \tag{2B.2}$$

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where V_{GS} is applied to the gate voltage, V_{fb} is the flat band voltage, $Q_{dep} = qN_a R/2$ is the fixed charge density per unit gate area, N_a is the doping concentration, R is the radius of the cylindrical silicon body, $\phi_t = \frac{kT}{q}$ is the thermal voltage, V_{ch} is the quasi-Fermi potential along the channel, $\phi_F = \phi_t \ln(N_a / n_i)$ is the Fermi potential, $\alpha = (\phi_s - \phi_o)/\phi_t$ is the normalized difference of potentials, ε_{si} is the permittivity of silicon, q is the electric charge. The inversion centroid is a function of the inversion charge. A simple relationship between inversion centroid and inversion charge obtained by fitting numerical simulation results is given by $\frac{1}{z_I} = \frac{1}{a+2bR} + \frac{1}{z_{IO}}\left(\frac{N_I}{N_{IO}(R)}\right)^n$ [21] with $a = 0.55$ nm, $b = 0.198$, $z_{IO} = 5.1$ nm, $n = 0.75$, and $N_{IO}(R) = 8.26\times10^{12}$ cm^{-2}- 4.9×10^{18} cm$^{-3}\times R(cm)$. The classical oxide capacitance C_{ox} was replaced in our model by another capacitance, corrected oxide capacitance (C_{ox}^*) , where the

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capacitance of the oxide was in series with a centroid capacitance, which is the capacitance of a silicon layer as [21]:

$$\frac{1}{C_{ox}^{*}}=\frac{1}{C_{ox}}+\frac{1}{C_{cen}} \qquad (2B.3)$$

where $C_{cen}=\dfrac{\varepsilon_{si}}{(R-z_I)\ln\left(1+\dfrac{z_I}{(R-z_I)}\right)}$ and

$C_{ox}=\dfrac{\varepsilon_{ox}}{R\ln\left(1+\dfrac{t_{ox}}{R}\right)}$ is the oxide capacitance per unit gate area in a SRG MOSFET, t_{ox} is the oxide thickness, ε_{ox} is the permittivity of oxide.

The final surface potential in all regimes are calculated as:

$$\phi_s=\phi_{sBT}\frac{1}{2}\{1-\tanh[10(V_{GS}-V_T-V_{ch})]\} + \phi_{sAT}\frac{1}{2}\{1+\tanh[10(V_{GS}-V_T-V_{ch})]\} \qquad (2B.4)$$

where V_T is the threshold voltage as shown in (2A.15) [22].

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2B.2.2 Mobile charge

Mobile charge as a function of the surface potential is obtained solving Poisson's equation. Their normalized values at the source, q_S, and at the drain, q_D, are given by the following expression as in [22]:

$$q_{S(D)} = \sqrt{\frac{4q_{dep}\varepsilon_{si}}{C_{ox}^{*}R}}\sqrt{\alpha}\sqrt{\frac{1}{2}+\left[\frac{1-\frac{1}{\alpha}+\frac{1}{\alpha}e^{-\alpha}}{\alpha}\right]e^{\frac{\phi_s - V_{S(D)} - 2\phi_F}{\phi_t}}} - q_{dep} \quad (2B.5)$$

where $q_{dep} = \dfrac{Q_{dep}}{C_{ox}^{*}\phi_t}$ is the normalized fixed charge density per unit gate area.

2B.2.3 DIBL Effect

The drain-induced barrier lowering (DIBL) is considered through a threshold voltage correction ΔV_T as [25]:

$$\Delta V_T = \sigma\phi_F\left(\frac{L_c}{L}\right)^2\left[1-e^{\left(-\frac{L}{0.25L_m}\right)}\right]\left[1+\frac{|V_{ch}|}{3.6\phi_t}-e^{\left(\frac{|V_{ch}|}{2.5\phi_t}\right)}\right] \quad (2B.6)$$

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where σ is the fitting parameter, L_m is a reference length = 1×10^{-5} cm and $L_c = \sqrt{\dfrac{2\varepsilon_{si}R^2 \ln\left(1+\dfrac{2t_{ox}}{R}\right)+\varepsilon_{ox}R^2}{16\varepsilon_{ox}}}$ is the characteristics length [4].

One of the most used expressions for the saturation potential [26] has been corrected as

$$V_{dssat} = \left(-\frac{Q_{seff}}{C_{ox}^*}\right)\left(\frac{v_{sat}}{\left(\dfrac{-Q_{seff}\mu_{eff}}{2LC_{ox}^*}\right)+v_{sat}}\right) \tag{2B.7}$$

with $$Q_{seff} = q_s + 4\frac{kT}{q}C_{ox}^*\left(\frac{v_{sat}}{v_{sat}-\dfrac{kT}{q}\left(\dfrac{\mu_{eff}}{L}\right)}\right) \tag{2B.8}$$

where v_{sat} the saturation velocity.

The effective drain voltage valid in linear and saturated region is calculated as:

$$V_{Def} = V_{dssat} + \frac{1}{2}\left[\left(V_{ch} - V_{dssat} - \frac{\phi_t}{3}\right) - \sqrt{\left(V_{ch} - V_{dssat} - \frac{\phi_t}{3}\right)^2 + 4\frac{\phi_t}{3}V_{dssat}}\right] \quad (2B.9)$$

In the subthreshold region, the effective voltage must be adjusted to represent the real behaviours, so a complementary effective drain voltage is defined as:

$$V_{Defs} = V_D \frac{1}{2}\{1 - \tanh[5(V_{GS} - V_T)]\} + V_{Def} \frac{1}{2}\{1 + \tanh[5(V_{GS} - V_T)]\} \quad (2B.10)$$

A smoothing function is used to interpolate V_{dss} :

$$V_{dss} = V_{Defs} - \frac{kT}{q} \frac{\ln\{1 + \exp[A(V_{Defs} - V_{dssat})/(kT/q)]\}}{A} \quad (2B.11)$$

where A is the parameter that controls the transition between saturated and nonsaturated channels.

2B.2.4 Velocity overshoot

In extremely short channel multigate MOSFET the transport regime is quasi-ballistic, thus an important overshoot velocity is expected. Using a simplified energy-balance model, the electron mobility is a function of the electron temperature related to the average energy of the carriers. The electron temperature T_e is governed by the following equation [23]:

$$\frac{dT_e}{dx} + \frac{T_e - T_O}{\lambda_w} = -\frac{q}{2k} E_x(x) \qquad \text{(2B.12)}$$

where the energy-relaxation length is defined as $\lambda_w \approx 2v_{sat}\tau_w$, τ_w being the energy relaxation time constant, v_{sat} the saturation velocity and $E_x(x)$ is the lateral electric field.

The velocity increases along the channel, and at the saturation voltage, the velocity reaches a saturation velocity. Assuming that the velocity is saturated we can divide the channel into two sections: the first section $0 \langle x \langle L_e = L - L_{sat}$, and the saturation region, $x \rangle L_e$. In contrast with classical drift-diffusion models, the saturated velocity in the saturation region due to nonstationary effects can achieve several times the stationary

saturation velocity, v_{sat}. This phenomenon is known as velocity overshoot. The velocity overshoot has been modeled through hydrodynamic transport model.

2B.2.5 Drain Current

The drain-current in a DG MOSFET is calculated as a function of the mobile-charge densities at the source Q_s and at the drain Q_d [22]:

$$I_{DS} = \frac{W\mu_{eff}}{L_e\left(1+\gamma_n V_{dss}\right)}\left[2\left(q_S - q_D\right) + \frac{q_S^2 - q_D^2}{2} + 2q_{dep}\ln\left[\frac{q_D + 2q_{dep}}{q_D + 2q_{dep}}\right]\right] \tag{2B.13}$$

The effective mobility defined as [24]

$$\mu_{eff} = \frac{\mu_o}{1+\theta_1\beta\log(1+\exp(1+\left(V_{GS}-V_T\right)/\beta)+\theta_2\beta^2\log(1+\exp(1+\left(V_{GS}-V_T\right)/\beta)^2} \tag{2B.14}$$

where μ_o is the low-field mobility, and θ_1 and θ_2 are the mobility attenuation coefficients of the first and second orders, respectively, which can be considered as fitting parameters,

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$\gamma_n = \frac{\mu_{eff}}{v_{sat} L}\left(\frac{1}{1+2\lambda_w / L}\right)$, V_{dss} is equal to V_{Defs} for a nonsaturated channel and $V_{dss} = V_{dssat}$ for a saturated channel, and $L_e = L - \Delta L$ and $W = 2\pi R$ are the device effective length and width respectively, where the saturated channel length is given by

$\Delta L = L_c \arcsin h\left(\frac{V_{Defs} - V_{dssat}}{E_{sat} L_c}\right)$, and E_{sat} is the saturation field when velocity reaches the saturation velocity.

2B.3. Simulated Device

The cylindrical SRG MOSFET shown in Figure 2B.1 has a physical gate length of 6 nm, a gate stack consisting of 2 nm of HfO2 on top of 0.7nm of SiO2 (EOT=1 nm). The channel is lowly doped (10^{15} cm^{-3}). The channel diameter is 4 nm.

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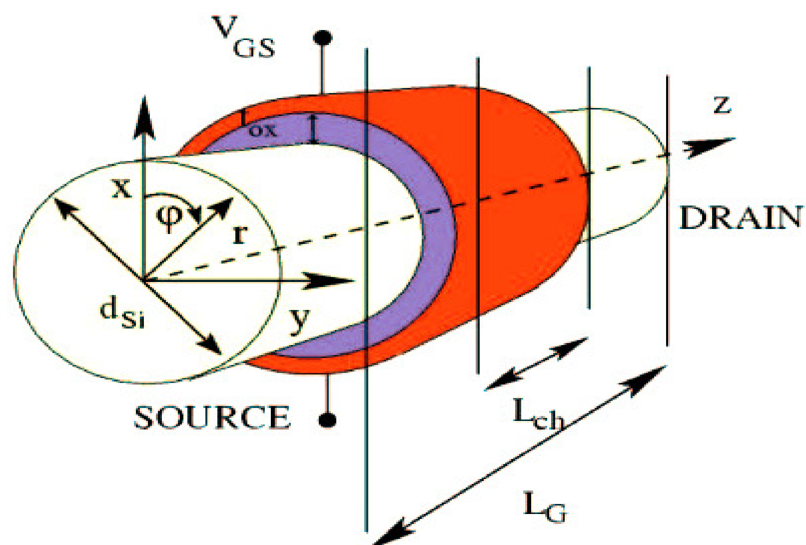

Figure 2B.1 Structure of the cylindrical SRG MOSFET template.

2B.4. Simulated Approaches

Each model is identified with the acronym of the main developer are presented. The possible modeling approaches range from modifications of the conventional drift-diffusion (DD) model used in commercial TCAD tools to advanced Monte Carlo models. The different numerical models used by the different groups [27]-[30], differ in terms of scattering mechanisms, simulation approaches, etc. In order to compare, all simulators have been calibrated first to reproduce the curves in silicon devices.

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2B.4.1 SNPS (Synopsis Switzerland LLC)

In SNPS model [27], at low drain bias, the effect of mobility degradation is seen at higher gate voltages.

2B.4.2 SNPS with Ion impurities (II)

In SNPS with ion impurities (II) [27], the drain current has a stronger mobility degradation effect when compared to the other groups. The effect of ion impurity scattering has a strong influence on the drain current and hence the drain current is lower than the other groups.

2B.4.3 IUNET- BO(Consorzio Nazionale Interuniversitario per la Nanoelettronica)-University of Bologna (Quantum Ballistic)

The tight-binding approach employed to work out the system Hamiltonian on quantum transport under ballistic condition [28]. The mobility degradation is not significant. It can be seen the velocity saturation takes place at higher values.

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2B.4.4 IUNET-BO (Semiclassical Ballistic)

Scattering events are accounted for via relaxation-time approximation, which holds for elastic collisions only [29]. The mobility degradation is not significant.

2B.4.5 IUNET-BO (Acoustic phonon and Surface roughness)

In IUNET-BO: with Acoustic Phonon (AP) and Surface Roughness (SR) [29], the mobility degradation has a slight influence on the drain current. Also, the effect of velocity saturation is stronger than the other groups which can be seen clearly.

2B.4.6 IMEP (Institut de Microélectronique, Electromagnétisme et Photonique), Grenoble (France)

In IMEP model [30], the drain current is higher than other models considered in this paper. It considers backscattering. The effect of mobility degradation is lower when compared to other models which consider scattering.

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2B.5. Results and Discussion

The results of the compact model have been compared with the 3D numerical simulation data obtained by several research groups using advanced transport models [27]-[30]. Figure 2B.2 shows the transfer characteristics of the Cylindrical SRG MOSFET at low and high V_{DS}. A good agreement between the compact model and the 3D numerical simulations [27]-[30] is obtained by considering the low field mobility and for a fitted saturation velocity. In the transfer characteristics it can be clearly noted that the mobility degradation at low drain voltages is significantly reproduced by the compact model. In the IMEP model it can be observed that the effect of mobility degradation parameter is lower when compared to the other models may be due to the fact that surface roughness scattering is not considered in the IMEP model.

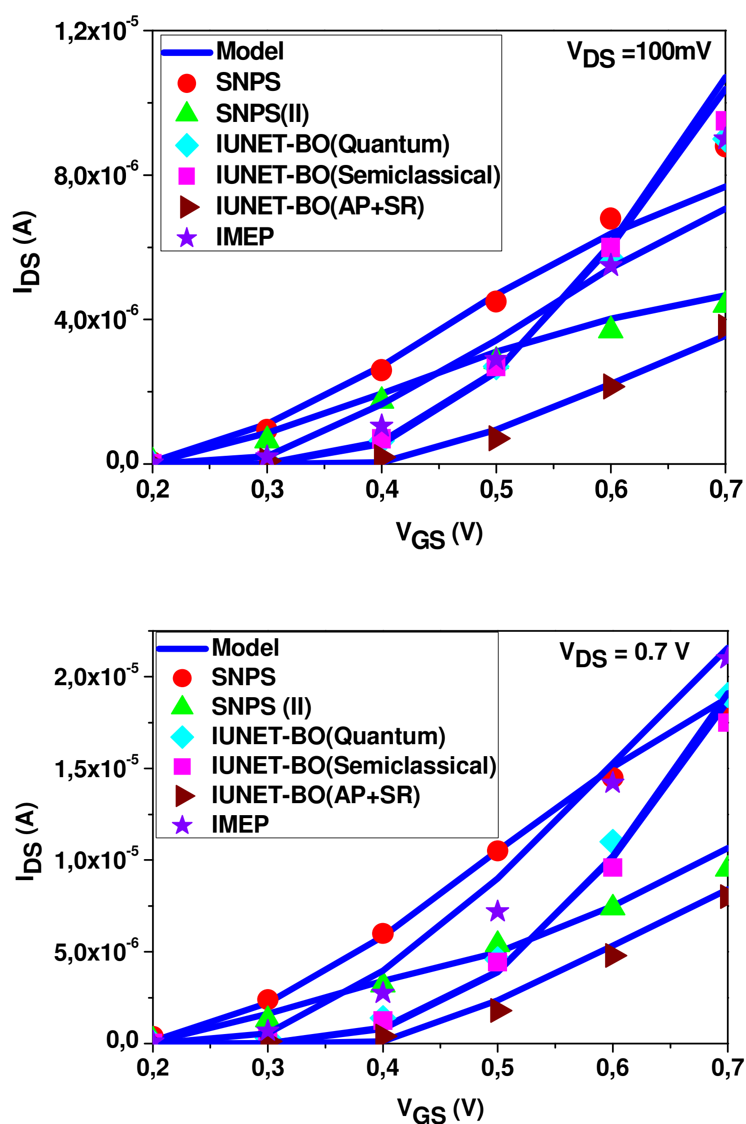

Figure 2B.2 Transfer characteristics of the cylindrical SRG MOSFET (Figure 2B.1) for low (top) and high (bottom) V_{DS}. 3D numerical simulation data by Synopsys (SNPS) [27], Univ. of Bologna (IUNET-BO) [28]-[29], IMEP [30]

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Table 2B.1 indicates the mobility degradation and velocity saturation parameter values that have been considered in the model to fit the different numerical simulations of the cylindrical SRG MOSFET shown in Figure 2B.1. From the table parameters it can be seen that strong mobility degradation is observed with the SNPS (ion impurities) model. It can be seen that lower mobility degradation is observed with the IMEP model as discussed before.

Models	**Cylindrical SRG MOSFET L_G=6nm Dsi=4nm EOT=1.0nm device parameters**		
	V_{sat} x 10^7 (cm-sec^{-1})	**$\theta_1(V^{-1})$**	**$\theta_2(V^{-2})$**
SNPS	**1.5**	**3.35**	**0.7**
SNPS (Ion Impurities)	**1.65**	**6.15**	**1.1**
IUNET-BO (Quantum Ballistic)	**1.05**	**0**	**0**
IUNET-BO (Semiclassical Ballistic)	**1.05**	**0**	**0**
IUNET-BO (Acoustic phonon and Surface Roughness)	**1.45**	**5.25**	**2.55**
IMEP	**1.35**	**3.25**	**0.55**

Table 2B.1 Parameters used in the proposed analytical model in order to fit the simulations obtained from advanced transport models.

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Figure 2B.3 shows the transfer characteristics of a longer-channel cylindrical SRG MOSFET at high V_{DS}. A good agreement between the compact model and the 3D numerical simulation data [31] is obtained both in subthreshold and above threshold by considering the low field mobility and for a fitted saturation velocity.

Figure 2B.4 shows the transfer characteristics of an L_G = 13 nm cylindrical SRG MOSFET at high V_{DS}. Also, a good agreement between the compact model and the 3D numerical simulation data [31] is obtained both in subthreshold and above threshold by considering the low field mobility and for a fitted saturation velocity.

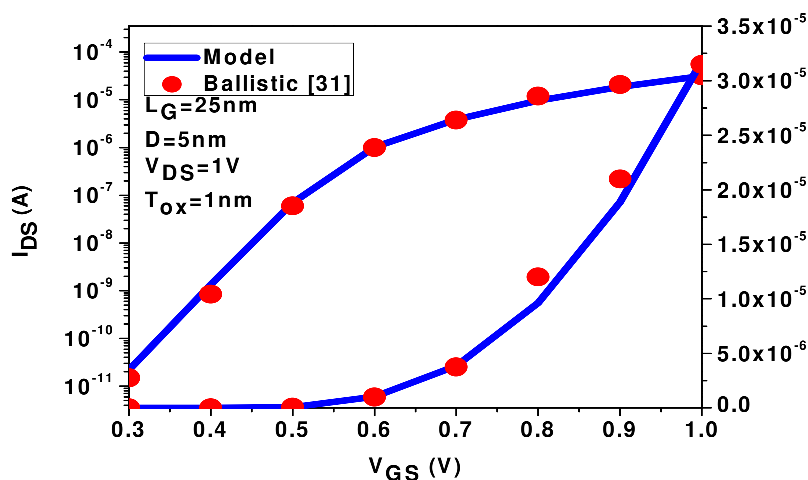

Figure 2B.3 Transfer characteristics of a cylindrical SRG MOSFET at high V_{DS} both in linear and logarithmic scale.

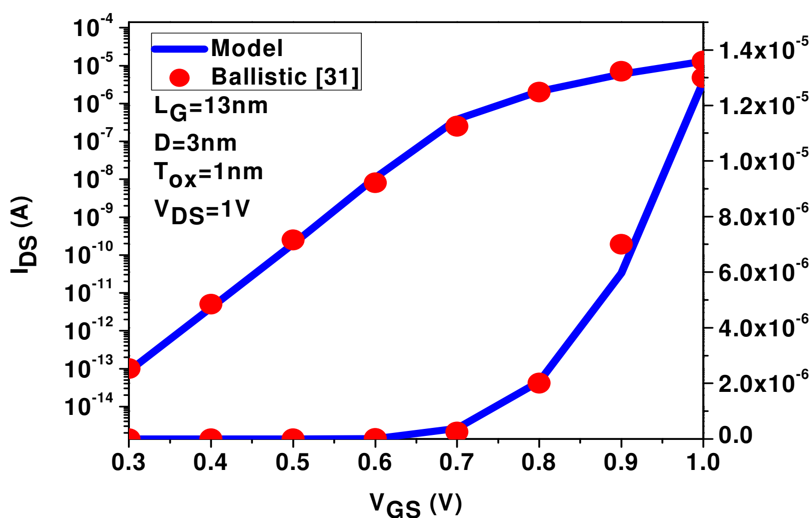

Figure 2B.4 Transfer characteristics of a cylindrical SRG MOSFET at high V_{DS} both in linear and logarithmic scale.

Table 2B.2 shows the mobility degradation and velocity saturation parameter values that have been used to fit the numerical simulations of [31], which is a longer-channel SRG MOSFETs.

Model	**Cylindrical SRG MOSFET L_G=25nm Dsi=5nm**			**Cylindrical SRG MOSFET L_G=13nm Dsi=3nm**		
	V_{sat} x 10^7 (cm-sec^{-1})	**$\theta_1(V^{-1})$**	**$\theta_2(V^{-2})$**	**V_{sat} x 10^7 (cm-sec^{-1})**	**$\theta_1(V^{-1})$**	**$\theta_2(V^{-2})$**
Ballistic [31]	**1.05**	**0**	**0**	**1.05**	**0**	**0**

Table 2B.2 Parameters used in the proposed analytical model in order to fit the simulations obtained from advanced transport models.

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2C Conclusions

In this chapter, we have presented a compact analytical model for long-channel doped surrounding-gate MOSFETs valid from low to high dopings. The channel charge density is calculated as an explicit expression resulting from explicit models of the surface and center potential. The current expression is written in terms of the expressions of the mobile charge densities at the source and drain. Good agreement is observed between the modeled characteristics and the 3D numerical simulations for the whole practical range of bias and doping concentrations.

The compact model is extended model to include hydrodynamic transport, short channel effects, mobility degradation due to scattering mechanisms, velocity overshoot and quantum effects. The comparisons between the advanced numerical transport models and the compact model for the drain current in cylindrical SRG MOSFET show that if our compact model includes the hydrodynamic transport model it can reproduce those simulation results based on 3D advanced transport models. The model is valid and continuous in all regimes.

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Chapter 3

Compact Drain Current model to reproduce advance transport model for double-gate (DG) MOSFETs

In this section, our compact drain current model for double-gate (DG) MOSFET has been extended to include the hydrodynamic transport and quantum mechanical effects. The final compact model can accurately reproduce simulation results of some of the most advanced transport simulators. The model is based on a compact model for charge quantization within the channel and it includes mobility degradation, channel length modulation, drain-induced barrier lowering, overshoot velocity effects and quantum mechanical effects. The temperature dependency is also accounted in the compact model.

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3.1 Introduction

State-of-the-Art devices in mass production are approaching to the performance limit of traditional MOSFET as the critical dimensions are shrunk. Multi-gate devices based on SOI technology, are one of the best candidates to become a standard solution to overcome the problems arising from such aggressive scaling [1]. Many modeling approaches for the determination of the drain current in MOSFETs are currently used and developed [2]. One of the main reasons driving these modeling efforts is the industry need to understand performance improvements due to ballistic or quasi-ballistic transport and other technology boosters such as strain, high-k dielectrics and extremely thin body Silicon-On-Insulator (ETSOI) architectures [3]. Among the various proposals, the SOI Double-Gate MOSFET (DG) appears to be one of the most promising due to the shield-effect played by the double gate, which strongly reduces drain-induced barrier lowering and minimizes threshold sensitivity to channel length [4]. Volume inversion (VI) regime is observed in DG MOS structure presenting a significant number of advantages, such as enhancement of the number of minority carriers; increase in carrier mobility and velocity; as a consequence, an increase in drain current and transconductance [5-6]. Hence, ETSOI DG MOS transistors are considered to be a very attractive option to improve the performance of CMOS devices. Nanoscale DG-MOSFETs introduce challenges to compact

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modeling associated with the enhanced coupling between the electrodes (source drain and gates), quantum confinement, ballistic or quasi-ballistic transport, gate unnelling current, etc. [7]. Most models presented so far are for undoped devices with a long enough channel to assume that the transport is due to the drift-diffusion mechanism [8–10]. Very little work has been done on the transition from the ballistic regime to drift diffusion [11-13]. For thinner layers, quantum effects start to play a role, but might eventually be considered as a correction to the classical derivation.

In this chapter we present the extension of a DG MOSFET model to nanoscale technology nodes by incorporating hydrodynamic transport and quantum mechanical effects, validating it by comparison with numerical 2D transport models ranging from drift-diffusion (DD) to direct solutions of the Boltzmann-Transport-Equation (BTE) with the Monte Carlo method. Our starting point in this work is our previous analytical classical model for the undoped DG MOSFET [14]. We extend this compact model for the drain-current to include mobility degradation, short-channel effects (SCE), channel length modulation (CLM), hydrodynamic transport (and therefore velocity overshoot) and quantum effects [15-16]. The backbone of our model is based on the charge control model [16]. The classical unified charge control model is extended to include quantization effects within the channel using the concept of

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inversion layer centroid. A correction in the oxide capacitance is included in order to improve the accuracy on the strong inversion region [7]. Finally, we obtain a compact charge control model including quantum effects whose explicit formulation is similar to classical charge control model. Also, we have included the channel length modulation effect, as well as the role played by quantum effects on the mobility degradation of these devices [4]. The model is validated by comparison with 2D numerical simulations based on different transport models including some of them quantum confinement effects.

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3.2 DC model

3.2.1 Classical Charge Control Model

The mobile charge densities at the source Q_s and at the drain Q_d are calculated by [14] and the charge expression also includes the DIBL effect.

$$Q=2C_g\left(\frac{2C_g\beta^2}{Q_o\exp\left(\frac{V_{sce}}{\beta}\right)}+\sqrt{\left(\frac{2C_g\beta^2}{Q_o\exp\left(\frac{V_{sce}}{\beta}\right)}\right)^2+4\beta^2\log^2\left[1+\exp\left[\frac{V_{gs}-V_{th}+\Delta V_{th}-V}{2\beta}\right]\right]}\right) \quad (3.1)$$

where $Q_o=4\beta C_{si}$ and $\beta=\frac{kT}{q}$, $C_{si}=\frac{\varepsilon_{si}}{T_{si}}$ is the silicon-film capacitance, ε_{si} is the permittivity of silicon, T_{si} being the silicon film thickness. V_{th} is defined as

$$V_{th}=V_o+2\beta\log\left(1+\frac{Q'}{2Q_o}\right) \quad (3.2)$$

where Q', shown in (3.3), is calculated by solving (3.1) for Q but using V_o instead of V_{th} (3.2) and without considering the ΔV_{th} correction.

$$Q^{'} = C_g \left(-\frac{2C_g\beta^2}{Q_o \exp\left(\frac{V_{sce}}{\beta}\right)} + \sqrt{\left(\frac{2C_g\beta^2}{Q_o \exp\left(\frac{V_{sce}}{\beta}\right)}\right)^2 + 4\beta^2 \log^2\left[1+\exp\left[\frac{V_{gs}-V_o-V}{2\beta}\right]\right]} \right) \qquad (3.3)$$

where $V_o = \Delta\phi - \beta \log\left(\frac{qn_iT_{si}}{2Q_o}\right)$ (3.4)

where $\Delta\phi$ is the work-function difference between the gate electrode and the intrinsic silicon, n_i being the intrinsic concentration. In (3.1), the term ΔV_{th} ensures the correct behavior of Q above threshold [17]

$$\Delta V_{th} = \frac{\left(\frac{C_g\beta^2}{Q_o}\right)Q^{'}}{Q_o + \frac{Q^{'}}{2}} \qquad (3.5)$$

where $C_g = \frac{C_{ox}}{\left(1+\frac{C_{ox}y_I}{\varepsilon_{si}}\right)}$ is the effective oxide capacitance, and

$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$ is the gate-oxide capacitance and ε_{ox} is the permittivity of oxide.

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The inversion centroid is a function of the inversion charge. A simple relationship between inversion centroid and inversion charge obtained by fitting numerical simulation results is given by $\frac{1}{y_I}=\frac{1}{a+bT_{si}}+\frac{1}{y_{IO}}\left(\frac{N_I}{N_{IO}}\right)^n$ with $a=0.35$ nm, $b=0.26$, $y_{IO}=6$ nm, $N_{IO}=7\times10^{12}$ cm^{-2} and $n=0.8$ [5].

3.2.2 Velocity overshoot

In extremely short channel DG MOSFET the transport regime is quasi-ballistic, thus an important overshoot velocity is expected. Using a simplified energy-balance model, the electron mobility is a function of the electron temperature related to the average energy of the carriers. The electron temperature T_e is governed by the following equation [7]:

$$\frac{dT_e}{dx}+\frac{T_e-T_O}{\lambda_w}=-\frac{q}{2k}E_x\left(x\right) \tag{3.6}$$

where the energy-relaxation length is defined as $\lambda_w\approx 2v_{sat}\tau_w$, τ_w being the energy relaxation time constant, v_{sat} the saturation velocity and $E_x\left(x\right)$ is the lateral electric field.

The electron velocity in the channel increases as they travel from source to drain. However, for a given bias, the velocity can

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saturate. Assuming this, we can divide the channel into two sections: the first section $0 \langle x \langle L_e = L - L_{sat}$, and the saturation region $x \rangle L_e$. In contrast with classical drift-diffusion models, the saturated velocity in the saturation region due to non-stationary effects can achieve higher values than v_{sat} . This phenomenon is known as velocity overshoot [7]

. In the linear region, the carrier velocity can be obtained from the mobility as

$$v(x) = \mu_n(x) E_x(x) = \frac{\mu_{eff}}{1 + \alpha\left[T_e(x) - T_0\right]} E_x(x) \qquad (3.7)$$

where the value of α is determined from (3.6) under static conditions,

where $\frac{dT_e}{dx} = 0$: $\alpha = \frac{2k\mu_{eff}}{q\lambda_w v_{sat}}$

The energy balance model gives higher currents when compared with the drift-diffusion model, due to the electron velocity overshoot within the channel. With the modified mobility expression which allows the carrier velocity to exceed the saturation velocity if the channel length becomes comparable with the energy-relaxation length. Thus, the energy relaxation length λ_w inherits the velocity overshoot within its expression.

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3.2.3 Channel Length Modulation (CLM)

In order to model the channel length modulation, we need to solve the 2D Poisson`s equation in the saturation region [14].

For $V_{ds} \langle V_{dssat}$, the device works in the linear region. For $V_{ds} \rangle V_{dssat}$, the channel is partially saturated, and the saturated channel length is given by

$$\Delta L = L_c \arcsin h\left(\frac{V_{ds} - V_{dssat}}{E_{sat} L_c}\right) \tag{3.8}$$

where E_{sat} is the saturation field when velocity reaches saturation.

One of the most used expressions for the saturation potential [18] has been corrected as

$$V_{dssat} = \left(-\frac{Q_{seff}}{2C_g}\right)\left(\frac{v_{sat}}{\left(\frac{-Q_{seff}\mu_{eff}}{4LC_g}\right) + v_{sat}}\right) \tag{3.9}$$

with $Q_{seff} = Q_s + 4\frac{kT}{q}C_g\left(\frac{v_{sat}}{v_{sat} - \frac{kT}{q}\left(\frac{\mu_{eff}}{L}\right)}\right)$ (3.10)

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Thus, Q_{seff} tends to Q_s in strong inversion and to a value that gives the correct V_{dssat} in weak inversion.

A smoothing function is used to interpolate V_{dss} :

$$V_{dss} = V_{ds} - \frac{kT}{q} \frac{\ln\left\{1 + \exp\left[A\left(V_{ds} - V_{dssat}\right) / \left(kT/q\right)\right]\right\}}{A} \tag{3.11}$$

where A is the parameter that controls the transition between saturated and nonsaturated channels.

The saturation characteristic length is given as $L_c = a\sqrt{\frac{\varepsilon_{si} t_{ox} T_{si}}{2\varepsilon_{ox}} + \frac{T_{si}^{\ 2}}{8}}$. It can be seen that the saturation characteristic length depends only on the device structure and a is a fitting parameter $\left(0 < a \le 1\right)$.

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3.2.4 DIBL Effect

The DIBL effect can be modelled by solving the 2D Poisson's equation in a similar way as for the channel-length modulation [14]

The potential φ at the ends of the channel (source and drain) is

$\varphi(x=0)=\varphi(\varphi_c=V_{dss}+V_{bi})=\varphi_d$ at the drain

$\varphi(x=-L)=\varphi(\varphi_c=0+V_{bi})=\varphi_s$ at the source

where V_{bi} is the source and drain junction built-in voltage. The value of the built-in voltage is difficult to calculate in DG MOSFET because the silicon film is floating. Hence, it can be considered as fitting parameter.

$$\varphi=\varphi_c-V_{gs}+V_{fb}-\left(1+\frac{C_g}{2C_{si}}\left(1-\frac{1}{n}\right)\right)\left(\left(\frac{Q_s+Q_d}{2}\right)\right)\left(\frac{1}{2C_g}\right) \tag{3.12}$$

where V_{fb} is the flatband voltage, Q_s and Q_d are the mobile charges at the source and drain, respectively. If $n=1$, we have a flat profile whereas if $n=2$, we have a parabolic profile.

Hence the $V_{sce}=2\sqrt{\varphi_s\varphi_d}\exp\left(\frac{-L}{2L_c}\right)$ (3.13)

This quantity, which is equal to zero for long-channel devices [19], can be considered as the barrier potential drop due to the DIBL effect. It is then introduced into the calculation of the charge Q in (3.1)-(3.5).

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3.2.5 Drain Current

Using the charge control models in (3.1) and the velocity expression in (3.7), the expression of the drain-current in a DG MOSFET is calculated as a function of the mobile-charge densities at the source Q_s and at the drain Q_d [14]

$$I_{DS} = \frac{W\mu_{eff}}{L_e(1+\gamma_n V_{dss})}\left[2\frac{kT}{q}(Q_s - Q_d) + \frac{Q_s^2 - Q_d^2}{4C_g} + 8\left(\frac{kT}{q}\right)^2 C_{si}\log\left[\frac{Q_d + 2Q_o}{Q_s + 2Q_o}\right]\right] \quad (3.14)$$

We define the effective mobility as [4]

$$\mu_{eff} = \frac{\mu_o}{1+\theta_1\beta\log(1+\exp(1+(V_{gs}-V_o)/\beta) + \theta_2\beta^2\log(1+\exp(1+(V_{gs}-V_o)/\beta)^2} \quad (3.15)$$

where μ_o is the low-field mobility, and θ_1 and θ_2 are the mobility attenuation coefficients of the first and second orders, respectively, which can be considered as fitting parameters, $\gamma_n = \frac{\mu_{eff}}{v_{sat}L}\left(\frac{1}{1+2\lambda_w/L}\right)$, V_{dss} is equal to V_{ds} for nonsaturated channel and $V_{dss} = V_{dssat}$ for saturated channel, and $L_e = L - \Delta L$ and W are the device effective length and width respectively.

The final compact model for the drain-current includes mobility degradation, short-channel effects (SCE), and channel length modulation (CLM). Velocity overshoot is also taken into account through a hydrodynamic transport approach.

3.2.6 Quantum Mechanical Effects

Quantum Mechanical Effects (QME) plays a significant role in devices in ultrathin body [5] modifying the electrical behavior in both weak and strong inversion regions. We consider that the first quantum sub-band is mainly responsible for the threshold voltage shift, and the other sub-bands are considered as a geometrical dependent correction. The threshold voltage shift is also due to the reduction of oxide capacitance due to the inversion-layer centroid change. In order to accurately model QMEs in all operating regions, we propose an efficient semiempirical approach valid for all ultrathin body given by [20]

$$\Delta E_{qm} = \frac{\hbar^2}{2m_{eff}\beta}\left(\frac{\pi}{T_{si}}\right)^2 . \left[1 + g\left(T_{si}, V_{gs}\right)\right] \tag{3.16}$$

with

$$g\left(T_{si}, V_{gs}\right) = \alpha_{qm1} + \alpha_{qm2} \cdot \frac{1}{2}\left[\left(V_{gs} - V_{fb} - V_O\right) + \sqrt{\left(V_{gs} - V_{fb} - V_O\right)^2}\right] + \alpha_{qm3} \cdot \frac{1}{2}\left[\left(V_{gs} - V_{fb} - V_O\right)^2 + \left(V_{gs} - V_{fb} - V_O\right) . \sqrt{\left(V_{gs} - V_{fb} - V_O\right)^2}\right] \tag{3.17}$$

and

$$\alpha_{qm1} = -0.83 + 0.033 \times T_{si}$$

$$\alpha_{qm2} = -0.011 + 0.0029 \times T_{si} + 0.000215 \times T_{si}^{\ 2}$$

$$\alpha_{qm3} = 0.00035 - 0.00017 \times T_{si} + 0.000046 \times T_{si}^{\ 2}$$

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where $\hbar$ is the reduced Planck constant, m_{eff} is the electron effective mass, and T_{si} is in nanometers.

Finally, the quantum effects are included in the model as a change in the threshold voltage.

$$V_{O_qm} = V_O + \frac{\Delta E_{qm}}{e} \qquad (3.18)$$

where e is the electronic charge.

The correction term is added to the V_O term as shown in (3.18). Thus, the correction makes a positive shift in the threshold voltage of the device (we are considering n-channel devices).

3.3 Simulated Devices

Two different DGSOI transistors have been considered for this study. The first one is an idealized 22 nm channel length device, Figure 3.1 (top) having a gate stack of 2.4nm of HfO_2 on top of 0.7nm of SiO_2 (EOT=1.1nm) and a silicon film thickness (T_{si}) of 10nm. The second one is an idealized 16 nm channel length device, Figure 3.1 (bottom) has a gate stack of 4.7nm of HfO_2 (EOT=0.8nm) and a silicon film thickness (T_{si}) of 8nm. The channels are lowly doped (10^{15} cm^{-3}) in both the devices.

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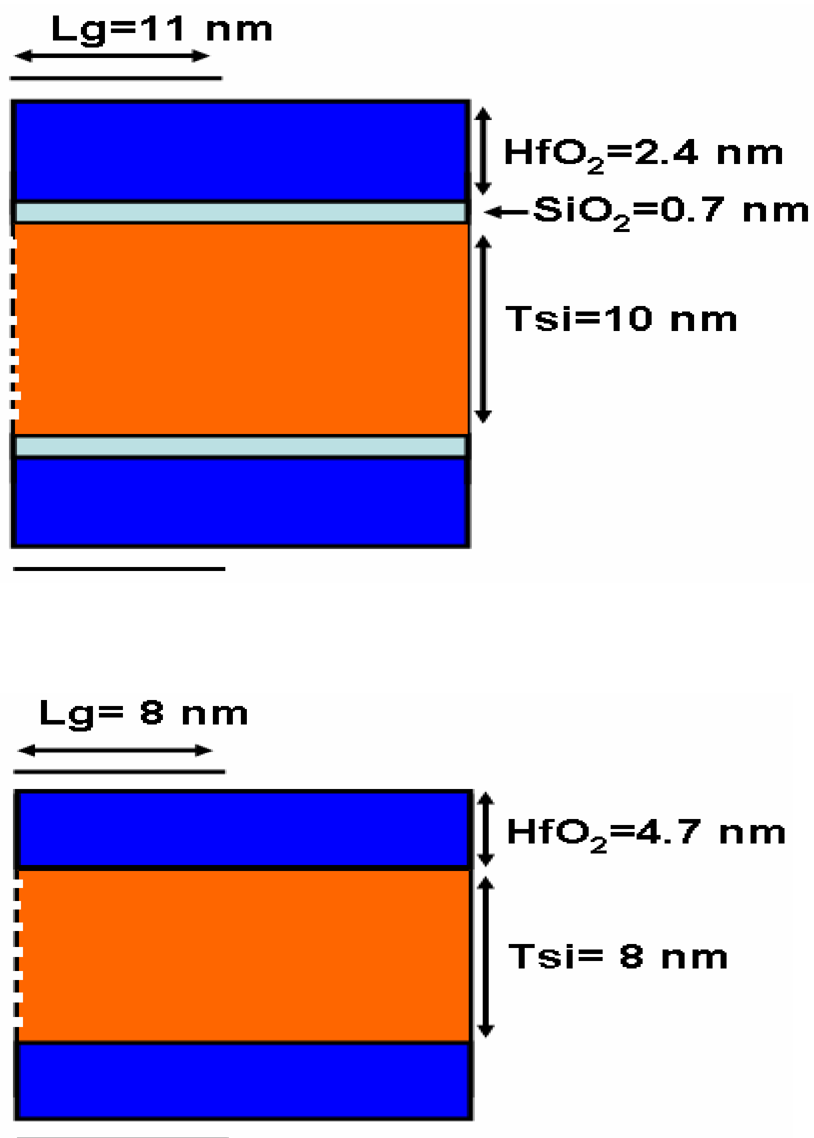

Figure 3.1 Show the half structures of the 22 nm (top) and 16 nm (bottom) LSTP DG-MOSFET template used in this work. All the dimensions are in nm.

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3.4 Simulated Approaches

The key features of each model (identified with the acronym of the main developer) are presented. The possible modeling approaches can be grouped in a few families which range from modifications of the conventional drift-diffusion (DD) model used in commercial TCAD tools to advanced Monte Carlo (MC) models. In the DD family, the model gathers drift-diffusion like models where only the first momentum of the Boltzmann-Transport-Equation (BTE) is calculated. The MC family collects models based on the direct solution of the BTE using Monte Carlo method [21]. The MC model incorporates all relevant scattering mechanisms such as ionized impurities (II), surface roughness (SR), phonon scattering, etc. Also, different simulation approaches have been implemented such as full-band, semi-classical, multi-subband ensemble Monte Carlo simulators. The numerical models used by the different groups [1-2], [22-28] differ in terms of scattering models, simulation approaches, etc. For comparison, all simulators have been first calibrated to reproduce the universal mobility curves as in bulk silicon devices [2].

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3.4.1 DD family

3.4.1a BO-DD (Univ.of Bologna)

1D drift-diffusion solver for SOI-MOSFETs combined with the solution of the coupled Schrödinger-Poisson equations on the device cross-section normal to the transport direction [22]. The mobility model [23] is also used in the DD solver.

3.4.2 MC family

3.4.2a BO-MC (Univ.of Bologna)

The full-band Monte-Carlo simulator treats electrons as a free carrier gas and introduces quantum corrections through the effective potential [24]. Scattering mechanisms include phonons, SR, II in the source/drain.

3.4.2b UD (Univ. of Udine)

Multi-Subband Ensemble Monte Carlo (MSMC) simulator as described in [25]. A first order approach to include quantum effects in the transport direction has been implemented. Scattering mechanisms such as SR and phonons are also included [2].

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3.4.2c UPS (Univ. of Paris-Sud)

Ensemble Monte Carlo simulator as described in [26]. Quantum corrections are not taken into account here and carriers are treated as a three-dimensional (free) gas in the simulator. All relevant scattering mechanisms are included.

3.4.2d SNPS (Synopsis Switzerland LLC)

Self-consistent semiclassical full-band Monte Carlo device simulator as described in [27]. Self-consistency is obtained by iterating single-particle simulations with solutions of the nonlinear Poisson equation until convergence. The scattering mechanisms comprise phonon, impurity and SR scattering.

3.4.2e UGR (Univ. of Granada)

Multi-Subband Ensemble Monte Carlo simulator described in [1]. This method is based on the mode-space approach for quantum transport. All relevant scattering mechanisms are included.

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3.5 Results and Discussion

The results of the compact model have been compared with the numerical simulation data obtained by several research groups using advanced transport models [1-2], [21-28]. Figure 3.2 shows the transfer characteristics of the 22 nm DG MOSFETs at low and high V_{DS}. A good agreement between the compact model and the numerical simulations [1-2] is obtained by considering the low field mobility and for a fitted saturation velocity.

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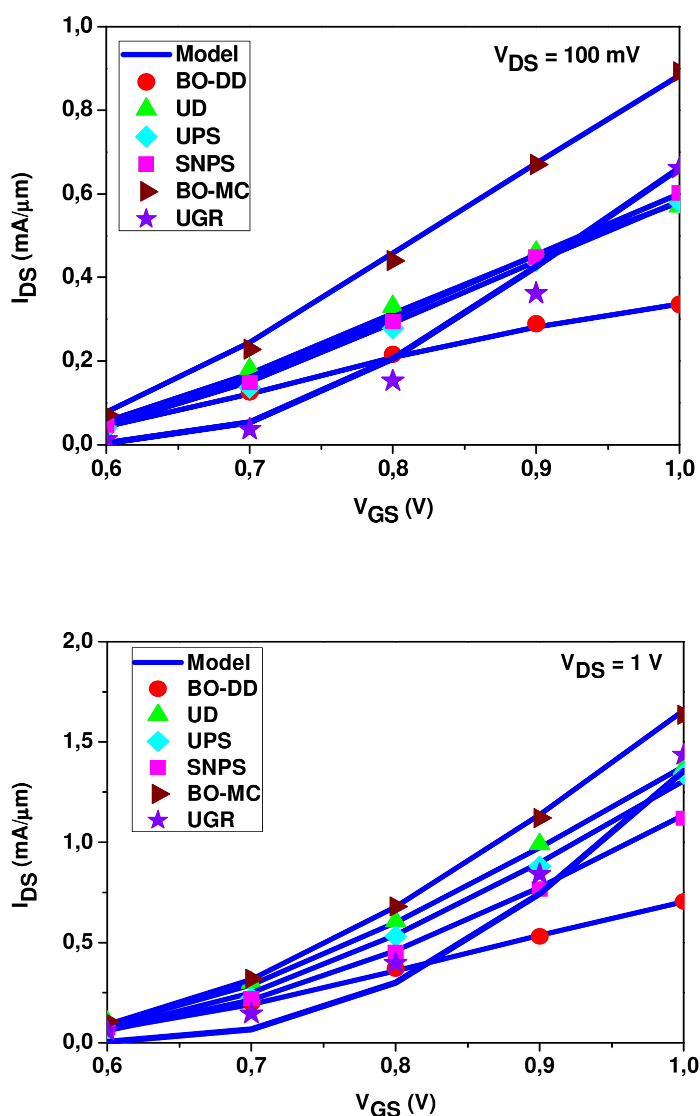

Figure 3.2: Transfer characteristics of 22 nm DG MOSFETs for low (top) and high (bottom) V_{DS}. 2D numerical simulation data by Univ.of Bologna (BO-DD) [2], Univ.of Udine (UD) [2], Univ.of Paris-Sud (UPS) [2], Synopsys (SNPS) [2], Univ.of Bologna (BO-MC) [2], Univ.of Granada (UGR) [1]

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Figure 3.3 shows the transfer characteristics of the 16 nm DG MOSFETs at low and high V_{DS}. A good agreement is obtained between the compact model and the numerical simulations [1-2]. In the transfer characteristics it can be clearly noted that the mobility degradation at low drain voltages is significantly reproduced by the compact model. As expected the drain current values provided by the drift-diffusion model (BO-DD) are lower than the other numerical models for both 22 nm and 16 nm devices.

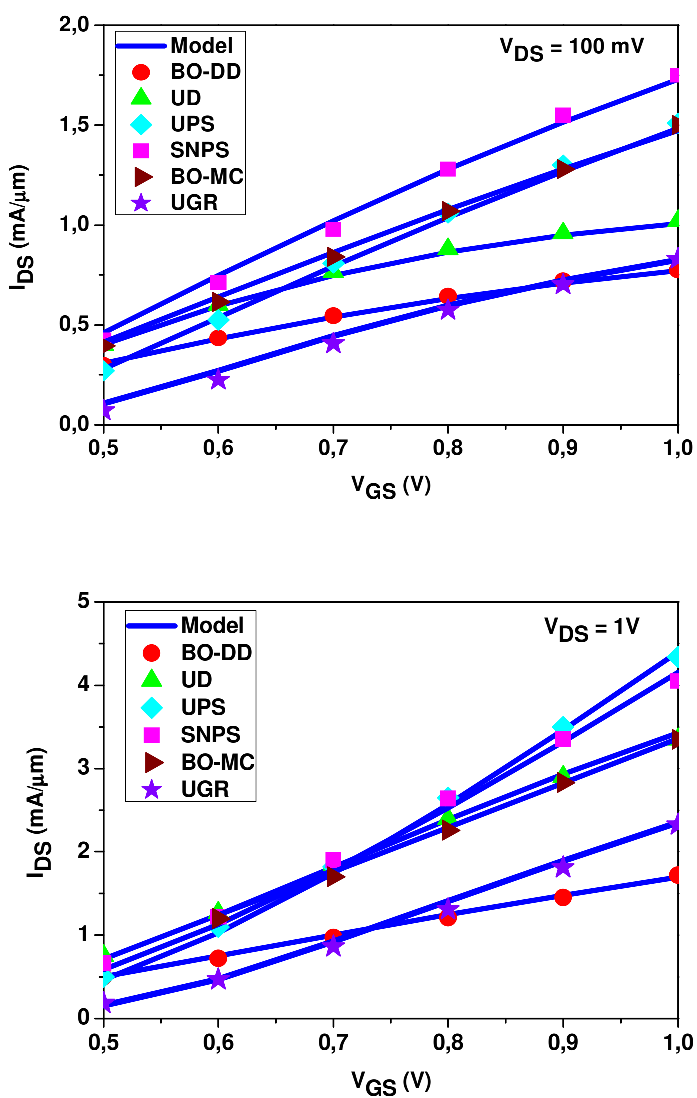

Figure 3.3: Transfer characteristics of 16 nm DG MOSFETs for low (top) and high (bottom) V_{DS}. 2D numerical simulation data by Univ.of Bologna (BO-DD) [2], Univ.of Udine (UD) [2], Univ.of Paris-Sud (UPS) [2], Synopsys (SNPS) [2], Univ.of Bologna (BO-MC) [2], Univ.of Granada (UGR) [1]

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Figure 3.4 shows the output characteristics of the 22 nm and 16 nm DG MOSFETs. A good agreement between the compact model and the numerical simulations [1] is seen. It can be observed that for the model without velocity overshoot and quantum effects a good agreement is obtained at low drain bias, and becomes worse at high drain bias. If the quantum effects are not included in the model, the current is significantly higher than the simulations. If the hydrodynamic transport is not considered the model gives a much lower current than the simulations. Hence, it can be inferred that all these effects should be considered to accurately reproduce results from advanced transport models.

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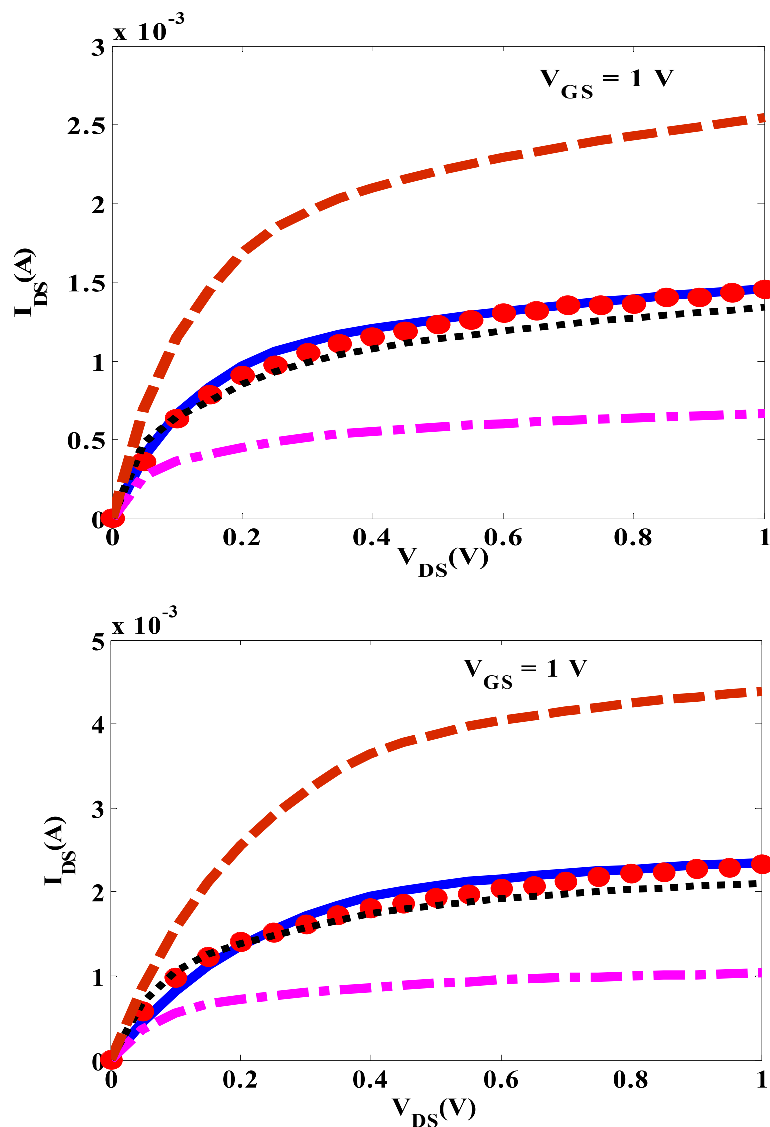

Figure 3.4: Output characteristics of 22 nm (top) and 16 nm (bottom) DG-MOSFET for V_{GS}=1V Dashed line: Without quantum effects, Solid line: Compact model, Dotted line: Without velocity overshoot and quantum effects, Dash-dotted line: Without hydrodynamic transport, Symbol: Simulation (UGR-MSB-EMC) [1].

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Table 3.1 indicates the mobility degradation and velocity saturation parameters considered in the model. From the table parameters it can be seen that strong mobility degradation is observed with the drift-diffusion model for both devices. It can be seen that low mobility degradation is observed with the UPS simulations for both the devices. The number of fitting parameters used in the compact model is not big (8). The fitting parameters are: μ_o, θ_1, θ_2, v_{sat}, a (which controls the characteristic length), V_{fb}, V_{bi}, A (controls the transition from V_{ds} to V_{dssat}).

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Models	**DG MOSFET 22nm T_{si}=10nmEOT=1.1nmdevice parameters**			**DG MOSFET 16nm T_{si}= 8nm EOT=0.8nm device parameters**		
	v_{sat} x 10^7 (cm-sec^{-1})	**θ_1(V^{-1})**	**θ_2(V^{-2})**	**v_{sat} x 10^7 (cm-sec^{-1})**	**θ_1(V^{-1})**	**θ_2(V^{-2})**
BO-DD	**1.1**	**0.8**	**1.93**	**0.9**	**0.3**	**1.16**
UD	**1.02**	**0.1**	**0.58**	**0.92**	**0.3**	**1.31**
UPS	**0.9**	**0.14**	**0.039**	**0.9**	**0.19**	**0.19**
SNPS	**0.9**	**0.14**	**0.039**	**0.8**	**0.01**	**0.39**
BO-MC	**1.01**	**0.1**	**0.039**	**0.8**	**0.35**	**0.19**
MSB-EMC (UGR)	**0.8**	**0.01**	**0.05**	**0.7**	**0.35**	**0.9**

Table 3.1 Parameters used in the proposed analytical model in order to fit the simulations obtained using different transport models.

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The effective mobility with temperature dependency is

$$\mu_{eff} = \frac{\mu_o \left(\frac{T}{300} \right)^{-\gamma}}{1+\theta_1 \beta \log(1+\exp(1+\left(V_{gs}-V_o\right)/\beta)+\theta_2 \beta^2 \log(1+\exp(1+\left(V_{gs}-V_o\right)/\beta)^2}$$

Figures 3.5, 3.6, 3.7, 3.8, 3.9 shows the transfer and output characteristics of the 22 nm DG MOSFETs for low and high V_{DS} at temperature = 27º C, 50º C, 75º C, 100º C and 125º C respectively. A good agreement between the compact model and the 2D numerical simulations [1] is obtained by considering the low field mobility and for a fitted saturation velocity and the parameter γ. It can be seen that for the output characteristics curves at T = 75º C, 100º C and 125º C, the model values are slightly lower than the 2D numerical simulations [1] in the transition regime which can be seen in the curves.

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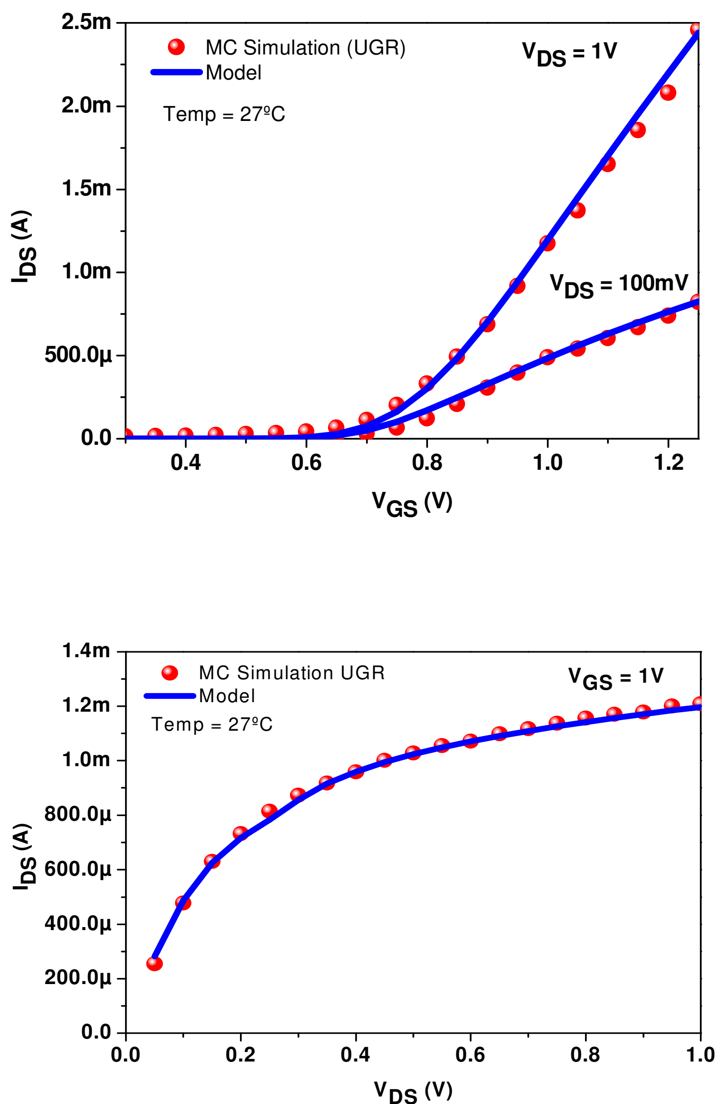

Figure 3.5 Transfer (top) characteristics of 22 nm DG MOSFETs for low and high V_{DS} and output (bottom) characteristics of 22 nm DG MOSFETs for high V_{GS} at temperature = 27ºC. 2D numerical simulation data by Univ.of Granada (UGR)[1]

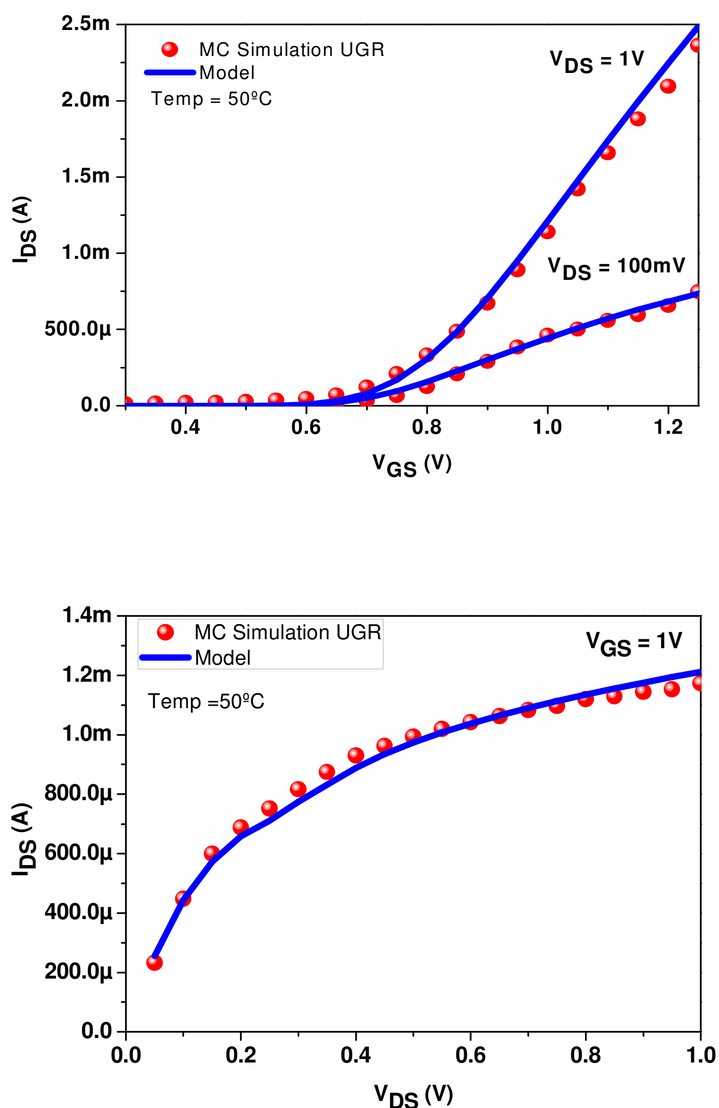

Figure 3.6 Transfer (top) characteristics of 22 nm DG MOSFETs for low and high V_{DS} and output (bottom) characteristics of 22 nm DG MOSFETs for high V_{GS} at temperature = 50ºC. 2D numerical simulation data by Univ.of Granada (UGR) [1]

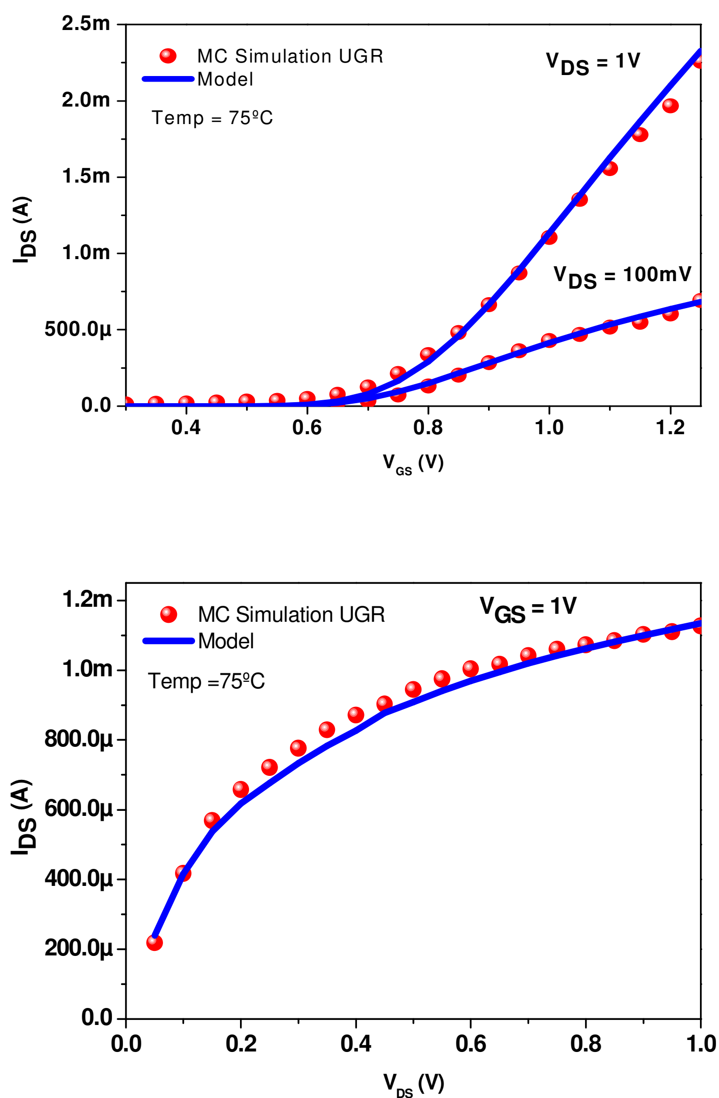

Figure 3.7 Transfer (top) characteristics of 22 nm DG MOSFETs for low and high V_{DS} and output (bottom) characteristics of 22 nm DG MOSFETs for high V_{GS} at temperature = 75ºC. 2D numerical simulation data by Univ.of Granada (UGR) [1]

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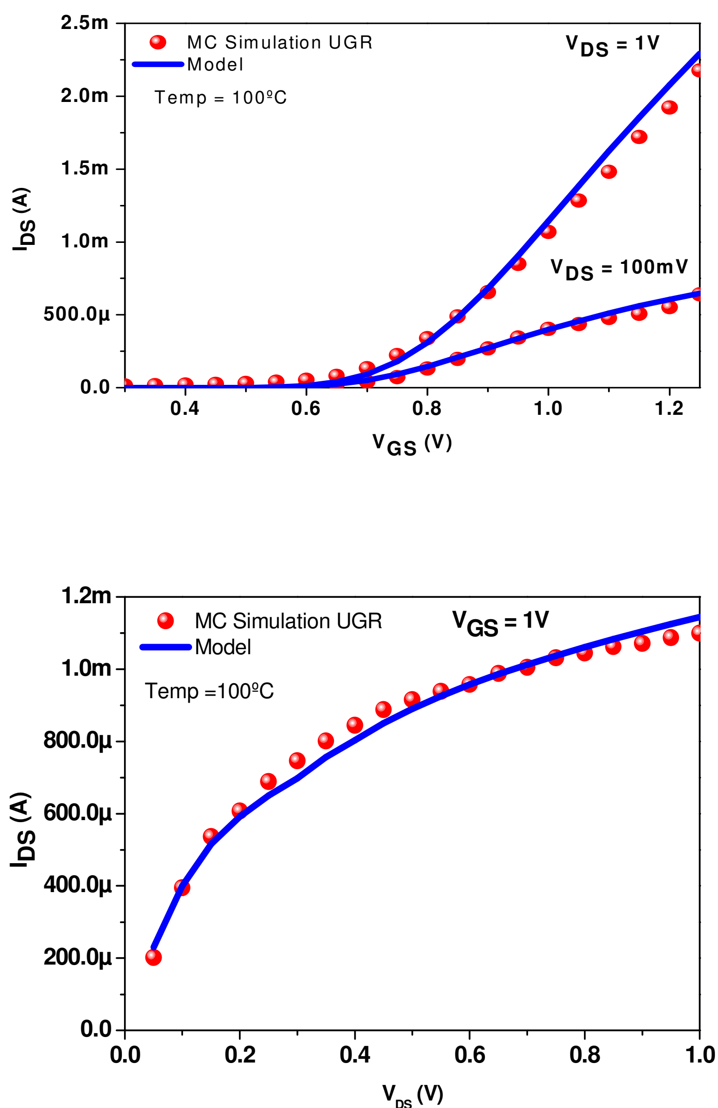

Figure 3.8 Transfer (top) characteristics of 22 nm DG MOSFETs for low and high V_{DS} and output (bottom) characteristics of 22 nm DG MOSFETs for high V_{GS} at temperature = 100ºC. 2D numerical simulation data by Univ.of Granada (UGR) [1]

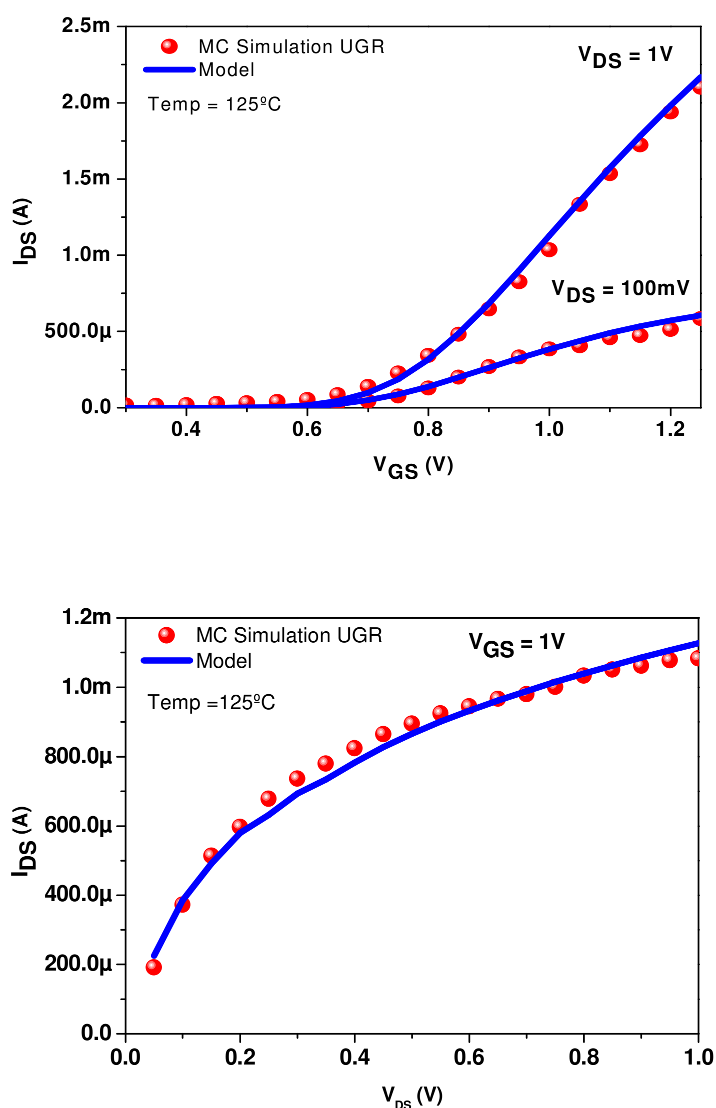

Figure 3.9 Transfer (top) characteristics of 22 nm DG MOSFETs for low and high V_{DS} and output (bottom) characteristics of 22 nm DG MOSFETs for high V_{GS} at temperature = 125ºC. 2D numerical simulation data by Univ.of Granada (UGR) [1]

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Table 3.2 indicates the mobility degradation and velocity saturation parameters considered in the model. From the table parameters it can be seen that stronger mobility degradation is observed as temperature increases.

Temperature (° C)	**DG MOSFET 22nm T_{si}=10nm EOT=1.1nm device parameters**			
	γ	v_{sat} **x 10^7 (cm-sec^{-1})**	θ_1**(V^{-1})**	θ_2**(V^{-2})**
27	**0.6**	**0.8**	**0.01**	**0.5**
50	**0.6**	**0.8**	**0.01**	**0.6**
75	**0.6**	**0.78**	**0.01**	**0.7**
100	**0.6**	**0.75**	**0.01**	**0.8**
125	**0.6**	**0.7**	**0.03**	**1.15**

Table 3.2 Parameters used in the proposed analytical model in order to fit the simulations obtained for the different temperature range.

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3.6 Conclusions

In this chapter we have extended a compact model for the drain current in DG-MOS transistors. Hydrodynamic transport model has been included in a way that can reproduce 2D simulation results of the advanced transport modeling methods. The model is valid and continuous in all operating regimes. Mobility degradation, velocity saturation, short-channel effects and quantum mechanical effects are included. The model includes the temperature dependency. The model shows a very good agreement with the 2D numerical simulation results obtained using different transport models for the practical range of voltages considered.

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Chapter 4

Nanoscale Multi-gate CMOS circuits simulation using compact models

This chapter is aimed at implementing the compact advanced transport models developed for multi-gate MOSFETs in circuit simulator.

The chapter is divided into two sections as follows:

In section 4A, the results of the implementation of a nanoscale double-gate (DG) MOSFET compact model, which includes hydrodynamic transport model, in Verilog-A in order to carry out circuit simulation are presented. The model is used with SMASH circuit simulator for the analysis of the DC and transient behaviour electrical CMOS circuits. A DG CMOS inverter circuit and a five stage ring oscillator circuit have been analysed.

In section 4B, compact model of a nanoscale cylindrical surrounding-gate (SRG) MOSFETs which includes hydrodynamic transport model, in Verilog-A implemented in circuit simulation are presented.

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4A. Implementation of nanoscale double-gate (DG) CMOS circuits using compact advanced transport models

4A.1. Introduction

The device-scaling concept has been the main guiding principle of the MOS-device engineering over the past few decades [1]. As the conventional bulk MOSFET technology is scaling down towards the practical limit, DG MOSFETs appeared as a promising technological alternative that has attracted substantial research interests due to superior short channel control, volume inversion, etc. There has been work dedicated to modeling and simulation of DG MOSFETs. Compact core models for undoped and doped symmetric DG MOSFETs have been presented [2-6]. The development of models to simulate circuits containing new devices is an important task to allow the introduction of these devices in practical applications. Accurate and time computationally efficient compact models of DG MOSFETs are required to predict or simulate circuit performance. For a circuit

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simulation the main task is to count with a precise transistor model to reproduce the transistor behavior, which is either already introduced or can be implemented in the commercial circuit simulators to be used. In recent years, some work has been done on the implementation of DG MOSFET compact models in circuit simulators [7-10].

In this section, we present the implementation of a DG MOSFET compact model including hydrodynamic transport model in Verilog-A for circuit simulators. The model is based on an analytical expression that models the variation of surface potential as well as the difference of potential at the surface and at the middle of the silicon layer [2]. This model for the potentials is used in an analytical compact model for the drain current of a double-gate MOSFETs derived from a core charge control model which results from the solution of the 1D Poisson's equation [3]. Electrostatic short-channel effects (threshold voltage roll-off, DIBL, subthreshold swing degradation) were introduced in the core model using scalable and geometry dependent equations. This model is valid from

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lightly doped to highly doped devices [3]. We have extended this model to include hydrodynamic transport model [11]. Besides, charge and capacitance models consistent with the DC model were developed. In [11] we validated this model for n-channel DG MOSFETs by comparison with numerical simulations obtained using advanced transport models. In this section, first of all, we extend this model to p-channel devices and we validate it by comparison with numerical simulations based on advanced transport models. The entire models for n-channel and p-channel devices is implemented in Verilog-A, which allows the use of the model in commercial circuit simulators for circuit design of both digital and analog applications. We have shown an example of DG MOSFET based CMOS inverter circuit. Finally, we compare results between drift-diffusion and hydrodynamic transport models within the practical range of voltages.

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4A.2. Device and Approaches

The 22 nm template transistor we considered is shown in Figure 4A.1. The 22 nm DG MOSFET with a gate length of 22 nm, a gate stack consisting of 2.4 nm of HfO_2 on top of 0.7 nm of SiO_2 (EOT = 1.1 nm). The silicon film thickness is 10 nm. The channel is undoped (10^{15} cm^{-3}). We have considered both n-channel and p-channel DG MOSFETs with these dimensions.

The main features of each transport models (represented with the acronym of the main developer) are presented. The modeling approaches can range from modifications of the conventional drift-diffusion (DD) model used in commercial TCAD tools to advanced Monte Carlo (MC) models. The numerical models used by the different groups [12-21] differ in terms of scattering models, simulation approaches, etc. For comparison, all simulators have been first calibrated to reproduce the characteristics curves as in silicon devices.

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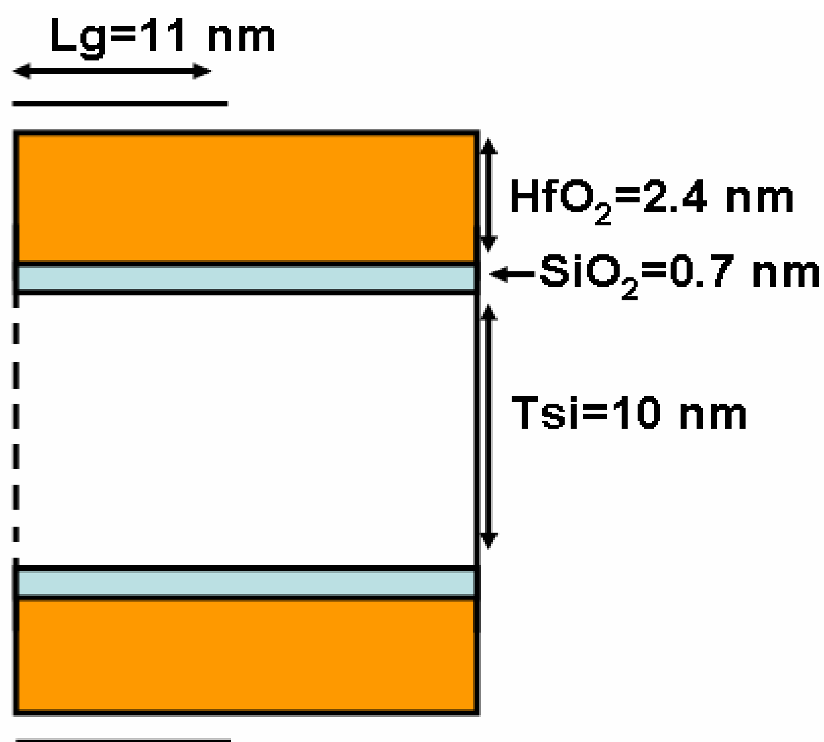

Figure 4A.1 Structure of the 22 nm template DG MOSFET considered in the work. One half of the symmetric structure is shown. All dimensions are in nm.

4A.2.1 BO-DD (Univ.of Bologna)

1D drift-diffusion (DD) solver for SOI-MOSFETs combined with the solution of the coupled Schrödinger-Poisson equations on the device cross-section normal to the transport direction [12]. The mobility model [13] is also used in the DD solver.

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4A.2.2 UD (Univ. Of Udine)

Multi-Subband Ensemble Monte Carlo (MSMC) simulator as described in [14-15]. A first order approach to include quantum effects in the transport direction has been implemented. Scattering mechanisms such as SR and phonons are also included [16].

4A.2.3 SNPS (Synopsis Switzerland LLC)

Self-consistent semiclassical full-band Monte Carlo device simulator as described in [17]. Self-consistency is obtained by iterating single-particle simulations with solutions of the nonlinear Poisson equation until convergence. The scattering mechanisms comprise phonon, impurity and SR scattering.

4A.2.4 TUBS (Tech. Univ. Braunschweig)

Self-consistent solution of 6x6 k.p SE, PE and multisubband BTE as described in [18-19]. Scattering due to phonons and surface roughness are also included [20-21].

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4A.3. DG MOSFET model

Our model presented in [10] for n-channel devices has been shown to reproduce 2D advanced transport simulations of nanoscale n-channel devices by means of the hydrodynamic transport formulation explained in [11]. Here, we extend it to p-channel devices. The potentials at the surface φ_s and in the center φ_o of the silicon layer can be calculated analytically as shown in [2]. The surface potentials in the subthreshold φ_{sBT} and in the above threshold φ_{sAT} regimes are calculated analytically using the Lambert function. Finally, the overall surface potential in all regions can be calculated as [10]:

$$\varphi_s = \varphi_{sBT}\frac{1}{2}\left\{1-\tanh\left[\pm 10\left(V_{gs}-V_T-V_{ch}\right)\right]\right\} + \varphi_{sAT}\frac{1}{2}\left\{1+\tanh\left[\pm 10\left(V_{gs}-V_T-V_{ch}\right)\right]\right\} \quad (4A.1)$$

where '+' for n-channel, '-' for p-channel, V_{gs} is the applied gate voltage, V_T is the threshold voltage and V_{ch} is the channel voltage. The Lambert function is represented in Verilog-A language as a built-in function conserving the requirements of a compact model. This analytical surface potential calculation gives the possibility of writing charge carrier calculation at source, q_s, and at the drain q_d as explicit functions of the applied voltages.

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The drain current in a p-channel DG MOSFET is calculated as a function of the mobile charge densities at the source q_s and at the drain q_d as (q_s and q_d are in absolute value) [10], assuming a drift-diffusion transport:

$$I_{DS} = \pm 2 \frac{W C_{ox} \phi_t^2 \mu_s}{L} \left[2(q_s - q_d) + \frac{q_s^2 - q_d^2}{2} + q_{dep} \ln \left[\frac{q_d + q_{dep}}{q_s + q_{dep}} \right] \right] \tag{4A.2}$$

where W and L are width and length of the device respectively. C_{ox} is the gate capacitance; Φ_t is the thermal voltage, $q_{dep}=qN_a t_{si}/C_{ox}\Phi_t$ is the normalized fixed charge concentration in the silicon layer of thickness t_{si}, q the electron charge, N_a is the doping concentration; μ_s is the surface mobility. The expression for the drain current in (4A.2) is used as the core model for DG MOSFET. In the complete model, the effects of velocity saturation, channel length modulation, threshold voltage roll-off, DIBL and subthreshold swing degradation are all included.

In extremely short channel devices, the transport regime is quasi-ballistic; thus, an important overshoot velocity is expected. The velocity overshoot is included in the model using a one dimensional energy-balance model [11]. The velocity overshoot is modeled assuming a hydrodynamic transport model which is included in the core drain current model. The final drain current expression accounting for the hydrodynamic transport model is given as:

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$$I_{DS} = \pm 2\frac{WC_{ox}\phi_t^2\mu_s}{L(1+\gamma_n V_{dss})}\left[2(q_s - q_d) + \frac{q_s^2 - q_d^2}{2} + q_{dep}\ln\left[\frac{q_d + q_{dep}}{q_s + q_{dep}}\right]\right] \tag{4A.3}$$

where, $\gamma_n = \frac{\mu_{eff}}{v_{sat}L}\left(\frac{1}{1+2\lambda_w/L}\right)$ takes into account both the velocity saturation effect and the hydrodynamic transport [11], through which the velocity overshoot is also modelled, $\lambda_w \approx 2v_{sat}\tau_w$ being the energy relaxation length, τ_w the energy relaxation time constant, v_{sat} the saturation velocity and V_{dss} is the effective drain-source voltage. The charge and capacitances expression are developed following the procedure presented in [6] for undoped devices, but considering the doping in the charge control model.

The results of the compact model for p-channel have been validated. Here we show the comparisons between the numerical simulation data obtained by several research groups using advanced transport models [12-21]. Figure 4A.2 shows the transfer characteristics of the 22 nm DG p-channel MOSFETs at low and high V_{DS}. A good agreement between the compact model and the numerical simulations [12-21] is obtained by considering the low field mobility and for a fitted saturation velocity.

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Table 4A.1 indicates the low field mobility, velocity saturation and mobility degradation parameters considered in the model. From the table parameters it can be seen that strong mobility degradation is observed with the drift-diffusion model. It can be seen that low mobility degradation is observed with the SNPS simulations.

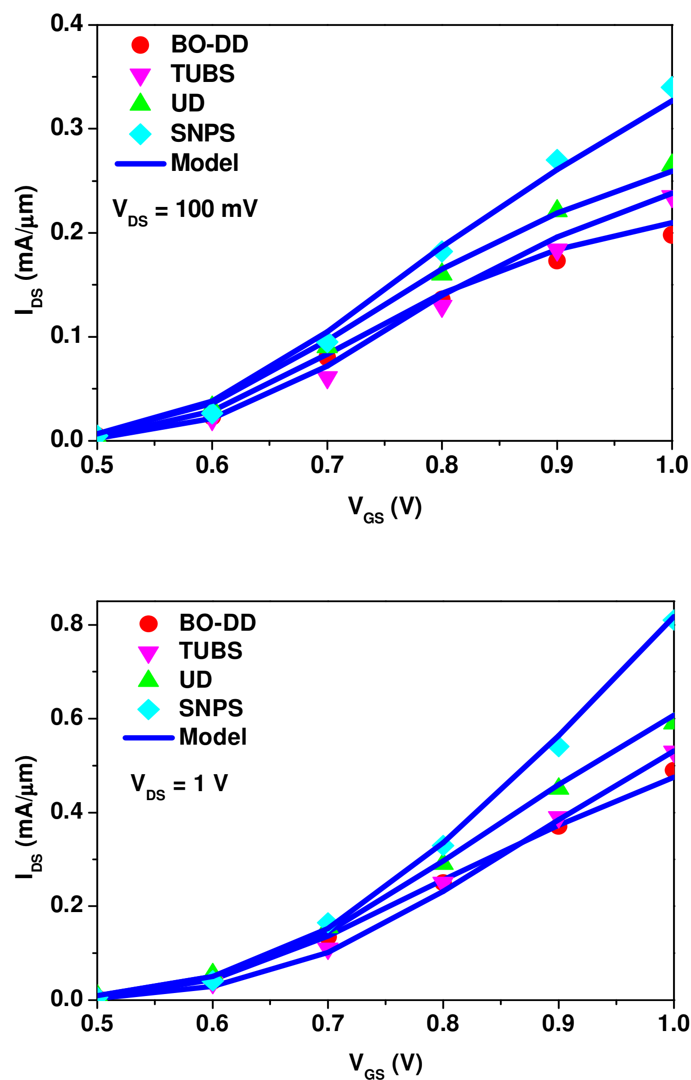

Figure 4A.2: Transfer characteristics of 22 nm DG p-channel MOSFETs for low (top) and high (bottom) V_{DS}. 2D numerical simulation data by Univ.of Bologna (BO-DD) [12-13], Tech. Univ. Braunschweig (TUBS) [18-21], Univ.of Udine (UD) [14-16], Synopsys (SNPS) [17].

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Models	22 nm DG p-channel MOSFET Tsi = 10 nm EOT = 1.1 nm			
	μ_0 (cm^2 V^{-1}sec^{-1})	v_{sat} (x 10^7 cm s^{-1})	θ_1 (V^{-1})	θ_2 (V^{-2})
BO-DD	95	1.01	0.4	3.9
TUBS	76	0.95	0.9	1.15
UD	75	0.90	0.7	1.15
SNPS	75	1.05	0.5	0.15

Table 4A.1 Parameters used in the proposed analytical model in order to fit the simulations obtained using different transport models.

4A.4. CMOS inverter

We have studied the behavior of a CMOS inverter based on DG MOSFETs with the technological features given in Figure 4A.3. The supply voltage is set to 1V. The load capacitance used for this inverter is 3.0fF. The aspect ratios are $(W/L)_p$ = (100 nm / 22 nm)$_p$ and $(W/L)_n$ = (50 nm / 22 nm)$_n$.

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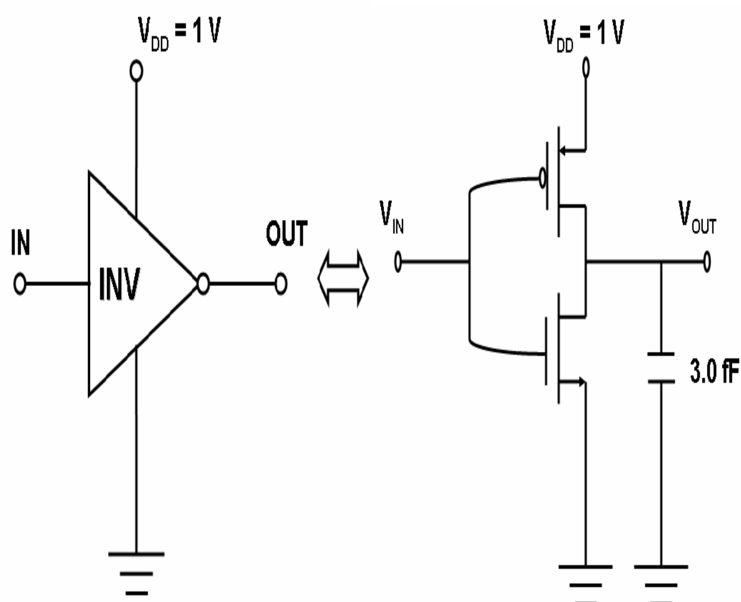

Figure 4A.3 Simulated CMOS Inverter

We have used SMASH circuit simulator [22] to carry out the circuit simulations presented in this work. The model has been implemented in Verilog-A code for both n-channel and p-channel DG MOSFETs and compiled to include the DG devices as new active components of the circuit simulator. We consider DG MOSFET devices with parameters as shown in Figure 4A.1.

In [11] it was shown that our hydrodynamic compact model agreed very well with Monte Carlo (MC) simulations of these 22 nm n-channel devices, including the same template device we are considering in this chapter.

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We have used the extracted parameters of n-channel and p-channel 22 nm DG MOSFETs to simulate the transfer and output characteristics using SMASH simulator. For the DD model, extracted parameters from BO-DD simulations were used. For the hydrodynamic transport model, extracted parameters from UD simulations were used. For this specific case, the quantum mechanical effects are not considered for thicknesses greater than 10nm in the Verilog-A code.

Figure 4A.4 shows the transfer characteristics of drift-diffusion (BO-DD) and hydrodynamic transport model (UD) at low and high V_{DS}. From the curves it can seen that the hydrodynamic transport model included in the core model gives higher drain current than the DD model, due to the velocity overshoot. This can be clearly seen at higher drain bias.

Figure 4A.5 shows the output characteristics of drift-diffusion and hydrodynamic transport model at high V_{GS}. As expected, (because of the velocity overshoot effect) it can be seen from the curves that the hydrodynamic transport model has higher drain current than the DD model in the saturation region.

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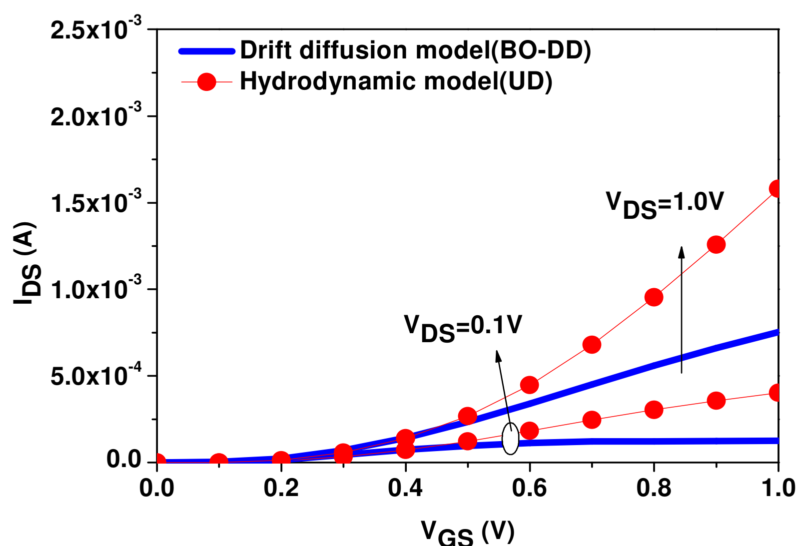

Figure 4A.4 Transfer characteristics obtained for an n-channel DG MOSFET Lg=22 nm Ts=10 nm and EOT=1.1 nm.

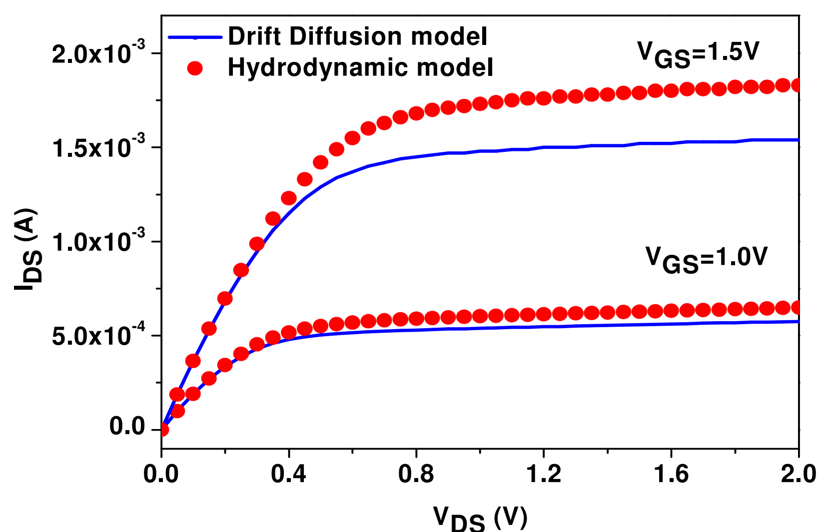

Figure 4A.5 Output characteristics obtained for an n-channel DG MOSFET Lg=22 nm Ts=10 nm EOT=1.1 nm.

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To use the capacitance model in Verilog-A with SMASH, we have to calculate the charges called Q_{gs} and Q_{gd} from the numerical integration of the device capacitances C_{gs} and C_{gd}, obtained from the model, from V_{gs}=0 to V_{GS}, and from V_{gd}=0 to V_{GD}, respectively, where V_{GS} and V_{GD} are the applied gate-source and gate-drain voltages:

$$Q_{gs} = \begin{Bmatrix} \sum_{i=0}^{n} C_{gs}(i) * (V_{gs}(i) - V_{gs}(i-1)) \\ where \\ V_{gs}(i=0) = 0 \\ V_{gs}(i=n) = V_{gs} \end{Bmatrix}$$

$$Q_{gd} = \begin{Bmatrix} \sum_{i=0}^{n} C_{gd}(i) * (V_{gd}(i) - V_{gd}(i-1)) \\ where \\ V_{gd}(i=0) = 0 \\ V_{gd}(i=n) = V_{gd} \end{Bmatrix}$$

The simulator then obtains the charging/discharging currents by differentiating of charges with respect to the time. This modeling is used to obtain the capacitances C_{gs} and C_{gd} in Verilog-A with SMASH, shown in Figure 4A.6.

Figure 4A.6 shows capacitance characteristics for the DG MOSFET as a function of gate voltage. We show that the approximation considered in the calculation of capacitances in the Verilog-A code using SMASH gives practically the same result as the values directly obtained from the capacitance model (Figure 4A.6).

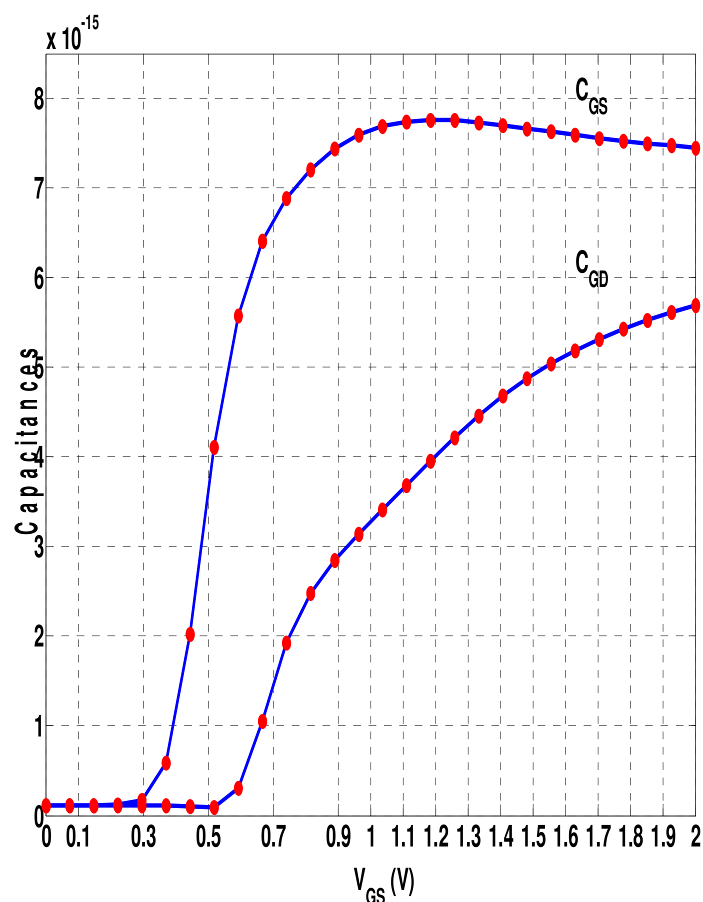

Figure 4A.6 Gate-to-source capacitance (Cgs) and gate-to-drain capacitance (Cgd), for V_{DS}=0.5V, obtained using the method implemented in Verilog-A with SMASH (Symbols) and the entire capacitance model developed (lines).

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Figure 4A.7 shows the voltage transfer of a CMOS inverter obtained using our DG MOSFET model in SMASH by Verilog-A. The channel width of the p-channel device is twice the one of the n-channel device. The curves show the DD and hydrodynamic model. It can be seen that the switching voltage is higher using the hydrodynamic model than the DD model.

Figure 4A.8 shows the transient response of a CMOS inverter with DD and hydrodynamic model. It can be seen that the rise time is much shorter in the hydrodynamic model than in the DD model. The hydrodynamic model gives a therefore a smaller delay than the DD model.

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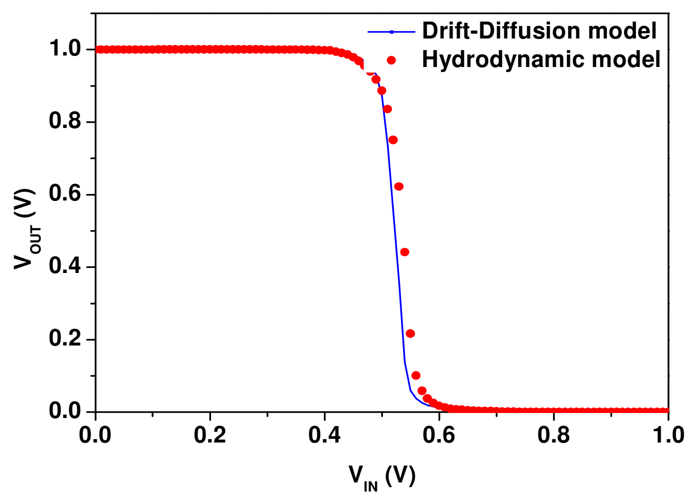

Figure 4A.7 Voltage transfer characteristics of a 22nm CMOS inverter using the DG MOSFET model in Verilog-A with SMASH.

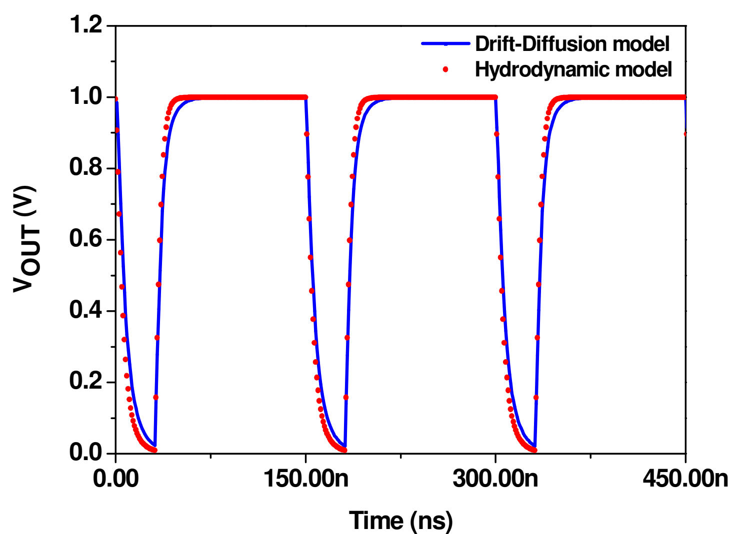

Figure 4A.8 Transient response of 22nm CMOS inverter using our DG MOSFET model in SMASH by means of Verilog-A.

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4A.5 Ring Oscillator

We have studied the behavior of a five stage CMOS ring oscillator based on DG MOSFETs with the technological features given in Figure 4A.3. The load capacitance used for this ring oscillator is 7.0fF. The aspect ratios are $(W/L)_p$ = $(100\ nm\ /\ 22\ nm)_p$ and $(W/L)_n$ = $(50\ nm\ /\ 22\ nm)_n$.

Figure 4A.10 shows the transient response of a five stage CMOS ring oscillator with DD and hydrodynamic model. It can be seen that the oscillation starts with much smaller delay in the hydrodynamic model than in the DD model.

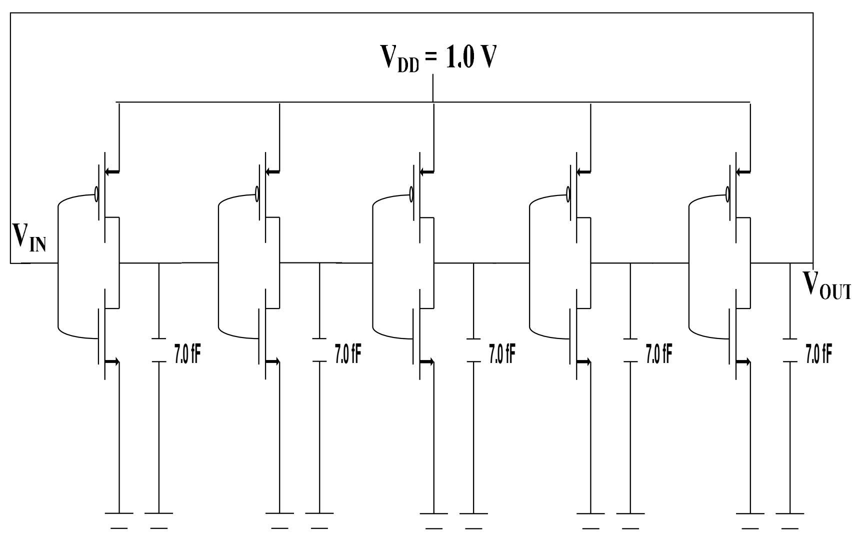

Figure 4A.9 Five stage Ring oscillator

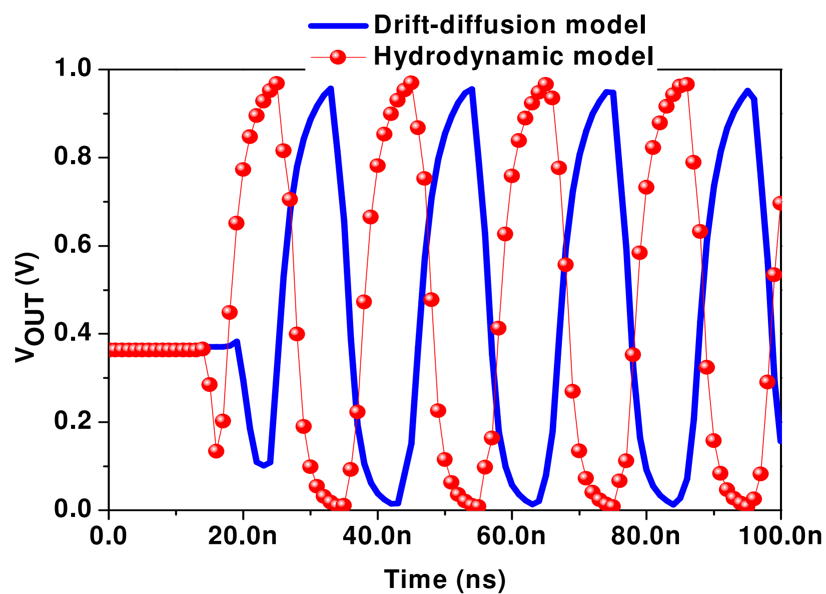

Figure 4A.10 Transient response of 22nm five stage CMOS ring oscillator using our DG MOSFET model in SMASH by means of Verilog-A.

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4B. Compact advanced transport models for nanoscale surrounding-gate (SRG) CMOS circuits

4B.1 Introduction

The main guiding principle of the MOS-device engineering over the past few decades has been based on device-scaling concept. The search of an increase in both the switching speed and the number of transistors integrated has pushed the miniaturization processes to the limit. The most drastically scaled parameters have been the MOSFETs channel length and the gate dielectric thickness. The reduction of the transistor channel length increases short channel effects (SCE). New device structures such as multi-gate MOSFETs (Double gate (DG) MOSFETs, Surrounding-gate (SRG) MOSFETs, PiFETs, FinFETs…), that show a much better electrostatic control are currently under investigation since they seem to be a good alternative to meet the ITRS roadmap requirements for the decananometer era [1][23-24]. One of the most promising multi-gate devices is the surrounding gate transistor SGT [23]. Some models for drain current, terminal charges, and capacitances of silicon based nanowire transistors (SNWTs) have also been proposed [25-27].To use SRG MOSFETs in circuit design, an compact model

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are required. Traditional MOSFETs compact models have been studied using Verilog-A which is becoming the standard language in compact model development. One of the main advantages is that Verilog-A models can be easily exported from a circuit simulator to another, making it use flexible and reusable. The main reason for preferring Verilog-A for compact modelling over general-purpose programming languages is that it frees the model developer from the simulator interface. Model developers have to develop the code only once and it runs in all circuit simulators.

Our starting point, in this section is a compact model for SRG MOSFETs including hydrodynamic transport model in Verilog-A has been implemented to study basic digital circuits. Based on the model for the potentials [28], an analytical compact model for the drain current of a cylindrical SRG MOSFETs has been derived. The model is valid from low to high doping. We extend the current model to include hydrodynamic transport model [28]. The entire compact model is implemented in Verilog-A, which allows the use of the model in any commercial circuit simulators. We have compared the results between drift-diffusion and hydrodynamic transport models of a SRG based CMOS inverter circuit.

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4B. 2 Device structure

The cylindrical SRG MOSFET structure given in chapter 2 (Figure 2B.1) has been considered, which has a physical gate length of 6 nm, a gate stack consisting of 2 nm of HfO2 on top of 0.7nm of SiO2 (EOT=1 nm). The channel diameter is 4 nm. The channel is lowly doped (10^{15} cm^{-3}).

We have studied the characteristics behaviour of a CMOS inverter based on SRG MOSFETs with the technological features as in chapter (Figure 2B.1). The simulated CMOS inverter is shown in Figure 4A.3. The load capacitances used for this inverter is 7.0 fF. The aspect ratios are $(W/L)_P$ = (100 nm / 6 nm$)_P$ and $(W/L)_N$ = (50 nm / 6 nm$)_N$. The supply voltage is set to 1.2 V.

Figure 4B.1 (Top) shows the transfer characteristics of drift-diffusion and hydrodynamic transport model at low and high V_{DS}. From the curves it can seen that the hydrodynamic transport model included in the core model gives higher drain current than the DD model, due to the velocity overshoot. This can be clearly seen at higher drain bias.

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Figure 4B.1 (Bottom) shows the output characteristics of drift-diffusion and hydrodynamic transport model at high V_{GS}. As expected, (because of the velocity overshoot effect) it can be seen from the curves that the hydrodynamic transport model has higher drain current than the DD model in the saturation region.

Figure 4B.2 shows the voltage transfer of a CMOS inverter obtained using our SRG MOSFET model in SMASH by Verilog-A. The channel width of the p-channel device is twice the one of the n-channel device. The curves show the DD and hydrodynamic model. It can be seen that the switching voltage is higher using the hydrodynamic model than the DD model.

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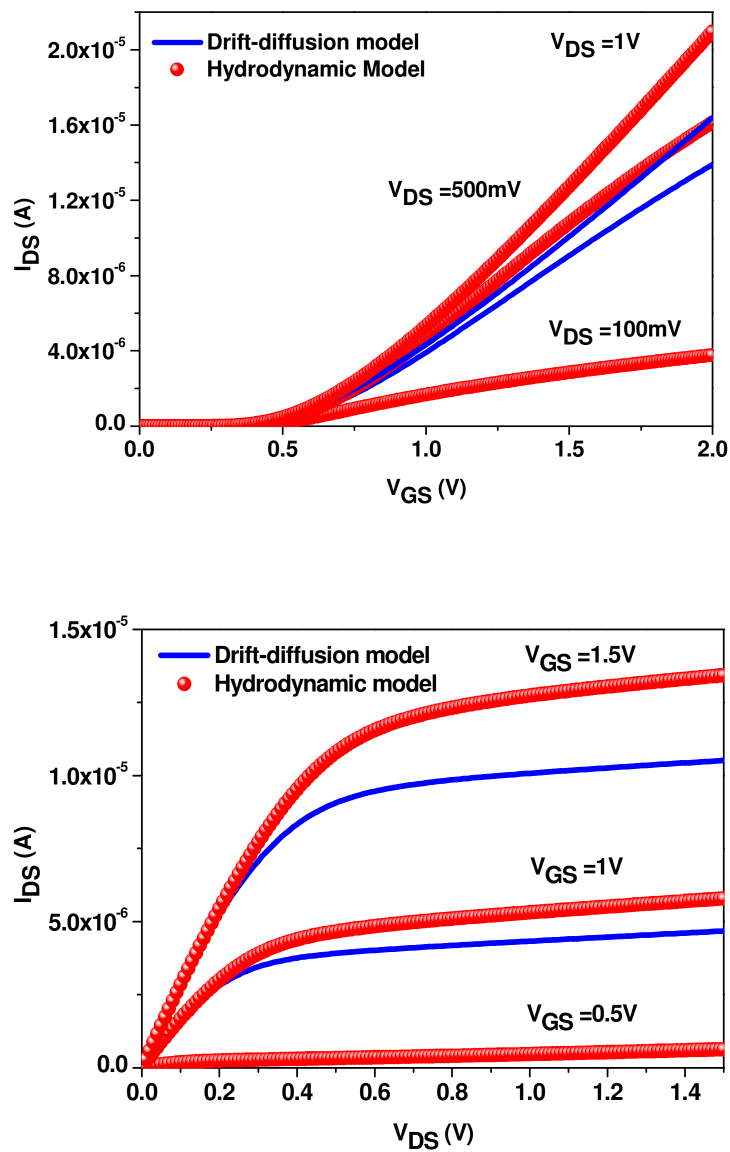

Figure 4B.1 Transfer (top) and output (bottom) characteristics for an n-channel SRG MOSFET Lg=6 nm Ts= 4 nm and EOT= 1 nm.

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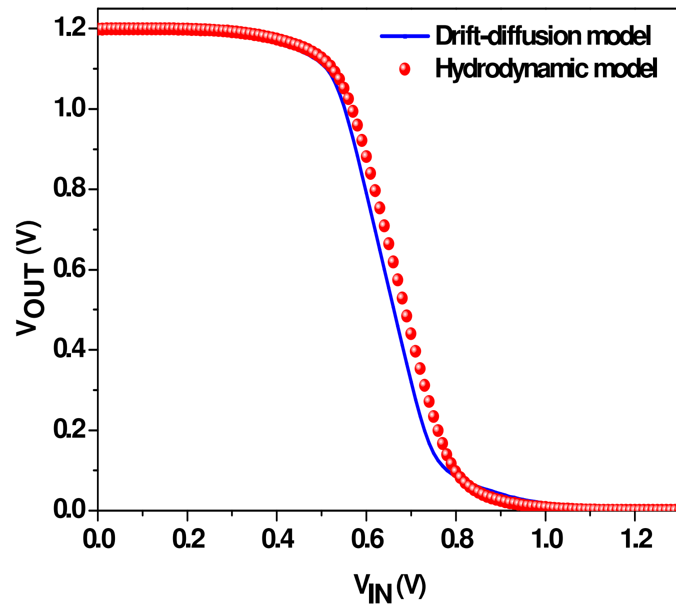

Figure 4B.2 Voltage transfer characteristics of a CMOS inverter using SRG MOSFET model in Verilog-A with SMASH.

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4C Conclusions

In this chapter, we present the implementation of compact nanoscale DG MOSFET models accounting for hydrodynamic transport model, in Verilog-A for circuit simulation. We have carried out a comparison of the simulated performance of a 22nm CMOS inverter using both the hydrodynamic transport model and the drift diffusion model for nanoscale DG MOSFETs with model parameters extracted from 2D advanced transport simulations. As expected, smaller delays are obtained with the hydrodynamic model.

The compact nanoscale SRG MOSFET models accounting for hydrodynamic transport model, in Verilog-A implemented in circuit simulation are presented. We have carried out a comparison of the simulated performance of a CMOS inverter using both the hydrodynamic transport model and the drift diffusion model for nanoscale SRG MOSFETs with model parameters extracted from 3D advanced transport simulations.

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Chapter 5

Conclusions

The world of nanoelectronics is moving forward at incredible speed, and its technology keeps improving at the same rate. The modern analytical tools are in fact a combination of numerical approaches and analytical expressions, and often rely on adjusting parameters that do not give any insight functioning of the device. A complete analytical modeling tool, based on a physical characterization of a device, taking into account all the new phenomena that come into play when lowering the dimensions of the devices towards tens of nanometers are of urgent need. This research work has been developed to cover precisely these aspects. The models described here are physical models, with very few adjusting parameters, that can be easily replaceable with values extracted from experimental measurements; they are compact models, making use of approximate expressions that have been tweaked to offer a very good fit with numerical simulations. Another major advantage is the fact that these models can be easily incorporated into circuit simulators, which allows designers to unleash the full capabilities of the design software to create new devices and applications.

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In this thesis we have developed an analytical and continuous compact model for long-channel cylindrical SRG MOSFETs. The analytical expression for the surface potentials are continuous and explicit function of the applied voltages. The expression obtained for the potentials are used to derive an analytical compact model for the drain current which is valid from low to high doping concentrations. The compact model is then enhanced to include the hydrodynamic transport and quantum mechanical effects, and we show that it can reproduce results of 3D numerical simulations using advanced transport models. The final compact model includes mobility degradation, drain-induced barrier lowering, velocity overshoot and quantum effects.

The same approach has been applied for the compact model in DG MOSFET. The model has been extended to include the hydrodynamic transport and quantum mechanical effects. The final compact model can accurately reproduce simulation results of some of the most advanced transport simulators. The model is based on a compact model for charge quantization within the channel and it includes mobility degradation, channel length modulation, drain-induced barrier lowering, overshoot velocity effects and quantum mechanical effects. The temperature dependency is also accounted in the compact model.

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The final goal of our study is the usage of the compact model in circuit simulator. For implementing and testing our models of multi-gate MOSFET devices has been done in SMASH circuit simulator. The results of our implementation of a nanoscale double-gate (DG) and cylindrical surrounding-gate (SRG) MOSFET compact models, which includes hydrodynamic transport model, in Verilog-A are presented. The model is used with SMASH circuit simulator for the analysis of the DC and transient behaviour electrical CMOS circuits.

We conclude this chapter with some recommendations for further work. With our proposed compact model for multi-gate MOSFETs the next step would be enhance the model to study the noise behaviour for these devices. The proposed model can be used to study and validate a tri-gate MOSFETs for the current technological nodes and for the future technological nodes. Further, the model can be improved in the Verilog-A source code by incorporating the quantum effects and also the noise behaviours.