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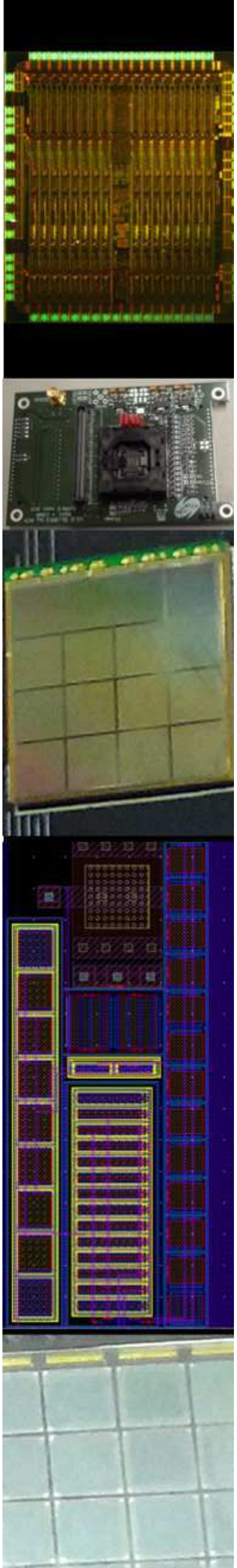

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Albert Comerma i Montells

Universitat de Barcelona

Institut de Ciències del Cosmos

UNIVERSITAT DE BARCELONA

INSITUT DE CIÈNCIES DEL COSMOS

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Development of a multichannel integrated circuit for Silicon Photo-Multiplier arrays readout

Albert Comerma i Montells

DIRECTOR

Dr. David Gascón i Fora

TUTOR

Dr. Atilà Herms i Berenguer

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Agraïments

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Abstract

The aim of this thesis is to present a solution for the readout of Silicon Photo-Multipliers (SiPMs) arrays improving currently implemented systems. Using as a starting point previous designs with similar objectives a novel current mode input stage has been designed and tested. To start with the design a valid model has been used to generate realistic output from the SiPMs depending on light input. Design has been performed in first place focusing in general applications for medical imaging Positron Emission Tomography (PET) and then using the same topology for a more constrained design in particle detectors (upgrade of Tracker detector at LHCb experiment).

A 16 channel ASIC for PET applications including the novel input stage has demonstrated an excellent timing measurement with good energy resolution measurement and pile-up detection. This document starts with the analysis of the requirements needed to fit such a system. Followed by a detailed description of the input stage and analog processing. Signal is divided in the input stage into three different signal paths: timing, energy and pile-up. Every channel performs different signal analysis to deliver; a fast time signal output (digital edge), energy output (a linear time over threshold digital output) and a digital bit to signal pile-up. The time information is then ORed between all channels to generate a single timing output. All the pile-up bits are combined in a digital word ready to be readout for the 16 channels. Design has been optimized for reduced power consumption and no components needed to interface inputs and outputs. Digital slow control to tune the circuit behaviour is also included. The prototype measurements have proved to be a valid option for integration in a full system scanner.

An adapted prototype of the input stage using different technology and adapted to the different constraints from a particle detector is also presented. Only simulation results are available since device is still under production. An analysis of the different requirements needed by the SciFi tracker design is summarized. Current specifications are still evolving since final sensor is still not defined, but other requirements and some tunable elements permits to design such prototypes.

Contents

Resum

L'objectiu d'aquesta tesi és presentar una solució per a la lectura de matrius de fotomultiplicadors de silici (**SiPM**) millorant les característiques de sistemes actuals. Amb aquesta finalitat s'ha dissenyat i provat el circuit d'una nova etapa d'entrada. En primer lloc s'ha dissenyat pensant en aplicacions genèriques i per a imatge mèdica, concretament per a escàners PET (Positron Emission Tomography). Però més endavant s'aplica la mateixa topologia per a una aplicació més concreta i específica com és un detector de partícules (l'actualització del Tracker a l'experiment **LHCb**).

Els SiPM són uns dispositius electrònics relativament nous[1] amb la possibilitat de comptar fotons i millorant algunes característiques dels sensors actuals, com serien la tensió d'operació més baixa, més guany o immunitat a camps magnètics, mentre manté unes prestacions excel·lents respecte el guany, resolució temporal i rang dinàmic. Aquest tipus de dispositius es troben en constant evolució encara i una gran varietat de fabricants intenten millorar les prestacions, sobretot respecte la eficiència en la detecció de llum, reduir el corrent d'obscuritat, construir matrius més grans i augmentar l'espectre al qual són sensibles.

En aquest document es presenta el disseny d'un circuit integrat específic amb les següents característiques: gran rang dinàmic, alta velocitat, multicanal, amb entrada en corrent i baixa impedància d'entrada, baix consum, control de la tensió de polarització del SiPM i amb les sortides de; temps, càrrega i apilament.

El preamplificador utilitza un circuit nou amb doble realimentació que redueix la impedància d'entrada al mateix temps que manté una polarització fixa en el node d'entrada.

Fotomultiplicador de Silici (SiPM)

Els fotomultiplicadors de silici són uns dispositius formats per centenars de micro-cel·les en paral·lel. Cada cel·la és un díode d'allau (APD) treballant en mode Geiger, amb una resistència que evita la destrucció del dispositiu. El comportament dels APDs és conegut i estudiat des de principis dels anys 60[7]. Totes les cel·les es combinen en una sola sortida (connectades en paral·lel). El resultat és una sortida molt similar a la produïda

per un Tub Fotomultiplicador convencional (PMT), però amb una senyal discreta (cada cel·la deixa anar una quantitat fixa de càrrega).

De la mateixa manera que els APDs els primers parells de portadors dins el silici es generen mitjançant efecte fotoelèctric i es multipliquen dins del silici. En aquest cas, però la multiplicació és una allau produïda pel fet d'estar per sobre la tensió de trencament del dispositiu. Per evitar un efecte destructiu de l'allau s'incorpora una resistència en serie al dispositiu per baixar la tensió per sota el trencament en el cas d'una allau. El guany resultant és semblant al d'un PMT de l'ordre de 10^5 a 10^7.

La probabilitat de detecció de llum d'un SiPM es defineix per la Eficiència de Detecció de Fotons (PDE). Aquesta eficiència es calcula mitjançant els efectes produïts per la zona no utilitzada entre les micro-cel·les (FF) i la eficiència quàntica del dispositiu (QE). El PDE es calcula fàcilment multiplicant els elements anteriors per la probabilitat que un parell electró-forat comenci una allau.

Moltes mesures sobre diferents propietats de diferents fabricants es poden consultar en la literatura[8] igual que la descripció de diferents efectes no desitjats dels dispositius[9].

Els SiPM ofereixen una sortida lineal respecte la il·luminació rebuda en un cert rang. La saturació dels SiPM es pot modelitzar mitjançant la equació[10] 1, on m és el nombre total de cel·les del dispositiu i ε el PDE.the photon detection efficiency.

$$N_{cel \cdot les disparades} = m * \left(1 - e^{-\frac{N_{fotons} * \varepsilon}{m}}\right) \tag{1}$$

Els fotomultiplicadors de silici tenen una important dependència entre la variació de la tensió de trencament i la temperatura, de manera que també afecten el guany. El coeficient de temperatura depèn del procés de fabricació però és habitual en aquest tipus de dispositius. En el cas que es polaritzin un conjunt de dispositius amb la mateixa tensió caldrà poder variar la tensió en el node de connexió amb la electrònica de lectura per a poder compensar aquestes variacions, de la mateixa manera que també pot variar la tensió de trencament entre diferents dispositius d'una matriu.

El fenomen anomenat com a After Pulsing és un efecte conegut que consisteix en la generació de senyal de forma espontània després d'un primer pic de senyal. És degut a l'acumulació de càrrega en els defectes del semiconductor. Aquesta càrrega atrapada es pot alliberar més tard. Si la càrrega s'allibera pot generar una nova allau. Els temps típics d'alliberament són des dels pocs ns a centenars de ns. Les primeres càrregues alliberades no afecten la senyal de sortida ja que les cel·les encara no s'han recarregat, però

incrementaran el temps de recuperació del dispositiu. Treballar a baixes temperatures fan aquest alliberament més lent, per tant l'efecte és més evident.

Un dels principals problemes dels SiPM és l'anomenat corrent d'obscuritat. Aquesta corrent es genera de forma espontània per càrregues excitades tèrmicament. Aquestes càrregues poden generar una allau en la cel·la que serà idèntica a una senyal generada per un fotó. El nombre d'allaus per temps dóna un resultat de comptes d'obscuritat (normalment en Hz).

Les principals avantatges i inconvenients dels Fotomultiplicadors de Silici es resumeixen en la taula següent:

Avantatges	Inconvenients
Alta eficiència Quàntica	Resistència a la radiació
Poca sensibilitat al camp magnètic	Baix PDE
Compacte i resistent	Comptes d'obscuritat
Baixa tensió (20V - 100V)	
Matrius de dispositius	

Table 1: Avantatges i inconvenients dels Fotomultiplicadors de Silici

Centellejadors

Un centellejador és un material que exhibeix emissió de llum (sense escalfar-se) quan s'excita mitjançant radiació ionitzant. Aquesta radiació es composa per partícules que tenen prou energia cinètica individualment per alliberar un electró d'un àtom o molècula, ionitzant. Quan el material rep una partícula absorbeix la energia i la re-emet en forma de llum. Depenent del material, l'estat d'excitació pot ser meta-estable de forma que la relaxació es pot retardar algun temps (des de microsegons a hores). Les primeres utilitzacions de centellejadors es daten a principis del segle 20[13] però fins a 1944 no es van utilitzar de forma generalitzada combinant-los amb fotomultiplicadors convencionals (PMTs). En aquests detectors moderns el primer element en el camí de la partícula ionitzant és el cristall centellejador i la converteix a una senyal lluminosa. Aquesta llum es converteix a una senyal elèctrica mitjançant un transductor (PMT, APD o SiPM) i llavors es processa. Els cristalls no són ideals i presenten variacions temporals importants en la generació de llum. Una vegada la llum s'ha generat aquesta ha de recórrer el camí fins el transductor que pot incrementar encara més la dispersió temporal, sobretot depenent de les dimensions del cristall[14].

Moltes de les propietats desitjades són; gran densitat, alta velocitat, bona linealitat, resistència a la radiació i baix cost. L'alta densitat redueix la necessitat de material per a produir llum de partícules d'alta energia i l'efecte Compton es redueix per partícules de més baixa energia. L'alta velocitat, amb temps de recuperació ràpids, porta a una millor resolució en les mesures i millor identificació del tipus de partícules mesurades, a més de reduir el temps de recuperació. La resistència a la radiació és necessària per mantenir els cristalls en detectors amb un ambient hostil. Finalment el cost també és un factor important ja que els cristalls solen necessitar processos de purificació complicats i terres rares per a la seva fabricació.

Les propietats típiques d'alguns centellejadors inorgànics es resumeixen en la taula 2. Els centellejadors orgànics tenen una densitat molt menor (1 g/cm^3) i menys emissió de llum (al voltant del 50% del NaI(Tl)).

Table 2: Propietats de centellejadors inorgànics

Material Centellejador	**Densitat (g/cm^3)**	**Longitud d'ona at max.(nm)**	**Índex de refracció**	**Temps relaxació(ns)**	**Llum emesa (ph/MeV)**
NaI(Tl)	3.67	415	1.85	230	38000
CsI(Tl)	4.51	540	1.80	680,3340	40000,25000
$Bi_4Ge_3O_{12}$	7.13	480	2.15	300	8200
BaF_2	4.89	220,310	1.56	0.6,630	1500,9500
CeF_3	6.16	310,340	1.68	5,27	4400
$YAlO_3$(Ce)	5.37	370	1.95	27	18000
Lu_2SiO_5(Ce)	7.4	420	1.82	47	25000
$LaBr_3$(Ce)	3.79	350	1.9	27	49000
BC-400	1.03	420	1.58	2.4	10000
BGO: $Bi_4(GeO_4)_3$	7.13	480	2.15	300	5700
LSO: $Lu_2(SiO_4)O$:Ce	7.4	420	1.82	42	28500
GSO: $Gd_2(SiO_4)O$:Ce	6.71	440	1.85	60	7600
LYSO: $Lu_{1.8}Y_{0.2}(SiO_4)O$:Ce	7.1	420	1.81	40	40000

Aplicacions dels SiPMs

Els fotomultiplicadors de silicis es poden utilitzar en qualsevol aplicació on es necessiti la mesura de senyals febles de llum. Les aplicacions més habituals són; l'ús en la detecció de rajos gamma emesos per un isòtop introduït en el cos per detectar l'acumulació en diferents àrees (com per exemple en la tomografia d'emissió de positrons, PET) o els detectors de partícules d'altes energies per a usos comercials o d'investigació en les seves variants (com per exemple la construcció de calorímetres a l'LHC).

Tomografia d'Emissió de Positrons, PET

La Tomografia d'Emissió de Positrons (PET) és una tècnica d'imatge mèdica que produeix imatges en tres dimensions dels processos funcionals del cos. Els sistemes PET es basen en la detecció de parells de rajos gamma emesos indirectament per un isòtop introduït en el cos. Les dades produïdes per la concentració de parells de rajos gamma i el seu temps d'arribada s'utilitzen per a construir imatges en tres dimensions de l'activitat dins del cos. Els aparells actuals utilitzen sistemes combinats de raigs X però seria desitjable substituir-los per ressonància magnètica ja que no augmenten la radiació a la que s'exposa el pacient i millora el contrast en els teixits tous. En la figura 1 es pot veure a nivell esquemàtic un sistema PET.

El bloc de detecció normalment està format per cristalls centellejadors (que converteixen el raig gamma a llum) seguits per tubs fotomultiplicadors (convertint la senyal de llum en una corrent elèctrica) i la electrònica de processat (amb amplificació i mesura del temps i de la senyal d'entrada). La resolució espacial final depèn de la mida dels cristalls i de la precisió del sistema global.

La combinació de sistemes PET amb raigs X o MRI donant mesures anatòmiques i metabòliques en el mateix aparell és molt útil ja que el pacient no es mou entre mesures. Això és més important en estructures amb variacions anatòmiques o en òrgans que es puguin moure.

Les dades generades per l'escàner són una llista d'esdeveniments en coincidència representant deteccions gairebé simultànies dels fotons aniquilats (en detectors situats a 180º). Cada coincidència representa una línia en l'espai connectant els dos detectors. Normalment és necessari molt processat per a generar les imatges finals.

Els sistemes PET només accepten esdeveniments vàlids al voltant de la finestra d'energia produïda per un raig gamma, 511keV. Si un esdeveniment es troba en aquesta finestra i amb coincidència amb un detector situat a

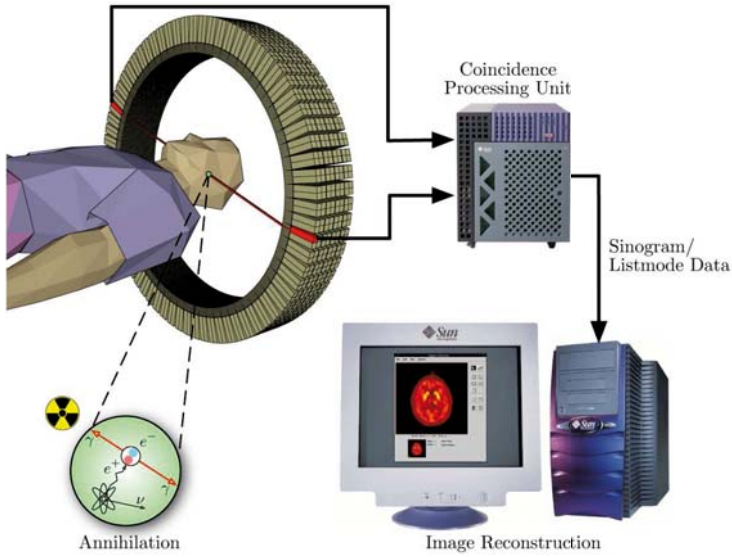

Figure 1: Esquema d'un sistema PET

l'altre costat l'esdeveniment s'accepta. Tota la resta es descarta. Per evitar l'acumulació de dades és important prendre aquestes decisions el més ràpidament possible en el detector.

Alguns cristalls tenen una emissió espontània de llum, emetent un espectre en la regió d'interès. Com a exemple Saint Gobain produeix el PRelude 420[24], un centellejador basat en un isòtop del Luteci generant 3 raigs gamma en cascada de 307, 202 i 88 keV, essent el més probable una energia de 597keV.

Temps de Vol

El Temps de Vol (ToF) és un mètode utilitzat per a mesurar el temps que triga una partícula per a recórrer una certa distància. Aquesta mesura s'utilitza per a determinar alguna propietat del medi de propagació o per a conèixer alguna propietat de la partícula. La partícula es pot detectar directa o indirectament. En sistemes PET els esdeveniments d'interès es detecten fàcilment mitjançant la coincidència. És una mesura indirecta ja que la partícula genera una senyal lluminosa en el centellejador i llavors aquesta senyal es converteix a corrent i és processada. La mesura de temps en els dos costats dels detectors ajuda a millorar la resolució sobre la posició on s'ha produït l'esdeveniment.

CERN i LHC

El Centre Europeu per la Recerca Nuclear o *Conseil Européen pour la Recherche Nucléaire* (CERN) es va fundar el 1954 amb la intenció d'esdevenir una institució líder en el món en aquest camp de recerca. Es va construir en la frontera Suïssa i Francesa, a prop de Ginebra. Els seus edificis s'estenen al llarg dels dos costats de la frontera, de la mateixa manera que el túnel on hi ha l'accelerador més potent creat fins al moment, el Gran Col·lisionador d'Hadrons (LHC). Durant la seva història ha tingut diferents acceleradors i experiments donant lloc a diferents descobriments i premis. Avui en dia 20 països formen part dels membres d'aquesta col·laboració internacional. L'LHC és un col·lisionador protó-protó situat en un anell de 27km construït sota el terra.

LHCb

L'experiment Large Hadron Collider beauty (LHCb) és un dels experiments actuals al CERN (Ginebra). En la figura 2 es mostra el detector. LHCb és un espectròmetre amb un angle de cobertura aproximat de 15 a 300 mrad en el pla horitzontal i de 15 a 240 mrad en el pla vertical. Aquesta geometria està motivada pel fet que els parells de partícules $b\bar{b}$ produïts a LHC es produeixen majoritàriament en una direcció única.

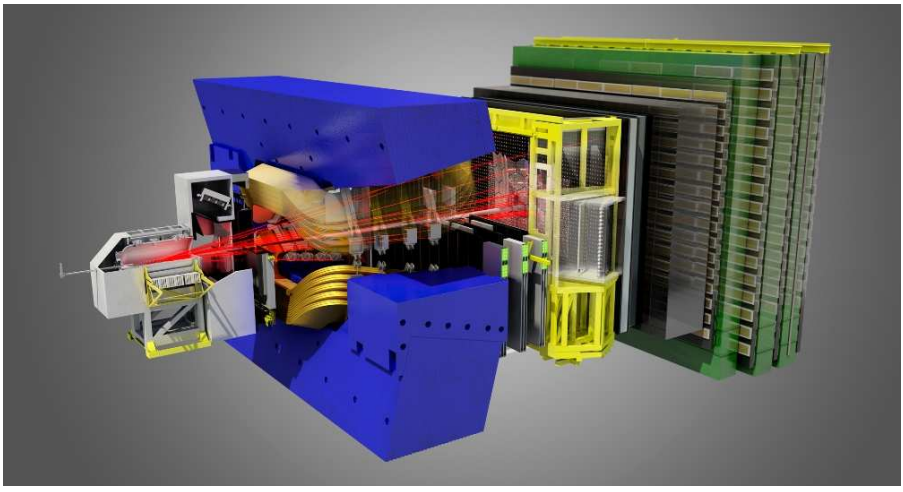

Figure 2: LHCb detector[a]

[a]Imatge proporcionada per la col·laboració LHCb

Començant des del punt d'interacció, a l'esquerra de la figura, el detector consisteix en un sensor de *tracking* construït amb tires de silici envoltant la zona d'interacció (el detector de Vèrtex). Tot seguit hi ha un imant que genera un camp aproximat de 4Tm i que corba la trajectòria de les partícules. Tot seguit els RICH (Ring Imaging Cherenkov) que identifiquen partícules carregades distingint pions i kaons. Després d'aquest punt els detectors són grans telons verticals que defineixen diferents plans paral·lels de mesura. Un detector de silici cobrint una gran àrea (el *trigger tracker, TT*) en combinació amb un detector gasós (el *Inner Tracker, IT, i Outer Traker, OT*). Detectors de muons i finalment calorímetres (Hadrònic i Eelctromagnètic) per a mesurar l'energia de les partícules.

SciFi Tracker

El tracker actual de LHCb està format pel detector gasós de l'OT i el detector de tires de silici de l'IT per cobrir la zona amb més ocupància al voltant de la canonada amb el feix de partícules. Per a l'actualització del detector s'ha escollit una nova tecnologia basada en fibres centellejadores[6], amb fibres clares generant i transportant la senyal. La zona central es reemplaçarà per fibres centellejadores cobrint tota l'alçada del detector. Contindrà fibres de 2.5m separades per miralls en el punt mig i llegides per fotomultiplicadors de silici muntats als extrems.

Amb aquesta configuració el material es redueix al mínim. Un dels problemes principals és determinar les prestacions dels fotomultiplicadors de silici en radiació. Alguns estudis s'han realitzat mitjançant una font radioactiva de PuBe[6], i s'han deixat mostres en el detector d'LHCb durant 2011.

Les tècniques per la producció de les matrius de SiPM encara es troben en desenvolupament. I s'han fabricat alguns prototips amb característiques adequades.

Una matriu de SiPMs a mida s'està desenvolupant per encaixar en la mida del mòdul evitant zona morta. Els prototips de Hamamatsu i Ketek consisteixen en matrius de 64 canals amb el càtode comú. Amb una àrea total de 0.23x1.32mm^2 per canal, 96 micro-cel·les i una mida de 57.5x55μm^2 per micro-cel·la. Els 128 canals es fabriquen unint dues oblees amb 64 canals amb un costat polit de forma que es redueix al mínim la distància entre les oblees.

Model dels SiPM

La utilització d'un model fiable és imprescindible per produir senyals fidels a la realitat al dissenyar la electrònica. Un model simple[26] s'ha implementat i utilitzat mitjançant eines SPICE. L'esquema del model es pot observar en la figura 3 amb els paràmetres corresponents en la taula 3.

En aquest model [26] les diferents cel·les es modelitzen com elements passius amb la diferència que les cel·les disparades tenen alguns elements més que la resta, que actuen com a càrrega.

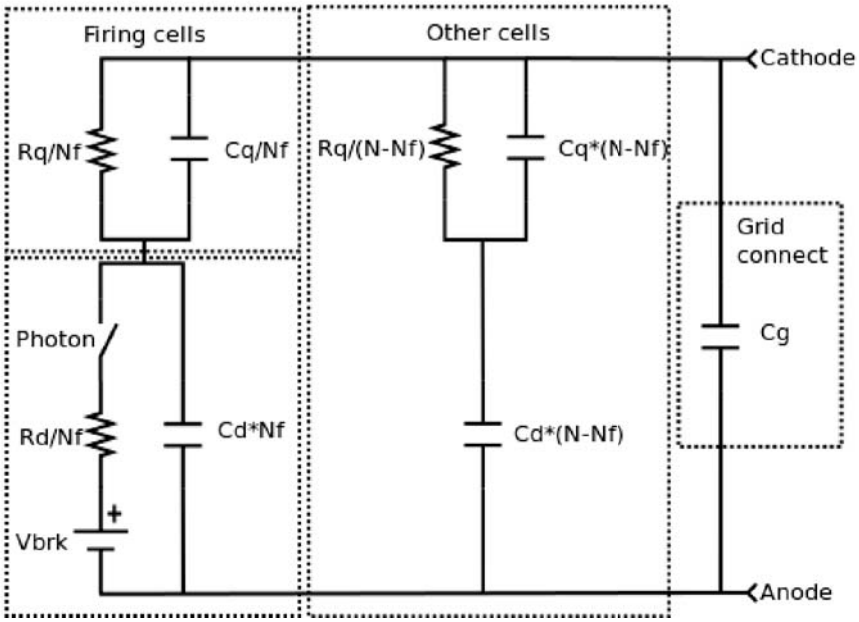

Figure 3: Esquema del model

Degut a que la base d'una micro-cel·la és un díode amb una resistència de quenching per evitar la seva destrucció, el model incorpora una capacitat paràsita en paral·lel al díode, una font de voltatge i una resistència en sèrie.

El díode començarà a conduir quan la font tingui un valor superior a la tensió de trencament i l'interruptor ideal es tanqui (simulant l'arribada de llum). Altres elements com la capacitat paràsita de connexió o la inductància paràsita dels pins es pot afegir al model en sèrie a la connexió.

Paràmetre	Descripció
Rq	Resistència Quenching
Cq	Capacitat paràsita Rq
N	Cel·les
Nf	Cel·les disparades
Cd	Capacitat del Díode
Rd	Resistència del Díode
Vbrk	Tensió trencament
Cg	Capacitat de connexió

Table 3: Paràmetres del model

Per determinar la resistència de quenching el més fàcil és mesurar la corba IV del dispositiu. Quan es posi a conduir, la pendent de la corrent serà la resistència del dispositiu dividit pel número de dispositius en paral·lel.

Per a determinar la suma de C_d i C_q es pot utilitzar la variació de càrrega generada per una sola cel·la en diferents tensions d'operació V_{op} [26]. D'aquesta manera també es pot estimar la tensió de trencament V_{brk} extrapolant el voltatge per una càrrega igual a zero.

Finalment el nombre de cel·les (N) i la capacitat dels terminals s'especifiquen al datahseet del dispositiu.

L'únic paràmetre no definit ni mesurable directament és la R_d però serà de l'ordre de centenars d'Ohms, sense afectar la forma de la senyal.

Resultats de les simulacions

Utilitzant la forma del pic d'obscuritat i la seva amplitud, podem comparar la senyal amb les simulacions. Els paràmetres utilitzats es resumeixen en la taula 5. En la figura 4 hi ha la comparació entre una senyal simulada i la mesura corresponent.

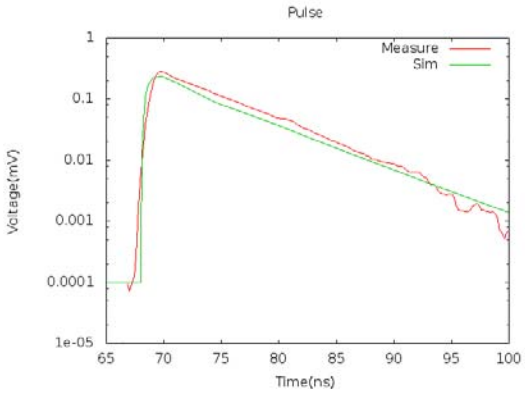

Figure 4: Simulació d'una cel·la i mesura

Paràmetre	Valor
Rq	300kΩ
Cq	5.7fF
N	1600
Cd	12fF
Rd	1kΩ
Cg	15.8pF
$\mathbf{V}_{brk}$	69.47V

Figure 5: S10362-11-025P paràmetres

ASICs de lectura de SiPMs

Un resum de diferents opcions per a la lectura de fotomultiplicadors de silici formen aquesta secció, amb una descripció de les diferents arquitectures. És important tenir en compte que probablement no tots els desenvolupaments hi estaran recollits degut a la gran quantitat d'opcions. L'objectiu és obtenir una visió global de l'estat de l'art en el desenvolupament de circuits integrats per a la lectura de fotomultiplicadors de silici.

Les implementacions típiques de pre-amplificadors es basen en Amplificadors Sensibles a la Càrrega (CSA) o en etapes d'entrada en mode corrent. Cadascun d'ells té les seves avantatges i inconvenients. L'amplificador de càrrega o tensió permet una connexió del sensor tant en l'ànode com el càtode i normalment es troba amb un acoblament en alterna per poder variar el valor en contínua del node d'entrada. Les implementacions en mode corrent només permeten la connexió en un dels dos terminals (la direcció de la corrent ha de ser la correcta) i solen oferir millors característiques de velocitat.

Degut als diferents anys de fabricació i en diferents tecnologies els prototips no es poden comparar directament pel que fa el consum i l'àrea. Però per tenir una primera aproximació de com s'han realitzat les implementacions pot ser un valor interessant.

Taules comparatives

Per tal de comparar algunes característiques de diferents ASICs els elements més interessants es resumeixen en les tables següents, 4 i 5. En la primera hi ha un resum de les sortides, tipus de sortides, magnitud mesurada, resolució i informació temporal. A la segona es resumeix el tipus d'etapa d'entrada, potència, àrea i tecnologia.

L'aproximació habitual és donar càrrega i informació temporal (realitzant una OR de diferents canals). Normalment aquesta mesura doble es realitza dividint en dos la senyal a la sortida del pre-amplificador, dividint-se en dos camins de senyal amb diferent processat. Es realitzen prototips amb molts canals degut als sistemes en els quals han d'anar instal·lats.

A les taules es pot veure que la lectura més popular és en càrrega. Sovint aplicant algun circuit per canviar la forma en el pre-amplificador. Aquests tipus de circuits s'utilitzen sovint en detectors de partícules, però no aprofiten les possibilitats temporals del sensor. Per altra banda la lectura en corrent s'utilitza menys i habitualment connectat al càtode.

Les implementacions diferencials no s'utilitzen massa degut a que el sensor és unipolar i normalment el consum se'n ressenteix i complica la connexió.

ASIC	Sortides	Measura	Resolució	Sortida Temporal
FLC_SIPM	Multiplexat analògic	Càrrega	-	No
MAROC3	Multiplexat analògic i digital	Càrrega	Fins 12 bits	64 + 2OR
SPIROC2c	Digital temps i càrrega	Temps i Càrrega	12 bits i 150ps	Paraula digital
NINO	Digital	Temps i amplada	60ps	LVDS
PETA	Digital	Temps i energia	28ps rms	Paraula digital
BASIC	Digital i analògic mux.	Temps i energia	650ps	OR temps
VATA64	Multiplexat analògic i digital	Temps i càrrega	-	Temps i analògic
RAPSODI	Digital	Temps i càrrega	-	Temps
TOFPET	Digital	Temps i càrrega	50ps	Paraula digital

Table 4: Sortides dels ASICs

Table 5: Propietats dels ASICs

ASIC	Tipus entrada	Tecnologia	Impedància entrada	Canals	Àrea (mm^2/ch)	Potència mW/ch	Any
FLC_SIPM	Càrrega	0.8μm AMS	AC	18	0.56	11	2004
MAROC3	Corrent	0.35μm SiGe AMS	$\approx$50Ω	64	0.25	2.5	2009
SPIROC2c	Càrrega	0.35μm SiGe AMS	AC	36	0.89	$\approx$2.5	2012
NINO	Dif. Càrrega	0.25μm IBM	$\approx$20Ω	8	1	40	2003
PETA	Diferencial	0.18μm UMC	-	16	0.66	86	2008
BASIC	Corrent	0.35μm SiGe AMS	$\approx$17Ω	8	0.88	>2.65	2008
VATA64	Corrent	-	AC	64	1	15	2007
RAPSODI	Corrent	0.35μm SiGe AMS	$\approx$20Ω	2	4.5	100	2008
TOFPET	Corrent	0.13μm	10-60Ω	64	0.39	7	2012

Disseny per PET

Els objectius principals per a un disseny multicanal que millori els sistemes actuals i utilitzable en sistemes PET es resumeix en els següents punts;

- Ample de Banda $\approx$ 250MHz
- Connexió directa al SiPM
- Valor de tensió DC controlable al SiPM
- Baixa impedància d'entrada
- OR ràpida entre tots els canals per a mesura temporal
- Mesura d'energia mitjançant una senyal digital del tipus Temps sobre un llindar (ToT)
- Minimitzar consum
- Bona linealitat

Arquitectura

En la figura 6 es mostra un diagrama de blocs del canal analògic implementat. Després d'analitzar els ASICs anteriors sembla que la millor solució per la mesura és una etapa d'entrada en corrent. La etapa implementada permet controlar el valor en contínua del node d'entrada i generar còpies de la senyal d'entrada. En aquest cas es generen tres còpies que s'utilitzen per a tres mesures; temps, energia i apilament.

Per la mesura temporal l'habitual és utilitzar un dels camins de senyal i comparar directament amb un llindar per detectar un flanc. Aquest procediment dóna prou bons resultats. Altres processats són molt més complexos i milloren la resolució lleugerament [40]. Per evitar la complexitat s'ha escollit un comparador ràpid en corrent per aquesta aplicació.

Per la mesura d'energia s'ha escollit una sortida digital degut a la seva flexibilitat en la lectura i els pocs recursos necessaris en l'ASIC (no cal ADC). Un integrador amb una corrent de descàrrega constant genera una senyal que va a un comparador amb histeresis. Utilitzant aquest circuit s'obté una sortida amb una amplada lineal respecte el pic de corrent d'entrada. D'aquesta manera s'eviten correccions a posteriori.

Per la mesura d'apilament simplement s'utilitza una altra branca amb un acoblament en alterna. La sortida de l'acoblament es passa per un comparador en corrent ràpid de manera que tenim una senyal digital curta per cada variació brusca de corrent a l'entrada. Aquesta senyal es passa llavors

per dos flip-flops en cascada de forma que generen una senyal lògica a nivell alt si hi ha hagut dos pics o més. La sortida es guarda en un registre de 16 bits de forma que es pot llegir el resultat de tots els canals.

Aquesta arquitectura manté una connexió molt simple tant a l'entrada com a les sortides, sense la necessitat de components afegits i amb una interfície digital compatible amb una FPGA comercial.

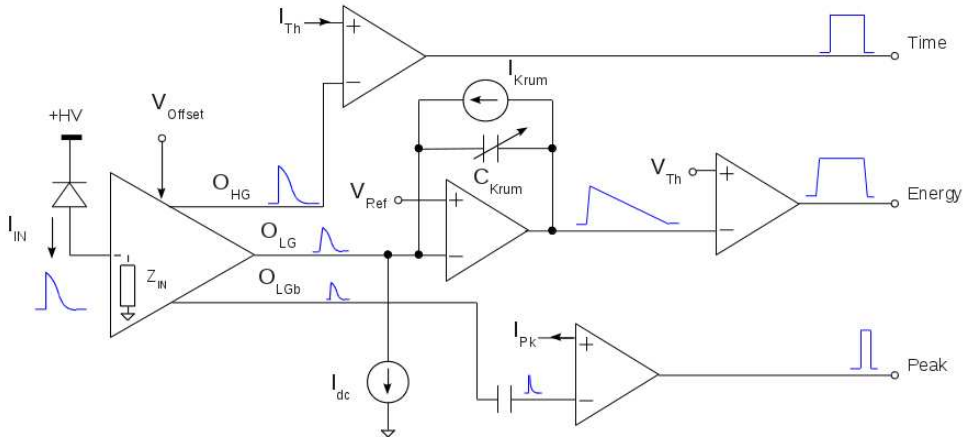

Figure 6: Blocs del prototip

La detecció d'apilament és una novetat respecte altres implementacions i ajudarà els algoritmes de post-processat.

Un sistema de control lent permet ajustar tots els voltatges i corrents de polarització i operació (llindars dels comparadors, tensió en el node d'entrada, etc...) i està inclòs en el prototip.

Temps sobre Llindar Linial (TOT)

El Temps sobre Llindar o Time Over Threshold (TOT) és un mètode de processat en el qual una senyal analògica es compara amb un valor (llindar) fixe per obtenir una senyal digital representant l'alçada de la senyal analògica. Mesurant l'amplada de la senyal digital de sortida hauríem de poder estimar la entrada. Els sistemes TOT són molt simples i útils per a sistemes multicanal ja que redueixen recursos i consum. Però normalment presenten una linealitat molt dolenta.

El comportament no lineal del TOT dependrà del processat de la senyal. Per exemple si un filtre Gaussià s'aplica, l'entrada es pot aproximar a un

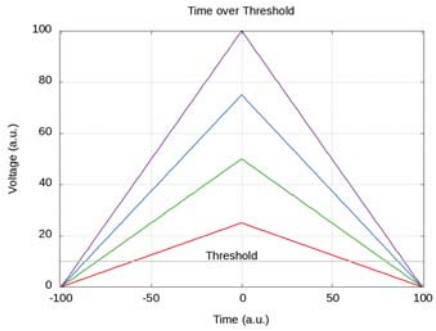

Figure 7: Entrada TOT

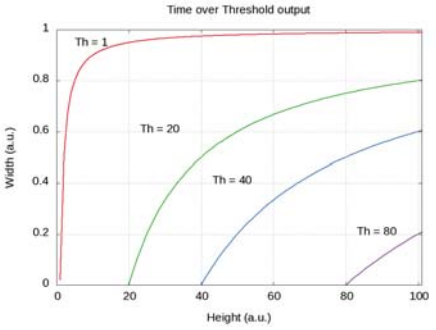

Figure 8: Sortida TOT per una entrada triangular

triangle. Utilitzant aquesta entrada [48] la no linealitat resultant es pot observar clarament depenent del valor llindar (a les figures 7 i 8). En alguns casos s'han utilitzat llindars dinàmics per evitar aquests efectes [48], però si s'aconsegueix una senyal amb un temps de pujada molt ràpid i una baixada lineal el resultat de la mesura hauria de ser molt millor.

Utilitzant les propietats de la senyal del SiPM ens podem aproximar a la senyal desitjable a l'entrada. Utilitzant un integrador amb una corrent constant de descàrrega abans d'un comparador s'hauria d'obtenir un TOT lineal. L'esquema bàsic es pot veure en la figura 9. Una tècnica molt similar s'ha utilitzat en altres circuits de lectura de sensors [49],[50].

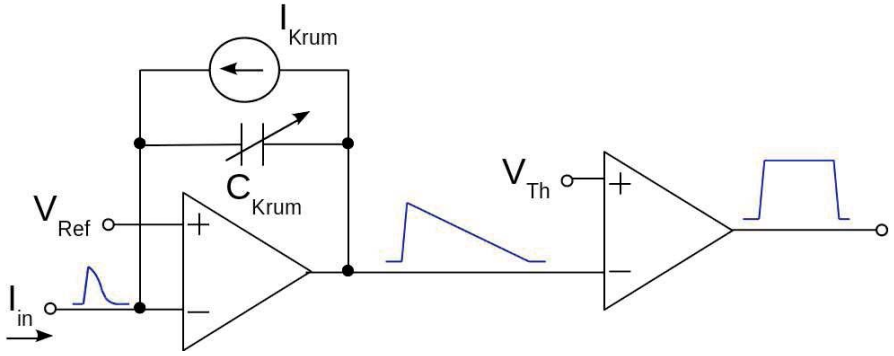

Figure 9: Esquema TOT lineal

Idealment el resultat del TOT es pot calcular fàcilment mitjançant la fórmula 2, tenint en compte com a entrada la càrrega (Q). Degut a que

el llindar (V_{Th}), la capacitat de realimentació (C_{Krum}) o la corrent de descàrrega (I_{Krum}) són constants la mesura haurà de ser lineal respecte Q. Els elements que introdueixen no linealitats seran el temps del flanc de pujada i la baixada de la senyal. Aquests efectes seran molt majors per senyals relativament petites en amplitud (petites per un sistema PET) o per a corrents de descàrrega molt petites.

$$T_{TOT} = \frac{Q}{I_{Krum}} - \frac{V_{Th}C_{Krum}}{I_{Krum}} \tag{2}$$

Una de les avantatges més importants d'aquesta estructura és la flexibilitat. Canviant la capacitat de realimentació i la corrent de descàrrega ens podem adaptar als requeriments de temps / resolució i corrent d'entrada de l'aplicació desitjada.

En la següent figura es poden observar unes simulacions de linealitat utilitzant una senyal d'entrada el més pròxima a la realitat (mesurada en un sensor amb un centellejador i una font radioactiva Na^{22}). La primera gràfica mostra la corrent d'entrada, la següent la tensió de sortida de l'integrador i finalment la sortida del comparador digital abans de l'error de linealitat per a cada punt.

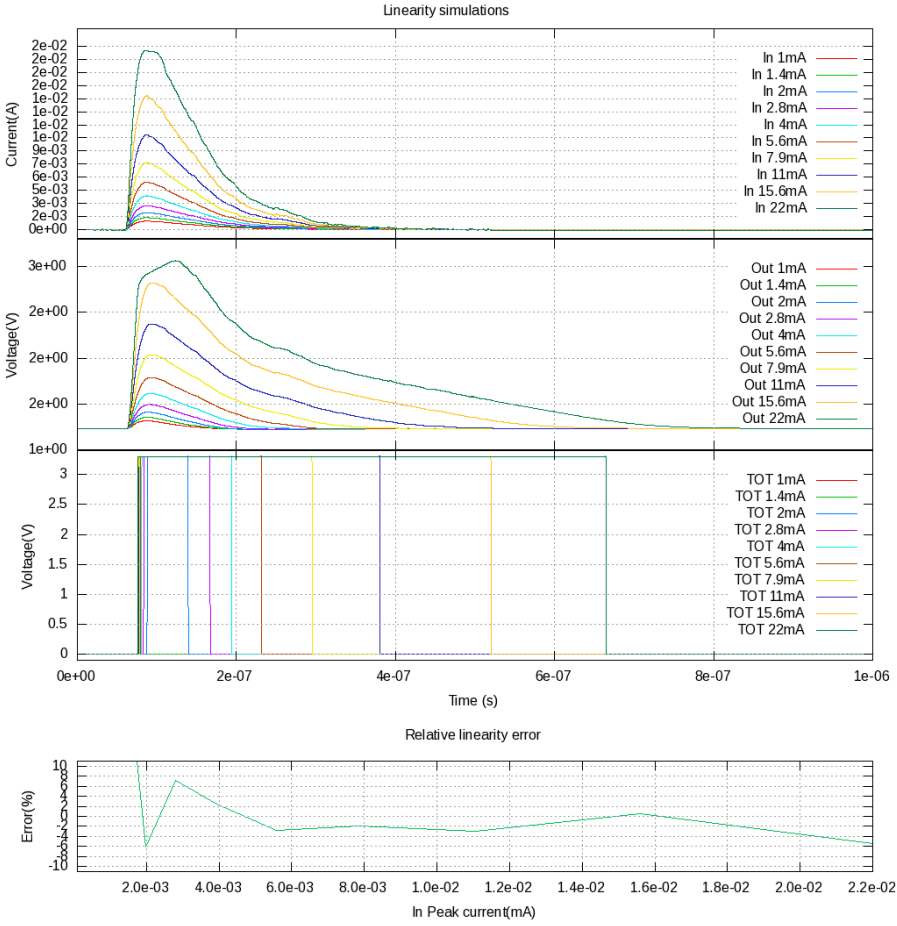

Figure 10: Simulació de linealitat

Resultats

El prototip del FLEXTOT es va rebre l'Octubre del 2012, amb 30 mostres encapsulades en un format QFN64 i 10 mostres sense encapsular. Mentre es realitzava la fabricació es va dissenyar un sistema de test per tal de mesurar el més ràpidament el màxim de característiques possibles del prototip.

Sistema de test

El sistema de test (en la figura 11) es basa en l'apilament de tres circuits impresos amb tots els elements necessaris; des del sensor fins a la comunicació de dades a un ordinador. L'únic element no inclòs és la font d'alt voltatge ($<$ 100V)necessària per alimentar els sensors. La següent electrònica es troba en els diferents circuits (de dalt a baix);

- Sensor: en aquest circuit es poden soldar diferents sensors. El sensor es connecta directament al següent circuit. Una variant amb un circuit d'injecció es pot utilitzar per la calibració amb una corrent coneguda a l'entrada.

- Circuit Analògic: en aquest circuit bàsicament hi ha el prototip amb algun regulador, capacitat de desacoblament i resistències de protecció. També incorpora un parell d'amplificadors per a poder extreure senyals de prova directament a l'oscil·loscopi i interruptors d'alta freqüència (SPDT) per a desconnectar les entrades dels canals.

- Circuit Digital: en aquest circuit hi ha una FPGA de baix cost (Altera Cyclone III, EP3C) i un circuit de comunicacions FT2232 que es connecta al port USB d'un ordinador. Utilitzant aquest sistema es pot controlar tots els elements del circuit i del prototip i realitzar una adquisició de la sortida del prototip (amb una resolució de 5ns en la mesura de l'amplada del pols digital).

Les alimentacions VDDA i VDDD s'alimenten a 3.3V. El consum mig és de 10.7mW per canal o 7.7mW de consum analògic (excloent la potència de l'alimentació digital que inclou les cel.les estàndard, els comparadors ràpids i alguns convertidors digitals / analògics).

Un element important per evitar canviar la forma de la senyal d'entrada i maximitzar la corrent d'entrada és la impedància d'entrada. La mesura realitzada compleix els resultats esperats; amb el comportament inductiu esperat la impedància es manté a valors baixos (34Ω) fins a uns 200MHz.

Figure 11: Sistema de test

Per tal de simular la senyal generada pels SiPM s'ha dissenyat un circuit que substitueix el dels sensors. Bàsicament es tracta d'un amplificador seguit d'un acoblament en alterna i una resistència en sèrie per mesurar el corrent. El pic es genera mitjançant un generador arbitrari per simular la forma de la senyal del SiPM.

Linealitat

Per tal d'obtenir una millor linealitat en l'amplitud de la senyal injectada s'ha col·locat un atenuador programable entre el generador i la entrada del circuit. El generador es configura amb una amplitud màxima de sortida i es va atenuant mitjançant l'atenuador programable. Aquest sistema permet una millor linealitat en la senyal d'entrada que simplement variar l'amplitud en el generador.

Degut als paràmetres de configuració del prototip alguna calibració és necessària per adaptar-se al rang de senyals d'entrada. Alguns exemples de les corbes de calibració resultants ens poden veure en els 16 canals en les figures 12, 14 per una constant de temps de l'entrada de $\tau \approx$36ns i en les figures 13, 15 per una constant de temps $\tau \approx$110ns.

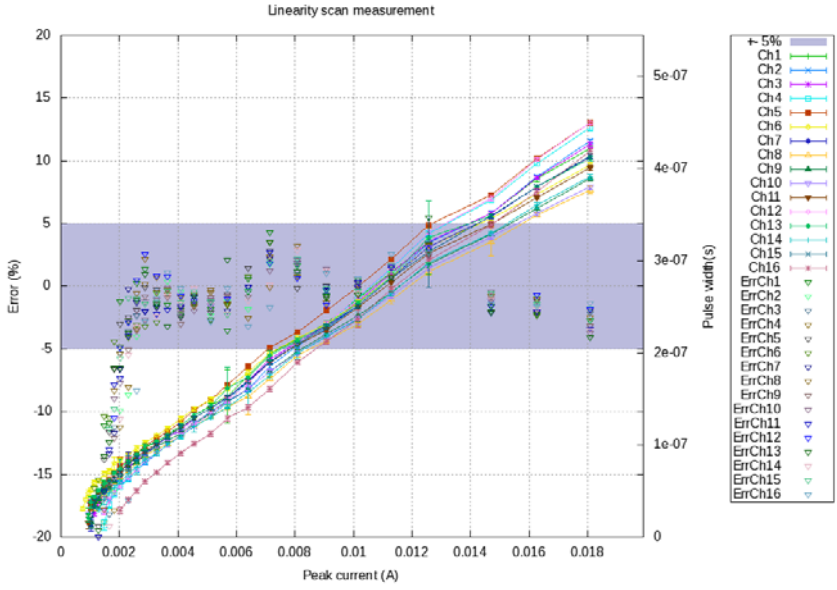

Figure 12: Linealitat $\tau \approx 36$ns, 18mA de rang

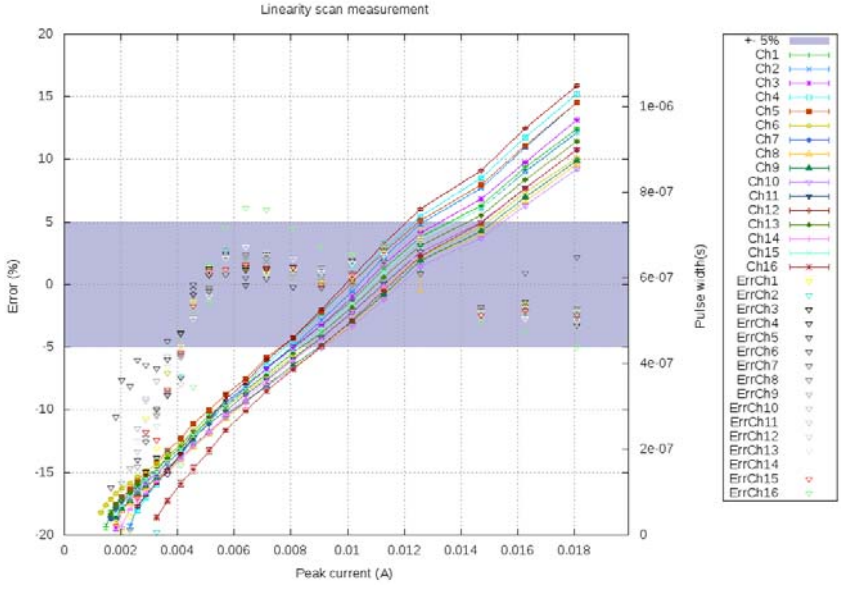

Figure 13: Linealitat $\tau \approx 110$ns, 18mA de rang

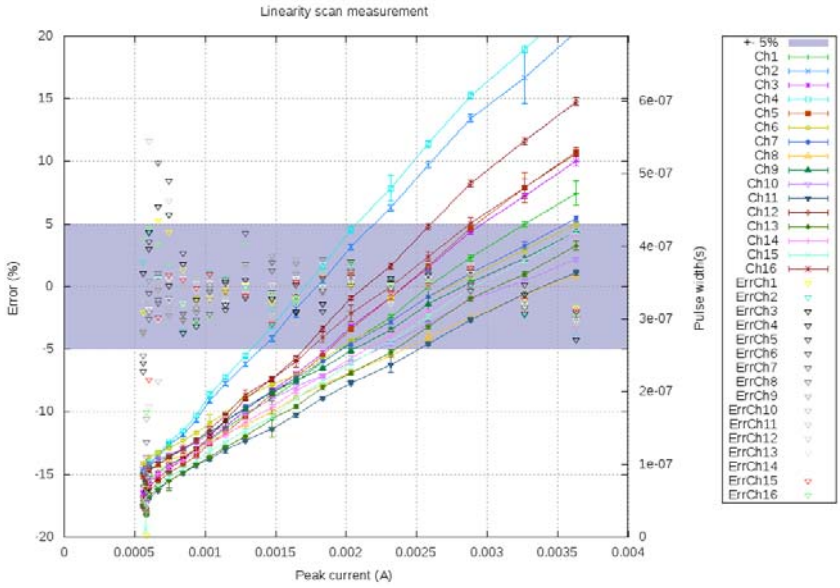

Figure 14: Linealitat $\tau \approx 36$ns, 3.5mA de rang

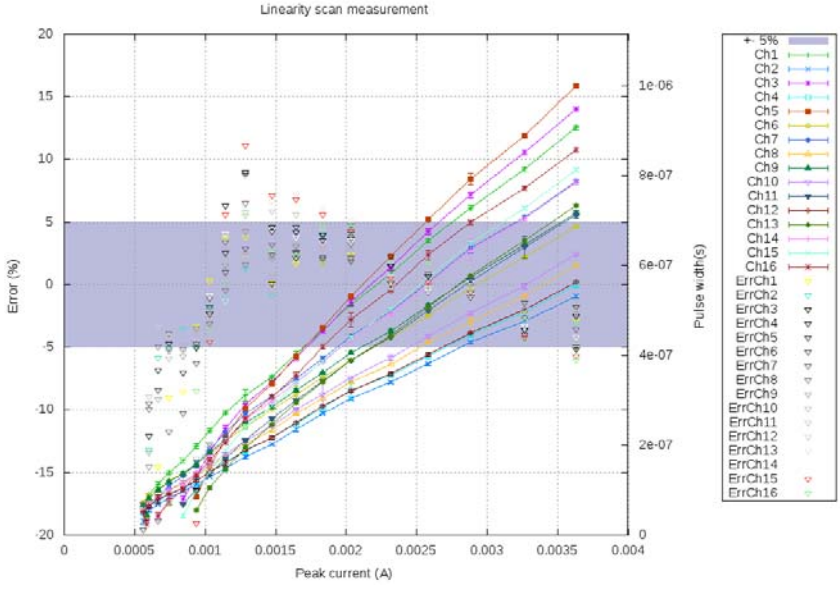

Figure 15: Linealitat $\tau \approx 110$ns, 3.5mA de rang

Mesures amb SiPM

Després de caracteritzar elèctricament el prototip es col·loca un sensor real connectat al sistema de test. La senyal d'entrada tindrà un temps realista i evitarà qualsevol efecte del circuit d'injecció. Amb aquesta configuració es realitzen algunes mesures.

Fonts Radioactives

Per caracteritzar amb una senyal el més propera a la realitat s'utilitzen diferents fonts radioactives. Un petit cristall LSO (de 2x2x8 mm^3) es col·loca sobre un canal del detector (de 3x3 mm^2) i llavors una font radioactiva a prop. Primerament es mesura l'espectre del cristall sol per tal que es pugui restar a posteriori (el material del cristall té una emissió de partícules de diferent energia que generen llum).. Les fonts utilitzades són Na^{22}, Co^{60} i Cs^{137}, i els resultats es resumeixen a la figura 16.

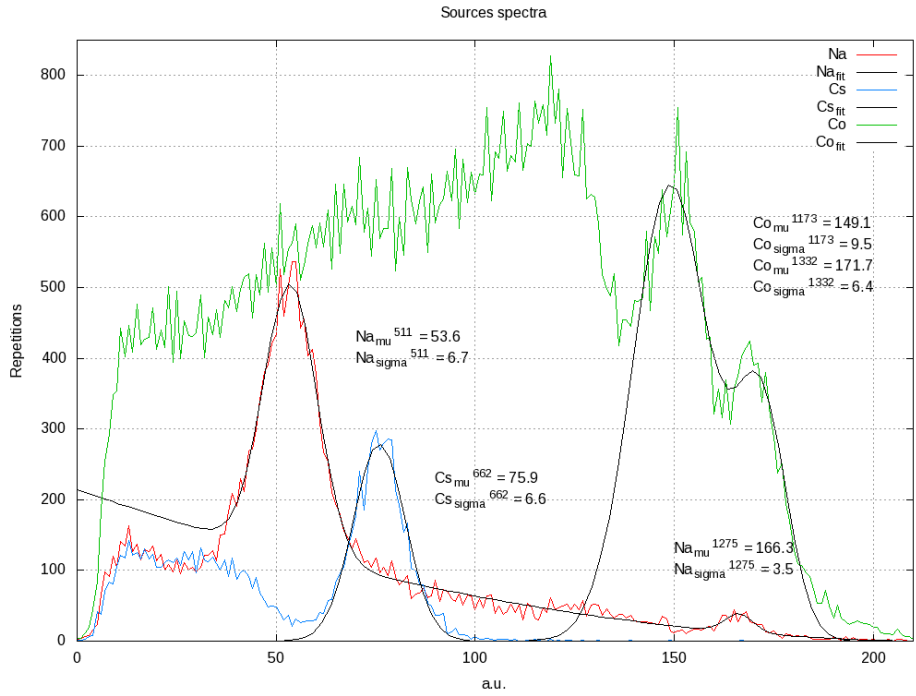

Figure 16: Mesura de l'espectre Na^{22}, Co^{60}, Cs^{137}

Es pot observar la bona linealitat del sistema en tot el rang. Utilitzant la posició dels dos pics més externs s'obté una constant de calibració. Utilitzant aquesta constant es converteixen les resolucions (σ) mesurades a energia. La resolució calculada es resumeix a la taula 6. Com s'esperava millora lleugerament al augmentar l'energia.

Font	**keV**	μ **(comptes)**	σ **(comptes)**	**Res.(%)**
Na^{22}	511	53.3	7.1	9.6
	1275	166.3	3.5[1]	-
Cs^{137}	662	75.9	6.6	6.9
Co^{60}	1173	149.1	9.5	5.6
	1332	171.6	6.4[1]	-

[1] Caldria més estadística

Table 6: Mesures de les Fonts radioactives

Mesura de coincidència temporal

Per obtenir una primera estimació de la resolució temporal del sistema complet s'ha reproduït un sistema de coincidència en el laboratori. Dos sistemes de test amb un sol canal es col·loquen un davant de l'altre. Sobre els dos SiPM es situen cristalls (s'han probat LSO i LYSO) i una font radioactiva de Na^{22} enmig. La sortida de temps i les d'energia dels dos canals es capturen amb l'oscil·loscopi.

Utilitzant l'espectre extret dels dos canals es seleccionen els esdeveniments dins del rang d'energies d'interès. Aquesta finestra es correspon al voltant dels 511keV ($\pm 1\sigma$). Una vegada seleccionats els esdeveniments d'interès es representa el retard entre les dues sortides temporals dels dos sistemes de test. El resultat final es mostra en l'histograma de la figura 17 obtenint una resolució temporal per sota dels 300ps FWHM ($\approx$115ps rms).

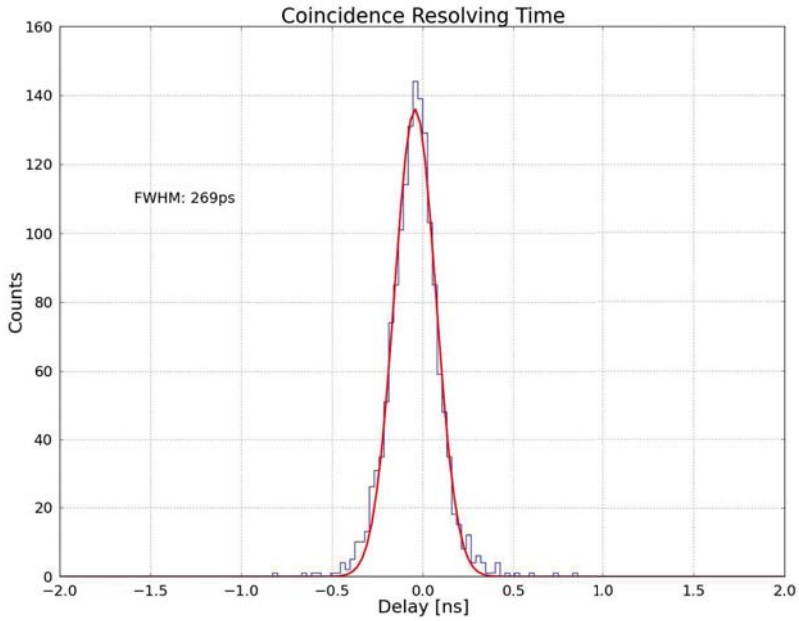

Figure 17: Mesura de coincidència

Mesures en un sistema complet

Algunes mesures preliminars s'han realitzat al CIEMAT amb un sistema que emula un sistema PET complet. Es tracta de dos sensors situats a dos costats d'una plataforma giratòria (d'aquesta manera no cal un anell complet de detectors ja que es fa girar la mosta). Al centre es situa una font radioactiva (Na^{22}) i una vegada adquirides les dades s'apliquen els algoritmes de reconstrucció d'imatge. Un resultat de la imatge generada i la mesura de posició es pot veure en la figura 18.

En aquest cas s'han realitzat dues mesures, una primera amb una sola font radioactiva (de 0.25mm de diàmetre) i superposant la mesura en dues posicions, i una segona amb dues fonts radioactives (de 1mm de diàmetre) mesurant al mateix temps. La precisió en la mesura de posició resultant és de pocs milímetres com s'espera.

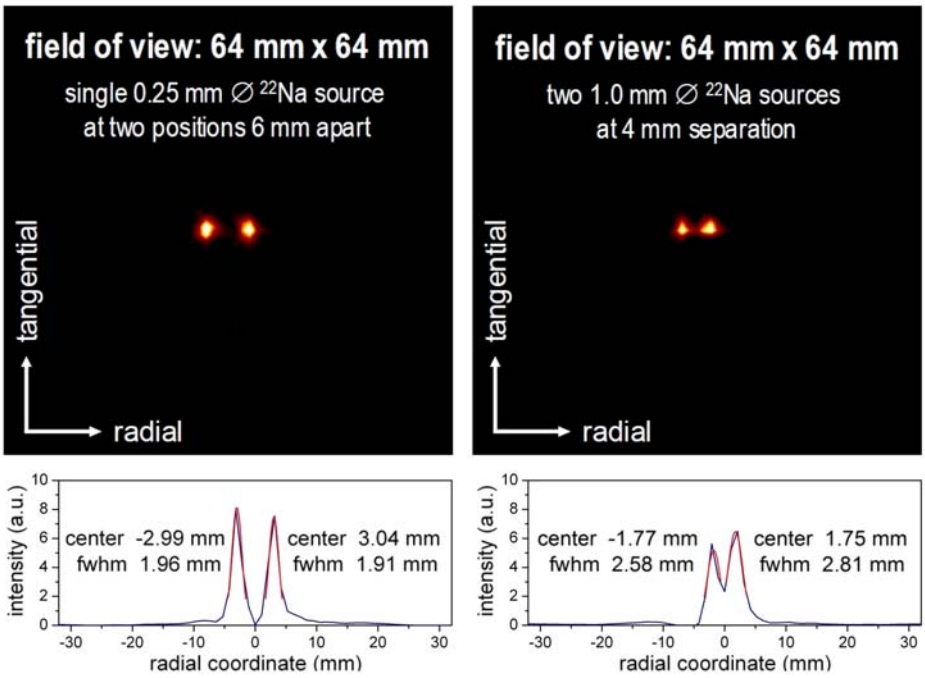

Figure 18: Mesura en un sistema complet

Disseny per al Tracker SciFi

En el cas del disseny per a detectors de partícules cal que es compleixin unes restriccions temporals molt diferents (comparant amb PET). La reutilització i implementació de la etapa d'entrada en una nova tecnologia i amb unes característiques temporals prou diferents són un repte per al disseny. En aquest cas es tracta d'una tecnologia més moderna amb una tensió d'alimentació molt inferior i completament CMOS.

El tracker és un sub-detector de LHCb que indica el camí que segueixen les partícules amb càrrega elèctrica que passa a través del detector i interacciona amb el material. Les partícules deixen una petita senyal elèctrica al moure's pel detector. Els detectors d'aquest tipus normalment utilitzen tires de silici o detectors gasosos (*straw tubes*). Una vegada s'ha generat, s'adquireix i processa i s'envia a un ordinador que reconstrueix la trajectòria de les partícules.

La tecnologia per a l'IT i l'OT es basarà en fibres centellejadores generant una senyal de llum i transportant-ne els fotons des d'on es generin fins a l'extrem on hi haurà els sensors. En el primer esborrany sobre com serà el detector es preveu utilitzar fibres de 2.5m cobrint almenys la zona central. Tot el detector es construirà mitjançant 3 panells cadascú dels quals amb 3 plans inclinats entre ells ($\leq 5^{o}$) per crear els plans X-U-V-X. Cada pla està construït amb 5 capes de fibres de 250μm de diàmetre i 2.5 m de llargada.

Un dels problemes més importants per a fer realitat aquest detector és la construcció dels mòduls de fibres. Algunes noves tècniques s'estan provant i desenvolupant per a la seva fabricació.

Per a dissenyar la electrònica de processat s'ha iniciat una col·laboració entre Barcelona i Clermont Ferrand, oberta a qualsevol altra institució de LHCb, per dissenyar el "*low **P**ower **A**sic for the s**CI**ntillating **FI**bres tra**C**ker*" PACIFIC.

S'han estudiat diferents alternatives per al processat, però sembla que la més senzilla serà la solució base, incorporant un canal amb un preamplificador, *shaper*, integrador mostrejat i ADC.

Resum de les especificacions

En la següent taula es pot veure un resum de les especificacions que haurà de complir la electrònica;

Paràmetre	Valor	Unitat
Canals	64 o 128	-
Potència	0.5 o 1	W
Encapsulat	BGA	-
Resolució temporal	25	ns
Constant de temps sensor	de 40 a 300	ns
Rang dinàmic	0-64	micro-cel·les
Temps d'arribada de la senyal	0-15	ns
Soroll referit a l'entrada	$\leq$143	$\frac{pA}{\sqrt{Hz}}$

Table 7: Especificacions del PACIFIC

Arquitectura

L'arquitectura del canal proposat per al PACIFIC es pot observar en la figura 19. Tot i que s'estan estudiant altres alternatives, específicament una digitalització ràpida seguida per un processat digital de la senyal, la solució més fàcil sembla realitzar un *shaping* de la senyal i integrar durant 25ns. Al no haver-hi temps mort entre mostra i mostra caldrà un doble integrador entrellaçat de forma que un estigui capturant al temps que l'altre torna a les condicions inicials. Després de l'integrador un convertidor analògic / digital generarà els valors representant l'amplitud a 40MHz. Finalment un enllaç sèrie (probablement diferencial seguint un estàndard) enviarà les dades a alta velocitat. Per aquest últim pas caldrà algun tipus de multiplicador de freqüència (com per exemple un PLL en la figura).

Algunes polaritzacions comunes i un control digital de les tensions, corrents i paràmetres d'operació també hauran d'estar integrats. Així que s'hauran de dissenyar blocs com convertidors digitals analògics (en tensió i corrent), resistències variables i capacitats variables, connectats a algun bus de control.

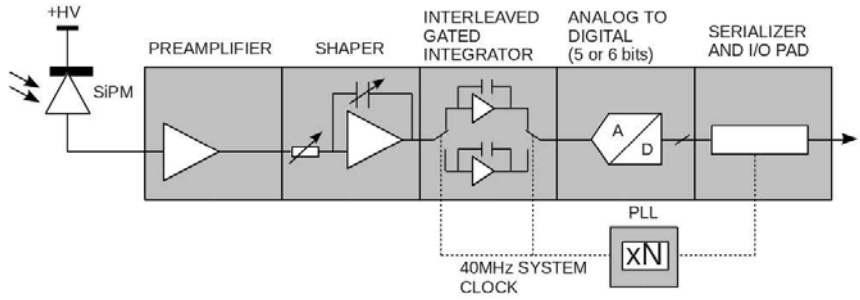

Figure 19: Blocs del canal del PACIFIC

Pre-amplificador

La etapa d'entrada és un amplificador en mode corrent amb la connexió directa al SiPM. L'objectiu és aconseguir les següents especificacions del bloc:

- Ample de banda ($\approx$ 250MHz).
- Baix consum ($<$ 2mW, màxim de 8mW/canal en tot l'ASIC).
- Baixa impedància d'entrada ($20\Omega < \mathrm{Z}_{in} < 40\Omega$).
- Tensió controlada al node d'entrada ($\approx$ 1V de rang).
- Soroll referit a l'entrada $\leq 143\frac{pA}{\sqrt{Hz}}$

El circuit utilitzat com a referència per aconseguir aquestes característiques es pot veure en la figure 20. La etapa d'entrada es basa en la mateixa nova estructura amb una realimentació doble amb alguna petita variació per adaptar-se a una tecnologia més moderna (IBM 0.13μ m).

Aquest circuit permet una impedància d'entrada baixa per aconseguir la màxima corrent d'entrada i així la millor resolució temporal. HF_{FB} és el llaç de realimentació d'alta freqüència que manté la impedància d'entrada baixa i constant (fins a certa freqüència). El segon camí LF_{FB} és un llaç de realimentació a més baixa freqüència i proporciona un valor de contínua (V_{offset} in figure) al node d'entrada utilitzant el curtcircuit virtual de l'amplificador que regula el seguidor.

El disseny s'ha realitzat tenint en compte que el node dominant ha de ser el d'entrada degut a la gran capacitat paràsita del detector. D'aquesta manera la estabilitat es veurà encara més reforçada al connectar un sensor amb una gran capacitat paràsita a l'entrada.

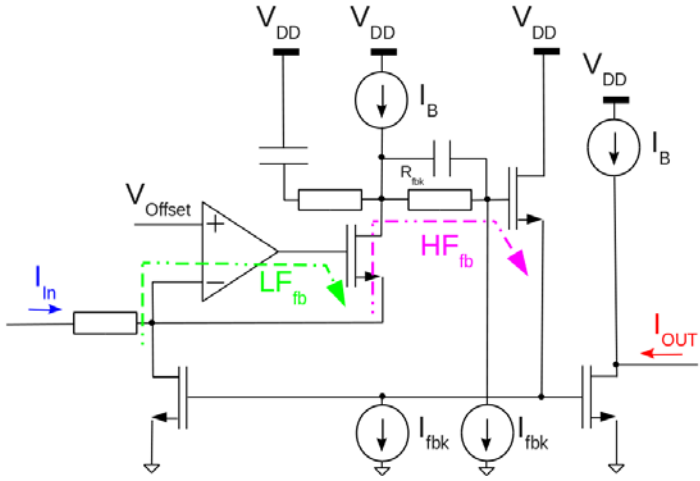

Figure 20: Etapa d'entrada PACIFICr1

Conclusions

En aquesta tesi s'ha descrit de forma detallada les propietats del sensor i els requeriments necessaris per a dissenyar la electrònica en dos àmbits ben diferenciats; física mèdica (PET) i detectors de partícules (SciFi Tracker). Prenent com a punt d'inici les implementacions realitzades anteriorment i proposant una nova solució amb una etapa amb doble realimentació per aconseguir un gran rang dinàmic i la possibilitat de configurar fàcilment el sistema. Un model del comportament del sensor s'ha utilitzat i ha sigut molt útil per al disseny de la electrònica. Els dos circuits dissenyats s'han comentat detalladament per a diferents tecnologies.

Els objectius principals per al sistema PET s'han complert amb el disseny d'una arquitectura multicanal i la connexió directa als SiPM amb el processat analògic. El prototipus s'ha dissenyat i testejat. L'ajust de voltatge al node d'entrada permet controlar el punt d'operació del sensor, mentre que els diferents camins de senyal permeten la realització de les diferents mesures amb una mesura de temps d'una resolució excel·lent, una mesura adequada de la energia i la detecció de l'apilament d'esdeveniments. Així doncs la etapa d'entrada compleix amb tot el que es demanava del circuit. Després del disseny i el test ja tan sols quedarà comprovar el seu funcionament en un detector real.

Les restriccions en el disseny del PACIFIC encarà s'estan concretant, i el primer prototipus descrit ha de servir com una primera etapa. El circuit dissenyat segueix la mateixa estructura que el de PET però portat a una tecnologia més moderna i simplificat per l'aplicació. Una vegada fabricat caldrà comprovar les seves prestacions. Mentre s'avança en el disseny de la resta d'etapes per tal de complir el calendari fixat.

Summary

The aim of this thesis is to present a solution for the readout of Silicon Photo-Multipliers (**SiPMs**) arrays improving current implemented solutions. With this purpose a novel current mode input stage has been designed and tested. In first place focusing in general applications for medical imaging (Positron Emission Tomography, **PET**) and then using the same topology for a more constrained design in higghe energy physics (upgrade of Tracker detector at **LHCb** experiment).

SiPM are recently developed electronic devices[1] with photon counting capabilities improving current state of the art detectors regarding high voltage requirements, signal gain and magnetic field tolerance, while keeping at the same time excellent gain and timing characteristics, and a wide dynamic range. They are semiconductor devices still under development to improve yield, reduce dark count, provide multi-channel architectures and increase light sensitivity spectrum.

A Front End Readout Application Specific Integrated Circuit (**ASIC**) for SiPMs is presented with the following features: wide dynamic range, high speed, multi channel, low input impedance current preamplifier, low power consumption, SiPM voltage control, and timing, charge and pileup signal output.

The pre-amplifier input stage includes a novel circuitry with double feedback loop to lower input impedance at the same time it keeps a constant DC value at the input node over the full range of operation and keeping the desired bandwidth.

Silicon Photo-Multipliers

A silicon photo-multiplier is a device formed by hundreds of micro-cells in parallel. Each micro-cell is an Avalanche Photo Diode (APD) working in Geiger mode, with their own quenching resistor to avoid destruction of the device. APDs behaviour is well known and has been studied during many years from 1960 [7]. All those micro-cells are combined in one single output (connected in parallel). The result is an output similar to the one produced by a PMT, but with a somehow discrete analog output (since each cell releases a fixed amount of charge when fired).

In the same way as the APDs the first pairs are generated by photoelectric effect and then multiplied inside the silicon. But in this case the multiplication is an avalanche, produced over breakdown voltage. In a normal multiplication process electrons are drawn through the high field region and create additional electron-hole pairs. The electrons continue in the same direction but holes are attracted in the opposite direction. At a sufficient high field values (over breakdown voltage) the holes can also multiply and, since hole multiplication also produces additional free electrons, this process leads to a runaway. To avoid a destructive effect a resistor (quenching resistor) in series is connected to each APD so the voltage it's dropped when it reaches some current limit. This combination of APD and quenching resistor is the micro-cell. The resulting gain is similar to the PMT on the order of 10^5 to 10^7.

SiPM detection capabilities are measured as it's **Photon Detection Efficiency (PDE)**. It's nothing more than joining the effects produced by the area lost between micro-cells and Quantum Efficiency. Since there is some area not able to detect incoming light a **Fill Factor (FF)** is defined as in 3. The resulting PDE will be calculated easily using formula 3 with P_{start} being the probability of an electron-hole pair to start an avalanche. Some techniques used to improve crosstalk between micro-cells (such as adding trenches) can degrade this value. The reduction of micro-cell size will also make a worse fill factor.

$$FF = \frac{Total\ \ Device\ \ Area}{Sensible\ \ Area} \quad \rightarrow \quad PDE = FF\ \ x\ \ QE\ \ x\ \ P_{start} \tag{3}$$

Several measurements and comparisons between different production devices can be found in literature[8] with deep description of different effects[9]. SiPM offer a linear output depending on incident light in a range of input photons. According to [10] the response of a SiPM can be extracted with equation 4, where m is the total number of cells of the device and ε the photon detection efficiency.

$$N_{cells fired} = m * \left(1 - e^{-\frac{N_{photons} * \varepsilon}{m}}\right) \tag{4}$$

SiPM devices have an important temperature coefficient which modifies it's breakdown voltage thus affecting it's gain. The temperature coefficient is different depending on manufacturing process but existent in all devices. If an array of devices should be compensated without modifying the general

polarization voltage some channel by channel polarization should be provided. Non uniformities between devices in array should also compensated using the same mechanism; SiPMs offer a very linear gain versus voltage characteristic permitting to compensate non uniformities between different sensors (those non uniform effects are much sensible at small over-voltages operation).

After Pulsing is a known effect which consists on the generation of a spontaneous peak output after a first peak. It is due to the trapping of some charge in the semiconductor defects. This charge has some probability to be released afterwards. If this charge is released will start a new avalanche. Typical release times range from few ns to several hundreds of ns. The first released charges (few ns) does not affect the signal because the micro-cells are not fully recharged, but will increase recovery time. Working at low temperatures will make release of this trapped charges more slow, so the after pulses will be more noticeable.

Dark Count is one of the most important drawbacks of the SiPMs. Dark count is generated by spontaneous thermally generated carriers. Those carriers can then generate an avalanche in the micro-cell that will be identical to a signal generated by a photon. The name of dark count comes from the fact that this signal will continue being generated without any illumination at all. The average number of avalanches in some time without signal would give the expected dark count rate (normally in Hz).

A summary of advantages and drawbacks of SiPMs are collected in table 8.

Advantages	Drawbacks
High quantum efficiency	Radiation hardness
Magnetic field insensitivity	Low PDE
Robust and small	Dark count
Low voltage operation (from 20V to less than 100V)	
Arrays available	

Table 8: SiPM advantages and drawbacks

Scintillators

A scintillator is a material that exhibits emission of light (not resulting from heat) when excited by ionizing radiation. This radiation is composed of particles that individually carry enough kinetic energy to liberate an electron from an atom or molecule, ionizing it. When hit by an incoming particle the scintillating material absorb its energy and re-emit the absorbed energy in the form of light. Depending on material the excited state could be metastable, so the relaxation back out of the excited state is delayed some time (from a few microseconds to hours). First scintillator usage dates at the beginning of 20^{th} century[13] but gained attention in 1944, when Curran and Baker replaced the naked eye measurement with the newly developed PMT. This was the birth of the modern scintillation detector.

In this modern scintillation detectors, the first part in the path of the ionizing particle are the scintillating crystals used to convert it into a light burst. Then those light burst are converted into electrical current by a transducer (PMT, APD or SiPM) and processed. This crystals are not ideal and present an important timing spread in the photon emission process. Once the photons are produced they should arrive to the electronics following different paths which will also increase the time spread in the detector itself, highly affected by the crystal dimensions[14].

Some of the desired properties of scintillators are high density, high speed response, good linearity, radiation hardness and low cost. High density reduces the material size of showers for high-energy γ-rays and electrons and the Compton scattered photons are reduced for low energy γ-rays. High speed response, with reduced decay times, leads to better resolution in measurements and also identification of the type of particle measuring decay time (different times are generated depending if they are γ-rays or ions) and also useful to avoid dead time. High speed in fast rise time will produce better timing measurements. Good linearity is mandatory for the measurement of energy in some range. Radiation hardness is needed to allow long life time of the detector since it could be placed in hostile environment (specially in particle detectors). Finally cost is an important factor since most crystal scintillators require high-purity chemicals and sometimes rare-earth metals that are expensive.

Typical properties of some inorganic scintillating materials are summarized in table 9. Organic ones present much lower density (around 1 g/cm^3) and lower light emission (around 50% of NaI(Tl)).

Table 9: Inorganic scintillators properties summary

Scintillator Material	**Density (g/cm^3)**	**Wavelength at max.(nm)**	**Refractive index**	**Decay time(ns)**	**Light yeld (ph/MeV)**
NaI(Tl)	3.67	415	1.85	230	38000
CsI(Tl)	4.51	540	1.80	680,3340	40000,25000
$Bi_4Ge_3O_{12}$	7.13	480	2.15	300	8200
BaF_2	4.89	220,310	1.56	0.6,630	1500,9500
CeF_3	6.16	310,340	1.68	5,27	4400
$YAlO_3$(Ce)	5.37	370	1.95	27	18000
Lu_2SiO_5(Ce)	7.4	420	1.82	47	25000
$LaBr_3$(Ce)	3.79	350	1.9	27	49000
BC-400	1.03	420	1.58	2.4	10000
BGO: $Bi_4(GeO_4)_3$	7.13	480	2.15	300	5700
LSO: $Lu_2(SiO_4)O$:Ce	7.4	420	1.82	42	28500
GSO: $Gd_2(SiO_4)O$:Ce	6.71	440	1.85	60	7600
LYSO: $Lu_{1.8}Y_{0.2}(SiO_4)O$:Ce	7.1	420	1.81	40	40000

SiPMs Applications

Silicon Photo Multipliers could be used in any application where a fast measurement of a small signal is needed. Today's main applications are the detection of the gamma rays emitted by a radionuclide in the body to detect accumulation in different areas of the body (for example in Positron Emission Tomography scanners) or particle detectors with the help of scintillating material to produce light from the incoming particles (for example in Scintillating Fibre Tracker at LHCb).

Positron Emission Tomography

Positron Emission Tomography (PET) is a nuclear medical imaging technique to produce three-dimensional images of functional processes in the body. PET systems are based on detection of gamma rays pairs emitted indirectly by a radionuclide (tracer) introduced into the body. Data produced with the concentration of the gamma rays pairs and their arrival time is used in computer analysis to produce 3D images of their activity inside the body. Modern devices complete the image performing a second scan with CT-X-ray in the same machine although a combination with MRI (Magnetic Resonance Imaging) would be preferred due to the lack of added irradiation of the patient and better contrast in soft tissues. A key element to the development and usage of PET systems is the parallel evolution of radiopharmaceuticals. In particular the development of several compounds (for example 2-fluorodeoxy-D-glucose, 2FDG) to determine it's concentration in different organs by the scanner. First scanners relied on two 2 dimensional arrays of detectors, but soon it was clear that a logical distribution for full readout detectors was to place it forming a ring around the patient. A schematic view of the system is shown in figure 21.

The detector block is usually formed by scintillator crystals (converting gamma ray into light bursts) followed by photomultiplier tubes (converting light burst into current pulses) and readout electronics (with amplification and time tagging of the input signal). The final spatial resolution of the hardware depends on the size of the crystals and time accuracy of the whole system.

Combination of PET scans with CT-X-ray or MRI giving both anatomic and metabolic information in the same scanner is very useful since patient won't move between scans and will make easier to correlate both images. This is important in structures with anatomic variations or moving organs (outside the brain).

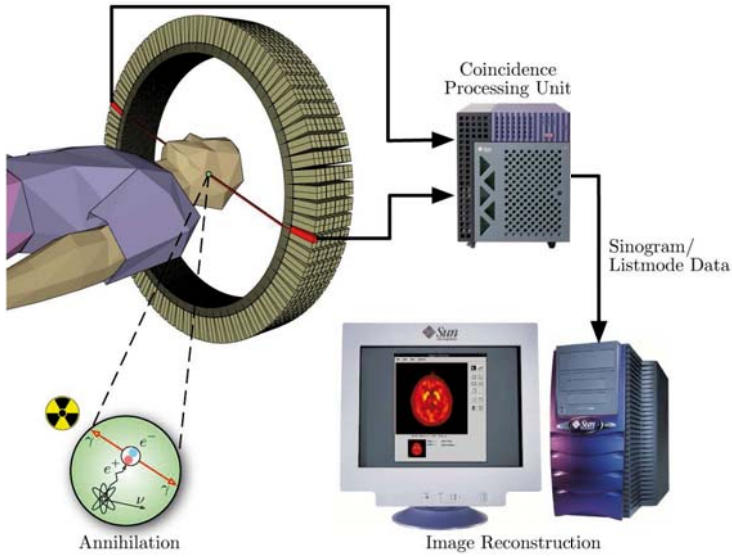

Figure 21: Schema of PET imaging system

The raw data generated by PET scanner are a list of coincidence events representing near-simultaneous detections of annihilated photons (in a 180 degrees placed detectors). Each coincidence represents a line in space connecting the two detectors (line of response, LOR). Coincidence events can be gropued into projection images, called sinograms. Those sinograms are analogous to the ones produced by CT-X-ray scanners, but with much less statistics (at least three orders of magnitude less). As such PET data suffer from scatter and random events much more dramatically than CT-X-ray scans. In practice considerable pre-processing of the data is required.

PET systems will only accept as valid events the ones in the energy window produced by the gamma ray. This is around 511keV. If an event is around this energy and in coincidence with an other event at a 180 degree block then it will be an accepted event. All the rest is discarded. To avoid system bottlenecks it's important to take the decision if an event is saved or dropped as soon of possible in the detector chain.

Some crystals have spontaneous emission of light, emitting an spectra in the region of interest. As an example Saint Gobain's Prelude 420[24] is a lutetium based scintillator with a radioactive isotope generating 3 gamma ray cascade of 307, 202 and 88 keV, being the most probable a 597keV deposited in the scintillator. This can be useful for offline calibrations of the detector (for example LSO and LYSO crystals).

Time Of Flight

Time of Flight (TOF) is the name given to several methods to measure the time it takes for a particle to travel some distance. This measure should be used as a way to determine some property of the medium (velocity) or to know more about the particle. The object could be detected directly or indirectly. In PET systems the relevant events are detected easily using coincidence of two particles of 511keV at 180 degrees. It's an indirect measurement since particles generate some light and this is what is detected and processed. Since detectors (scintillator crystals) have a finite size (in 3 axis) the line where the event has been produced has some angular uncertainty (not an ideal line). If a time stamp is added on the two sides with time better than ns then the distance from the two detectors is also defined (the resolution will increase with the timing resolution). Using this technique the signal to noise ratio (SNR) of the events is improved, leading to less events needed for a given image quality.

CERN and LHC

European Organization for Nuclear Research or *"Conseil Européen pour la Recherche Nucléaire"* (CERN) was funded in 1954 with the aim to became a world leading institution in this research topic. It was built beside the French and Swiss frontier, close to Geneva. It's buildings and sites extent in both sides of the frontier, and also the tunnel constructed to hold the most powerful accelerator created up to date, the Large Hadron Collider (LHC). During it's history it has hold different accelerators and experiments leading to some discoveries and prizes. Today it has 20 countries as members of this international collaboration. The LHC is a proton-proton collider placed in the 27km ring previously build underground for the LEP machine.

LHCb

Large Hadron Collider beauty (LHCb) experiment is one of the ongoing experiments at CERN (Geneva). Shown in figure 22, LHCb is a forward spectrometer with a polar angle coverage of approximately 15 to 300 mrad in the horizontal bending plane and 15 to 250 mrad in the vertical non-bending plane. This geometry choice is motivated by the fact that $b\bar{b}$ pairs produced at the LHC are produced in a large proportion in the same direction, either forward or backward.

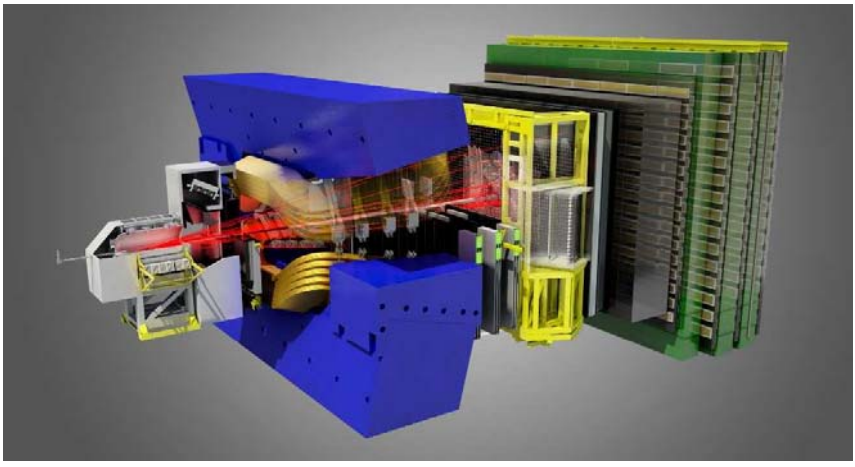

Figure 22: LHCb detector[a]

[a]Image courtesy of LHCb collaboration

Starting from the interaction point, at the left of figure 22, the LHCb tracking system consists of a silicon strip device surrounding the proton-proton interaction region (the Vertex Locator), a large area silicon strip detector (the trigger tracker, TT) located upstream of a dipole magnet which has a bending power of about 4 Tm, and a combination of silicon strip detectors and straw drift-tubes placed downstream of the magnet (the Inner Tracker, IT and the Outer Tracker, OT).

Scintillator Fibre Tracker

The current LHCb Tracker stations are composed of an Outer Tracker (OT) with straw tube detectors and an Inner Tracker (IT) with silicon strip detectors to cover the high-occupancy area near the beam pipe. A new technology for the IT upgrade, based on scintillating fibres, was introduced in the Upgrade Letter of Intent[6], with clear fibres carrying the photons from the inner region to the sensors placed outside the LHCb acceptance.

In the mean time, a new scintillating-fibre layout has been proposed (Central Tracker, CT), with 2.5 m long fibres covering the whole central region of the Tracker stations, from the LHC beam plane all the way to the top and bottom of the LHCb acceptance. In this option, the IT and several OT modules are replaced by the new scintillating-fibre modules. Tracking downstream of the dipole magnet with scintillating-fibre modules in the central region is being considered. In this new configuration, the existing outermost straw tube modules, four on each side, are kept as in the current LHCb detector and their electronics upgraded to allow readout at 40MHz. The central part (OT and IT) is replaced with scintillating fibre modules covering the full height of the detector. The upper and lower halves of the modules contain 2.5 m long scintillating fibres, separated with mirrors at the inner boundary and read out with Silicon Photomultipliers (SiPM) mounted outside the LHCb acceptance.

With this configuration, passive material in the detector acceptance is minimized and exposure to radiation is reduced for the SiPMs and FE electronics. One of the key development challenges will be to determine how the SiPM performance will evolve as a function of radiation dose and under what conditions these photon detectors will represent a viable solution for the LHCb CT. The radiation fluence at the SiPM location is expected to be of the order of $10^{12} n_{eq} cm^{-2}$. Besides previously described irradiation studies with 65 MeV protons and with neutrons from a PuBe source [6], SiPM samples have been placed in the LHCb detector at the bottom of the tracking stations during the 2011 data taking period.

The techniques for the production of fibre matrices are still under development for both methods presented in the LoI, namely winding fibres on a cylindrical surface of radius larger than 40 cm or on a long cuboid. Dummy fibre matrices have been produced with both methods. Recently, a 2.5 m long sample module has been fabricated on the cylindrical barrel with scintillating fibres of 0.25 mm diameter. The sample contained five layers of about 100 fibres each.

Specially designed SiPM array is undergoing to fit the mechanical size of the module with the minimum dead area possible. The prototypes from Hamamatsu and Ketek consist in 64 channels arrays with a common cathode configuration. With a total size of 0.23x1.32mm^2 per channel, 96 micro-cells and 57.5x55μm^2 micro-cell size. The 128 channels are constructed joining to dies of 64 channels with the edge polished, dead area between pixels is kept to the minimum with a value of 0.25mm between two arrays.

SiPM modelling

A reliable SiPM model is mandatory to produce accurate input signals for the electronics. A simple model [26] has been implemented and simulated using the standard SPICE tools in conjunction with the electronics. A general view of the circuit model can be seen in figure 23 with its parameters on table 10.

In this model [26] the different micro-cells in the SiPM are modelled as passive elements with the difference that the firing cells by some light have several more elements than the passive cells, acting as a load.

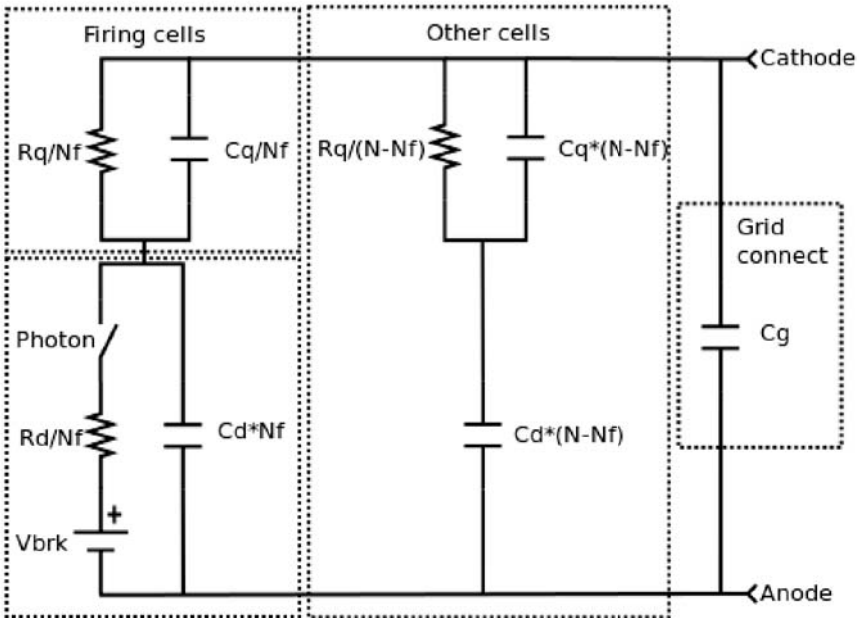

Figure 23: Model schematics

Since the base of a micro-cell is a diode with a quenching resistor (to avoid it's destruction), the model comprises the union capacitance in parallel with the diode reverse voltage power supply plus a series resistor to the diode.

The quenching resistor is simulated with an ideal resistor in parallel with a parasitic resistance.

The diode will start conducting when the power supply is greater than it's breakdown voltage and an ideal switch is closed (simulating the incoming light). Apart from this parameters an interconnection parasitic capacitance is also included.

Parameter	Description
Rq	Quenching resistor value
Cq	Parasitic capacitance of Rq
N	Number of cells
Nf	Number of firing cells
Cd	Diode capacitance
Rd	Diode resistance
Vbrk	Breakdown voltage
Cg	Grid connect capacitance

Table 10: Model parameters

Other parameters such as parasitic inductance of the pins can also be added to the model in series with the anode and cathode connection.

To determine the quenching resistor, the easiest way is to produce an IV curve with the device biased in the direct region. At some point the diode will start to conduct limiting it's current only by the resistor in series of the diode plus the quenching resistor. Since the quenching resistor is expected to be much greater than the device resistance the value of the slope of the curve (in the linear region) will be approximately the quenching resistor divided by the number of cells (all in parallel).

In order to determine the C_d and C_q sum, the charge variation of the output single cell fired has been measured and plotted changing V_{op} value[26]. With this procedure V_{brk} can also be determined extrapolating the voltage when output charge should be 0.

Finally the number of cells (N) and charge seen on the device terminals is specified on the datasheet. Assuming the terminal capacitance value is specified in dc conditions, the C_g value can be extracted as documented in[26].

The only non specified and non measurable directly parameter is R_d but can be estimated in the order of hundreds of Ohms, not affecting the shape of the signal.

Simulation results

Using the shape of the dark count peak and amplitude we can approximate the real values of the device with the simulations, summarized in table 25. In figure 24 there is a comparison between the simulated pulse and the measured single cell fired at V_{op}.

For the SciFi Tracker design a VerilogA model has been implemented using the described model as a basis. This model permits much faster com-

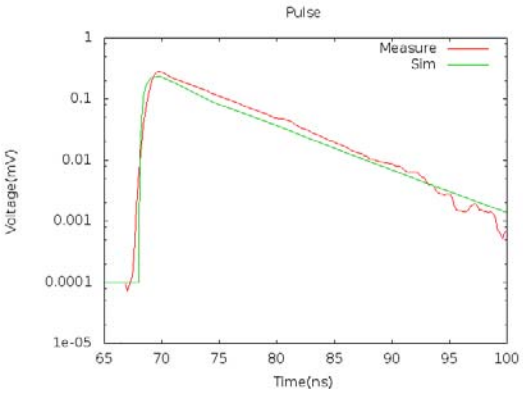

Figure 24: Single cell fired pulse and simulation

Parameter	Value
Rq	300kΩ
Cq	5.7fF
N	1600
Cd	12fF
Rd	1kΩ
Cg	15.8pF
$\mathbf{V}_{brk}$	69.47V

Figure 25: S10362-11-025P parameters

putation of the output and avoids convergence parameters problems that often appear in the simulation of non linear devices (such as ideal switch included in the PSpice model). This model is being extensively used to simulate the different SiPMs under test for the SciFi tracker and to fit the electronics to it's signal shape.

SiPM readout ASICs

A brief status of different integrated options for the readout of SiPMs is summarized in this chapter with detailed description of different architectures. It is important to note that probably not all existing devices will be listed and commented due to the amount of existing options. At the end of this section a snapshot of the "state of the art" in the development of integrated electronics specific for the readout of silicon photo-multipliers should have been provided.

The main results on different charge or current mode input stages is stressed. Typical pre-amplifier implementations are based on **Charge Sensing Amplifiers (CSA)** or **Current Mode** input stages. Each of them have some advantages and drawbacks being the speed of the current mode input the most significant advantage. The charge (or voltage) amplifier permits the connection of the sensor both in the anode or cathode, and normally is AC coupled in order to tune the DC voltage applied at the connection node. Current mode implementations only permit the current flow in one direction (if a good ratio between biasing current and input

current range is desired) thus it must be fixed by design.

Due to different years of production and different technologies used in the production of the prototypes a direct comparison on charge or area can't be made. But in general terms a first approach on the order of magnitude of how this implementations deal with area and power can be obtained.

Comparison tables

To compare several characteristics of the previous ASICs the figures of merit are summarized in next tables, 11 and 12. In first table there is a summary of outputs, outputs type, measurement, measurement accuracy and timing information. Second table summarizes input stage type, power consumption, area usage and also technology.

The typical approach is to deliver charge and timing information, often as a result of the OR of different channels. Normally this double measurement is performed splitting the signal at the output of the pre-amplifier and driving two different signal paths. A multi-channel architecture is always envisaged due to the high numbers of channels needed in current particle detectors or PET systems. Typically a power of 2 channel number is used.

On tables we can see the most popular readout is to use charge based readout. Sometimes applying some shaping just at the pre-amplifier. This is a well known circuit widely used in particle detectors, but does not exploit the speed possibilities of the sensor. On the other hand current mode readout is less used and a connection with the sensor must be defined prior to design, in all examples cathode connection is used.

Differential implementations are not much used since it's not a natural connection of the sensor to the electronics (SiPMs are basically single ended). They offer much better performance in terms of noise but the price to pay is a much important power consumption which does not seem to compensate the advantages.

ASIC	Outputs	Measure	Accuracy	Timing output
FLC_SIPM	Multiplexed analog	Charge	-	No
MAROC3	Multiplexed analog and digital	Charge	Up to 12 bits	64 + 2OR
SPIROC2c	Digital time and charge	Time and Charge	12 bits and 150ps	Digital word
NINO	Digital	Time and width	60ps	LVDS
PETA	Digital	Time and energy	28ps rms	Digital word
BASIC	Digital and Analog mux.	Trigger and energy	650ps	OR trigger
VATA64	Multiplexed analog and digital	Time and Charge	-	Trigger and analog
RAPSODI	Digital	Trigger and Charge	-	Trigger
TOFPET	Digital	Time and Charge	50ps	Digital word

Table 11: Different ASICs outputs summary

Table 12: Different ASICs properties summary

ASIC	Input type	Technology	Input impedance	Channels	Area (mm^2/ch)	Power mW/ch	Year
FLC_SIPM	Charge	0.8μm AMS	AC couple	18	0.56	11	2004
MAROC3	Current	0.35μm SiGe AMS	$\approx$50Ω	64	0.25	2.5	2009
SPIROC2c	Charge	0.35μm SiGe AMS	AC couple	36	0.89	$\approx$2.5	2012
NINO	Diff. Charge	0.25μm IBM	$\approx$20Ω	8	1	40	2003
PETA	Differential	0.18μm UMC	-	16	0.66	86	2008
BASIC	Current	0.35μm SiGe AMS	$\approx$17Ω	8	0.88	$>$2.65	2008
VATA64	Current	-	AC couple	64	1	15	2007
RAPSODI	Current	0.35μm SiGe AMS	$\approx$20Ω	2	4.5	100	2008
TOFPET	Current	0.13μm	10-60Ω	64	0.39	7	2012

Design for PET applications

The main design objectives of a multichannel prototype to improve current state of the art are:

- Pre-amplifier Bandwidth $\approx$ 250MHz
- Direct connection to SiPM
- Controllable DC voltage at SiPM
- Low input impedance
- Fast OR of all channels for timing measurements
- Digital Time Over Threshold output for energy measurement
- Minimize power consumption
- Good linearity

Architecture

In figure 26 a block diagram of the analog channel can be seen. After analysis of previous ASICs it seems the better solution for the readout is current mode input to achieve good timing resolution measurements keeping low power consumption. Current mode input stage provides a low impedance input with a controlled DC voltage and multiple scaled copies of the input current. In this case three copies have been implemented for different measurements; timing, energy and pile-up.

For the timing measurement the common approach is to use one of the signal paths and compare directly with some threshold to detect the leading edge. This process leads to reasonably good timing measurement results. Other more complex processing[40] can lead to slightly better resolution but are often much more complex. For this reason a simple fast current mode comparator has been designed for this application.

For the energy measurement a digital output is desired due to it's flexibility for the readout and low resources usage (no ADC). An integrator with a constant current discharge will provide signal to an hysteresis comparator. Using this circuit a linear output depending on input charge will be delivered. This linear behaviour is desired to avoid extra offline corrections on data.

For the pile-up measurement an extra path with less gain and AC coupled has been used. The AC coupled signal is compared to a fixed threshold using the same fast current comparator used in the timing stage. The output of the comparator is then feed into two cascaded registers to provide a logical

output. Pile-up of all channels is stored in a 16bit register with it's own interface to be controlled and readout.

This architecture keeps interface simplicity both at the input with no extra components needed for SiPM connections and at the output with a direct digital interface to the readout system (typically an FPGA).

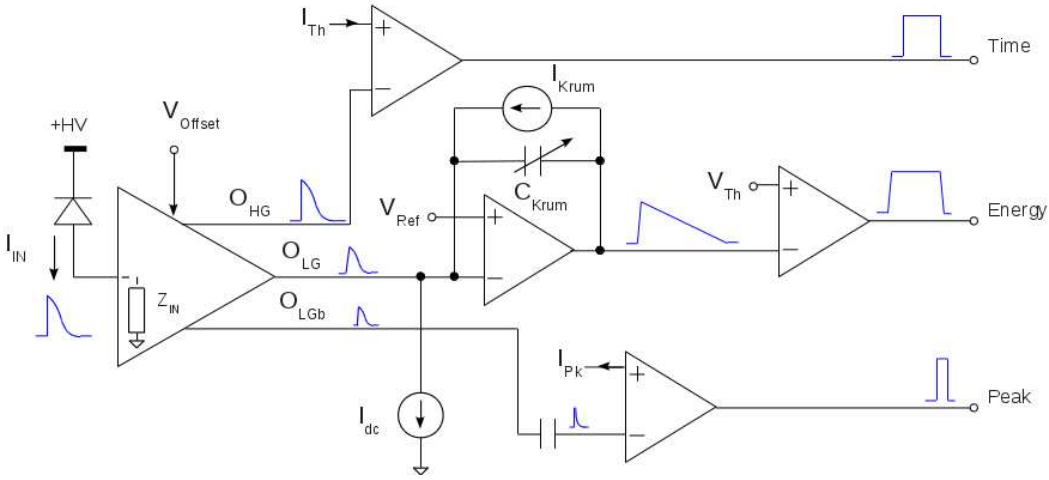

Figure 26: FLEXTOT channel blocks diagram

The added pile-up detection circuitry adds a feature not present in previous designs and useful to avoid extra effort in offline processing of the interesting events.

Slow control for thresholds setup, control voltages and polarization currents of the circuit is also included in the prototype.

Linear Time Over Threshold

Time Over Threshold (TOT) is a processing methodology in which an analog signal is compared to a fixed threshold to obtain a digital pulse representing the height of the analog one. Measuring the width of the digital output the amplitude of the input signal can be obtained. TOT offers simple circuitry for multichannel systems with low power consumption. However typical TOT implementations have poor linearity.

The non linear behaviour of the TOT will depend on signal processing. For example if a simple Gaussian shaping is used on the input signal a triangular approach can be used.Taking this triangular input signal (as

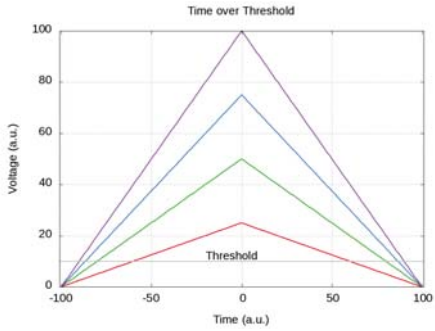

Figure 27: TOT input

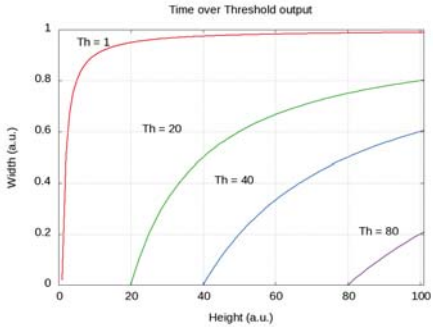

Figure 28: TOT output for triangular input

suggested [48]) the resulting non-linearity is clearly observed depending on threshold value (see figures 27 and 28). Dynamic threshold variation depending on incoming signal has been studied to achieve a linear output [48]. But if an ideal signal with an extremely fast rising edge and constant linear falling edge the resulting TOT measurement should be close to an ideal one.

A similar signal to the ideal can be obtained taking advantage of the fast rising edge given by the SiPM. Using an integrator with a constant discharge current before a comparator, a linear TOT measurement is obtained. Basic schematics can be seen in figure 29. Similar approach has been used in the past in other detector systems[49],[50].

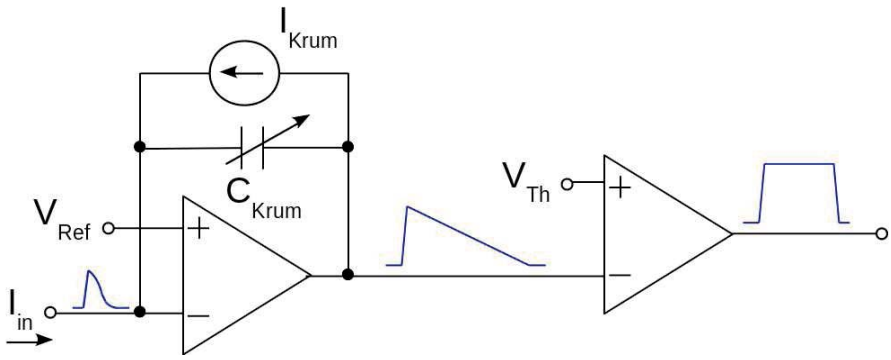

Figure 29: Linear TOT schematic

Ideally resulting TOT measurement can be easily calculated using for-

mula 5, taking as input the injected charge signal (Q). Since threshold voltage (V_{Th}), capacitance (C_{Krum}) and discharge current (I_{Krum}) will be constant the measured time will have a linear behaviour with Q. The non ideal behaviour will be introduced by the slope of the rising edge of our signal and the long decay of some SiPMs. This effect will be noticeable for very small signals, but not for usual events from PET systems.

$$T_{TOT} = \frac{Q}{I_{Krum}} - \frac{V_{Th}C_{Krum}}{I_{Krum}} \tag{5}$$

Some linearity simulations of the linear time over threshold measurement is summarized in figure 30 using a real measured signal as input and including pre-amplifier. First plot represents input signal (in current), second is the voltage output of the integrator, third is the resulting time over threshold output and last one represents the linearity error of every measurement.

One of the most important advantages of this structure is the flexibility. Changing the feedback capacitor and the discharge current much different ranges and time / resolution results can be obtained fitting the range of the desired input signal.

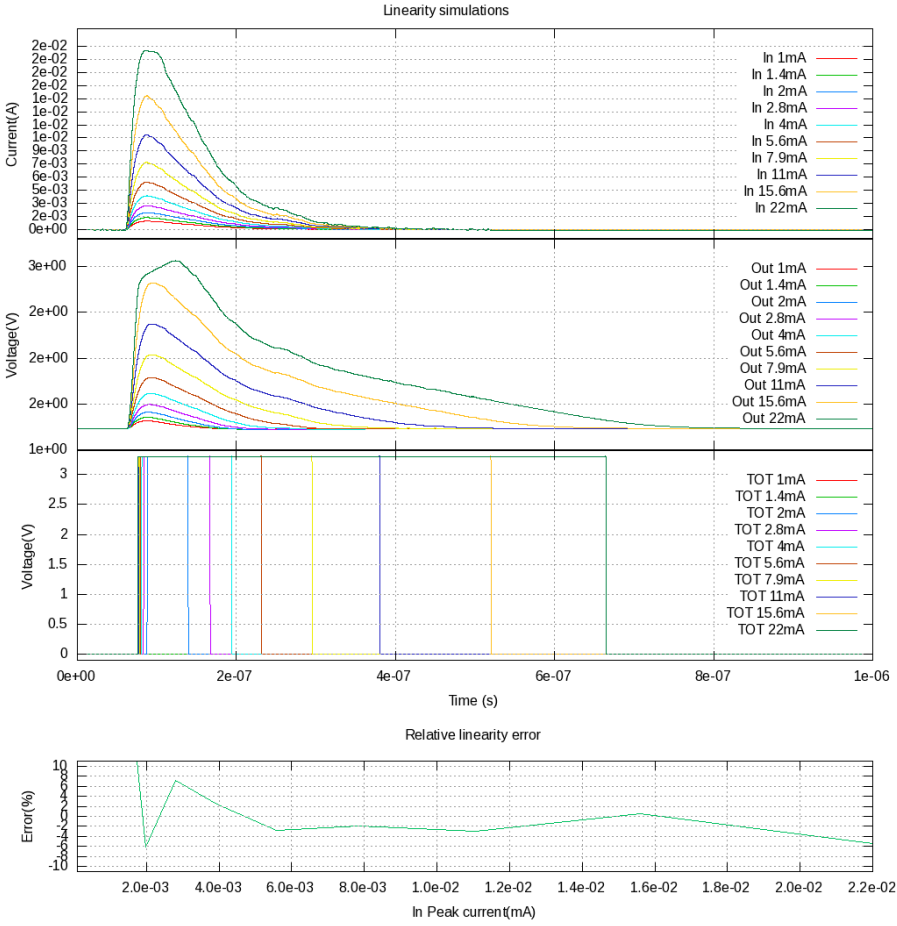

Figure 30: Linearity simulation

Results

FLEXTOT prototype was received in October 2012, with 30 encapsulated dies on a QFN64 and 10 non encapsulated dies. During manufacturing a test system was designed thinking on testing the maximum parameters as possible. First electrical characterization was followed by more realistic tests with SiPM and light sources or radioactive sources.

Test system

Test system (see figure 31) is based on a stack of three PCB with all the needed electronics for a full system. From the sensor to the data communication with a host computer. The only thing not included is the high voltage power supply for the sensors. The following electronics features are present in each of the different PCBs (from top to bottom):

- Sensor PCB: different manufacturers sensors can be placed over this PCB. The sensor connects directly to next PCB, only high voltage connector is available. A variation PCB with a charge injection circuit can be placed in the same position to calibrate channels with a known input shape and peak current.

- Analog PCB: the analog PCB is basically a QFN64 test socket with low drop-out (LDO) linear regulators and some decoupling capacitors and resistors. It also uses a pair of amplifiers to check debug signals directly to an oscilloscope and a high speed switch (SPDT) to be able to disconnect input to channels.

- Digital PCB: EP3C low cost FPGA with FT2232 transceiver to handle communications with host computer. Using the FPGA the slow control can be configured, pile-up interface managed, SPDT switches connection enabled and also a low resolution (5ns) pulse width measurement can be performed for all channels. It houses a basic DAQ for testing the capabilities of the ASIC.

VDDA and VDDD are powered at nominal 3.3V power supply. The average power consumption is 10.7mW per channel or 7.7mW per analog channel (excluding digital power and fast comparators with it's threshold DACs).

An important element to avoid changing the shape of the input signal and to maximize the input current to the input stage is the input impedance. In the design process this value has been kept to a reasonably low value. The

Figure 31: Test system setup

measurement verify the results are as expected; with the typical inductive behaviour at high frequencies and a value close to the typical one (around 34Ω until 200MHz).

To simulate the signal generated by a SiPM a small pcb with the same size as the one supporting the sensors have been designed. The basic circuit is an amplifier followed by an AC coupling with a resistor in series to measure input current. The peak used is generated from an arbitrary waveform generator to mimic the signal from a SiPM.

Linearity

To obtain good linearity in the amplitude of the signal injected between the AWG and the injection circuit a programmable attenuation is inserted. The generator is setup with the maximum output and is then attenuated just before the injection. This setup permits much better linearity in the input signal than just modifying generator output voltage. Previous to linearity measurement a calibration on current input peak value is performed. Using this calibration the energy width of every channel is measured.

Since the prototype has some configurable values it will need some calibration to achieve good linearity results in a defined range and times of input signals. Some examples of the resulting curves from a full prototype (16 channels) are plotted in 32, 34 for a $\tau \approx$36ns and 33, 35 for a $\tau \approx$110ns.

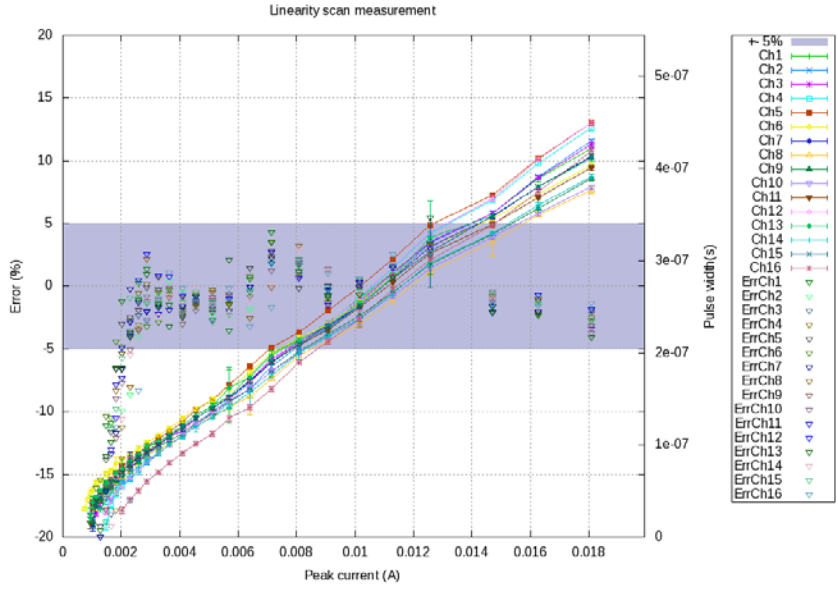

Figure 32: Linearity τ ≈36ns 18mA range

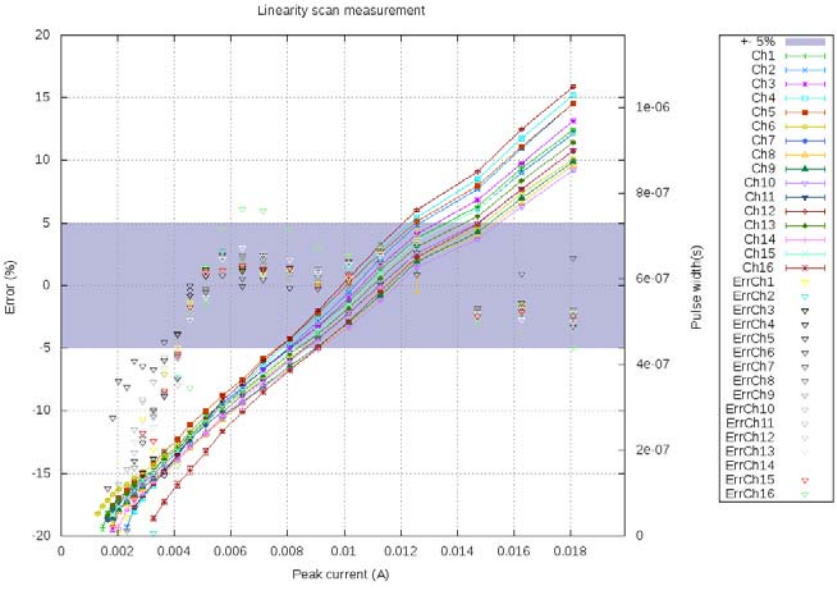

Figure 33: Linearity τ ≈110ns 18mA range

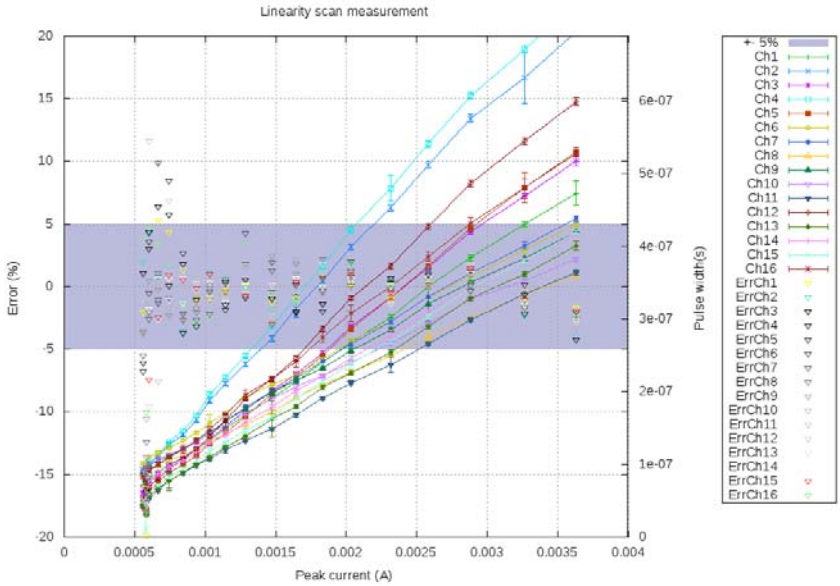

Figure 34: Linearity τ ≈36ns 3.5mA range

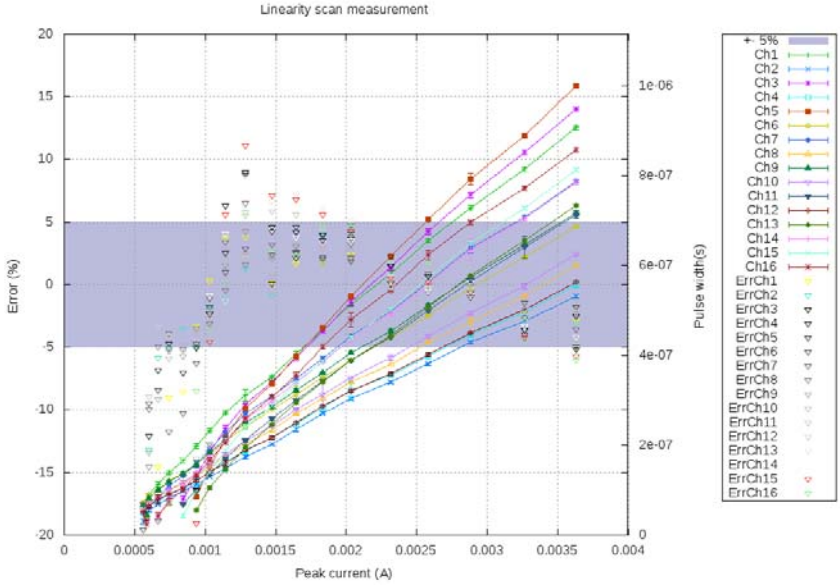

Figure 35: Linearity τ ≈110ns 3.5mA range

SiPM measures

After electrical characterization of the prototype a real sensor is attached to the test system. The input signal will have a realistic timing and avoid any undesired effect introduced by the injection circuit. With this configuration several measurements are performed.

Radioactive sources

To characterize with a signal close to reality several radioactive sources have been used. A small LSO crystal (2x2x8 mm^3) has been placed over a detection channel (3x3 mm^2) and then a radioactive source close to the crystal. Previous to the measurement with sources background (LSO emission spectra) is also measured and should be substracted. The sources used have been Na^{22}, Co^{60} and Cs^{137}, see figure 36.

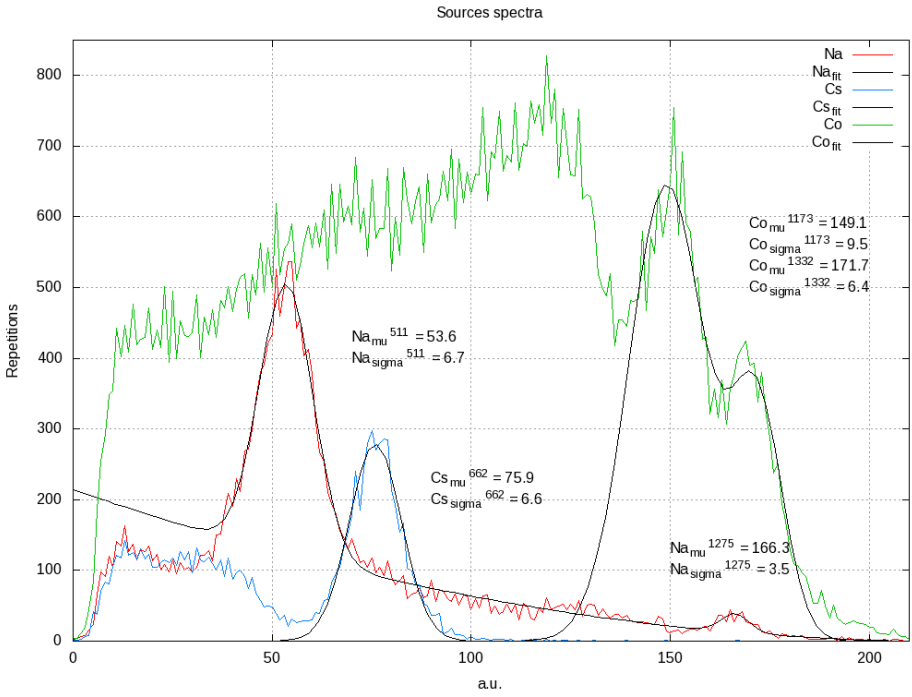

Figure 36: Na^{22}, Co^{60}, Cs^{137} spectra measurement

We can observe excellent linearity in the full range. Using the position of the two more external peaks a calibration constant is determined. The

measured resolutions (σ) are then converted to energy using this constant. The resulting resolution computation is summarized in table 13. As expected resolution improves for higher energies.

Source	**keV**	μ **(counts)**	σ **(counts)**	**Res.(%)**
Na^{22}	511	53.3	7.1	9.6
	1275	166.3	3.5[1]	-
Cs^{137}	662	75.9	6.6	6.9
Co^{60}	1173	149.1	9.5	5.6
	1332	171.6	6.4[1]	-

[1] Some more statistics or better fit should be needed

Table 13: Sources measurements for TH=40

Coincidence Resolving Time

To obtain a first estimation about the overall system timing accuracy, a preliminary measurement has been performed. The basics is to reproduce a coincidence system in the laboratory. Two test boards with single channel SiPMs are placed facing to each other. On top of the SiPM the crystal is placed (LSO and LYSO have been tested). The Na^{22} radioactive source is placed as close as possible to both crystals and just in the middle to obtain coincident signals. The CML output is readout using differential probes. In the oscilloscope the timing and energy signals are acquired.

Plotting both channels energy spectra is used to select a window with the interesting events. This window corresponds to the energies around 511keV ($\pm 1\sigma$). Previous window is used to filter relevant events from the acquisition. The resulting delay measurements of timing outputs from those events are plotted in an histogram to obtain the timing accuracy of the full system in figure 37 resulting in a Coincidence Resolving Time resolution below 300ps FWHM ($\approx$115ps rms).

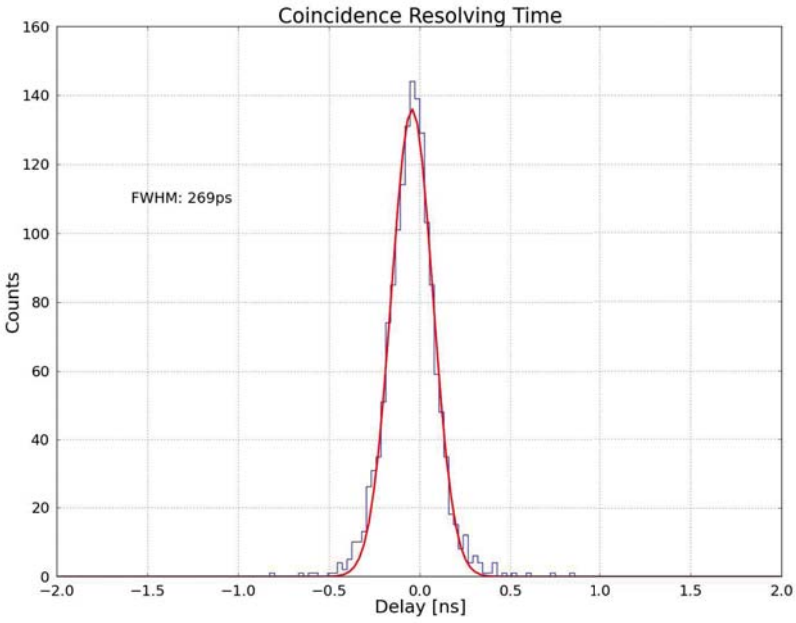

Figure 37: Coincidence Resolving Time measurement

Full system tests

Some measurements have been carried out at CIEMAT with a full PET system emulator. In this case two sensor boards are placed face to face with a rotating plate in the middle (removing the need of the full ring of sensors). The desired samples are placed in the rotating plate and the acquisition is performed including image reconstruction. The measured output can be seen in figure 38.

In this case two measures have been carried out, a first one including a single Na^{22} radioactive source (0.25mm diameter) and mixing measurements of two different positions in the same imgae. And a second measure with two radioactive sources (1mm diameter) measured at the same time. The final position resolution is at the order of few mm as expected.

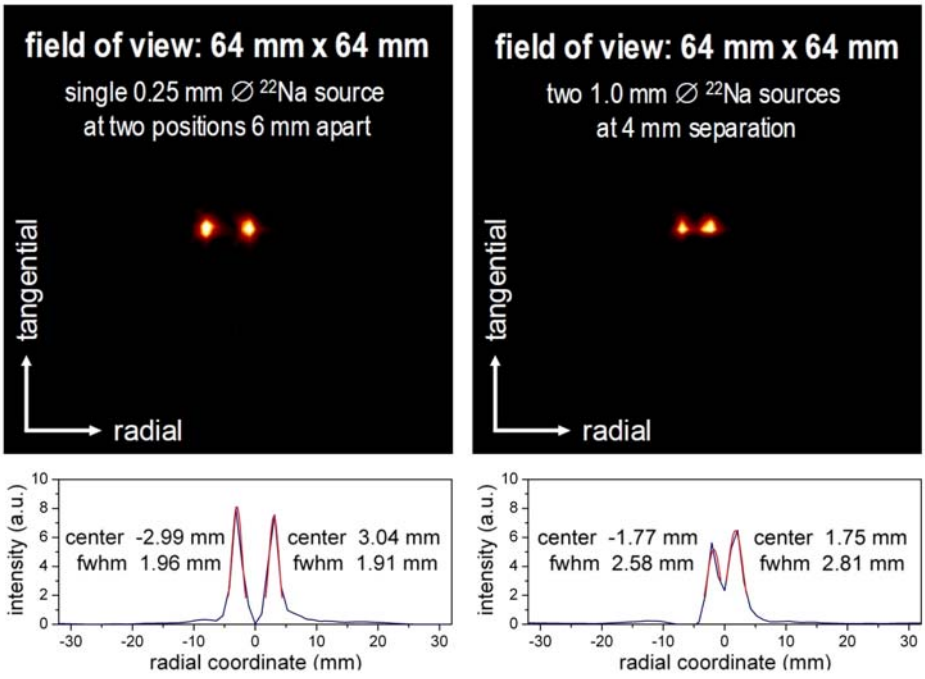

Figure 38: Full system measurements

Design for SciFi Tracker

Design for high energy particle detectors must meet some relevant timing constraints much more different than in other systems (such as PET).

The tracker sub-detector of the LHCb experiment reveals the paths of electrically charged particles as they pass through and interact with suitable substances. The detector records a tiny signal (light or charge) that particles trigger as they move through the detector. Some built detectors use silicon devices (strip detectors) or gaseous detectors (straw tubes). Once the signal is acquired and readout a computer program reconstructs the recorded patterns of tracks.

The new technology for the OT IT upgrade will be based on scintillating fibres, with clear scintillating fibres generating and carrying the photons from the inner region to the sensors placed outside the LHCb acceptance.

In the first draft of the Technical Design Report (TDR), a new scintillating-fibre layout has been proposed, with 2.5 m long fibres covering the whole central region of the tracker stations, from the LHC beam plane all the way to the top and bottom of the LHCb acceptance. In this Central Tracker (CT) option, the IT and several (or all of the) OT modules are replaced by the new scintillating-fibre modules. Full detector is built by 3 stations with three tilted ($\leq 5^o$) fibre planes of X-U-V-X. Every plane is made of 5 layers of fibres with 250 μm in diameter and 2.5 m long.

One of the major concerns is the production and alignment of the fibres in the modules. Some new techniques have been developed to produce such modules and showed promising results.

Regarding the electronics a collaboration with Clermont Ferrand and opened to any other institute from LHCb is ongoing and a common design effort for the production of a readout ASIC will be developed, the low Power Asic for the sCIntillating FIbres traCker, PACIFIC.

Several processing strategies are under study, but the simplest one seems to be the baseline solution, involving pre-amplifier, shaper, gated integrator and ADC. More complex processing is also under study.

Specifications summary

A summary of the specifications for the PACIFIC readout ASIC is detailed in table 14.

Parameter	Value	Unit
Channels	64 or 128	-
Power	0.5 or 1	W
Package	BGA	-
Double peak resolution	25	ns
SiPM time constant	40 - 400	ns
Dynamic range	0-64	micro-cells
Signal time of arrival	0-15	ns
Input referred noise	$\leq$143	$\frac{pA}{\sqrt{Hz}}$

Table 14: PACIFIC specifications summary

Architecture

The channel architecture proposed for the PACIFIC design is depicted in figure 39. Although other alternatives are under study, specifically a fastest digitization followed by digital processing, the easiest solution seems to shape and integrate signal in the 25 ns window. Since no dead time is allowed a double and interleaved gated integrator will be needed. After the integration a 40MHz ADC will convert the signal to digital. Afterwards a serial link will take the signal from one or several channels and serialize them into a single (probably differential) high speed link. For this last step some kind of multiplication frequency circuit will be needed (for example a PLL in the figure).

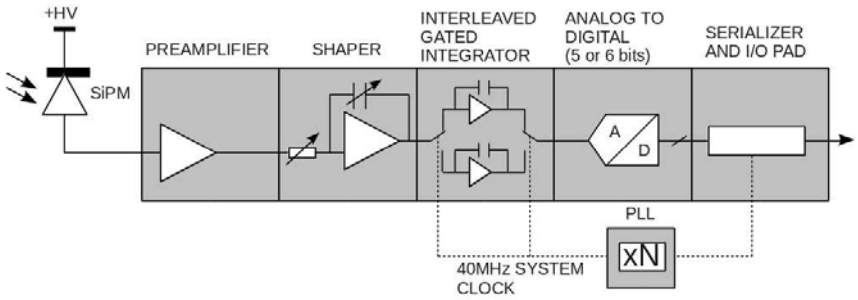

Figure 39: PACIFIC channel blocks

Some common bias and digital control of configurable voltages, currents and shaping parameters will also be needed. So current DACs, voltage

DACs and variable resistors and capacitors will also be designed, with a slow control interface built in standard cells.

Preamplifier

The input stage is current mode preamplifier with the current flowing from the SiPM anode to the circuit. The goal is to achieve the following specifications in this block;

- High bandwidth ($\approx$ 250MHz).
- Low power ($<$ 2mW, maximum of 8mW/channel including all ASIC).
- Low input impedance ($20\Omega < Z_{in} < 40\Omega$).
- DC voltage controllable at input node ($\approx$ 1V range).
- Input referred noise $\leq 143\frac{pA}{\sqrt{Hz}}$

The basic circuit to achieve previous features is depicted in figure 40. The input stage is based on the same novel approach of double feedback but with some variations to adapt to a newer technology process (IBM 0.13μm).

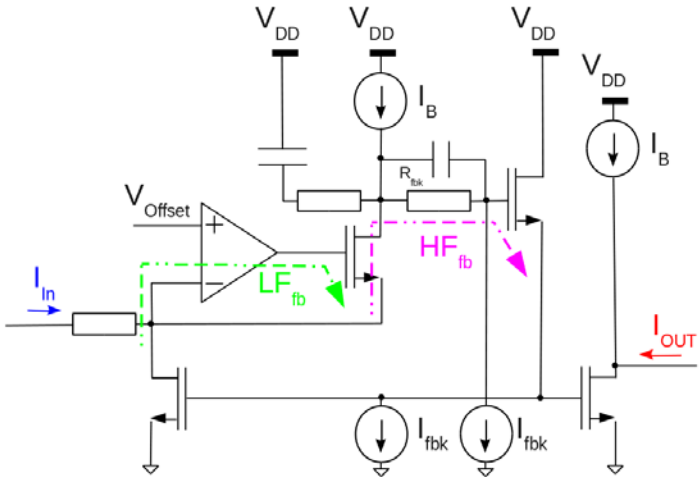

Figure 40: PACIFICr1 input stage

It provides a low input impedance in order to avoid affecting timing behaviour of the SiPM and increase input current. HF_{FB} is the high frequency

feedback path that keeps this input impedance constant (in a certain frequency range). The second labelled path, LF_{FB} will provide the dc voltage (V_{offset} in figure) of the input node using the virtual short circuit in the amplifier that will drive a follower in a lower frequency range. The design has been implemented taking into account that dominant pole should be set at the input node (SiPM parasitic capacitance is at the order of tenths of pF). In this way stability is not compromised when an important capacitance is added at the input.

Conclusions

A detailed description on the sensor properties and requirements for both a PET detector and SciFi tracker has been exposed. Taking as a starting point several implementations of readout circuits a novel input stage has been proposed with a novel double feedback structure making possible to achieve wide dynamic ranges and easily configurable. A behaviour model from the sensor has been useful in the design stage to simulate circuit behaviour. Two designs using this circuit intended for PET and SciFi have been detailed. Both of them use similar input stage but implemented on different technologies. PET prototype uses SiGe technology and benefits from the bipolar transistors usage (specially on input stage and reference circuits), while SciFi prototype is a CMOS technology but benefits from a smaller feature size.

The main goals for the PET system have been fulfilled. A multi-channel architecture with direct connection to the SiPMs and analog processing has successfully been designed and tested. The voltage adjustment on the input will permit to change sensor gain. Multiple signal paths proved to give the desired results. With excellent timing measurement and also good energy measurement and pile-up detection. The proposed input stage fits all the requirements and the rest of processing benefits from this. After design and production, full device testing has been performed including some tests that exceeds the mere electronics characterization (radiation sources tests and coincidence). The only test remaining is to integrate this electronics in a real PET system to verify it's functionality.

The design constrainis on the PACIFIC project are still under analysis and this first prototype has served as a starting point. The circuitry designed for the SiPM readout has been ported to a new technology and simplified for the application. Real prototype testing is still needed but meanwhile design is ongoing adding the needed signal processing chain to achieve the goal.

Patent notice

As a result of the work described in this document a shared patent application was submitted in 2012:
"Readout circuits for multi-channel photomultiplier arrays", D. Gascón, A. Comerma, and Ll. Freixas (Applicants: Universitat de Barcelona and CIEMAT), European Patent Application EP12382516.8, December 20, 2012.

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Introduction

The aim of this thesis is to present a solution for the readout of Silicon Photo-Multipliers (**SiPMs**) arrays improving current implemented solutions. With this purpose a novel current mode input stage has been designed and tested. Design focuses in general applications for medical imaging (Positron Emission Tomography, **PET**). The same input stage topology is also used for a more constrained design in particle physics (upgrade of Tracker detector at **LHCb** experiment).

SiPMs are recently developed electronic devices[1] with photon counting capabilities improving current state of the art detectors regarding high voltage requirements, signal gain and magnetic field insensitivity, while keeping at the same time excellent gain and timing characteristics and a wide dynamic range. They are semiconductor devices still under development by some manufacturers[a] in order to improve yield, to reduce dark count, to provide multi-channel architectures and to increase light sensitivity spectrum.

Immunity to magnetic field and compact form factor make SiPMs an ideal choice for their usage in particle detectors and medical imaging systems such as MR-PET scanners when used with an optically coupled scintillating material providing the conversion between particles to light pulses.

A Front-End Readout Application Specific Integrated Circuit (**ASIC**) for SiPMs is presented with the following features: wide dynamic range,

[a] Some manufacturers, but not all include: Hamamatsu, KETEK, SENSL, STM, Excelitas, AdvanSID, Photonique and Zecotek.

high speed, multi channel, low input impedance, low power consumption, SiPM voltage control and timing, charge and pileup signal outputs.

Special emphasis in a detailed description on the SiPM modeling and parameter extraction to be used in the design stage is also included. This model makes possible the emulation of the signal generated by different commercial devices in the design stage using SPICE simulations. The parameters needed by the model are simple enough to be measured directly on the devices with standard equipment.

The pre-amplifier stage includes a novel circuitry with saturation control that permits to be operational on the various signal paths (timing, charge and pileup) even when the path with higher gain is completely saturated. This circuitry permits the correct operation of the measurement outputs in a wide input dynamic range. Input stage introduces a novel double feedback loop to lower input impedance at the same time it keeps a constant DC value at the input node.

First prototype was submitted on June 2011 and manufactured by AustriaMicrosystems 0.35 μm BiCMOS technology. A second mixed mode and more complex prototype was submitted in June 2012 with the same technology for PET applications. A third prototype is envisaged for beginning 2014. For a high energy physics application like the Scintillating Fibre Tracker of LHCb, very different timing constraints should be met. A first pre-amplifier version was submitted in May 2013 and using standard CERN technology IBM 130nm.

Chapter 1 with a basic detector systems overview introduces several light sensors with their advantages and drawbacks. An important part in a detector is the scintillator, generating light bursts on particle crossing, a description of the functionality and characteristics of different types and their properties is also present. The chapter ends with an introduction to the two main applications developed in this work, Positron Emission Tomography (PET) and Scnitillator Fibre (SciFi) Tracker detector for the upgrade of LHCb experiment at CERN.

Chapter 2 details the model used for the simulation of signal coming from a SiPM with some real measurements. This Spice model is used in simulations with the schematics of the pre-amplifier block.

Chapter 3 is a summary of different developed ASICs for the readout of SiPMs. They are intended not only for SiPMs and sometimes are compatible with other similar devices such as PMTs. This chapter should give an overview of the current state in development of such electronics, with their good points and drawbacks. This will be the basis for defining specifications

for the optimal design of the electronics.

Chapter 4 details the novel input stage implementation with exhaustive description of it's behaviour and advantages from the state of the art described in previous chapter.

Chapter 5 focuses on the design developed for PET applications. This is a multi-channel design in AMS 0.35μm BiCMOS technology for the readout of arrays of SiPMs, with energy, timing and pileup outputs.

Chapter 6 is a modified version of the design in previous chapter adapted to a completely different technology (IBM 130nm) with a much lower operation voltage (1.2V or 1.5V in spite of 3.3V), fully CMOS implementation and requiring much less area.

Finally in **Chapter 7** the conclusions of the results achieved with current prototypes and next steps to follow are commented.

On the **Appendices** several datasheets generated as documentation for different prototypes are compiled including the main simulations and measurements.

1.1 Detector Systems Overview

[b]Most of detector systems include the same basic functions. The signal from each sensor or sensor channel in a detector array must be amplified, shaped and processed for storage and analysis. Some functions are clearly associated with individual circuit blocks while other functions are carried out by more than one block. In single channel systems digitization and data storage are often combined in a single unit, but multi-channel systems normally use external digitizers and data is then feed to a computer. In highly compact detectors (such as high energy physics detectors) some channels of analog and digital electronics are often accommodated in specific circuits (ASICs).

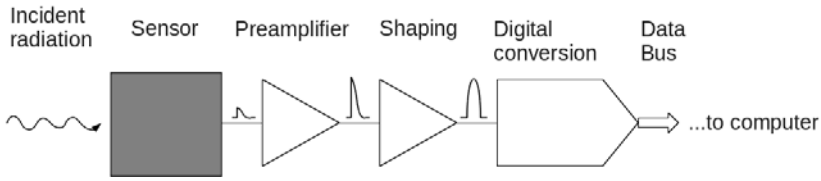

Figure 1.1: Typical detector system [2]

The typical sequence of detector functions is illustrated in figure 1.1. The **sensor** converts the energy deposited by a particle or photon to an electrical signal. This can be achieved in different ways (see section 1.2). In some cases the resulting sensor pulses can be quite short (few nanoseconds or less).

The signal charge can be quite small (of the order of few fC for typical sensors and signal) so it will need some amplification. The **pre-amplifier** will perform this amplification keeping in mind that the minimal electronic noise is required to avoid degradation of the signal. The specific factor of amplification will depend on the original gain of the sensor, signal range and resolution requirement of the measure.

Normally the function of the **shaper** in detector systems is to improve the signal to noise ratio (SNR). Signal and noise do not present the same frequency spectra so one can improve the SNR by applying a filter that tailors the frequency response, attenuating the noise. This change in the frequency response will produce a change in the signal shape, thus the name of the stage. Simple shapers normally reduce the bandwidth. The result of

[b]Based on [2]

this reduction is that the signal becomes slower. This can lead to overlapping between signals (if high rate is expected), called pile-up. Shapers can be of high complexity with several stages, but it is common to all shapers to constrain maximum and minimum frequency bounds, determining rise time and pulse duration. When designing a system it is necessary to find the proper balance between noise and speed. Sometimes the shaper is hidden, an input stage integrating the input pulse should translate the charge into voltage that can be held for digitization. This is also a form of shaping.

Digital conversion will translate the voltage amplitude into discrete steps corresponding to a digital bit pattern. Analog to Digital Converters (ADCs), are widely used nowadays. Generally speed and resolution are opposing parameters in ADCs, as speed and power.

1.2 Light sensors

Several light sensors exist and have been used in the past. The most notable is the classical Photo-Multiplier Tube (PMT), but some other alternatives are also present such as Avalanche Photo-Diode (APD) and recently the SiPMs. Their usage ranges from particle detectors to medical imaging and astroparticle detectors.

1.2.1 Photo-Multiplier Tube, PMT

This devices are a type of vacuum tubes. They are very sensitive light detectors in different spectra (typically optimised for visible or ultraviolet). They are so sensitive that even single photons can be measured. This combination of high gain, low noise, fast response and large area of light collection are often desired in high energy physics applications or medical imaging. First photomultiplier produced is dated around 1935 [3].

Figure 1.2: PMT[c]

The basic of operation combines the photoelectric effect with amplification produced by secondary emission. In figure 1.3 a schematic view of its parts and operation can be seen when coupled to a scintillating material. The two major components inside the tube are a photosensitive layer, called photo-cathode, coupled to an electron multiplier structure. Once the incoming photons hit the photo-cathode, the photoelectric effect produces some low-energy electrons (photo-electrons). If the incoming light consists of a pulse from a scintillation crystal, the photoelectrons produced will also be a pulse of similar duration. Because only a few hundred photoelectrons may be involved in a typical pulse, their charge is too small at this point to serve as a convenient electrical signal.

The electron multiplier section in a PMT provides an efficient collection geometry for the photoelectrons as well as serving as a nearly ideal amplifier to greatly increase their number. Electrons from the photo-cathode are accelerated and caused to strike the surface of an electrode, called a dynode. If the dynode material is properly chosen, the energy deposited by the incident electron can result in the re-emission of more than one electron. Electrons leaving the photo-cathode have a very low kinetic energy. Therefore, if first dynode has a positive potential of several hundred volts the

[c]Image extracted from wikipedia

kinetic energy of electrons at arrival is determined almost by the accelerating voltage. The usage of several stages produce more and more amplification on every stage. After amplification through the multiplier structure, a typical pulse will give rise to 10^7-10^{10} electrons, sufficient charge to be processed after being collected in the anode[4].

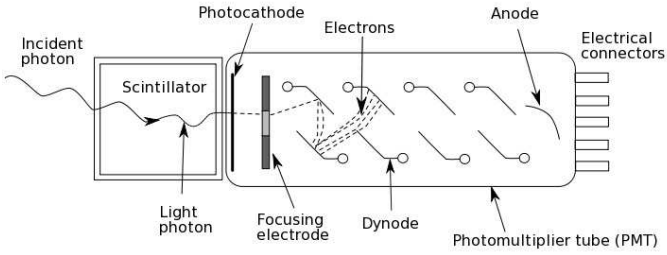

Figure 1.3: Photomultiplier basic operation

Photo-cathodes can be constructed as either opaque or semitransparent layers. Several photo-cathode materials provide sensitivity to a wider or narrower spectra adapting to the application. The variety of spectra sensitivity of the PMT (changing the material of the photo-cathode) makes it an ideal solution for ultra violet light measurement. An important practical property of photo-cathodes is the uniformity to which their thickness can be held over the entire area. Variations in thickness give rise to corresponding changes in sensitivity and can be one source of resolution loss.

Spontaneous electron emission is produced by thermal emission. Normal conduction electrons within the photo-cathode material will always have some thermal kinetic energy that, at room temperature, will average a low value. There is a spread in this distribution, however, and those electrons at the extreme upper end of the distribution can occasionally have an energy that exceeds the potential barrier. If that electron is close enough to the surface, it may escape and give rise to a spontaneous thermally induced signal.

The sensitivity of photo-cathodes cathodes can be quoted in several ways. A unit with great significance is the **Quantum efficiency (QE)**. The quantum efficiency is as simple to describe as in formula 6[4]. The efficiency would be 100% for an ideal photo-cathode, but practical devices show much smaller values.

$$QE = \frac{photoelectrons\ emitted}{incident\ photons} \tag{6}$$

The quantum efficiency of any photo-cathode will be a strong function of the wavelength (or energy of incoming photons). To estimate the effective quantum efficiency when used with a particular light source, the curve of QE versus wavelength must be averaged over the emission spectrum.

To define the overall detection capabilities of the sensor the most common measure is the **Photon Detection Efficiency (PDE)**. It is the result of joining the QE of the photo-cathode and the **Collection Efficiency (CE)** of the amplifications dynodes (see formula 7). The Collection Efficiency will include geometrical effects on the construction that lead to dead area or signal loss before the first dynode.

$$PDE = QE \ x \ CE \tag{7}$$

Multi-channel devices with arrays of 8x8 channels have been produced and arranged in a rectangular packaging to improve area coverage with small crosstalk and keeping excellent properties [5].

Most important drawbacks of using PMTs are:

- Dark current (noise) produced by photo cathode thermal emission of electrons.
- Low Quantum Efficiency.
- High voltage needed for it's operation (typically between 1000 and 2000 V).
- Magnetic field sensitivity.
- Mechanically fragile.
- Size.
- Ageing (photo-cathode degrades with use).

1.2.2 Avalanche Photo-Diode, APD

Avalanche Photo-Diodes are semiconductor devices based on the photoelectric effect and avalanche multiplication. By applying a high inverse voltage polarization just over breakdown (from 100 to 1000 V depending on devices), an important gain can be obtained (in the range of 100 to 1000). If more gain is needed (10^5 or 10^6) this devices can be operated over the breakdown voltage in Geiger mode, with external circuitry to provide quenching of the device.

On conventional photo-diodes, when light is incident on the semiconductor, electron-hole pairs are generated. Photons from a scintillator typically carry about double the energy of the semiconductor bandgap, thus sufficient to create the electron-hole pairs. Since this conversion is not limited by the need of carriers to escape from a surface (as in a photo-cathode) the maximum quantum efficiency can be larger upto 60-80%. The sensible wavelength is often also wider than from PMTs, so it results in more primary charge generated from the incoming light.

A typical configuration[4] can be seen in figure 1.4, with a p-layer as thin as possible to enhance transmission of light, and a volume polarized with an electric field to collect the generated pairs. Generally APDs are designed as fully depleted detectors, consisting of high purity p or n silicon with highly doped p and n type contacts at opposite surfaces. Electronic noise in such devices is much more important that dark current in PMTs.

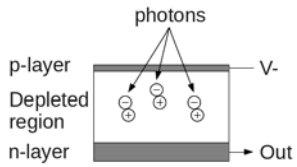

Figure 1.4: Typical photo-diode configuration

The small amount of charge that is produced by photoelectric effect in a conventional photo-diode can be increased through an avalanche process that occurs in a semiconductor at high values of applied voltage. The charge carriers are accelerated sufficiently between collisions to create additional electron-hole pairs along the collection path. The internal gain helps pull the signal up from the electronic noise level and permits good energy resolution than conventional photo-diodes. Because gain is very sensitive to temperature and voltage, they require well-regulated high-voltage supplies.

Figure 1.5: Typical APD configuration

A typical construction[4] known as reach-through configuration is shown in figure 1.5. Light enters through the thin p^+ layer on the left of the diagram and interacts somewhere within the π region that constitutes most of the diode thickness. The results of interactions are electron-hole pairs, and the electrons are drawn to the right through the drift portion and into the multiplying region, with high electric field (p-n^+ union in the right). Here additional pairs are created increasing the signal. Gain factor of a few hundred are typical and quantum efficiency can be as high as 80%.

Typical applications for APDs are on telecommunications, laser rangefinders and in some cases have been used in medical imaging and particle detectors. APDs arrays are becoming commercially available.

Compared to PMTs, APDs offer some advantages;

- High Quantum Efficiency.
- Relatively low voltage needed (between 50 V and 400 V typically).
- Magnetic field insensitivity.
- Robust and small.

And also some drawbacks;

- Electronic noise is important.
- Small gain.
- Radiation hardness.

1.2.2.1 Hybrid devices

A variation between PMTs and APDs is the called hybrid photomultiplier tube (HPMT) or hybrid photo-diode (HPD). The basic principle involves fundamentally a different way of multiplying the charges created in the photo-cathode by incident light. In figure 1.6 a schematic view of a typical construction is shown.

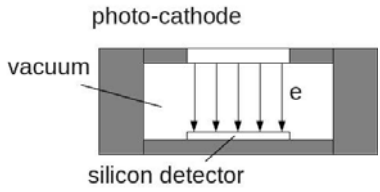

Figure 1.6: Typical HPD construction

As in a conventional PMT the light is converted to electrons with a photo-cathode, but here the conventional multiplier structure is replaced by a silicon detector placed in the same housing. A large voltage difference is applied between the photo-cathode and the silicon detector to accelerate electrons between the two elements. The resulting amplification is much less than the typical from a PMT. The most important advantage in front of conventional tubes is the lower statistical spread in the amplitude of the output signal. An important advantage comparing with PMT is that gain will increase linearly with the voltage applied and not exponentially as in a PMT (this makes easier to setup and control the high voltage). The consumption from the high voltage will also be much smaller.

1.2.3 Silicon photo-multipliers, SiPM

A silicon photo-multiplier is a relatively new device formed by hundreds of micro-cells in parallel. Each micro-cell is an Avalanche Photo Diodes (APDs) working in Geiger mode, with its own quenching resistor to avoid destruction of the device. APDs behaviour is well known and has been studied during many years since 1960 [7]. All those micro-cells are combined in one single output (connected in parallel). The result is an output similar to the one produced by a PMT, but with a somehow discrete analog output (since each cell releases a fixed amount of charge when fired). In figures 1.7 and 1.8 and table 1.1 some commercial devices from Hamamatsu can be compared.

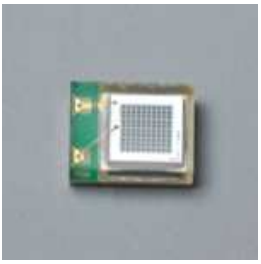

Figure 1.7: S10362-11-025P

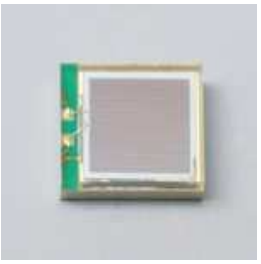

Figure 1.8: S10931-050P

Parameter	025P	050P	100C
Number of cells	1600	2600	100
Cell size (μm^2)	25x25	50x50	100x100
Active area (mm^2)	1x1	3x3	1x1
Voltage operation (V)	$\approx$ 70V	$\approx$ 70V	$\approx$ 70V
Gain	2.75x10^5	7.5x10^5	2.4x10^6
Fill Factor	0.31	0.62	0.79

Table 1.1: Hamamatsu SiPMs characteristics

In the same way as the APDs, the first pairs are generated by photoelectric effect and then multiplied inside the same silicon. But in this case the

All referred commercial devices must be taken in the context of an evolving technology. Thus real numbers may have varied with time and newer models introduced. Values should be taken just as example.

multiplication is an avalanche, produced over breakdown voltage.

In a normal multiplication process electrons are drawn through the high field region and create additional electron-hole pairs. The electrons continue in the same direction but holes are attracted in the opposite direction. At a sufficient high field values (over breakdown voltage) the holes can also multiply and, since hole multiplication also produces additional free electrons, this process leads to a runaway. To avoid a destructive effect of the avalanche a resistor in series is connected to each APD so the voltage it's dropped when it reaches some current limit. This combination of APD and quenching resistor is the micro-cell. The resulting gain is similar to the PMT on the order of 10^5 to 10^7.

Since SiPMs are constructed as a group of smaller micro-cells an extra concept should be added when defining the characteristics, this concept is called **Photon Detection Efficiency (PDE)**. It's nothing more than joining the effects produced by the area lost between micro-cells and Quantum Efficiency. Since there is some area not able to detect incoming light a **Fill Factor (FF)** is defined as in 8. The resulting PDE will be calculated easily using formula 8 with P_{start} being the probability of an electron-hole to start an avalanche. Some techniques used to improve crosstalk between micro-cells (such as adding trenches) can degrade this value. The reduction of micro-cell size to increase dynamic range will also make a worse fill factor.

$$FF = \frac{Total\ \ Device\ \ Area}{Sensible\ \ Area} \quad \rightarrow \quad PDE = FF\ \ x\ \ QE\ \ x\ \ P_{start} \tag{8}$$

Most important advantages with respect to other sensors are:

- High quantum efficiency.
- Magnetic field insensitivity.
- Robust and small.
- Low voltage operation (from 20V to less than 100V).
- Arrays available.

And drawbacks or possible problems:

- Radiation hardness.
- Low PDE.
- Dark count.

Several parameters are commonly measured and taken into account to determine the properties of a concrete manufactured SiPM. Following sections try to summarize the most important ones. Several measurements and comparisons can be found in literature[8] and deep description of different effects[9].

1.2.3.1 Dynamic range

SiPM offer a linear output depending on incident light in certain range of input photons. According to [10] the response of a SiPM can be extracted with equation 9, where m is the total number of cells of the device and ε the photon detection efficiency. A plot of this function for previous commercial devices can be seen in figure 1.9. Extracting the deviation from the theoretical detection value (see figure 1.10) and cutting to a maximum tolerable error of 10% or 20% the different devices saturation is summarized in table 1.2.

$$N_{cells fired} = m * \left(1 - e^{-\frac{N_{photons} * \varepsilon}{m}}\right) \tag{9}$$

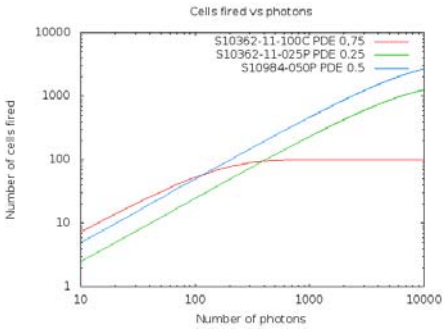

Figure 1.9: SiPM saturation

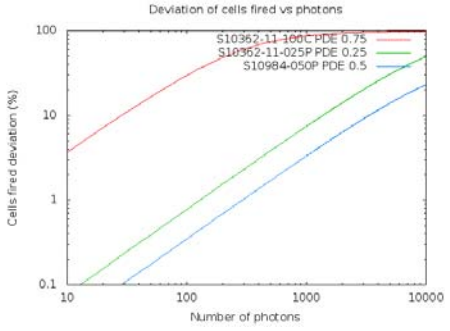

Figure 1.10: SiPM detection deviation

Device	10% deviation	20% deviation
S1032-11-100C	28ph	62ph
S1032-11-25P	1400ph	2730ph
S10931-50P	3300ph	7800ph

Table 1.2: Device saturation on incoming photons detection

1.2.3.2 Gain Variation with Temperature

SiPM devices have an important temperature coefficient which modifies their breakdown voltage thus affecting their gain. The temperature coefficient is common to all devices and equal to 56mV/°C. In figures 1.11 and 1.12 it is represented the gain variation with the temperature change [11].

The gain change extracted from previous figures is 4%/°C in 50μm devices and 2%/°C in 25μm devices. If an array of devices should be compensated without modifying the general polarization voltage in a range of 10°C the voltage applied is calculated in 10.

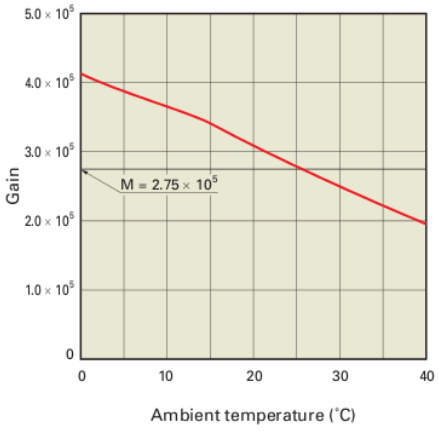

Figure 1.11: S10362-11-025 Gain variation with temperature

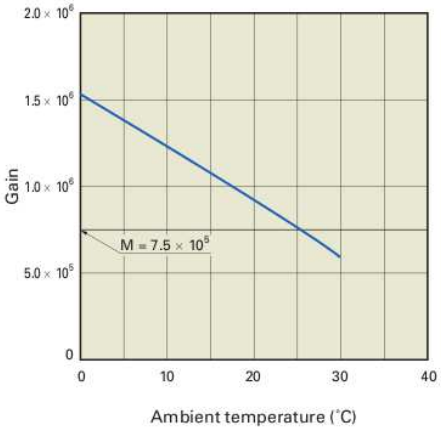

Figure 1.12: S10362-11-050 Gain variation with temperature

$$\begin{aligned} \Delta T &= 10^{\circ}C, \quad \Delta V_{25} = \Delta T * 0.02\frac{1V}{0.5} = 400mV \\ \Delta T &= 10^{\circ}C, \quad \Delta V_{50} = \Delta T * 0.04\frac{1V}{1.5} = 267mV \end{aligned} \tag{10}$$

The resulting controlling DAC should provide a range to compensate the temperature and gain uniformity variations (1.1V for the 25μm device while only 500mV for the 50μm devices) with resolution (to achieve 1% gain adjustment) of around 6.66mV for the 50μm devices and 20mV for the 25μm devices.

All referred commercial devices must be taken in the context of an evolving technology. Thus real numbers may have varied with time and newer models introduced. Values should be taken just as example.

1.2.3.3 Gain Uniformity

Those devices offer a very linear gain versus voltage characteristic that permits to compensate uniformities between different sensors. This linear characteristic is around 50%/V in 25μm devices and 150%/V in 50μm devices, as seen in figures 1.13 and 1.14 extracted from [11]. If the gain should be adjusted at a level of 1% a voltage adjust resolution of 6.66 mV in the 50μm devices while only 20mV in the 25 μm devices.

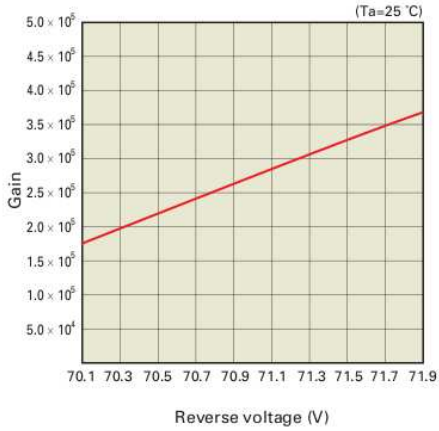

Figure 1.13: S10362-11-025 Gain variation with Voltage

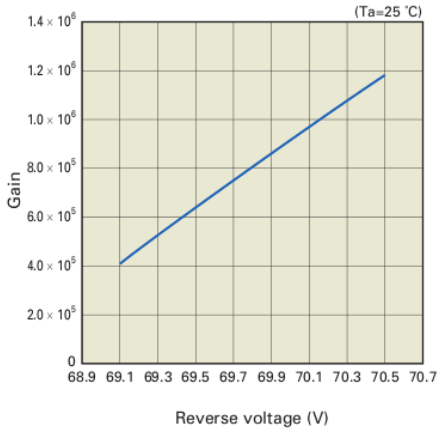

Figure 1.14: S10362-11-050 Gain variation with Voltage

The expected dispersion between gain in devices should also be compensated and is expected to be as high as 35% [12][d]. In the worst case a 25μm device would need a voltage compensation calculated in 11, while a 50μm device should need much less voltage adjust due to it's gain variation.

$$\begin{aligned} \Delta G &= 0.35, \quad \Delta V_{25} = \frac{1V\Delta G}{0.5} = 700mV \\ \Delta G &= 0.35, \quad \Delta V_{50} = \frac{1V\Delta G}{1.5} = 233mV \end{aligned} \tag{11}$$

[d] This gain dispersion should be verified with a significant number of devices, recent tested arrays of SiPMs does not report a dispersion bigger than 13%, but they could have been selected on manufacturing process
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1.2.3.4 Typical Signal

Typical output signal from a SiPM connected directly to a load (50Ω) resistor can be observed in figure 1.15. Measurement is performed using an oscilloscope with long retention on the screen (30s), so signals are accumulated on the same screen.

The trigger is connected to the same signal firing a red laser LED facing the SiPM. Signal is adjusted to be as low as possible so different cells firing can be observed directly and distinguished on the screen. The different peak amplitudes on the screen result from a different number of micro-cells triggered by single photons.

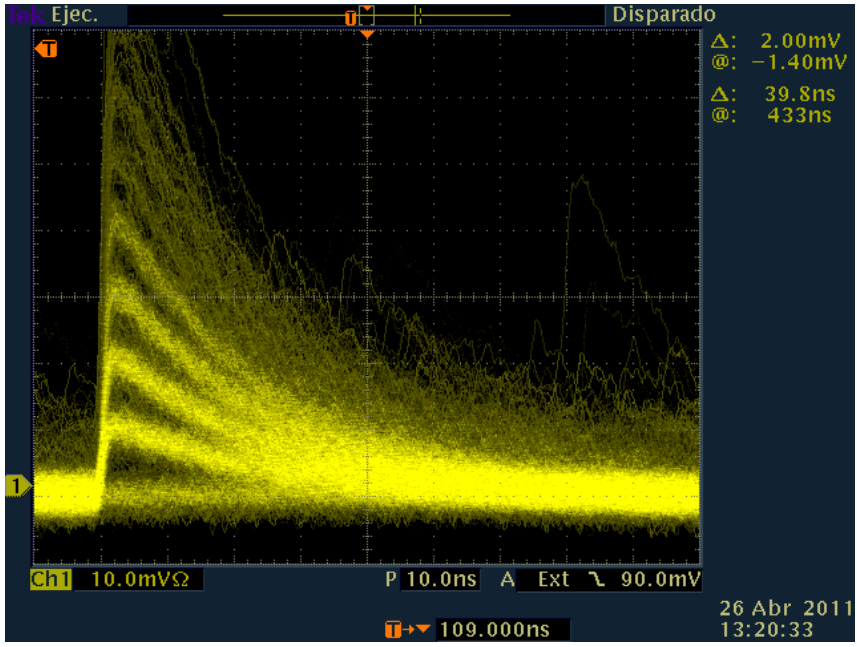


Figure 1.15: Typical signal from SiPM

1.2.3.5 After Pulsing

After Pulsing is a known effect which consists on the generation of a spontaneous peak output after a first peak. It is due to the trapping of some charge in the semiconductor defects. This charge has some probability to be released afterwards. If this charge is released will start a new avalanche. Typical release times range from few ns to several hundreds of ns. The first released charges (few ns) do not affect the signal because the micro-cells are not fully recharged, but will increase recovery time. Working at low temperatures will make release of this trapped charges slower, so the after pulses will be more noticeable.

1.2.3.6 Dark Count

Dark Count is one of the most important drawbacks of the SiPMs. Dark count is generated by spontaneous thermally generated carriers. Those carriers can then generate an avalanche in the micro-cell that will be identical to a *true* signal generated by a photon. The name of dark count comes from the fact that this signal will continue being generated without any illumination at all. The average number of avalanches in some time would give the expected count rate (normally in Hz).

The evolution of dark count rate with over-voltage applied to the device typically follows an exponential increase. In figures 1.16 and 1.17 dark count versus operation voltage is plotted by the manufacturer with two different thresholds to determine if dark count exists, one set to 0.5 photo electrons (0.5 micro-cell amplitude) and a second set to 1.5 photo electrons. For this reason over-voltage is kept to the minimum to obtain the desired gain. Since breakdown voltage, thus gain, thus dark count will change depending on temperature, it's important to keep under control the operating temperature of the device.

All referred commercial devices must be taken in the context of an evolving technology. Thus real numbers may have varied with time and newer models introduced. Values should be taken just as example.

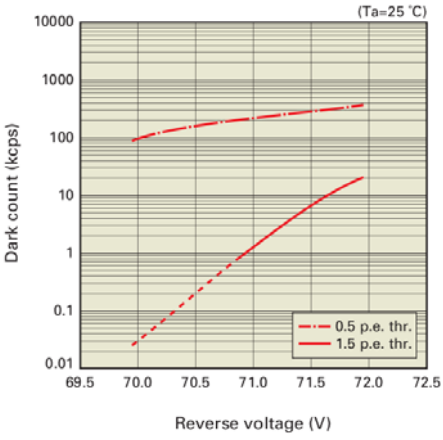


Figure 1.16: S10362-11-025 Dark Count variation with Voltage

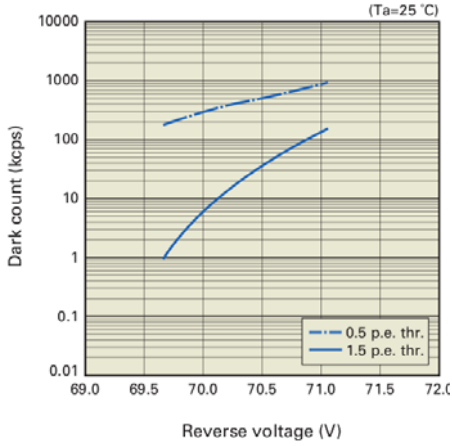


Figure 1.17: S10362-11-050 Dark Count variation with Voltage

1.2.3.7 Crosstalk

An important aspect is the crosstalk between different micro-cells. Crosstalk can be **electrical** or **optical**. Electrical crosstalk is produced when some carrier (electron or hole) produced by an avalanche of a micro cell crosses the boundary between micro cells producing a second avalanche in the neighbouring cell. Optical crosstalk is produced by photons generated in the avalanche going to neighbour micro-cell crossing oxide over the cells (optically transparent).

Worse crosstalk will increase statistical fluctuations in the signal generated from the device. Thus it should be reduced to the maximum. Several techniques are applied to reduce crosstalk. Most used ones are: increasing distance between micro cells and producing trenches between devices. Increasing distance has the inconvenient of reducing fill factor, and PDE so it should be avoided if possible. Trenches between devices are a much more reliable method since a barrier is produced between micro-cells and the loss of fill factor is the minimum permitted by the trenching technology. Trenches are often filled by some opaque material to avoid optical transmission.

1.2.4 Arrays construction

SiPM can be constructed in two different configurations depending on the substrate doping. A p-on-n device or a n-on-p device can be defined, see figure 1.18. The operation principle in both cases is the same but the final

behaviour is slightly different; in a p-on-n structure (figure 1.18, left) blue light will be absorbed in first nm of p+ layer. In this process an electron-hole pair will be created and the electron will drift to the junction and generate an avalanche with high probability. Longer wavelengths will be absorbed in deeper silicon on the n layers after the junction and holes will drift to the junction, leading to less probability of generating avalanche. Opposite to that, in a n-on-p structure photons with shorter wavelength will have less probability of generating an avalanche.

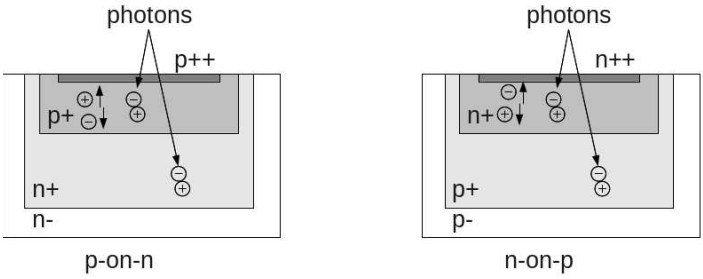


Figure 1.18: SiPM construction topologies

Those differences of the carrier probabilities lead to different PDE for a specific wavelength (see figure 1.19, p-on-n device, extracted from Hamamatsu technical information). The peak of PDE will move from around 400-450nm to 550-600nm depending on construction topology.

Observing carefully table 1.3 most scintillating materials provide the maximum signal in the range of 400-450nm. Then it is more interesting in order to maximize the final PDE to use a p-on-n structure.

If it is assumed that the substrate should be common to all channels of an array (to avoid wells and dead area between channels) the final device should have a common-cathode arrangement by construction. Discrete channels packaged together to construct arrays can also be produced, but the price to pay will be more dead area between channels. Those discrete channels could be pre-selected to achieve better overall behaviour in the array (gain uniformity between channels, dark count and operating voltage).

All referred commercial devices must be taken in the context of an evolving technology. Thus real numbers may have varied with time and newer models introduced. Values should be taken just as example.

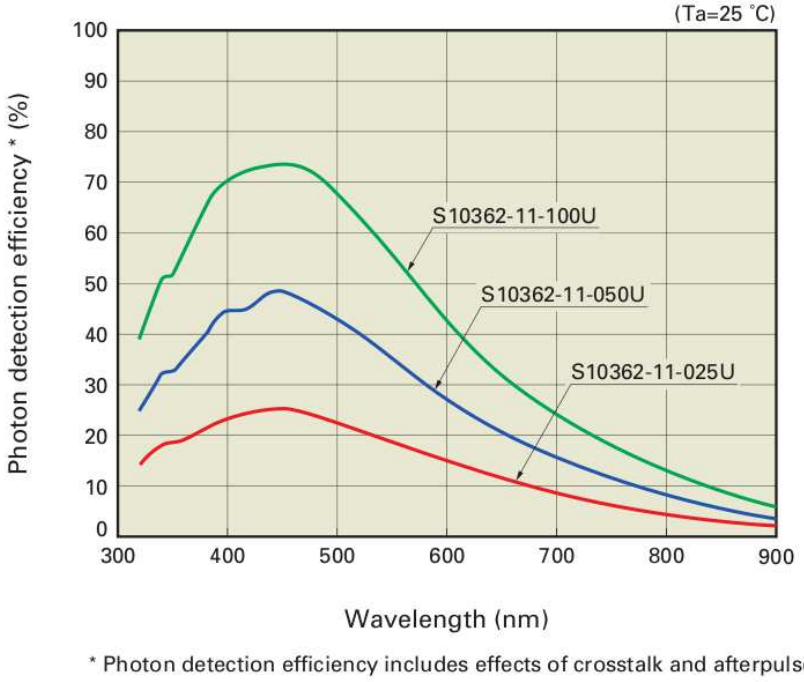


Figure 1.19: PDE variation with Wavelength

1.3 Scintillators

A scintillator is a material that exhibits emission of light (not resulting from heat) when excited by ionizing radiation. This radiation is composed of particles that individually carry enough kinetic energy to liberate electrons from an atom or molecule, ionizing it. When hit by an incoming particle the scintillating material absorb its energy and re-emit the absorbed energy in the form of light. Depending on the material, the excited state could be metastable, so the relaxation back out of the excited state is delayed some time (from a few microseconds to hours). First scintillator usage dates at the beginning of 20^{th} century[13] but gained attention in 1944, when Curran and Baker replaced the naked eye measurement with the newly developed PMT. This was the birth of the modern scintillation detector.

In this modern scintillation detectors, the first detector part in the path of the ionizing particle is the scintillating crystal (or could also be plastics or even liquids) used to convert it into a light burst. Then those light burst are converted into electrical current by a transducer (PMT, APD or SiPM) and processed. These crystals are not ideal and present an important timing spread in the photon emission process. Once the photons are produced they should arrive to the transducer following different paths, which will also increase the time spread in the detector itself, highly affected by the crystal dimensions[14].

Knowing well the behaviour of the crystals to be used is fundamental for the design of the readout electronics. Statistical simulations can be performed with the help of Geant4[15] to determine the final arrival time spread in the transducer input[17].

Figure 1.20: LYSO crystals[e]

On figure 1.20 a view of this transparent plastic crystals can be seen, manufactured by Omega Piezo as a standard or custom made product.

Often the desired properties of scintillators are: high density, high speed response, good linearity, radiation hardness and low cost. High density reduces the material size of showers for high-energy γ and electrons and the Compton scattered photons are reduced for low energy γ. High speed response, with reduced decay times, leads to better resolution in measurements and also

[e]Image from Ω Omega Piezo Technologies, Inc.

identification of the type of particle measuring decay time (different times are generated depending if they are γ and ions) and also useful to avoid dead time. High speed rise time will produce better timing measurements. Good linearity is mandatory for the measurement of energy in some range. Radiation hardness is needed to allow long life time of the detector since it will be normally placed in a hard environment (in the case of high energy physics or radiation measurement equipment). Finally cost is an important factor since most crystal scintillators require high-purity chemicals and sometimes rare-earth metals that are expensive. Many crystals also require expensive furnaces and long time (months) of growth.

Trying to improve the previous commented properties several types of scintillating materials have been developed:

- **Organic crystals**: Organic scintillators are aromatic hydrocarbon compounds. They have a typical decay time of a few nanoseconds. Most common types are anthracene ($C_{14}H_{10}$, decay time $\approx$ 30ns), stilbene ($C_{14}H_{12}$, 4.5 ns decay time) and naphthalene ($C_{10}H_8$, few ns decay time). They are very durable but their energy resolution is not optimal and can not be easily manufactured, so they are not often used. Anthracene has the highest light output and is chosen as a reference in organic scintillators.
- **Plastic**: Plastic scintillators typically refers to a scintillating material in which the primary fluorescent emitter (called fluor) is suspended in the base (a solid polymer matrix). Polyethylene naphthalene exhibit scintillation by itself and is expected to replace existing plastic scintillators. The advantage of plastic scintillators include high light output and fast signal (with decay time of 2-4 ns) and they can be shaped easily. Several combinations of bases and fluors lead to different properties.
- **Inorganic crystals**: Inorganic scintillators are usually crystals grown in high temperature furnaces often with a small amount of activator impurity. The most widely used is NaI(Tl)(sodium iodide doped with tallium). Newly developed products include $LaCl_3$(Ce), lanthanum chloride doped with Cerium, as well as Cerium-doped lanthanum bromide, $LaBr_3$(Ce). They are both very hygroscopic but offer excellent light output and energy resolution with a fast response and excellent linearity. LYSO has an even higher density, is non-hygroscopic, and has a higher light output in addition to being rather fast.
- **Gaseous**: Gaseous scintillators consist of nitrogen and the noble gases helium, argon, krypton and xenon. The detector response is

very fast (≈1 ns), they typically emit in the ultraviolet so some wavelength shifting is needed.

- **Glasses**: Most common glass scintillators are cerium-activated lithium or boron silicates. Glass detectors are particularly well suited for the detection of slow neutrons. Lithium is more used since it has greater light output. Their response time is ≈10 ns but their light output is typically low.

Typical properties of some inorganic scintillating materials are summarized in table 1.3. Organic ones present much lower density (around 1 g/cm^3) and lower light emission (around 50% of NaI(Tl)).

1.3.1 Phoswich

Phoswich[16] or "phosphor sandwich" is a combination of scintillators with two very different pulse shape characteristics (typically very different decay time) optically coupled to each other and to a common light sensor (typically a PMT). Analysis of the output signal can distinguish the scintillator originating the signal.

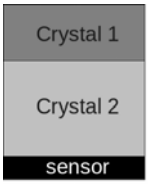


Figure 1.21: Phoswich

In figure 1.21 a schematic view of the configuration of a typical phoswich system is presented. In this configuration a thin crystal is followed by a second more thick one and then followed by the light sensor.

The main advantage of this technique is that without incrementing the number of channels it improves resolution of the direction of incoming particle. This is achieved because the interaction deep in the sensor is better constrained due to the determination of the crystal that generated the signal.

Scintillator Material	**Density (g/cm^3)**	**Wavelength at max.(nm)**	**Refractive index**	**Decay time(ns)**	**Light yeld (ph/MeV)**
NaI(Tl)	3.67	415	1.85	230	38000
CsI(Tl)	4.51	540	1.80	680,3340	40000,25000
$Bi_4Ge_3O_{12}$	7.13	480	2.15	300	8200
BaF_2	4.89	220,310	1.56	0.6,630	1500,9500
CeF_3	6.16	310,340	1.68	5,27	4400
$YAlO_3$(Ce)	5.37	370	1.95	27	18000
Lu_2SiO_5(Ce)	7.4	420	1.82	47	25000
$LaBr_3$(Ce)	3.79	350	1.9	27	49000
BC-400	1.03	420	1.58	2.4	10000
BGO:					
$Bi_4(GeO_4)_3$	7.13	480	2.15	300	5700
LSO:					
$Lu_2(SiO_4)O$:Ce	7.4	420	1.82	42	28500
GSO:					
$Gd_2(SiO_4)O$:Ce	6.71	440	1.85	60	7600
LYSO:					
$Lu_{1.8}Y_{0.2}(SiO_4)O$:Ce	7.1	420	1.81	40	40000

Table 1.3: Inorganic scintillators properties summary

1.4 SiPMs Applications

Silicon Photo Multipliers could be used in any application where a fast measurement of a small light signal is needed. Today's main applications are medical imaging and particle detectors.

Applications have very different timing constraints and expected signal requirements, but most of them include a huge number of channels and often the design uses arrays of detectors. In this work two applications are explored; first would be the detection of the gamma rays emitted by a radionuclide in the body to detect accumulation in different areas of the body (for Positron Emission Tomography scanners). And then for building tracking detectors with the help of scintillating material to produce light from the incoming particles (Scintillating Fibre Tracker at LHCb).

1.4.1 Medical Imaging

The usage of SiPMs in medical imaging applications is basically reduced to PET or Single-Photon Emission Computed Tomography (SPECT) systems. SiPMs offer similar or better performance than other types of sensors[20] with the advantages of it's low operation voltage, magnetic field tolerance and robustness. Permitting combined systems such as MR-PET.

1.4.1.1 Positron Emission Tomography

Positron Emission Tomography (PET) is a nuclear medical imaging technique to produce three-dimensional images of functional processes in the body. PET systems are based on detection of gamma rays pairs emitted indirectly by a radionuclide (tracer) introduced into the body. Data produced with the concentration of the gamma rays pairs and their arrival time is used in computer analysis to produce 3D images of their activity inside the body. Modern devices complete the image performing a second scan with CT-X-ray in the same machine although a combination with MRI (Magnetic Resonance Imaging) would be preferred due to the lack of added irradiation of the patient and better contrast in soft tissues.

The concept and basics of emission and transmission tomography was introduced by David E. Kuhl, Luke Chapman and Roy Edwards in the late 1950s. The first demonstration of this process in medical imaging was performed by Gordon Brownell, Charles Burnham and their associates at the Massachussetts General Hosbital in 1953[21]. In 1961, James Robertson and his associates at Brookhaven National Laboratory built the first

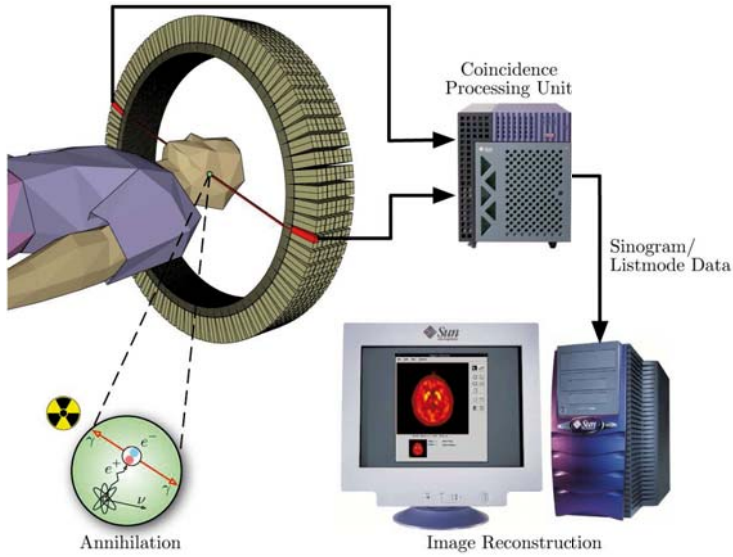


Figure 1.22: Schema of PET imaging system

single-plane PET scan, nicknamed the "head-shrinker". The developments at University of Pensilvania and Washington University School of Medicine produce first scanners[22][23].

A key element to the development and usage of PET systems is the parallel evolution of radiopharmaceuticals. In particular the development of several compounds (for example 2-fluorodeoxy-D-glucose, 2FDG) to determine its concentration in different organs by the scanner.

First scanners relied on two 2 dimensional arrays of detectors, but soon it was clear that a logical distribution for full readout detectors was to place it forming a ring around the patient. A schematic view of the system is shown in figure 1.22.

The detector block is usually formed by scintillator crystals (converting gamma ray into light bursts) followed by photomultiplier tubes (converting light burst into current pulses) and readout electronics (with amplification and time tagging of the input signal).

The final spatial resolution of the hardware depends on the size of the crystals and time accuracy of the whole system. In figure 1.23 a detailed view of the detector block can be observed, note the size of the photomultiplier compared with the scintillating crystals.

Combination of PET scans with CT-X-ray or MRI giving both anatomic and metabolic information in the same scanner is very useful since patient won't move between scans and will make easier to correlate both images. This is important in structures with anatomic variations or moving organs (outside the brain).

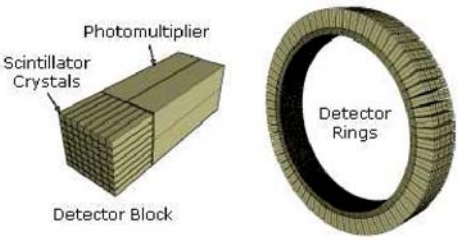


Figure 1.23: Detail of PET imaging system detector block and ring

Radionuclides used in PET scanning are typically isotopes with short half-lives such as carbon-11 (20 min), nitrogen-13 (10 min), oxigen-15 (2 min), fluorine-18 (110 min) or rubidium-82 (1.27 min). These nuclides are incorporated into compounds normally used by the body such as glucose, water or ammonia or into molecules that should bind to receptors. Such labelled compounds are known as radiotracers. PET technology can be used to trace the biologic pathway of those compounds. At present, the most used radiotracer in PET is fluorodeoxuglucose (FDG), with fluorine-18, used in all scans of oncology and most of neurology. Those radionuclides have traditionally been produced using a cyclotron in close proximity to the PET scanner. The minimization of radiation dose to the subject is the reason to use short-lived radionuclides but the proximity to cyclotrons (and cost) and the need of preparation of the tracer after irradiation of the isotope limit its adoption. Because of the half-life of fluorine-18 is about two hours, the prepared dose will need frequent recalibration and careful planning with respect to patient scheduling.

The raw data generated by PET scanner are a list of coincidence events representing near-simultaneous detections of annihilated photons (in a 180 degrees placed detectors). Each coincidence represents a line in space connecting the two detectors (line of response, LOR). Coincidence events can be gropued into projection images, called sinograms. Those sinograms are analogous to the ones produced by CT-X-ray scanners, but with much less statistics (at least three orders of magnitude less). As such PET data suffer from scatter and random events much more dramatically than CT-X-ray scans. In practice considerable pre-processing of the data is required.

PET systems will only accept as valid events the ones in the energy window produced by the gamma ray. This is around 511keV. If an event is around this energy and in coincidence with an other event at a 180 degree then it will be an accepted event. All the rest is discarded. To avoid system

bottlenecks it is important to take the decision if an event is saved or dropped as soon of possible in the detector chain.

Some crystals have spontaneous emission of light, emitting an spectra in the region of interest. As an example Saint Gobain's Prelude 420[24] is a lutetium based scintillator with a radioactive isotope generating 3 gamma ray cascade of 307, 202 and 88 keV, being the most probable a 597keV deposited in the scintillator. This can be useful for offline calibrations of the detector. This are the case of LSO and LYSO crystals, widely used in PET systems.

1.4.1.2 Time Of Flight

Time of Flight (TOF) is the name given to several methods to measure the time it takes for a particle to travel some distance. This measure can be used as a way to determine some property of the medium (velocity) or to know more about the particle. In PET systems the relevant events are detected easily using coincidence of two particles of 511keV at 180 degrees. It's an indirect measurement since particles generate some light and this is what is detected and processed. Since detectors (scintillator crystals) have a finite size (in 3 axis) the line where the event has been produced has some angular uncertainty (not an ideal line). If a time stamp is added on the two sides with time better than ns then the distance from the two detectors is also defined (the resolution will improve with the timing resolution). Using this technique the signal to noise ratio (SNR) of the events is improved, leading to less events needed for a given image quality.

1.4.1.3 Single-Photon Emission Computed Tomography

PET and SPECT systems are similar, they are based on the detection of the signal produced by a gamma rays. However the difference of SPECT system is the tracer used emits gamma radiation that is measured directly, whereas PET tracer emits positrons that annihilate with electrons a few millimeters away, causing two gamma photons to be emitted in opposite directions. A PET scanner detects the coincidence arrival in time of those gamma photons, which provides more precise localization information of the radiation event. Normally PET images have higher resolution than SPECT (which has about 1 cm resolution). SPECT systems are significantly less expensive than PET because they can use more easily-obtained radioisotopes.

To acquire SPECT images, the gamma camera is rotated around the

patient. The patient lies on a table that slides through the machine. Projections are acquired at defined points, typically every 3–6 degrees. A full 360-degree rotation is used to obtain an optimal reconstruction with a time needed for every position around 15–20 seconds, thus giving a total scan time of 15–20 minutes. Multi-headed gamma cameras provide accelerated acquisition and dual-headed with 180-degree spacing or triple-head cameras with 120-degree spacing are also used.

1.4.2 Particle Detectors

SiPM usage in particle detectors has been explored in several studies [19]. Its main usage is focused (but not reduced to) tracking systems, calorimeters, imaging Cherenkov counters and astroparticle detectors.

Tracking devices reveal the paths of electrically charged particles as they pass through and interact with suitable substances. Most tracking devices do not make particle tracks directly visible, but record tiny electrical signals that particles trigger as they move through the device. A computer program then reconstructs the recorded patterns of tracks.

A calorimeter measures the energy a particle loses as it passes through. It is usually designed to stop entirely or "absorb" most of the particles coming from a collision, forcing them to deposit all of their energy within the detector. Calorimeters typically consist of layers of "passive" or "absorbing" high-density material – for example, lead – interleaved with layers of an "active" medium such as solid lead-glass or liquid argon.

Electromagnetic calorimeters measure the energy of electrons and photons as they interact with the electrically charged particles in matter. Calorimeters can stop most known particles except muons and neutrinos.

In both detectors a scintillating material is directly coupled to the SiPM and the light produced by the particles is directly readout by the SiPM. The excellent photon counting capabilities and SNR of SiPM make its usage on these detectors a perfect option.

In calorimeters the results of reading out the light signal with SiPM have been proved to be similar to a classical PMT system.

In Cherenkov detectors the excellent photon counting capabilities and SNR are added to the fast response usable for sub nanosecond measurement. This factors make them an ideal candidate of the readout of imaging Cherenkov counters.

Astroparticle detectors on earth are based on the detection of the light burst produced by particles entering the atmosphere. SiPM characteristics, robustness and dynamic range make them a good candidate for the Cherenkov Telescope Array, CTA, competing with PMTs.

1.4.2.1 CERN and LHC

European Organization for Nuclear Research or *Conseil Européen pour la Recherche Nucléaire* (CERN) was funded in 1954 with the aim to became a world leading institution in this research topic. It was built beside the French and Swiss frontier, close to Geneva. Its buildings and sites extent in both sides of the frontier, and also the tunnel constructed to hold the most powerful accelerator created up to date, the Large Hadron Collider (LHC). During its history it has hold different accelerators and experiments leading to some discoveries and prizes. Today it has 20 countries as members of this international organization.

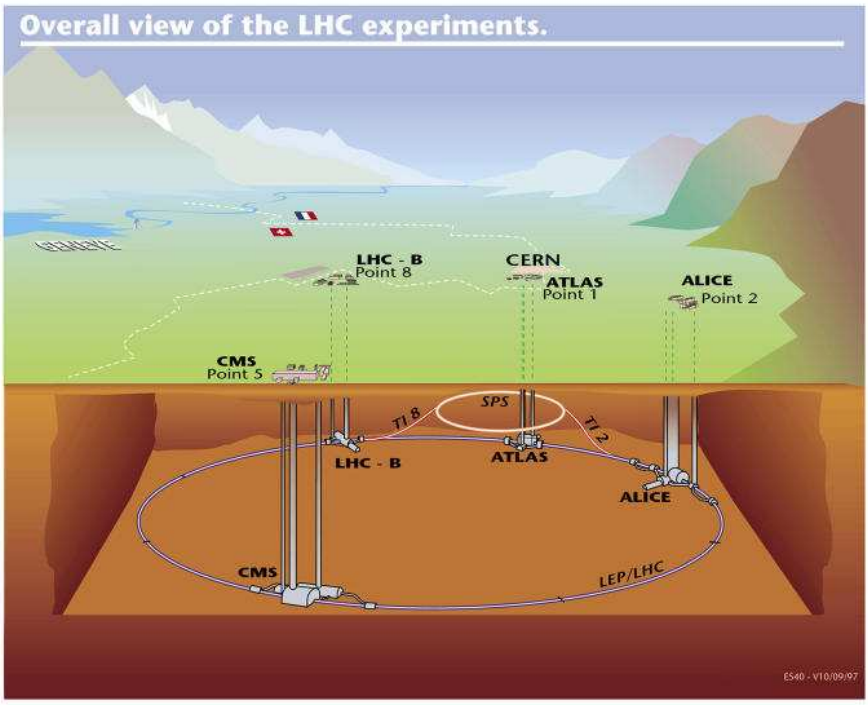


Figure 1.24: Overall view of the LHC experiments location[f]

The LHC is a proton-proton collider placed in the 27km tunnel previously build underground for the LEP machine. It was designed to run at 14 TeV center-of-mass energy. Four experiments among other smaller detectors are placed around the interaction points of LHC (see figure 1.24). The

[f]Image courtesy of CERN

experiments are placed on average at 100m below surface.

These experiments are:

- ALICE, dedicated to the study of the physics of strongly interacting matter and quark-gluon plasma in heavy nuclei (Pb-Pb) collisions with dedicated runs in the accelerator.
- ATLAS, a general purpose experiment with the objective to test the Standard Model at the TeV scale, and to search for the Higgs boson and physics beyond the Standard Model.
- CMS, another general purpose experiment with the aim of studying the mechanism of electroweak symmetry breaking, for which the Higgs mechanism is presumed to be responsible, and testing the Standard Model at energies above one TeV.
- LHCb, dedicated to the study of Charge-Parity violation and rare decays in the b and c quark sector.

1.4.2.2 LHCb

Large Hadron Collider beauty (LHCb) experiment is one of the ongoing experiments at CERN (Geneva). It is located at Interaction Point 8 of the LHC accelerator, previously used by the DELPHI experiment from LEP. The LHCb experiment is dedicated to the study of heavy flavor physics at the LHC. Its main aim is to make precise measurements of CP violation and rare decays of beauty and charm hadrons. Shown in figure 1.25, LHCb is a forward spectrometer with a polar angle coverage of approximately 15 to 300 mrad in the horizontal bending plane and 15 to 250 mrad in the vertical non-bending plane. This geometry choice is motivated by the fact that $b\bar{b}$ pairs produced at the LHC are produced in a large proportion in the same direction, either forward or backward.

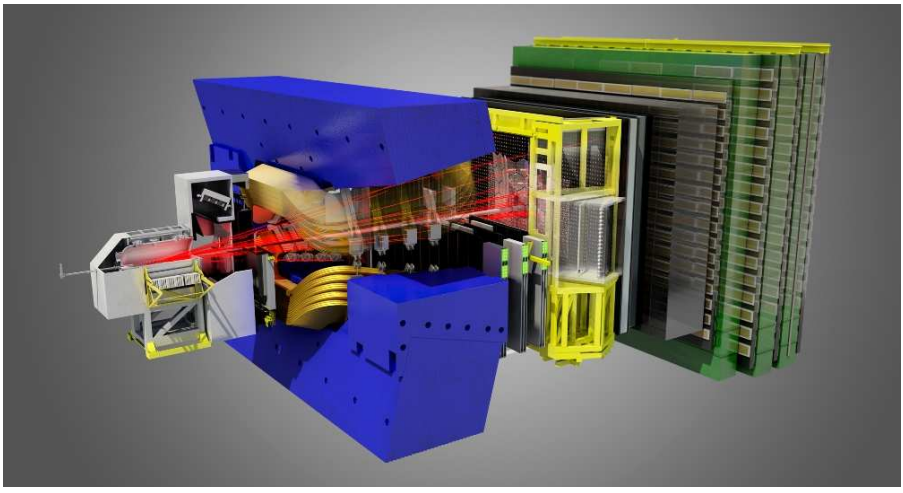


Figure 1.25: LHCb detector[g]

Starting from the interaction point, at the left of figure 1.25 and 1.26 (cross section of the detector), the LHCb tracking system consists of a silicon strip device surrounding the proton-proton interaction region (the Vertex Locator), a large area silicon strip detector (the trigger tracker, TT) located upstream of a dipole magnet which has a bending power of about 4 Tm, and a combination of silicon strip detectors and straw drift-tubes placed downstream of the magnet (the Inner Tracker, IT and the Outer Tracker, OT), forming the tracking stations (T1, T2 and T3 in figure 1.26).

[g]Image courtesy of LHCb collaboration

The combined tracking system has a momentum resolution that varies from 0.3% to 0.5% in the 5 to 100 GeV/c range.

Charged hadron identification in the momentum range 2 to 100 GeV/c is provided by two Ring Imaging Cherenkov (RICH) detectors (RICH1 and RICH2).

A calorimeter system is used for the detection of neutral particles and for the identification of electrons and photons. It consists of an electromagnetic (ECAL) and a hadronic (HCAL) sampling calorimeter. In addition, two scintillating planes separated by a lead absorber placed upstream of the ECAL are used to provide improved particle identification, especially for the first level of trigger. The first of these planes provides separation between electrons and photons (SPD), while the second one is used for tagging electromagnetic showers (PS).

Finally, muons are identified and measured by means of the muon chambers, which consist of five layers of multi-wire proportional chambers separated by iron absorbers (M1, M2, M3, M4 and M5).

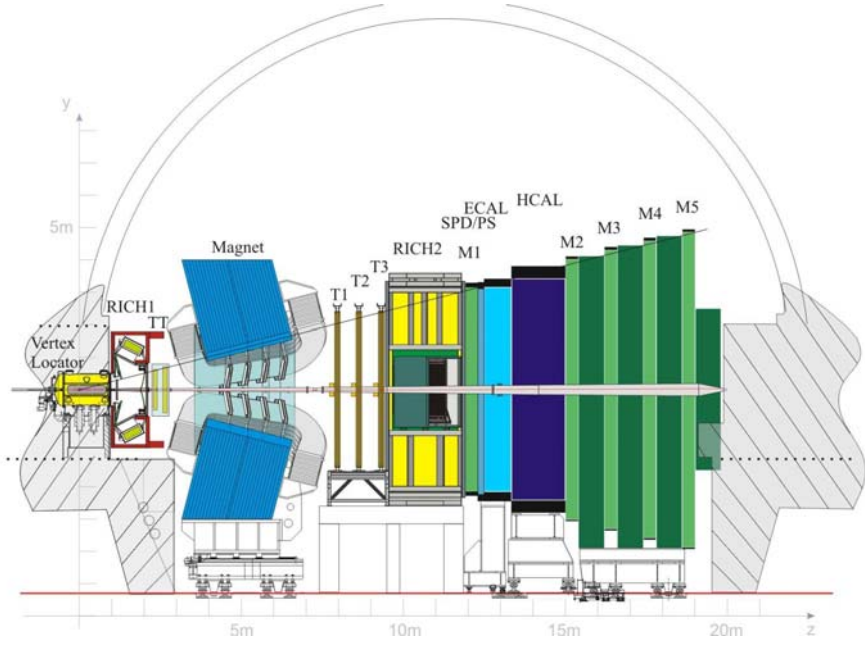


Figure 1.26: LHCb cross section[h]

[h]Image courtesy of LHCb collaboration

1.4.2.3 Scintillator Fibre Tracker

The current LHCb Tracker stations are composed of an Outer Tracker (OT) with straw tube detectors and an Inner Tracker (IT) with silicon strip detectors to cover the high-occupancy area near the beam pipe.

A new technology for the IT upgrade, based on scintillating fibres, was introduced in the Upgrade Letter of Intent[6], with clear fibres carrying the signal photons from the inner region to the detectors situated outside the LHCb acceptance.

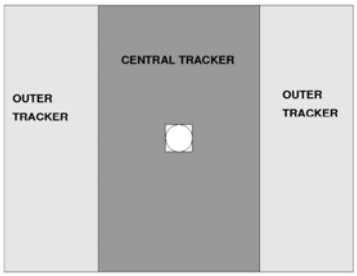


Figure 1.27: LHCb tracker upgrade layout

In the mean time, a new scintillating-fibre layout has been proposed (Central Tracker, CT), with 2.5 m long fibres covering the whole central region of the Tracker stations, from the LHC beam plane all the way to the top and bottom of the LHCb acceptance. In this option, the IT and several OT modules are replaced by the new scintillating-fibre modules (see figure 1.27). The decision has been taken that any change to the LHCb detector should be made such that the new implementation is compatible with operation at a leveled, i.e. constant, luminosity of $2\text{x}10^{33} cm^{-2} s^{-1}$.

In this new configuration, the existing outermost straw tube modules, four on each side, are kept as in the current LHCb detector and their electronics upgraded to allow readout at 40MHz. The central part (OT and IT) is replaced with scintillating fibre modules covering the full height of the detector. The upper and lower halves of the modules contain 2.5 m long scintillating fibres, separated with mirrors at the inner boundary and read out with Silicon Photomultipliers (SiPM) mounted outside the LHCb acceptance.

With this configuration, passive material in the detector acceptance is minimized and exposure to radiation is reduced for the SiPMs and FE electronics. One of the key development challenges will be to determine how the SiPM performance will evolve as a function of radiation dose and under what conditions these photon detectors will represent a viable solution for the LHCb CT. The radiation fluence at the SiPM location is expected to be of the order of $10^{12} n_{eq} cm^{-2}$. Besides previously described irradiation studies with 65 MeV protons and with neutrons from a PuBe source [6], SiPM samples have been placed in the LHCb detector at the bottom of the tracking stations during the 2011 data taking period.

Adding 1 mm of Pb shielding (and then 1 mm of Cd) between the SiPM and the polyethylene had little impact on the evolution of the leakage current. The effects of radiation damage can also be reduced by operating the SiPMs at low temperature. The dark current is predicted to be reduced by a factor 2 for about every 8°C temperature step. The option to cool the SiPM is being studied, with a temperature as low as -25°C being considered. This development effort will determine whether a combination of neutron shielding and active cooling will allow the SiPM lifetime to be extended to the required level. The signal deterioration due to radiation damage in the fibres was already mentioned and will now be measured on irradiated 2.5 m modules.

Figure 1.28: Cross section of a fibres module prototype

The techniques for the production of fibre matrices are still under development for both methods presented in the LoI, namely winding fibres on a cylindrical surface of radius larger than 40 cm or on a long cuboid. Dummy fibre matrices have been produced with both methods. Recently, a 2.5 m long sample module has been fabricated on the cylindrical barrel with scintillating fibres of 0.25 mm diameter. The sample contained five layers of about 100 fibres each. Figure 1.28 shows a photograph of the cross section of this 2.5 m long module. The distance between the centres of adjacent fibres was measured with an accuracy of 6 μm rms relative to each other.

Specially designed SiPM array is undergoing to fit the mechanical size of the module with the minimum dead area possible. The prototypes from Hamamatsu and Ketek consist in 64 channels arrays with a common cathode configuration. A mechanical view can be observed in figure 1.29, with a total size of 0.23x1.32mm^2 per channel, 96 micro-cells and 57.5x55μm^2 micro-cell size. The 128 channels are constructed joining to dies of 64 channels with the edge polished, dead area between pixels is kept to the minimum with a value of 0.25mm between two arrays.

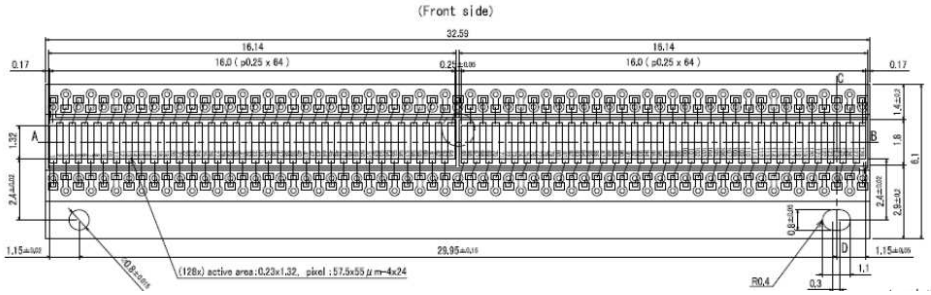


Figure 1.29: SiPM array prototype

1.4.3 Other Applications

As commented previously SiPM can be used in any application where measurement of light is needed. Most of applications using as sensor a PIN diode, APD or PMT can be substituted by a SiPM. Different uses from the previously commented include Laser Range Finder and imaging LIDAR systems[25].

A Laser Range Finder is a device using a laser beam to determine distance. The typical operation consists on the measurement of Time of Flight by sending a laser pulse in a narrow beam towards the object and measuring the time taken by the pulse to be reflected off the target and returned. Due to the speed of light and time measurement precision this technique can not be used for high precision sub-millimeter measurements. The pulse may be modulated to reduce the chance that the Range Finder measurement could be erroneous. It is possible to use Doppler effect techniques to measure whether the object is moving and its speed.

A LIDAR is a remote sensing technique involving the illumination of a surface by a laser light and studying the reflected light. Such systems normally use visible light or close in the spectra; ultraviolet or near infrared. A narrow light pulse can be used to scan most of surfaces and materials with very high resolution.

Typically light is reflected via backscattering and different types of scattering can be the basis for the LIDAR measurement, defining different types of LIDAR.

LIDAR is often used for the production of high resolution maps, meteorology or atmospheric research.

2

SiPM modelling

Correct model of the input signal to be processed by the analog electronics is crucial to achieve the desired results. For this reason a PSpice model has been chosen. This model permits simulation of both sensing device and electronics under design.

2.1 PSpice model

A reliable SiPM model is mandatory to produce accurate input signals for the electronics. A simple model [26] has been implemented and simulated using the standard SPICE tools in conjunction with the electronics. A general view of the circuit model can be seen in figure 2.1 with its parameters on table 2.1.

In this model [26] the different micro-cells in the SiPM are modelled as passive elements with the difference that the *fired* cells by some light have several more elements than the passive cells, acting as a load.

Since the base of a micro-cell is a diode with a *quenching* resistor (to avoid its destruction), the model comprises the union capacitance in parallel with the diode reverse voltage power supply plus a series resistor to the diode.

The quenching resistor is simulated with an ideal resistor in parallel with a parasitic resistance. The diode will start conducting when the power supply is greater than its breakdown voltage and an ideal switch is closed (simulating the incoming light). Apart from this parameters an interconnection parasitic capacitance is also included.

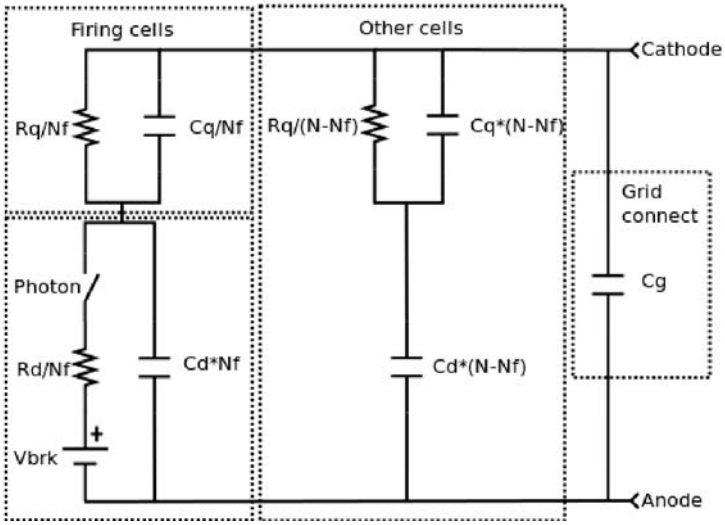


Figure 2.1: SiPM circuit model schematics

Parameter	Description
Rq	Quenching resistor value
Cq	Parasitic capacitance of Rq
N	Number of cells
Nf	Number of firing cells
Cd	Diode capacitance
Rd	Diode resistance
Vbrk	Breakdown voltage
Cg	Grid connect capacitance

Table 2.1: Model parameters

Other parameters such as parasitic inductance of the pins can also be added to the model in series with the anode and cathode connection.

2.1.1 Parameters extraction

To determine the quenching resistor, the easiest way is to produce an IV curve with the device biased in the direct region. At some point the diode will start to conduct limiting its current only by the resistor in series of the diode plus the quenching resistor. Since the quenching resistor is expected to be much greater than the device resistance the value of the slope of the curve (in the linear region) will be approximately the quenching resistor divided by the number of cells (all in parallel). In figure 2.2 the resulting voltage-current graph from the direct region of different devices can be observed.

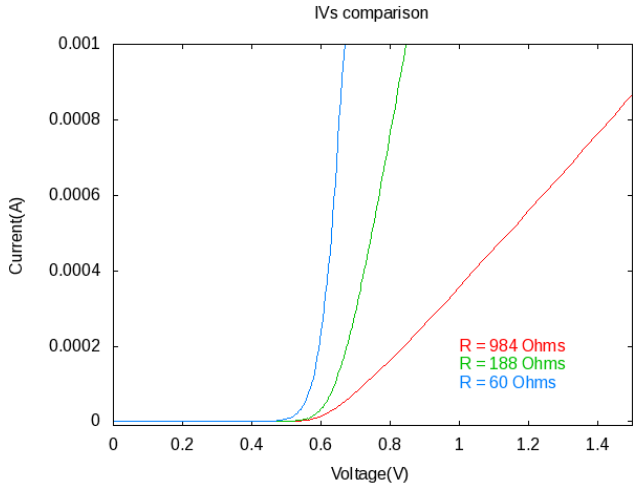


Figure 2.2: IV characterization of different devices

In order to determine the C_d and C_q sum, the charge variation of the output has been measured and plotted as a function of V_{op} value. On formula 12 [26] the relation between charge and capacitance can be observed. With this procedure V_{brk} can also be determined extrapolating the voltage when output charge should be 0. Measurements are plotted on figures 2.3 and 2.4.

$$Q = (C_d + C_q).(V_{op} - V_{brk}) \tag{12}$$

Finally the number of cells (N) and charge seen on the device terminals is specified on the datasheet. Assuming the terminal capacitance value is

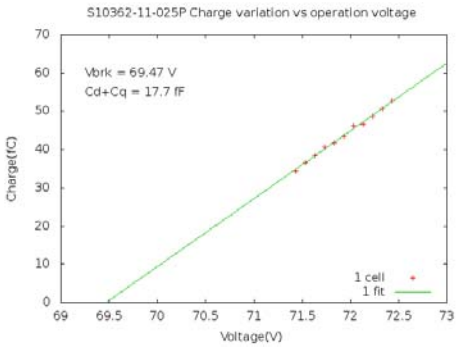


Figure 2.3: S10362-11-025P Charge vs V_{op}

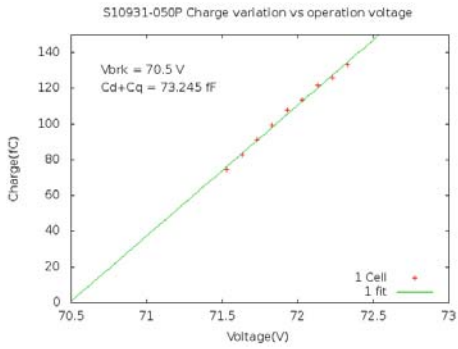


Figure 2.4: S10931-050P Charge vs V_{op}

specified in dc conditions, the C_g value can be extracted using formula 13 as documented in[26].

$$\begin{aligned} C_g &= C_\omega - N_{tot}C_d + \frac{\omega^2 C_d^2 R_q^2 N_{tot}\left(C_d + C_q\right)}{1 + \omega^2 R_q^2 \left(C_d + C_q\right)^2} \\ for \quad \omega &\rightarrow 0, \quad C_g = C_{tot} - N_{tot}C_d \end{aligned} \tag{13}$$

The only non specified and non directly measurable parameter is R_d but it can be estimated in the order of hundreds of Ω, not affecting the shape of the signal.

2.1.2 Measurement setup

Several measurements have been performed to obtain the desired parameters and cross check the model on real devices. A small test board was designed to do so, using the usual AC coupled measure, only changing load resistor from the usual 50Ω value to 1kΩ, since amplifier has a 50Ω input impedance. The output amplifier is a MAN-1LN, 500MHz. On figure 2.5 and 2.7 there is the circuit used for testing the dark count signals shape. On figure 2.6 a typical output with some light applied to a S10362-11-025P device can be observed. Measurements are done using a 300MHz bandwidth oscilloscope.

To calibrate the gain of the amplifier the SiPM signal has been measured at the input and output of the amplifier. The results can be observed in figure 2.8 concluding a gain of 60(35.5dB). Different amplitudes have been tested until saturation has been observed (at around 20 mV peak input signal).

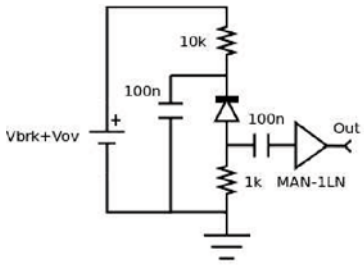


Figure 2.5: SiPM basic test circuit

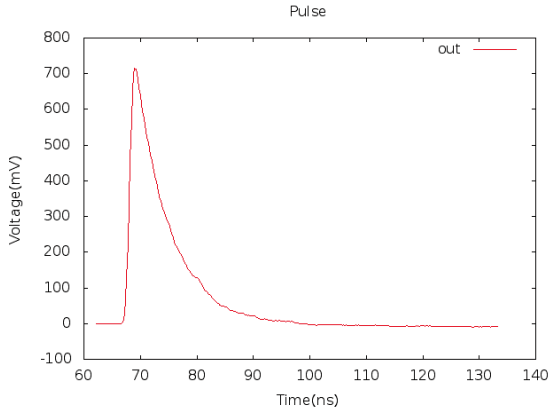


Figure 2.6: Output for illuminated S10362-11-100P

Figure 2.7: SiPM basic test board

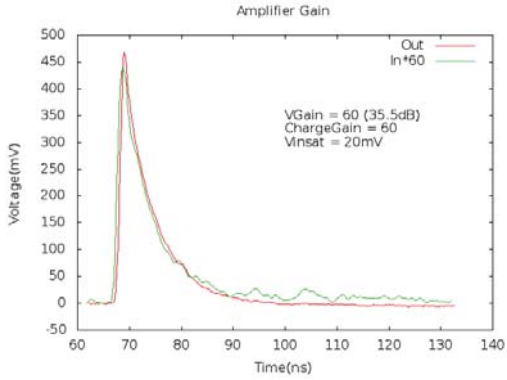


Figure 2.8: SiPM test board gain

2.1.3 Simulation results

Using the shape and amplitude of the dark count peak one can approximate the real values of the device with the simulations, summarized in tables 2.2 and 2.3. In figures 2.9 and 2.10 there is a comparison between the simulated pulse and the measured single cell fired at V_{op}.

In order to be more realistic the generation of a light pulse in a scintillator will have some time dispersion in the generation of the photons thus some cells will fire at different times; once the photons are produced they should arrive to the electronics following different paths which will also in-

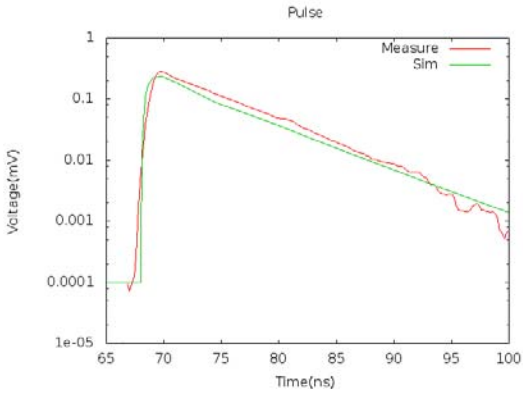


Figure 2.9: Single cell fired pulse and simulation

Parameter	Value
Rq	300kΩ
Cq	5.7fF
N	1600
Cd	12fF
Rd	1kΩ
Cg	15.8pF
$\mathbf{V}_{brk}$	69.47V

Table 2.2: S10362-11-025P parameters

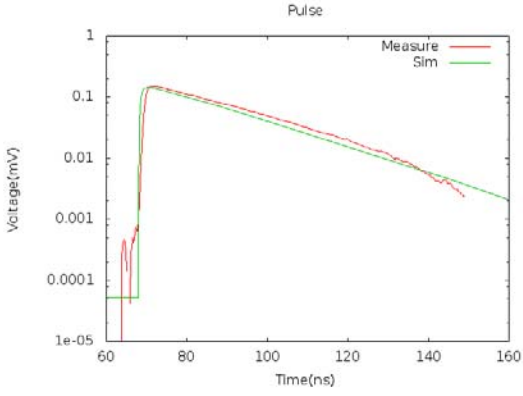


Figure 2.10: Single cell fired pulse and simulation

Parameter	Value
Rq	216kΩ
Cq	43.2fF
N	3600
Cd	30fF
Rd	1kΩ
Cg	212pF
$\mathbf{V}_{brk}$	70.5V

Table 2.3: S10931-050P parameters

crease the time spread in the detector itself, highly affected by the crystal dimensions[18]. This can be easily added in the model producing different branches of firing cells at different times, as shown in figures 2.11 and 2.12.

LSO segmented crystals are not expected to produce more than 15000 photons (for a 511keV event). So the light input should be between 50 and 15000 photons. With an overall efficiency of around 0.1 (including optical losses and PDE) a maximum of 1500 cells should fire (excluding any saturation effect in the device). A simulation with a typical fast light pulse generated from a crystal with incoming photons with a $\tau_{fall} = 20ns$

Device	V_{OV}	1k	510	200	100	50	20	10
S1032-11-25P	1V	0.252	0.367	0.525	0.626	0.68	0.7	0.8
	1.5V	0.383	0.556	0.815	0.93	1.04	1.25	1.4
	2V	0.514	0.747	1.07	1.25	1.31	1.51	1.8
	2.5V	0.645	0.949	1.36	1.56	1.76	2.05	2.3
	3V	0.782	1.13	1.61	1.85	2.06	2.45	2.8
S10931-50P	1V	0.22	0.384	0.76	1.15	1.58	2	2.3
	1.5V	0.335	0.582	1.16	1.74	2.4	3.1	3.3
	2V	0.45	0.78	1.56	2.35	3.24	4.2	4.6
	2.5V	0.56	0.98	1.96	2.99	4.04	5.25	6.06
	3V	0.68	1.19	2.35	3.51	4.88	6.2	**7.2**

Table 2.4: Peak current (mA) vs Z_{in} and V_{ov}

and a total of 1500 cells firing has been performed to simulate the maximum current under this conditions. The output of the device is connected to a fixed resistor with a value of Z_{in}. The results are summarized in table 2.4 for different overvoltage values. The typical waveforms can be seen in figures 2.11 and 2.12. Taking these numbers, a maximum input current of 10mA is expected from such devices.

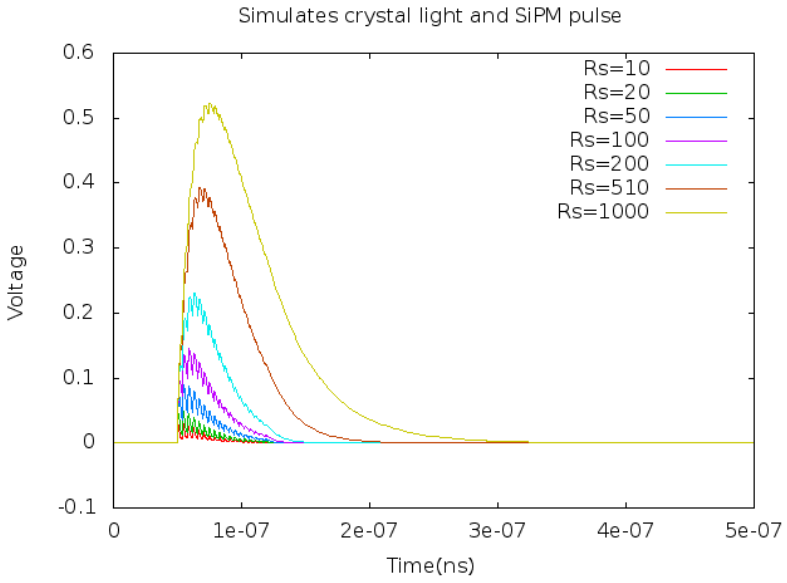


Figure 2.11: Crystal light simulation S10362-11-025P

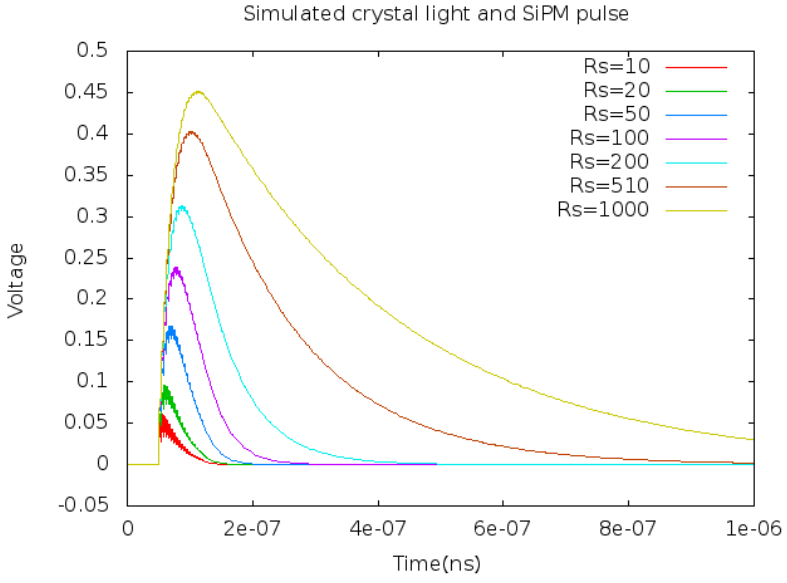


Figure 2.12: Crystal light simulation S10931-050P

2.2 VerilogA model

For the SciFi Tracker design a VerilogA model has been implemented using the described model as a basis. This model permits much faster computation of the output and avoids convergence parameters problems that often appear in the simulation of non linear devices (such as ideal switch included in the PSpice model). This model is being extensively used to simulate the different SiPMs under test for the SciFi tracker and to fit the electronics to its signal shape.

3

SiPM readout ASICs

The status of different integrated options for the readout of SiPMs is summarized in this chapter with detailed description of different architectures. It is important to note that probably not all existing devices will be listed and commented due to the amount of existing options. At the end of this section a snapshot of the "state of the art" in the development of integrated electronics specific for the readout of silicon photo-multipliers should have been provided.

The main results on different charge or current mode input stages is stressed. Typical pre-amplifier implementations are based on **Charge Sensing Amplifiers (CSA)** or **Current Mode** input stages. Each of them have some advantages and drawbacks being the speed of the current mode input the most significant advantage. The charge (or voltage) amplifier permits the connection of the sensor both in the anode or cathode, and normally is AC coupled in order to tune the DC voltage applied at the connection node. Current mode implementations only permit the current flow in one direction (if a good ratio between biasing current and input current range is desired) thus it must be fixed by design.

Due to different years of production and different technologies used in the production of the prototypes a direct comparison on charge or area can not be made. But in general terms a first approach on the order of magnitude of how this implementations deal with area and power can be obtained.

3.1 FLC_SiPM

FLC_SiPM[27] is a current mode ASIC designed for high energy physics. It was developed in Orsay (France) by the Omega group. It aims to provide readout of SiPMs for the International Linear Collider (ILC) hadron calorimeter. It is designed using a variable gain low-noise pre-amplifier followed by a variable shaper and Track and Hold (T&H). The output multiplexes the analog signal of several channels. An 8 bit DAC is added to every input to tune the High Voltage of the SiPM.

The hadronic calorimeter prototype for ILC uses scintillator tiles read out by SiPMs. The SiPM is coupled directly to the scintillator tiles and uses some coaxial cable to the electronics box. The connection to the ASIC is direct with a high voltage decoupling and cable matching components placed in both conductors of the cable (shielding and signal).

Architecture

FLC_SiPM provides a multiplexed analog output of the 18 channels. Each channel output is a shaped signal proportional to the input charge. A variable gain charge pre-amplifier followed by a CRRC2 shaper with a variable shaping time performs the analog processing and then feeds a track and hold. All bias is common to all channels. Channel architecture is depicted in figure 3.1.

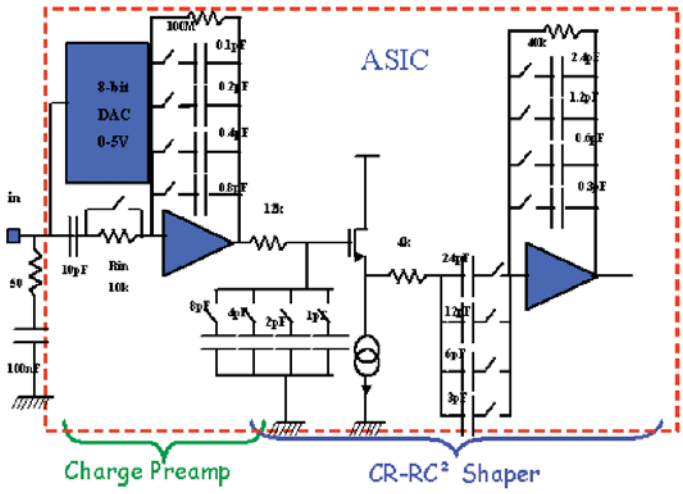


Figure 3.1: FLC_SiPM channel [27]

At the input node, an 8 bit DAC provides 5V voltage change to be able to tune the High Voltage per channel. After this node, the input is ac coupled to the pre-amplifier and followed by a resistor to perform a first derivative constant time. This resistor can be shorted. A low noise charge pre-amplifier follows with 1300 electrons of noise (compared to 10^6 electrons of a photo-electron). The gain can be controlled externally with 4 bits (setting the feedback capacitor value) from 0.7 to 10 V/pC. At the output of the pre-amplifier the signal is filtered using a CRRC2 shaper with a variable time constant selected externally with 4 bits from 12 to 180 ns. The fast shaping (called calibration mode) is used for calibration while the long shaping (called physics mode) is necessary to be compatible with the current readout.

Measurements permit to distinguish single photons (in calibration mode) and show good linearity with the different gain configurations (in physics mode).

3.2 MAROC

MAROC[28] ASIC stands for Multi Anode Read-Out Chip. In fact is a family of devices intended for the readout of Multi Anode PMTs. It was developed in Orsay (France) by the Omega group. The first prototype was OPERA_ROC in 2001 in AMS 0.8μm technology. The MAROC family started with porting this prototype to AMS 0.35μm SiGe CMOS technology. First version MAROC1 was a 64 channels prototype in 2004 with 12mm^2 and 5mW/ch power consumption. MAROC2 followed in 2006 and MAROC3 in 2009 with less power consumption and a Wilkinson ADC. The requirements of MAROC were defined by the ATLAS luminometer design with a valid trigger for signal above 1/3 photo-electron.

Architecture

MAROC3 version includes 64 low impedance pre-amplifier channels with 8 bit variable gain for each channel to equalize gain dispersion in PMTs. Shown in figure 3.2 the signal is first amplified by a low impedance preamplifier (about 50Ω). The amplified current then connects to a slow shaper and a sample and hold circuit to multiplex the analog output. A second sample and hold measures the baseline and the maximum. This analog voltage can also feed the Wilkinson ADC providing 8, 10 or 12 bit digital output.

In parallel to those charge signals 64 trigger outputs coming from two fast channels are provided. First channel is a fast shaper followed by low offset discriminator, second comes from a bipolar fast shaper with lower gain for higher signals followed by discriminator. The outputs of two discriminators are multiplexed to provide 64 outputs. The thresholds of the discriminators can be changed using two 10 bit DACs common for all channels. Two more outputs are available (OR1 and OR2) which are the OR of all channels from first or second discriminators. Like in MAROC2 the sum of up to eight preamplifier outputs can be extracted from the ASIC.

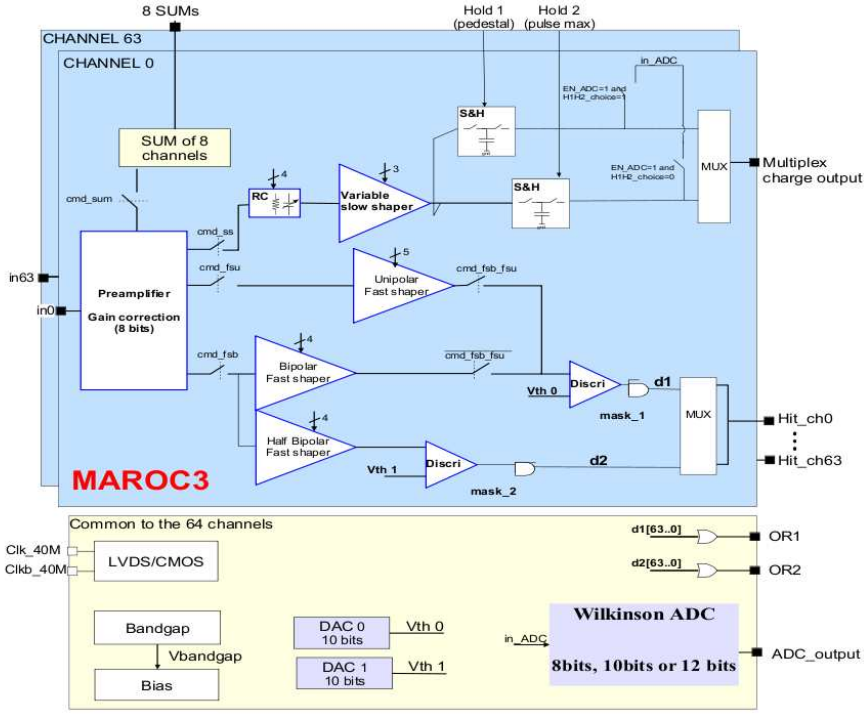


Figure 3.2: MAROC3 block diagram [28]

3.3 SPIROC

SPIROC2[29] is a System on Chip (SOC) designed to read-out the foreseen calorimeter from ILC equipped with SiPM. It was developed in Orsay (France) by the Omega group. The prototype is being built at DESY laboratory in Germany by the CALICE collaboration. They aim to design a dense, high granularity calorimeter (10 million channels). The design relies on small detector blocks with the readout electronics attached, thus power consumption of the electronics should be reduced to the maximum to avoid extra needs of cooling. Version 2c submitted in February 2012 improves noise performance and includes a new Time to Digital Converter (TDC).

Architecture

The analog part of the design includes 36 channels, each of them can tune the SiPM voltage at the input node using a DAC with 5V full-scale. Two input pre-amplifiers (see figure 3.3) process the same signal. One has a larger gain than the other permitting to handle smaller input signals. High gain pre-amplifier is followed by a fast shaper and a discriminator to detect a trigger condition. To measure the charge the output of the two pre-amplifiers are connected to a configurable shaper circuit and to a 16-deep switched capacitor array (SCA), storing the value (as a T&H).

Time is measured using a coarse counter running at 5MHz and 12 bits, while a more precise measurement is performed using a TDC. The value of the TDC is stored at the same time as the signal in the analog memories formed by the array of capacitors (SCA). Finally data is converted using a Wilkinson 12 bit ADC. Time resolution achieved by the TDC is around 150ps. Digital part manages all operations and also readouts the previously converted values from a memory (RAM).

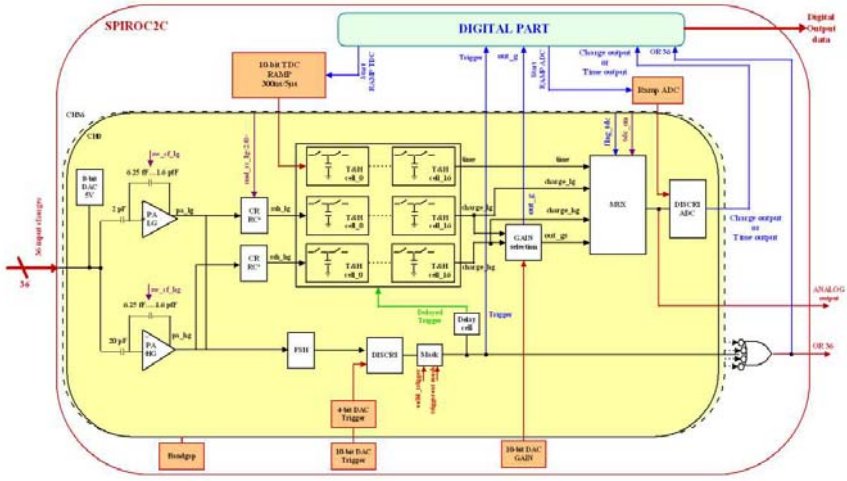


Figure 3.3: SPIROC2c block diagram [29]

3.4 NINO

NINO[31] was first developed to fit the constraints of the readout of the Multigap Resistive Plate Chamber (MRPC) detector at the ALICE experiment. Since the MRPC is build with extremely small gas gaps of $250\mu m$ between plates, it delivers a fast signal with excellent time resolution. For this reason the specifications to design this ASIC where to use differential input, to profit from the differential signal from the MRPC using a fast amplifier with less than 1 ns peaking time and input charge measurement by Time-Over-Threshold. The design was outsourced but the layout was done at CERN. With little adaptation[30] on the input connection it can be used for the readout of SiPMs.

Architecture

NINO input pre-amplifier is designed to fit the transmission line between the detector and the electronics. In the case of a MRPC a single transistor at the input will keep impedance to a low level enough to fit this requirement. After this pre-amplifier four low gain and high bandwidth amplifier stages follow (see figure 3.4). A slow feedback circuit keeps this input stages correctly biased. At this point some offset voltage can be added (similar to adjusting the threshold). Just before the output LVDS driver the width of the signal is incremented in width with a pulse stretcher circuit adding 10ns of duration.

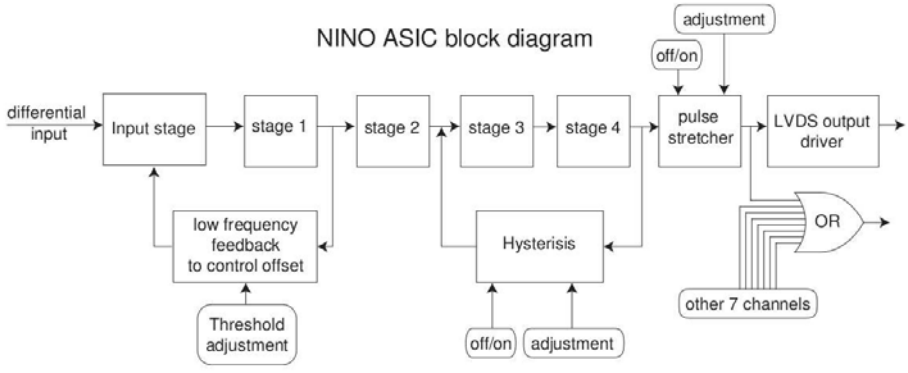


Figure 3.4: NINO block diagram [31]

3.5 PETA

PETA[32] is a 16 channel self triggered readout chip for time and energy measurement. It was developed for the HyperImage european project in Heidelberg. When a differential low-noise discriminator detects a hit signal it is time stamped and, in parallel, integrated. After integration it is digitized with 8-bit resolution. Readout is performed using a serial protocol. Several chips can be synchronized using an internal PLL that can be locked to the same reference clock.

Architecture

Simplified block diagram of the chip is shown in figure 3.5. The low noise differential input discriminator will trigger a hit when the input signal is above the programmed threshold. This hit will freeze the contents of the time counters (common to all chip). This time counters are formed by a coarse value (15 bit counter using reference clock) and a more fine counter coming from a 16 stage ring oscillator connected to the reference clock. The same hit signal will start the integration of the input signal for a fixed (and programmable) time period. When this period has elapsed the resulting value is converted to digital using a DAC and a comparator (DAC value is increased until comparator changes state). Once time stamp, integration and conversion has been performed the data can be read out using a serial interface based on shift registers. In addition some other common DACs are also included in the design. All analog blocks are fully differential while fast digital blocks use differential constant current logic to reduce emitted noise.

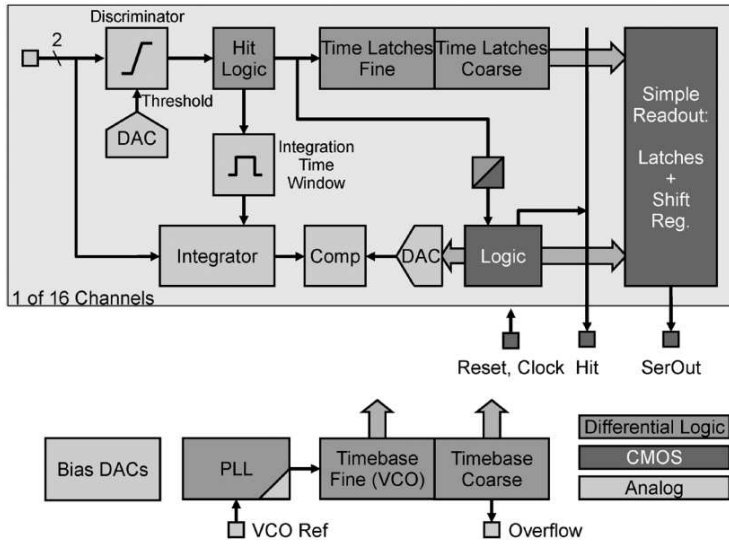


Figure 3.5: PETA block diagram [32]

3.6 BASIC

BASIC[33] is an 8 channel self triggered ASIC for SiPM readout. It has been designed by *Universita di Pisa* and *Politecnico di Bari*. A 32 channel version also exists keeping the same architecture. This ASIC uses a current mode input stage connected at the Cathode of the sensor.

Architecture

The BASIC architecture can be observed in figure 3.6. It features a double signal path, a fast one which uses a current discriminator to provide a timing signal, and a slow one which generates an analog signal proportional to the charge delivered by the sensor, which is finally converted to digital by an 8-bit successive approximation-register (SAR) ADC.

The first stage is a current buffer to keep input stage impedance low and to deliver a copy of the input current to the two signal paths with high bandwidth and virtual connection to ground in the input node. In the timing path a direct copy of the input current is used to generate a trigger signal in a fast current discriminator. All channels are ORed to obtain a single timing output. At the slow signal path another replica of the current is used, but now scaled by some factor to fit the desired dynamic range. It is integrated by means of a CSA with variable gain. A peak detector keeps voltage output of the CSA constant to process it easily. A baseline holder is added to control the DC value of the CSA output without affecting the fast signals in a very low feedback loop. The current buffer implementation also permits to fine tune the voltage applied to the SiPM input node by 1V.

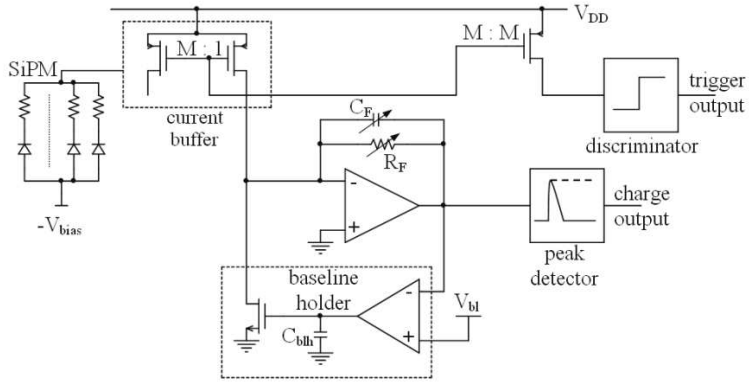


Figure 3.6: BASIC analog channel block diagram [33]

3.7 VATA64

VATA64-HDR16[34] is a commercial development lead by Gamma Medica - Ideas (Norway / USA). This evolution of the VA32HDR14 design which was intended for the readout of standard PMTs. Its evolution is more suited to readout of SiPMs and increase the number of channels to 64. The main application is in PET or SPECT systems. The design includes calibration capabilities, multiplexors for the readout and all the needed biasing and control of the channel operation.

Architecture

In figure 3.7 the blocks diagram of the analog channel can be observed. The pre-amplifier is a CSA using the virtual short circuit between inputs to define the DC value at the input, with one input connected directly at the SiPM and the other connected to a DAC. After the CSA the signal is AC coupled and derived in two signal paths, one for timing measurement and one energy measurement.

On the timing path a fast ($\tau_p \approx 50$ns) shaper follows the pre-amplifier and its output is connected to a fast discriminator with a programmable threshold. The output of the discriminator is connected directly to the output pad and to a Time to Analog Converter (TAC). The function of the TAC is to generate an analog signal proportional to the delay between the S&H and triggers in channels. The output of the TAC is multiplexed so it can be read out externally.

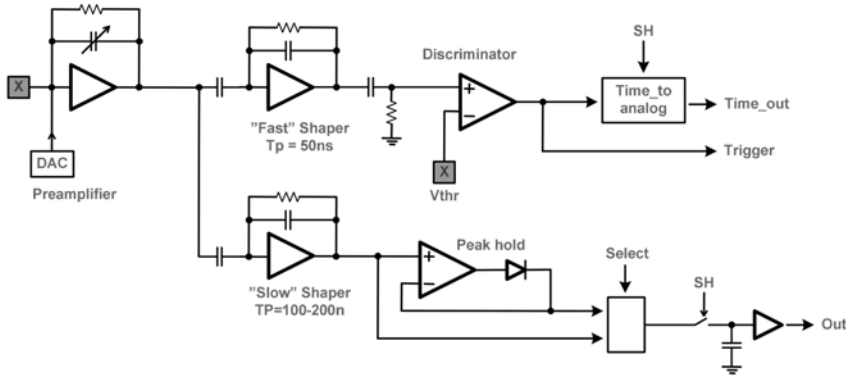


Figure 3.7: VATA64-HDR16 analog channel block diagram, extracted from specifications

On the energy measurement path a programmable slower (τ_p = 50 - 300ns) shaper is connected at the output of the pre-amplifier. This shaper is of a semi-Gaussina CR-RC type. After the shaper a peak hold circuit keeps the voltage to the maximum to be able to sample it and multiplex at the output. The user can select between sampling the peak hold output and the signal itself.

3.8 RAPSODI

RAPSODI[35] is a SiPM readout ASIC with two channels. This two channels can work standalone or in coincidence.

Architecture

RAPSODI (see figure 3.8) is formed by two identical channels plus some coincidence logic. Each channel consists on a preamplifier, comparator, peak detector and ADC. Some common coincidence logic permits to mix the output of each channel. The full system is controlled by an external FPGA.

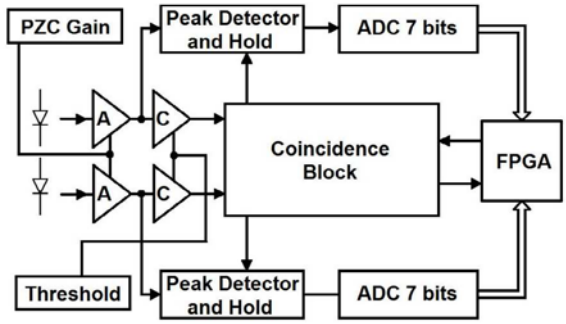


Figure 3.8: RAPSODI block diagram and external FPGA connection[35]

The pre-amplifier is formed by two folded cascode amplifiers with a configurable pole-zero cancellation circuit between them. This permits to avoid the undershoot of the signal and adjust to different SiPM timing constants. The pre-amplifier gain is also configurable by changing the value of the feedback elements. After the pre-amplifier the signal is split in two paths, one going to a peak hold circuit and a second one going to a comparator. The peak hold circuit has the function of keeping the maximum voltage constant for the ADC conversion (7 bit flash ADC). The comparator signal will generate a trigger signal when it is above the voltage threshold and act over the coincidence logic (if enabled).

3.9 TOFPET

TOFPET[36] is a 64 channels SiPM readout ASIC designed for the EndoTOFPET-US collaboration. The input stage can be designed for n or p type inputs (changing current flow direction). After a pre-amplifier, the signal uses two signal paths in voltage to obtain the desired timing and charge information.

Architecture

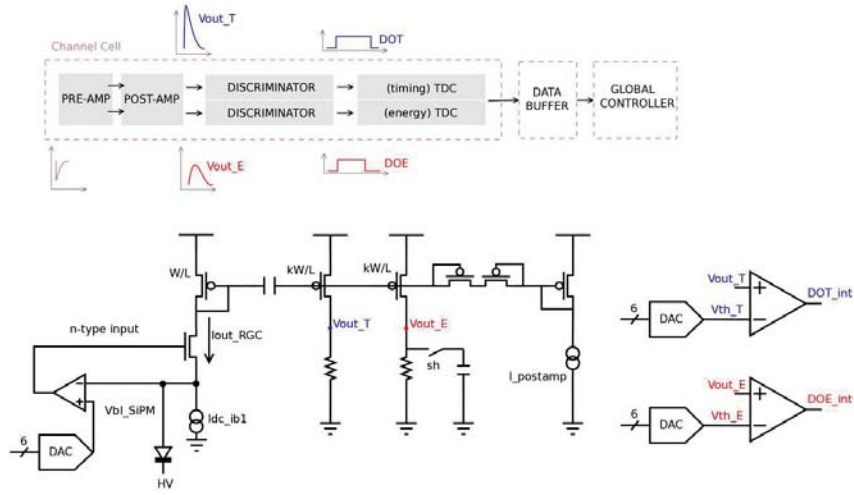


Figure 3.9: TOFPET channel block diagram [36]

The TOFPET ASIC readout channel starts with a current mode analog pre-amplifier. The signal is AC coupled and drives two mirrors to generate a voltage signal with the same characteristics as the current input from the SiPM. On the timing path the signal directly drives a voltage comparator with a threshold set by a 6 bit DAC. On the energy path the signal can be shaped with different time constants before driving an other voltage comparator generating a time-over-threshold (TOT) signal. The resulting digital values are then used in a TDC to generate a data set containing information on the time of the trigger and the TOT of the processed input signal.

To overcome the fact that the timing signal is susceptible to variations of the trigger time with the amplitude of the pulse, the charge information can be used to correct offline the timing degradation, due to time-

walk. The output of the TOT is highly non linear and will need the usage of external calibration and offline correction also to obtain better energy measurements.

Running at 160 MHz the chip yields a 50 ps time bin and dissipates 7 mW per channel (simulated for 40 kHz event rate p/channel) for high capacitance SiPM (320 pF).

One pad-free edge to allows to package two dies into a 128-channel BGA package.

3.10 Comparison tables

To compare several characteristics of the previous ASICs the figures of merit are summarized in next tables, 3.1 and 3.2. In first table there is a summary of outputs, outputs type, measurement, measurement accuracy and timing information. Second table a summarizes input stage, power, area usage and also technology.

The typical approach is to deliver charge and timing information, typically as a result of the OR of different channels. Normally this double measurement is performed splitting the signal at the output of the pre-amplifier and driving two different signal paths. A multi-channel architecture is always envisaged due to the high numbers of channels needed in current particle detectors or PET systems. The number of channels is typically a power of 2.

On tables we can see the most popular readout is to use charge based readout. Sometimes applying some shaping just at the pre-amplifier. This is a well known circuit widely used in particle detectors, but does not exploit the speed possibilities of the sensor. On the other hand current mode readout is less used and a connection with the sensor must be defined prior to design, in all examples cathode connection is used.

Differential implementations are not much used since it is not a natural connection of the sensor to the electronics (SiPMs are basically single ended). They offer much better performance in terms of noise but the price to pay is a much important power consumption which does not seem to compensate the advantages.

ASIC	Outputs	Measure	Accuracy	Timing output
FLC_SIPM	Multiplexed analog	Charge	-	No
MAROC3	Multiplexed analog and digital	Charge	Up to 12 bits	64 + 2OR
SPIROC2c	Digital time and charge	Time and Charge	12 bits and 150ps	Digital word
NINO	Digital	Time and width	60ps	LVDS
PETA	Digital	Time and energy	28ps rms	Digital word
BASIC	Digital and Analog mux.	Trigger and energy	650ps	OR trigger
VATA64	Multiplexed analog and digital	Time and Charge	-	Trigger and analog
RAPSODI	Digital	Trigger and Charge	-	Trigger
TOFPET	Digital	Time and Charge	50ps	Digital word

Table 3.1: Different ASICs outputs summary

ASIC	Input type	Technology	Input impedance	Channels	Area (mm^2/ch)	Power mW/ch	Year
FLC_SIPM	Charge	0.8μm AMS	AC couple	18	0.56	11	2004
MAROC3	Current	0.35μm SiGe AMS	$\approx$50Ω	64	0.25	2.5	2009
SPIROC2c	Charge	0.35μm SiGe AMS	AC couple	36	0.89	$\approx$2.5	2012
NINO	Diff. Charge	0.25μm IBM	$\approx$20Ω	8	1	40	2003
PETA	Differential	0.18μm UMC	-	16	0.66	86	2008
BASIC	Current	0.35μm SiGe AMS	$\approx$17Ω	8	0.88	>2.65	2008
VATA64	Current	-	AC couple	64	1	15	2007
RAPSODI	Current	0.35μm SiGe AMS	$\approx$20Ω	2	4.5	100	2008
TOFPET	Current	0.13μm	10-60Ω	64	0.39	7	2012

Table 3.2: Different ASICs properties summary

4

Input Stage

The major improve presented in this thesis is a novel input stage and current mode processing. The main challenge is to improve other implementations performance. Previous section presented several implementations of readout stages for SiPMs. One of the most common approach is to include a charge amplifier at the input. This is a good approach for a charge measurement but degrades the timing of the signal: The processing is slow for TOF measurement and if input impedance is high the recharge time of the SiPM will be incremented. Several studied implementations use current mode input stages which provide better time measurement results. This is the chosen input mode to obtain excellent timing measurement.

A recurrent architecture is to use multiple path processing for the different time and charge information. This approach seems to be the correct since it permits independent gain of the different signal paths and different signal shape processing. In current mode this signal can be reproduced easily using current mirrors just keeping in mind some control of the saturation of the mirrors; If the most gain mirror saturates it could avoid the other mirrors to work properly, so some saturation control should permit to extend the range of the other mirrors while the saturated one continues working.

A first prototype was submitted in July 2012 to test the most critical part in the design, the pre-amplifier. This first prototype, SiPMVFEr1 (SiPM Very Front End), uses a cathode connected device and buffers it's current to two different signal paths (time and energy) with a gain similar to 1 in

the time path and some attenuation in the energy path. Some saturation control circuitry must be added in the timing path to keep the energy current mirrors operating correctly after saturation of time output (see appendix A for details).

After this first attempt and during it's test more devices and arrays of devices started to show up. Most of them having the anode and cathode available for readout but some using a common cathode structure between channels. The decision taken with this new information was to change the input stage to be able to read in the anode (opposite current flow). Since results from first prototype where promising and reproducible by simulations it was decided to add more functionality to this second prototype in a multi-channel architecture (16 channels to start with). This prototype is FLEXTOT and it's input stage is described.

4.1 Architecture

The main goals of the input stage are to keep low input impedance and voltage controlled at the input node with a reasonable bandwidth. The input signal will be a current burst that should be replicated at the outputs. Full circuit of input stage (with some simplified blocks) can be observed in figure 4.1.

Requirements are achieved with two independent feedback loops, a high frequency feedback look to keep input impedance low, and a second low frequency feedback to keep voltage constant at the input node.

Several parts are highlighted in the schematics;

- HF_{fb} : High Frequency feedback loop to keep input impedance low.
- LF_{fb} : Low Frequency feedback loop to keep input voltage controlled.
- PROT : Protection circuit to avoid voltages over 2V or below 1V at the input (voltage outside this range would lead to over current flowing in the input stage).
- Current mirrors : A bipolar master cascode with a number of elements equal to n with it's slaves (with a, b and c elements) to replicate input current with different ratios ($\frac{a}{n}$, $\frac{b}{n}$ and $\frac{c}{n}$).

Transistor M_{fb} is shared by both feedback paths, while the rest of MOS transistors are used for biasing (M_b, M_{b2} and M_B) or as an active load (D).

The design can be scaled to obtain any number of desired current replicas with any gain.

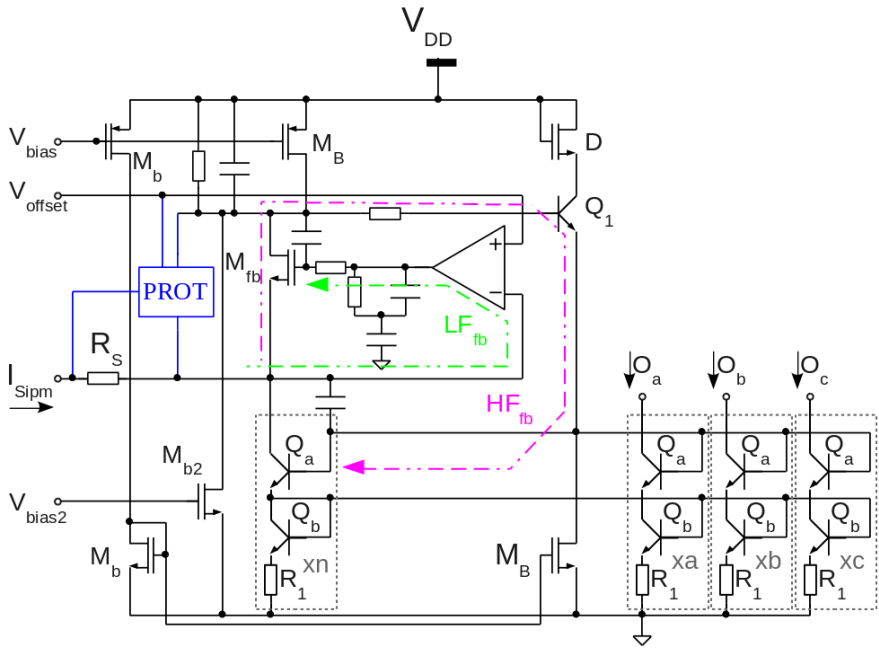


Figure 4.1: Input stage schematic

In following stages some protection circuitry has been added to achieve a correct output in the mirrors when the one with most gain is under saturation. The solution applied is the evolution of the one presented in CTA design[37].

4.2 Circuit analysis

Even though some other circuitry is present in the design, the most fundamental part is described by the two related feedback loops (HF_{fb} and LF_{fb}). Since superposition can be applied both are analysed individually.

Simulations have been performed during design stage to fine tune the final values of the different elements included in the circuit to obtain better results. And to cross-check functionality when the parasitic elements are added (layout and bonding inductance).

4.2.1 Low Frequency feedback loop

Using the simplified circuit depicted in figure 4.2 the behaviour of the circuit is described.

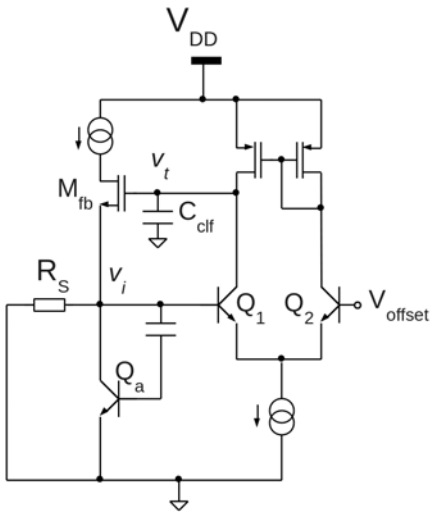


Figure 4.2: Low Frequency feedback loop simplified circuit

Transistors Q_1, Q_2 with it's CMOS load acts as a differential amplifier with a fixed gain of A_0.

The output of the amplifier is then buffered at the input by M_{fb} as in equation 14 and voltage at input forced to v_i'.

$$v_i' = -A_0.v_i.gm_{fb} \tag{14}$$

In large signal this voltage will be equal to V_{offset} since differential pair will keep $v_{diff} = 0$.

In order to avoid interference with high frequency feedback loop the overall cut frequency of this loop is kept at low values. Since the dominant pole of the circuit will be delivered by the input capacitance (of the SiPM) the cut frequency will be provided by equation 15.

$$f_{cut} = \frac{1}{2.\pi.\frac{1}{gm_{fb}}.C_{MAX}} \tag{15}$$

For typical values of 4 m and 300pF the cut frequency will be around 2 MHz.

In figure 4.3 stability simulations are performed for a typical case (low input capacitance) resulting with a Unity Gain around 2.5 MHz and a Phase Margin around 79 degrees. Montecarlo process and mismatch variations are also plotted in the same figure.

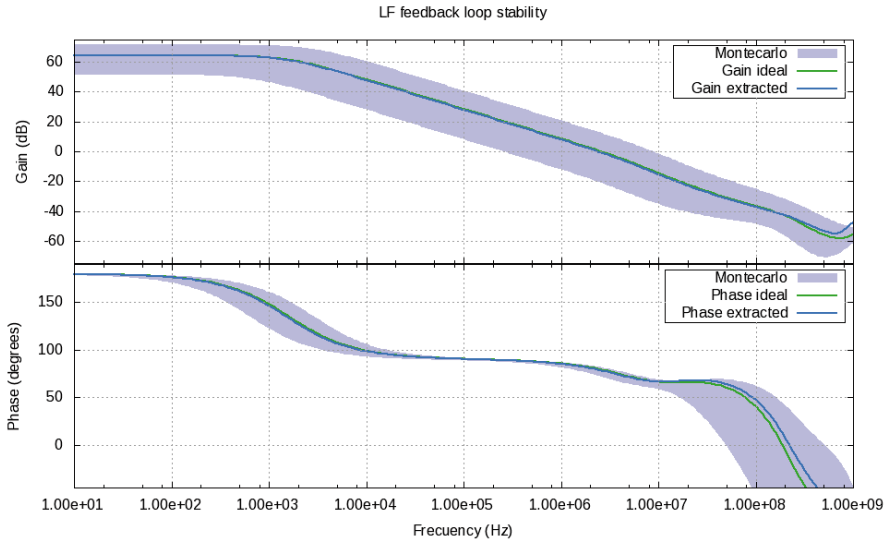


Figure 4.3: Low Frequency feedback loop stability

4.2.2 High Frequency feedback loop

Using the simplified circuit depicted in figure 4.4 the behaviour of the circuit is described.

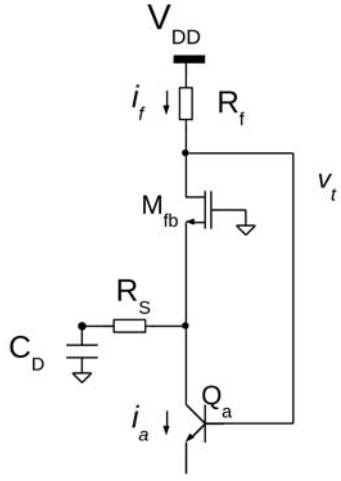


Figure 4.4: High Frequency feedback loop simplified circuit

The basic equations of the system are summarized;

$$i_f \approx i_c \frac{Z_i}{Z_i + \frac{1}{gm_{fb}}} \tag{16}$$

$$i_a = gm_a.v'_t \tag{17}$$

$$v_t = -R_f.i_f \tag{18}$$

$$Z_i = R_s + \frac{1}{s.C_D} = \frac{s.Rs.C_D + 1}{s.C_D} \tag{19}$$

The transfer function can be extracted from previous equations:

$$T(s) = -\frac{v_t}{v'_t} = gm_a.R_f.\frac{\frac{s.R_s.C_D+1}{s.C_D}}{\frac{s.R_s.C_D+1}{s.C_D} + \frac{1}{gm_{fb}}} \tag{20}$$

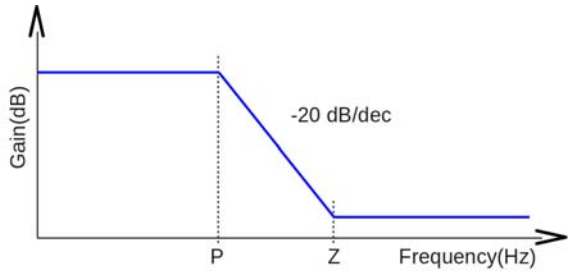


Figure 4.5: High frequency feedback transfer function

$$P = \frac{1}{2.\pi.\left(R_s + \frac{1}{gm_{fb}}\right).C_D} \qquad Z = \frac{1}{2.\pi.(R_s + C_D)} \tag{21}$$

The resulting transfer function has one pole and one zero, as depicted in figure 4.5.

With typical values of sensor capacitance around 30 pF, series resistor of 12 Ω and transconductance of 100 Ω pole is located at around 50 MHz and zero around 500 MHz. If the approximated GBW should be around 500 MHz, then;

$$GBW \approx \frac{gm_a.R_f}{2.\pi.\left(R_s + \frac{1}{gm_{fb}}\right).C_D} \approx 500MHz \rightarrow gm_a.R_f \approx 10 \tag{22}$$

But in previous assumptions (equation 16) the influence of Low Frequency feedback loop is not taken into account. This feedback will change the results;

$$i_f = i_c \frac{Z_i}{Z_i + Z_{iLF}} \tag{23}$$

$$Z_{iLF} = \frac{\frac{1}{gm_{fb}}}{A(s)+1} = \frac{\frac{1}{gm_{fb}}}{\frac{GBW_{LF}}{s+w_c}+1} = \frac{\frac{1}{gm_{fb}}.(s+w_c)}{GBW_{LF}+s+w_c} \tag{24}$$

Now transfer function is:

$$gm_a.R_f.\frac{(s.R_s.C_D+1).(s+GBW_{LF})}{s^2.\left(R_s+\frac{1}{gm_{fb}}\right).C_D + s.\left(R_s.C_D.GBW_{LF}+\frac{C_D.w_c}{gm_{fb}}+1\right)+GBW_{LF}} \tag{25}$$

$$\frac{C_D.w_c}{gm_{fb}} = \frac{C_D.GBW_{LF}}{gm_{fb}.A_0} \rightarrow R_s >> \frac{\frac{1}{gm_{fb}}}{A_0} \tag{26}$$

Equation 25 can be simplified to:

$$T(s) = gm_a.R_f.\frac{(s.R_s.C_D+1).(s+GBW_{LF})}{s^2.\left(R_s+\frac{1}{gm_{fb}}\right).C_D + s.\left(R_s.C_D.GBW_{LF}+1\right)+GBW_{LF}} \tag{27}$$

Circuit is simulated with the final schematic taking into account process and mismatch variations to check it's functionality (see figure 4.6).

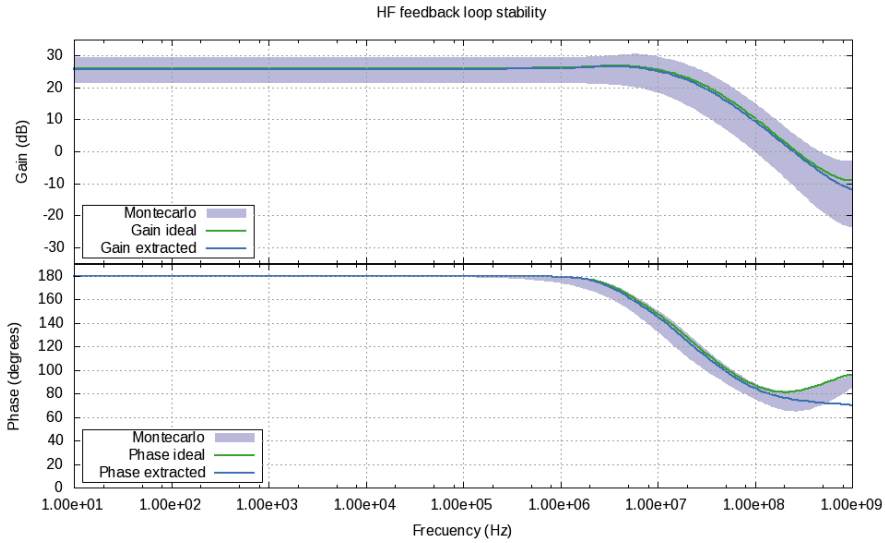


Figure 4.6: High Frequency feedback loop stability

4.2.2.1 Input impedance

As observed in formula 19 the input impedance has an inductive behaviour (increases with frequency). The final schematics are simulated taking into account process and mismatch variations and depicted in figure 4.7. As expected impedance is constant for low frequencies and equal to R_s, for medium resistances it raises to around 34Ω and for higher frequencies it starts rising fast over the circuit Bandwidth.

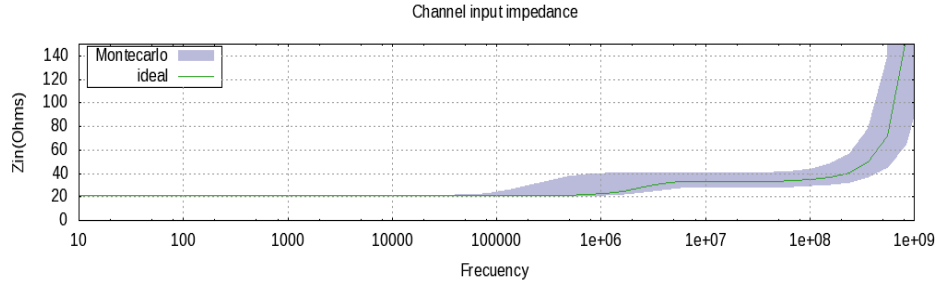


Figure 4.7: Input impedance

4.2.2.2 Input capacitance

In the case of a very small input capacitance:

$$R_s.C_D.GBW_{LF} << 1 \quad (28)$$

$$T(s) = \left(R_s + \frac{1}{gm_{fb}}\right).\left[s^2 + \frac{s}{\left(R_s + \frac{1}{gm_{fb}}\right).C_D} + \frac{GBW_{LF}}{\left(R_s + \frac{1}{gm_{fb}}\right).C_D}\right] \quad (29)$$

$$\left(R_s + \frac{1}{gm_{fb}}\right).C_D.\left(s + \frac{1}{\left(R_s + \frac{1}{gm_{fb}}\right).C_D}\right).(s + GBW_{LF}) \quad (30)$$

To obtain a stable feedback the condition of equation 31 is fixed. In this conditions dominant pole is $\frac{1}{\left(R_s+\frac{1}{gm_{fb}}\right).C_D}$, thus input node. The circuit will be more stable as much as input capacitance increases. To keep this condition for typical values GBW_{LF} should be kept below 5 MHz.

$$GBW_{LF} <<< \frac{1}{\left(R_s + \frac{1}{gm_{fb}}\right).C_D} \quad (31)$$

Simulation of final circuit phase margin relation with input capacitance shows an increase in the margin when capacitance value increases as expected by design (see figure 4.8).

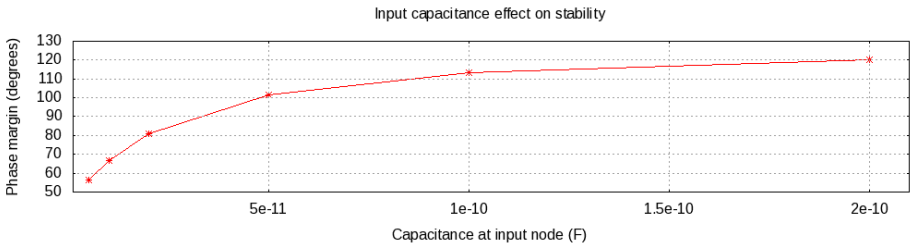


Figure 4.8: Effect of input capacitance to stability

4.2.3 Input voltage variation

Protection circuitry has been added at the input stage to avoid extra current consumption in the input stage. The input node voltage has been limited between 1V and 2V to avoid this condition. In figure 4.9 a simulation with schematic and extracted (post-layout) elements has been performed, including Montecarlo simulations with process and mismatch variations.

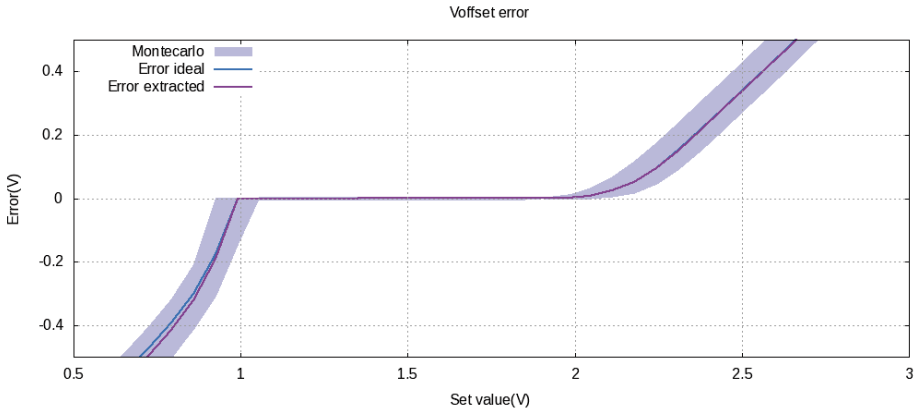


Figure 4.9: Input node voltage variation

The error on setting node voltage is plotted on y axis while desired voltage is on x axis. The limiting circuit keeps the input voltage on the desired range as expected. Thus a total adjustment rage around 1V is achieved.

4.2.4 Noise

Some simulations to characterize the input stage noise have been performed. In figures 4.10 and 4.11 series and parallel input referred noise is depicted. Note the low value in the frequency range of interest (2 $\frac{nA}{\sqrt{Hz}}$ in the series noise and below 30 $\frac{pA}{\sqrt{Hz}}$ in the parallel noise).

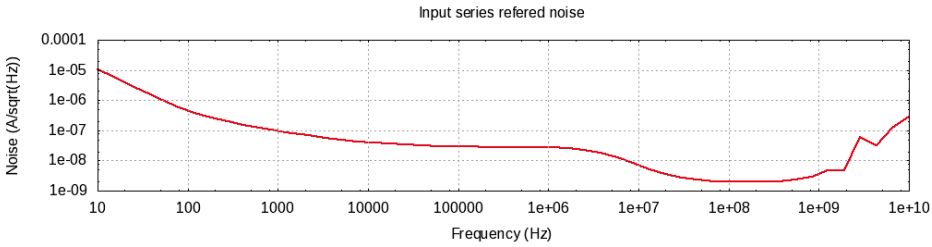


Figure 4.10: Series input referred noise

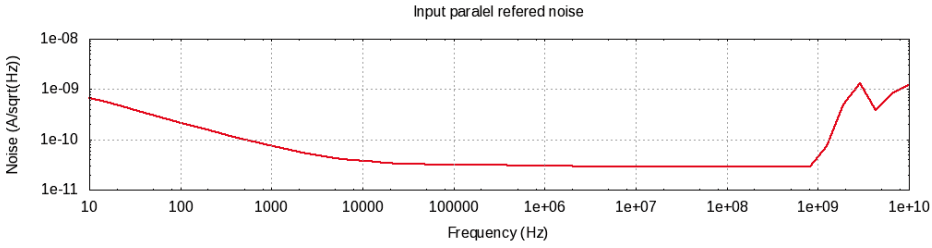


Figure 4.11: Parallel input referred noise

The integrated noise evolution with the input capacitance has also been simulated and is depicted in figure 4.12 with a slow increase with input capacitance value.

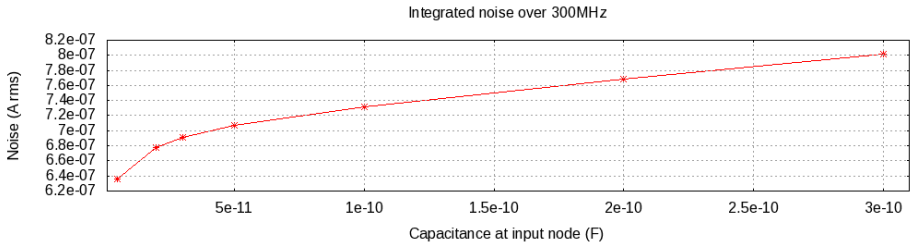


Figure 4.12: Integrated noise evolution with input capacitance

5

Design for PET applications

The design of the readout of a PET scanner is probably one of the most direct applications for SiPM. Current PET scanners provide sufficient imaging capabilities to be the most sensitive molecular imaging technique. Its fast and successful development has allowed this technique to be implemented in practically every large hospital and biomedical laboratory in developed countries.

Three are the main specifications to be improved in state-of-the-art PET systems: First the compatibility with morphological imaging systems with less radiological risks than CT; PET provides a functional image but the intakes providing information of metabolic functions, lesions or abnormal functionalities can only be properly evaluated if the PET image is merged within a morphological image of the body. This is usually provided by computed tomography (CT), with the problem that this technique provides a non-negligible radiological risk. Second the improvement of spatial resolution (around 1 mm for preclinical and beyond that figure for human whole body systems). Third the improvement of detector efficiency.

Current PET technology integrates CT or magnetic resonance imaging (MRI), providing the clinician with both anatomical and functional information. Presently there are commercially available PET-CT scanners capable of simultaneous acquisition of both imaging modalities from major vendors (Siemens, Philips and General Electric), and only one truly simultaneous PET-MRI, the mMR scanner from Siemens. The major problems for PET-MR compatibility are the need for replacement of classical

photo detectors by high gain semiconductor photo detectors (such as SiPM) and new challenging requirements of RF and magnetic compatibility of the front-end electronics attached close to the detector ring.

Recent technological developments have made possible the implementation of time-of-flight (ToF) techniques in PET scanners. These techniques improve the image resolution and enhance the efficiency of the system by reducing the uncertainty of the location of the positron source along each PET line of response (LoR). While most PET-CT systems feature ToF capabilities to improve sensitivity and overall image quality, particularly in the case of large patients, PET-MRI systems do not have this capability because of the use of silicon avalanche photodiodes (APDs) as light sensors, which are not fast enough. The use of faster SiPM in several prototype detector designs is pushing towards ToF, however these sensors require very fast electronics in order to preserve their excellent timing properties. New ASIC designs with fast response for the readout of SiPMs, capable of operating in strong magnetic fields, are being pursued by several groups, aiming towards setting a new state of the art in molecular imaging: simultaneous PET-MRI hybrid systems featuring ToF PET.

A present technological limitation derived from the design of PET detector elements is the parallax error, defined as the uncertainty in the location of the photon interaction position in the detector due to the thickness of the crystal. Conventional PET scanners are unable to provide a 3D interaction location in the detector, thus introducing an uncertainty in the depth of interaction. Since the average detector thickness is around 20 mm, this becomes a non-negligible problem for off-centered LoRs, mainly in small ring PET detectors. Several solutions have been implemented to address this problem, such as double readout, phoswich and using statistical methods, but with limited success.

Regarding the improvement of the spatial resolution, trends move towards replacing the simple analog detector readout techniques (cost-effective for commercial development) with reduced number of electronics channels by more complex electronics, coupling one electronics channel to each single crystal in the detector block. This will allow the use of signal processing to improve the photon position identification. But it will imply more complexity, which might turn out in an unacceptable increase of the price. The only way to advance in this approach is to develop custom integrated electronics capable to provide a large amount of detector channels (>64 per detector block) plus digital signal processing, providing to the next electronics readout modules a fully processed data array [p, t, E] (3D inter-

action position, time mark of the event and deposited energy). Therefore, it is most likely that the way to improve the spatial resolution will be linked to the development of more complex, cost-effective digital front end integrated electronics.

In terms of detector efficiency, there are two direct ways to improve the current figures: New scintillators, with larger density and higher atomic number but providing excellent specifications on light yield and fast signal, or thicker detector with current materials. On the one hand, the search for new scintillator materials is not evident, and has not provided in the last years relevant results. On the other hand, the use of thicker detector crystals has a limit due to geometrical factors: the light output in a crystal detector with an area in the order of 2 mm x 2 mm becomes inefficient when the crystal exceeds a certain thickness. One way to increase the detector efficiency while avoiding the intrinsic limitations described above is to use non-segmented detectors, i.e. monolithic detector blocks. Some key researches on new PET technologies (see references [38],[39]) foresee that the next generation PET detectors will be monolithic-block detectors coupled to arrays of Si-PMs supported by statistical-based estimation algorithms that locate events in the crystal block in three dimensions.

It is clear that a path to advance towards the next generation PET scanners (MR-compatible, ToF capable, high efficiency, high resolution) is related to the capability of providing cost-efficient, reliable, accurate, fast front-end electronics with digital processing capabilities. Only a reduced number of institutions and companies in the world have resources to face such challenging electronics development.

Although the most usual readout technique is based on integrated charge pulses digitized by ADCs, the time-over-threshold technique (ToT) has become a promising alternative in the last years. The ToT technique is based on digitizing the time a signal spends over a fixed threshold. The leading edge provides the information on the time of arrival of the photon and the time lapse between the leading and falling edge supplies the energy information. ToT has an advantage of a conventional pulse height system with respect to circuit integration and power consumption since ToT can be composed simply and without an ADC. A higher level of integration would allow PET scanners based on the individual readout method to achieve both a high count rate and better spatial resolution. ToT is now very often applied in High Energy Physics (HEP) for indirect amplitude measurement with moderate resolution, for instance in tracking, or in medical applications [41],[42],[43]. A survey in the 2011 IEEE NSS MIC Conference reveals

that research institutes in Europe (Italy, Poland, Czech Republic), Japan and Canada are active in this field, providing promising results. Typical ToT method suffers from poor linearity, but the non-linear relationship between energy and time, properly processed, can be useful to provide compression (higher dynamic range) or faster conversion time. Linear ToT methods can provide better resolution and are based in constant current discharge of a capacitor.

5.1 Requirements

Good definition of the requirements will lead to a prototype with minimal or no changes to be done to fit the final application. One of the most important things for defining specifications in this case is the Sensor to be used. For this reason some emphasis has been done in previous sections in the characterization and modelling on various Hamamatsu devices with different cell sizes. In common PET systems seems that the only usable device is the 3x3mm sensor. This is because with a reasonable size it can achieve the desired dynamic range and PDE needed by the incoming light from an LSO / LYSO crystal without saturation in the range of PET energies. Some other manufacturers such as SenSL or KETEK have similar products with reasonably similar characteristics for PET systems. This wide sensor options leads to some adjustable parameters in the signal processing since they will provide different signal shape, PDE, crosstalk and dynamic range.

5.1.1 Number of channels

Common PET systems use a detector block with an array of sensors. Those arrays are typically a 6x6 or 8x8 (formed joining smaller arrays of 3x3, 4x4 or 2x2). On the detector block there can be a monolithic crystal block over the sensors covering all the area or a segmented crystal block on every channel. If a monolithic crystal is used the light will spread over several channels, if few channels are used and summed the final measure can be weighted and measure with most precision the originating point of the light (leading to better resolution). In a similar way if the crystal is already segmented the resolution will be defined by this segmentation, but more signal will be present in every channel (all light goes to the same sensor).

As PET systems become more compact, the number of channels and its density increases so some important efforts have been done to reduce the readout channel number. The most typical case is to sum the rows an

columns [46]. Thinking on a discrete implementation this solution seems a good option. But on an integrated basis it doesn't seem to be so much important. All channels would need a connection to the readout electronics so if a single digital line is used for the output of the measured signal it will have a symmetric input output structure. With this approach it can be decided afterwards if the signal should be added or other processing having all the information is needed.

To sum up a reasonable goal for the number of channels should be as close as possible to the sensors array. If that number can not be achieved a divisor is the most desirable option.

5.1.1.1 Packaged electronics power consumption

Initially power consumption is not constrained, but a reasonable power consumption should be obtained to avoid cooling systems. The thermal circuit is depicted in figure 5.1. With only the junction to case resistance and the case to ambient resistance[45].

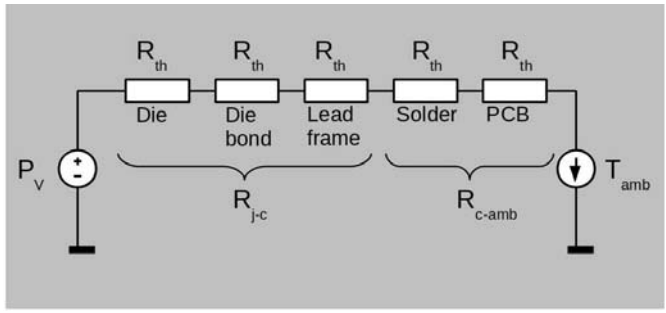


Figure 5.1: Thermal circuit

Assuming a typical thermal resistance (R_{j-c}) of a QFN package with exposed pad of 7°C/W, a typical thermal resistance from the case to the ambient temperature (R_{c-amb}) with no air flow of 50°C/W, a maximum operating temperature of the junction ($T_{j_{MAX}}$) of 125°C and a maximum ambient temperature ($T_{amb_{MAX}}$) of 70°C, the maximum power consumption ($P_{V_{MAX}}$) can be calculated easily in 32.

$$P_{V_{MAX}} = \frac{T_{j_{MAX}} - T_{amb_{MAX}}}{R_{j-c} + R_{c-amb}} = \frac{125 - 70}{7 + 50} = 0.96W \tag{32}$$

According to previous calculation a maximum of ≈ 1W for the full processing electronics should be achieved to avoid any cooling if a 64 channels typical system is used then the consumption of a single channel should be around 15mW.

5.1.2 Rate constraints

An optimal design on the detector should avoid any dead time produced by the signal processing. This would reduce the acquisition time to obtain the needed statistics to generate an image. The expected gamma ray generation is in the order of kHz (below 1MHz). Thus the processing time should be kept at the order of 500 ns (to minimize pile-up), with no dead time between different events introduced by the electronics. Double peak resolution should be around 500ns.

5.1.3 Bandwidth

The timing signal is usually obtained after discrimination of the input signal, thus it is the jitter of the discriminated signal what limits the timing resolution of the electronics. The random jitter (σ_t) is proportional to the noise (σ_n) and inversely proportional to the signal slope ($\frac{\delta S}{\delta t}$) around the threshold level. Then the signal BW in first order approximation is calculated in equation 33.

$$\sigma_t = \frac{\sigma_n}{\frac{\delta S}{\delta t}|_{S_T}} \approx \frac{t_r}{\frac{S}{N}} \qquad BW \approx \frac{0.35}{t_r} \tag{33}$$

For a TOF PET application a temporal resolution of around 100ps should be needed. Expecting a S/N ratio around 10 a rise time of less than 1ns is needed, leading to an expected minimum analog bandwidth of around 350MHz.

But in the case of a TOF PET system timing accuracy will not only be constrained by the electronics, and in fact the S/N ratio will depend on the threshold level, being greater than 10 in most of the cases. In fact it can be demonstrated[44] that the coincidence resolving time of two sensors with electronics is mainly limited by photon statistics while crosstalk, electronic noise and signal bandwidth have relatively little influence. Thus a bandwidth around **250MHz** should be enough.

5.1.4 Linearity

PET systems use the energy measurement to cut off non coincident events. The system is only interested in events around 511keV that should produce the LoR with some time information (if ToF is used). The rest of events are usually discarded. Thus system linearity does not need to be very accurate. Good scintillating materials used in PET provide an energy resolution around 7%[24], the goal for the electronics in order not to degrade much the performance of the full system should be around ±5 %.

5.1.5 Specifications summary

A summary of previous section conclusions is detailed in table 5.1.

Parameter	Value	Unit
Channels	16, 32 or 64	-
Power	<15	mW/ch
Double peak resolution	<500	ns
Bandwidth timing	>250	MHz
Package	QFN or BGA	-
Linearity	±5	%

Table 5.1: PET readout ASIC specifications summary

5.2 Implementation

Taking into account previous requirements it was decided to first design a block test prototype including the most critical part in the design: the pre-amplifier. Some basic current discriminator was also included. Afterwards a multi-channel prototype with more functionality should be designed.

The main design objectives of the final prototype are:

- Pre-amplifier Bandwidth $\approx$ 250MHz
- Direct connection to SiPM
- Controllable DC voltage at SiPM
- Low input impedance
- Fast OR of all channels for timing measurements
- Digital Time Over Threshold output for energy measurement
- Minimize power consumption
- Good linearity

5.2.1 Architecture

In figure 5.2 a block diagram of the analog channel can be seen. After analysis of previous ASICs it seems that the best solution for the readout is current mode input. The current mode input stage is described in previous section. It provides a low impedance input with a controlled DC voltage and multiple scaled copies of the input current. In this case three copies have been implemented; timing, energy and pile-up.

For the timing measurement the common approach is to use one of the signal paths and compare directly with some threshold to detect the leading edge. This process leads to reasonably good timing measurement results. Other more complex processing can lead to better resolution in some applications but are often much more complex[40]. For this reason a simple fast current mode comparator has been designed for this application. Afterwards all timing signals for the different channels are combined in a logic OR to generate only one timing signal for the full ASIC.

For the energy measurement a digital output is desired due to the flexibility for the readout and low resource usage. An integrator with a constant current discharge will provide signal to an hysteresis comparator. Using this circuit a linear output depending on input charge will be delivered. This linear behaviour is desired to avoid extra offline corrections on data.

For the pile-up measurement (detection when two incoming signals occur during our measurement window, thus changing signal shape) an extra

AC coupled path with less gain has been used. The AC coupled signal is compared to a fixed threshold using the same fast current comparator used in the timing stage. The output of the comparator is then feed into two cascaded registers to provide a logical output. Pile-up of all channels is stored in a register with its own interface to be controlled and readout.

This architecture keeps interface simplicity both at the input with no extra components needed for SiPM connections and at the output with a direct digital interface to the readout system (typically an FPGA).

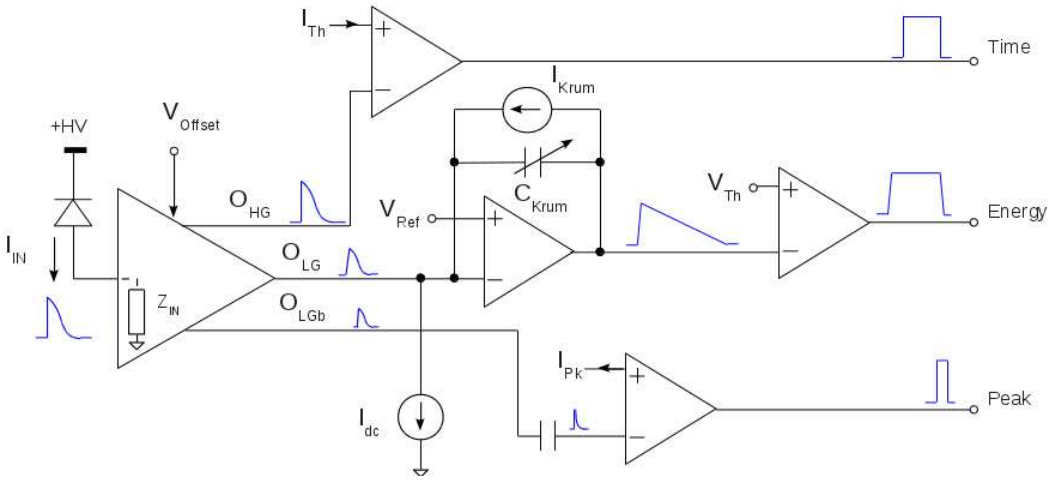


Figure 5.2: FLEXTOT channel blocks diagram

The added pile-up detection circuitry adds a feature not present in previous designs and helps offline processing.

Slow control for the setup of thresholds, control voltages and polarization currents of the circuit are also included in the prototype.

5.2.1.1 Floorplan

Since one of the main purposes of this design is to include an important number of channels that should be extended in future prototypes it is important to keep a regular and easy to reproduce shape. For this reason the analog channel has been designed in a hard macro including input pad.

Common biasing block is placed in the center of the prototype to reduce the length of the connections to all channels. Common biasing parameters are copied to all channels using long vertical lines, thus voltage signals are used. In the central part also the common slow control and registers are placed.

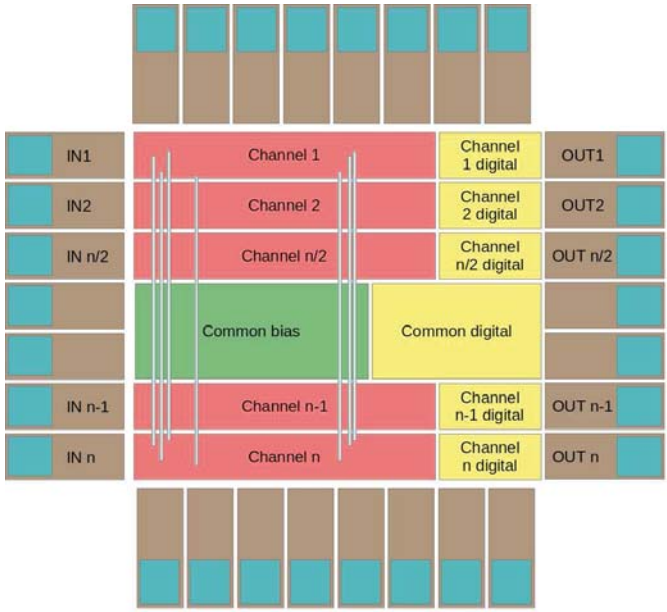


Figure 5.3: FLEXTOT floorplan

Since prototype was 16 channels in a 64 package, the sides of the design is already fully populated by the input and output signals of the channel. Top and bottom parts are used for power supplies, debugging signals and slow control needed pins.

All power lines go from top to bottom of the prototype with double pads in each side to reduce the parasitic inductance and length of connections.

5.2.2 Power

Four different power domains have been defined for the internal circuits polarization;

- $\mathbf{V}_{DDA}$ Analog power supply, feeds all signal processing blocks.
- $\mathbf{V}_{DDD}$ Digital power supply, feeds all digital parts and discriminator circuits.
- $\mathbf{V}_{DDO}$ Output power supply, feeds single ended output pads and OR gates generating the timing signal
- $\mathbf{V}_{DDCML}$ Power CML output pad only.

This division together with a different substrate connection for the different region should minimize the switching noise induced to the analog design. Double connections to reduce inductance and track length and in circuit decoupling capacitors have been taken into account in the layout process.

5.2.3 Energy measurement Blocs

The energy measurement signal path is formed by a linear Time Over Threshold measurement at the output of a pole-zero cancellation (passive) of signal shape and connected to an hysteresis comparator. With the pole zero cancellation any effect of undershoot is mitigated for some time constants of incoming signals. The rest of the processing chain (TOT and comparator) provide a linear digital output representing the energy (charge) of input signal.

5.2.3.1 Linear Time Over Threshold

Time Over Threshold (TOT) is a processing methodology in which an analog signal is compared to a fixed threshold to obtain a digital pulse representing the height of the analog one. Measuring the width of the digital output the amplitude of the input signal can be obtained. TOT offers simple circuitry for multichannel systems with low power consumption. However typical TOT implementations have poor linearity.

The non linear behaviour of the TOT will depend on signal processing. For example if a simple Gaussian shaping is used on the input signal a triangular approach can be used.Taking this triangular input signal (as suggested [48]) the resulting non-linearity is clearly observed depending on

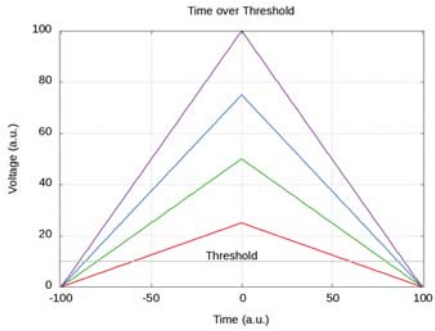


Figure 5.4: TOT input

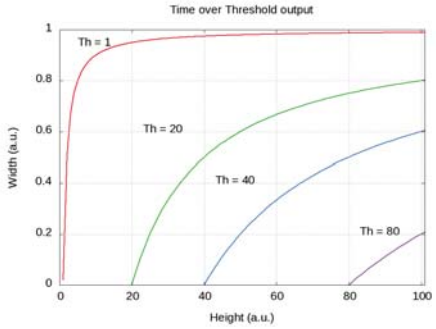


Figure 5.5: TOT output for triangular input

threshold value (see figures 5.4 and 5.5). Dynamic threshold variation depending on incoming signal has been studied to achieve a linear output [48]. But if an ideal signal with an extremely fast rising edge and constant linear falling edge the resulting TOT measurement should be close to an ideal one (see figure 5.6 and 5.7).

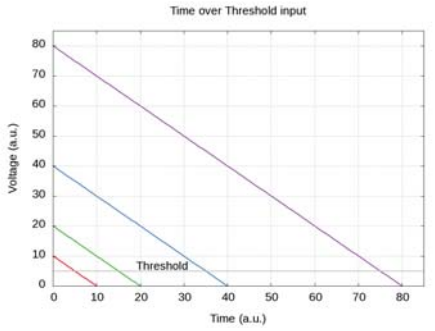


Figure 5.6: TOT input

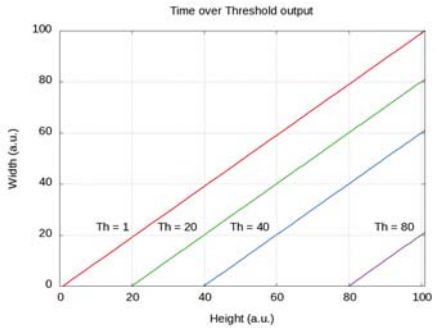


Figure 5.7: TOT output

A similar signal to the ideal can be obtained taking advantage of the fast rising edge of the input signal generated by the SiPM. Using an integrator with a constant discharge current before a comparator, a linear TOT measurement is obtained. Basic schematics can be seen in figure 5.8. Similar approach has been used in the past in other detector systems[49],[50].

Ideally resulting TOT measurement can be easily calculated using formula 34, taking as input the injected charge signal (Q). Since threshold voltage (V_{Th}), capacitance (C_{Krum}) and discharge current (I_{Krum}) will

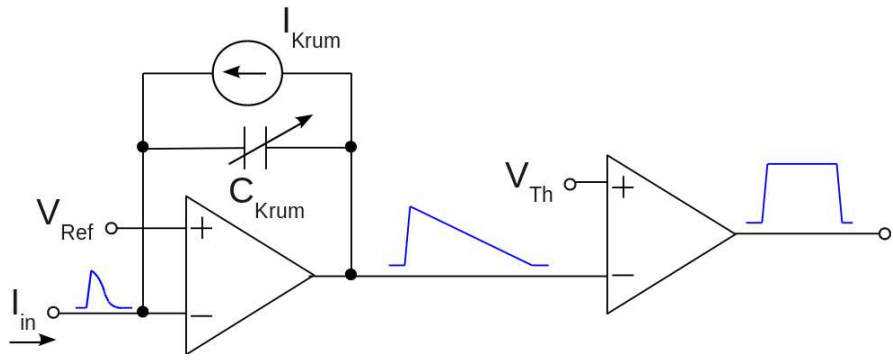


Figure 5.8: Linear TOT schematic

be constant the measured time will have a linear behaviour with Q. The non ideal behaviour will be introduced by the slope of the rising edge of our signal and the long decay of some SiPMs combined with the scintillating material. A pole-zero passive cancellation is also included to avoid undershoot in input signal to the integrator. Those non ideal effects will be noticeable for very small signals, but not for usual events from PET systems.

$$T_{TOT} = \frac{Q}{I_{Krum}} - \frac{V_{Th}C_{Krum}}{I_{Krum}} \tag{34}$$

Some linearity simulations of the linear time over threshold measurement is summarized in figure 5.9 using a real measured signal as input and including pre-amplifier.

One of the most important advantages of this structure is the flexibility. Changing the feedback capacitor and the discharge current offers the possibility to trade-off resolution versus output time over threshold width.

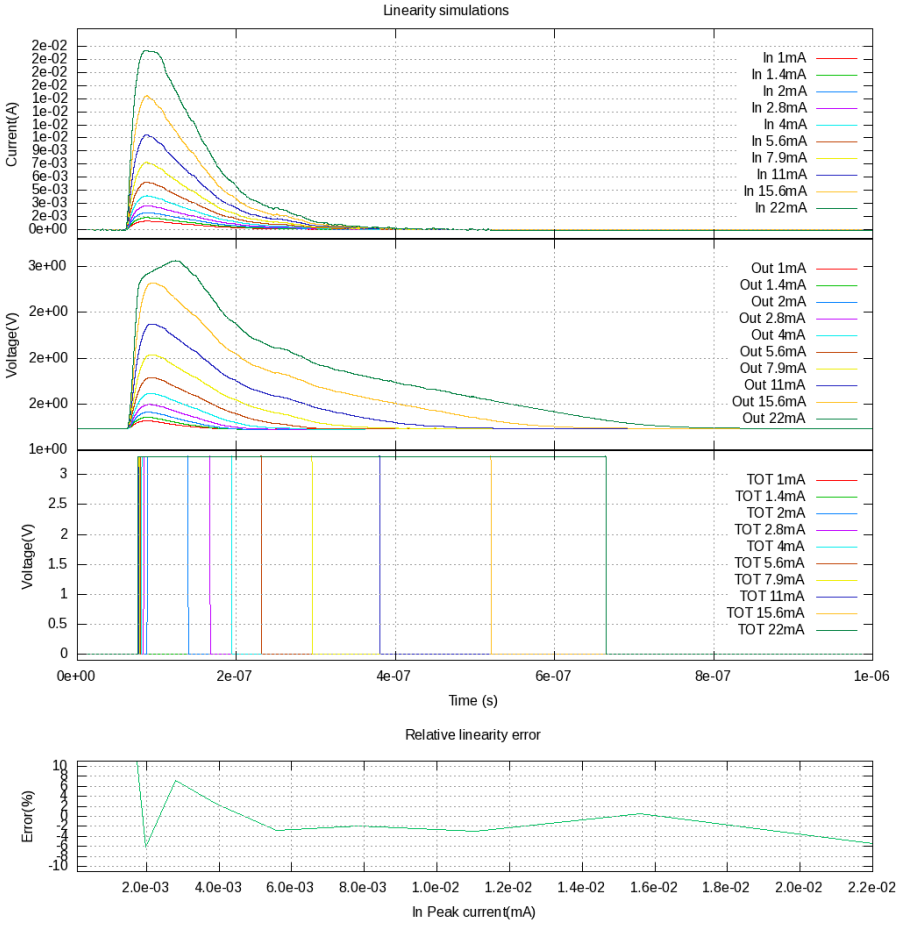


Figure 5.9: Linearity simulation

5.2.3.2 Hysteresis comparator

The hysteresis comparator is needed to avoid multiple transitions produced by noise in the signal tail. The added hysteresis will provide a clean signal at the output of the comparator. For this reason a design based on a standard CMOS comparator [52] has been used. A source coupled differential pair with positive feedback and a differential to single ended converter has been designed. For the differential pair bipolar transistors have been used. To improve performance cascoded current mirrors have been used. The schematic can be observed in figure 5.10.

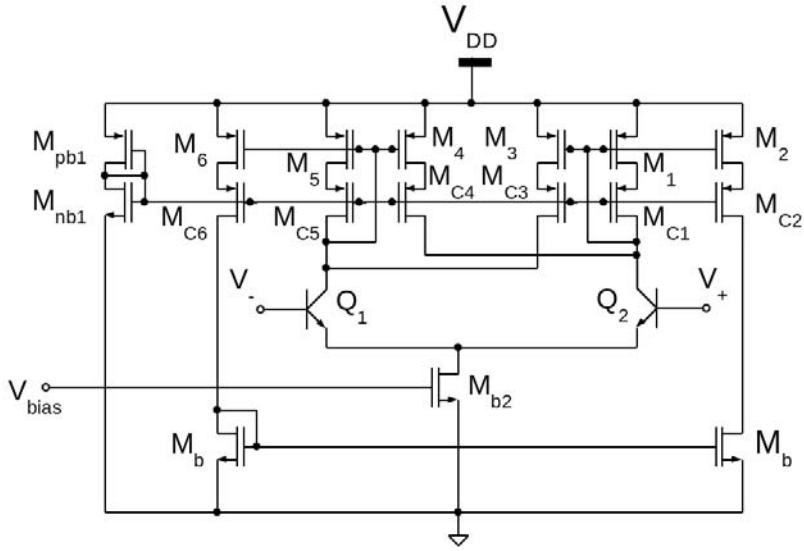


Figure 5.10: Hysteresis comparator schematic

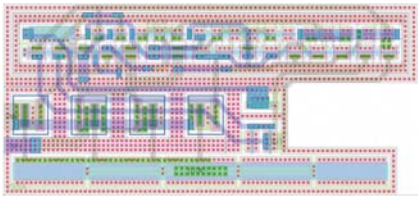


Figure 5.11: Hysteresis comparator layout

By design the cascodes in the differential pair will be equal in sizes and also Q_1 and Q_2. If we define as α the relation in currents from cascode master and slave (related to their dimensions), the resulting hysteresis from the circuit can be calculated using formula 35, basically controlled by the cascode current gain between M_3 and M_1 or the same size M_4 and M_5. By design the hysteresis is set to 30mV. Layout only

requires 73μm x 33μm and can be seen in figure 5.11.

$$V_{Histeresys} = 2.\sqrt{\frac{I_{biasM_{b2}}}{gm_{Q_1,Q_2}}}.\frac{\sqrt{\alpha}-1}{\sqrt{1+\alpha}} \tag{35}$$

MonteCarlo simulations with a fixed input set to 1.65V and varying the other comparator input is shown in figure 5.12 including process and mismatch variations. Hysteresis width presents small variations in this circuit as desired.

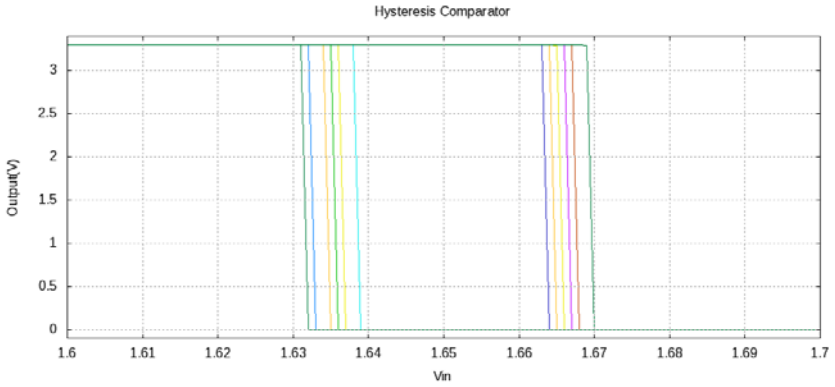


Figure 5.12: Hysteresis comparator MonteCarlo simulation

5.2.4 Time measurement Blocs

Timing signal path only includes a fast current discriminator at the output of the pre-amplifier to generate the timing information.

5.2.4.1 Current discriminator

Current discriminator should have an extremely fast response for low signal currents. This is important because the first electrons generated by the SiPM would give the better timing for the incoming signal. Implemented design is based in a combination of a extremely fast low current discriminator[51] with a constant current mirror. The current mirror is connected to a DAC used for setting the threshold (deriving some fixed amount of current at the input). The basic schematic can be observed in figure 5.13.

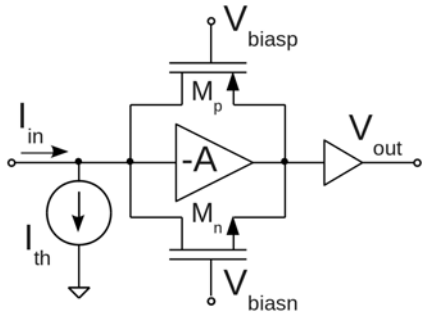


Figure 5.13: Current fast discriminator

Initial conditions keep output voltage equal to input voltage and in a range keeping M_n and M_p OFF. On the event of incoming current it will be integrated by the parasitic input capacitance, generating an increasing voltage at the input node. The voltage at the output node will decrease faster than the input since the amplifier gain (-A). V_{gs} for M_n transistor will increase until its operation point is set to the ON state. Once ON a negative feedback loop is created driving input node to virtual ground. If current signal is inverted (flowing from the discriminator to the previous stage), M_p will perform the complementary operation. This structure is simple and delivers very fast response time specially in low input currents.

The output buffer isolates output node from next stage. It will generate a voltage signal suitable for further processing or readout.

The resulting layout has a total size of 21μm x 83μm (seen in figure 5.14).

MonteCarlo simulations points to very small variation (of the order of nano amperes) on the switching point, keeping the transition around 178μA of input current with implemented dimensions.

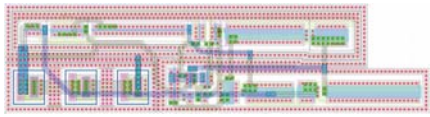


Figure 5.14: Fast current discriminator layout

5.2.5 Pile-up detection blocs

To avoid costly offline processing a pile-up flag is available on every channel at every acquisition. This is achieved using an extra signal path to detect a double peak at the input during the acquisition window. The differentiated signal (using in series capacitor) at the output of the pre-amplifier will trigger a comparator and if two comparator outputs have been triggered before resetting pile-up logic, a logic assertion will be marked in the pile-up register. The basic schematic of the pile-up detection logic is depicted in figure 5.15.

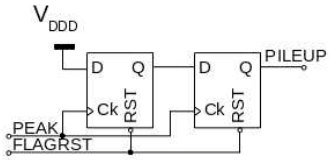


Figure 5.15: Pile-up detection logic

Figure 5.16: Pile-up reset logic

To reduce latency on the readout a dedicated readout and control for the pile-up register has been designed. To reduce input / output signals for the control, some combinational logic has also been added to generate different reset signals in the blocks. In figure 5.16 the reset logic can be observed and in figure 5.17 a full readout sequence is depicted.

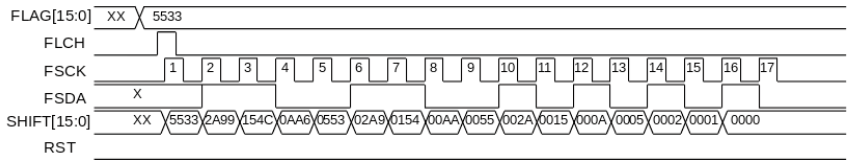


Figure 5.17: Pile up register readout

5.2.6 Common Blocs and Biasing

Several blocs have been designed to provide the needed voltages and currents for setting the operation point of the circuitry and also to provide all the configurable analog values.

5.2.6.1 Bandgap references

Two Bandgap references previously used in other designs has been reused to provide a voltage and a current reference for all the biasing and DACs circuitry. The voltage reference generates 1.21V while the current reference generates a 100μA current. See SiPMVFEr1 appendix for further details.

5.2.6.2 DACs

Several DACs are included in the design in order to tune the circuit behaviour. Some of them can be read directly from the input/output pins. All DACs are based on the current output DAC shown in figure 5.18. Upper transistor acts as a slave of a current mirror, while the transistor connected in series acts as a switch. Binary inputs enable those switches to permit a fixed current to cross to the output. Multiplied circuits in parallel generate the weighted output depending on bit pattern.

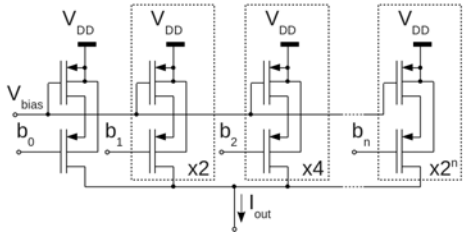
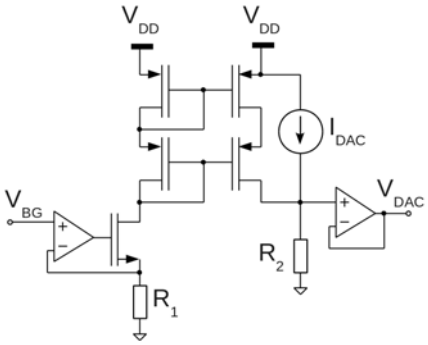


Figure 5.18: Current output DAC

For the generation of voltage DACs between a determined value the signal from the current DAC and the Bandgap reference voltage are combined achieving a fixed offset and resolution with small changes with temperature. In figure 5.19 a general schematic for the voltage output DACs can be seen using those two elements. The Bandgap voltage is used to add a fixed current at the output of the current DAC. The process and temperature variation of the resistors value is compensated between the reference of the fixed current and the load of the current DAC. The sum of currents is converted to voltage and buffered. The resulting voltage output will have

an offset defined by 36, an LSB defined by 37 and a maximum output given by 38.



$$V_{offset} = \frac{V_{BG}}{R_1}.R_2 \tag{36}$$

$$V_{LSB} = I_{LSB_{DAC}}.R_2 \tag{37}$$

$$V_{MAX} = \frac{V_{BG}}{R_1}.R_2 + I_{MAX_{DAC}}.R_2 \tag{38}$$

Figure 5.19: Voltage output DAC

To reduce area and power consumption all DACs share common references from the common bias block. Those references are used to copy a constant current master (for the current DACs, V_{bias} in schematic) or a fixed current (amplifier connected to V_{BG} and master mirror with resistor load). Due to area constraints only a pair of current DACs where designed (3 bits and 6 bits) and they are combined to generate greater resolution DACs connecting it's output in parallel. Such combination can lead to non uniformities due to unmatched current copies.

A MonteCarlo simulation of a 6bit voltage DAC including mismatch and process variations can be observed in figure 5.20. Step size matches desired value (around 10mV) and full scale is as expected.

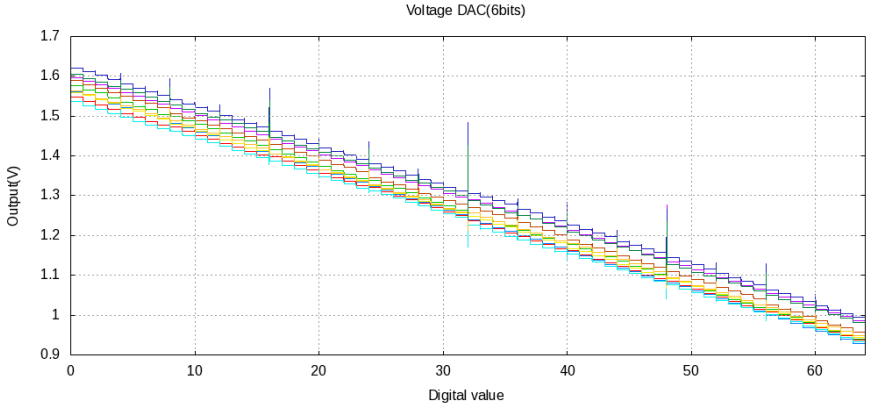


Figure 5.20: Voltage DAC(6b) MonteCarlo

5.2.6.3 Single Ended CMOS Pad

Standard output pads have been used when possible (input wire connection, power pads, digital on top and bottom zone of pad ring). But for some reasons two pads have been designed and used as a hard macro. Looking at section 5.2.1.1 the width of the full channel including input and output pads is fixed. The size of a standard analog input pad (wire connection) is around 100μm height, but standard CMOS output buffers double this width.

For this reason it was decided to implement a custom output pad keeping the same height of the analog one but incrementing it's length. It was also designed to be able to tolerate short circuit at the output and with a slew rate control.

The basis to obtain this features is to control the output impedance. In this case an output resistance with a pass gate to connect two in series controls the slew rate by a single bit (the inverter of the pass gate is also included). Schematic can be seen in next figure 5.22. The controlled output resistance limits output current to around 5mA (with high resistor) and 10mA (with small resistor).

On the layout the width is kept to the same as a standard analog pad (around 100μm) but the length is extended to fit the rest of introduced elements with a total of around 362μm. Full layout can be seen in figure 5.21.

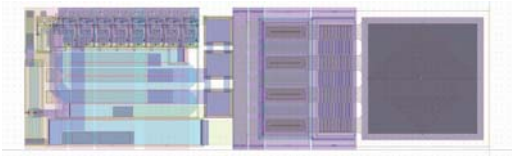


Figure 5.21: Output pad buffer layout

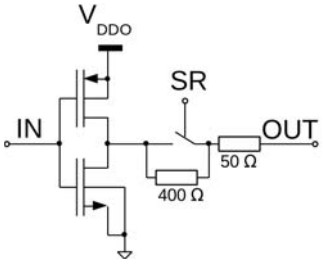


Figure 5.22: Output pad buffer with SR control schematic

5.2.6.4 Differential Current Mode Logic Pad

For the fast timing output it is desirable to generate a signal with minimum jitter and maximum speed and signal integrity. For this reason a differential standard seems the most robust option. After some analysis an adjustable output with the base of the CML standard was chosen.

The output current can be adjusted by a current DAC and the termination style can also be changed, so it can be compatible with the LVDS standard. The schematic is based on a differential pair with two resistors pull-up and constant current load as seen in figure 5.24. Previous to the differential pair, a buffer and inverter, are also included to generate complementary signals with the same delay from a single ended input. The total layout size is around 420μm x 290μm including power and ground pads as seen in figure 5.23.

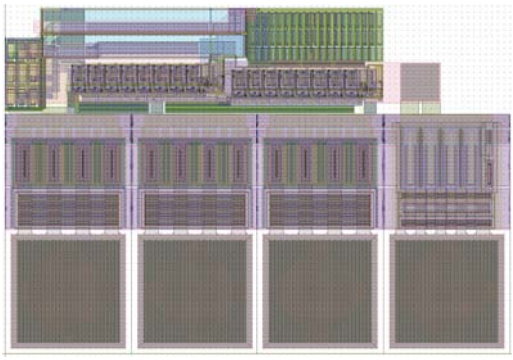


Figure 5.23: CML output layout

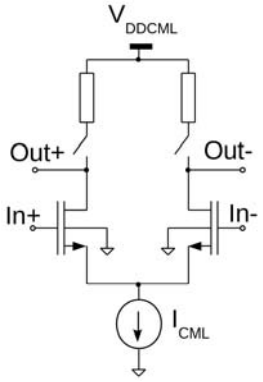


Figure 5.24: CML output schematic

If the circuit is terminated with a resistor R_{TERM} between Out+ and Out-, the voltage swing and common mode can be calculated easily using 39.

$$\begin{aligned} V_{SWING} &= I_{CML} * R_{TERM} \\ V_{CM} &= V_{DDCML} - \frac{V_{SWING}}{2} \end{aligned} \tag{39}$$

5.2.6.5 Temperature sensor

A small temperature sensor based on the voltage drop across a diode connected FET has been introduced in the circuit. To achieve more voltage variation with temperature three diodes have been placed in series (see figure 5.26. The output drives directly an analog (wire) pad. Total size of the sensor (including current mirror) is 34μm x 47μm (see figure 5.25).

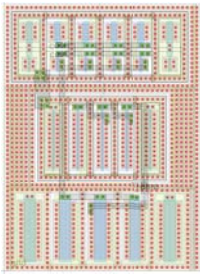


Figure 5.25: Temperature sensor layout

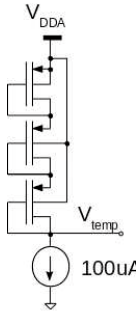


Figure 5.26: Temperature sensor schematic

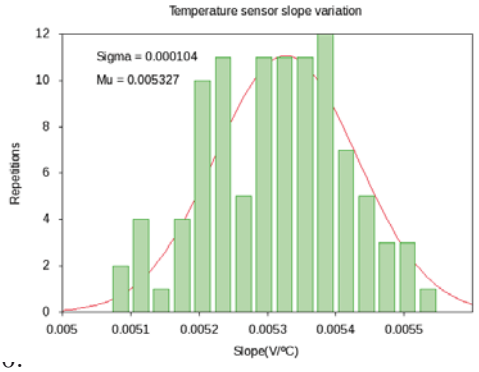


Figure 5.27: Temperature sensor slope montecarlo simulation

The voltage drop of a diode with a constant current will vary depending on the temperature. Since all diodes are at the same temperature, the change in voltage will be three times bigger with three diodes. The resulting output voltage is expected to have a slope of 5mV/°C (see montecarlo simulation in figure 5.27). Process variations will change the absolute value of the temperature output at a given temperature, but not the slope thus allowing an easy single point calibration.

5.2.6.6 Slow Control

Slow control interface is based on a standard JTAG[47] interface with user defined data registers. Synopsys® tools permit automatic insertion of the Test Access Port (TAP) controller and connect the registers at compilation time, easing the introduction of this protocol in the design. Only using 5 lines, TDI, TDO, TMS, TCK and TRST internal registers can be read and written. Using standard TAP controller FSM (see figure 5.28), any of the control registers can be read or written by selecting the instruction register that points to the corresponding data register and then writing the data. TAP controller FSM changes it's state depending on TMS value on every rising edge of TCK.

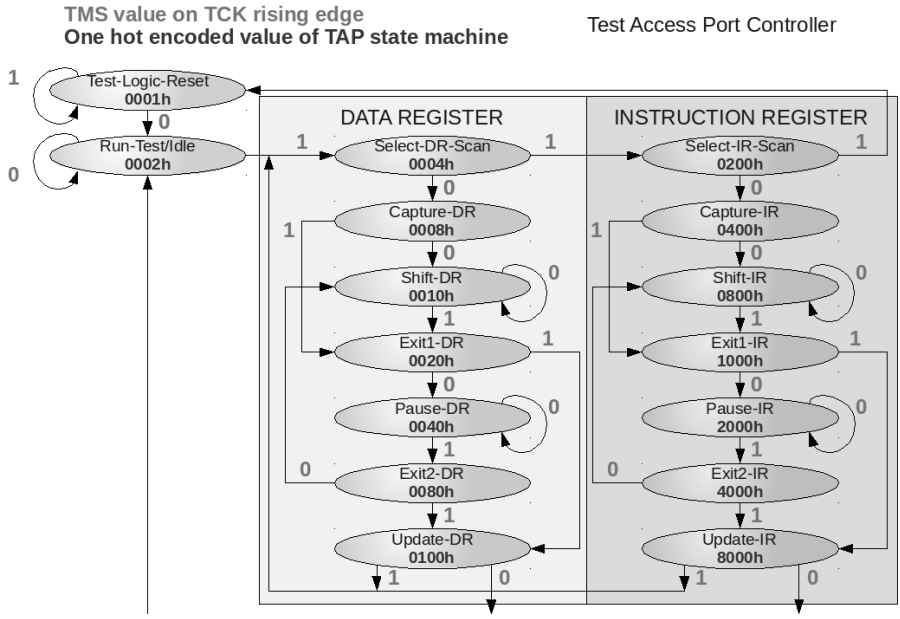


Figure 5.28: TAP controller FSM

Following FSM a typical write to a register with 33 bits length should be as depicted in figure 5.29.

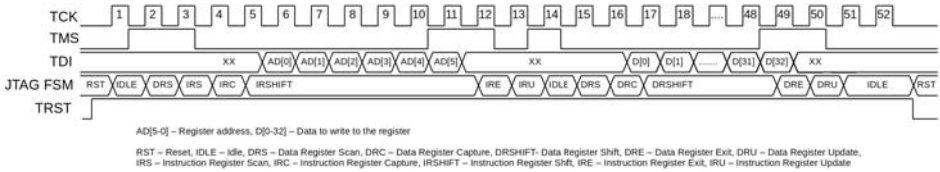


Figure 5.29: JTAG 33 bits register write

5.2.6.7 Debug signals

Several interesting signals have been ported to debug pads (see figure 5.30. Those signals are the timing output of each channel and the output of the integrator. In the timing signal all channels share a common line with a pass gate on every channel to connect or disconnect the output. The case of the integrator output is slightly different; there are two pads multiplexing top 8 channels and bottom 8 channels to avoid crossing the digital common control in the middle and reduce connection length (parasitic resistance and capacitance). At the end of both integrator debug outputs an amplifier to drive an external capacitive load is attached. All this multiplexors are directly controlled using the slow control interface.

A third debug signal is the OR of all timing channels, it is ported to a single ended output pad, equal to the energy ones.

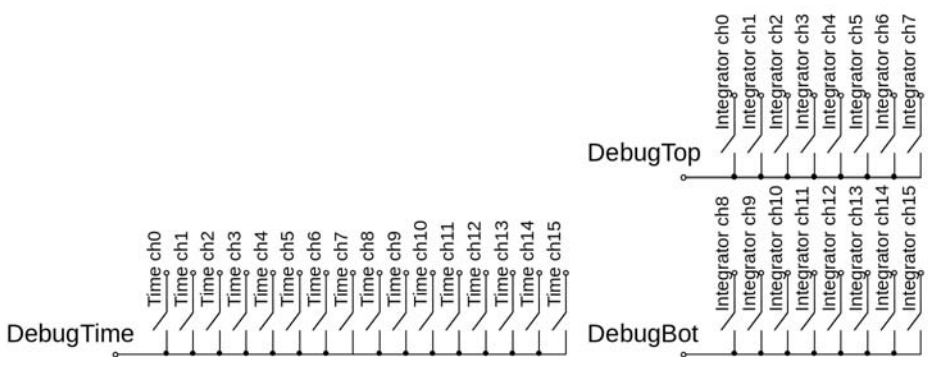


Figure 5.30: Debug outputs connection

5.2.7 Layout

Full layout of final prototype can be seen in figure 5.31. Channel processing chain is placed from left (channel input) to right (channel output), with separated power supply for digital part (right end of channel) and output pads. In the middle of the prototype the common bias and DACs with the common digital is placed, thus the length of connections to all channels is minimized. Left and right pads are reserved for input / output of the channels (with ground connection on the middle left and debug digital outputs on the middle right). Top and bottom are mostly for digital interface and power supplies.

Figure 5.31: Final FLEXTOT layout

To avoid coupling through power supply separated supplies for analog,

digital and output pads have been selected. Different power domains can be observed in figure 5.32. Power supplies are connected from top to bottom, doubling the pads (whenever possible) in both sides of the design. In this way a good connection with as low as possible parasitic resistance is achieved. Few decoupling capacitors are also placed in free areas and in power rails.

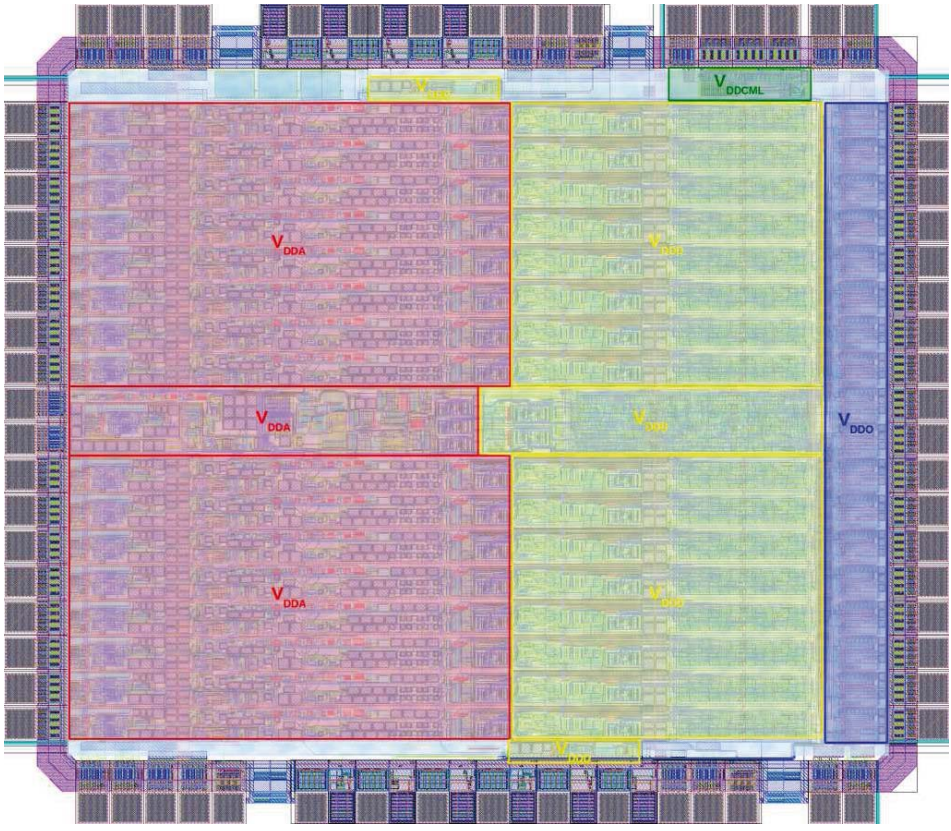


Figure 5.32: FLEXTOT power domains

5.3 Results

FLEXTOT prototype was received in October 2012, with 30 encapsulated dies on a QFN64 and 10 non encapsulated dies. During manufacturing a test system was designed thinking on testing the maximum parameters as possible. First electrical characterization was followed by more realistic tests with SiPM and radioactive sources.

5.3.1 Test system

Test system (see figure 5.33.) is based on a stack of three PCB with all the needed electronics for a full system. From the sensor to the data communication with a host computer. The only thing not included is the high voltage power supply for the sensors. The following electronics / features are present in each of the different PCBs (from top to bottom):

- Sensor PCB: different manufacturers sensors can be placed over this PCB. The sensor connects directly to next PCB, only high voltage connector is available. A variation PCB with a charge injection circuit can be placed in the same position to calibrate channels with a known signal shape and amplitude.
- Analog PCB: the analog PCB is basically a QFN64 test socket with low drop-out (LDO) linear regulators and some decoupling and resistors. It also uses a pair of amplifiers to check debug signals directly from oscilloscope and a high speed switch (SPDT) to be able to disconnect input to channels.
- Digital PCB: EP3C low cost FPGA with FT2232 transceiver to handle communications with host computer. Using the FPGA the slow control can be configured, pile-up interface managed, SPDT switches connection enabled and also a low resolution (5ns) pulse width measurement can be performed for all channels. It houses a basic DAQ for testing the capabilities of the ASIC.

Figure 5.33: Test system setup

5.3.2 Power consumption

Using test points in the analog PCB the power consumption from different power supplies can be measured. A summary of the tested ASICs is available in table 5.2, VDDO and VDDCML are not measured, since in normal conditions and no commutations at the outputs VDDO will draw a negligible current and VDDCML current draw will depend on configuration. VDDA and VDDD are powered at nominal 3.3V power supply. The average power consumption is 10.7mW per channel or 7.7mW per analog channel (excluding digital power).

ASIC$_{REF}$	**VDDA (mA)**	**VDDD (mA)**	**TOTAL (mA)**
8	38	14.8	52.8
9	37.5	14.2	51.7
10	37.4	14.4	51.8
11	38.6	14.9	53.5
12	37.4	14.1	51.5
13	37	14.2	51.2
14	37.6	14.3	51.9
15	37.8	14.5	52.3
16	37.6	14.4	52
17	37.2	14.1	51.3
18	37.8	14.5	52.3
19	37.9	14.6	52.5
20	36.5	13.9	50.4
21	37	14.3	51.3
22	37.1	14.4	51.5
23	37.3	14.5	51.8
24	37	14.2	51.2
25	37.6	14.4	52
26	36.9	14.1	51
27	37.4	14.2	51.6
28	37.4	14.4	51.8
29	37.3	14.4	51.7
30	37.6	14.3	51.9
AVERAGE	37.4	14.8	51.8

Table 5.2: FLEXTOT power consumption

5.3.3 Input stage Bloc

On input stage direct measurable behaviour can be done in the input impedance and the voltage control circuitry (see DACs section).

5.3.3.1 Input Impedance

An important element to avoid changing the shape of the input signal and to maximize the input current to the input stage is the input impedance. In the design process this value has been kept to a low reasonable value. The measurement on figure 5.34 verify the results are as expected; with the typical inductive behaviour at high frequencies and a

value close to the typical one (around 34Ω until 200MHz).

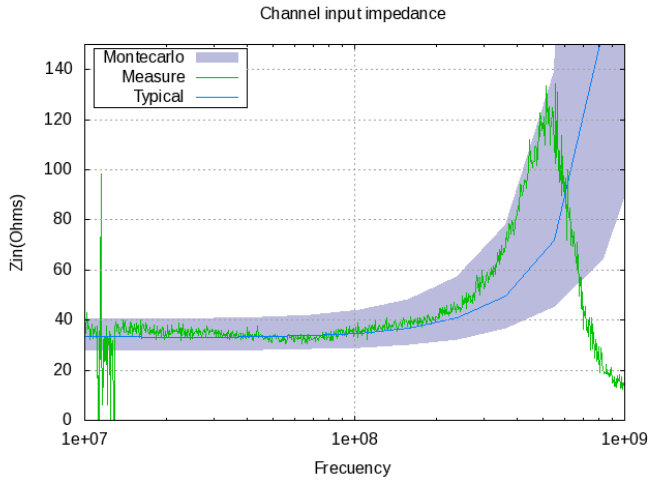


Figure 5.34: Input impedance

5.3.4 Energy measurement Blocs

Energy measurement chain can be tested indirectly using the full chain, but some parts (such as Hysteresis comparator) can be tested without input signal.

5.3.4.1 Hysteresis comparator

To test hysteresis comparator an S-curve has been measured in both directions on the threshold values (from low voltage to high and then opposite direction). The results of a full ASIC (16 channels) is depicted in figure 5.35. Uniformity between channels is quite good but the hysteresis can not be seen in measures because introduced hysteresis (30mV) is too close to two threshold DAC LSBs (22mV).

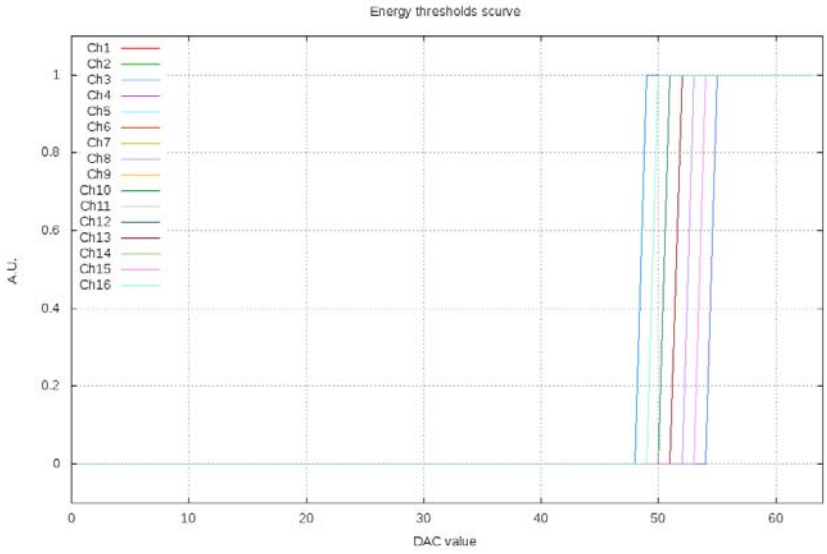


Figure 5.35: 16 channels hysteresis comparator S-curve

5.3.4.2 Electrical signal injection measurements

To simulate the signal generated by a SiPM a small pcb compatible with the sensors pcb has been designed. The basic circuit is an amplifier followed by an AC coupling with a resistor in series to convert voltage into current (see figure 5.36). The signal used is generated using an arbitrary waveform generator (AWG) emulating the signal from a SiPM. Typical signals can be observed in figure 5.37 and 5.38 for two different time constants (corresponding to different SiPM with scintillating material combinations).

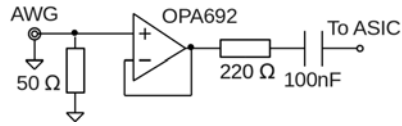


Figure 5.36: Signal injection circuit schematic

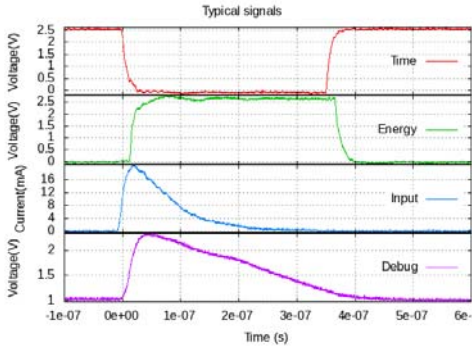


Figure 5.37: $\tau \approx$36ns

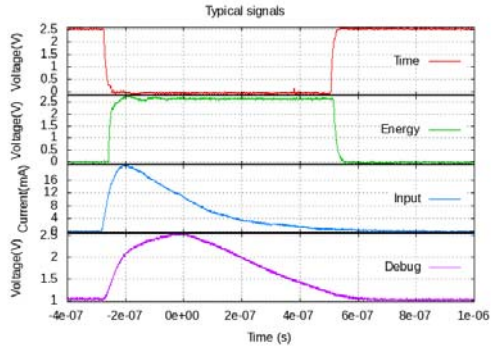


Figure 5.38: $\tau \approx$110ns

To obtain good linearity in the amplitude of the signal injected between the AWG and the injection circuit a programmable attenuation is inserted. The generator is setup with the maximum output and is then attenuated just before the injection. This setup permits much better linearity in the input signal than just modifying generator output voltage. Previous to linearity measurement a calibration on current input peak value is performed. Using this calibration the energy width of every channel is measured.

Since the prototype has some configurable values it will need some calibration to achieve good linearity results in a defined range and shape of input signals. Some examples of the resulting curves from a full prototype (16 channels) are plotted in figures 5.39, 5.41, 5.43 for a τ ≈36ns and in figure 5.40, 5.42, 5.44 for a τ ≈110ns.

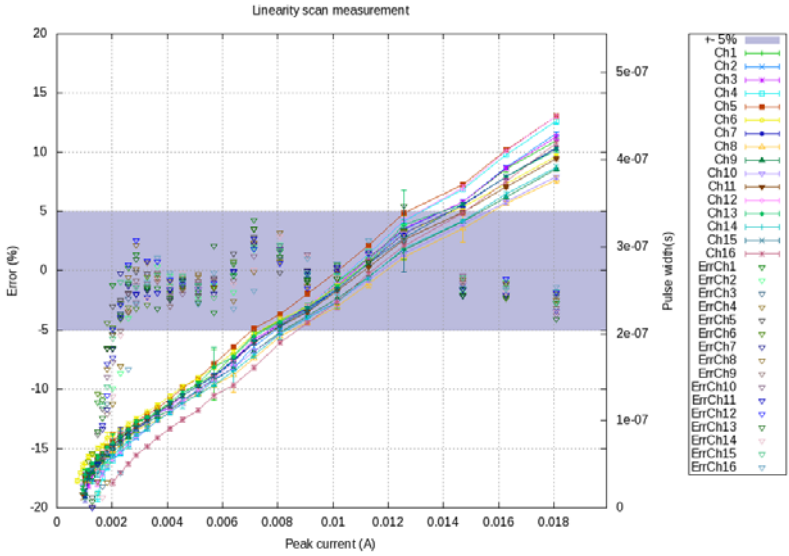


Figure 5.39: Linearity τ ≈36ns 18mA range

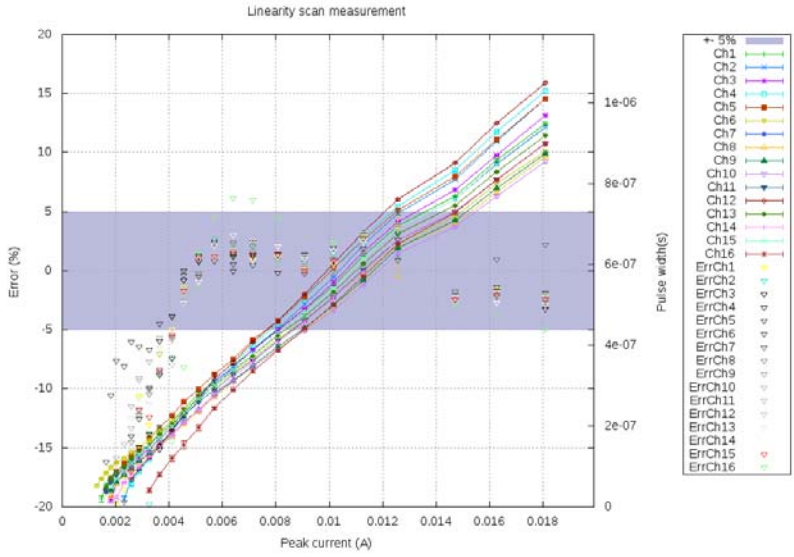


Figure 5.40: Linearity τ ≈110ns 18mA range

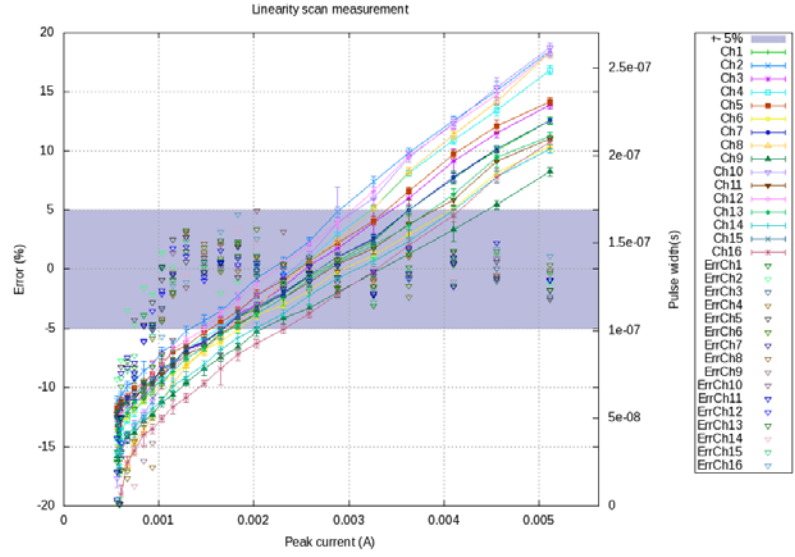


Figure 5.41: Linearity τ ≈36ns 5mA range

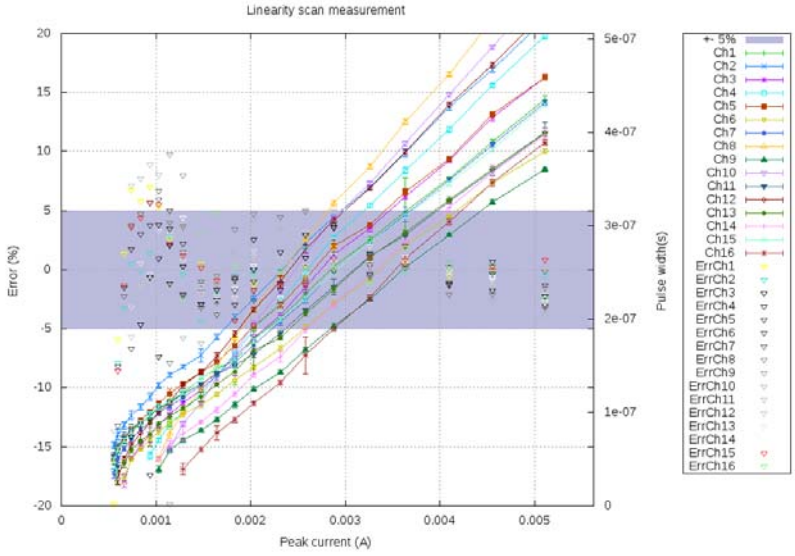


Figure 5.42: Linearity $\tau \approx$110ns 5mA range

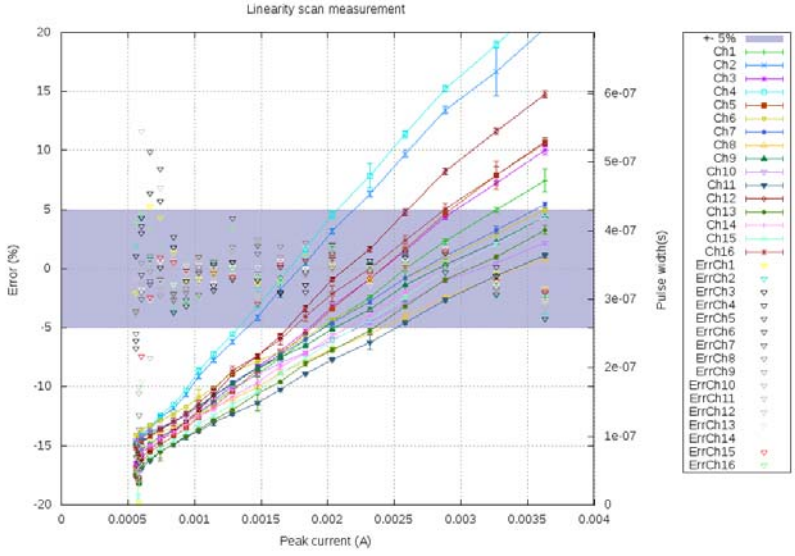


Figure 5.43: Linearity $\tau \approx$36ns 3.5mA range

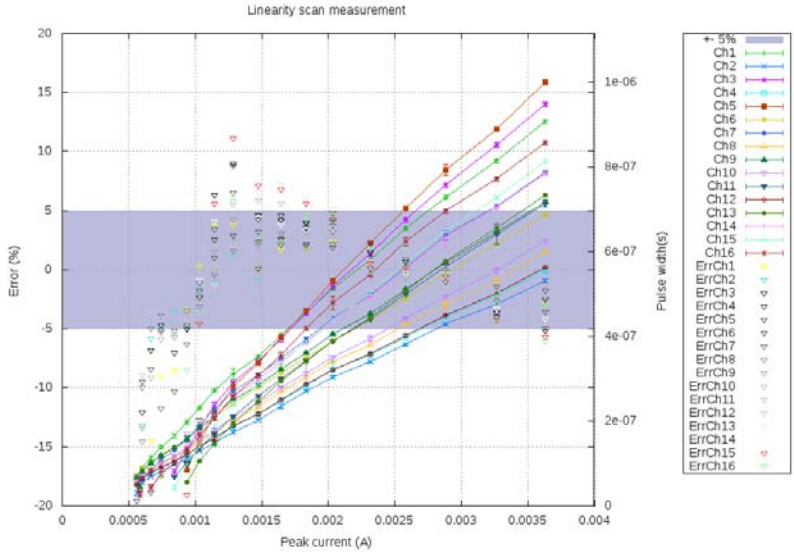


Figure 5.44: Linearity τ ≈110ns 3.5mA range

5.3.5 Time measurement Blocs

Timing signal path can be measured indirectly injecting signal at the input stage and evaluating it's response.

5.3.5.1 Jitter

Jitter is measured as the variation of the delay measurement between a trigger signal and the timing (CML) output. The signal is generated using an arbitrary waveform generator (AWG2021) reproducing a signal similar to a 511keV signal (previously measured at section 5.3.9). Typical signals are plotted in figure 5.45, input signal should match the rising edge of a detector ($\approx$ 4ns) and output CML is deskewed to reduce the oscilloscope window for the measurement. Measurement is depicted as two vertical bars measuring the delay between input rising edge and output.

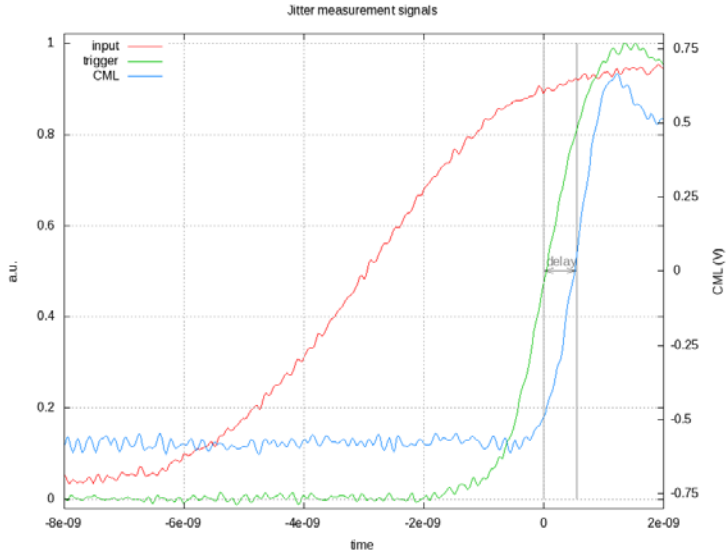


Figure 5.45: Jitter measurement signals

The variation of this delay measurement (sigma) will be the jitter measured (rms). As an example a measurement with no capacitance at the input is plotted in figure 5.46. The total signal measured is the generator jitter added to the system jitter including oscilloscope. Expecting oscilloscope jitter is much less than the rest the assumption that jitter is provided

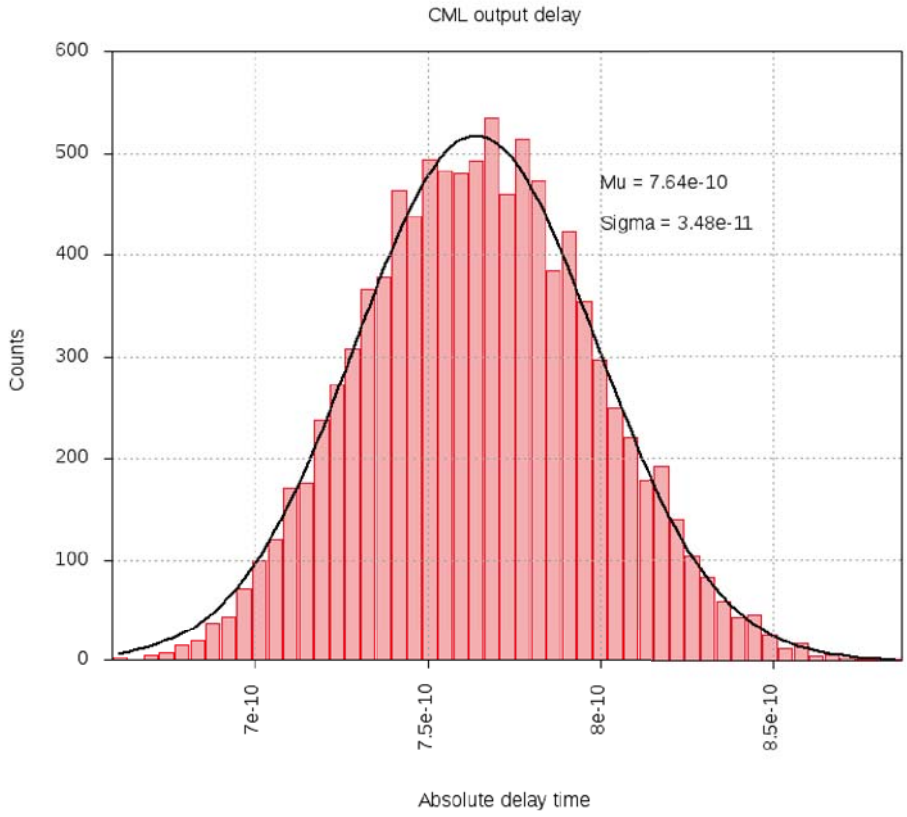


Figure 5.46: Total jitter measurement

by generator and electronics can be done. According to technical documentation jitter between signal and marker output (used for trigger) from AWG2021 is 20ps rms, thus electronics jitter can be easily calculated using 40.

$$\begin{aligned} \sigma_{TOTAL} &= \sqrt{{\sigma_{Generator}}^2 + {\sigma_{Electronics}}^2} \\ \sigma_{Electronics} &= \sqrt{{\sigma_{TOTAL}}^2 - {\sigma_{Generator}}^2} \end{aligned} \tag{40}$$

An important feature of the input stage is the capacitance seen at the input should not increment the noise (so jitter) at the output. To test this feature with the test injection circuitry different capacitance is placed at the input. As expected the jitter is not incremented dramatically. The

results are plotted in figure 5.47 (correcting the jitter introduced by the generator), a minimum capacitance of 5pF is added due to the parasitics on the PCB.

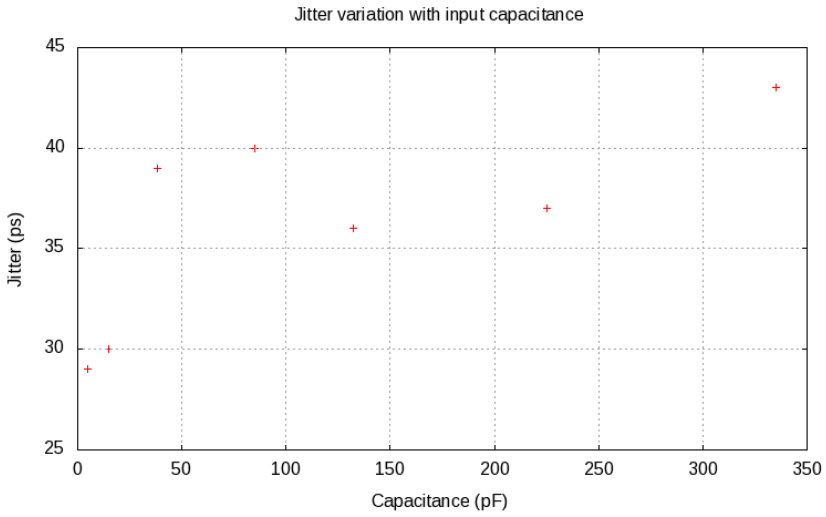


Figure 5.47: Jitter variation with input capacitance

5.3.6 Pile-up measurement Blocs

On pile-up some preliminary measurements have been performed using an arbitrary waveform generated signal with two equal peaks close to each other (separated by 10 ns). The signal chain detects always a pile-up in this case, while with a clean signal it is not detected. Further measurements must be performed to characterize fully this bloc.

5.3.7 Common Blocs and Biasing

5.3.7.1 DACs

Several DACs can be measured directly from input / output pins. Probably the most representative is the 9 bit voltage DAC used to change the voltage at the input node of the ASIC. In figure 5.48 the measurement of 16 channels from the same ASIC can be observed compared with the monte-carlo simulations. To keep the input stage in the operating point the input

node voltage can not be set to any value and a protection circuit could require a little bit more current from the DAC than in normal conditions, fixing the voltage in a certain range. For this reason a clear effect at low or high values can be observed, keeping voltage between 1 and 2 V.

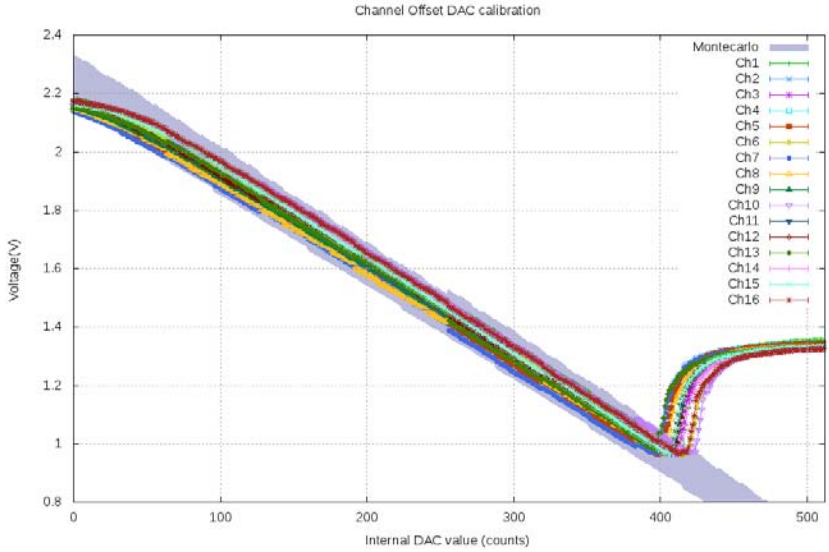


Figure 5.48: Channel DAC measurement

Typical calculations of INL and DNL are represented in figure 5.49. It is important to note the increment in INL should be produced by the effect of the voltage limiting circuit in the input node.

The same measurement performed in the Debug outputs (with no signal should be equal to V_{ref} set internally by a DAC) in figure 5.50. In this case signal is not affected by a voltage limiting circuit, but since it is read at the output of the amplifier it will have it's range limited. In this case INL takes more usual values.

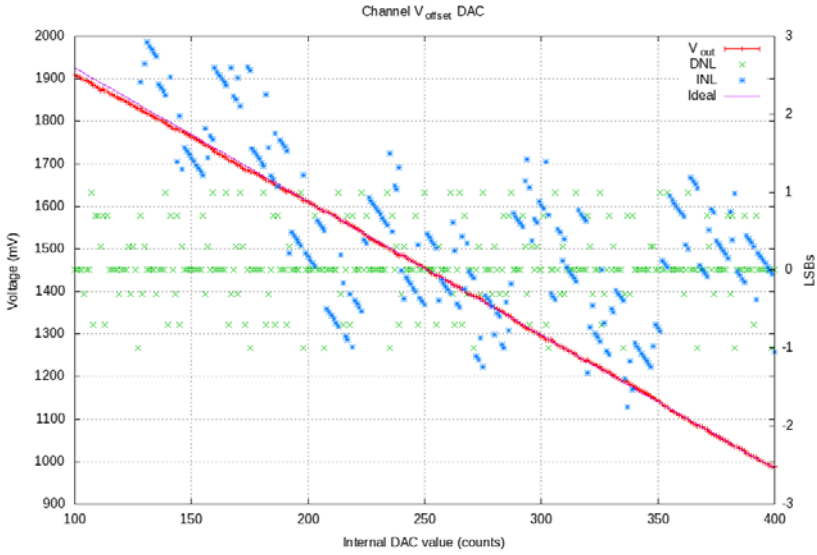


Figure 5.49: Single channel Offset DAC measurement

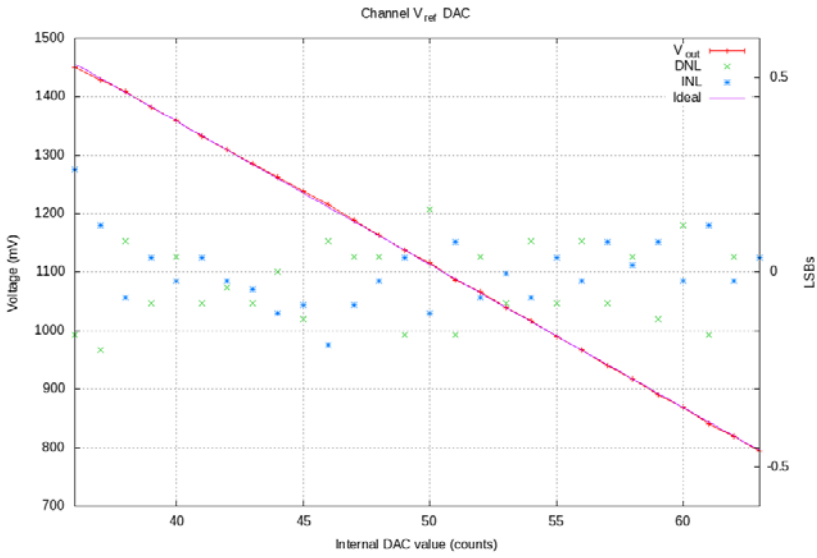


Figure 5.50: Single channel Vref DAC measurement

5.3.7.2 Single Ended CMOS Pad

A simple measurement on the single ended output pads with a passive probe has been performed. As it can be seen in figure 5.51 two clearly different slew rates are available depending on configuration bits.

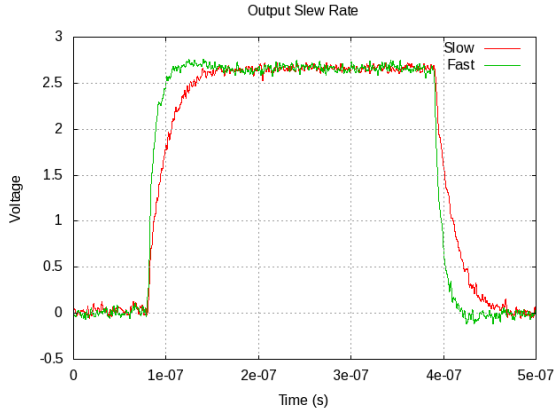


Figure 5.51: Single ended pad slew rate

5.3.7.3 Differential Current Mode Logic Pad

On the CML output pad a pseudoLVDS configuration is tested with 330Ω external pull-up resistors and 100Ω termination. Different current configurations are also measured and summarized in table 5.3 with the optional internal pull-up (switch) configuration.

Figure 5.52: CML output

Digital configuration	Internal switch	Current(mA)
000X0	Off	21[1]
000X1	On	21[1]
001XX	On or Off	18[1]
010XX	On or Off	15[1]
011XX	On or Off	12[1]
100XX	On or Off	9
101XX	On or Off	6
110XX	On or Off	3
111XX	On or Off	0

[1] For agressive power consumption external resistors are needed to avoid voltage drop in internal switches, limiting current.

Table 5.3: CML configuration options

5.3.7.4 Temperature sensor

Temperature sensor has been tested to verify its output behaviour. As an initial test the transient on internal temperature raise has been measured. Since the calibration slope was constant to ($\approx$ 5mV/°C) a simple calibration with just one point (ambient temperature at power up) has been used. The resulting transient after power up permits to obtain the estimated working temperature of the electronics (see figure 5.53.

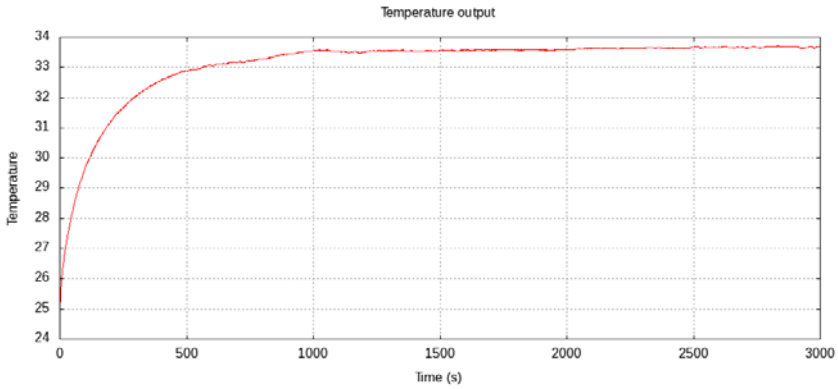


Figure 5.53: Temperature transient at power up

5.3.8 SiPM measurements

After electrical characterization of the prototype a real sensor is attached to the test system. The input signal will have a realistic timing and avoid any undesired effect introduced by the injection circuit. With this configuration several measurements are performed.

5.3.9 Radioactive sources

To characterize with a signal close to reality several radioactive sources have been used. A small LSO crystal (2x2x8 mm^3) has been placed over a detection channel (3x3 mm^2) and then a radioactive source close to the crystal. The system setup (without radioactive source) is depicted in figure 5.54. Previous to the measurement with sources background (LSO emission spectra) is also measured and should be substracted. The sources used have been Na^{22}, Co^{60} and Cs^{137}, see figure 5.55.

Figure 5.54: LSO setup detail

Using the resulting fitted points a plot of the linearity achieved on the signal with the resulting TOT value is plotted. We can observe excellent linearity in the full range. Varying threshold of the energy comparator the resulting line will move over the x-axis, as seen in figure 5.56 for two different thresholds in channel (40 and 50 DAC counts).

With the position of the two more external peaks a calibration constant is determined (see formula 41). The measured resolutions (σ) are then converted to energy using this constant. The resulting resolution computation is summarized in table 5.4 and table 5.5, for the two threshold configuration cases. As expected resolution improves for higher energies.

$$\varepsilon_s = \frac{\mu_{peak_1} - \mu_{peak_2}}{keV_{peak_1} - keV_{peak_2}} \rightarrow Pk_{Err} = \frac{\sigma}{\varepsilon_s} \rightarrow Pk_{res} = \frac{Pk_{Err}}{keV_{peak}} * 100 \quad (41)$$

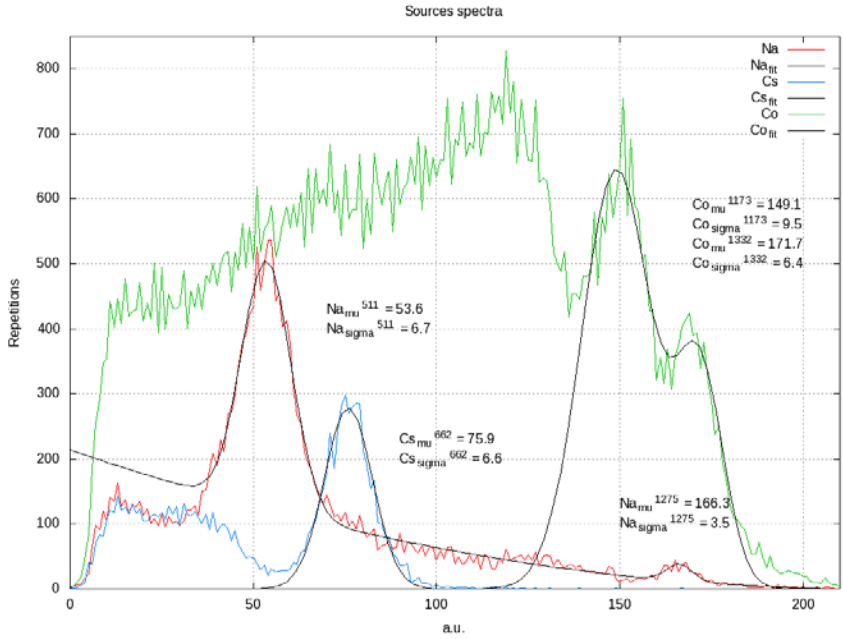


Figure 5.55: Na^{22}, Co^{60}, Cs^{137} spectra measurement

Source	**keV**	μ **(counts)**	σ **(counts)**	**Res.(%)**
Na^{22}	511	53.3	7.1	9.6
	1275	166.3	3.5[1]	-
Cs^{137}	662	75.9	6.6	6.9
Co^{60}	1173	149.1	9.5	5.6
	1332	171.6	6.4[1]	-

[1] Some more statistics or better fit should be needed

Table 5.4: Sources measurements for TH=40

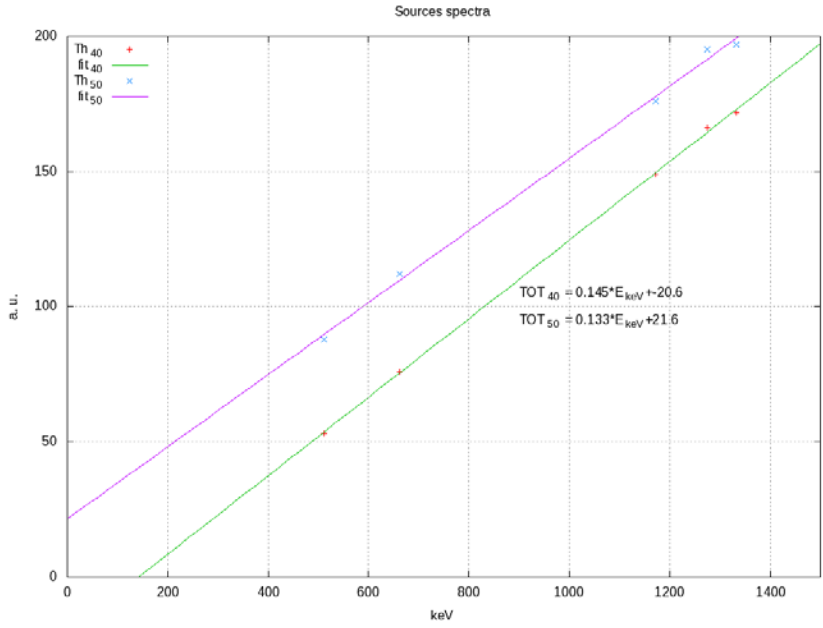


Figure 5.56: Linearity of the resulting spectra measurements

Source	**keV**	μ **(counts)**	σ **(counts)**	**Res.(%)**
Na^{22}	511	88	5.6	8.3
	1275	195	8[1]	-
Cs^{137}	662	112	6.2	7.1
Co^{60}	1173	176	9	5.8
	1332	197	5.7[1]	-

[1] Some more statistics or better fit should be needed

Table 5.5: Sources measurements for TH=50

5.3.10 Coincidence Resolving Time

To obtain a first estimation about the overall system timing accuracy, a preliminary measurement has been performed. The basics is to reproduce a coincidence system in the laboratory. The setup can be seen in figure 5.57 Two test boards with single channel SiPMs are placed facing to each other. On top of the SiPM the LSO crystal is placed. The Na^{22} radioactive source is placed as close as possible to both crystals and just in the middle to obtain coincident signals. The CML output is readout using differential probes. In the oscilloscope the timing and energy signals are acquired.

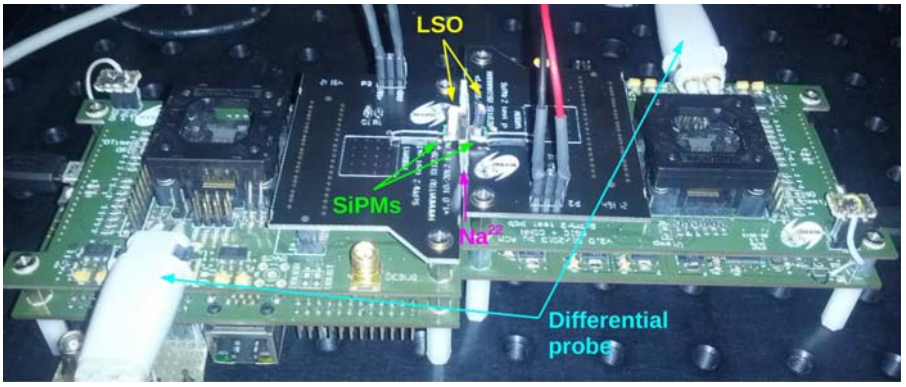


Figure 5.57: Coincidence system setup

Typical signals obtained by the system can be observed in figure 5.58.

Plotting both channels energy spectra results in a variation of clusters mostly concentrated in the 511keV energy. After running a clustering algorithm the events around 511keV are obtained (see figures 5.59 and 5.60).

Plotting those events and fitting the result, the final relevant events for the CRT measurement are reduced to $\pm\sigma$ (see figures 5.61 and 5.62 with the $\pm\sigma$ zones highlighted).

The resulting delay measurements of timing outputs from those events are plotted in an histogram to obtain the timing accuracy of the full system in figure 5.63.

The results show a consistent measurement of resolutions below 300ps FWHM (around 115ps rms).

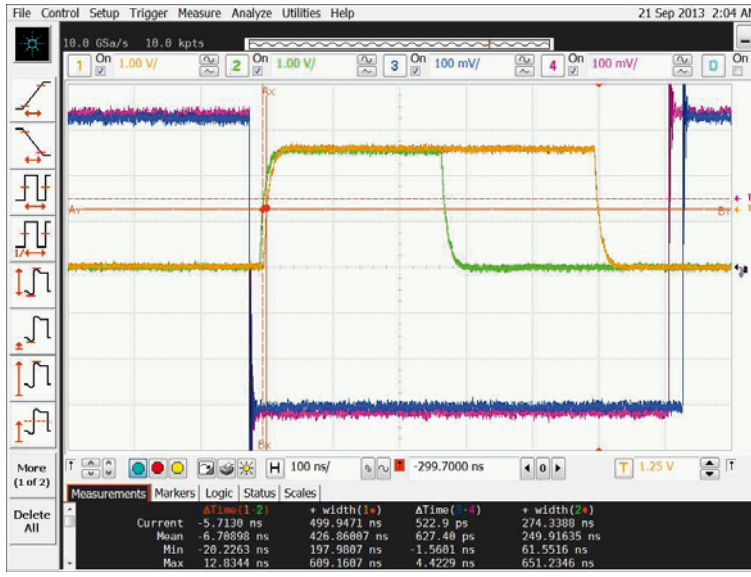


Figure 5.58: Typical signals acquired by oscilloscope

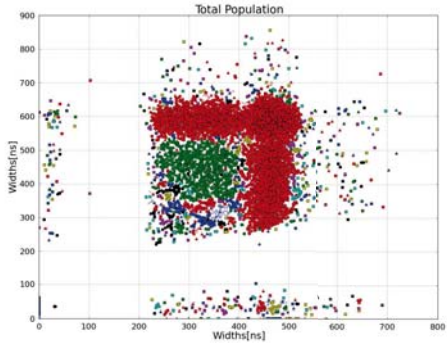


Figure 5.59: CRT data clusters identified

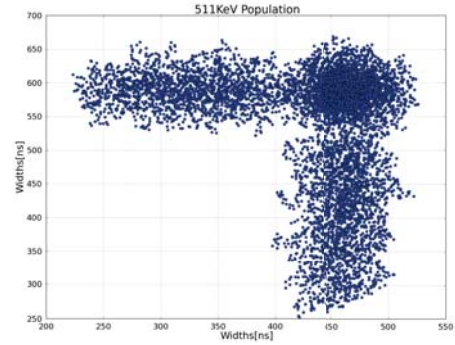


Figure 5.60: CRT data around 511keV

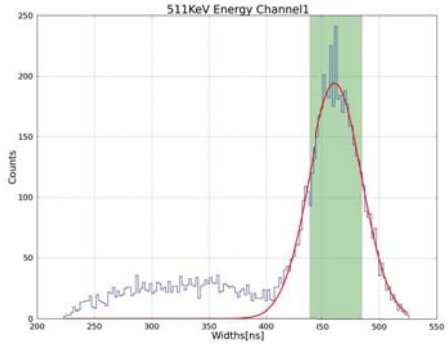


Figure 5.61: Channel 1 energy measurement

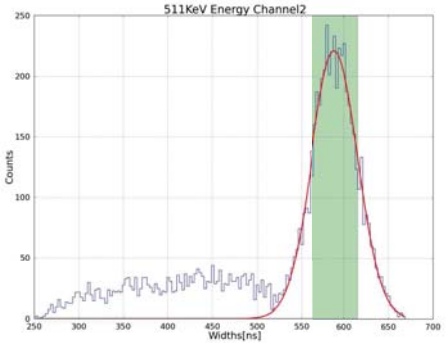


Figure 5.62: Channel 2 energy measurement

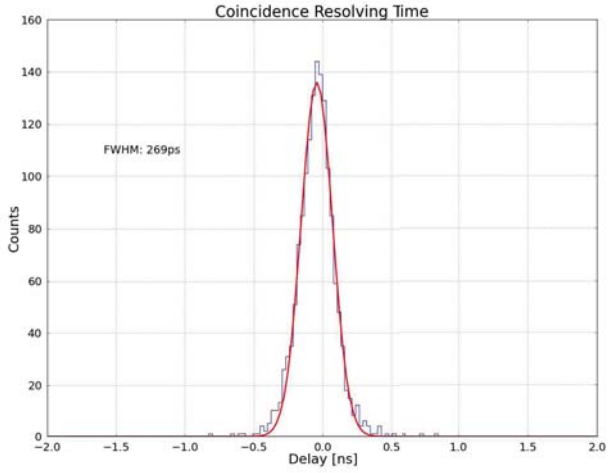


Figure 5.63: Coincidence Resolving Time

5.3.11 PET system measurements

Several measurements have been performed at CIEMAT to check the viability of the electronics for a full PET system. Including two sensors placed face to face with a mobile (rotating) platform in the middle (used to emulate a full ring of detectors). The setup can be seen in figure 5.64. Several samples (radioactive sources) are placed in the mobile platform to characterize the system.

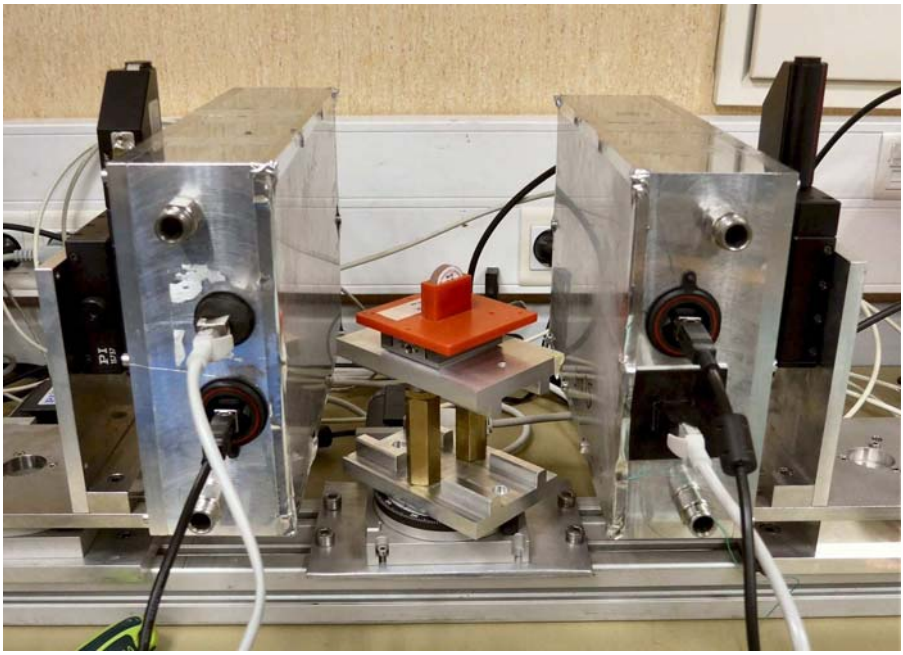


Figure 5.64: Test system at CIEMAT

Once data is acquired image reconstruction techniques are used to derive a 2D image representing the zone from the incoming signal. The reconstruction algorithm applied in this case has been Filter Backprojection (FBP)[53], even though more complex algorithms[54] could also be used to improve spatial resolution with the cost of incrementing reconstruction time.

A first measurement can be observed in figure 5.65 with the measurement of a single Na^{22} (0.25mm diameter) radioactive source (left) placed in two different positions and reconstructing the position in the same image. On the right two Na^{22} (1mm diameter) sources are placed at 4mm separation

and data acquired and reconstructed. More systematic measurements with different separation of the sources can be seen in figure 5.66 with a summary on table 5.6. As expected final spatial resolution is around few mm.

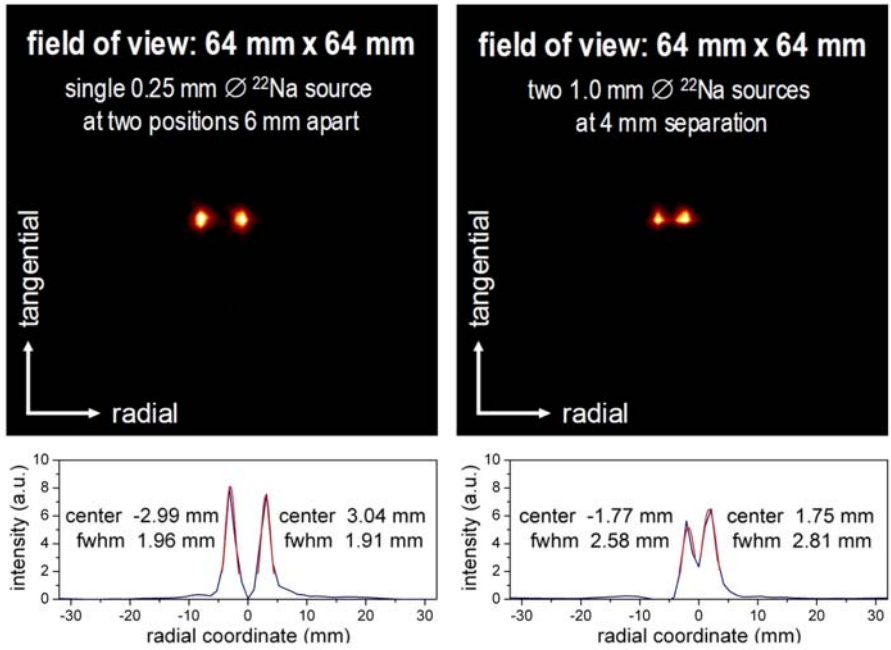


Figure 5.65: PET initial tests at CIEMAT

Distance	**Center Na_1^{22}**	**FWHM Na_1^{22}**	**Center Na_2^{22}**	**FWHM Na_2^{22}**
2 mm	0.11 mm	3.03 mm	0.11 mm	3.03 mm
3 mm	-1.18 mm	2.94 mm	1 mm	2.65 mm
4 mm	-1.77 mm	2.58 mm	1.75 mm	2.81 mm
5 mm	-2.26 mm	2.57 mm	2.25 mm	2.48 mm

Table 5.6: CIEMAT spatial resolution measurements

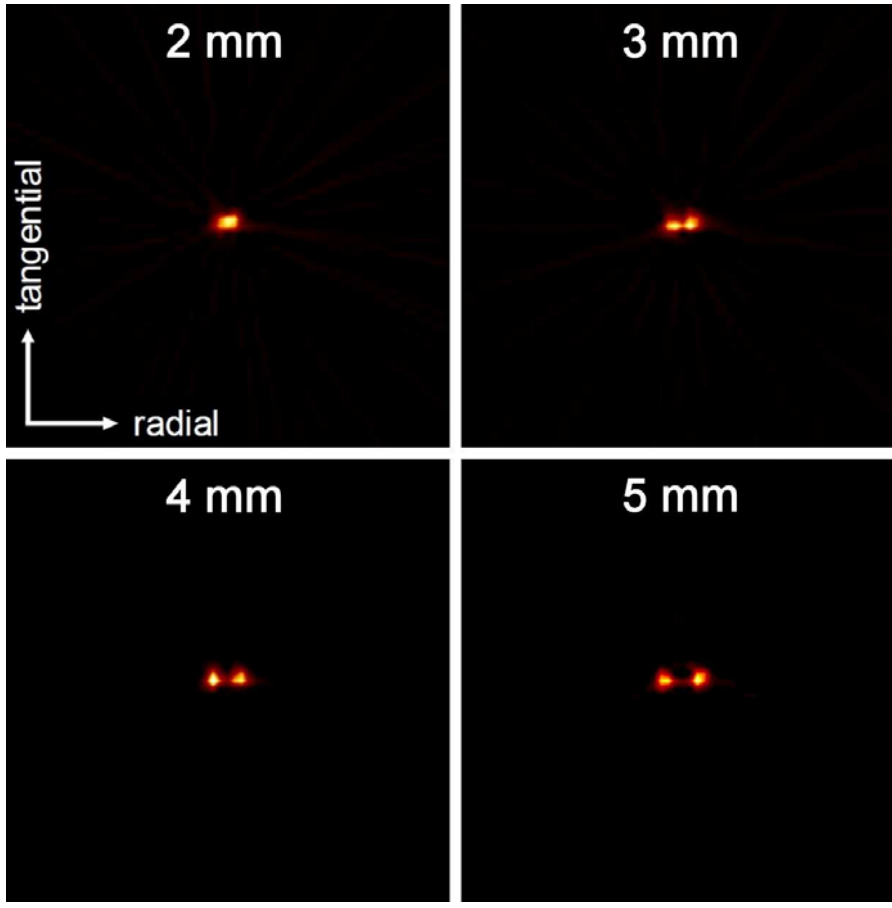


Figure 5.66: PET spatial resolution measurements

6

Design for SciFi Tracker

High luminosity particle detectors must operate at much higher rates than in other systems (such as PET). The tracker sub-detector of the LHCb experiment reveals the paths of electrically charged particles as they pass through and interact with suitable substances[6]. Particle records a weak electrical signal that particles trigger as they move through the device. Normal detectors use silicon devices (strip detectors) or gaseous detectors (straw tubes). Once the signal is acquired and readout a computer program reconstructs the recorded patterns of tracks.

The current LHCb Tracker stations are composed of an Outer Tracker (OT) with straw tube detectors and an Inner Tracker (IT) with silicon strip detectors to cover the high-occupancy area near the beam pipe (see figure 6.1). The new technology for the OT IT upgrade will be based on scintillating fibres, with clear fibres carrying the signal photons from the inner region to the detectors situated outside the LHCb acceptance.

In the first draft of the Letter of Intent for the LHCb upgrade[6], a new scintillating-fibre layout has been proposed, with 2.5 m long fibres covering the whole central region of the tracker stations, from the LHC beam plane all the way to the top and bottom of the LHCb acceptance (see figure 6.2). In this Central Tracker (CT) option, the IT and several (or all of the) OT modules are replaced by the new scintillating-fibre modules. Full detector is built by 3 stations with three tilted ($\leq 5^o$) fibre planes of X-U-V-X. Every plane is made of 5 layers of 250 μm in diameter fibres and 2.5 m long.

One of the major concerns is the production and alignment of the fibres

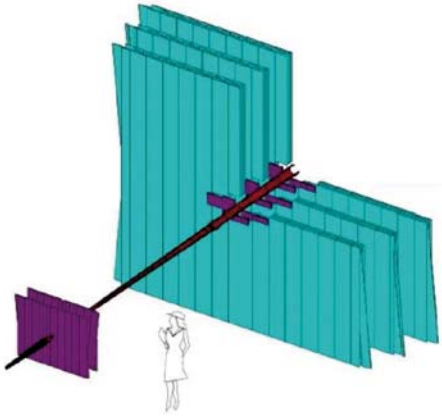


Figure 6.1: Current tracker in LHCb

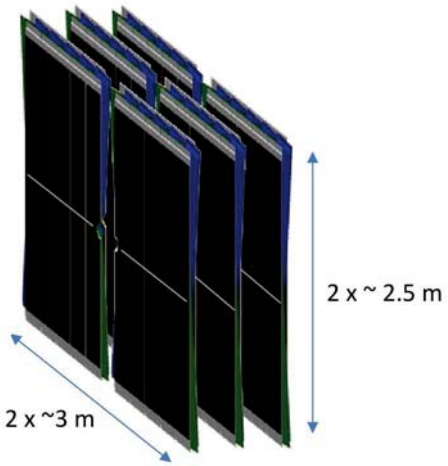


Figure 6.2: New design of LHCb tracker

in the modules. Some new techniques have been developed to produce such modules and showed promising results. In figure 6.3 a photography of a prototype using double cladded Kurarary SCSF-78 250μm diameter fibres can be seen.

Figure 6.3: SciFi fibres module

The previously presented current mode input stage will need redesign (to fit a different technology and requirements). Current input stage proved excellent characteristics for larger scale SiPM and can also be used for the proposed detector focusing on a more integrated design with optimized layout to reduce size and increase integration. A fully CMOS version has been developed for this purpose.

A collaboration with Clermont Ferrand and opened to any other institute from LHCb is ongoing and a common design effort will be developed. Development will be the low Power Asic for the sCIntillating FIbres traCker, PACIFIC.

Several processing strategies are under study, but the simplest one seems to be the baseline solution, involving pre-amplifier, shaper, gated integrator

and ADC. More complex processing is also under study.

The SciFi Tracker is a detector with a very compact mechanical design. This leads to some problems when defining the electronics basically related to the amount of power required in a very small space. The integration of 128 channels in the sensor also claims for very compact readout electronics. One can imagine in a maximum of two ASICs per sensor or an ideal value of 1 sensor 1 ASIC.

A tentative design of the front end electronics board is depicted in figure 6.4. In this design the SiPMs are depicted with a flexible printed circuit board adapter and a cooling bar block in contact. The flexible circuit rotates 90 degrees and then connects to the front end board. On the board in an area of 12x10cm should fit the readout ASICs of 3 arrays of 128 channels, the digital processing (FPGA or ASIC), the power conversion and the optical links (bottom middle, 2 double in the picture). Optical links could be managed using the GBTx[56] designed by CERN or by an FPGA[57]. GBT-SCA is for the slow control of the ASICs.

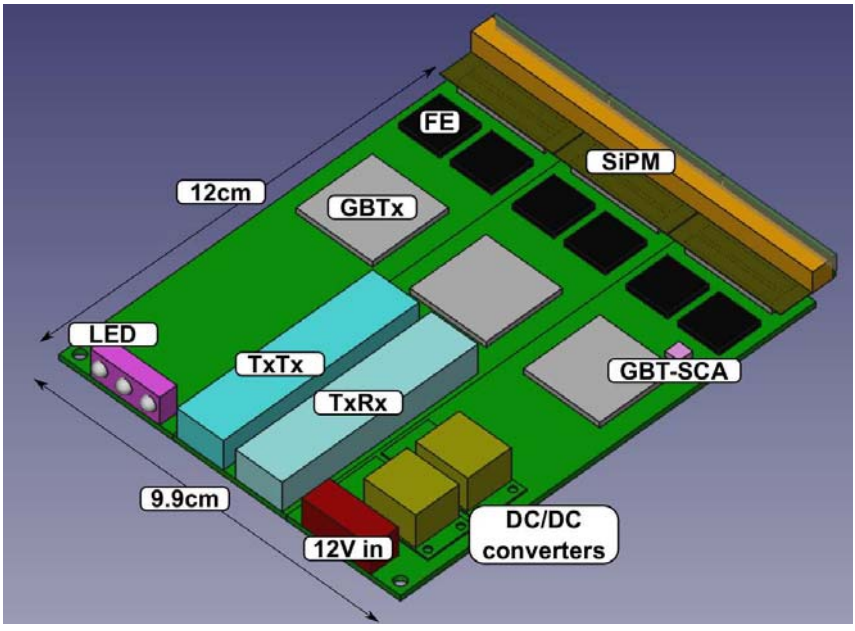


Figure 6.4: SciFi readout electronics

In conclusion the final space available should limit the number of ASICs per sensor array to one or a maximum of two, defining the number of channels to either 64 or 128. The packaging of the ASIC should also reduce

to the maximum the routing space needed. The BGA package seems the best option.

6.1 Front End Electronics

In terms of Bandwidth the requirements are the same as in previous design (chapter 5) since no extra constraints are added. But in this case more constraints are applicable.

6.1.1 Number of channels

Currently prototypes being developed keep a goal of 128 channels in the same device (normally 2 dies packaged together). This should be the goal of the designed electronics, to have a perfect match between sensor and readout electronics. This simple approach but leads to some important problem, die size. In IBM 0.13μm technology (the default used by CERN and thus in this project) area costs are important and should be kept to a reasonable value.

For the high number of channels it seems reasonable that the design will be PAD limited. In this scenario we could think on two different PADs arrangements (see figures 6.6 and 6.5). The typical arrangement (6.5) is a simple row of input output PADs in a row keeping minimum distances. A more compact design alternative (6.6) is the so called staggered PADs layout, in which two columns of PADs are used for input output.

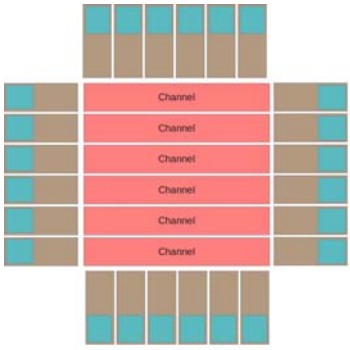


Figure 6.5: Inline PADs

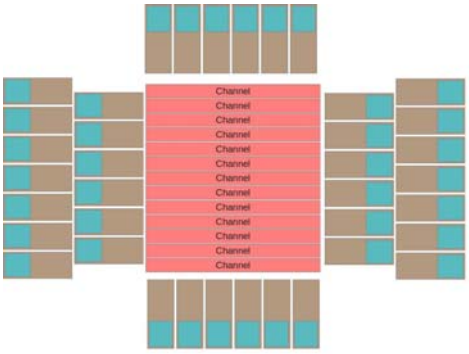


Figure 6.6: Staggered PADs

The staggered PADs option is the optimal one for this design but since the density of channels is doubled the height of the resulting channel is

reduced to half. In this technology the minimum pitch between two analog PADs is around 80μm so the maximum height of channel by design should be 40μm.

Some extra space (not depicted in previous figures) will also be needed to accommodate the needed common bias and control blocks for the full ASIC. Normally this block should be placed in the middle of the channels to reduce the routing distance between this part and the channels.

6.1.2 Power consumption

Although power consumption is not limited, a first approach suggests it should be reduced to the minimum. The main issue is the sensors (SiPM array) will probably be cooled to very low temperature to avoid dark count increase with radiation damage. As the sensors will be close to the analog ASIC, the heating produced by the electronics could affect the sensor cooling system. An other limiting factor is the power supply, DC-DC converters radiation tolerant are being developed at CERN, but their output current is 3A maximum. If a single converter is used for the analog electronics a maximum of 1A should be available for 128 channels. Taking into account nominal supply is 1.2V this leads to a maximum of 1.2W per 128 channels. If some margin is added a reasonable power consumption should be 1W for a 128 channels ASIC or 7.5mW/channel. This calculation agrees with previous chapter maximum power consumption without cooling of around 1W (depending on package and thermal design).

6.1.3 Timing constraints

Incoming particles bunches in LHC arrive every 25ns so at this frequency collisions are generated.

6.1.3.1 Double peak resolution

The most important constrain for the electronics is an output must be given every 25ns being able to process next event. This is commonly described as a double peak resolution time of 25ns.

6.1.3.2 Spill over

In order to minimize spill over (two events overlapped due to slow tails) the electronics must preserve the pulse shape from the SiPM with a small

input impedance (for a fast recovery), but keeping in mind low power consumption trade-off. Some signal processing should also be needed to reduce at an acceptable level the spill over.

6.1.4 Noise

As in general designs for a single fired cell resolution the S/N ratio should be greater than 10 in the charge spectra. The input referred noise in function of the input charge and integration time is determined[55] by equation 42, being T the integration time and Q_{in} the input charge. For a SiPM typical gain of the order of 10^6 thus for a single photon a total of 1.10^6 electrons will be generated (or multiplying by the electron charge, 16.10^{-14} Coulombs).

$$i_{in} \leq \frac{\sqrt{2}.Q_{in}}{\sqrt{T}.\frac{S}{N}} \leq \frac{\sqrt{2}.16.10^{-14}}{\sqrt{25.10^{-9}}.10} \leq 143\frac{pA}{\sqrt{Hz}} \tag{42}$$

Keeping the S/N>10 the referred noise at the input should be smaller than $\frac{143pA}{\sqrt{Hz}}$.

6.1.5 Signal from SiPM

Two manufacturers SiPM are being studied at the moment. 128 channels prototypes are being manufactured by Ketek and Hamamatsu. They are designed to provide the 128 channels with the minimum dead area possible and fitting the fibres modules size. In figure 6.7 a photograph of one of the Hamamatsu prototypes can be seen with it's mechanical drawing.

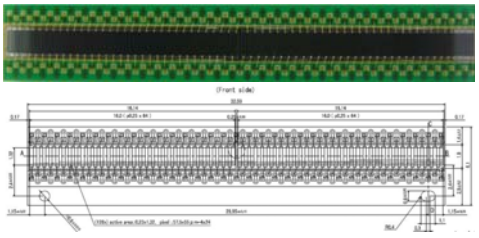


Figure 6.7: Hamamatsu SiPM array prototype

The prototype is based on two 64 channels devices in the same die glued together over a substrate with align holes to minimize the dead area between them. Ketek prototypes follow the same form factor.

During December 2012 several preliminary measurements on a prototype fibres module where carried out at CERN denoting the different shape of the signal provided by two sensors. The fibres are excited by a Sr^{90} radioactive source with a fixed magnet to filter only signals with energy equal to a Minimum Ionizing Particle (MIP). It is the same source used for the characterization of LHCb pre-shower and Scintillator Pad Detector (see figure 6.8). In those tests a single fibre was replaced by a fibres module with an array of SiPMs connected at the end. Signal is read using a low gain high speed amplifier with the output connected directly to the oscilloscope. A small PCB was designed to fit the amplifier and a pair of connectors to the flexible board adapter where SiPMs are placed (see figure 6.9).

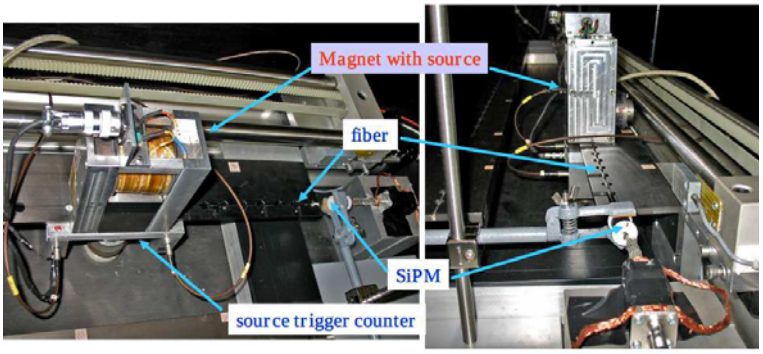


Figure 6.8: Measurement system setup

The resulting measurements show very different shapes depending on the detector used. In Hamamatsu devices the signal follows a fast rising edge and an exponential decay. In Ketek prototype the signal follows a much faster rising edge with a first and fast decay followed by a second and much slower than Hamamatsu exponential decay, see figures 6.10 and 6.11.

With previous measurements it's clear some shaping circuitry will be needed to compress the signal in a 25ns window.

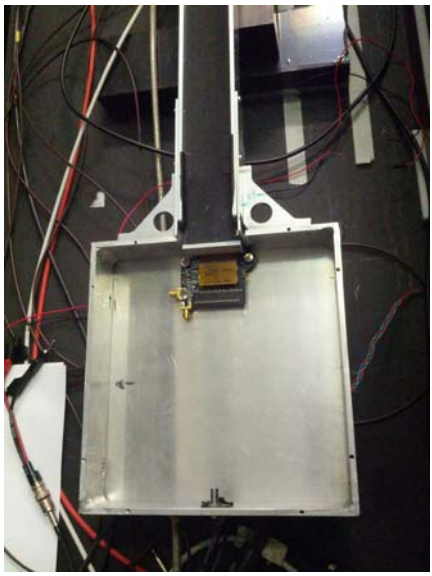


Figure 6.9: Adapter board for the module readout

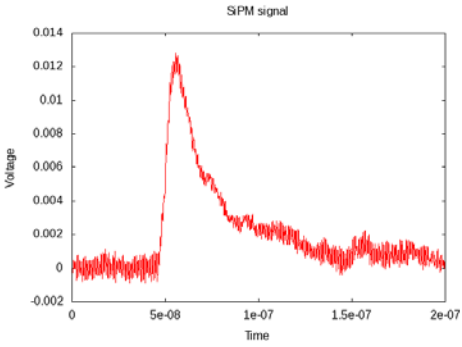


Figure 6.10: Hamamatsu signal

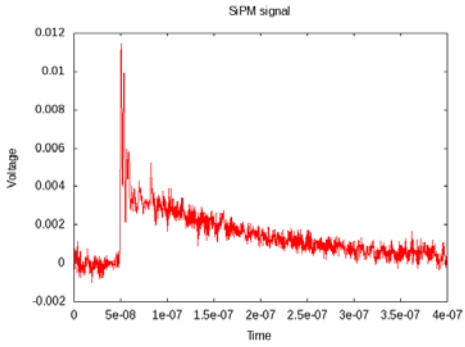


Figure 6.11: Ketek signal

6.1.5.1 Dynamic range

SiPM prototypes have a fixed number of 96 micro-cells. This should be the absolute maximum value to be read from the devices. But in real measurements signal is much more limited by the photo-statistics which is rather low. For this reason and also for calibration it is important to be sensitive to very small signals from a single micro-cell.

6.1.5.2 Propagation delay

In previous measurements the position of the radioactive source was moved between different positions. Those positions are near to the SiPM, in the middle of the module and far from the sensor. Using an extra sensor placed over the radioactive source as a trigger signal the absolute time of arrival at the SiPM can be measured. If wthe shape of the signal obtained in the three positions is compared, it can be seen it's very constant (see figure 6.12), measurement is done using Hamamatsu sensor.

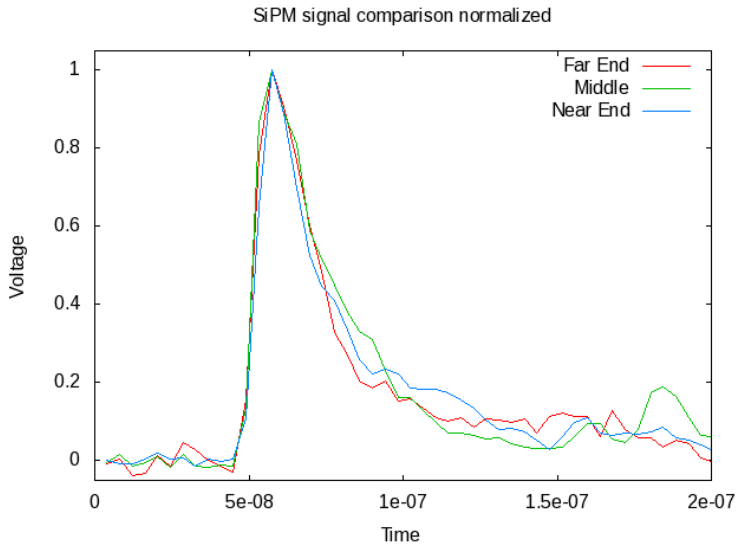


Figure 6.12: Normalized comparison of signals

If the different times of arrival are plotted (see figure 6.13 we obtain a maximum variation of around 12-15ns. This is around 50% the time window available for processing the signal.

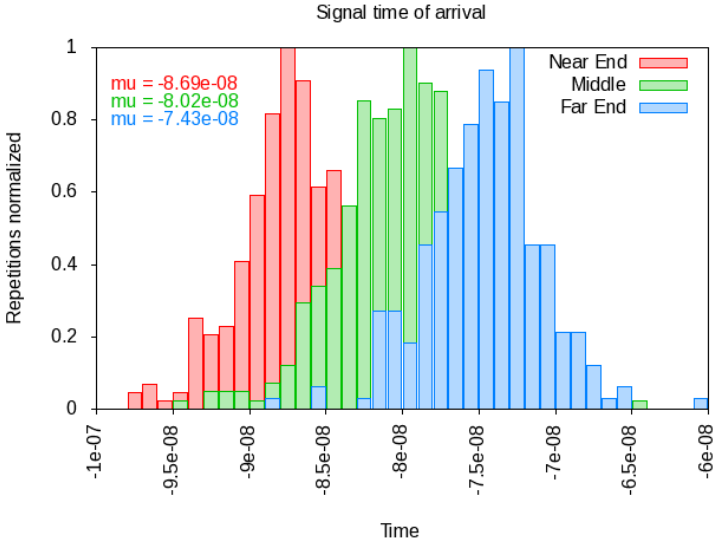


Figure 6.13: Time of arrival of signals

6.1.5.3 Mirror

To improve the light yield produced by the fibres it is expected to add a mirror at the end of the detector. It will have the effect of increasing the photons produced at the far end, since the ones generated in the opposite direction will be reflected. In the event of a production in the middle of the detector some signal will arrive later than the main signal. In figure 6.14 a signal with a mirror placed at the end of the detector can be compared to a signal without the mirror. The light is produced in the middle of the detector. If the event is produced at the near end of the detector it is expected that nearly no signal will be back from the mirror due to the attenuation. Note a second peak after the main signal generated by the mirrored light around 30ns later.

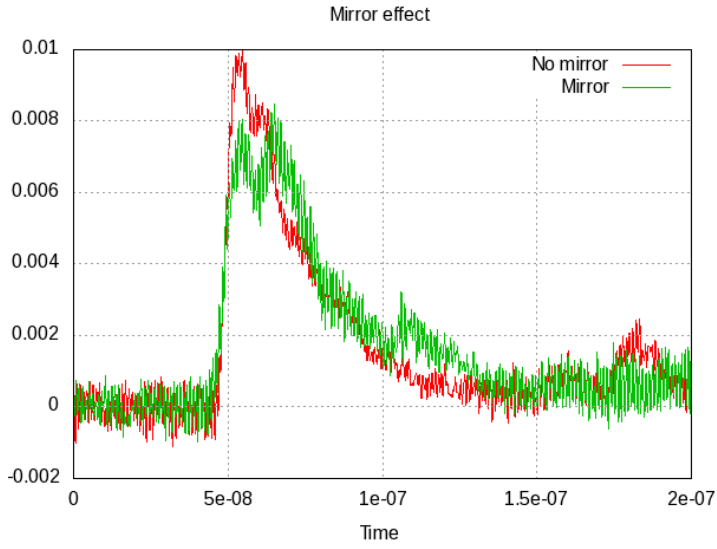


Figure 6.14: Mirror effect on signal

6.1.6 Slow control

The inclusion of some controllable elements for polarization mainly and for tuning the SiPM voltage will lead to some digital control interface. To keep the number of pins low a serial protocol is expected to be integrated in the forthcoming prototypes. An I^2C protocol is a good candidate for this purpose.

6.1.7 Data link

The amount of channels that should be included in the final design, the number of bits to be extracted by each of them (5 or 6) and the high rate (every 25ns) suggests that even if occupancy is low a high volume of information will be produced. This information should be transmitted to next step in the processing chain (probably an FPGA). The problems of going from the ASIC to an other commercial device is mainly the number of lines to connect both and the voltage swing (power consumption and noise generated). For this reason a single ended LVCMOS signal should be dropped and replaced by high speed serialized signals with low voltage swing interface (LVDS or CML). The final implementation will depend on the capabilities of the FPGA.

6.1.8 Specifications summary

A summary of previous section conclusions is detailed in table 6.1.

Parameter	Value	Unit
Channels	64 or 128	-
Power	0.5 or 1	W
Package	BGA	-
Double peak resolution	25	ns
SiPM time constant	To Be Defined	-
Dynamic range	0-64	micro-cells
Signal time of arrival	0-15	ns
Input referred noise	$\leq$143	$\frac{pA}{\sqrt{Hz}}$

Table 6.1: PACIFIC specifications summary

6.2 Implementation

In next section the implementation for the first prototype submitted (PACIFICr1) is described. It is an optimized version of the previously presented pre-amplifier prototype double feedback structure. Adapted to a newer 0.13μm technology with much lower power supply. The portability and flexibility of this input stage permitted to be adapted to a pure CMOS technology keeping excellent characteristics.

6.2.1 Architecture

The channel architecture proposed for the PACIFIC design is depicted in figure 6.15. Although other alternatives are under study, specifically a fastest digitization followed by digital processing, the easiest solution seems to shape and integrate signal in the 25 ns window. Since no dead time is allowed a double and interleaved gated integrator will be needed. After the integration a 40MHz ADC will convert the signal to digital. Afterwards a serial link will take the signal from one or several channels and serialize them into a single (probably differential) high speed link. For this last step some kind of multiplication frequency circuit will be needed (for example a PLL in the figure).

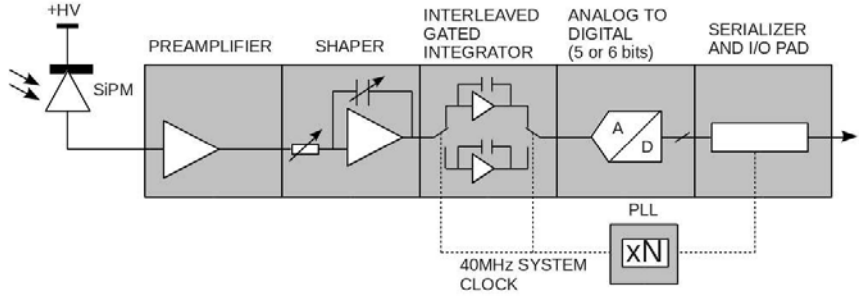


Figure 6.15: PACIFIC channel blocks

Some common bias and digital control of configurable voltages, currents and shaping parameters will also be needed. So current DACs, voltage DACs and variable resistors and capacitors will also be designed, with a slow control interface built in standard cells.

6.2.2 Preamplifier

The input stage is current mode preamplifier with the current flowing from the SiPM anode to the circuit. The goal is to achieve the following specifications in this block;

- High bandwidth ($\approx$ 250MHz).
- Low power ($<$ 2mW, maximum of 8mW/channel including all ASIC).
- Low input impedance ($20\Omega < Z_{in} < 40\Omega$).
- DC voltage controllable at input node ($\approx$ 1V range).
- Input referred noise $\leq 143\frac{pA}{\sqrt{Hz}}$

The basic circuit to achieve previous features is depicted in figure 6.16. The input stage is based on circuit described in chapter 4 using a novel approach of double feedback but with some variations to adapt to a newer technology process (IBM 0.13μ m).

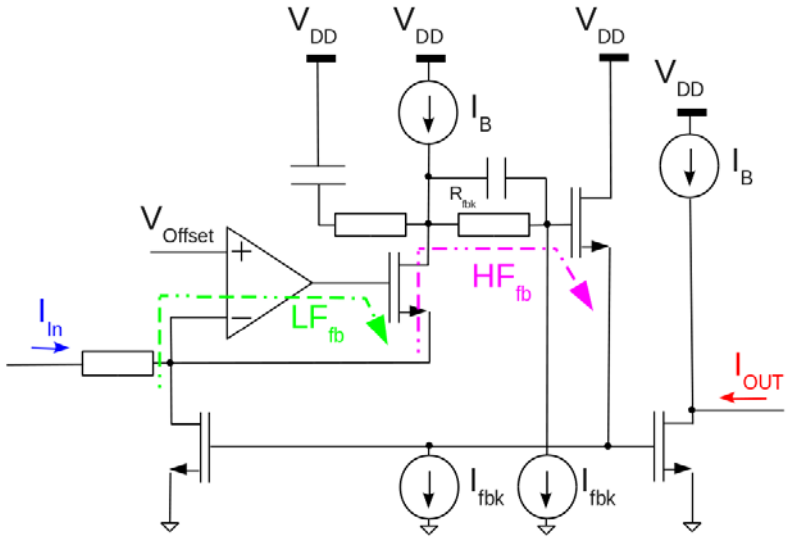


Figure 6.16: PACIFICr1 blocks

It provides a low input impedance in order to avoid affecting timing behaviour of the SiPM and increase input current. HF_{FB} is the high frequency feedback path that keeps this input impedance constant (in a certain frequency range). The second labelled path, LF_{FB} will provide the dc voltage

(V_{offset} in figure) of the input node using the virtual short circuit in the amplifier that will drive a follower in a lower frequency range. The design has been implemented taking into account that dominant pole should be set at the input node (SiPM parasitic capacitance is at the order of tenths of pF). In this way stability is not compromised when an important capacitance is added at the input.

6.2.2.1 Multiple voltages operation

As described in the requirements an important element of the circuit is the possibility to tune the voltage at the input node. Due to the fact this technology uses low voltage polarization (1.2V) an important effort has been made to maximize the range of this voltage variation. The easiest option is to power the circuit at a higher voltage (1.5V). For this reason a configurable pre-amplifier optimized for the two operating conditions has been designed. The only part needing changes is the high frequency feedback path. An adjustable pair of RC values can be switched by an external control pin. This change adapts behaviour to the desired operating voltage. In table 6.2.2.1 the selection options are described.

VSEL	Switch	VDD
1.2	ON	1.2
0	OFF	1.5

Table 6.2: VSEL operation

6.2.3 Simulation results

PACIFICr1 prototype is still under production, for this reason only simulation results are presented. Some precautions on design (add parasitic elements such as wire bonding inductance) should assure a real behaviour close to simulations.

6.2.3.1 Input impedance

Input impedance is kept low using the high frequency feedback loop. This kind of feedback loops present an inductive behaviour at high frequencies. The simulation can be observed in figure 6.17. The input impedance is kept to a low value corresponding to the resistance in series (16Ω) at the pre-amplifier input until around 100KHz. From this point increases slowly to reach a value of around 34Ω at 100MHz. Passed this frequency impedance increases fast reaching a value of 50Ω at around 250MHz.

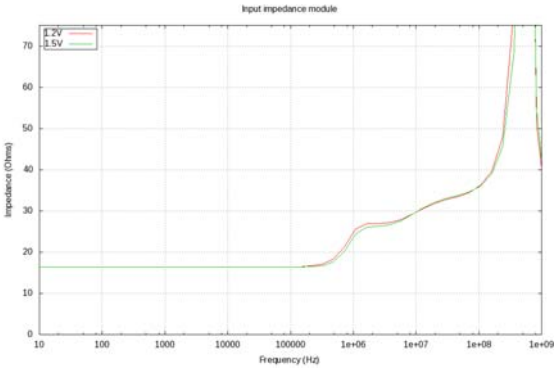


Figure 6.17: PACIFICr1 pre-amplifier input impedance

6.2.3.2 Input voltage variation

To determine the range of input node voltage adjustment the error on voltage adjustment is plotted. The results can be seen in figure 6.18. When feedback loop starts to became out of the operation range the voltage error increases faster. The obtained ranges are around 0.6V for a 1.2V power supply and around 0.9V for a 1.5V power supply as expected. In order to increase voltage variation triple well transistors have been used for the MOS feedback.

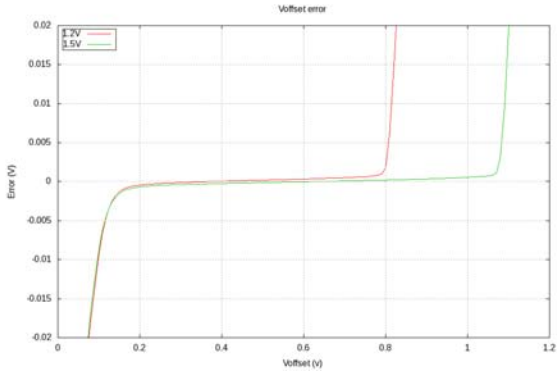


Figure 6.18: PACIFICr1 Voffset error

6.2.3.3 Bandwidth

The Bandwidth of the pre amplifier should be greater than 250MHz. The influence of input capacitance is to reduce the Bandwidth of the circuit. For this reason it is important to design it as immune as possible to this effect. In figure 6.19 the AC analysis of the input stage with a pair of input capacitances (5pF and 15pF) show greater values than 250MHz bandwidth. So it should not be a problem with those values.

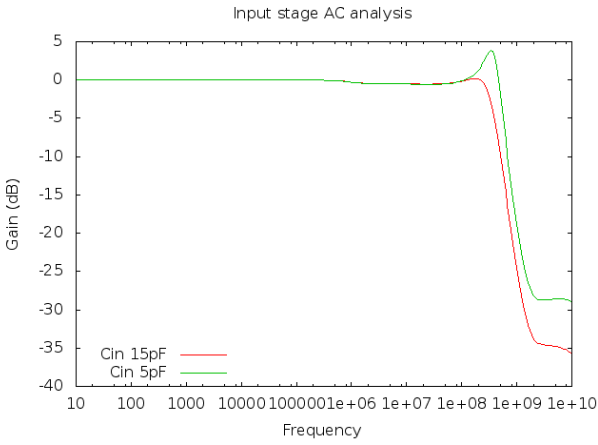


Figure 6.19: PACIFICr1 pre-amplifier Bandwidth

6.2.3.4 Linearity

An important measurement to be performed on the input stage is the linearity expected in the full range of input signal.

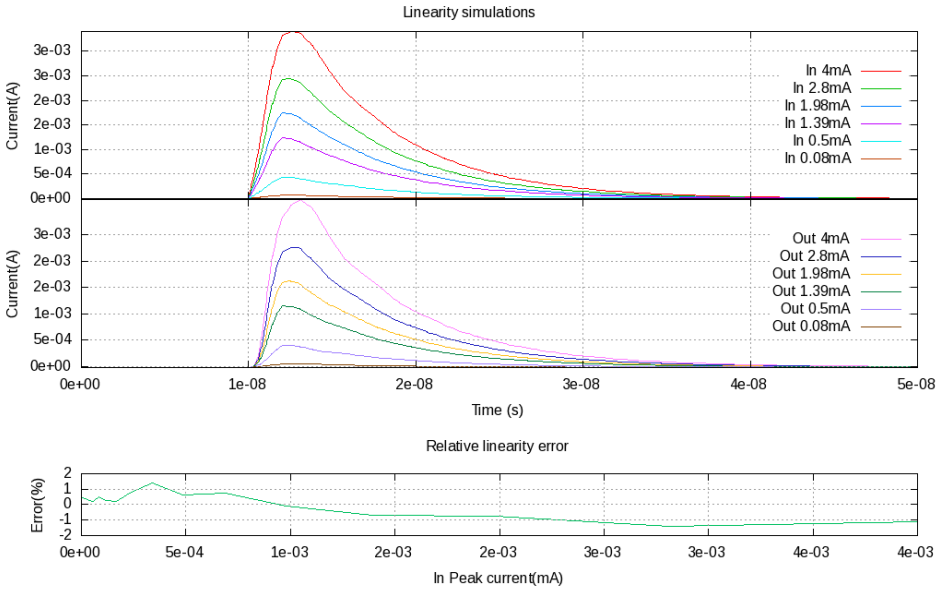


Figure 6.20: PACIFICr1 Linearity simulation

6.2.3.5 Noise

Noise simulations show no issues with just input stage, it's below 100 $\frac{pA}{\sqrt{Hz}}$ until 250MHz frequencies (see figure 6.21).

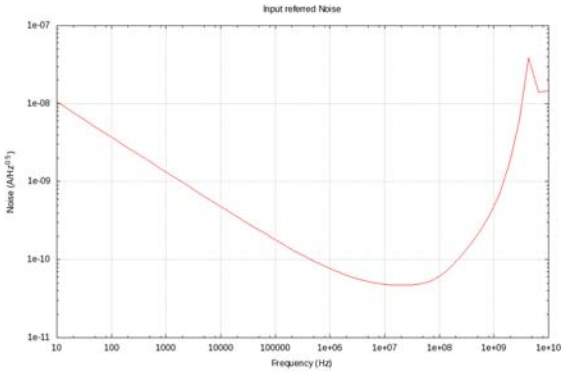


Figure 6.21: PACIFICr1 Noise simulation

6.2.4 Layout

Final layout of the pre-amplifier only needs an area of 335μm x 40μm. The usage of high levels capacitors (MIMCAPS) with electronics buried below helped in reducing the overall area needed in the design keeping the needed characteristics.

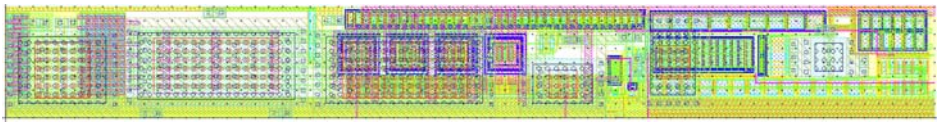


Figure 6.22: PACIFICr1 pre-amplifier layout

7

Conclusions

A novel current conveyor topology with double feedback structure has been presented and demonstrated it's excellent characteristics, with low noise, low power, wide dynamic range and low input impedance. The full system tests proved to be a good option compared to previous similar ASICs.

A detailed description on the sensor properties and requirements for both a PET detector and SciFi tracker has been exposed. A behaviour model from the sensor has been useful in the design stage to simulate circuit behaviour. Two designs using this circuit intended for PET and SciFi have been detailed. Both of them use similar input stage but implemented on different technologies. PET prototype uses SiGe technology and benefits from the bipolar transistors usage (specially on input stage and reference circuits), while SciFi prototype is a CMOS technology but benefits from a smaller feature size.

7.1 Achievements

Compared to previous designs the proposed solution keeps an excellent balance between power consumption, dynamic range, noise and timing resolution (see table 7.1 with a qualitative representation of the achieved values comparing with ASICs providing timing and charge information). It is also the only available for a direct current mode anode connection for SiPM arrays.

The main goals for the PET system have been fulfilled. A multi-channel architecture with direct connection to the SiPMs and analog processing has successfully been designed and tested. The voltage adjustment on the input will permit to change sensor gain. Multiple signal paths proved to give the desired results. With excellent timing measurement and also good energy measurement and pile-up detection. The proposed input stage fits all the requirements and the rest of processing benefits from this. After design and production, full device testing has been performed including some tests that exceeds the mere electronics characterization (radiation sources tests and coincidence).

The design constraints on the PACIFIC project are still under study and this first prototype has served as a starting point. The circuitry designed for the SiPM readout (specifically the input stage) has been ported to a new technology and simplified for the application. Real prototype testing is still needed but meanwhile design is ongoing on the other blocks needed.

7.2 Outlook

In the FLEXTOT line of prototypes even if the basic functionality has been tested and verified and current prototype has shown promising results some issues should be addressed. It has proved to be an excellent solution for segmented crystals readout, but probably would not be the case for monolithic crystals. First because the resulting signal from a shared crystal between pixels would need higher gain in the electronics and secondly because uniformity between channels would require an important effort in post processing.

In the PACIFIC line of development a new prototype submission has been made on November 2013. It included pre-amplifier, shaper (different versions or tunable for the various SiPMs time constants) and gated integrator. This prototype should verify if the required functionality needed for the readout electronics of the SciFi tracker is feasible, before a more ambitious multi-channel ASIC with more functionality (and analog to digital conversion included) to be submitted at 2014. A tight schedule is foreseen after the verification of 2013 prototype to be ready for installation on the foreseen upgrade window in 2018.

Name	Manufacturer process	Time resolution	Energy resolution	Power	Array readout in current	Dynamic range
FLEXTOT	AMS 0.35μm	Very good	Very good	Low	Yes	Wide++
TOFPET	0.13μm	Very good	Good	Low	No	Narrow
SPIROC	AMS 0.35μm	Good	Very good	Low	No	Wide
NINO	IBM 0.25μm	Very Good	Good	High	Limited	Narrow
PETA	UMC 0.18μm	Very Good	Good	High	No	Narrow
BASIC	AMS 0.35μm	Poor	Very good	Low	No	Wide
VATA64	-	Poor	Very good	High	No	Wide

Table 7.1: FLEXTOT comparison with other ASICs

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List of Acronyms

2FDG 2-fluorodeoxy-D-glucose

ADC Analog to Digital Converter

ALICE A Large Ion Collider Experiment

AMS Ausria Micro-Systems

APD Avalanche Photo Diode

ASIC Application Specific Integrated Circuit

ATLAS A Toroidal LHC Apparatus

BGO $Bi_4(GeO_4)_3$

BiCMOS Bipolar Complementary Metal-Oxide-Semiconductor

CALICE CAlorimeter for LInear Collider Experiment

CE Collection Efficiency

CERN *Conseil Européen pour la Recherche Nucléaire* or European Organization for Nuclear Research

CML Current Mode Logic

CMS Compact Muon Solenoid

CP Charge-Parity

CSA Charge Sensitive Amplifier

CTA Cherenkov Telescope Array

CT Central Tracker

CT-X-ray X-ray Computed Tomography

DAC Digital to Analog Converter

DAQ Data AQuisition

DELPHI DEtector with Lepton, Photon and Hadron Identification

DESY *Deutsches Elektronen-SYnchrotron* or German Electron Synchrotron

DNL Differential Non Linearity
ECAL Electromagnetic CALorimeter
FBP Filter Backprojection
FF Fill Factor
FPGA Field Programmable Gate Array
FSM Finite-State Machine
FWHM Full Width at Half Maximum
GSO $Gd_2(SiO_4)O$:Ce
HCAL Hadronic CALorimeter
HEP High Energy Physics
HPD Hybrid Photo-Diode
I^{2}C Inter-Integrated Circuit
IBM International Business Machines Corporation
ILC International Linear Collider
INL Integral Non Linearity
IT Inner Tracker
JTAG Joint Test Action Group
LDO Low Drop-Out
LED Light Emitting Diode
LEP Large Electron-Positron Collider
LHCb Large Hadron Collider *beauty*
LHC Large Hadron Collider
LIDAR LIght raDAR
LOR Line Of Response
LSO $Lu_2(SiO_4)O$:Ce
LVDS Low Voltage Differential Signaling
LYSO $Lu_{1.8}Y_{0.2}(SiO_4)O$:Ce
MIP Minimum Ionizing Particle
MRI Magnetic resonance Imaging
MRPC Multigap Resistive Plate Chamber
OT Outer Tracker
PACIFIC low Power Asic for the sCIntillating FIbres traCker
PDE Photon Detection Efficiency

PET Positron Emission Tomography
PLL Phase Locked Loop
PMT Photo Multiplier Tube
PS Pre-Shower detector
QE Quantum Efficientcy
RAM Random Access Memory
RICH Ring Imaging CHerenkov detector
RMS Root Mean Square
SAR Successive Approximation Register
SCA Switched Capacitors Array
SiPM Silicon Photo Multiplier
SNR Signal to Noise Ratio
SOC System On Chip
SPD Scintillator Pad Detector
SPDT Single Pole Double Throw
SPECT Single-Photon Emission Computed Tomography
SPICE Simulation Program with Integrated Circuit Emphasis
TAC Time to Analog Converter
TAP Test Acces Port
TCK Test Clock
TDC Time to Digital Converter
TDI Test Data Input
TDO Test Data Output
T&H Track And Hold
TMS Test Mode Select
TOF Time Of Flight
TRST Test Reset
TT Trigger Tracker

List of Figures

List of Tables

A

SiPMVFEr1 Datasheet

SiPM readout blocks

Data Sheet SiPMVFEr1

FEATURES

Current mode input.
Low input impedance.
Zero components interface between sensor and device.
High Bandwidth preamplifier (≈350MHz).
Relative linearity error ±5%.
High Dynamic Range to operate SiPM at high overvoltage.
Low Power consumption (≈7.3mW/channel).

APPLICATION

Readout of Silicon Photo Multipliers arrays.

DESCRIPTION

SiPMVFEr1 is a prototype with some blocks for the readout Silicon Photo Multipliers with current mode input.
SiPMVFEr1 has been developed using Austria Micro Systems (AMS) 0.35 μm HBT BiCMOS technology and operates over the -40°C to +125°C junction temperature range.
SiPMVFEr1 is available in a QFN32 package.

TYPICAL APPLICATION CIRCUIT

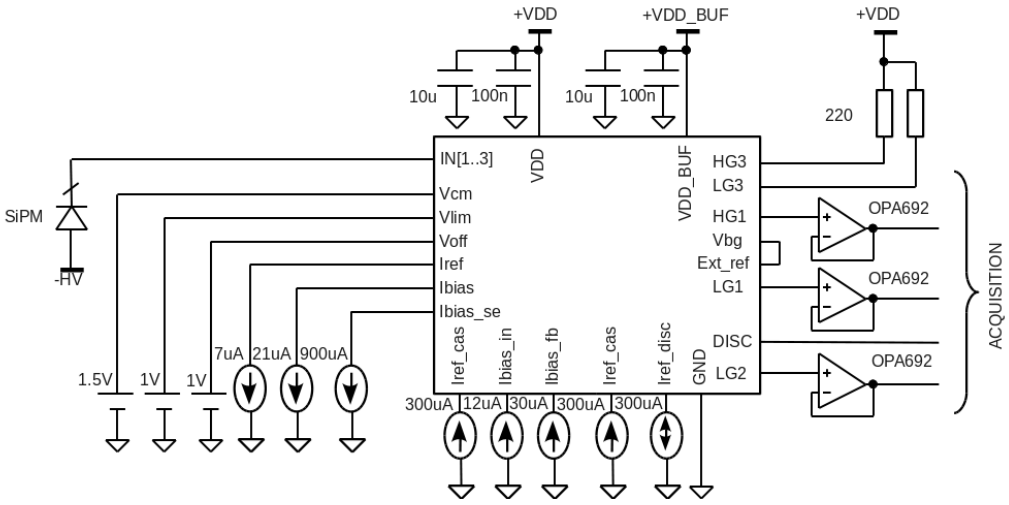

Figure 1: Typical application schematic

Av. Diagonal 645, Barcelona, ES08028, SPAIN
Tel. 934021587
Fax. 934037063
http://icc.ub.edu

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REVISION HISTORY

03/13 - First version

FUNCTIONAL BLOCK DIAGRAM

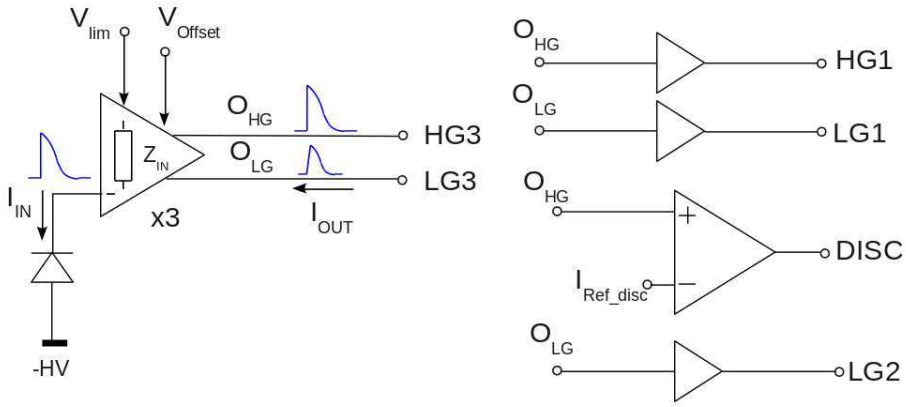


Figure 2: Channel block diagram

Every channel contains three different paths used for time of arrival measurement and energy measurement;

The time of arrival measurement performed using a High Gain path. In channel 2 this High Gain output is connected to a current mode discriminator to generate a digital signal.

The energy measurement uses a lower gain output, Low Gain path. In channel 1 and 2 this Low Gain output is connected to a buffer to attack the external load, while in channel 3 it's directly connected to the PAD.

Apart from the channel analog chain a common bias block is also present with a BandGap Voltage reference which can be measured directly.

SPECIFICATIONS

T_A=25°C, V_{DD}=3.3V, V_{DD_BUF}=3.3V

Parameter	Conditions	Min	Typ	Max	Unit
INPUT					
Z_{in}	Default input stage polarization currents	20	22	24	Ω
POWER CONSUMPTION					
VDD	Default parameters	6.39	6.62	6.78	mA
VDD_BUFF	Default parameters	19.6	29.41	33.38	mA
INPUT SIGNAL					
HIGH GAIN LINEARITY					
Input range	Default parameters	0.5	-	1	mA peak
Linearity error	Default parameters	-	$\leq \pm 5$	-	%
LOW GAIN LINEARITY					
Input range	Default parameters	0.5	-	8	mA peak
Linearity error	Default parameters	-	$\leq \pm 5$	-	%
SIPM VOLTAGE CONTROL					
V_{off}	Default parameters	0.25	-	1.25	V

Table 1: Specifications summary

DEFAULT PARAMETERS

Default polarization conditions are summarized in next table.

Parameter	Value	Function
VDD	3.3V	Power supply
VDD_BUFF	3.3V	Power supply for output buffers
I_{ref}	-7μA	Reference current for bandgap
I_{bias_in}	12 μA	Input amplifier bias current
I_{bias_fb}	30 μA	Feedback amplifier bias current
I_{bias}	-21 μA	Input amplifier bias current for mirrors control
I_{ref_se}	-900 μA	Output buffers bias current
I_{ref_cas}	300 μA	Output buffers cascode current
V_{CM}	1.5V	Common mode voltage for buffers output
V_{lim}	1V	Voltage control of High Gain saturation
V_{off}	1V	Common mode voltage at input node
I_{ref_disc}	300μA	Discriminator threshold

Table 2: Default parameters

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating
V_{DD}	3.2 to 3.4 V
V_{DD_BUF}	3.2 to 3.4 V
Temperature Range	
Operatingjunction	-40°C to 125°C
Storage	-65°C to 150°C
Soldering Conditions	JEDEC J-STD-020

Table 3: Absoulte maximum ratings summary

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Boundary Condition

θ_{JA} is measured using natural convection on JEDEC 4-layer board, and the exposed pad is soldered to the printed circuit board (PCB) with thermal vias. Due to the exposed pad different thermal resistance may be extracted from top or bottom of the packaging.

Package type	θ_{JA}	Unit
32-Lead QFN top	7 TBC[1]	°C/W
32-Lead WFN bottom	1 TBC[1]	°C/W

[1] To be confirmed

Table 4: Thermal Resistance

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PINS CONFIGURATION AND DESCRIPTION

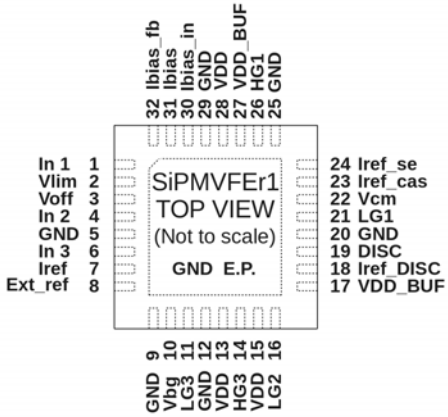


Figure 3: Pin configuration (Top view)

Pin No.	Mnemonic	Type	Description
13,15,28	VDD	Power	Analog power supply
17,27	VDD_BUF	Power	Buffer power supply
5,9,12,20,25,29	GND	Power	Ground
1,4,6	IN	Signal	Channel Input
2	Vlim	Input	Control of High Gain saturation
3	Voff	Input	Control of DC voltage at input node
7	Iref	Input	Bandgap reference current
8	Ext_ref	Input	External voltage reference
10	Vbg	Output	Bangap output
11	LG3	Output	Low Gain channel 3 output
14	HG3	Output	High Gain channel 3 output
16	LG2	Output	Low Gain channel 2 output
18	Iref_DISC	Input	Discriminator comparator current
19	DISC	Output	Discriminator digital output
21	LG1	Output	Low Gain channel 1 output
22	Vcm	Input	Common mode control of output buffers
23	Iref_cas	Input	Output buffers cascode current
24	Iref_se	Input	Output buffers bias current
26	HG1	Output	High Hain channel 1 output
30	Ibias_in	Input	Input amplifier bias current
31	Ibias	Input	Input stage bias current
32	Ibias_fb	Input	Feedback amplifier bias current
EP	GND	Power	Ground

Table 5: Pin function descriptions

BANDWIDTH

Bandwidth of High Gain path and Low Gain path is measured using the setup in figure 4 with a Rhode & Schwarz spectrum analyzer. It is compared to simulations (*_Sim) and extracted layout simulations (*_Ext) in figures 5 and 6. As expected it's around 350MHz and 250MHz for HG and LG respectively.

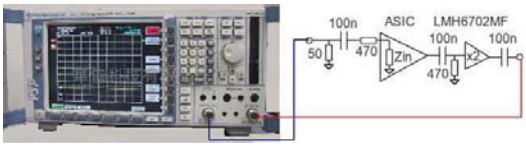


Figure 4: Bandwidth measurement setup

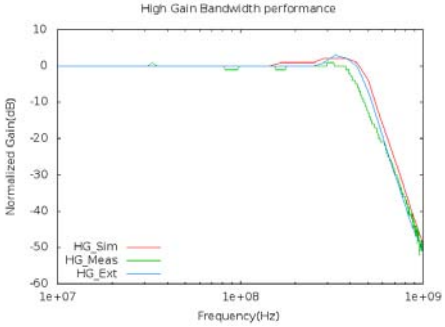


Figure 5: High Gain path Bandwidth measurement

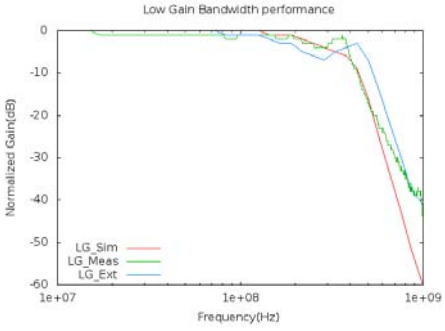


Figure 6: Low Gain path Bandwidth measurement

BANDGAP

A Bandgap reference circuit has been included in current design. It's output is directly connected at the output pin V_{bg} pin and it's directly connected to channel 1 and 2 biasing circuits. Channel 3 can be connected either to the output of this reference or to an external reference using the Ext_{ref} pin. The output measurement of the Bandgap reference is depicted in figure 7, the variation with temperature agrees perfectly with simulations although it's absolute value is a little bit different (probably due to some process variation).

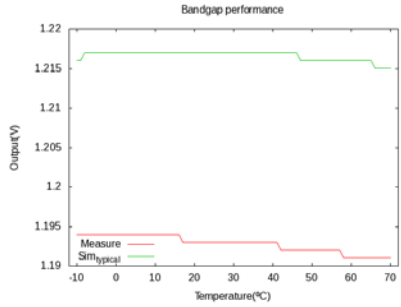


Figure 7: Bandgap voltage variation with temperature

Power Supply Rejection Ratio (PSRR) in AC and DC is also measured in figures 8 and 9 and results as expected.

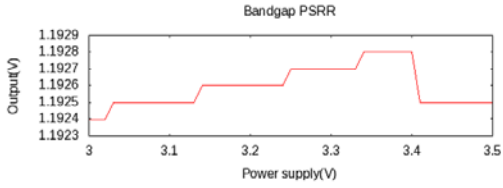


Figure 8: Bandgap PSRR

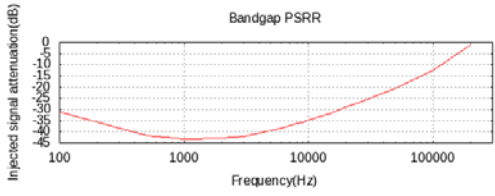


Figure 9: Bandgap PSRR in AC

TEST SYSYTEM

The test system consists in a signal injection circuit to simulate the SiPM shape. This signal is generated using an Arbitrary Waveform Generator (AWG). The output of the generator has a fixed amplitude and is attenuated using a programmable attenuator, permitting a better linearity injection of signal. The output of the ASIC is readout using a standard oscilloscope. Some programmable DACs and current sources are in the test PCB and controlled using a USB connection to an FPGA. The whole setup can be seen in figure 10.

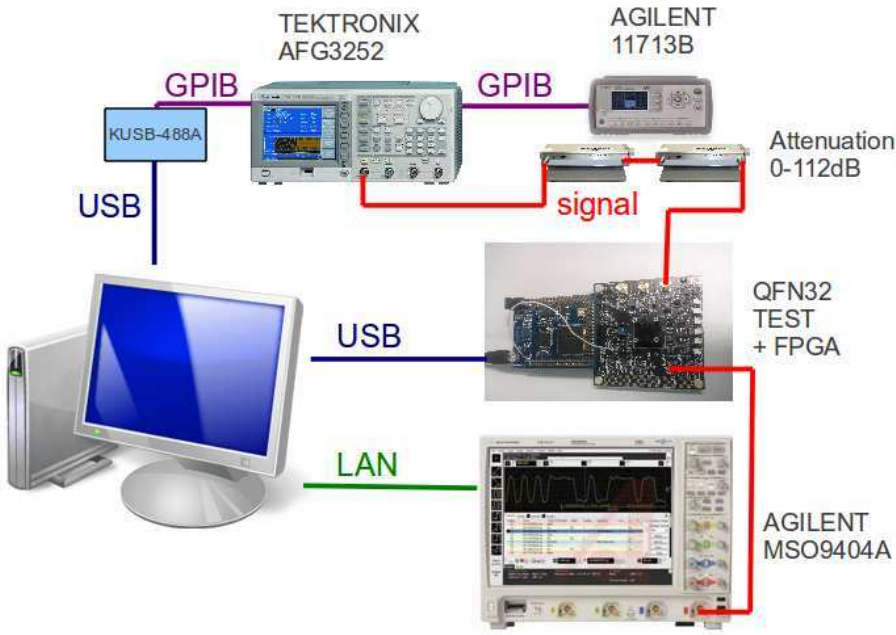


Figure 10: Test system

The ASIC is placed inside a QFN32 test socket to permit the exchange between different prototypes. Using this test setup several measurements have been performed including linearity, noise and jitter.

LINEARITY

For the linearity measurement the system is calibrated and the peak output signal is measured. The resulting plot can be seen in figure 11. As expected HG (around 1mA) path saturates more early than LG (around 8mA).

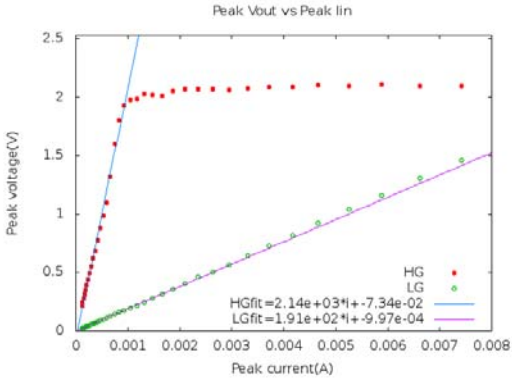


Figure 11: Linearity measurement

JITTER

Jitter is measured as the delay variation between the trigger signal from the generator and the output of the discriminator. This jitter will depend on the threshold value used for the comparator. A plot of the variation of the jitter measurement depending on the threshold value is plotted in figure 12

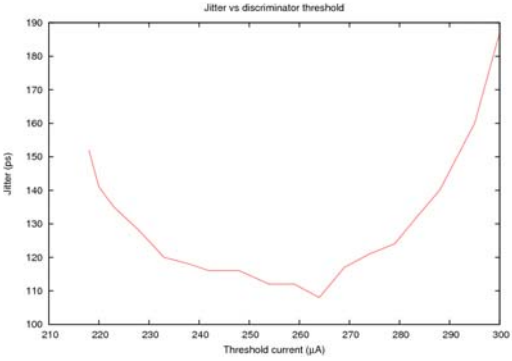


Figure 12: Jitter measurement

INPUT CAPACITANCE EFFECT

The input capacitance will affect the noise behaviour of the system thus the resulting jitter. A measurement with a few points can be compared with simulations in table

Cin	Simulation	Measure
0pF	15ps	8ps
33pF	32ps	33ps
100pF	84ps	93ps

Table 6: Jitter variation with input capacitance

NOISE

Noise is measured indirectly using the S-curve of the discriminator. Changing the threshold and calculating the area of the transition. A measurement can be observed in figure 13.

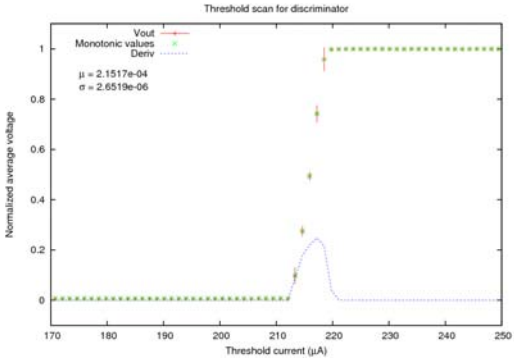


Figure 13: Noise measurement

INPUT CAPACITANCE EFFECT

Repeating the noise measurement for different input capacitance, we can observe how noise increases with capacitance as expected. A summary of the measurements can be seen in figure 14.

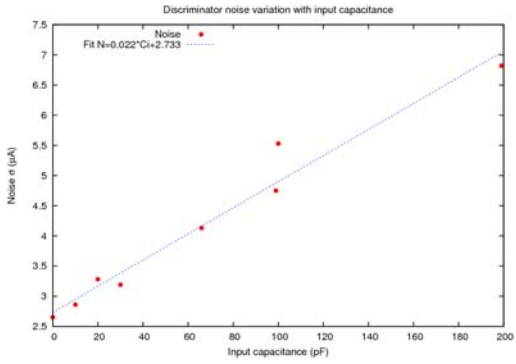


Figure 14: Noise variation with input capacitance

HG SATURATION CONTROL

The saturation point of the High Gain signal path can be tuned using the external V_{lim} control voltage. The resulting measurement is summarized in figure 15.

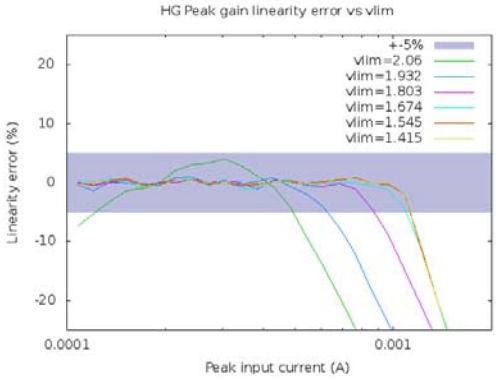


Figure 15: Saturation control of High Gain

SIPM VOLTAGE CONTROL

The DC voltage of the input node can be controlled externally using the V_{off} pin. A measurement of the linearity error on the HG with the variation of this voltage is performed and summarized in figure 16. The permitted variation range is around 1V as expected.

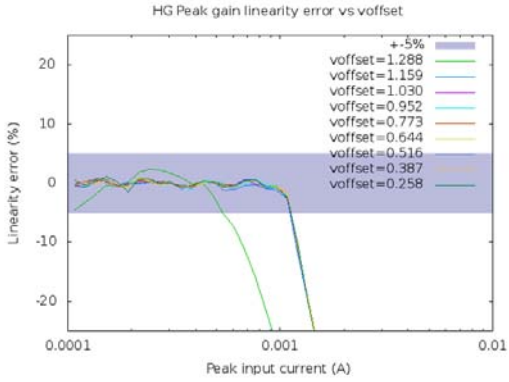


Figure 16: V_{off} variation effect in High Gain

LAYOUT

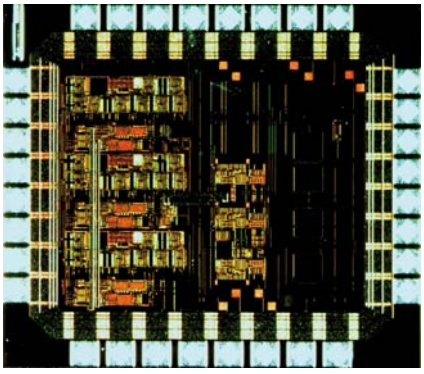


Figure 17: SiPMVFEr1 layout, $\approx$ 2x2mm , 4mm^2 die

BONDING DIAGRAM

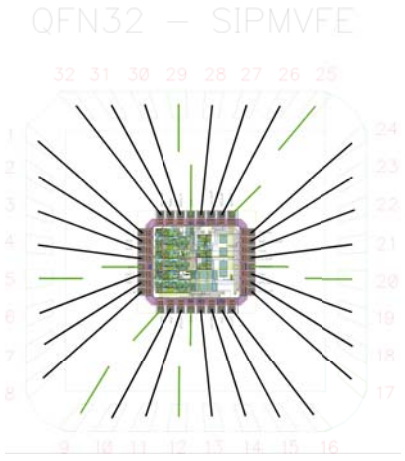
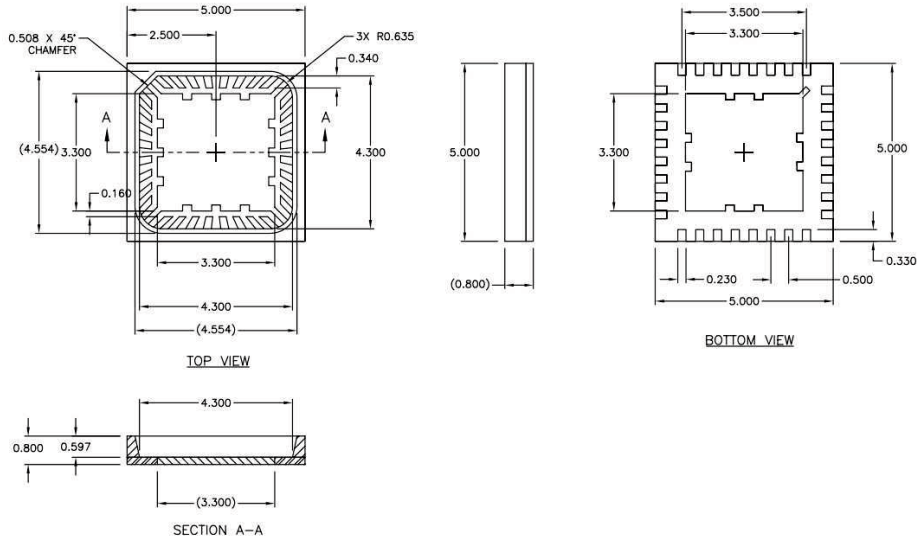


Figure 18: SiPMVFEr1 bonding diagram with downbonds to the cavity/exposed pad

OUTLINE DIMENSIONS



NOTES:
1. BODY: PLASTIC, SEMICONDUCTOR GRADE.
3. LEAD FRAME: COPPER, 194 FH.
4. LEAD FINISH: FULL GOLD PLATE.
5. FRAME THICKNESS: 0.2030 ±.0076.
6. DIE PAD: 3.300mm X 3.300mm.
7. JEDEC OUTLINE: MO–220 (VHHD–4).

Figure 19: Packaging outline

Packaging provided by SEMPAC, INC.

ORDERING IFORMATION

Model	Temperature Range[1]	Package Description[2,3]
SiPMVFEr1	-40°C to 125°C	32 Lead QFN

[1] Temperature range from the ASIC technology used. To be tested.
[2] Package dimensions without lid 9 x 9 mm, 0.8 mm thick.
[3] Lid dimensions 9 x 9 mm, 0.2 mm thick.

NOTES

Institut de Ciències del Cosmos

B

PACIFICr1 Datasheet

PACIFICr1 SiPM preamplifier block design for SciFi detector

Data Sheet PACIFICr1

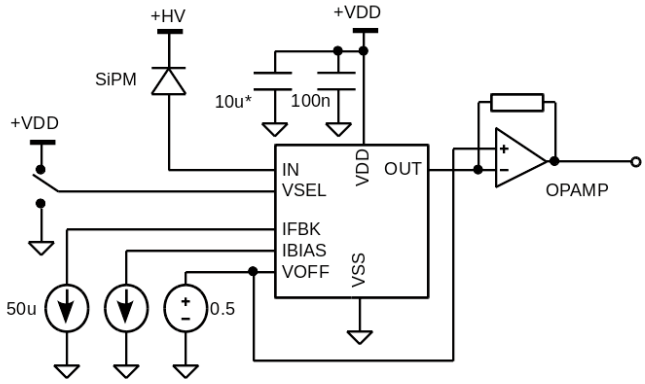
FEATURES

Current mode input.
Low input impedance (≈34Ω).
Zero components interface between sensor and device.
High Bandwidth preamplifier (≈400MHz).
Relative linearity error ±5%.
Small pitch of 40μm height.
Extended range in DC input voltage.
Low Power consumption (≈2mW/channel).
Low Noise 3.3μA rms integrated noise until 300MHz.

DESCRIPTION

PACIFICr1 is a single channel Silicon Photo Multiplier readout circuit with current mode input and analog output.
PACIFICr1 has been developed using International Business Machines Corporation (IBM) 0.13 μm technology through CERN.
PACIFICr1 is available without package and will need of wire bonding for testing.

TYPICAL APPLICATION CIRCUIT



*Due to high current consumption transients for input signals in the range of mA, a 10uF capacitor should be placed close to the power pins.

Figure 1: Typical application schematic

APPLICATION

Readout of Silicon Photo Multipliers arrays.

Av. Diagonal 645, Barcelona, ES08028, SPAIN
Tel. 934021587 http://icc.ub.edu
Fax. 934037063

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REVISION HISTORY

05/13 - First version A

FUNCTIONAL BLOCK DIAGRAM

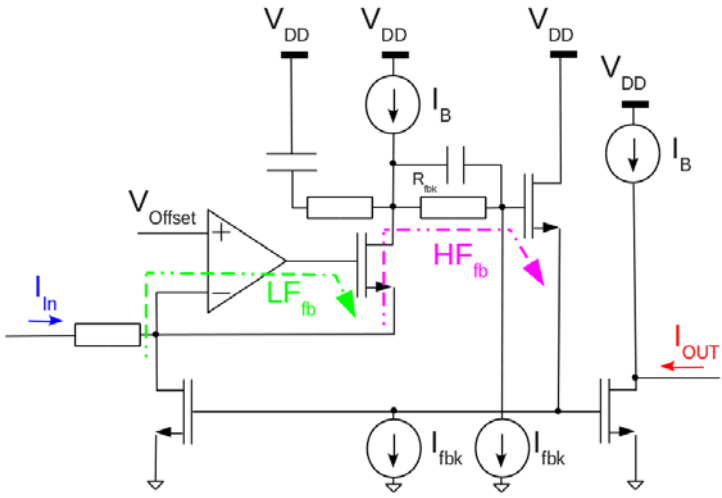

Figure 2: Channel block diagram

The input stage uses a novel approach of double feedback. Detailed schematics can be observed in figure 2. It provides a low input impedance in order to avoid affecting timing behaviour of the SiPM and increase input current. HF_{FB} is the high frequency feedback path that keeps this input impedance constant (in a certain frequency range). The second labelled path, LF_{FB} will provide the dc voltage (V_{offset} in figure) of the input node using the virtual short circuit in the amplifier that will drive a follower in a lower frequency range.

The design has been implemented taking into account that dominant pole should be set at the input node (SiPM parasitic capacitance is at the order of tenths of pF). In this way stability is not compromised when an important capacitance is added at the input.

In order to work at different supply voltages two resistor values of the high frequency path are available. This resistor can be switched using an external control pin.

SPECIFICATIONS

T_A=25°C

Parameter	Conditions	Min	Typ	Max	Unit
INPUT					
Z_{in}	Default input stage polarization currents		34		Ω
POWER CONSUMPTION					
I_{VDD}	1.2V and 1.5V power supply		1.6		mA
VOLTAGE ADJUST AT INPUT					
	1.2 V power supply	0.2	-	0.75	V
	1.5 V power supply	0.2	-	1.05	V
INPUT SIGNAL					
Input range		5	-	4000	μA peak
BANDWIDTH	15pF input capacitance (min) and 5pF (max)	340		540	MHz
NOISE	Integrated rms noise from 10Hz to 300MHz	3	3.2	4	μA

Table 1: Specifications summary

PINS CONFIGURATION AND DESCRIPTION

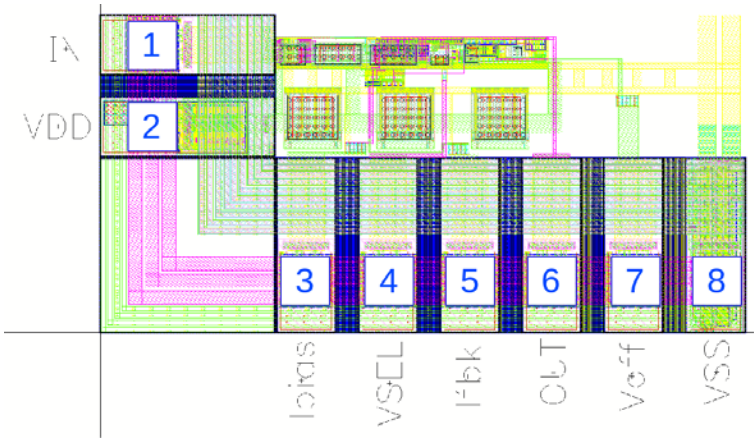

Figure 3: Pin configuration (Top view)

Table 2: Pin function descriptions

Pin No.	Mnemonic	Type	Description
1	In	Analog	Channel input
2	VDD	Power	Analog power supply
3	Ibias	Analog	Polarization current
4	VSEL	Digital In	Selection of operating voltage
5	Ifbk	Analog	Feedback polarization current
6	OUT	Analog	Analog Output
7	Voff	Analog	Offset voltage to input node
8	VSS	Power	Analog ground

OPERATING VOLTAGE SELECTION (VSEL)

In order to adapt to both 1.2V and 1.5V power supply keeping the desired dynamic range, an internal switch to change the resistor in the high frequency feedback path has been implemented (resistor R_{fbk} in figure 2). The connection is a pass gate (switch) connected in parallel to a resistor. This pin is called VSEL and follows next table operation;

VSEL	Switch	VDD
1.2	ON	1.2
0	OFF	1.5

Table 3: VSEL operation

With this configurable resistance the input stage behaves as expected in both operating conditions.

INPUT IMPEDANCE

Input impedance is kept low using the high frequency feedback loop. This kind of feedback loops present an inductive behaviour at high frequencies. The simulation can be observed in figure 4.

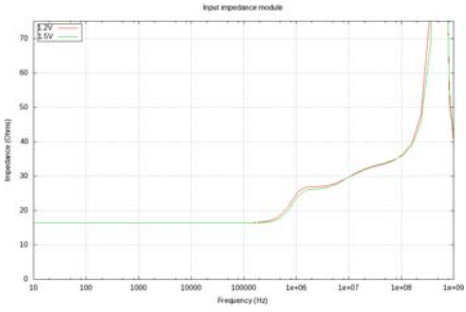

Figure 4: Input impedance for different VDD*

* Simulation does not include input inductance that will affect high frequency (over GHz) behaviour

The input impedance is kept to a low value corresponding to the resistance in series (16Ω) at the pre-amplifier input until around 100KHz. From this point increases slowly to reach a value of around 34Ω at 100MHz. Passed this frequency impedance increases fast reaching a value of 50Ω at around 250MHz.

VOLTAGE ADJUST RANGE

One key parameter is the option to adjust anode voltage of every device directly from the ASIC connection. That's the function of the low frequency feedback loop, but it's limited due to the voltage drop needed from the transistors. Special effort has been made to try to maximize this range (using LVT transistors and minimizing the number of transistors in series in the signal path). The final range of adjustment is around 0.55V for 1.2V power supply and around 0.85V for 1.5 power supply.

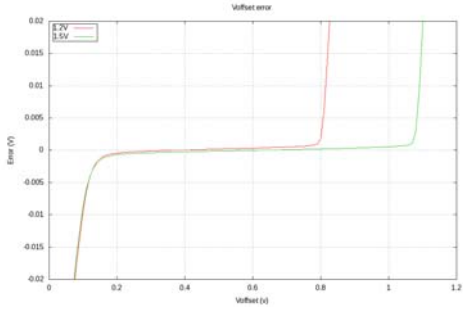

Figure 5: Voffset adjustment error for different VDD

CURRENT REFERENCES IFBK AND IBIAS

In order to flexibly test the behaviour of the pre-amplifier two polarization current references have been taken to external pins. This way the modification of the parameters respect this currents can be observed. General input stage current reference (I_{bias}) and feedback current (I_{fbk}) are in different inputs to control independently the behaviour of the feedback loop and input stage. The default value of all bias currents is 50μA to ground.

NOISE

Integrated noise from 10Hz to 300MHz (the range affecting the shape of input signal) should be smaller than 5μA. Typical simulations in the worst case (1.5VDD) show an expected value of around 3μA.

LINEARITY

According to simulations linearity is better than ±5% in either configurations in full range. In figure 6 some input / output signals can be observed with the corresponding linearity error on the full range.

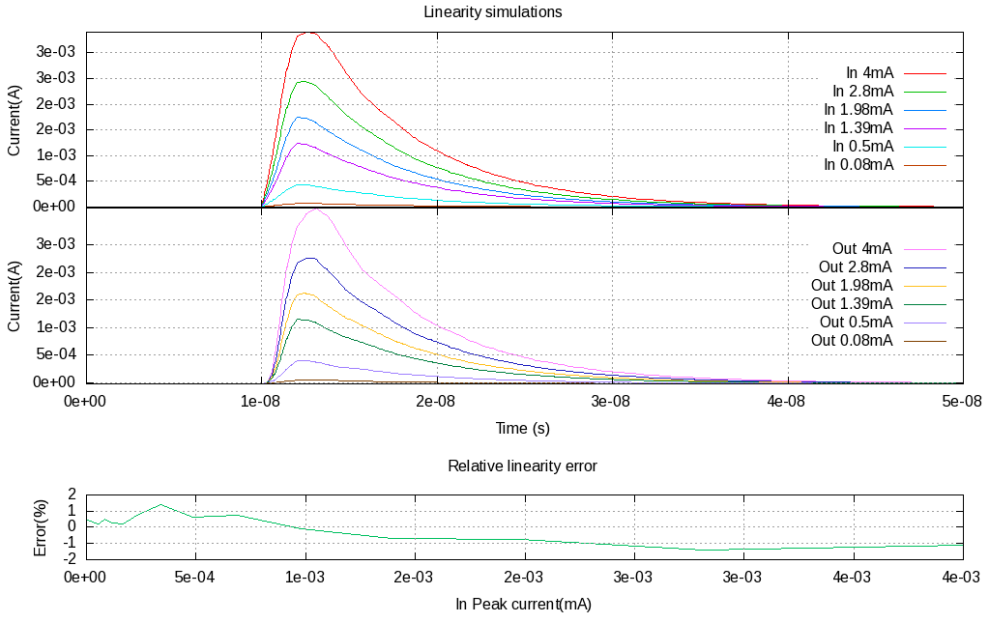

Figure 6: Linearity simulation

DC GAIN

DC gain is expected to be equal to 1 since current mirrors have the same dimensions. When this DC gain starts to decrease a worse linearity is obtained. A simulation on DC gain for the various operating voltages can be observed in figure 7.

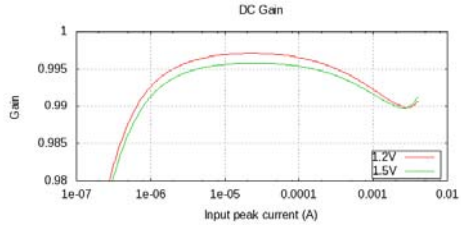

Figure 7: DC gain simulation

BANDWIDTH

Input node voltage control is slow in comparison to input impedance control. This feedback structure transfer function can be observed in figure 8. Comparing two cases of input capacitance (determined by sensor), as input impedance is increased bandwidth is reduced as expected.

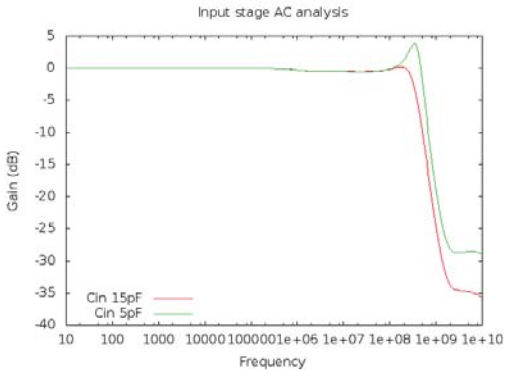

Figure 8: Input stage bandwidth

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating
V_{DD}	1.2 to 1.5 V
Temperature Range	
Operatingjunction	-40°C to 125°C
Storage	-65°C to 150°C
Soldering Conditions	To Be Determined

Table 4: Absoulte maximum ratings summary

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

LAYOUT

The layout of the channel have been optimized to use staggered input pad's on the ASIC. This leads to a maximum of 40μm pitch between channel.

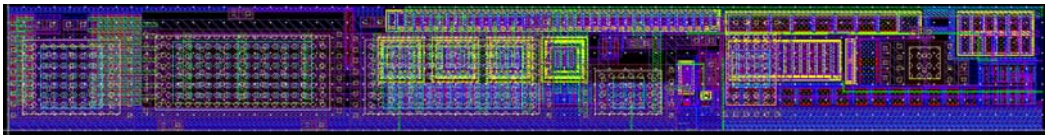

Figure 9: PACIFICr1 channel layout, 335μm x 40μm

BONDING DIAGRAM

To Be Determined

NOTES