UNIVERSITAT DE BARCELONA

Departament d'Electrònica

ANALYSIS OF INTEGRATED TRANSFORMERS AND ITS APPLICATION TO RFIC DESIGN

Tesi doctoral presentada per a l'obtenció del títol de doctor Enginyer en Electrònica

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En José M. López Villegas, Professor Titular de la Facultat de Física de la Universitat de Barcelona,

CERTIFICA:

que la memòria "*Analysis of Integrated Transformers and its Application to RFIC Design*", que presenta en Josep Cabanillas Costa per optar al grau de Doctor en Enginyeria Electrònica, s'ha realitzat sota la seva direcció.

Dr. José M. López Villegas Josep Cabanillas Costa

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Acknowledgments

Four years later, here we are. It has been a longtime since my advisor offered me the chance of pursuing a Ph.D. During this time, I asked myself several times why I decided to start and continue it. Research work is always interesting and attractive but it is also plenty of uncertainties: by definition you do not know where you will end up and the results you will get (but, this is exciting and challenging !!!!, isn't it?). Unfortunately, there are other uncertainties non-intrinsic to the Research you have to deal with (usually a low salary and its consequences, and sometimes time constants too long for a 4 year carriere). However, I suppose that Research is mainly a vocation (rather than a job) and you are ready to sacrifice or postpone some stuff in order to satisfy your curiosity and interests. In life, as in many problems in engineering, you have to find the better possible combination of tradeoffs for each particular situation/moment.

I must admit that sometimes it was hard to deal with these uncertainties of the student research life (even in spite of being a very convinced Ph.D. student). But the affection of your family and friends helps to overcome these bad (and few) moments. I know that it was also 'hard' for my parents. It is still difficult for me to explain to them what I did during my thesis and all the profits and good experiences I had during this time. Instead, they have seen a lot of work without an apparent reward other than a personal satisfaction. Despite, they always kept supporting and encouraging any decision I took. Now, it is done!!! and I specially want to dedicate this thesis to them. Thanks for your love, generosity and patience. Also to my sister and brother, who deserve a special recognition for everything they have generously and patiently managed in my absence all these years.

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And of course, let me finish (this is getting too long) by thanking Merce Deumal (Javier's wife) and Raimon Rubires for their friendship and support.

INTRODUCTION

1. Wireless World. Long and short range communications

The radio frequency and wireless market has suddenly expanded to unimaginable dimensions. Cellular phones, once considered yuppie toys or exotic extravagances have become indispensable items in our lives and work. Actually, by the time 2004 rolls by, there will be one billion mobile phone subscribers worldwide. Industry observers predict that by then the wireless phone population will equal –or exceed- that of wired phones [1], pointing out the fast penetration of the wireless technology in our society; much faster than other technologic advances such as the television or the wired phone.

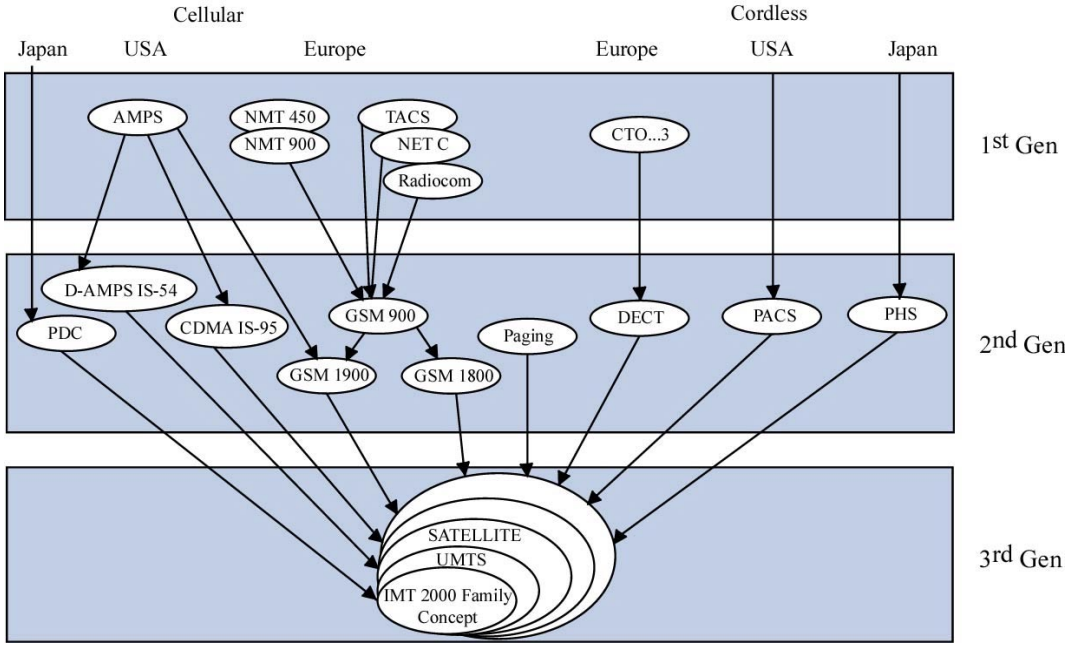

Figure 1. Evolution to the Third Generation[1]

[1]Data extracted from "Migration Paths 2G to 3G.Planning the Evolution to IMT 2000" by W. Groenen at ITU-D Seminar on IMT 2000, Warsaw, October 2001.

Nowadays, the second generation of mobile systems is consolidated. The GSM (Global System for Mobile Communications), probably the most successful 2G standard, provides digital wireless services (mainly digital telephony but also facsimile) to more than 721 million subscribers (end June 2002), accounting for approximately 71% of the wireless digital market today [2]. However, the existence of different standards in the USA, Japan and Europe as well as the low transmission data rate available (9.6 Kbits/s for GSM) suggest the need to evolve to a worldwide high-performance standard (UMTS, Universal) in the bosom of third generation of mobile communication systems (3G). The goal of this third generation is to deliver multimedia services to the user in the mobile domain. Thus, UMTS users will be provided with data rates up to 144 Kbits/s, 384 Kbits/s and 2 Mbits/s in macrocellular, microcellular and indoor environments respectively, enabling services such as real-time video (video-conferencing or video-telephony), mobile entertainment, etc [3].

Due to the endless possibilities of the UMTS and the enormous expectation seeded around it, the difficulties of the implementation of this technology were under-estimated and the initial planning for its progressive introduction had to be modified. At this time, Asian operators (Japan) are testing the waters with the first commercial 3G networks. In the United States, operators are still migrating away from TDMA technology as long as the European operators, struggling with high debt loads and a subscriber base nearing saturation, have postponed the introduction of the first UMTS services to the year 2003. However, in spite of the difficulties of the current situation, UMTS seems to be "inevitable" in the next future.

Along with mobile phones or pagers, where the distance between the emitter and the receiver can be very large, different applications with a much shorter range have also appeared. Between these short-range applications market, the wireless LAN's (WLAN) industry should be highlighted as one of the fastest-growing segments of the communication industry. Experts foresee the WLAN industry growing from the $1.1 billion of 2000 to 5.2 billion by 2005, with significant growth beyond that [4]. Although, different standards for WLAN still exist in the marketplace, industry has converged on the standards sanctioned by the Wireless Ethernet Compatibility Alliance (WECA) based on the standard created by the 802.11 committee of the IEEE. These standards use modulations based on frequency-hopping spread spectrum around 2.4

GHz (Wi-Fi or IEEE802.11a) and 5 GHz (IEEE802.11a or HiperLAN2) with transmission speeds of 11 Mbps.

Another standard also intended for short-range communications (10-100m), is known as Bluetooth (named after Harald Blaatand "Bluetooth", king of Denmark 940-981). Invented by LM Ericsson in 1994 and followed by more than 1900 companies around the World (including Nokia, IBM, Intel, Motorola, Lucent, etc.), it operates in the unlicensed 2.4 GHz ISM band and allows transmission speeds of 780 Kbs/s [5,6]. Bluetooth attempts to provide a low cost (estimated around 5$) method for short-range data communication between computers and their peripherals (file transfer, printing), but can also be useful for industrial automation or in domotic applications (heating or Hi-Fi systems, smart appliances, etc). Bluetooth is supposed to become a key technology as soon as very low cost transceivers are available.

2. The Integrated RF Design. The RF Front-end

With this spectacular popularity of wireless communications (closely related to the advances in the IC technologies) and the increasing demand on communication portable systems of small size, low power, low cost and high performance, wireless architectures and circuit techniques have experienced a renaissance in the last decade. Once (and not so long ago), radio circuits were thought to be incompatible with the Silicon IC technologies, due to two main reasons:

1) The heavy reliance of RF integrated circuits (RFIC's) on tuned circuits and discrete filters (apparently, not suited to be integrated).
2) The limited bandwidth of the Silicon technologies.

Thus, for many decades the "RFIC" design was restricted to the GaAs technologies, due to the wide bandwidth of the MESFET GaAs transistors and to the high quality of the passive components. Inductors with relative high quality factors were affordable thanks to the insulating properties of the substrate and to the Au interconnections used typically in GaAs technologies [7,8]. This situation lasted until early 90's.

Then, as a result of technological improvements that increased noticeably the bipolar and specially the MOS transistors bandwidth (cut-off frequencies well above 30 and 50 GHz are found for CMOS and bipolar SiGe technologies respectively), the interest of Silicon integrated passive components was renewed. In 1990 Nguyen et al. published experimental measurements on integrated LC filters and inductors [9,10]. The quality factors reported ranged from 3 to 8, at frequencies above 1 GHz. Since then, huge efforts have been dedicated to improving the performance of the integrated inductors, resulting in quality factors close to 20 for bipolar processes using thick metal layers. Although these quality factors are still too low for some specific functions (as image or channel filters, or high Q resonators), they can be considered good enough for many other applications and as a consequence, can be included on-chip reducing the number of external components.

This relative youth of the RFIC design may help to explain that although today's pocket phones contain more than one million transistors (with only a very small fraction, often in the order of hundreds, operating in the RF range), the RF section is still the bottleneck of the complete system. In many applications, the front-end is still responsible for more than half of the power dissipation or the circuit area. Moreover, one of the largest and most expensive components in portable systems is often the battery. Since the total power consumption is dominated by the radio rather than by the digital circuits, the RF front-end also impacts the size and cost of the system through the battery size.

The difficulties involved in the RFIC design at current state-of-art may be summarized in three main categories:

1. **Technology related**. Digital circuits benefit directly from advances (scaling) in IC technologies since they can be translated almost directly to a newer process with the following reduction of the power consumption and area. Unfortunately, RF (analog) circuits involve many more design trade-offs in terms of gain, linearity, noise, power, etc (compared to the common trade-off speed-power consumption found in digital design) and hence do not benefit as much of the reduction of the transistor dimensions. Moreover, the large area of the passive components (mainly inductors) may prevent the area reduction associated to the technology scaling if they are included on a chip. Also,

the cross-talk across the substrate between the high speed digital circuits and the high-sensitive RF circuits represents an important challenge.

2. **Design tools related**. CAD tools for RF circuits are still in their infancy when compared with digital design tools, forcing the designer to rely on experience and intuition to predict the circuit performance. This increases the number of design cycles (design-fabrication-test) needed to obtain an optimum design. Related to the previous item, many digital processes are not accurately characterized for analog design. Thus, digital models can cause inaccuracies in the simulation results when the noise or non-linear characteristics of the designed circuit have to be predicted.

3. **System related**. RFIC design is a multi-disciplinar field that demands a solid understanding of many areas that are not related to integrated circuits such as microwave theory, communication theory, analog and digital modulation, transceivers architecture, etc. By example, the design of an LNA, a mixer or a PA depends strongly on the architecture in which it will be embedded and the type of modulation used. However, it is difficult for an IC designer to acquire the necessary knowledge of these disciplines in a short time. Therefore, traditional wireless system design has been performed at somewhat disjointed levels of abstraction: communication theoreticians create the modulation scheme and base-band signal processing, RF systems experts plan the transceiver architecture and IC designers develop the building blocks. In order to obtain an optimum system, it is essential the interaction and feedback between these different levels.

In spite of the previous difficulties, an amazing progress has already been done towards the single-chip integration of the RF transceiver. Nevertheless, the ultimate goal of the Software Radio is still far [11]. In the Software Radio, the A/D conversion would take place at the carrier frequency, and from that moment on, any signal processing would be carried out at the digital level. The main advantage of this architecture would be its reconfiguration capability via software. Thus, the same equipment could work either as a cell phone using different bands and standards.

Nowadays, the requirements on the A/D converter (17-20 bits of resolution for 100dB dynamic range and 10 Gsamples/s sampling speed) and on the DSP speed (more than 10 GIPS) prevent the accomplishment of such an ideal architecture in the next future and

make it just a dream. However, the idea of moving the A/D closer to the antenna seems very promising.

A much plausible goal in the short term consists in the integration on a single-chip of the transceiver and, specially, of the RF front-end, the part of the system responsible for providing gain (to convert weak signals to convenient amplitude levels for further processing) and frequency conversion. Figure 2 shows the typical structure of a RF front-end based on a direct conversion architecture where the different building blocks (Low Noise Amplifier, Mixer, Voltage-Controlled Oscillator, and Power Amplifier) can be identified.

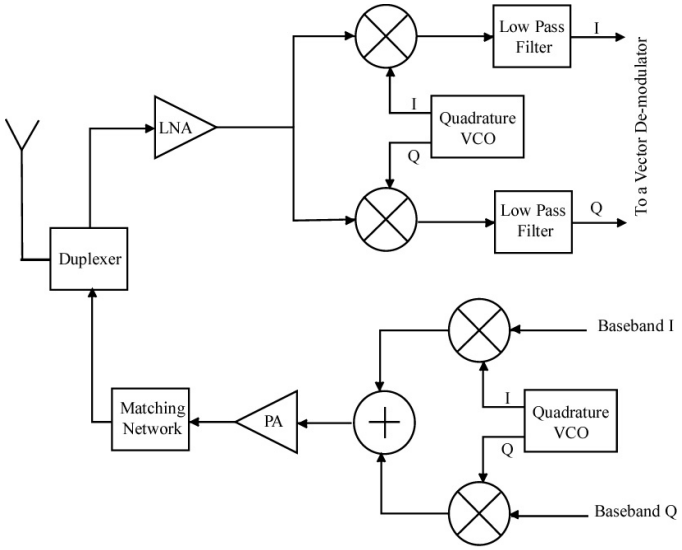

Figure 2. Direct Conversion RF Front-end

Between these blocks, integrated CMOS LNA's [12,13,14] and mixers [15,16,17] with a good performance have already been reported and can be considered state-of-the-art. Conversely, the integration in CMOS processes of high performance VCO's and PA's able to satisfy the tight requirements imposed by the communication standards show considerable difficulties and is topic of active research.

The fully integrated oscillators (and not exclusively CMOS) suffer from the relatively low quality factor of the integrated resonators, and in particular of integrated inductors, that limit the oscillator phase noise performance. A minor drawback, but also important, in the integration of VCO's consists in their limited tunning range.

The main difficulties associated to the PA are related to the high value of voltage needed to deliver a power in the order of watts to a 50Ω antenna while operating with low voltage supplies. Thus, due to the higher product of the cuttoff frequency and the breakdown voltage as well as to the high mobility and the high quality factor inductors, the power amplifiers still rely on the III-V technologies, particularly GaAs MESFETS and heterojunction bipolar transistors. However, recently SiGe technologies have also become an interesting alternative to the GaAs [18]. Unfortunately, it is not clear if submicron CMOS processes can achieve a similar performance, and at the moment, they are used basically for short-range applications or as pre-amplifiers [19].

Due to the intensive use of digital signal processing in modern transceivers as well as to the convenience of adding digital blocks into the front-end for frequency synthesis, adaptability, multi-mode operation and sophisticated detection, a single-chip solution has to be implemented using a CMOS technology or any of its variants (such as the Silicon-on-Insulator (SOI) CMOS, BiCMOS or the SiGe BiCMOS). This raises questions such as how well digital CMOS circuits can co-exist on the same substrate as the radio front-end, or whether there is sufficient on-chip isolation in a low cost package to guarantee stable operation of a receiver with more than 100 dB of base-band gain, or how the power amplifier modulates the on-chip local oscillator. The future of single chip CMOS transceivers may well depend on the satisfactory answers to these questions, and will demand technological improvements along with circuit and architecture design techniques that take advantage of the strengths of CMOS, and circumvent its weakness. Next section is dedicated to the direct conversion architecture that nowadays is playing a key role in the way towards this integration.

3. RF Architectures. Direct Conversion

In the previous section, we have mentioned the different levels of abstraction involved in the RFIC design. Thus, parameters as the gain, the noise figure or the third-order intercept point used at the circuit level to specify the properties of different building blocks of a RF front-end, increase their meaning when considered in a higher abstraction level, that is, the system level.

Let us illustrate this situation with an example: connect in cascade a LNA and a matched mixer characterized by their respective noise figures NF_{LNA}, NF_{mix} and gains A_{LNA}, A_{mix}. The resulting noise figure for the cascaded system NF_{tot} is given by:

$$NF_{tot} = NF_{LNA} + \frac{NF_{mix} - 1}{A_{LNA}^2}$$

This expression shows that the resulting noise figure depends mainly on the LNA noise figure for the common values of gain found in LNA's. A reversed expression would be found if the mixer and the LNA interchange their positions, pointing out that the properties of the system depend strongly not just on the specific properties of its building blocks but also on their proper connectivity, that is, on the system architecture.

Complexity, cost, power dissipation and the number of external components have been the primary criteria in selecting the transceiver architecture. However, as the IC technologies evolve embracing more parts of RF systems, the relative importance of each of these criteria changes, and transceiver architectures as the direct conversion architecture that once seemed impractical may return as plausible solutions.

The direct conversion or homodyne architecture, invented many decades ago, has recently become the topic of active research again [20,21,22]. In spite of being the natural or intuitive approach for the receiver architecture, its implementation was tried many times, and failed almost every time, justifying thus the omnipresence in the practical implementations of the super-heterodyne receivers. Nowadays, several reasons account for this renewed interest:

1. Direct conversion, in principle, lends itself to monolithic integration much more easily than do heterodyne receivers and would result in systems with smaller size, weight and power consumption.
2. Direct conversion past failures were due primarily to effects (offsets, mismatches, etc) that could not be removed in discrete implementations, but may be controlled or suppressed in integrated circuits.

In order to appreciate why DCR's are amenable for integrated implementations, let us briefly review the heterodyne receiver shown in fig.3a where the RF input signal is firstly amplified by a low-noise amplifier and subsequently filtered by an image reject

filter [20]. The result is then mixed with a local oscillator, producing the intermediate frequency IF signal where the out-of-channel interferers are suppressed by the IF filter.

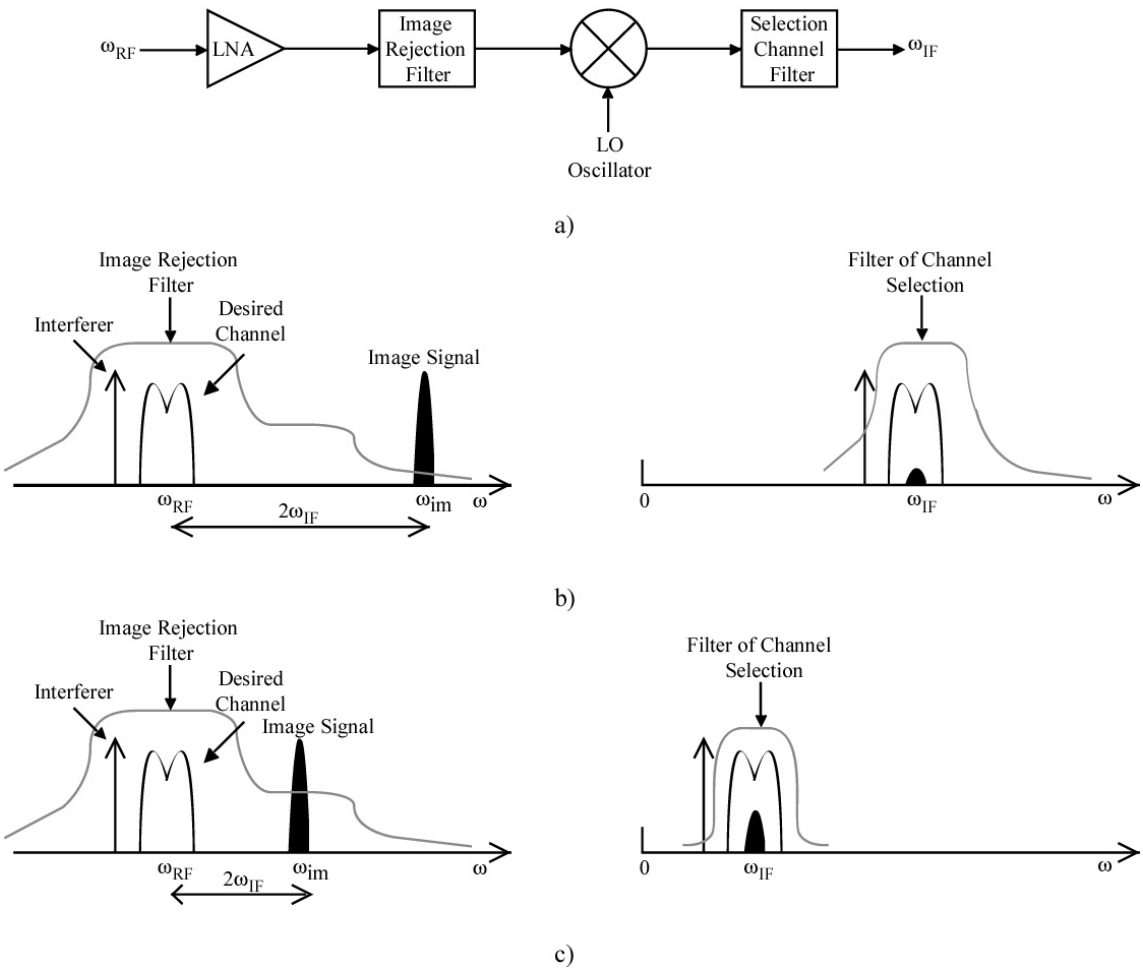

Figure 3. a) The super-heterodyne receiver. b) High IF frequencies favours the rejection of the image frequency c) Low IF frequencies favours the rejection of near interferers

The main issue in the heterodyne architecture consists in the trade-off between adjacent channel suppression and image rejection. Thus, taking into account that Q relates the filter bandwidth Δf with its central frequency f_c, $Q = \frac{f_c}{\Delta f}$, the lower is the IF frequency, the most suppressed are the interferers (if a constant quality factor is assumed for the channel filter). However, lowering the IF frequency results in a significant corruption of the down-converted signal associated to the frequency image. Conversely, if the IF is high, the image is greatly attenuated whereas nearby interferers remain at significant levels, as shown in fig. 3c. For this reason, both the image rejection filter and the IF channel filter require highly selective transfer functions that are impractical in today's

IC technologies. The solution has been to employ external bulky filters such as surface acoustic wave (SAW) devices, limiting seriously the integration of the receiver.

Another drawback of heterodyne receivers is that the LNA must drive a 50 ohms load because the image rejection filter is placed off chip. This adds an additional constraint to the LNA design and establishes another dimension to the trade-offs among noise, linearity, gain and power dissipation of the amplifier.

Direct conversion receivers translate the band of interest directly to zero frequency (that is why they are also called zero-IF receivers), circumventing the problem of the image frequency and removing the necessity of the IF SAW filters. Instead, the nearby interferers are suppressed using low pass high-order active filters and base-band amplifiers that are amenable of monolithic integration and have very low power consumption since they operate at very low frequencies. Moreover, the LNA does not need to drive a 50 ohms load, because no image filter is required.

The direct conversion architecture requires quadrature channels (I-Q) for vector modulation and demodulation since each sideband of the RF spectrum contains different information and would result in irreversible corruption if they overlap each other without being separated properly (as shown in fig. 2). Whereas in superheterodyne receivers, the quadrature down-conversion is performed at the second LO frequency, in direct conversion receivers this has to be done at the much higher carrier frequency. Thus, it is a great challenge to produce quadrature phases with good amplitude match at RF frequencies. In case of double-sideband signals no quadrature signals are needed and a simpler receiver can be used (fig.4). Nevertheless, double sideband modulations are not employed in practice due to their inefficient bandwidth use.

In spite of its apparent simplicity, direct conversion entails a number of issues that do not exist or are not serious in a heterodyne receiver and have prevented the proliferation of successful implementations [20]. Since in the direct conversion architecture the down-converted band extends to zero frequency, any dc offset voltages can corrupt the signal and, more importantly, saturate the following stages. To understand the origin and impact of these offsets, consider the simple receiver shown in fig.4 and let us analyze how the finite isolation of the mixer affects the performance of the receiver.

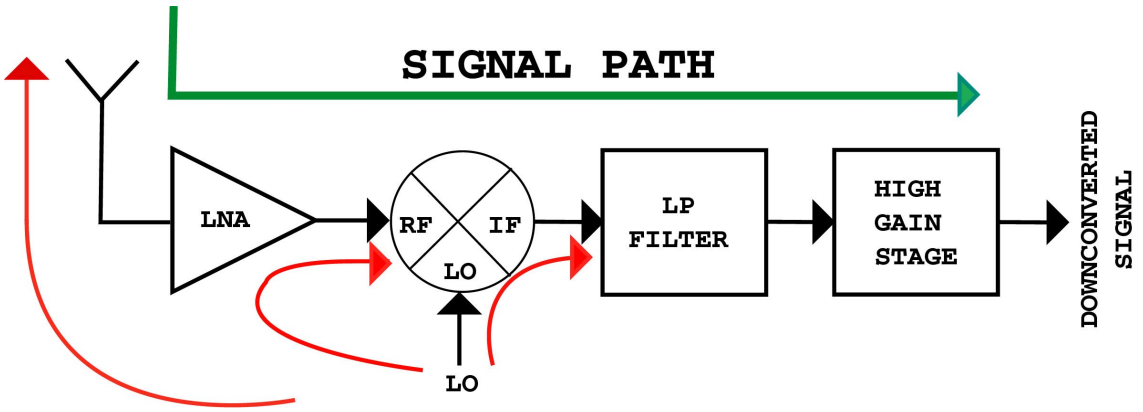

Figure 4. "Self-Mixing" and "LO leakage" in Direct Conversion Receivers

The isolation between the LO port and the inputs of the mixer and the LNA is not perfect (common values for the mixer LO-IF isolation are around 40 dB), i.e., a finite amount of feed-through exists from the LO port to the input and output of the LNA. Called "LO leakage" this effect arises from the capacitive and substrate coupling and, if the LO signal is provided externally, bond-wire coupling. Mixer mismatches are also responsible for this finite isolation. Then, the leakage signal appearing at the inputs of the LNA and the mixer is mixed with the LO signal, thus producing at the IF port a dc component that overlaps with the down-converted signal. This phenomenon is called self-mixing.

A similar effect occurs if a large interferer leaks from the LNA or the mixer input to the LO port and is multiplied by itself. The problem of offset is even exacerbated if the self-mixing varies with time, as it occurs if the leaked LO signal is radiated by the antenna and then reflected back to the receiver or in frequency hopping receivers. Different techniques as AC coupling, offset cancellation schemes or use modulations with negligible energy below few kilohertz can be applied to alleviate the offset problems [20,24,25].

Along with the dc offsets, the direct conversion architecture suffers from some additional drawbacks [26]:

1) I-Q accuracy. Phase and amplitude imbalances in the I-Q channels can corrupt the down-converted signal, thereby raising the bit error rate. The problem of the I-Q

mismatch has been a major obstacle in discrete designs, but it tends to decrease with higher levels of integration.

2) Even-order distortion. Typical RF receivers are susceptible only to odd-order inter-modulation effects, but in direct conversion receivers, even-order distortions become also problematic. Thus, if two strong interferers of frequencies ω_1 and ω_2 close to the channel of interest experience a second order nonlineariy (in the LNA or the mixer), a low frequency term ω_1-ω_2 will appear at the receiver output associated to the finite isolation and mismatches in the mixer.

3) Flicker noise. Due to the extremely low power of the RF signal, the down-converted signal is very small and quite sensitive to noise. Thus, the low frequency amplifiers have to be designed carefully to minimize the influence of flicker noise of the devices, especially in MOS implementations.

4) Local Leakage. Apart from creating serious offset problems, the LO signal may leak through the antenna in spite of the reverse isolation of the mixer and the LNA and generate in band interferences to other close receivers. The regulatory bodies and wireless standards limit the level of this LO leakage.

In spite of these drawbacks, direct conversion seems to be the most suitable solution in the next future for the implementation of portable, low power RF front-ends and some functional designs have been already reported [27].

4. Future trends

Despite a general optimistic landscape, we do still have many uncertainties in our way towards the fully integrated wireless systems. Although the SiGe and SOI technologies will be available, we can wonder ourselves if their cost will match the requirements of BiCMOS RF-Analog-Digital radio integration in the next few years? Are these or other technologies the right ones indeed? If we consider that the ultimate goal in the design of wireless systems would be to combine the RF front-end and the base-band processors in a single-chip low cost solution, many problems still remain to be solved (specially, for high performance applications):

1. The signal-to-noise ratio of the analog blocks can be degraded by the digital (noisy) parts due to the coupling via the substrate or the power lines.
2. Analog circuit and especially RF circuits have a lower yield than digital circuits due to the inevitable parametric variations, reducing the yield of a monolithic implementation of the overall system.
3. An important percentage of the area of the RF circuits (around 60%) is dedicated to passive components, mainly inductors. Unfortunately, the performance of these passive components built on a standard IC process is relatively low and have a direct effect on the system performance (power consumption, noise figure, phase-noise, etc). Moreover, the area of the passive components does not decrease with the technology scaling, increasing the cost of these integrated components.
4. Some blocks, as the power amplifier with high output power or the antenna switch, suffer an important performance penalty if they are implemented in CMOS processes compared to their bipolar or GaAs counterparts, decreasing the performance of a whole system implemented in a pure CMOS process.

Moreover the realization of a single chip RF transceiver should not just be technically feasible, but also cost effective. Recently, the cost reduction of high performance systems (and not exclusively wireless systems) has raised a noticeable interest in a new design philosophy known as system on a package (SOP) as alternative to the single chip approach [28-29].

In this technology, several components or circuits can be each implemented in the most suitable (in terms of cost or performance) IC technology and then assembled together in a common 'substrate' (carrier substrate) by using a Muti-Chip Module (MCM) technology. This interconnection technology is relatively simple and economical and consists in alternating layers of low k dielectrics and low resistivity metal layers (copper) on a carrier substrate as diverse as high resistivity silicon, glass or low loss ceramics. In some way, this process can be seen as a 'high performance PCB process' (still done in a clean room) and allows heterogeneous devices/circuits to be integrated into a small form factor.

As an example, in a RF front-end the PA or the antenna duplexer/switch could be implemented in a GaAs process as long as a cheaper BiCMOS technology would be

used for the rest of the circuit. A similar system-partitioning could be done in digital circuits where the technologies used in memories are considerably cheaper than the ones used for processors or ASIC's. The system partitioning also allows the revision of each IC without being forced to upgrade the complete system, increasing the design flexibility.

In addition to matching the circuit functionality and performance to the best technology available in terms of cost, the SOP offers more advantages. In particular, the MCM interconnection technology (with copper and low k dielectrics) can be used to implement wide bandwidth I/O busses between high-speed digital circuits that are difficult to implement between packaged circuits [30-31]. This interconnection process can also be used in RF applications to obtain high quality and low cost passive components (not just inductors, but also filters, MEMS switches or varactors and even antennas), since they are built on a low loss and low cost substrate. Additional benefits of this approach consist in an improved isolation between the different IC's; thus low cost digital and high performance analog circuitry can share the same package, thereby retaining a high level of integration as well as a good relation cost, performance and functionality [32,33,34].

5. Organization and Goals of this Thesis

In this Introduction we have performed a top-down description of the environment around the wireless communications, mainly addressed to the design of RF circuits and the issues related to the fully integration of a RF front-end such as circuit architecture or available technologies. Eventually the complete RF transceiver has also been considered. The required coexistence of digital blocks and the analog-RF circuitry in modern transceivers sets the CMOS (or some of their variants such as the BiCMOS) as the only suitable technology for this monolithic implementation.

The direct-conversion architecture also plays a key role in this way towards the monolithic integration of wireless systems since it solves the problem of the IF image signal of super-heterodyne receivers and removes the necessity of the (non-integrable) image rejection filters. Unfortunately, the direct conversion architecture also comes with

some new issues that either did not exist or were not as relevant in the classical super-heterodyne architecture. The generation of quadrature signals at RF frequencies as high as 5 GHz, or the dc offsets and the self-mixing that can saturate the high gain amplifiers of the signal path are some of the most important.

The context of this thesis is the design of CMOS low power RFIC's suitable for direct conversion architectures. Our starting point is the analysis of the characteristics of the integrated passive components (inductors and mainly transformers) from a circuit designer perspective. Then, the achieved understanding of these components is exploited in order to optimize the performance of some of the building blocks of a RF front-end.

This thesis is divided in three main chapters. Chapter 1 is dedicated to the analysis of integrated transformers. It starts with a revision of the state of the art of the integrated inductors in order to set up the basis for the analysis of the monolithic transformers. Due to their influence on the component quality factor, a special insight is dedicated to the analysis of the eddy currents. Then, we introduce the integrated transformers and revise the topologies used in their implementation and their characteristics and electrical equivalent models. However, it is important to remark that the goal of this thesis is not the modeling of the component. Instead, we will use EM simulators to reproduce their behavior and point out some physical mechanisms present in integrated transformers that have not been properly considered in the equivalent electrical models presented in the literature so far. In particular, we will study eddy currents in integrated transformers and will demonstrate their dependence on the operating mode of the transformer as well as on the loads connected to the primary and the secondary. As we will see this phenomenon has a direct influence on the component model as well as on the component optimization. Thus, different optimization procedures should be applied to minimize the component losses depending on the application.

Finally, this chapter finishes with the design of a double balanced mixed that uses two differential transformers to increase the isolation between ports. It is demonstrated that a differential driving minimizes the effects of the parasitic capacitances and increases noticeably this isolation. It is also shown that the etching of the silicon underneath of

the integrated transformers that reduces these parasitic capacitances also increases this isolation (even if a single-ended excitation is applied).

Chapter 2 investigates the design of oscillators having low phase noise and large tunning range. After identifying the quality factor of the integrated inductors as one of the main factors limiting the oscillator phase noise, a novel transformer-based (parallel) resonator is introduced. This new topology overcomes the performance of the common inductor-based resonators in terms of tuning range and effective quality factor.

A detailed description of the resonator is then performed in order understand its potentially and limitations. Thus, its properties are firstly studied from an electrical circuit perspective using the equivalent models discussed in the previous chapter. Then, it is realized the analysis in the EM domain in order to compare its performance with the standard inductor-based resonator. Once again, eddy currents are identified as the main factor limiting the effective quality factor of the transformer-based resonator. Thanks to the already achieved understanding of integrated transformers, the layout optimization method proposed by López-Villegas [35] for integrated inductors can be extended to the optimization of the transformer (when working in common-mode). The extension of the parallel design to N-resonators is also shortly discussed. Finally, the proposed resonator is used in a low phase-noise 1.7 GHz CMOS VCO.

Chapter 3 presents a new topology of quadrature oscillator based on the differential coupling at the second harmonic of two differential oscillators. As in the previous design, an integrated transformer plays a relevant role in this circuit being used to establish the coupling between oscillators. In order to obtain a basic understanding of the phenomena involved in the generation of quadrature signals using the proposed method and set up the design procedure several concepts must be revised. In particular, the theory on forced (or injected) and coupled oscillators is discussed and applied to the proposed quadrature oscillator. Finally, to show the feasibility and potentiality of this methodology, different designs in integrated and hybrid implementations are presented.

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INTEGRATED TRANSFORMERS

Introduction

Since Nguyen and Meyer demonstrated the feasibility of integrated inductors on Silicon substrates, huge research efforts have been dedicated to their analysis, design, modelling and optimization. The hundreds of papers dealing with integrated inductors published in specialised journals during the last ten years corroborate this fact. As a result of these efforts, the inductor performance has been noticeably improved. Conversely, integrated transformers still remain strange components and are rarely used.

In this chapter we will analyze the integrated or monolithic transformers and we will try to set up a fundamental understanding of their properties. This knowledge will prove very useful to guide the circuit designer towards an efficient/optimum design of these components and help him to fully exploit their potential or skip their limitations.

Since a transformer is nothing else than two coupled inductors, a solid knowledge of the characteristics and limitations of the integrated inductors will be an excellent starting point for the analysis of integrated transformers. Therefore, this chapter starts with a short revision of the state-of-the-art of the integrated inductors, pointing out how the technology affects their performance and in particular, their quality factors.

Reproducing a lumped equivalent electric model for an integrated inductor, commonly found in the literature and based on physical assumptions, the improvements achieved by the technological advances can be easily understood. Many times this equivalent model is the only tool available for the circuit designer and the lack of an additional comprehension of the component characteristics leads to an inefficient or non-optimum use of it.

In spite of the many similarities between inductors and transformers, there are some important differences in how magnetically induced losses affect these components and are considered in their equivalent models. Thus, during the inductor revision, special attention is given to the analysis (based on EM simulators) of the different mechanisms that contribute to inductor losses (i.e. limit their quality factor) for a further comparison. The transcendence of the quality factor from the circuit point of view is widely discussed in Chapter 2.

Later, the ideal transformer is presented and the different topologies used to implement integrated transformers are compared. The transformer equivalent model is shortly discussed since the modeling of the component is out of the scope of this work. However, some important facts that affect directly the modeling of the component are pointed out for the first time. In particular, in this work we will demonstrate that the transformer losses can not be reproduced with the transformer models proposed so far. Moreover, the understanding of the transformer losses will point out that the optimization of the transformer layout is strongly dependent on the application.

Finally, this chapter finishes with the design of a double balanced mixer that uses two differential transformers to increase the isolation between ports. It is demonstrated that a differential driving reduces the effects of the parasitic capacitances and increases noticeably the LO-RF isolation, a key parameter when the mixer is intended for direct conversion since it minimizes the self-mixing. It is also shown that the etching of the silicon underneath the integrated transformers which, decreases these parasitic capacitances also increases this isolation (even when a single-ended excitation is applied).

1.1 Integrated Inductors

Basically, two parameters, the self-resonant frequency and the quality factor characterize the performance of any inductor. The self-resonant frequency (SRF) is caused by the parasitic capacitances and offers an estimation of the maximum operating frequency of the component. For frequencies above the SRF the inductor shows a negative reactance, i.e. acts like a capacitor.

The quality factor is defined as the ratio between the magnetic power stored and the power dissipated in the component. Thus, the higher the quality factor, the smaller the power lost in the component. For an inductor, the previous definition of Q results in $Q=\omega L/r_s$ where L is the inductance value and r_s is the series resistance associated to the metal strips. It is also quite common to define the quality factor of a resonator in terms of the phase of the impedance θ as:

$$Q=-\frac{\omega_o}{2}\frac{d\theta}{d\omega}\bigg|_{\omega=\omega_o} \qquad \textbf{(1.1)}$$

being $\omega_o=2\pi f_o$, with f_o the resonant frequency.
For a simple LC resonator, built with a lossless capacitor both definitions of Q are equivalent.

High Q inductors can be used in LNA's [1,2] as passive loads to increase their gain (gain peaking) or as matching elements to reduce its noise figure [3]. In Gilbert cell mixers [4], inductors can be used as degeneration elements to increase the circuit linearity. High Q inductors also improve the phase noise performance of oscillators and reduce their power consumption [5,6]. Moreover, when inductors are used as passive loads or as degeneration elements, it allows the reduction of the dc voltage headroom since no dc voltage appears across them. In summary, the benefits of high Q values translate directly to low-noise and low-power systems.

To understand the limited performance of the integrated inductors, the characteristics of the technologies used in their implementation and their evolution must be revised. Besides, this technological review may allow us to predict future trends in their implementation or how new technology advances will affect their performance.

1.1.1 Silicon Technologies for RF Applications

In the early 60's, the first studies about passive components integrated on Silicon substrates realized by Warner and Fordemwalt led to the conclusion that their performance would be limited even for HF frequencies [7]. Low self-resonant frequencies and high losses were the unwanted but actual characteristics of Silicon integrated inductors.

The overall inductor losses can be divided into two main contributions: substrate losses and strip metal losses. Due to the low resistivity of the Silicon substrates (and specially, of the substrates used in CMOS processes) and to capacitive coupling, conduction currents flow not only along the metal strips but also in the silicon substrate. Besides, the magnetic field generated by the inductors may also induce currents in the low resistivity substrate. The losses caused by both current contributions impact dramatically on the component performance.

The substrate losses can be minimized or even removed placing an insulator in the local area underneath the inductor. Actually, the best solution would consist in the complete removal of the substrate underneath the component. This can be easily accomplished using bulk or surface silicon micromachining [8,9] and yields clear advantages:

1) The self-resonant frequency is shifted up.
2) Substrate losses are completely removed.

However, this method, applied by Chang et al. [9] to the design of a CMOS RF amplifier in the early 90's, has not been well received by the industry. The reasons are the necessity of a post-processing step to remove the substrate and mainly the possibility of mechanical failure of the device during the packaging process.

A more conservative approach to improve the inductor performance, but still in the same direction, consists in placing the device on an insulating substrate such as quartz [10,11], sapphire [12,13], glass [14,15] or high-resistivity silicon [16]. When comparing this technique to the micromachining, the main advantage is the presence of mechanical robustness. However, self-resonance is decreased due to the higher permittivity of these materials.

An additional source of losses in integrated inductors arises from the strip resistance due to the thin metal layers of aluminium typically used in digital IC processes. These losses are still more evident if either of the techniques described previously is employed. Losses in the metal regions are mainly related to the metal strip resistance (sheet resistance) and their analysis requires taking into account conduction (ohmic) losses and magnetically induced losses (related to eddy currents). Actually, at the end of this section, a detailed analysis of these magnetically induced losses is performed. Several techniques can be introduced to decrease the value of this sheet resistance:

1) Increase the metal thickness or use stacked metal layers [17].
2) Use metals with lower resistivity (Cu instead of Al) [16,18].

Nowadays, most of the commercial analog high performance processes still do not exploit fully the above mentioned techniques. In most of the cases, an additional module is added to the basic process to obtain high Q inductors. This additional module consists in a thick metal layer (around 3 μm) on top of a thick dielectric layer to separate the spiral from a relatively high resistivity substrate.

Currently, for short channel digital technologies, the interconnection delay is becoming comparable to the gate delay, and affecting seriously the circuit speed [20]. To solve this issue digital technologies are moving to other types of metals (in particular copper) and low k dielectrics. Thus, it is expected that in the next future the inductor performance will benefit from this technological evolution.

On the contrary to this technological evolution, the eventual introduction of high permeability magnetic materials compatible with IC processes would have a revolutionary implication since inductor and transformer dimensions will shrink dramatically.

1.1.2 Modelling of Integrated Inductors

The actual performance of the integrated inductors is mainly limited by the technology characteristics. Nevertheless, their efficient use is also restricted by the partial lack of accurate models and design rules able to guide the designer towards the choice of the optimum component for a specific application. These models should provide the characteristics of the inductor (inductance, quality factor and SRF) in terms of technological parameters and the inductor layout (strip width, number of turns, distance between strips, etc).

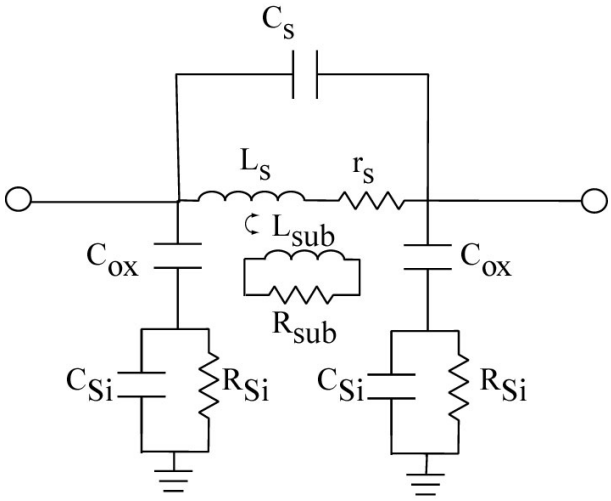

Figure 1-1. Equivalent model for an integrated inductor

An example of such an inductor equivalent model based on physical hypothesis is shown in fig.1-1. Obviously, the core of the model is an ideal inductor, L_s. r_s models the series resistance of the interconnect metallization increased by the eddy currents, and hence, it depends on the frequency. This resistance could also include the losses caused by the eddy currents induced in the Silicon substrate. However, in the model of fig. 1-1 these currents are modelled through a coupled inductor L_{sub} and an additional resistor R_{sub}. This approach gives more insight in the nature of these magnetically induced losses and in its frequency dependence [21]. Fortunately, several authors have already pointed out that for substrates with resistivities in the order of 10Ωcm these currents are negligible for frequencies below 10 GHz and hence the most common models do not include these elements [22].

Finally, the capacitor C_{ox} models the capacitance from the spiral to the substrate, C_c models the capacitance between the windings and C_{si} and R_{si} model the capacitance and resistance of the substrate.

These lumped models are attractive as they are easily included into standard circuit design tools. Furthermore, most of the parasitic capacitances and resistances in these models have simple, physically intuitive, analytical expressions. Unfortunately, they are not accurate enough for design purposes. To overcome this problem, EM simulators can be used to predict the behaviour of passive devices with a high degree of accuracy. However, the designer must have some expertise with these EM solvers and the design time increases due to the required computation time.

In the past many efforts have been dedicated to the elaboration of compact models based on analytical expressions (obtained from the physical behaviour) in order to save the large amount of computing time associated to EM solvers. Nowadays, thanks to the dramatic improvement of personal computers the time penalty associated to EM solvers is not as important. Still, these models can guide the designer towards the best geometry and give further insight in the optimization procedure. Thus the designer can skip the EM tools until the last steps of the design cycle are reached, when fine-tuning of the component is required.

1.1.3 Eddy Currents in Integrated Inductors

Once the substrate losses are minimized or removed using high resistivity substrates or micromachining techniques, the magnetically induced currents in the metal strips become important. These crowding currents or eddy currents are due to the time variation of the magnetic field and manifest themselves as a non-uniform current distribution along the strip width and not along the thickness as assumed by the skin effect.

EM simulations will allow us to corroborate this point. Throughout this work, we have intensively used Momemtum, an EM simulator based on the Moments method, to analyze the characteristics of integrated inductors and transformers. However, it does not offer the possibility to visualize the shape of the magnetic field generated by the

inductor or the current distribution along the strips width. Thus, we have obtained this particular data using the ANSYS quasi-static magnetic solver.

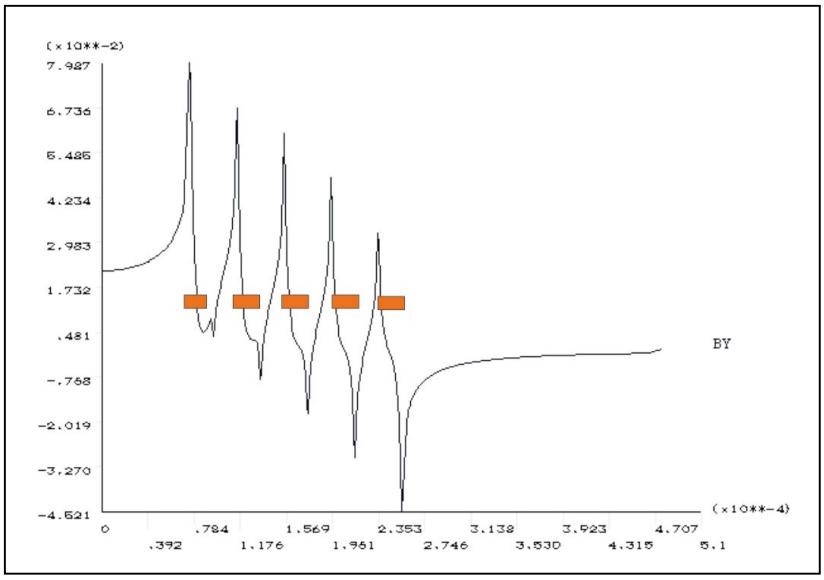

Figure 1-2. Magnetic field (in Tesla) perpendicular to the inductor plane with N=5, w=20µm, d=20µm and ri=75µm

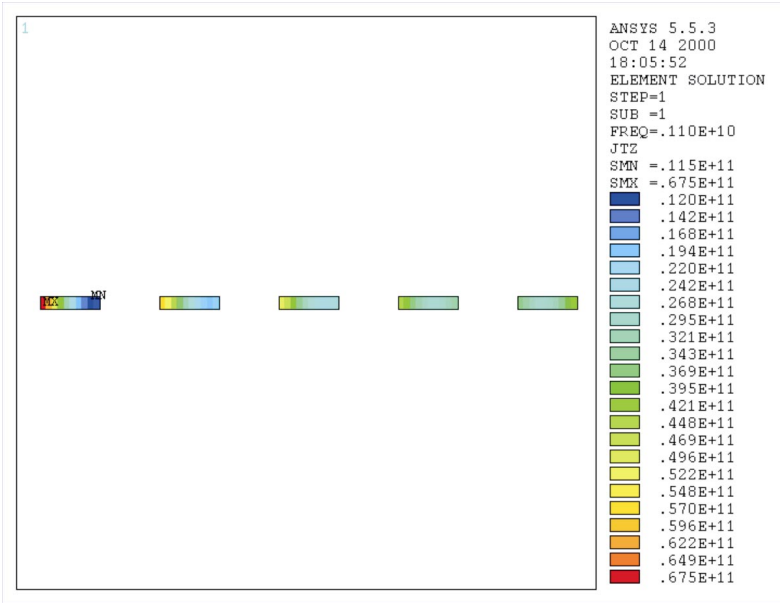

Figure 1-3. Current density (A/m^2) for an inductor strips with N=5, w=20µm, d=20µm and ri=75µm

Previous figures show the magnetic field in the direction perpendicular to the inductor plane and the resulting current distribution across the strips width for a circular inductor with the following characteristics: 5 turns, 20 µm of strip width, 20 µm of distance

between strips and an inner radius of 75 μm. In this simulation the inductor was fed with a current of 1A at 1 GHz.

The magnetic field is stronger at the centre of the inductor and decreases as we move away from it. The larger current gradients are also found for the inner turns as long as the outer turns present a much more uniform current distribution. This fact justifies the widely used hollow inductors [23], consisting in removing the inner turns of the inductor, since they do not contribute significantly to the inductance value but they suffer considerable losses magnetically induced.

Although these crowding currents do not modify noticeably the value of the inductance [24], they cause an important increase of the effective resistance of the metal traces with the frequency and hence limit the inductor quality factor. To illustrate this fact, an inductor has been simulated under different conditions as it is done in [8]. In the first simulation, the inductor has been meshed in simple cells (just one cell along the strip width). Therefore, the effects of eddy currents are not taken into account. Then, the inductor is meshed using a more refined mesh and the strip width is split into more than one cell (3 in our particular case). The results of the simulations are shown in fig. 1-4.

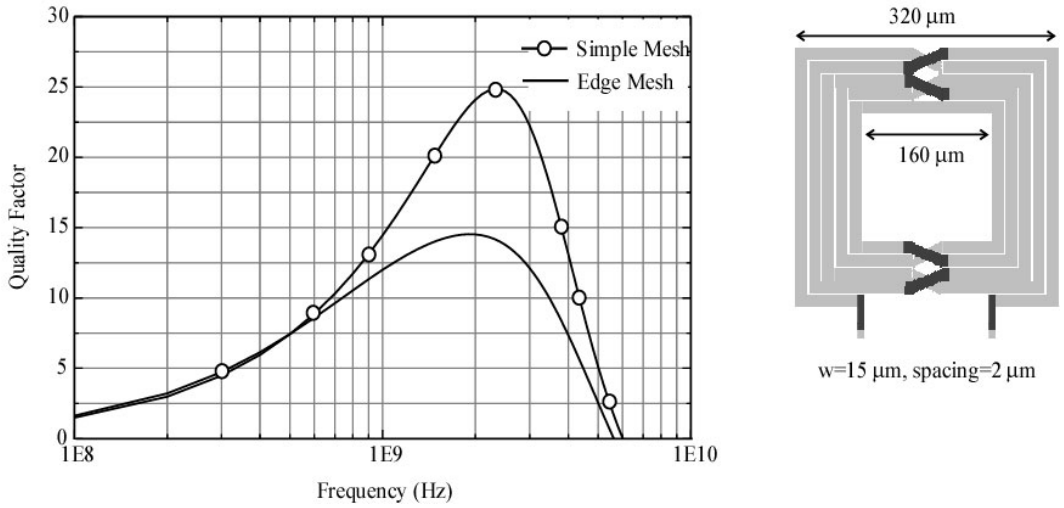

Figure 1-4. Comparison of the quality factor of an integrated inductor obtained using a simple mesh (considers only ohmic losses) and an edge mesh (considers also eddy currents)

Compact inductor models take into account the losses generated by the eddy currents adding an additional term R_{rf} to the series resistor R_s, that increases with the square of the frequency, with the magnetic field strength and with the strip width [25,26,27]. For

frequencies of few GHz, the term R_{rf} may be comparable to DC resistance of the inductor. Thus, since the losses caused by these crowding currents grow with the strip width, they may prevent the improvement of the quality factor by increasing the strip width (i.e decreasing the ohmic resistance).

1.2 Integrated Transformers

The operation of passive transformer is based on the mutual coupling between two or more conductors, or more currently, inductors. An example of an integrated implementation it is shown in fig. 1-5 where two inductors are interwound in order to favour their mutual coupling. According to the Lenz law, the variations of the magnetic flux produced by the current flowing in the primary induce a current in the secondary winding that flows out of the terminal S. This produces a positive voltage across a load connected between terminals S and S'. Since just the variations of magnetic field generated by the primary can induce currents in the secondary, it should be noted that dc signals are blocked by the transformer allowing the windings to be biased at different voltages.

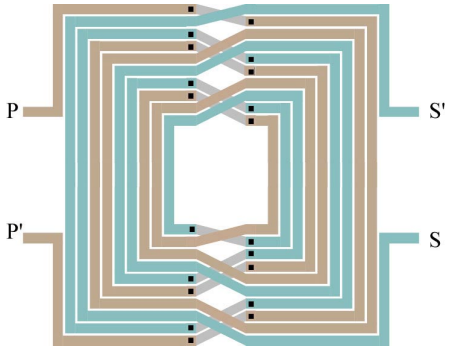

Figure 1-5. Symmetric transformer layout

The phase of the voltage induced at the secondary of the transformer depends on the choice of the reference terminal. For an ac signal source with the output and ground applied between terminals P and P', there is a minimal phase shift of the signal at the secondary if the load is connected to the terminal S (with S' grounded). This is the non-inverting connection. In the inverting connection, terminal S is grounded and S' is connected to the load so that the secondary output is antiphase to the signal applied to the primary. Aside from the phase shift between the input and the output ports, other

aspect of the transformer electrical behaviour depend on the choice of the terminal configuration [28,29].

An ideal transformer may be defined as one that is transparent to the source and the load and delivers 100% power from the source to the load without dc connection. In order to get such a performance, transformers are expected to have infinite inductance for each coil, no resistive losses in the coil conductors, 100% magnetic coupling between the primary and the secondary coils and no power losses through adjacent materials. Unfortunately, its monolithic implementation do not satisfy by far a single one of these requirements. We will analyze later in this chapter how this departure from the ideal behaviour affects the performance of circuits containing them.

In spite of their apparent limitations, integrated transformers have been used in many RFIC's such as LNA's [30], oscillators [31,32,33] and mixers [34,35] to perform functions such as impedance matching/transforming, signal coupling, phase splitting, low noise feed-back networks, etc. But probably, the most common use of a transformer in IC applications is the balun where the transformer couples a balanced (or differential) circuit to an unbalanced (single-ended) one. This can be easily accomplished by grounding the center-tap or mid-point of one transformer winding.

1.2.1 Transformer topologies

Many different structures have been proposed for integrated transformers but the most successful are shown in fig. 1-6. The first one, the SCS sided-coupled structure, exploits the magnetic coupling between two inter-wounded inductors and requires a process with two metal layers. In this topology the primary and the secondary are equal and hence it is suitable for applications demanding a symmetrical component. However, a center tap can not be established in any of the windings due to the asymmetry of the primary and the secondary. This issue can be solved using a fully symmetrical SCS topology as shown in fig. 1-6b at expense of an important increment of the number of vias. One problem with the SCS is the area efficiency. As the primary and the secondary coils are placed on every other lanes, this topology takes more silicon area compared to others structures, for the same amount of coil inductance.

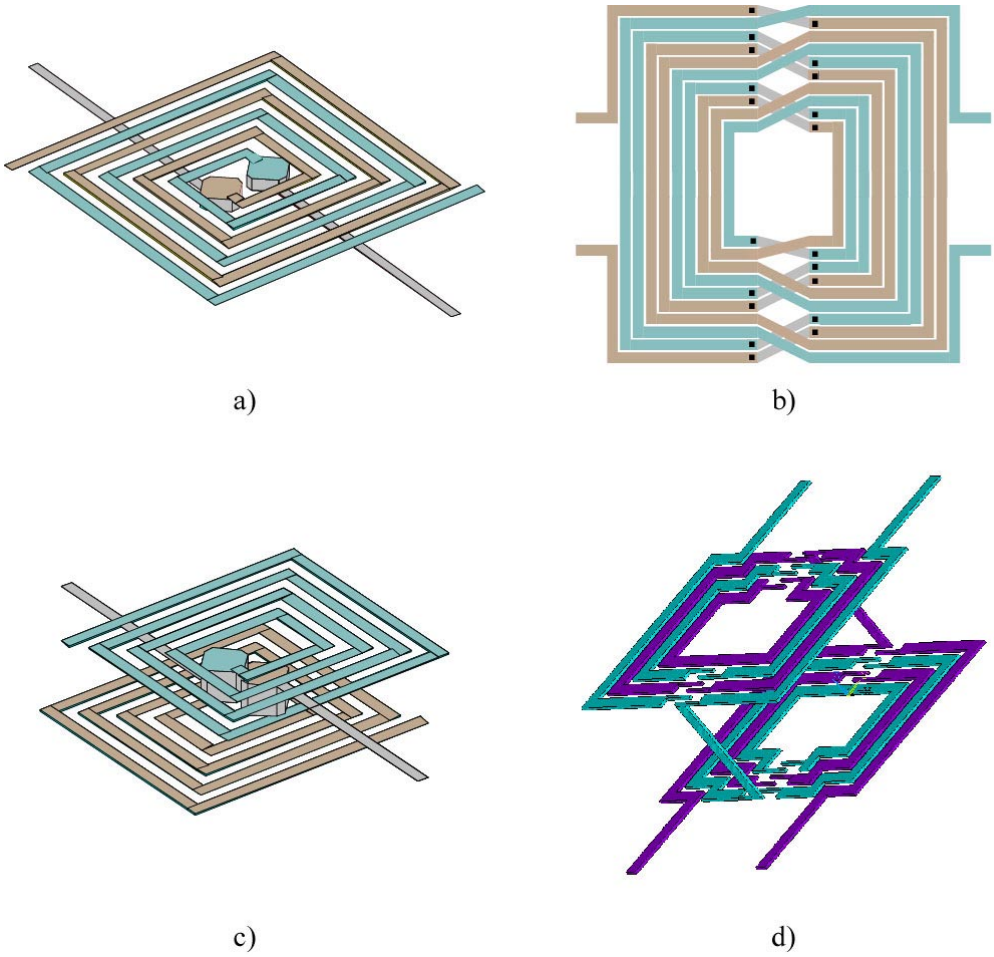

Figure 1-6. Different implementations of Integrated Transformers

As an alternative to the SCS, the vertical coupling structure VCS places the primary on top of the secondary coil resulting in a higher mutual coupling due to the proximity between both spirals. Typically, the metal-to-metal spacing is less than 1 micron. Considering the pressure for low cost implementations of the RFIC's, the area efficiency is a fundamental advantage of the VCS. However, the VCS has also a couple of problems. The VCS requires a process with 3 metal layers and is not symmetric. Part of this asymmetry arises from the different thickness between metal layers in most VLSI interconnects schemes, which results in unequal resistances for the upper and lower winding. Also, the lower winding shields the upper winding from the conductive substrate, and hence the parasitic capacitance to the substrate differs for each winding. In addition, there is a large capacitance between both windings due to the overlaping of metal layers, which limits the frequency response. In many RF applications, this non-symmetric nature of the VCS can be a limiting factor for its usefulness.

Fig. 1-6d shows a transformer topology, which takes advantage of the strong points of the previous two structures [35]. Like VCS, the MCS has the advantage of the area efficiency. MCS is expected to show good mutual coupling, comparable to the VCS, not only, by the placement of the primary on top of the secondary but also by the cross-placement of the coils. Moreover, MCS is nearly symmetric and can be implemented with just double metal process. The primary or the secondary of the MCS can have higher series resistance due to the vias used to switch between the top and the bottom metal layers.

As for inductors, bond-wires can be used to implement transformers. Thus, in the bond-wire transformer proposed by [36] an individual loop consists of two bonding pads, a bond-wire and a micro-strip line. This transformer has low insertion losses due to the thick gold bond-wires. We should also mention that passive transformers have their active counterpart, but as in the case of inductors they suffer from several drawbacks as power consumption, noise or non-linearities.

1.2.2 Transformer modeling

As in the inductor case, the design and optimization of circuits containing transformers requires the existence of accurate models derived from the physical layout and the process technology specifications. Unfortunately, the complete electrical behaviour of monolithic transformers can not be accurately predicted from closed-form equations, and hence numerical methods must be used. The numerical solution of Maxwell equations in three dimensions will give the most accurate results, and this technique is becoming more practical for the design of multiturn spirals transformers as computing technology and simulation software improve. Nowadays, the most common tools of circuit design already include some EM tool or some direct interface to a specific EM tool and favour its use. EM solvers also provide faster means to explore novel structures and devices before analytical models are developed.

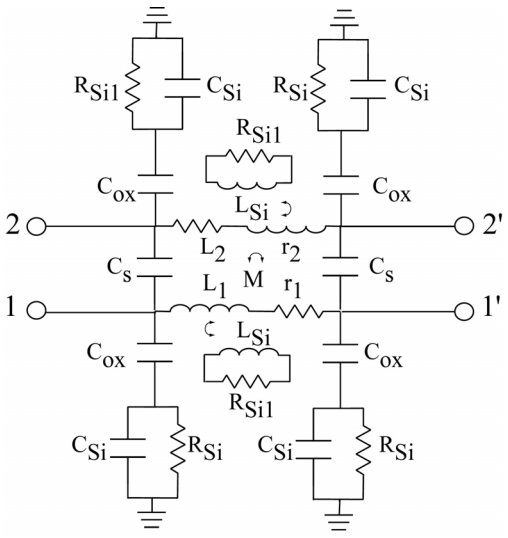

Figure 1-7. Equivalent model for an Integrated Transformer

An example of compact model for a transformer with four ports is shown in fig. 1-7. In many practical implementations, the compact model can be simplified since one or more ports are grounded and hence some devices are short-circuited. At the core of the model, there are two coupled inductors. Resistors r_s represent the ohmic losses in the windings. The interwinding capacitances are modelled by capacitors connected between the primary and the secondary C_s. The dominant capacitive parasitics between each winding and the underlying substrate are represented by the series connection of capacitors C_{Si} and C_{ox}, and substrate loss is included through the addition of a resistor R_{si} in parallel with C_{Si}.

The definition of a loss-related figure of merit for RF transformers, in analogy to the quality factor of inductors, is not straightforward. Maybe the insertion losses could be the most important characteristic to evaluate the performance of integrated transformers since they give an idea of how efficiently a signal in the primary coil is transmitted to the secondary coil. Insertion losses are determined by metal ohmic losses, substrate dissipation, and magnetic coupling factor and can be reduced placing a tunning capacitor in shunt with each winding, at expense of narrowing the frequency bandwidth. Also, many of the techniques that have been applied to optimization of monolithic inductors are also applicable to the transformers. For example, ohmic losses are reduced when multiple layers are used to construct each winding. The current trend in Silicon technologies toward thicker and lower permitivity dielectrics will result also in improved performance from stacked winding transformers in the future.

1.2.3 Eddy Currents in Integrated Transformers

In the previous section, devoted to the revision of the state of the art of integrated inductors, we have given a special insight to the analysis of eddy currents. The goal of this section is to extend this analysis to the integrated transformers and to highlight some important differences existing between both components. In particular, we will try to identify any eventual cancellation of eddy currents due to the transformer effect and how it may affect the design, modelling and optimization of the component.

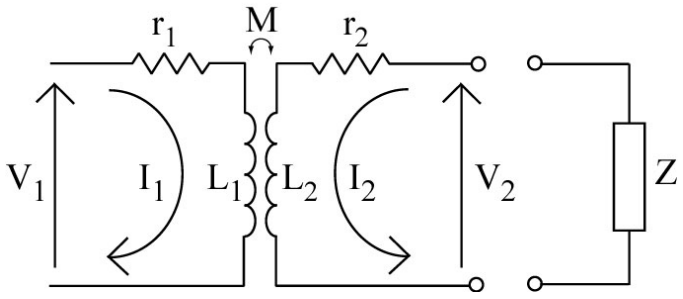

Figure 1-8. Simplified transformer model

As eddy currents depend on the strength of the magnetic field, the first step in this discussion will be to obtain its distribution over the transformer in terms of the currents flowing in the primary and the secondary for a general impedance attached to the secondary. This can be addressed using this simple transformer model:

$$\begin{aligned} V_1 &= jL_1\omega I_1 + jM\omega I_2 + r_1 I_1 \\ I_2 Z &= jM\omega I_1 + jL_2\omega I_2 + r_2 I_2 \end{aligned} \qquad \textbf{(1.2)}$$

Solving these equations:

$$\frac{I_2}{I_1} = \frac{-j\omega M}{j\omega L + r_2 - Z} \qquad \textbf{(1.3)}$$

(1.3) shows that for an ideal transformer (M=L and large inductance coils) with a turn ratio equal to 1, the current in the secondary is equal to the current in the primary. Unfortunately, in practical implementations the load impedance Z can be comparable to the impedance of the windings, and hence it will affect seriously the current flowing in the secondary.

The magnetic field could be written as the product of a constant depending on geometric parameters and the respective currents flowing in the primary and the secondary:

$$B_{1n} = G_n I_1 - g_n I_2 = (G_n + \frac{j\omega M g_n}{Z - j\omega L_2}) I_1$$
$$B_{2m} = g_m I_1 - G_m I_2 = (g_m + \frac{j\omega M G_m}{Z - j\omega L_2}) I_1 \quad \textbf{(1.4)}$$

where B_{1n} and B_{2m} are the magnetic field over the n and m turn of the primary and the secondary. (1.4) introduces explicitly the dependence of the magnetic fields (i.e, of the eddy currents) with the load attached to the secondary. Thus, for the same value of I_1, different distributions of the magnetic field will be found depending on the impedance attached in the secondary, i.e, the eddy currents will be different in each case.

To corroborate this fact, the ANSYS quasi-static solver has been used again to compute the magnetic field and the current distribution for two different loads connected to the secondary, an open circuit and a short-circuit. These results have been obtained for a stacked transformer with the following characteristics: 5 turns, 20 microns of strip width and distance between strips and 75 microns of inner radius. Primary and secondary were separated vertically by 10 microns and were embedded on air. The primary was fed with an ideal current source of 1A at 1.1 GHz. The model has radial symmetry.

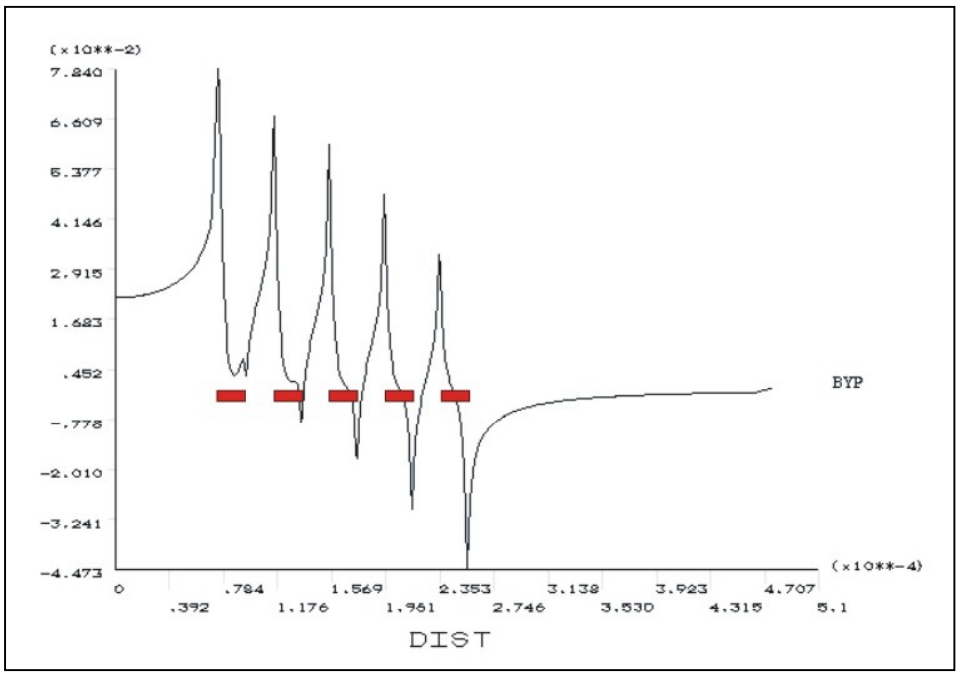

Figure 1-9. Magnetic field (in Tesla) for an integrated transformer with the secondary in open circuit

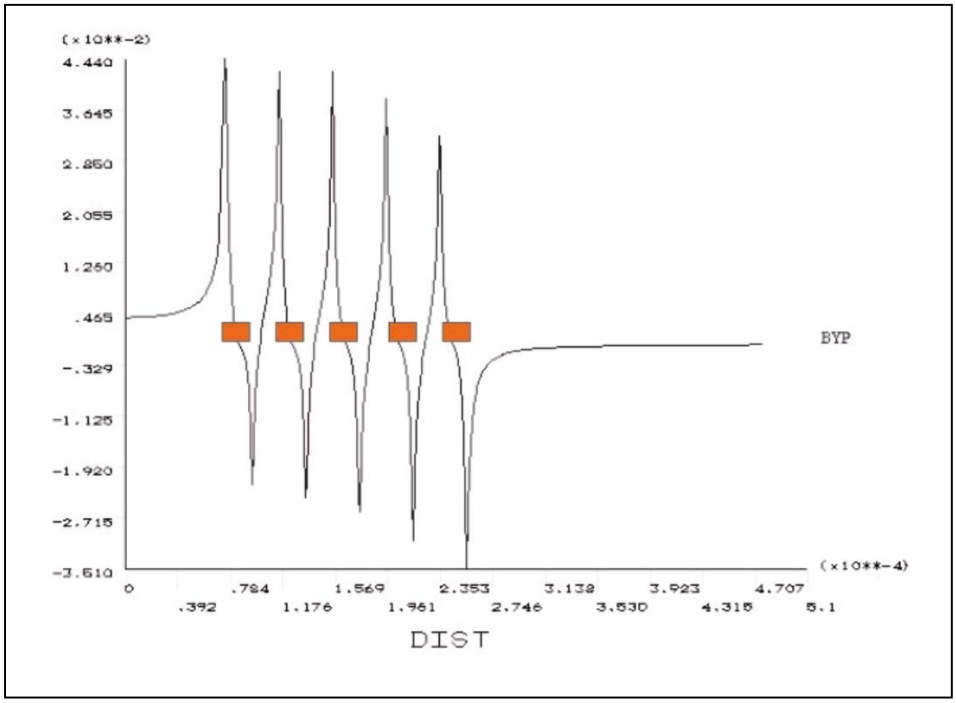

Figure 1-10. Magnetic field (in Tesla) for an Integrated Transformer with the secondary in short circuit.

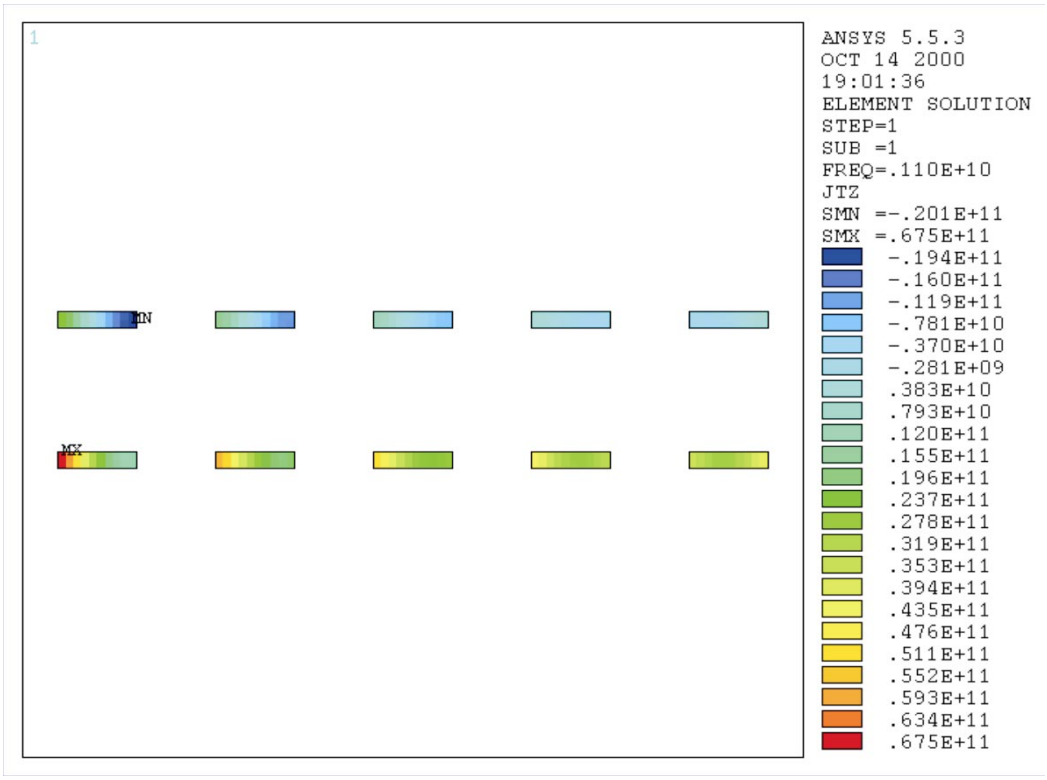

Figure 1-11. Current density (A/m^2) **for an integrated transformer with the secondary in open circuit**

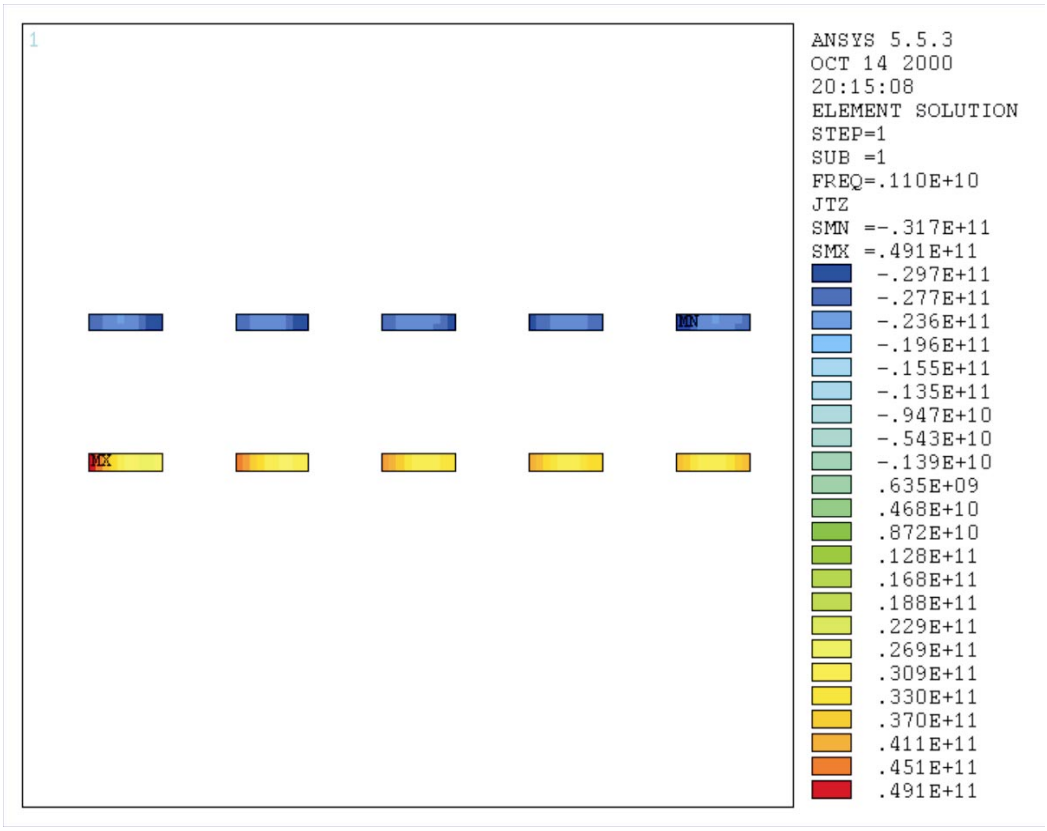

Figure 1-12. Current density (A/m^2) for an integrated transformer with the secondary in short-circuit

For the transformer with secondary open, as expected the magnetic field and the current distribution across the strips are very similar to the inductors one, since no current can be induced along the secondary. Significant gradients of current can be observed in the primary. The main difference of this structure when compared with the inductor is that in this case eddy currents are also induced in the secondary, increasing the losses of the component.

When the secondary is short-circuited the situation suffers an important change. Now, current can be induced along the secondary and the distribution of the magnetic field changes drastically. The geometry of this transformer, with the lateral dimensions much larger than the vertical, favours the cancellation of the magnetic field turn-to-turn; the m-spiral of the secondary cancels the m-spiral of the primary. This cancellation is more efficient as the m and n spirals are further away from each other. As a result, the magnetic field distribution over the inductor strips for a short-circuited secondary is very similar to the field distribution found for an isolated strip. Thus, the influence of eddy current will be much lower in this case and a much more uniform current distribution across the strip width is observed.

So far, we have considered that the current flowing in the secondary tries to cancel the variations of magnetic field generated by the current flowing in the primary. However, in some applications both currents can generate magnetic fields that are added constructively. In this case, the transformer will not result in a compensation of eddy current but in an increase. To prove it, a transformer previously simulated with Momemtum has been excited in two different modes.

In the first mode, know as differential, a current source is applied at the primary and the secondary of the transformer, resulting in the partial cancellation of the magnetic field. In the second mode, know as common mode, the sense of one of these current sources is reversed so the magnetic fields generated added constructively. Exciting the transformer with ideal current sources prevents any loading of the primary by the load connected to the secondary or viceversa. As a consequence, the series resistance observed from the primary or the secondary is indeed the actual resistance of the winding. This resistance is plotted in fig. 1-13 for both operating modes. As expected, the series resistance in the common mode increases considerably faster with frequency than in the differential

mode. It is important to note that this series resistance also increases with the frequency (even in absence of eddy currents) as the self-resonant frequency of the component gets closer and this is much more important in the common mode since the overall inductance is much higher. To remove this effect the transformer used in this analysis was embedded on air to increase its resonant frequency. Moreover, the transformer was used in a resonator circuit (we will analyze them deeply in next chapter) to verify the series resistance plotted in fig. 1-13 was the actual resistance of the coil.

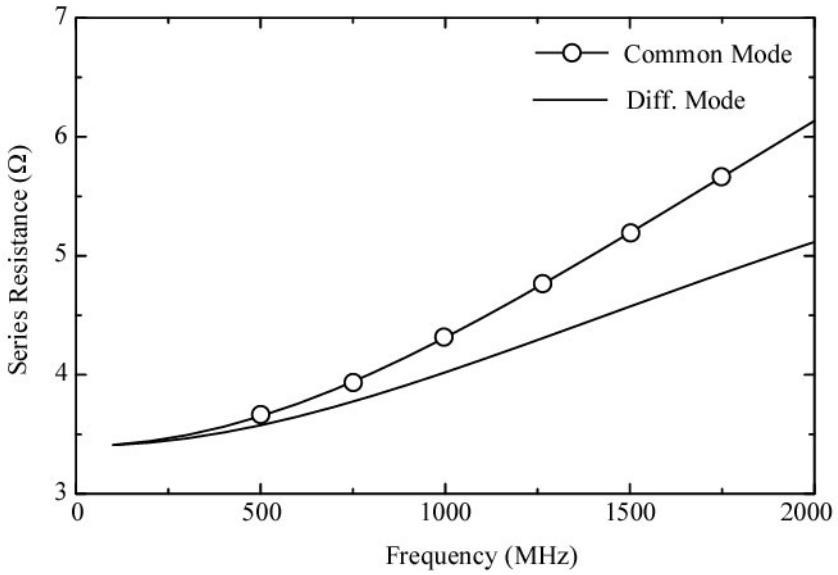

Figure 1-13. Series resistance of the primary or secondary coil in the common and differential modes

The previous discussion has several consequences that manifest themselves in the modeling of the component as well as in its optimization. These consequences can be summarized in the following items:

1) Eddy currents depend on the currents flowing in both the primary and in the secondary and hence can not be estimated independently on the load attached to the secondary. Therefore, a frequency dependent resistor (but independent on the secondary load) as the used in the modeling of the series resistance of integrated inductors can not reproduce the series resistance of the transformer coils for a general case. At the moment, no model considering these effects has been presented.
2) Eddy currents are minimized when the transformer operates in its differential mode as long as they reach a maximum in the common mode where the transformer is equivalent to an inductor.

This analysis has also showed that the optimization of the transformer is strongly dependent on the application. Thus, when the transformer acts as a power transferer or balun (i.e, it works in its differential mode) the reduction of the component losses can be achieved increasing the strip width (reducing the ohmic losses) since eddy currents are considerably low. Instead, in applications where the transformer acts in its common mode (such as matching or transforming impedance networks, resonators) losses related to eddy currents are significant and should be minimized. This fact will be intensively exploited in chapter 2.

1.2.4 Capacitive effects

In the previous section we have seen that eddy currents manifest a more complex behavior for the transformers than in the inductors case. Capacitive effects present some peculiarities as well.

For instance, the effects of the interwinding capacitance on the transformer performance depend on its configuration. Thus, considering a non-inverting topology (fig.1-14) the voltage at the non-grounded port of the primary and the secondary coils are essentially the same (assuming a turn ratio 1:1). Consequently, the capacitance C_s has a little influence (ideally none) on the transformer behaviour. This situation changes drastically if we consider, instead, an inverting configuration for the transformer. In that case, the voltage across C_s is twice the voltage at the primary or secondary and its effect on the transformer performance could be very important.

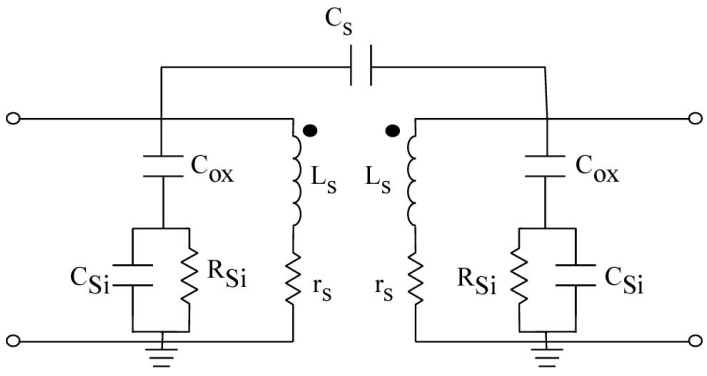

Figure 1-14. Equivalent transformer model containing the capacitive parasitc effects

This example clearly shows that port grounding on transformers modifies the influence of parasitic capacitances. This effect will be particularly important on transformed-

based baluns. These components are intended to generate a differential signal from a single-ended. This can be accomplished using a transformer with a center tap on the secondary.

To illustrate the effect of parasitic capacitances at the circuit level we have designed a double balanced mixer based on a ring of Shottcky diodes. In this circuit, two integrated transformers are used to couple the input signals to the diode ring. Due to its symmetry, this structure has inherently a high isolation between the input ports which is only apparently limited by the mismatch between the diodes and transformers and by parasitic couplings. Fig. 1-15 shows the schematic of a passive double balanced mixer and fig. 1-17, its monolithic implementation using the DIMES03 Technology from Delft University.

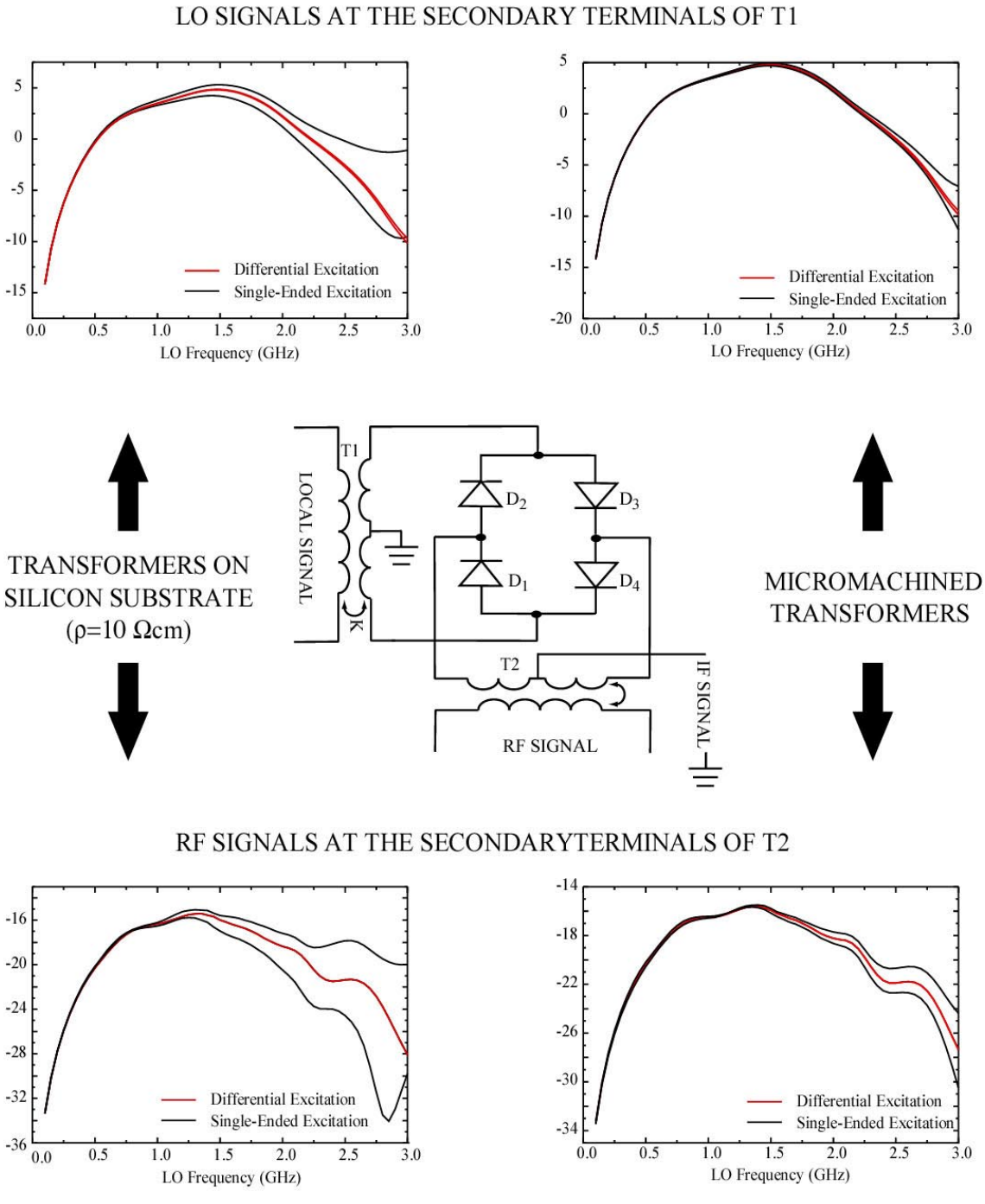

Figure 1–15. Analysis of the signals present in a double balanced mixer in terms of the type of excitation (single-ended or differential) and the type of substrate used to implement the integrated transformers (Silicon with ρ=10Ωcm and a micromachined substrate). The Shottcky diodes used in these simulations are the HSMS2810 from Agilent Technologies

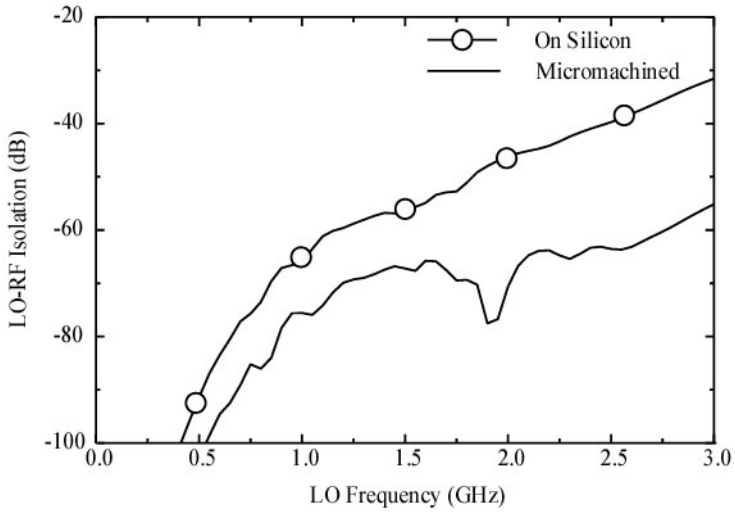

Figure 1-16. LO-RF Isolation for a double balanced mixed with a single-ended excitation

In this circuit, capacitive effects break the symmetry of the differential signal generated at the secondary of the transformer baluns. This is clearly observed on the graphics of fig. 1-15. Curves labeled "Single-ended excitation" show different voltage magnitudes at both terminals of the secondaries. Differences increases as the frequency increases. This effect is clearly seen when the baluns lay on a Silicon substrate. When the Silicon is removed the decrement of the parasitic capacitances is translated to small differences between voltage magnitudes at the secondary terminals. In both cases, no differences are observed if the baluns are excited with a differential signal.

The break of symmetry under single-ended excitation directly impacts on the isolation between ports of the double balanced mixer. This is shown in fig. 1-16 where the LO-RF isolations are plotted for on Silicon and micromachined mixers. The reduction of coupling capacitance is clearly observed as an improvement of the LO-RF isolation of about 20 dB for frequencies above 2 GHz. The specific value of isolation found in the previous simulations has no a real meaning since neither mismatches in the diodes nor parasitic coupling through the transformers are considered. Still, it highlights the effects of grounding the input ports.

Currently, several configurations of the mixer show on fig. 1-17 (micromachined and on high resistivity substrates and also with single-ended and differential excitations) are being fabricated on the DIMES03 Technology in order to corroborate the expected behaviour.

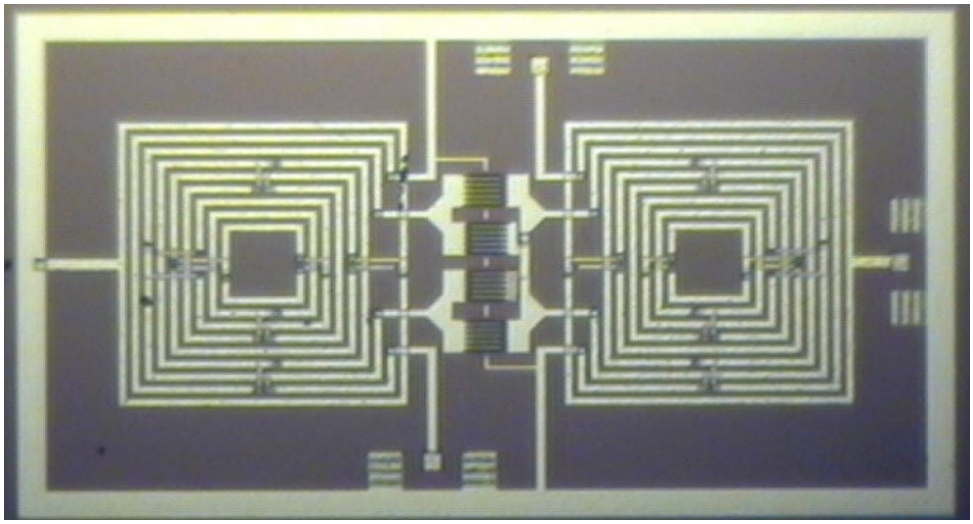

Figure 1-17. Layout of a passive double balanced mixer

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LOW PHASE-NOISE OSCILLATOR

Introduction

In the Introduction chapter, we have shown how the present state of the art of the BiCMOS technologies suggest that it is possible to afford with guaranties the integration of a whole RF front-end based on a direct-conversion architecture. However, the integration of the oscillator still presents some difficulties. These are mainly related to the limited tuning range achievable in practical implementations and to the tight requirements in terms of phase noise performance imposed by the communication standards.

Let us revise shortly the concept of phase noise and how it affects the performance of a RF system. A real oscillator has different noise sources (internal, due to its constituting devices, and external) that manifest themselves in the amplitude and frequency of the output signal. In most of the practical cases, the amplitude noise is negligible or unimportant. Unfortunately, frequency (or phase) noise has much more harmful effects [1]. This frequency noise can be seen as a random variation of the zero crossing points (jitter) of the oscillator signal in the time domain, and as a consequence, can be expressed as $x(t)=A\cos\left(\omega_o t+\phi_n(t)\right)$ where $\phi_n(t)$ is called phase noise and takes into account the random variation of the frequency generated by the noise sources. If

$\phi_n(t)<<1$, then $x(t)=A\cos(\omega_o t)-A\phi_n(t)\sin(\omega_o t)$, and the spectrum of $\phi_n(t)$ is translated around $\pm\omega_o$. In the previous expression it should be noted that the phase noise is added in quadrature with the oscillator signal, an essential characteristic of the phase noise.

Thus, the output spectrum of a real oscillator consists in a noisy skirt around the oscillator frequency (fig. 2-1a). To quantify the oscillator phase noise, the power in a 1 Hz bandwidth at an offset $\Delta\omega$ from the carrier is calculated and then normalized to the average carrier power. Consequently, it is expressed in dBc (dB referred to the carrier).

Now, let us see how this noise skirt limits the ability of a RF system to refuse nearby interferers. Assume that the input signal of a receiver consists of an interferer (as an adjacent channel) close to the wanted signal. An ideal oscillator will translate these signals without modifying their shapes. However, in presence of the phase noise, both signals will overlap after the frequency translation and hence, the interferer will inevitably corrupt the wanted signal. Moreover, after the down-conversion, the overlapped region can not be removed from the wanted signal using filtering techniques. This phenomenon is illustrated in figures 2-1b and 2-1c.

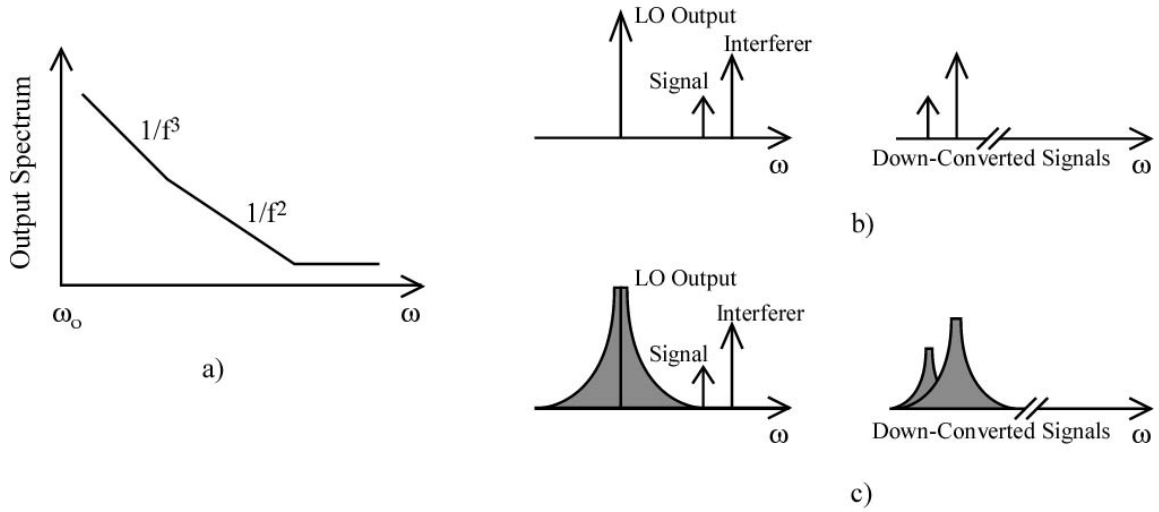

Figure 2-1. a) Oscillator output spectrum around the carrier frequency b) Down-Conversion by an ideal oscillator c) Down-Conversion by a noisy oscillator (reciprocal mixing)

The tight requirements on the oscillator phase noise performance are due to the extreme proximity between adjacent channels in the modern communication systems. Since the difference between these channels can be as small as tens of kilohertz, while each of

them is around a carrier frequency of 900 MHz or 1.8-1.9 GHz, the output spectrum of the oscillator must be extremely sharp. Figure 2-2 shows the phase noise requirements imposed by the GSM standard, nowadays probably the most used worldwide.

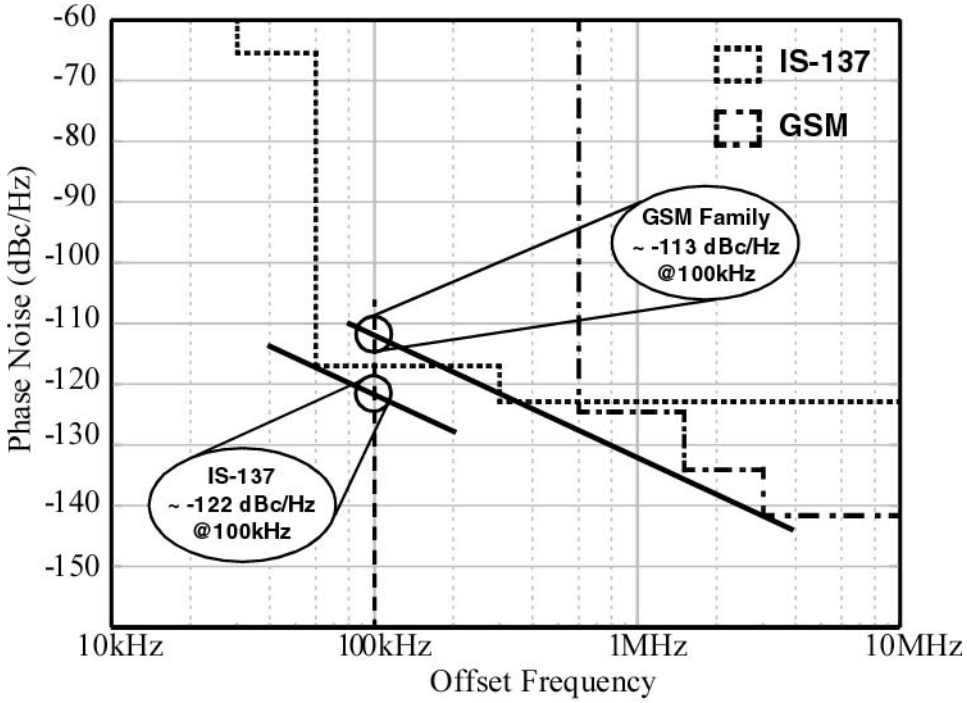

Figure 2-2. Phase Noise requirements for the GSM and IS-137 standards[2]

The phase noise also affects directly frequency or phase modulated signals since after the down-conversion the phase noise spectrum is superimposed to the wanted signal degrading the SNR.

Besides the phase noise, the tunning range is also a fundamental characteristic in the oscillator performance. Most of the oscillators used in communications systems are variable oscillators. Strategies as frequency hopping (where the carrier is moving around a fixed frequency following a pseudo-random pattern) or systems having different frequencies for the transmitter and the receiver may explain this interest in a large tuning range. Moreover, even if fixed oscillators are desired, a frequency-tunning element may be used to compensate any frequency deviation over its nominal value due to the parametric variations in fabrication process or temperature drifts.

[2] Extracted from "A 900 MHz Local Oscillator using a DLL-based Frequency Multiplier Technique for PCS Applications", G.Chien, and P.R.Gray at http://kabuki.eecs.berkeley.edu/~gchien/slides/ isscc00/isscc2KslidesC.pdf.

When an oscillator is designed for low phase noise, the tuning range is also an important parameter to consider. To achieve low phase-noise, the oscillator amplitude must be maximized. This means either increasing the biasing current or the tank inductance (assuming a given quality factor). The former increases the power consumption, the latter reduces the frequency tunning range. Therefore, it exists a trade-off between low phase noise, high tunning range and power consumption.

The tunning element used in integrated oscillators is the varactor. This device acts as a variable capacitor modifying its capacitance depending on the dc voltages applied to its terminals. Currently, in standard Bipolar or BiCMOS technologies, varactors are realized as junction diodes (reverse biased) [2],[3] or as MOS varactors [4],[5]. The varactor performance is characterized by two parameters, the capacitance ratio (C_{max}/C_{min}) and the quality factor. The former has a direct influence on the oscillator tunning characteristics since the tunning range is limited by:

1) The ratio between the fixed (parasitic) capacitances and the varactor capacitance.
2) The voltage-frequency characteristics of the varactor (capacitance ratio).

In the low GHz frequency range, varactors shown quality factors considerably higher than inductors and hence they have a light influence on the oscillator phase noise performance. However, for frequencies of 10 GHz and above, the quality factor of the varactors can seriously limit the resonator performance [6] and consequently, the oscillator phase noise.

In this chapter, we investigate the design of oscillators having low phase noise and large tunning range. Thus, section 1 revises the phase noise theory and the state of the art of integrated oscillators and identifies the quality factor of the resonator as one of the main factors limiting their phase noise performance. Section 2 introduces a novel transformer-based resonator, which overcomes the performance of the common inductor-based resonators in terms of tuning range and effective quality factor. The properties of this resonator are then analyzed from a circuit perspective, and the even/odd operation modes are examined. The extension of the parallel design to N-resonators is also shortly discussed. Section 3 analyzes the transformer-based resonator in the EM domain and section 4 compares its performance (quality factor) with the standard inductor-based resonator. At this point, eddy currents are identified as the main

factor limiting the effective quality factor of the transformer-based resonator. Section 5 applies a layout optimization technique to improve the quality factor of integrated inductors. Then, this technique is extended to the optimization of integrated transformers. As a result, an equivalent inductor of 11 nH with an effective quality factor as high as 25 at 1.7 GHz is obtained.

Finally, section 6 shows the design and the implementation of the parallel high-Q resonator in a 1.7 GHz oscillator using the Conexant BC35 CMOS process. The VCO core consumes 4.5 mA of current from a 2.5 V supply, and results in a phase noise of -137, –142 and –152 dBc/Hz at 600K, 1 MHz and 3 MHz from the carrier, respectively. The tuning range is 107 MHz for a tuning voltage range of 0-2.5V. The measured phase noise of the 1.7 GHz CMOS oscillator results in –152 dBc /Hz at 3 MHz from the carrier, which is a state-of-the-art performance using integrated resonators.

2.1 Phase Noise Theory

Fig. 2-1a shows the typical output spectrum of a real oscillator at frequencies close to the carrier, where three different regions can be identified. The first region, the closest to the carrier, follows a dependence of $1/f^3$ and is due to the up-conversion of the 1/f noise of the active devices used to build the oscillator. The second region has a $1/f^2$ dependence and is related to the shaping of the thermal noise by the oscillator resonator. Finally, a flat response is observed for high frequency offset from the carrier and can be associated to the noise floor of the test system.

Circuit designers required a theory able to explain this output spectrum and relate it to circuit parameters in order to optimize the oscillator performance. In 1966 Leeson presented a phase noise theory based on a linear model of an LC resonator in the steady-state oscillation through the application of either feedback or a negative conductance [7]. Most of the details involved in Leeson's model are retained by the following expression for the power spectral density of the oscillator:

$$L(\omega_m)=\frac{4FkTR}{V_o^2}\left(\frac{\omega_o}{2Q\omega_m}\right)^2 \qquad \textbf{(2.1)}$$

where k is the Boltzman constant, T is the absolute temperature, R and Q are the oscillator impedance and quality factor at the resonant frequency ω_o respectively and ω_m is the offset frequency from the carrier. (2.1) contains an unspecified noise factor F that prevents to predict the phase noise if no further analysis is performed. In spite of its simplicity, this model already pointed out the dependence of the phase noise with the oscillation amplitude and the resonator quality factor. Thus, the great majority of RF oscillators today are implemented using high quality resonators outside the chip containing the active devices. This also explains the important efforts of the IC research community to improve the quality of the integrated passive inductors.

A legacy, product of a wrong interpretation of the Leeson expression, is the concept of the active inductors [8,9,10]. The transfer function of an inductor can be implemented using only transistors (and their parasitic capacitances) through a circuit known as gyrator resulting in very high values of Q (as high as 600). Nevertheless, all the attempts to minimize the oscillator phase noise using active inductors done in the past have failed. Nowadays, it is well known that the noise of the active devices used to build the active inductor as well as their non-linearities increase dramatically the noise factor F in (2.1). Thus, the expected phase noise improvement due to their high Q is not achieved in practical implementations. Still, there is some research going on in active inductors, since their small area compared to their passive counterparts make them very attractive. However, at the moment, no oscillator using active inductors and achieving a phase noise performance comparable to the oscillators based on their passive counterparts has been reported.

Leeson's model has been the most popular model for phase noise in the last 30 years, but Q.Huang and Hajimiri have presented recently much more exhaustive phase noise models [11],[12],[13]. These models consider the essential non-linear (or time variant) nature of the oscillators and avoid non-rigorous linear approaches and allow the calculation of closed forms for the noise factor unspecified by Leeson. Moreover, the noise is supposed to be added to the carrier waveform in the time domain rather than directly in the carrier phase, and as a consequence, no amplitude gain control has to be invoked to remove amplitude noise.

According to this approach, the phase noise analysis should be split into two steps. In the first step, the non-linear steady-state response of the oscillator has to be found. Then, the noise sources can be added to this steady-state solution as perturbations. Since the steady-state waveform retains all the non-linearities present in the circuit, after the addition of the noise sources appear mixing products and hence, noise up-conversion from frequencies close to dc and noise down-conversion from frequencies around the oscillator harmonics.

Using this methodology, some authors have developed closed expressions for the noise factor included in the Leeson's expression for several oscillator topologies that take into account the above mentioned noise up/down-conversions. It should be noted that these expressions are just valid for the thermally induced noise, that is, in region where noise goes as $1/f^2$. Some additional variations have to be applied to the Leeson expression in order to capture the $1/f^3$ and flat regions [14].

Along with the better understanding of the different mechanisms responsible of the phase noise summarized in the previous discussion, other advances have allowed the improvement of the performance of the oscillators using LC integrated resonators:

1) The accuracy of modern non-linear tools and transistor models used to predict the oscillator performance [15].
2) The better quality of CMOS transistors (lower channel noise, higher fmax and ft, etc.).
3) The increased quality factor of integrated inductors built using a 2-3 um-thick top metal layer placed over a 2-3 um thick oxide layer over the silicon substrate.

Thus, Tiebout built a 1.8 GHz quadrature CMOS oscillator, which exploited the magnetic coupling between the inductors in the resonating tank, and achieved –143 dBc/Hz at 3 MHz from the carrier [16]. Hegazi et al. used a filtering technique at the second harmonic to reduce the injected noise in the oscillator, and for a 1.1 GHz oscillator, achieved a phase noise of –153 dB/Hz at 3 MHz from the carrier [17]. Kucera used exclusively pMOS transistors for lower flicker noise, and with a bond-wire inductor, achieved a 2.05 GHz oscillator with a phase noise of –128.5 dBc/Hz at 600 KHz from the carrier [18]. Zannoth used an inductive feedback so as to connect a low impedance bias source at the base of the active bipolar transistors [19]. This eliminates resistive elements, which result in white noise that could be converted to phase noise by

the non-linear devices. The 2.0 GHz VCO achieved a phase noise of –136 dBc/Hz at 4.7 MHz from the carrier. In this work, we present a new oscillator design, compatible with the previously mentioned techniques and based on an integrated transformer that allow us to extend the tuning range and reduce the oscillator phase-noise.

2.2. Circuit Analysis of the Transformer-Based (Parallel) Resonator

2.2.1 Electrical Analysis

A simplified transformer model consisting of two inductors, L_1 and L_2, with a mutual inductance M and two series resistors, r_1 and r_2, is used in the circuit analysis (fig. 2-3). The magnetic coupling between the spirals can also be expressed by the coupling factor, k, through:

$$M = k\sqrt{L_1 L_2} \tag{2.2}$$

This simple model neglects the transformer parasitics as the capacitive coupling with the substrate and between spirals as well as the substrate losses. These effects will be considered in sections 3 and 4 using electromagnetic simulations. Still, this model allows us to obtain some insight into the transformer behavior as an integral part of the novel resonator.

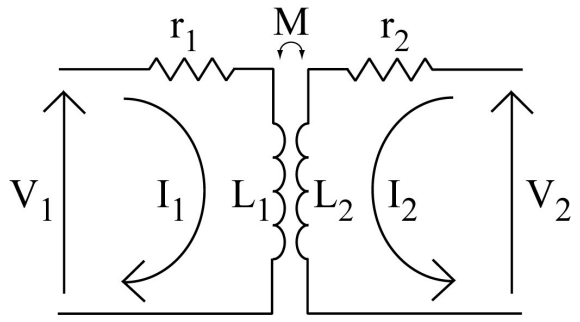

Figure 2-3. Simplified electrical model of an integrated transformer

The relation between currents and voltages in the transformer is given by (see fig. 2-3):

$$\begin{aligned} V_1 &= jL_1\omega I_1 + jM\omega I_2 + r_1 I_1 \\ V_2 &= jM\omega I_1 + jL_2\omega I_2 + r_2 I_2 \end{aligned} \tag{2.3}$$

The proposed transformer-based resonator and the standard inductor-based resonator are shown in fig. 2-4, where the input impedances are defined as Z_{in}^{Transf} and Z_{in}^{Ind}, respectively. The capacitors C_1 and C_2 are added to both sides of the transformer in order to obtain the novel resonant tank. These input impedances can be calculated applying basic circuit analysis, resulting in:

$$Z_{in}^{Ind} = \frac{r_s + jL_s\omega(1 - L_sC_s\omega^2) - jrC_s\omega}{(1 - L_sC_s\omega^2)^2 + r_s^2C_s^2\omega^2} \tag{2.4}$$

$$Z_{in}^{Transf} = \frac{(M^2 - L_1L_2)\omega^2 + \frac{L_1}{C_2} + r_1r_2 + j(L_1r_2\omega + L_2r_1\omega - \frac{r_1}{C_2\omega})}{r_2 - C_1\omega(L_1r_2\omega + L_2r_1\omega - \frac{r_1}{C_2\omega}) + j[C_1\omega((M^2 - L_1L_2)\omega^2 + \frac{L_1}{C_2} + r_1r_2) + L_2\omega - \frac{1}{C_2\omega}]} \tag{2.5}$$

In particular, three different characteristics should be analyzed to define the resonant tank performance: the resonant frequency, and the corresponding peak impedance and phase slope. The resonant frequencies are found from (2.4) and (2.5) using $\mathrm{Imag}(Z_{in})=0$. For the values of inductance, capacitance and resistance common in integrated resonators, the resistors r_1 and r_2 have a negligible influence on the resonant frequency and can be neglected in the calculations.

In the inductor-based resonator, the resonant frequency is given by:

$$\omega_1^2\Big|^{Ind} = \frac{L_s - r_sC_s}{L_s^2C_s} \approx \frac{1}{L_sC_s} \tag{2.6}$$

The transformer-based resonator results in two resonant frequencies, ω_1 and ω_2 given by:

$$\omega_{1,2}^2\Big|^{Transf} = \frac{-(L_1C_1 + L_2C_2) \pm \sqrt{(L_2C_2 + L_1C_1)^2 + 4C_1C_2(M^2 - L_1L_2)}}{2C_1C_2(M^2 - L_1L_2)} \tag{2.7}$$

where the sub-index 1 corresponds to the plus sign and sub-index 2 corresponds to the minus sign. For a symmetric transformer-based resonator with $L_1=L_2=L$, $C_1=C_2=C$, and $r_1=r_2=r$, the resonant frequencies are:

$$\omega_1^2\Big|^{Transf} = \frac{1}{(L+M)C} \qquad \omega_2^2\Big|^{Transf} = \frac{1}{(L-M)C} \tag{2.8}$$

and in the case of k→1 (or when M→L), ω_1 will tend to $\omega_1 = \frac{1}{\sqrt{2LC}}$ and ω_2 will tend to infinity. Also, it should be noted that (2.7) is symmetric concerning sub-index 1 and 2, and for a non-symmetric transformer with $L_1 \neq L_2$, the same resonant frequencies will be observed from both sides of the transformer.

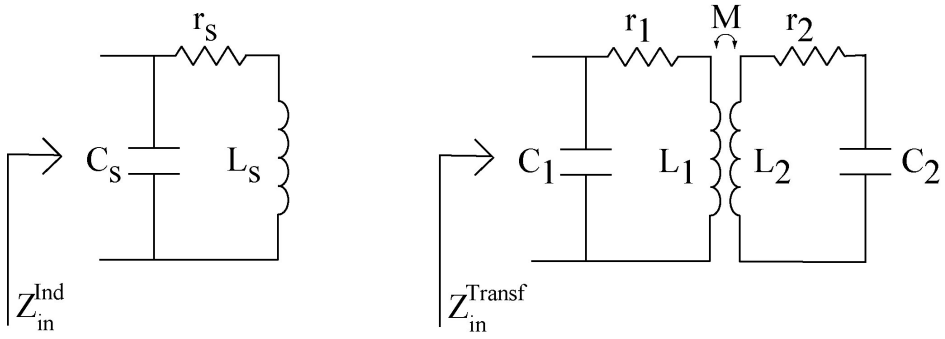

Figure 2-4. Standard inductor-based resonator and the novel transformer-based resonator

The peak impedance at the resonant frequencies can be found substituting (2.7) and (2.8) in (2.4) and (2.5), respectively, resulting in:

$$Z_{in}(\omega_1)\Big|^{Ind} \approx \frac{L_s}{r_s C_s} = \frac{(\omega L_s)^2}{r_s} = Q^2 r_s \qquad \textbf{(2.9)}$$

$$Z_{in}(\omega_1)\Big|^{Transf} \approx \frac{L+M}{2rC} \qquad Z_{in}(\omega_2)\Big|^{Transf} \approx \frac{L-M}{2rC} \qquad \textbf{(2.10)}$$

where Q is the quality factor of the inductor in fig. 2-4 ($Q = \frac{\omega L_s}{r_s}$) or of the primary (or secondary) of the transformer.

It should be noted that for the peak impedance the transformer acts as an inductor of value L+M (2L for k=1) with a series resistance 2r at ω_1, and as an inductor of value L-M and a series resistance 2r at ω_2. As a result, the resonator will show better performance at ω_1 since its quality factor is much higher than at ω_2.

The performance of the transformer–based resonator is now compared to an equivalent standard inductor resonator using the phase slope around ω_1. The phase slope around the resonance frequency is an accurate parameter for resonators since the quality factor, if defined as the ratio between the real and imaginary parts of the impedance, will be

zero at this frequency. Consider a symmetric transformer with $L_1=L_2=L$, each with a quality factor Q (or equivalently with a resistor r) and with a coupling factor, k=1. The phase slope of the impedance at the resonance frequency can be calculated using:

$$\theta = \tan^{-1}\frac{\mathrm{Im}(Z_{in})}{\mathrm{Re}(Z_{in})} \tag{2.11}$$

and differentiating with respect to ω:

$$\left.\frac{d\theta}{d\omega}\right|^{Transf}_{\omega=\frac{1}{\sqrt{(L+M)C}}} = \frac{2(L+M)+r^2C}{r+\frac{r^3C}{2L}} \qquad \left.\frac{d\theta}{d\omega}\right|^{Ind}_{\omega=\frac{1}{\sqrt{LC}}} = \frac{2L+r^2C}{r+\frac{r^3C}{L}} \tag{2.12}$$

and:

$$Q = -\frac{\omega}{2}\left.\frac{d\theta}{d\omega}\right|_{\omega=\omega_o} \tag{2.13}$$

For the values used in planar resonators, the terms r^2C and r^3C/L can be neglected in (2.12). Thus, the transformer-based resonator basically doubles the Q when compared to the inductor-based resonator. The impedance of two different resonators are compared in fig. 2-5 for the case of $L_s=L_p=L=5.5$ nH, Q=10, k=1, C= 0.9 pF, and $f_o=1.7$ GHz. It is seen that the transformer-based resonator results in the same peak impedance (i.e, similar power consumption) as the 2L-inductor resonator (as expected), but with double the effective resonator Q. In actual implementations, and as a result of the non-perfect magnetic coupling between the spirals (k<1), the equivalent inductance of the transformer-based resonator is lower than 2L, and the effective transformer-based quality factor is less than 2Q. In general, $Q_{eff}=(1+k)Q$.

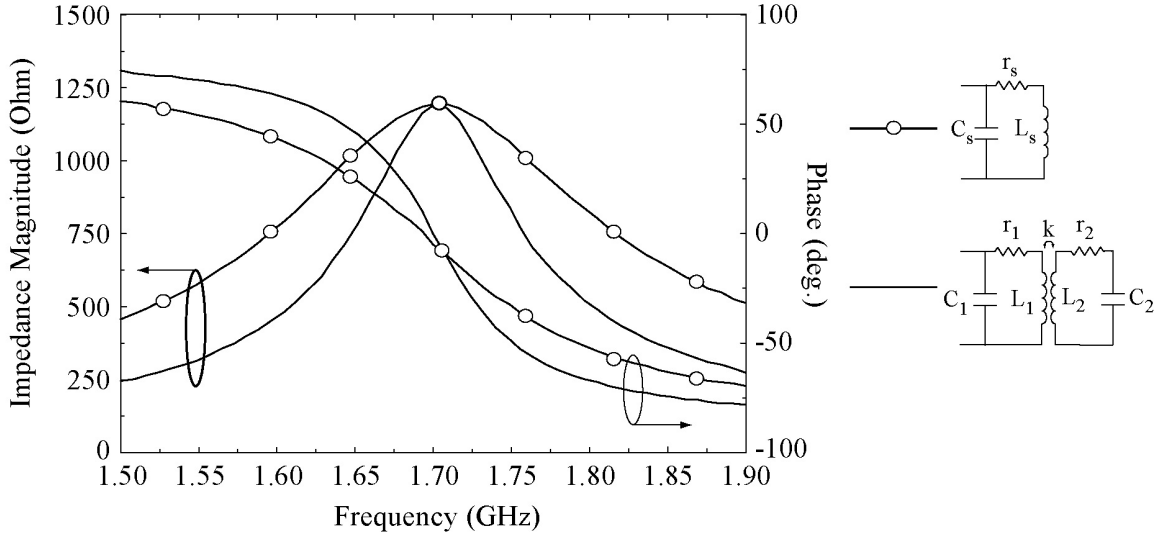

Figure 2-5. Impedance of the transformer-based resonator with $L_p=L_s=5.5$nH, $Q_p=Q_s=10$ and k=1 (solid) vs. a standard LC resonator with L=11 nH and Q=10 (symbols)

Concerning fig. 2-5, it is important to remark that the transformer-based resonator results in a sharper impedance (which results in a better phase noise performance) but does not reduce the power consumption of an oscillator (since both resonators have the same peak impedance).

The extension of the 2 coupled-inductors to N-coupled inductors is straightforward. The equivalent inductance L_{eq} and quality factor Q_{eq} of the resulting resonator would:

$$L_{eq} = [1+(N-1)k]L$$
$$Q_{eq} = [1+(N-1)k]Q$$

where L and Q are the inductance and the quality factor of the individual inductors, respectively. Also, as was already seen, the total loading capacitance of the N-parallel resonator is Nx higher (for k=1) than the capacitance of the single inductor resonator, thereby reducing the effect of the transistor, transformer and interconnect parasitic capacitances.

However, the practical implementation of N-coupled resonators presents some drawbacks. For a fixed value of inductance to be synthesized, the value of each individual inductor lowers with N, and smaller inductors result in a lower coupling factors and quality factors.
Moreover, if the number of coupled resonators is increased, additional resonant frequencies based on even/odd modes could appear and could cause instability problems. In section 5, we will show practical implementations of N-coupled resonators (with N>2) and their properties.

2.2.2 Even-Odd Mode Analysis

The even-odd mode analysis offers additional insight into the transformer-based resonator and points out the influence of symmetry on the resonator properties. Let us consider the transformer-based resonator as a general two-port network (notice that the 2-port includes the capacitors) characterized by an impedance matrix:

$$\begin{aligned} V_1 &= Z_{11}I_1 + Z_{12}I_2 \\ V_2 &= Z_{21}I_1 + Z_{22}I_1 \end{aligned} \qquad \textbf{(2.14)}$$

where $Z_{12}=Z_{21}$ due to the reciprocity. The parameter Z_{11}, also referred as Z_{in}, is the input impedance and was calculated in (2.5). Fig. 2-6 shows that the transformer-based resonator excited only from the primary can be analyzed as the superposition of two different modes, the common mode and the differential mode. In this analysis, current sources instead of voltage sources are used since they are more suitable for transformer analysis.

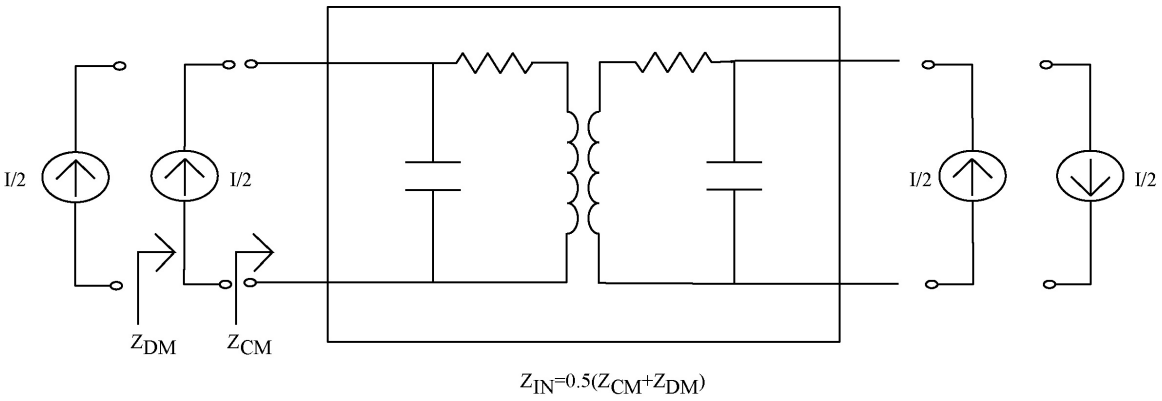

Figure 2-6. Analysis of the input impedance of the transformer-based resonator in terms of the even/odd impedances

The common-mode impedance Z_{CM} is ($I_1=I_2=I_{CM}$):

$$Z_{CM}=\frac{V_{CM}}{I_{CM}}=Z_{11}+Z_{12} \tag{2.15}$$

The differential mode impedance Z_{DM} is ($I_1=I_{DM}$ and $I_2=-I_{DM}$):

$$Z_{DM}=\frac{V_{DM}}{I_{DM}}=Z_{11}-Z_{12} \tag{2.16}$$

and the input impedance of a general two-port network can be written as:

$$Z_{11}=\frac{1}{2}(Z_{CM}+Z_{DM}) \qquad Z_{12}=\frac{1}{2}(Z_{CM}-Z_{DM}) \tag{2.17}$$

Again, analytical expressions for Z_{CM} and Z_{DM} can be found using circuit techniques and are:

$$Z_{CM}=\frac{\omega^2(M^2-L_1L_2)+r_1r_2+\frac{L_1+M}{C_2}+j\omega(L_1r_2+L_2r_1)-j\frac{r_1}{C_2\omega}}{(1-\omega^2L_1C_1+j\omega C_1r_1)(j\omega L_2+r_2+\frac{1}{jC_2\omega})+j\omega^3M^2C_1} \tag{2.18}$$

$$Z_{DM} = \frac{\omega^2(M^2 - L_1L_2) + r_1r_2 + \frac{L_1 - M}{C_2} + j\omega(L_1r_2 + L_2r_1) - j\frac{r_1}{C_2\omega}}{(1 - \omega^2L_1C_1 + j\omega C_1r_1)(j\omega L_2 + r_2 + \frac{1}{jC_2\omega}) + j\omega^3M^2C_1} \quad \textbf{(2.19)}$$

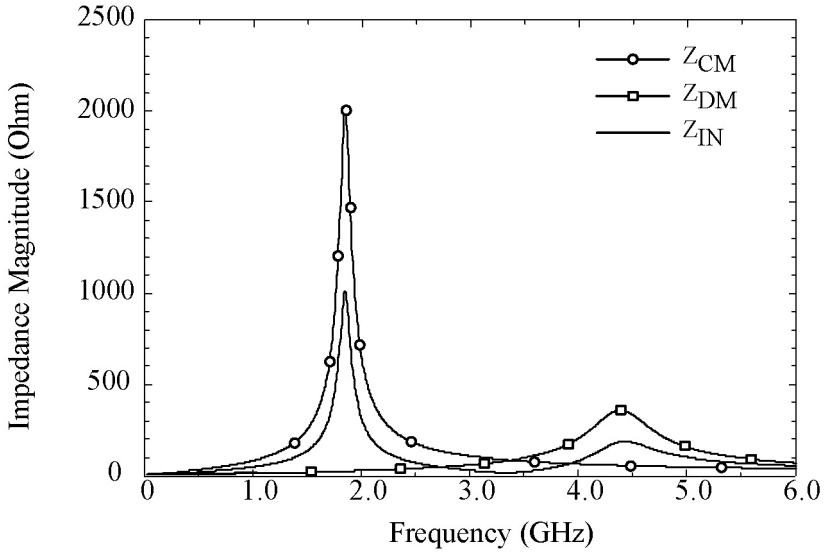

Figure 2-7. Comparison of the transformer-based resonator impedance: a) Input impedance (solid line) b) Even impedance (circles) c) Odd impedance (squares)

Figure 2-7 shows the input impedance as well as the common and differential mode impedances for the transformer-resonator of fig. 2-4 where k has been changed from 1 to 0.8 in order to observe the differential resonance. The resonant frequencies of the input impedance, ω_1 and ω_2, match the resonant frequencies of the common and differential mode impedances, respectively (this can also be proved using (2.18) and (2.19)). Also, at ω_1, $Z_{in} \approx Z_{CM}/2$ since Z_{DM} is much lower than Z_{CM}. Actually it could be established that for a symmetric transformer embedded in the resonator of fig. 2-6, at ω_1, the currents (and voltages) in the primary and the secondary are equal and generate magnetic fields that are added constructively.

2.3 EM Analysis of the Transformer-Based (Parallel) Resonator

In the previous section, we have used a simple transformer model to simplify the analytical calculations. In this one, EM simulations will be used to verify the accuracy of this model at 0.1-3 GHz and will be applied to a specific layout used later in the

oscillator design. The EM simulator is the MoMemtum planar solver, which is embedded in the ADS design environment (Agilent Technologies). The simulation includes a complete layer description of the BC35 CMOS (Conexant) technology. The transformer consists of two closely-coupled loops of five and six turns respectively with a strip width of 8 µm, a turn-to-turn spacing of 2 µm and an outer dimension of 250 µm. It was implemented using the top metal with a sheet resistance of 10 mΩ/sq., and is separated from the 8 Ω-cm silicon substrate by a silicon-dioxide layer of 4 µm (fig. 2-8). The under-crossings were realized as a parallel connection of the lower metal levels.

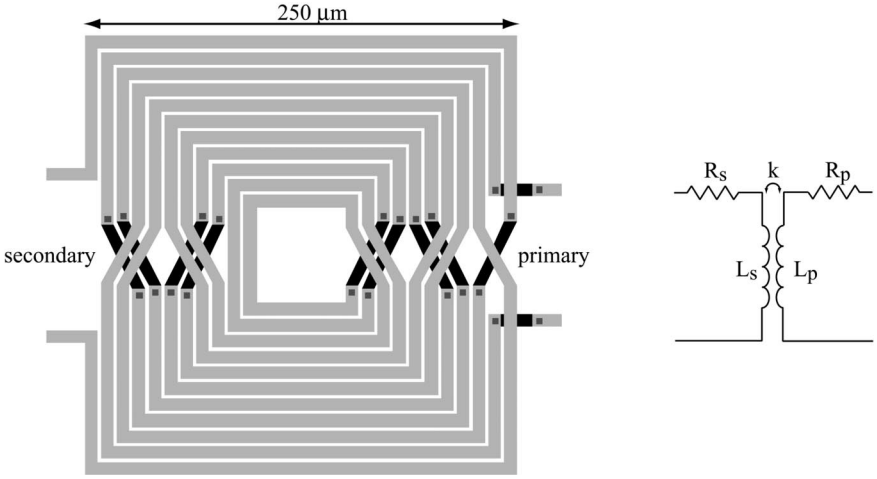

Figure 2-8. The integrated transformer with L_p=5.5 nH, L_s=7 nH, k=0.83 and Qp≈Qs≈10 at 1.7 GHz

From the EM simulation results, it is possible to extract a simplified electrical model of the transformer suitable at 0.1-3 GHz where the capacitive parasitics can be neglected. Also, in this model, all the component losses (substrate and metal strips) have been summarized in the series resistor. The EM analysis is fitted with Lp=5.5 nH, Ls=7 nH, a series resistance of rs_1=5.5 Ω, rs_2= 6.5 Ω (low frequency values), and a coupling factor of k=0.83 (fig. 2-8). The measured scattering parameters of the transformer in the range of 50 MHz to 3 GHz were obtained using a vector network analyzer calibrated with the line-reflection-match (LRM) method. Additional test elements were also measured for pad de-embedding purposes. The S-parameters match closely the simulated results in the 0.1-3 GHz range (fig. 2-9).

The transformer model uses a fixed resistor to take into account the component losses. It should be noted that the reactance of the 5.5 nH inductor at 1.7 GHz is close to 60 Ω,

which is compared with the resistive value of just 5.5 Ω. Therefore, variations in the resistance value at 1.7 GHz due to the eddy currents in the metal strips or to displacement currents in the substrate can be easily masked when fitting the model to EM simulations.

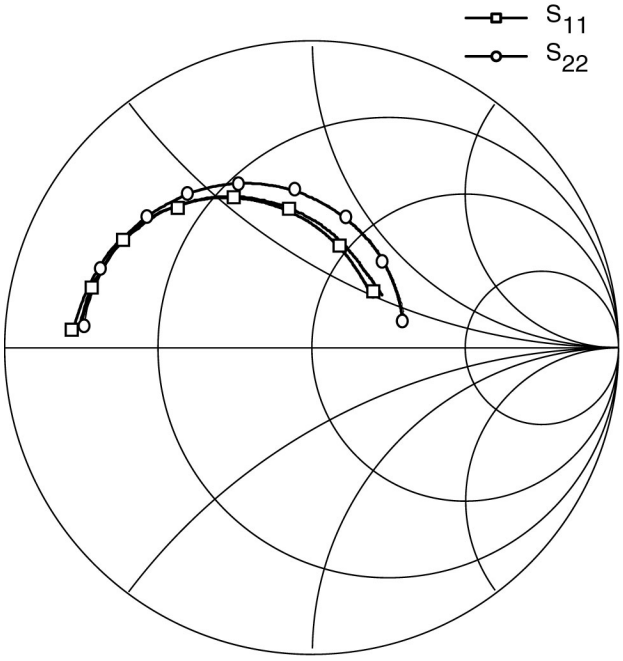

Figure 2-9. Measured vs simulated reflection parameters of the integrated transformer (0.1-3 GHz)

This increment of the resistance (typically 20-40% depending on the inductance value and strip width) can be neglected in many transformer applications where the transformer works basically as a power transferer. Nevertheless, it becomes important in the transformer-based resonator performance since it limits the resonator Q. Recently, analytical expressions for the series resistance of integrated inductors, that neglect substrate effects and take into account the influence of eddy currents, have been reported [20-21]. Similar expressions are not still available for integrated transformers, and as a consequence the analysis of the frequency dependent losses for these structures requires the use of e-m tools.

To evaluate the influence of eddy currents at 1.7 GHz in the metal strips (current crowding effects) and the substrate, the transformer was simulated under different conditions to point out the relative loss contributions at the design frequency. In the first simulation, the silicon substrate is substituted by air, and the transformer is meshed in simple cells. Consequently, the influence of eddy currents in metals strips or in the

substrate is not taken into account, and only the ohmic component contributes to the loss. In the second simulation (still using an air substrate), an edge mesh is used which takes into account the influence of the current redistribution along the strip width. This simulation considers magnetically induced losses in the strips but not the substrate losses. Finally, a third simulation is done using a silicon substrate with a resistivity of 8Ω-cm, and a refined mesh. This case presents the entire loss of the transformer.

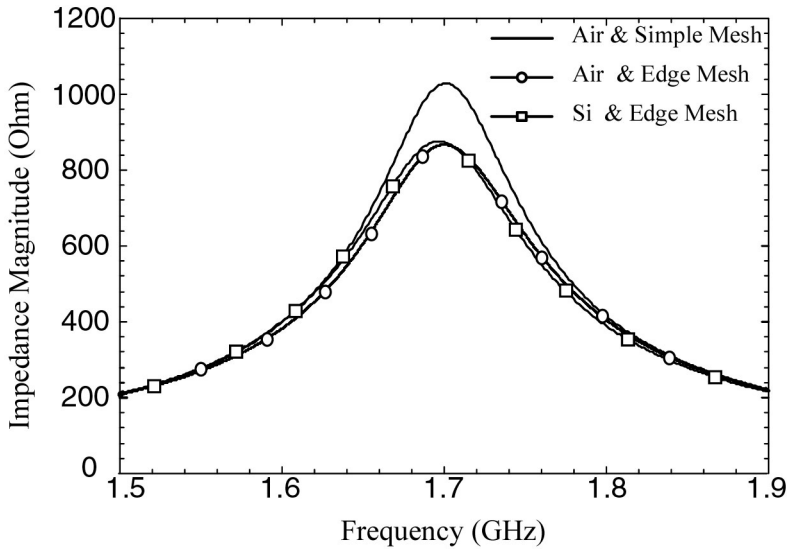

Figure 2-10. Impedance of transformer-based resonator. The transformer is simulated under different conditions to observe the different contributions (metal strips and substrate) to the components losses

The transformer results are then placed in a circuit simulator to obtain the resonator performance with zero-loss capacitors (fig. 2-10). It is seen that, using the BC035 CMOS technology, at 1.7 GHz the contribution to the losses of the eddy currents in the metal strips is much higher than the electric losses or eddy current losses in the 8 Ω-cm substrate. Also, the equivalent series resistance in the primary and secondary loops of the transformer can be obtained from the peak resonator impedance using (2.9) and is rs_1=6.3 and rs_2=7.5 Ω at 1.7 GHz. This is an increase of around 10-15% percent over the DC series resistance of rs_1=5.5 Ω and rs_2=6.5 Ω. Although the resonator shows different peak impedance from each side, it shows the same impedance shape (or phase slope). Thus, one can deduce that the effective Q of the transformer-based resonator is 17 at 1.7 GHz.

Quality factors lightly lower than 17 (fig. 2-12) can be achieved in this technology using standard inductors with optimum width. Therefore, the expected improvement in the effective quality factor due to the transformer use is not apparently observed. Next section addresses this issue.

2.4 Comparison between Series and Parallel Resonators

So far, in our comparison between the inductor and the transformer-based resonators, we have assumed the same quality factor for any inductor independently of its inductance value (fig. 2-5). However, in practical implementations it is well known, the larger the inductance value, the larger the quality factor. We have also assumed (wrongly) than the coupling does not modify the quality factor of each individual inductor. A fear comparison of the inductor and transformer-based resonators must include all the geometry and frequency dependent phenomena and hence requires the use of EM tools (in absence of accurate equivalent electric models). This section intends to perform this comparison and quantify, in practical implementations, the actual improvement of quality factor achieved by the transformer-based topology.

Figure 2-11 shows once again the inductor and the transformer-based resonators and their respective layouts. Let us apply now a differential excitation to these resonators (as it occurs in many oscillator designs). For a symmetrical inductor layout, the corresponding resonator has a symmetry plane and the capacitor C_s can be split into two capacitors of $2C_s$ each one connected in parallel with L_s. Therefore, the inductor-based resonator can be seen as the series connection of two resonators constituted by an inductor of value L_s+M_s, a series resistance r_s and a capacitor of $2C_s$. This is why the inductor-based resonator can be also called series resonator. Instead, in section 2, we have seen that for a symmetric transformer layout the currents and voltages at the primary and the secondary are equal at the resonance. Thus, the transformer-based resonator can be seen as the parallel connection of two uncoupled resonators constituted by an inductor of value L_p+M_p, a series resistance r_p and a capacitor C_p. Actually, each one of these parallel resonators can be seen indeed as the series connection of two resonators.

Due to the connection between the inductors in the series resonator, the total equivalent inductance is $Leq_s=2(L_s+M_s)$ as compared to $Leq_p=(L_p+M_p)$ for the parallel resonator. For the same equivalent inductance and in order to obtain the same resonant frequency, C_p should be equal to C_s, and the parallel resonator will employ 2x the capacitance of the series resonator (C_p in both windings). This larger capacitance lowers the effect of the parasitic capacitances of the transistors, and is therefore more suitable for a large tuning range.

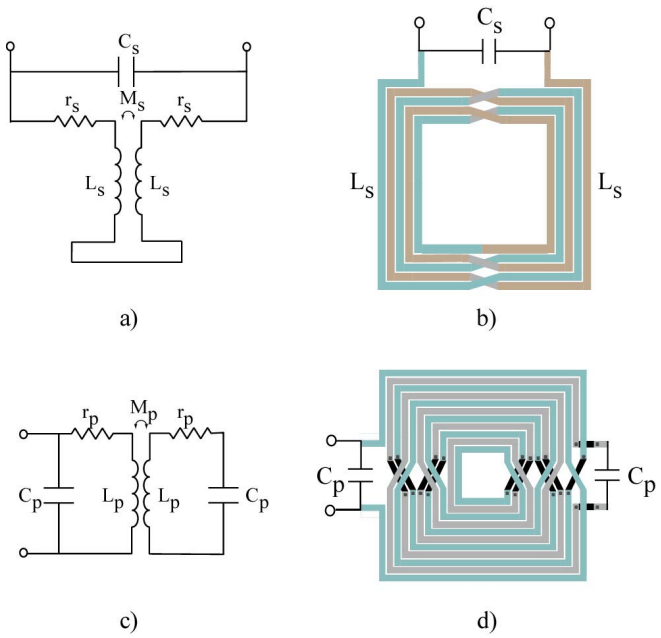

Figure 2-11. Inductor (series) vs. transformer (parallel) based resonators and their respective layouts

The previous analysis has already pointed out that the standard inductors exploit the magnetic coupling to increase their resonator quality factor. Actually, the equivalent inductance $Leq_s=2(L_s+M_s)$ has theoretically a quality factor twice than the single inductors L_s (if k=1 is assumed). The practical values of k ranging from 0.5 to 0.8 reduce this improvement. As a result of this discussion, some authors have claimed that a symmetric inductor differentially driven overcomes the performance of two identical (uncoupled) inductors in terms of oscillator phase noise (inductor quality factor) and area consumption [22-23]. We will demonstrate later than the improvement achieved in the quality factor maybe marginal but the area reduction and the symmetry still remain as advantages of the differentially driven symmetric inductors.

A close look at the transformer of fig. 2-11d shows that the transformer is actually composed of two of these symmetric inductors nested within each other and as a consequence, strongly coupled. In section 2, we have deduced theoretically that the transformer-based resonator increases the effective quality factor by kQ. Actually, EM simulations show that if eddy currents are neglected (using a simple mesh) this improvement is achieved. However, if eddy currents are considered, the expected improvement is considerably reduced because after the coupling the quality factor of the inductors constituting the transformer is noticeably degraded (when compared to a single isolated inductor).

This degradation of the quality factor of the transformer primary or secondary is caused by the increment of the losses generated by the eddy currents. In particular, two additional contributions to these losses can be identified:

1) The magnetic field generated by the primary induces eddy currents in the secondary (even if the secondary is kept in open circuit).
2) Since eddy currents are proportional to the square of the overall magnetic field, the magnetic field generated by the current flowing in the secondary (added constructively to the magnetic field generated by the primary) also increases the eddy currents in the primary.

To identify clearly these additional losses and evaluate their magnitude, the transformer analyzed in section 3 has been simulated under different conditions. In the first simulation, the transformer is meshed in simple cells, and therefore only ohmic losses are considered. Then, the primary (secondary) is meshed using a refined mesh but the secondary (primary) is removed. This corresponds to the primary or the secondary acting as isolated inductors. Later, the whole transformer is meshed using a refined cell but the primary or the secondary are kept in open circuit. In this situation, no current can flow across the spiral in open circuit but still it is possible to induce eddy currents on it degrading the quality factor of the other spiral. Finally, the whole transformer is simulated with currents flowing across the primary and the secondary. This presents the entire loss of the transformer. The obtained results are summarized in the next table.

	Q Simple Mesh	Q Refined Mesh wt Prim/Sec	Q Refined Mesh with Prim/Sec in Open Circuit	Q Refined Mesh[3]
Primary	13.2	11.6	11.0	8.90
Secondary	12.1	11.0	10.5	7.87
Transformer	23.0	----	----	16.5

Table 2.1 Degradation of the inductor quality factor due to different contributions of the eddy currents at 1.7 GHz

Data indicates that for this particular case eddy currents lower the quality factor of the isolated primary or secondary by approximately 10% and that this percentage is increased to almost 35% when currents flow through the primary and the secondary. Thus, in the expression of the effective quality factor $Q_{eff}=(1+k)Q$ the values of Q of the primary or the secondary to consider are the corresponding to the fourth column of table 2.1 instead of the corresponding to the second column. This reduces the effective quality factor of the resonator from the theoretical 20.7 (calculated using the average quality factor of column 2 in table 2.1) to the actual 16.5.

There is still an additional aspect to consider in the comparison between both resonators. As we have already mentioned and it is shown in fig. 2-12, the larger the inductance value, the larger the quality factor. As a consequence, the single inductor used in the inductor-based resonator will have a higher value of Q than the primary or secondary inductors used in the equivalent transformer-based resonator.

In order to take into account all these phenomena and compare fairly the performance of the inductor and transformer-based resonators, a wide set of integrated inductors and transformers has been simulated. All the simulated inductors and transformers use a minimum spacing of 2 μm; the number of turns (N) of the inductors ranges from 3 to 5 and from 2 to 4 in transformer case (number of turns of the primary or the secondary). The strip width has been chosen for each inductor and transformer to optimize the value of Q at 1.7 GHz. Moreover, an additional constraint is added in terms of the component size. Therefore, no outer dimensions larger than 350 μm are included in the simulations

[3] The primary/secondary Q was found exciting the transformer in common mode (with a current source in each side).

(even when values of Q lightly higher could be obtained). For a fixed number of turns, the outer dimensions of the component have been reduced from 350x350 μm at steps of 20 μm until the component collapsed.

Figure 2-12 shows the dependence of Q vs. L at 1.7 GHz for the optimum width inductors and transformers. The effective Q of the transformer (or the inductor) has been obtained fitting the phase slope around the resonance of the transformer (or inductor)-based resonator centered at 1.7 GHz to the phase slope of an ideal equivalent inductor resonator (fig. 2-4). This method removes the effects on the quality factor of the parasitic capacitances that can misleadingly increase its value if it is determined as the ratio between the imaginary and real parts of the impedance.

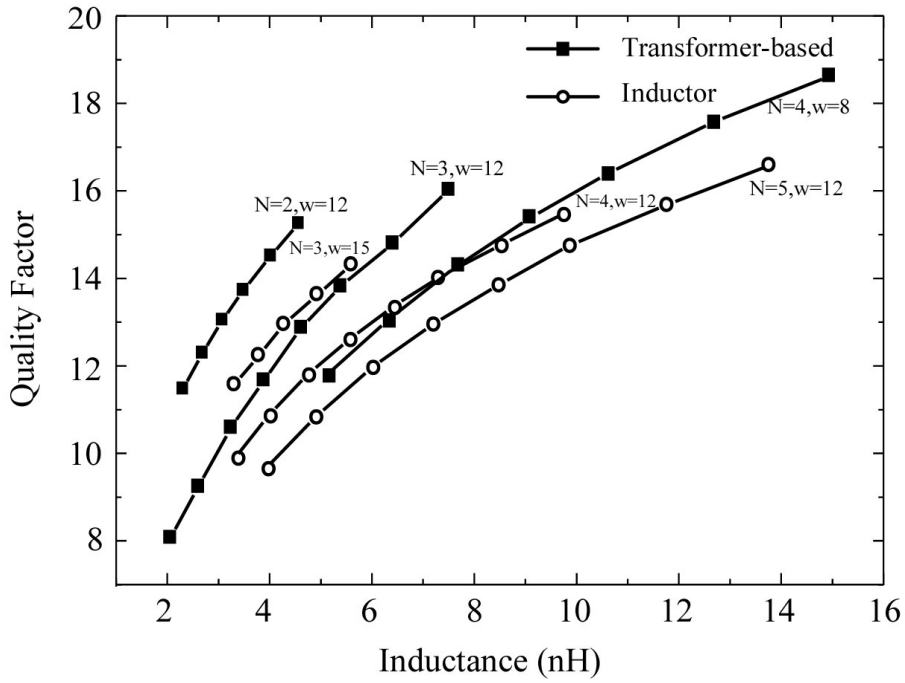

Figure 2-12. Comparison of the quality factor of the inductor and transformer based resonators at 1.7 GHz

This figure confirms that the theoretical improvement of 80% (is a k=0.8 is assumed) is reduced to approximately 15% in practical implementations, being more significant for higher values of inductance (around 10 nH), where higher effective Q's can be synthesized in smaller areas. A similar phenomenon can be identified when a differential symmetric inductor is used instead of two uncoupled inductors [22,23]. It should be remarked that the optimum width for inductors and transformers synthesizing

the same value of equivalent inductance is narrower for the transformer structure. This fact corroborates that eddy currents, which are proportional to the strip width, are more significant in the transformer-based resonator.

Fig. 2-12 also indicates that, the larger number of turns, the lower the quality factors for a given inductance value. This degradation of the quality factor is also related to the increment with the number of turns of the losses caused by the eddy currents. Therefore, high Q inductors should be synthesized using the minimum number of turns at the expense of a considerable increment of the area, resulting in the well-known 'hollow inductors' [3].

2.5 Transformer Optimization

In the previous section, we have identified the eddy currents in the metal strips of the transformer as the reason that prevents or limits the improvement in the quality factor of the transformer-based resonator. In [24], Lopez-Villegas et al. presented a design technique that allows the optimization of the inductor layout in order to maximize its quality factor. This method basically trades losses due to eddy currents (that increase with the strip width) and ohmic losses (that decrease with the strip width) and establishes the optimum strip width (for each inductor turn) that minimizes the overall losses. Although this technique was firstly applied to micromachined inductors (where the Silicon underneath the inductors had been removed) and later to GaAs substrates [25], it is also useful in our technology since the Silicon substrate does not contribute to the component losses as we have proved in section 3 (fig. 2-10).

A careful analysis shows that this algorithm can be applied straightforward to the optimization of transformers working in common mode. Since for a symmetric transformer-based resonator the currents in the primary and the secondary are equal at the resonance, the transformer can be seen and optimized as an inductor. To illustrate it, let us consider that a symmetric inductor with value 2L and quality factor Q is cut at the center tap resulting in two coupled inductors, namely, a transformer (see fig. 2-13). Then, the resulting transformer-based resonator will act as an inductor L but with a quality factor Q. Basically a 10 nH inductor can be synthesized as a 20 nH inductor.

Combining this layout optimization method and the idea of hollow inductors an optimized transformer can be obtained. The process of optimization can be split into two steps. First, it should be found the inductor with optimum constant width and then, the optimum inductor with a different width for each turn. The values deduced from the algorithm presented in [24] can be used as an initial trial for the widths of the optimized inductor. Then, these values can be refined using the layout optimizer embedded in ADS, that takes into account more accurately the geometry of the component and the capacitive effects (that are neglected in [24]). Applying this procedure, the geometry of an inductor can be optimized in few hours (for a large inductor of five turns).

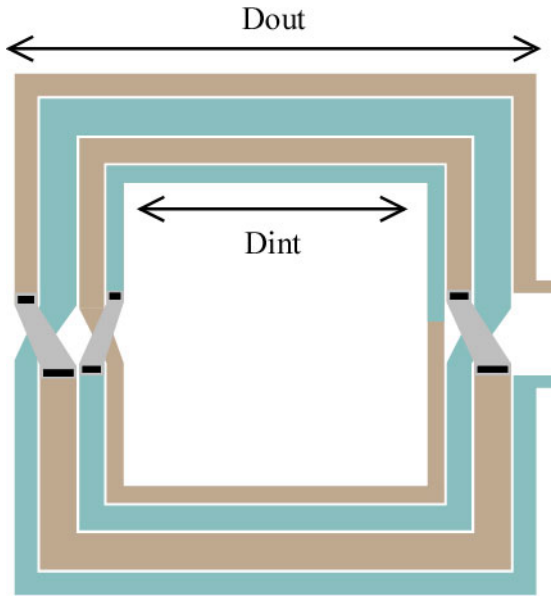

Figure 2-13. Optimized inductor layout. (The different colors represent the primary and secondary of an eventual transformer)

Fig. 2-13 shows the typical layout of an optimized inductor with wide outer turns and narrower inner turns. This layout can be easily explained considering the magnetic field distribution over the inductor (or the transformer in common mode) found in chapter 1. Since the magnetic field is more intense at the center of the spiral, the strip width is reduced for the inner turns in order to minimize the losses due to the eddy currents in spite of increase the ohmic losses. Instead, since the magnetic field (and eddy currents) decreases with the distance to the center of the spiral the outer turns become wider in order to reduce the ohmic losses. An exception to this rule is the last turn that usually it is narrower because the magnetic field changes its direction for this turn and starts to increase again.

Using this method a set of inductors with 3 and 4 turns and diverse values of inductance have been optimized. For all the inductors the distance between strips was 2 microns (the minimum allowed by the technology). Table 2.2 summarizes the main characteristics of these inductors. In this table, d1 represents the width of the outer turn and d3-4 the width of the inner turn. Dout and Dint represent the outer and inner dimensions of the inductor respectively.

Data shows that quality factors higher than 18 have been achieved for a broadband of inductance values. Moreover, if these inductors were used to build a transformer-based resonator (as shown in fig. 2-13) they will overcome considerably the performance of the optimum-fixed width inductors. As an example, inductors 5 and 6 will act as inductors of 8.8 nH (Q_{eff}=20.1) and 7.15 nH (Q_{eff}=19.0) respectively. Also, it should be noted that inductance values as low as 2.27 and 2.95 nH with quality factors of 18 could be synthesized using inductors 3 and 4.

	#	d1	d2	d3	d4	Dint	Dout	L(nH)	$r_s(\Omega)$	C(pF)	Q
N=3	1	14.5	24.0	15.0	-----	380	495	9.22	5.28	0.946	18.6
	2	17.3	28.7	15.4	-----	332	463	7.47	4.38	1.168	18.2
	3	20.0	35.0	15.0	-----	282	430	5.90	3.48	1.479	18.1
	4	25.0	40.0	15.0	-----	237	405	4.55	2.82	1.919	17.2
N=4	5	9.0	15.7	15.0	11.5	374	488	17.6	9.38	0.494	20.1
	6	9.4	15.2	15.2	13.6	323	438	14.3	8.07	0.609	19.0
	7	10.8	17.0	14.5	11.5	273	393	11.0	6.41	0.791	18.4
	8	14.5	23.8	16	10.7	198	340	7.1	4.49	1.229	16.9
	9	16.3	35.0	23.5	10.5	147	330	5.0	3.42	1.775	15.5

Table 2.2 Layout characteristics and equivalent circuits for optimized inductors at 1.7 GHz (all the dimensions are given in microns)

At the end of section 2 we have mentioned that the transformer-based resonator could be extended to the parallel connection of N resonators that would result theoretically in an effective quality factor N times higher than the quality factor of single (uncoupled) inductor. Unfortunately, we have already demonstrated for N=2 that this improvement is reduced in practical implementations. However, we will still dedicate some efforts to the analysis of 3 coupled resonators based on the layout shown in fig. 2-14.

The optimization of a 3-port transformer can not be addressed as directly as the optimization of an inductor due to the difficulties of defining the optimization goals for

a three port structure. Instead, to perform this optimization we have firstly optimized an equivalent inductor with a geometry similar to the 3-ports transformer (6 turns inductor) and then these widths are translated to the transformer layout. The obtained results are summarized in the table 2.3. Note that the values of L and Q given in this table refer to the phase properties of the equivalent inductor-based resonator. As an example, if a capacitor of 0.951 pF is attached to each port of the 3-filar transformer numbered as 2 in table 2.3, the resulting resonator will have identical phase characteristics around 1.7 GHz than an inductor-based resonator with L=9.19nH, C=0.951pF and Q=23.7. However, the impedances of both resonators will be quite different as it can be deduced from (2.9) and (2.10).

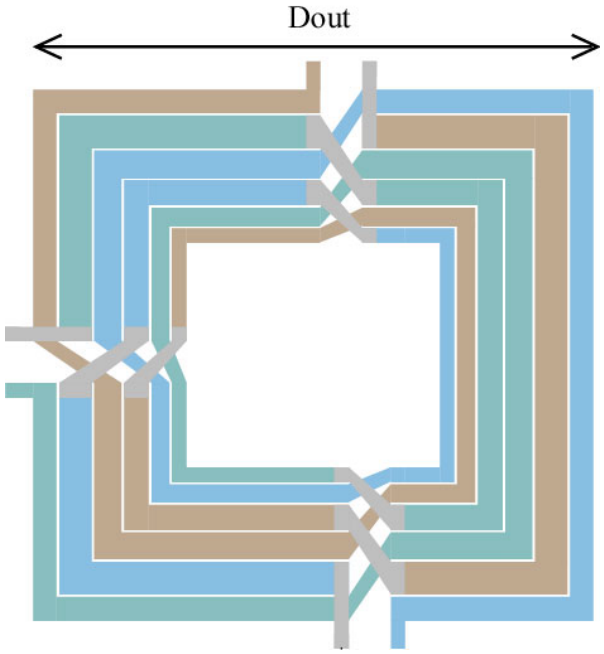

Figure 2-14. Trifilar transformer used to build a 3-parallel resonator (a capacitor is attached to each port)

#	d1	d2	d3	d4	d5	d6	Dout	L_{eq}(nH)	$r_s(\Omega)$	C(pF)	Q_{eff}
1	12.8	23.2	20.0	17.5	14.7	11.2	603	11.0	4.61	0.797	25.4
2	14.5	18.0	15.5	17.0	15.2	11.0	530	9.19	4.15	0.951	23.7
3	14.2	20.0	23.7	20.0	16.0	10.7	482	7.22	3.49	1.210	22.0
4	16.7	23.0	19.0	17.5	12.7	10.0	397	4.19	2.41	2.080	18.6

Table 2.3 Layout characteristics and equivalent circuits for 3-parallel resonators at 1.7 GHz (all the dimensions are given in microns)

This table points out that using an optimized 3-port transformer results in effective quality factor as high as 23.7 for a 9.29 nH inductor at 1.7 GHz. Comparing this value with figure 2-12, it results in an improvement greater than 50%.

2.6 Oscillator Design and Measurement

2.6.1 Designing oscillators based on N-coupled resonators

The characteristics, and in particular the phase-noise performance, of the LC oscillators based on a double CMOS cross-pair has been deeply analyzed by Hajimiri [12,13,27]. Concerning the phase-noise performance, this author has identified two different operating regions for the oscillator named as current-limited (or inductance-limited) and voltage limited. In the current limited region, the phase-noise decreases as the tail current increases. However, when the amplitude of the signal reaches levels close to the oscillator dc bias, it saturates and no further improvement in the oscillator phase-noise is achieved by increasing the tail current. This is the voltage-limited region.

In the non-linear analysis performed in the next chapter we will show that this saturation is related to the cut-off of the cross-pair transistors for large amplitude signals. Thus, an oscillator designed for minimum phase-noise should be close to the transition between both regions (working deep into the voltage-limited region results in a waste of power).

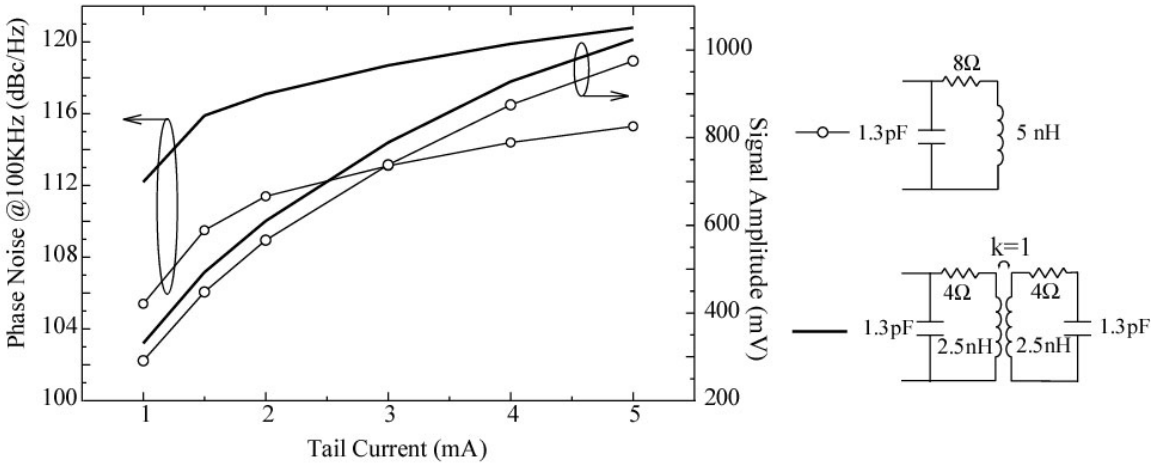

Figure 2-15. Comparison of the amplitude and phase noise of an oscillator using an inductor and a transformer-based resonator. Both resonators have the same peak impedance but the parallel resonator has an effective quality factor twice than the inductor

Fig. 2-15 shows the dependence of the amplitude with the tail current of the oscillator shown in fig. 2-16 for two different resonators where the current-limited and voltage-limited regions can be easily identified. Since both resonators have the same peak

impedance, their amplitudes are very similar. However, the transformer-based resonator has an effective quality factor twice than the inductor-based and hence it results in a 6 dB lower phase noise as predicted by Leesson's model (see. fig. 2-15). This fact corroborates (as expected) that the phase noise performance is determined by the effective quality factor (given in terms of the phase slope of the resonator) rather than by the peak impedance.

Since for the same effective quality factor the peak impedance of the N-coupled parallel resonator is lower than for the inductor-based resonator, I_{tail} can be increased to higher values before reaching the voltage limited region. Of course, this improvement does not increase the oscillator figure of merit since it is achieved at expenses of higher power consumption. However, this method may result interesting if an absolute (or specified) value of phase noise is desired.

Also, if the tunning range is not a main goal in the oscillator design the overall capacitance used in the parallel resonator NxC_p could be reduced. This increases the peak impedance (reducing the power consumption) and allows the utilization of a higher value of inductance that can reach a higher quality factor.

As summary, the advantages of the N-parallel resonators over their inductor-based counterpart can be synthesized in the following items:

1) N-parallel resonators can achieve higher effective quality factors usually with lower peak impedances.
2) The use of a higher capacitance in the transformer-based resonator results in an extended tunning-range.
3) Since the center tap of secondary/ies is grounded to bias properly the varactors it acts as a short circuit for the common mode harmonics. Thus, no second harmonics can appear across the varactors in the secondary/ies, avoiding noise down-conversion associated to the varactor non-linearities.

2.6.2 Prototype Design and Test

In order to evaluate the performance of the transformer-based resonator in a practical oscillator design, the VCO shown in Fig. 2-16 was implemented in the Conexant 0.35µm BiCMOS process [26]. This structure combining PMOS and NMOS cross-pairs minimizes the up-conversion of the 1/f noise compared to NMOS topology [13] and hence it is traditionally intended for low-phase noise designs. However, we should mention that recently the differential CMOS Colpitts oscillator has appeared as an alternative to this topology for very low phase-noise performance and should be investigated in future works.

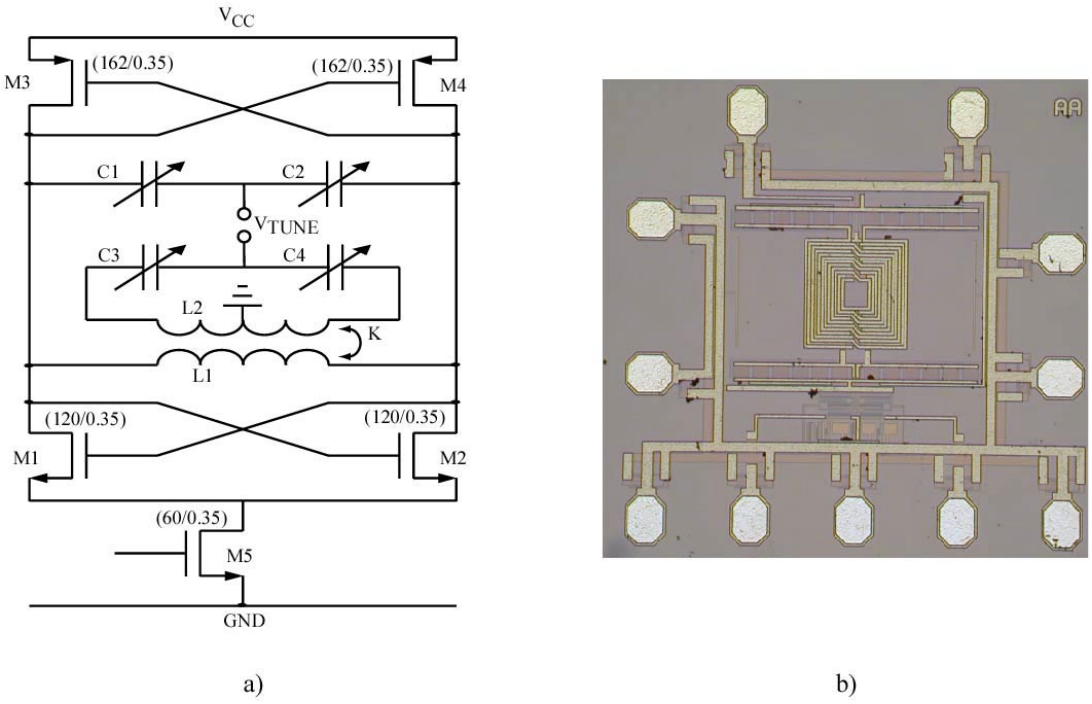

Figure 2-16. a) Schematic of the transformer-based VCO (C=900 fF at 1.7 GHz) and b) its layout

The VCO was optimized for minimum phase noise using Spectre RF (Cadence) simulator. The transistor channel length was set to the minimum allowed value (i.e., 0.35 µm) in order to minimize the parasitic capacitances. The transistor widths were chosen for minimum phase noise as long as a reliable startup of the oscillator was guarantied for a bias current of 4 mA. A simple common-drain stage, biased with 2 mA and adding 125 fF to the resonant tank, was used as the output buffer. Special care was dedicated to keep the inherent symmetry of the circuit during the layout process. Both

NMOS and PMOS transistors were laid out as multi-finger structures in order to minimize their gate resistance.

The transformer-based (parallel) resonator is implemented using the integrated transformer of Section 3, and two sets of varactors, one at the primary loop and one at the secondary loop. The varactors are lateral npn transistors, and have a capacitance of 900 fF at 1.6 V bias with a Q of 40-50 at 1.8 GHz. The control voltage is attached to the primary and secondary varactors .The ground connections of the transformer, required to bias properly the varactors, are realized in the transformer center taps. The chip (shown in fig. 2-16), with outer dimensions of 1250x900 μm, is defined by the size of the available probes.

The oscillator characteristics are summarized in Table 2.4. The total supply current is 14 mA from a 2.5 V supply which includes the bias circuit, core VCO (4.5 mA), and differential buffer amplifier. The measured output power is 0.5 mW and was taken off-chip differentially using a G-S-G-S-G differential probe from Picoprobe and converted to a single-ended signal using a 0-180° power-combiner. It is important to note that a differential measurement is convenient, not just for common mode noise immunity, but also in order to minimize any asymmetry due to loading both oscillator outputs with a different load (even if output buffers are present).

Vdd	2.5V
Idd	14 mA
Icore	4.5 mA
F_0	1.7 GHz at 2.5 V
Tuning	107 MHz at 0-2.5 V
Pout	0.5 mW (differential.)
Pn	-138 dBc/Hz at 600 kHz -142 dBc/Hz at 1 MHz -152 dBc/Hz at 3 MHz
Pushing	1.6MHz/V at Vdd=2.5V 0.5MHz/V at Vdd=2.6V

Table 2.4 Summary of Measured Characteristics

The VCO phase-noise was measured at Agere Systems in the base-station group (Dr. Jenshan Lin) using the Agilent E5500 phase noise measurement system with the FM discrimination method. The measurements were obtained at a varactor bias voltage of 2-2.5 V, and using battery operation. Two oscillators were measured and were within 2 dB of each other over the 100 KHz – 3 MHz range (fig. 2-17). Notice the change in the slope of the phase noise between low and high frequency offsets pointing out the up-conversion of 1/f noise and the high 1/f frequency corner characteristic of MOS devices compared to bipolar devices. The measurements show that the presented CMOS VCO satisfies GSM, CDMA and mini-base station phase-noise requirements.

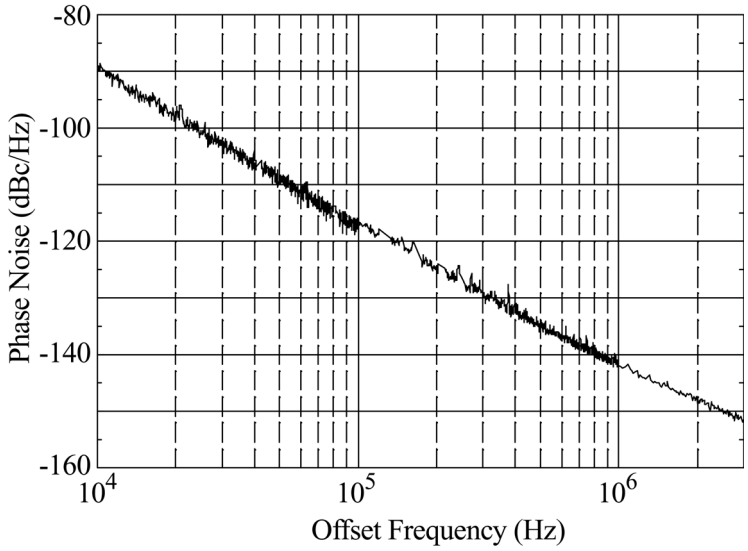

Figure 2-17. Measured phase noise of the integrated CMOS VCO at 1.7 GHz

In spite of the excellent phase noise performance reported recently by several authors [16-19], the presented transformer-based design outperforms the previously published results in terms of phase noise. In order to compare the presented oscillator with previous designs, we have used the figures of merit defined in [2, Eqs.29-30] for fixed and tunable oscillators. A value of 22 dB (using the phase noise a 3 MHz) is obtained as fixed oscillator and 8 dB as tunable oscillator. This leads to an improvement of 6-8 dB over the best design reported in [27].

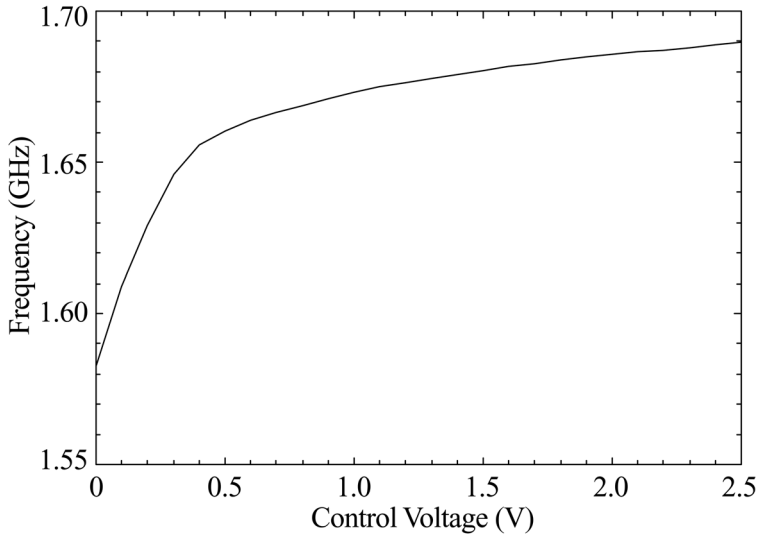

Figure 2-18. Measured tuning characteristics of the CMOS VCO

The VCO tuning characteristics are shown in fig. 2-18. The lateral npn varactors available in this process had a poor capacitance ratio and resulted in a narrow tuning range. Therefore, for all practical reasons, the oscillator in this work should be considered as a fixed-frequency oscillator (or a VCO with a very small tuning range, 5%). In future designs, nMOS varactors will be used in order to exploit the high capacitance and corresponding high tuning range of the parallel resonator.

Acknowledgments

I would like to thank Matt Straayer for proposing the transformer-based resonator and designing and testing the VCO presented in this chapter as a demonstrator of the N-parallel resonators. Without his first steps, the analysis performed in this chapter would never have been carried out.

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QUADRATURE OSCILLATORS

Introduction

In the Introduction chapter, we highlighted the relevance of quadrature oscillators in the modern wireless communications systems, since they make easier the integration of the RF front-end and allow a more efficient use of the restricted RF bandwidth. In this chapter, we present a novel method for designing quadrature oscillators, based on the differential coupling at the second harmonic of two-separated differential oscillators [1]. As in the previous design of the low phase-noise VCO, an integrated transformer plays a key role in this circuit being used to establish the desired coupling between the oscillators.

This chapter intends to establish a basic understanding of the phenomena involved in the generation of quadrature signals using the proposed method and verify experimentally its applicability. Thus, it is organized in 7 sections. The first section revises shortly the different topologies of quadrature oscillators and their characteristics (quadrature accuracy, amplitude mismatching, etc) in order to compare the advantages and drawbacks of the new topology with the currently existing state-of-the-art. Section two consists in a non-linear 'hand' analysis (equivalent to an harmonic balance analysis) of an oscillator based on a single NMOS cross-pair and sets up the basis for the analysis of injected oscillators performed in section three. A special insight is given to the second harmonic due to its fundamental role in the quadrature oscillator presented

later. Section 4 revises briefly some theory on coupled oscillators and points out the importance of different design parameters (resonator quality factor, transformer coupling factor, frequency mismatch between coupled oscillators) in the quadrature accuracy. Section 5 applies all the previous concepts to the design of a general quadrature oscillator, points out the design parameters that affect directly the accuracy of the quadrature and identifies different phenomena (parasitic coupling, oscillator mismatches) that degrade the oscillator performance. Section 6 presents a 900 MHz prototype based on the double CMOS cross-pair topology and implemented in the BC35 (0.35 μm BiCMOS) Conexant process. This prototype has a power consumption of 5 mW and an output power of –9 dBm. The measured phase noise is –116, -133 and –138 dBc/Hz at 100 KHz, 600 KHz and 1 MHz from the carrier respectively.

Finally, in order to illustrate the broad range of possibilities and the applicability of the presented method to generate quadrature signals, two additional circuits in a hybrid implementation are also shown in section 7. The first circuit consists in a hybrid implementation of a quadrature oscillator at 150 MHz realized on a PCB board and employs packaged transistors and transformers. The main advantage of this approach (compared to the integrated design) is its versatility, since changes in the topology or in the components can be easily done, becoming a useful tool for the analysis and test of the new topology. The second circuit consists in a quadrature generator also implemented as a hybrid circuit. In this circuit, a second harmonic is injected and signals in quadrature are obtained at the fundamental harmonic as in the previous designs. However, it has an important difference with the previous designs: in absence of the injected signal at 2f, there is no oscillation since the injected signal is used to compensate the resonator losses. Thus, the only active devices present in the circuit are the varactors used in the resonator.

Although it is not investigated in this work, it is worthy to remark that the proposed method could be applied to stacked structures. Thus, if two quadrature oscillators running at f are used to inject a set of four new oscillators running at f/2, it will result in a system with 8 phases.

3.1. Quadrature Oscillator Topologies

Besides the standard requirements on the oscillator performance in terms of phase noise, power consumption, area or tuning range, quadrature oscillators must satisfy some additional demands such as quadrature accuracy or amplitude matching. Moreover, as we will see later, some quadrature topologies may need two oscillators or use large passive devices, increasing the relevance of parameters as power consumption or chip area.

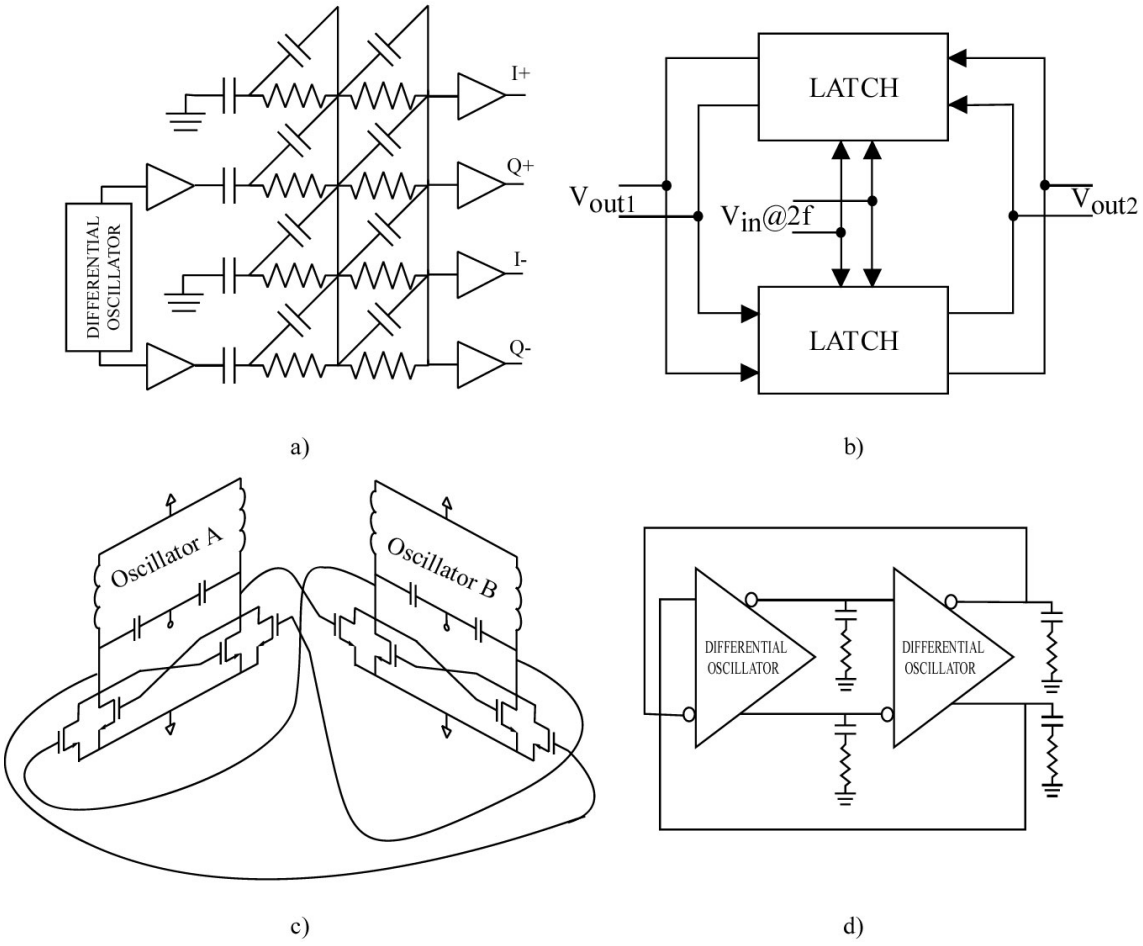


Figure 3-1. Circuit topologies used in the implementation of quadrature oscillators at RF frequencies

Basically four different design approaches have been reported in the literature to generate quadrature signals at RF frequencies and they are schematically shown in fig. 3-1:

1. Combination of VCO´s, poly-phase filters (or RC-CR networks) and output buffers (or amplitude limiters) as used in [2], [3].
2. VCO at double frequency followed by master-slave flip-flops.
3. Two cross-coupled VCO´s as proposed in [4].
4. Poly-phase oscillators, such as a ring oscillators [5,6,7].

The first approach, probably the most widely used, is based on the phase shift generated by a RC-CR network and needs a single oscillator and four output buffers acting as amplitude limiters. These output buffers result in a high power consumption that is even increased if additional buffers are inserted between the VCO and the RC-CR network. However, if the filters are directly connected to the VCO, the tank capacitance is increased, leading to a higher power consumption and worse phase noise. This alternative may become also area consuming since a good matching between the filters requires a large chip area.

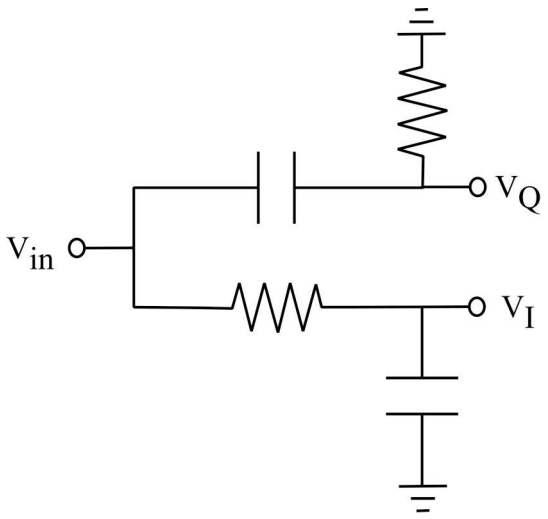


Figure 3-2. 90 Degrees phase shift RC-CR network

Let us revise shortly the characteristics of this method to generate quadrature signals. So, consider a simple RC-CR network as shown in fig. 3-2. The phase difference between V_{out1} and V_{out2} is known to be $\pi/2$ for all the frequencies, but the amplitudes of both signals are equal only at $\omega = \frac{1}{RC}$. In more detail,

$$|V_I| = \frac{V_{in}}{\sqrt{1+(\omega RC)^2}} \qquad \theta_I = \frac{\pi}{2} - \arctan(\omega RC) \qquad \textbf{(3.1)}$$

$$|V_Q| = \frac{V_{in}}{\sqrt{1+\left(\frac{1}{\omega RC}\right)^2}} \qquad \theta_Q = -\arctan(\omega RC) \tag{3.2}$$

If there is no process deviations between two resistors or the capacitors, we have:

$$|V_I - V_Q| = \frac{(\omega RC - 1)V_{in}}{\sqrt{1+(\omega RC)^2}} \qquad \theta_I - \theta_Q = \frac{\pi}{2} \tag{3.3}$$

When ω equals $\frac{1}{RC}$, the I-Q signals have a common amplitude of $V_{I-Q} = \frac{V_{in}}{\sqrt{2}}$ and a phase shift of π/2. However, in real situations, we will inevitably find mismatches of both amplitude and phase caused by process parameter gradient on wafers, non-linearities, temperature dependencies and interfering signals. In order to improve the quality of the quadrature, more complex circuits still based on RC-CR networks have been proposed [3,8].

In the second option, two flip-flops perform a digital frequency division of a signal coming from a VCO designed at double frequency. Although the oscillator at 2f can have a reasonable power consumption, the master-slave flip-flops driven by the 2f signal consume too much power in the current widely used CMOS technologies (0.25 μm). This high power consumption is an important drawback mainly for frequencies of 5 GHz and higher. However, if the main design concern is low cost or small area, then this solution must be clearly preferred, as the VCO designed at double frequency features a smaller coil and the area of master-slave flip-flops in sub-micron CMOS processes is negligible.

This approach to generate quadrature signals is similar to the method we are presenting later in this chapter. However, two important differences should be pointed out. In our design, an analog division of the frequency substitutes the digital frequency division performed by the flip-flops, decreasing the power consumption. Moreover, the own second harmonics of the analog frequency dividers are used to synchronize themselves so no additional oscillator at 2f is needed.

The third alternative was reported firstly by Rofougaran in 1996 and consists in two cross-coupled oscillators as shown in fig. 3-1.c [4]. To understand how this circuit generates quadrature signals, let us suppose that the two oscillators are synchronized in-

phase. Then the cross-coupled path from oscillator B to A absorbs the negative resistance current produced by oscillator A, and oscillator A ceases. The inductors in oscillator A pull up both drains nodes to VCC and through the cross-coupled FETs this shuts off oscillator B. The same process applies in reverse if the two oscillators are synchronized anti-phase. Therefore, the oscillators only co-exist when they synchronize in quadrature. Recently, Andreani and Tiebout have reported small variations that improve the phase noise performance of this circuit [9,10]. This option comes at the cost of double VCO area but outperforms the previous solutions in terms of power consumption, since a well-designed VCO consumes less power than the four buffers or limiters of the first option, or than the master-slave flip-flops of the second option. The two-core solution, moreover, provides a very high voltage swing, which makes easier the design of the pre-scaler or the mixer connected to the VCO.

So far all the designs presented are (LC) resonator based oscillators and hence their phase noise at frequencies far enough from the resonance decreases at a rate proportional to the square of the resonator Q. Ring (resonator-less) oscillators constitute an alternative to them in order to produce quadrature outputs.

Thus, in a four-delay stage ring oscillator, taps at diametrically opposite points yield quadrature phases at every oscillation frequency. When the oscillator is composed of an odd-number of delay units, the desired phases may be synthesized by interpolating two taps with a voltage-controlled phase-shifter in feedback around a quadrature-sensing circuit [11]. The mismatches of the unit cells limit the attainable phase accuracy. This form of resonator-less oscillator is attractive because it is fully integrated (even in fully digital technologies) and may be used when the specifications on phase-noise close to the carrier are not very stringent.

3.2. Non-linear Analysis of a NMOS cross-pair

A broad range of oscillators can be modeled by a passive network (the resonator) and an active circuit, that restores the energy dissipated in the resonator. In the previous

chapter, we have focused our interest in the passive part of the oscillator and in its influence on the oscillator performance. Thus, we have analyzed a new resonator topology based on an integrated transformer and pointed out its impact on the oscillator phase noise and tuning range characteristics.

In the present section, we will analyze the role of the active circuitry with a special attention to the non-linearity of the active devices (bipolar or MOS transistors) used in the common oscillator design. This non-linear analysis allows us to explain the phenomena of the oscillator injection locking as well as to set up some important considerations required in the analysis and design of the new topology of quadrature oscillator presented at the end of this chapter.

In sake of simplicity, we have chosen the oscillator shown in fig.3-3. Since the inverter transformer is ideal (k=1), it acts as a short circuit (ground) for the common mode signals, and hence for the even harmonics of the oscillator. Therefore, no even harmonics are found at the drains of the MOS transistors. We have used a simple model for the MOS transistors given by:

$$\begin{aligned} I_{DS} &= 0 && \text{if } V_{GS} < V_{TH} \quad (Off) \\ I_{DS} &= \frac{k}{2}(V_{GS} - V_{TH})^2 && \text{if } V_{DS} > V_{GS} - V_{TH} \text{ and } V_{GS} > V_{TH} \quad (Saturation) \\ I_{DS} &= k(V_{GS} - V_{TH})V_{DS} - \frac{k}{2}V_{DS}^2 && \text{if } V_{DS} < V_{GS} - V_{TH} \text{ and } V_{GS} > V_{TH} \quad (Linear) \end{aligned} \qquad \textbf{(3.4)}$$

Although, this basic quadratic model does not accurately describe sub-micron MOS devices (as the ones used later in the presented designs), the extracted conclusions are still valid when higher order non-linearities or device parasites are considered. Using the previous model, the dc, the first and the second harmonics of the drain-source current can be found in terms of the oscillation signal $V_1\cos(\omega t+\theta_1)$ and the signal at 2f at the sources of the transistors $V_2\cos(2\omega t+\varphi_2)$ (see fig. 3-3). This second harmonic signal could be neglected in a first approach. However, if considered, it allows us to extend the analysis to second harmonic injected oscillators. The current through the MOS transistors can be written as a Fourier series:

$$I_{DS} = I_{DC} + I_{1I}\cos(\omega t+\theta_1) + I_{1Q}\sin(\omega t+\theta_1) + I_{2I}\cos(2\omega t+2\theta_1) + I_{2Q}\sin(2\omega t+2\theta_1) \quad \textbf{(3.5)}$$

if the third and higher harmonics are neglected. The sub-indexes I and Q refer to the current components in-phase and in quadrature with the oscillation voltage $V_1\cos(\omega t+\theta_1)$.

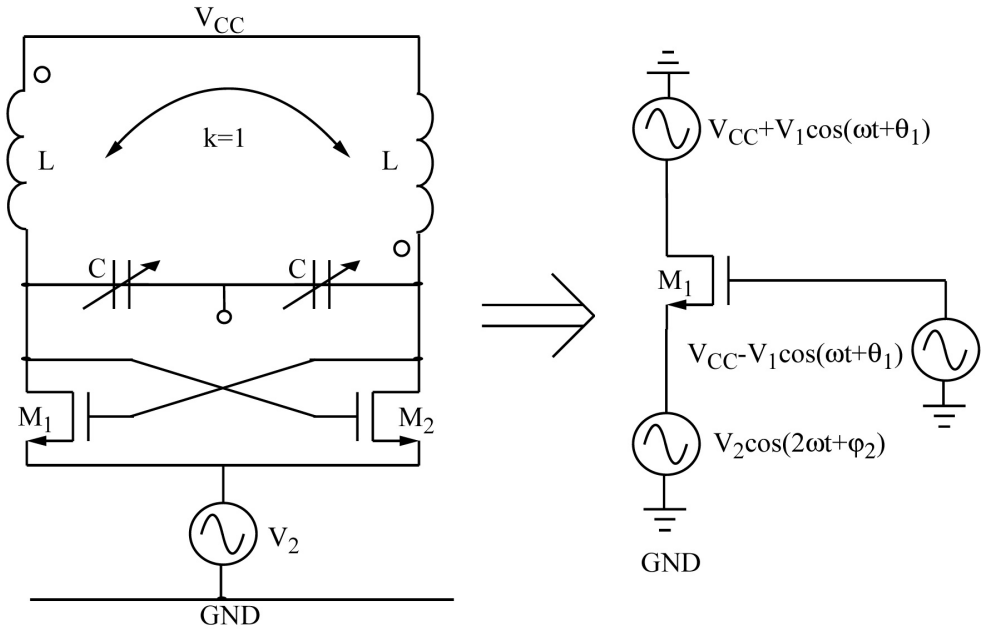


Figure 3-3. Differential oscillator and its equivalent model for the non-linear analysis

In order to compute the different current harmonics, it is necessary to find the points where the transistors change their operating region in terms of the signal amplitude during the oscillation period.

If no oscillation exists, both switching transistors are in saturation, and the cross-coupled transconductance offers a small-signal negative differential conductance that induces the start-up of the oscillation. For $V_1<0.5V_{TH}$, both transistors remain in the saturation region during the whole oscillation cycle. As the oscillation voltage crosses $V_{TH}/2$ ($V_1>0.5V_{TH}$), one FET gets into the linear region as long as the other is driven deeper into saturation. Finally, if $V_1> V_{CC}-V_{TH}$ one FET is momentarily switched off as long as the other FET is in the linear region. Fig.3-4 shows these transitions and allows us to define t_1 and t_2 as the linear-to-saturation and saturation-to-off transition times:

$$t_1 = \frac{1}{\omega}\cos^{-1}\frac{-V_{TH}}{2V_1} \qquad t_2 = \frac{1}{\omega}\cos^{-1}\frac{V_{CC}-V_{TH}}{V_1} \quad \textbf{(3.7)}$$

As a work hypothesis, we have assumed $V_2 << V_1$ so the influence of the second harmonic in these transitions can be neglected.

After some calculation efforts, the different harmonics of the current can be written as[4]:

$$
\begin{aligned}
&\textbf{\textit{if }} V_1 < \frac{V_{TH}}{2} \\
&I_{DC\_S} = \frac{k}{2}(V_{CC} - V_{TH})^2 + \frac{k}{4}V_1^2 + \frac{k}{4}V_2^2 \\
&I_{1I\_S} = -\frac{k}{2}(V_{CC} - V_{TH})V_1 - \frac{k}{4}V_1 V_2 \cos\phi \\
&I_{1Q\_S} = -\frac{k}{4}V_1 V_2 \sin\phi \\
&I_{2I\_S} = \frac{k}{8}V_1^2 + \frac{k}{2}(V_{CC} - V_{TH})V_2 \cos\phi \\
&I_{2Q\_S} = \frac{k}{2}(V_{CC} - V_{TH})V_2 \sin\phi
\end{aligned}
\qquad \textbf{(3.8)}
$$

$$
\begin{aligned}
&\textbf{\textit{if }} V_1 < V_{CC} - V_{TH} \\
&I_{DC\_SL} = I_{DC\_S} - \frac{kV_{TH}^2(T - 2t_1)}{2T} + \frac{2kV_1 V_{TH}}{\pi}\sin\alpha - kV_1^2\left(\frac{(T - 2t_1)}{T} - \frac{\sin 2\alpha}{2\pi}\right) \\
&I_{1I\_SL} = I_{1I\_S} + \frac{kV_{TH}^2}{2\pi}\sin\alpha - kV_1 V_{TH}\left(\frac{(T - 2t_1)}{T} - \frac{\sin 2\alpha}{2\pi}\right) + \frac{2kV_1^2}{\pi}\left(\sin\alpha - \frac{\sin^3\alpha}{3}\right) \\
&I_{1Q\_SL} = -\frac{k}{4}V_1 V_2 \sin\phi \\
&I_{2I\_SL} = I_{2I\_S} + \frac{kV_{TH}^2}{4\pi}\sin 2\alpha + \frac{kV_1 V_{TH}}{\pi}\left(\sin\alpha + \frac{\sin 3\alpha}{3}\right) + \frac{kV_1^2}{2\pi}\left(\sin 2\alpha + \frac{\sin 4\alpha}{4}\right) - \frac{kV_1^2}{2T}(T - 2t_1) \\
&I_{2Q\_SL} = -\frac{k}{2}(V_{CC} - V_{TH})V_2 \sin\phi
\end{aligned}
\qquad \textbf{(3.9)}
$$

[4] Note that these expressions are recursive. Thus, by example, in order to compute the dc current for $V_1 > V_{CC} - V_{TH}$, first should be computed I_{dc} for $V_1 > 0.5V_{TH}$ and I_{dc} for $V_1 < V_{CC} - V_{TH}$.

if $V_1 > V_{CC} - V_{TH}$

$$I_{DC\_SLO} = I_{DC\_SL} - k(V_{CC} - V_{TH})^2 \frac{t_2}{T} - \frac{kV_1^2}{2}\left(\frac{t_2}{T} + \frac{\sin 2\beta}{4\pi}\right) + \frac{k(V_{CC} - V_{TH})V_1}{\pi}\sin\beta -$$
$$- \frac{kV_2^2}{2}\left(\frac{t_2}{T} + \frac{\sin 4\beta \cos 2\phi}{8\pi}\right) - \cos\phi\left[\frac{k(V_{CC} - V_{TH})V_2}{2\pi}\sin 2\beta - \frac{kV_1V_2}{2\pi}\left(\sin\beta + \frac{\sin 3\beta}{3}\right)\right]$$

$$I_{1I\_SLO} = I_{1I\_SL} - \frac{k(V_{CC} - V_{TH})^2}{2\pi}\sin\beta - \frac{V_1^2}{8\pi}\left(3\sin\beta + \frac{\sin 3\beta}{3}\right) + k(V_{CC} - V_{TH})V_1\left(\frac{t_2}{T} + \frac{\sin 2\beta}{4\pi}\right) -$$
$$- \frac{kV_2^2}{4\pi}\sin\beta - \frac{kV_2^2}{4\pi}\left[\frac{\sin 3\beta}{6} + \frac{\sin 5\beta}{10}\right]\cos 2\phi + \left[\frac{kV_1V_2}{2}\left(\frac{t_2}{T} + \frac{\sin 2\beta}{2\pi} + \frac{\sin 4\beta}{8\pi}\right) - k(V_{CC} - V_{TH})V_2\left(\frac{\sin\beta}{2\pi} + \frac{\sin 3\beta}{6\pi}\right)\right]\cos\phi$$

$$I_{1Q\_SLO} = I_{1Q\_SL} + \left[\frac{kV_1V_2}{2}\left(\frac{t_2}{T} - \frac{\sin 4\beta}{8\pi}\right) - k(V_{CC} - V_{TH})V_2\left(\frac{\sin\beta}{2\pi} - \frac{\sin 3\beta}{6\pi}\right)\right]\sin\phi - \frac{kV_2^2}{4\pi}\left(\frac{\sin 3\beta}{6} - \frac{\sin 5\beta}{10}\right)\sin 2\phi$$

$$I_{2I\_SLO} = I_{2I\_SL} - \frac{k(V_{CC} - V_{TH})^2}{4\pi}\sin 2\beta + \frac{k(V_{CC} - V_{TH})V_1}{2\pi}\left(\sin\beta + \frac{\sin 3\beta}{3}\right) - \frac{kV_2^2}{4}\left(\frac{t_2}{T} + \frac{\sin 2\beta}{2\pi} + \frac{\sin 4\beta}{8\pi}\right)$$

$$- \frac{kV_2^2}{8\pi}\sin 2\beta + \left[\frac{kV_1V_2}{2\pi}\left(\sin\beta + \frac{\sin 3\beta}{6} + \frac{\sin 5\beta}{10}\right)\right]\cos\phi - \left[k(V_{CC} - V_{TH})V_2\left(\frac{t_2}{T} + \frac{\sin 4\beta}{8\pi}\right)\right]\cos\phi - \left[\frac{kV_2^2}{8}\left(\frac{\sin 2\beta}{2\pi} + \frac{\sin 6\beta}{6\pi}\right)\right]\cos 2\phi$$

$$I_{2Q\_SLO} = I_{2Q\_SL} + \left[\frac{kV_1V_2}{2\pi}\left(\sin\beta - \frac{\sin 3\beta}{6} - \frac{\sin 5\beta}{10}\right)\right]\sin\phi - \left[k(V_{CC} - V_{TH})V_2\left(\frac{t_2}{T} + \frac{\sin 4\beta}{8\pi}\right)\right]\sin\phi - \left[\frac{kV_2^2}{8}\left(\frac{\sin 2\beta}{2\pi} - \frac{\sin 6\beta}{6\pi}\right)\right]\sin 2\phi$$

$$\alpha = cos^{-1}\frac{-V_{TH}}{2V_1} \qquad \beta = cos^{-1}\frac{V_{CC} - V_{TH}}{V_1} \qquad \phi = 2\theta_1 - \varphi_2 \qquad \textbf{(3.10)}$$

In these expressions, the sub-indexes S (saturation), SL (saturation-linear) or SLO (saturation-linear-off) refer to the regions the transistors go through during the oscillation cycle as the oscillation voltage increases.

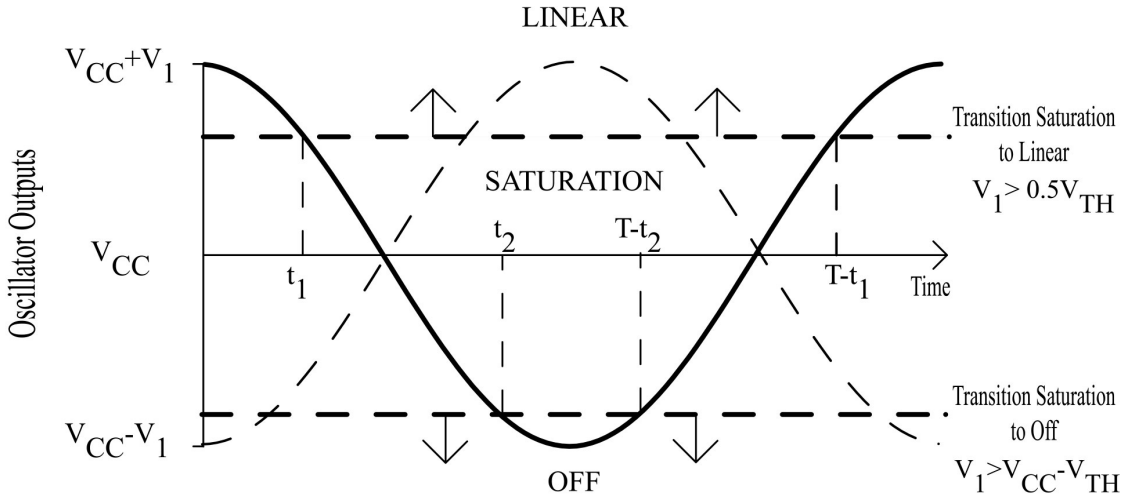


Figure 3-4. Evolution of the operating region of MOS transistors during an oscillation cycle

The preceding equations, verified using a numeric FFT of I_{DS} performed in MATLAB, have been plotted in terms of the oscillation amplitude for a particular case (V_{TH}=0.45V, V_{CC}=1.2V, V_2=100mV, θ_1=0°,φ_2=180°). To compare the agreement between the

transistor model given by (3.4) and the complex models implemented in the non-linear simulators, a MOS cross-pair (W=150 μm, L=0.35 μm, freq=1.7 GHz) has been simulated using SPECTRE RF and the BSIM3 models of Conexant technology (fig. 3-5, 3-6 and 3-7). To normalize the currents found by SPECTRE and through the analytical expressions (3.8)-(3.10) we have calculated the constant k comparing the values of the dc currents for V_1=0. It is remarkable that the obtained value (0.0758 A/V^2) matches perfectly the value of k determined theoretically through the well-known expression:

$$k = \frac{\mu\varepsilon}{t_{ox}}\left(\frac{W}{L}\right) \tag{3.11}$$

where μ is the surface mobility of the carriers, ε is the permittivity of the gate insulator and t_{ox} is the oxide thickness.

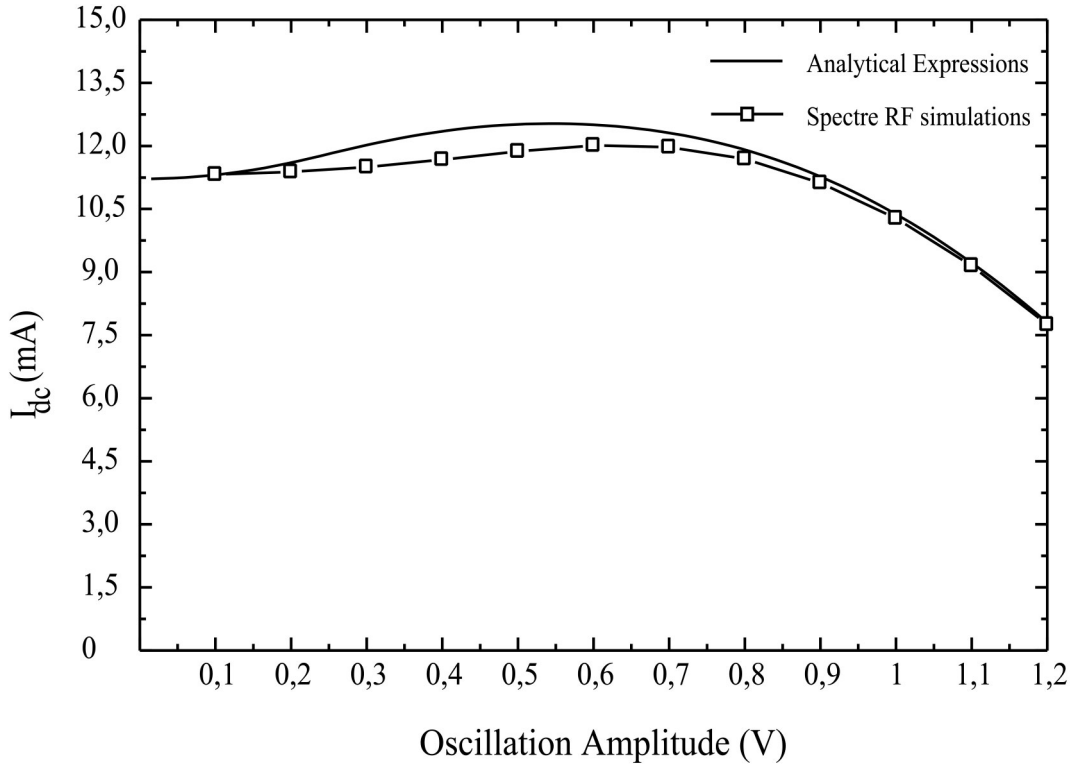


Figure 3-5. dc Current vs. the oscillation amplitude for a MOS cross-pair

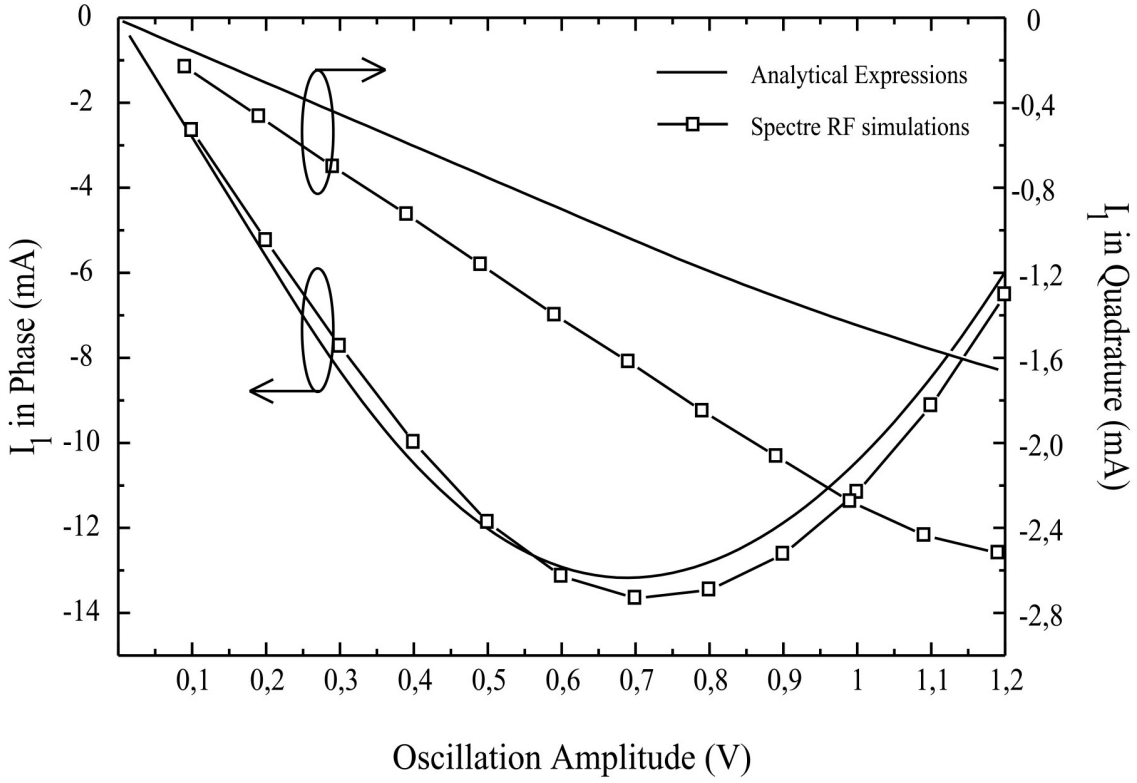


Figure 3-6. 1st Harmonic Currents vs. the oscillation amplitude for a MOS cross-pair

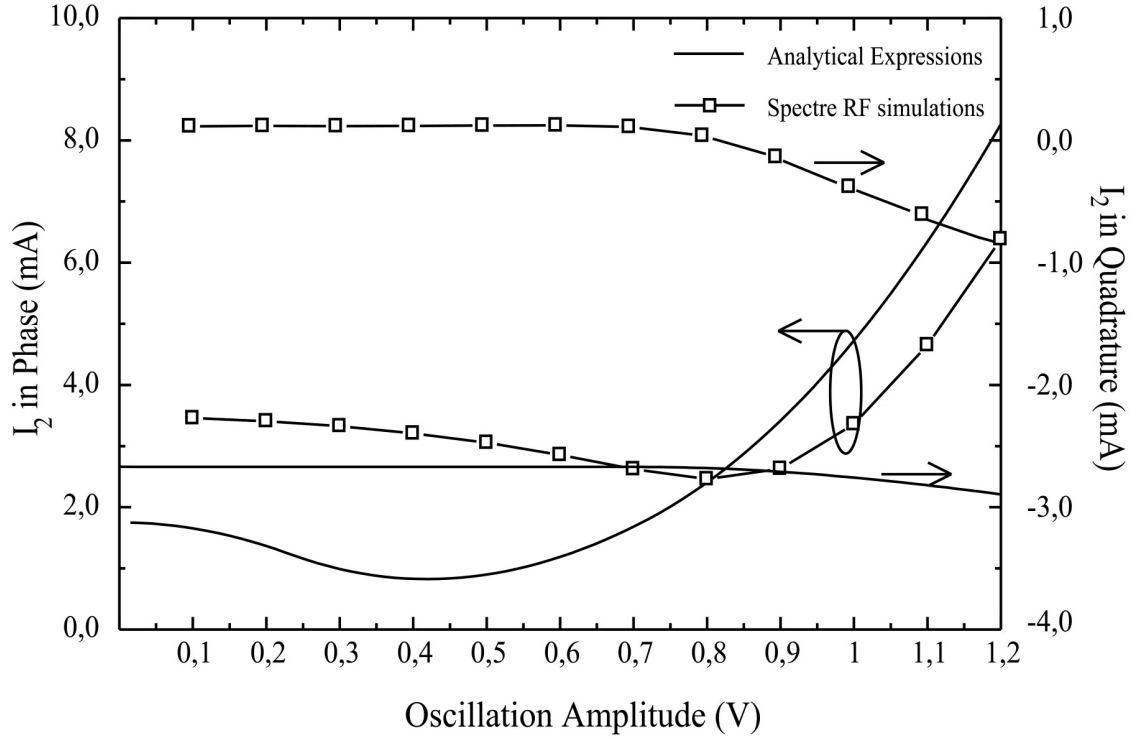


Figure 3-7. 2nd Harmonic Currents vs. the oscillation amplitude for a MOS cross-pair

In spite of the simplicity of the transistor model used in our calculations, these figures show an excellent agreement between the currents found through the analytical expressions and the ones resulting from the SPECTRE RF simulations, mainly for the dc and first harmonic. However, some (expected) differences can still be observed. It is noteworthy that our calculations have neglected the fourth harmonic of the signal, but SPECTRE RF simulations show that actually this harmonic can be comparable or even larger than the second harmonic. This explains why the second harmonic currents are not as well reproduced as the dc or the first harmonic.

Moreover, two additional reasons can be invoked to explain the observed differences: the dependence of V_{TH} with V_{BS} known as body effect and the parasitic capacitances of the MOS devices.

Since the transistors bulk is grounded and a component at twice the fundamental frequency is found at the sources of the transistors, the threshold voltage is given in a first approach by:

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{\phi_s - V_{sb}} - \sqrt{\phi_s}\right) = V_{TH0} + \gamma\left(\sqrt{\phi_s - V_2\cos\left(2\omega t + \varphi_2\right)} - \sqrt{\phi_s}\right) \qquad \textbf{(3.12)}$$

where ϕ_s is the surface potential and γ is the body bias coefficient. When this dependence of V_{TH} is introduced in the non-linear model of the MOS devices, appear additional current contributions not considered in our calculations.

The quadrature components are also affected by the parasitic capacitances of the MOS transistors as it is clearly pointed out by the figures 3-6 and 3-7. Thus, for the quadrature current at the first harmonic the difference between the analytical expression and the SPECTRE RF simulations grows linearly with the magnitude of V_1, and hence, can be associated to the overall parasitic capacitance attached at the transistors drain node. Actually, from fig. 3-6, it is possible to deduce the value of this parasitic capacitance as:

$$C_{dd} = \frac{m_{SPECTRE} - m_{analitycal}}{\omega} = \frac{(2{,}363 - 1{,}530)x10^{-3}}{2\pi(0.9x10^{9})} = 156\,fF$$

where $m_{analytical}$ and $m_{SPECTRE}$ are the respective slopes in the plots of the quadrature currents vs. V_1. The obtained value of C_{dd} matches perfectly the parasitic capacitance calculated by SPECTRE RF for the drain node.

For the quadrature components of the second harmonic a similar effect can be easily identified. However, since in this case the voltage V_2 is kept constant, the difference between the analytical expression and the SPECTRE RF simulations is also constant.

From the above figures, it is noteworthy the linear dependence of the in-phase first harmonic current with V_1 for 'small' amplitudes, corroborating that the cross-pair acts as a negative resistance. It is also remarkable that this negative resistor starts to decrease when a certain value of V_1 is reached. This value sets up the border between the current and the voltage limited regions mentioned in chapter 2 and as we have already seen, has a direct influence of the oscillator phase noise.

The previous calculations (that results in a second order harmonic balance analysis) give us the general solution of any oscillator based on a single cross-pair of ideal MOS transistors (as shown in fig.3-3). Once the impedance at the sources of the transistors, the resonator tank and the dc current (or the V_{CC} voltage) are defined, the oscillator can be solved using an iterative process with V_1, V_2 and φ_2-$2\theta_1$ as unknown magnitudes. Although the use of non-linear simulators offers an accurate solution for these equations, the previous hand analysis allows us to point out some relations/facts (mainly related to the second harmonic) that otherwise would be hardly induced from the simulation results.

In the standard RFIC oscillator design, a small emphasis has been done in the influence of the second harmonic on the oscillator performance and just lately, some authors have reported a noticeable reduction of the oscillator phase noise based on its proper filtering that minimizes the down-converted noise [12]. Instead, at microwave frequencies, the second harmonic has been intensively exploited to increase the operating frequency by using sub-harmonic injection or push-push configurations. In next sections, we will focus our interest on the second harmonic and its impact on the first harmonic in order to establish some design/analysis principles for the quadrature oscillator presented later.

However, before that, we will analyze the characteristics of the second harmonic (current and voltage) and will show the influence of the impedances connected in the even nodes and the parasitic capacitances on the phase relation between the first and the

second harmonics. So, let us find the I and Q current components related to the voltage at the sources of the MOS transistors $V_2\cos(2\omega t+\varphi_2)$. These currents ($I'_{2I}$ and I'_{2Q}) are directly related to the components I_{2I} and I_{2Q} found previously through the jacobian matrix:

$$\begin{aligned} I'_{2I} &= I_{2I}\cos(2\theta_1-\varphi_2)+I_{2Q}\sin(2\theta_1-\varphi_2) \\ I'_{2Q} &= I_{2Q}\cos(2\theta_1-\varphi_2)-I_{2I}\sin(2\theta_1-\varphi_2) \end{aligned} \qquad \textbf{(3.13)}$$

Now, let us consider two different impedances connected at the sources of the MOS transistors, a purely resistive load (as the output resistance of an ideal current source or a resonator) and a purely reactive impedance (as an inductor). These impedances establish two different boundary conditions in the oscillator solution. For a resistive load, the quadrature component of the current I'_{2Q} must be cancelled. Instead, for an inductor, the in-phase component I'_{2I} must be cancelled. Since I'_{2Q} and I'_{2I} depend on V_1, V_2 and $\varphi_2-2\theta_1$ it results that different values of V_2 and $\varphi_2-2\theta_1$ are obtained for the same value of V_1 depending on the type of impedance connected at the transistor sources.

As we will show in detail in next section in the analysis of injected oscillators, changes in the relative phase of the first and second harmonic modify the resonant frequency of the oscillator. This could suggest the possibility of tuning the oscillator frequency by using a variable load (as a variable resonant tank) at the sources of the cross-pair. Unfortunately, although it is possible, the resulting tuning range is very narrow (≈1%).

Combining (3.8) and (3.13), simple expressions for I'_{2I} and I'_{2Q} can be found when both transistors remain in the saturation region during the whole oscillation cycle as:

$$\begin{aligned} I'_{2I} &= \frac{kV_1^2}{8}\cos\left(2\theta_1-\varphi_2\right)+\frac{k(V_{CC}-V_{TH})V_2}{2} \\ I'_{2Q} &= -\frac{kV_1^2}{8}\sin\left(2\theta_1-\varphi_2\right) \end{aligned} \qquad \textbf{(3.14)}$$

If a purely inductive load is attached at the sources nodes, I'_{2I} must be cancelled and as consequence, $\pi/2<2\theta_1-\varphi_2<3\pi/2$. This fact has been corroborated using SPECTRE RF simulations of a cross-pair with Conexant BC35 models.

Although the previous equations for the second harmonic currents can not reproduce exactly the actual values found in SPECTRE simulations, they allow us to point out

some important facts. In particular, let us calculate the second harmonic impedance seen at the sources node and defined as:

$$Z_{2f} = \frac{V_2}{I_2} = \frac{V_2}{\sqrt{I_{2I}^2 + I_{2Q}^2}} \tag{3.15}$$

$$I_2^2 = \left(\frac{kV_1^2}{8}\right)^2 + \left(\frac{k(V_{CC} - V_{TH})V_2}{2}\right)^2 + k(V_{CC} - V_{TH})V_2\left(\frac{kV_1^2}{8}\right)\cos(2\theta_1 - \varphi_2)$$

(3.15) shows explicitly that Z_{2f} depends not linearly on V_2 and hence increasing the impedance attached to this node does not involve increasing the second harmonic voltage. As we will see in the analysis of injected oscillators, performed in the next section, this voltage should be maximized to increase the oscillator locking range.

3.3. Injected Oscillators

In 1940, Adler realized that under certain conditions, it is possible to modify the free running frequency of an oscillator and to synchronize it to an incident or interferer signal provided both frequencies (or their harmonics) are close enough [13]. This phenomenon is known as injection locking. Depending on the frequency ratio between the incident and the oscillator signals, three different cases of injection can be defined: first harmonic, sub-harmonic (the incident signal is a sub-harmonic of the oscillation frequency) and super-harmonic (the incident signal is a harmonic of the oscillation frequency).

The locking phenomenon requires the existence of a non-linear element capable of translating energy between different frequencies (even if the injection is realized at the fundamental frequency), but it is relatively independent on the specific properties of the non-linear device. Thus, bipolar or MOS transistors as well as p-n or Schottcky diodes (or more rare devices as Gunn or IMPATT diodes) have been used in different injection-locked oscillators designs. However, it is noteworthy that the characteristics of the device may favor the injection of a particular harmonic. Thus, for instance, second harmonics are efficiently injected in circuits containing MOS transistors due to their quadratic characteristics.

Besides the characteristics of the non-linear device, another important issue to consider for an efficient injection is the node to be injected and the type of injection. Namely, differential (odd) harmonics should be injected differentially in differential nodes as long as even harmonics should be injected in common-mode nodes. Moreover, since the magnitude of the Fourier coefficients in the expansion of the non-linearity usually decreases when the order increases, the higher harmonics (or smaller sub-harmonics) are injected less efficiently. Fig.3-8 shows an example of how the same oscillator can be injected by different harmonics provided the injection is applied conveniently.

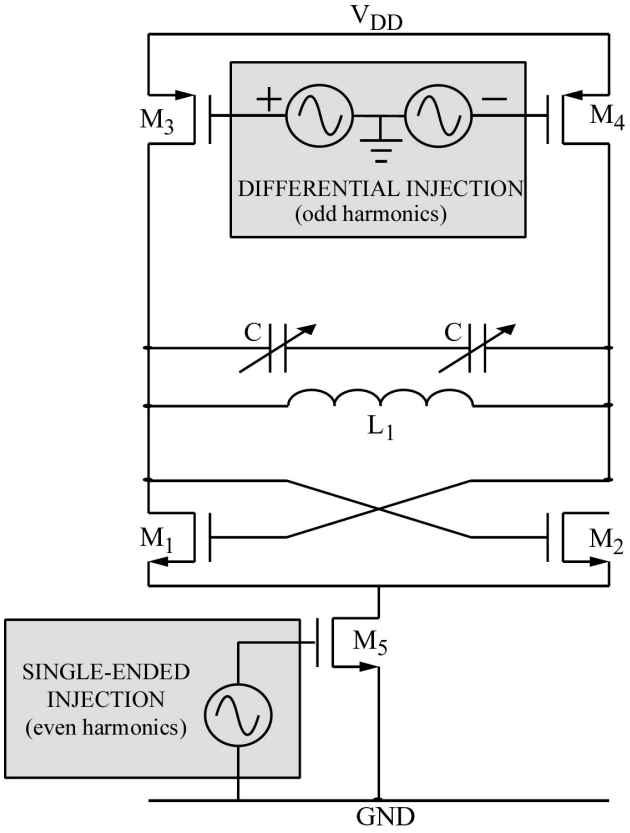


Figure 3-8. 2nd Harmonic Currents vs. the oscillation amplitude for a MOS cross-pair

In this section, we are interested in the analysis of the injection of the second harmonic. Actually, Rategh and Lee have already shown for an oscillator based on a MOS cross-pair, that it is possible to use a common-mode node to inject a frequency close to twice the fundamental frequency and lock the oscillator over a certain frequency band known as locking range [14]. However, we would like to extend this analysis using the results obtained in section 3.2 in order to obtain some additional understanding on the locking process as well as some analytical expressions useful for design purposes.

Thus, let us revise the expressions for the currents found in the non-linear analysis of the cross-pair. In these equations, it has been assumed that the frequency of V_2 is twice the fundamental frequency the oscillator, independently on the origin of this second harmonic. Thus, an injected signal at 2f or the natural second harmonic of the oscillator will satisfy identical expressions as long as the oscillator is able to track this injected signal.

According to (3.8)-(3.10) and in absence of V_2, the harmonics of the current are in-phase with the first harmonic voltage (since the parasitic capacitances of the transistors are neglected). However, in presence of a 2f signal at the sources (or drains) of the MOS transistors appear additional contributions in quadrature with the first harmonic voltage. These quadrature components (Q) are proportional to $\sin(\varphi_2-2\theta_1)$ as long as the in-phase components (I) are proportional to $\cos(\varphi_2-2\theta_1)$. The quadrature components modify the apparent properties of the resonant tank and may shift the oscillator free-running frequency to the injected frequency provided both frequencies (or their harmonics) are close enough and/or the injected signal has enough power.

To understand why these quadrature components modify the resonant frequency of the tank, let us revise the simple LCR parallel tank. At the resonance, the net current and the voltage across the resonator are in phase as long as the currents in the inductor and the capacitor (in quadrature with the net current and Q times higher) cancel each other. When a signal is injected, it appears a net quadrature current, which modifies the balance between the inductor and capacitor currents and causes a shift in the resonant frequency that tries to re-establish the current balance. Actually, according to (3.8) and (3.9) the quadrature components of the current can be modeled by a reactive admitance given by $Y_1=\frac{I_{1Q}}{V_1}=-\frac{k}{4}V_2\sin\phi$ that will act as an inductor or a capacitor depending on the sign of $\sin\phi$.

It should be noted that this re-tuning occurs due to the presence of a second harmonic independently of its nature (injected or non-injected). Thus, the oscillator frequency could not match the resonant frequency of the tank even if the parasitic capacitances of the active devices are considered as a part of the tank. Besides, since even for the free-

running oscillator it exists already a phase shift ϕ different than zero, it is expected that the locking range will not be symmetrical around the free-running frequency. From the currents I_{1I} and I_{1Q} deduced previously, it is possible to obtain the phase deviation of the first harmonic net current due to the injection as $\Delta\theta = \tan^{-1}\frac{I_{1Q}}{I_{1I}} \approx \frac{I_{1Q}}{I_1}$. Thus, as long as the transistor is not turned off during the oscillation period, the following expression can be derived for the locking range using (3.8) and (3.9):

$$\frac{kV_1V_2\sin(2\theta_1-\varphi_2)}{4I_1} = \frac{2Q}{\omega_o}\Delta\omega \qquad \textbf{(3.16)}$$

or equivalently:

$$\frac{\Delta\omega}{\omega_o} = \frac{kZ_oV_2}{8Q}\sin(\varphi_2-2\theta_1) \qquad \textbf{(3.17)}$$

where Z_0 is the tank impedance at the resonant frequency.

(3.17) is an explicit form of the famous Adler's equation in terms of circuit or design parameters and establishes that there is a limited frequency range (locking bandwidth) where the oscillator can be locked to the injected signal. The phase $\Delta\phi=2\theta_1-\varphi_2$ is the steady-state phase difference between the oscillator and the injected signal. Thus, when the injected signal sweeps the locking bandwidth, the phase difference $\Delta\phi$ will vary between –90° and 90°.

Besides the phase condition given by (3.16), an additional condition on the gain must be satisfied in order to obtain the oscillator locking. This condition establishes that the cross-pair should synthesize a negative impedance high enough in order to compensate the resonator losses, and can be written in the saturation region of the cross-pair as:

$$\frac{k}{2}(V_{CC}-V_{TH})+\frac{k}{4}V_2\cos(\varphi_2-2\theta_1) > \frac{1}{Z_0} \qquad \textbf{(3.18)}$$

The injection locking fails and the locking range is limited by failure of either the phase or the gain conditions. Next figure shows the evolution of the amplitude of the fundamental harmonic as well as the phase shift ϕ all along the complete locking range of the oscillator shown in fig. 3-9b for two different amplitudes of the injected signal.

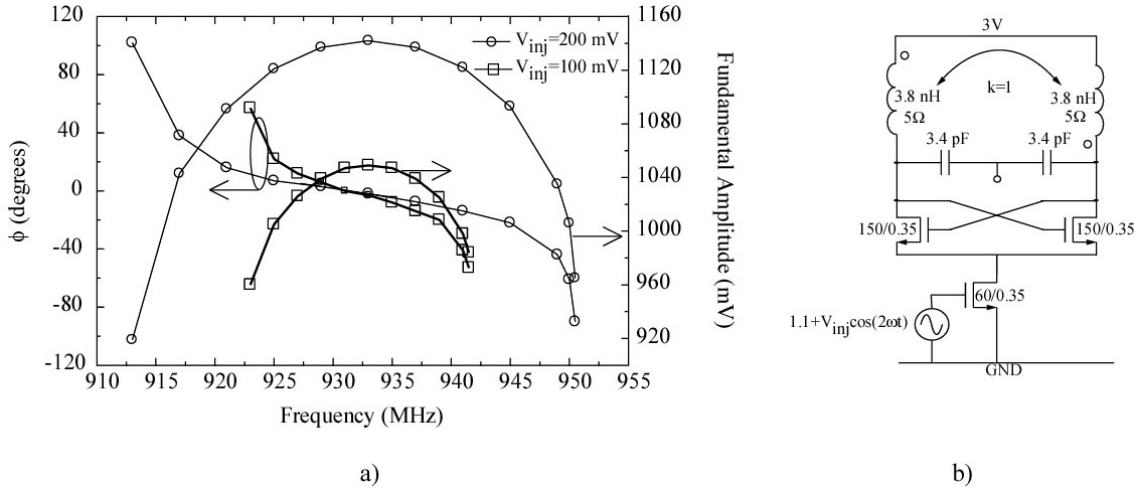


Figure 3-9. Variation of the first harmonic amplitude and the phase shift between the first and the second harmonics along the oscillator locking range

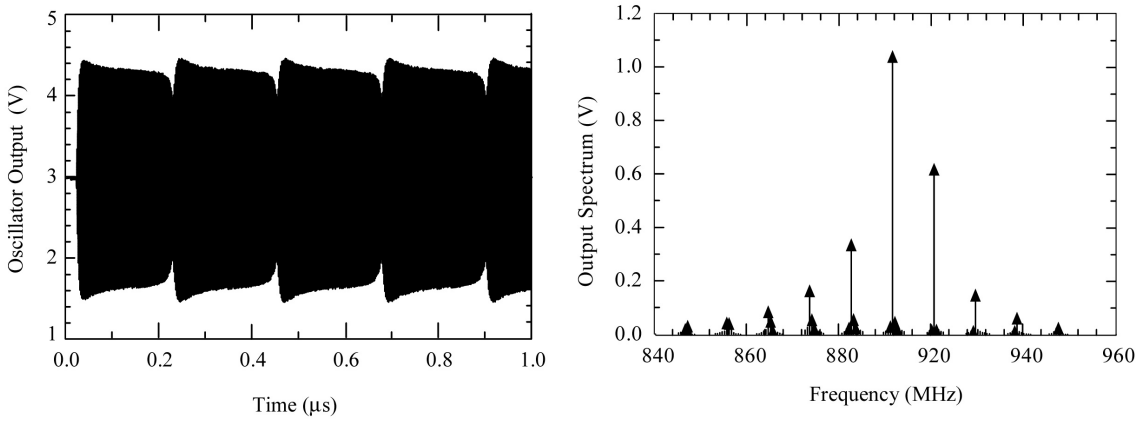


Figure 3-10. Signal in the time domain and Output Spectrum of an unlocked oscillator

For completeness, fig.3-10 shows the characteristic waveforms (signal in time domain and spectrum) of an unlocked oscillator. In the time domain, the output of the unlocked oscillator shows a complex modulation in both amplitude and phase as reflected in its spectrum.

(3.17) suggests that the locking range grows with Z_0/Q or with the amplitude of the injected signal V_2. Increasing Z_0/Q in a LC oscillator is equivalent to using an inductor of larger value. The self-resonant frequency of the inductor sets the maximum inductor size and limits the locking range by failing to satisfy the phase condition. The locking can also be extended increasing the injected power or using at least one high impedance common-mode node (not necessarily the injection node). Resonant tanks or current sources can be used to implement these high impedance nodes. However, this increase with V_2 is also limited.

To point out the influence of the second harmonic impedances in the locking range, let us compare two implementations, based on MOS and BJT transistors respectively, of the same oscillator topology. In both oscillators, if a current source is used as a injection device, the voltage at the sources (or emitters) should not move the device to the linear region (saturation for the BJT's) in the whole range of injected power. Otherwise, increasing the injected power could result in a decrease of the locking range. An integrated transformer can be also used as linear injecting device substituting the current source and lowering the power supply voltage required for the circuit. In this case, the previous topologies have an important difference. Due to the transformer used in the resonator, the drain and gate of the transistors are grounded and as a consequence, the only voltage at 2f is found at the sources of the cross-pair. If a low impedance (as a transformer in differential mode) is attached at this node, this voltage will be small and the injection poor. Thus, in the MOS implementation a current source or a resonator at 2f can improve the efficiency of the injection. Instead, in the BJT implementations, two feedback capacitors are usually connected between the collectors (grounded at 2f) and the bases in order to avoid the saturation of the transistors in the cross-pair. Thus, a significant voltage signal at 2f can be found at the bases of the transistors and no additional impedance at 2f is required to obtain a large locking range.

Surprisingly and according to (3.17), the oscillator locking range does not depend on the quality factor of the resonator tank. This independence is due to the assumption performed in the derivation of (3.17) that $I_1 \approx I_{1I}$ or equivalently that I_{1Q} is negligible compared to I_{1I}. However fig. 3-6 shows that although I_{1Q} is smaller than I_{1I} still has the same order of magnitude. Thus, there is an actual dependence of the locking range on the quality factor that becomes even more evident for large values of V_1, i.e. when the transistors are switched off during part of the oscillation cycle (see fig.3-6). Next figure shows the locking range versus the resonator (or inductor) quality factor of the oscillator shown in figure 3-11b for two different amplitudes of the injected signal.

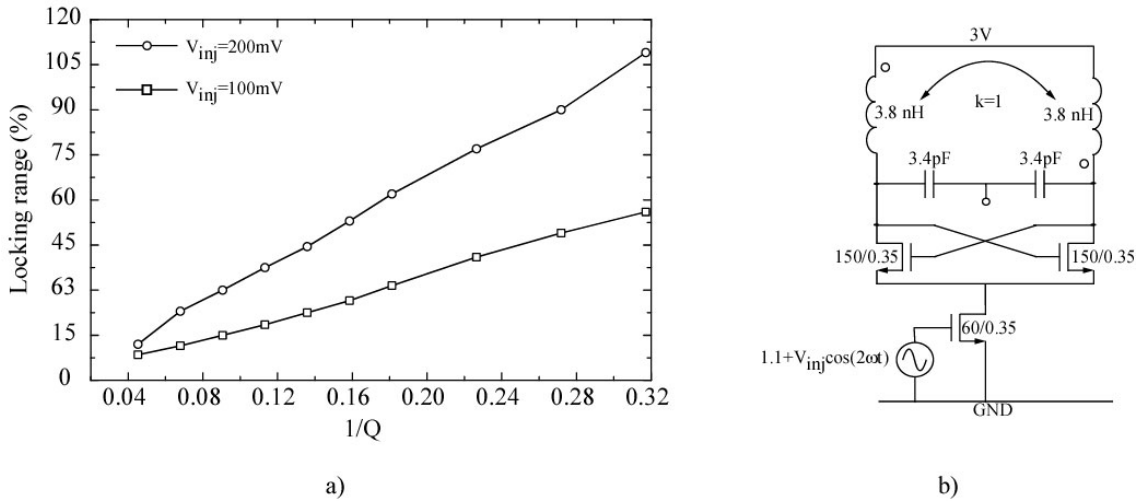


Figure 3-11. Locking range vs. the quality factor of the resonator

The most important conclusion of this analysis regarding the design of the proposed quadrature oscillator is that the angle $\phi=\varphi_2-2\theta_1$ depends just on $\Delta\omega$. Thus, if the phase of the injected signal φ_2 is modified in δ degrees (as long as its frequency is kept constant), the phase of the fundamental will change in $\delta/2$ degrees since ϕ should not change. From this point of view, the oscillator is working as an analog frequency divider if we consider the fundamental harmonic as the circuit output. As a consequence, if two identical oscillators are injected by two-second harmonics with a phase shift of 180 degrees, their fundamental output will be in quadrature. The fig. 3-9 shows a quadrature oscillator based on this principle. In next section we will study the possibility of removing the differential oscillator at 2f by coupling properly two oscillators.

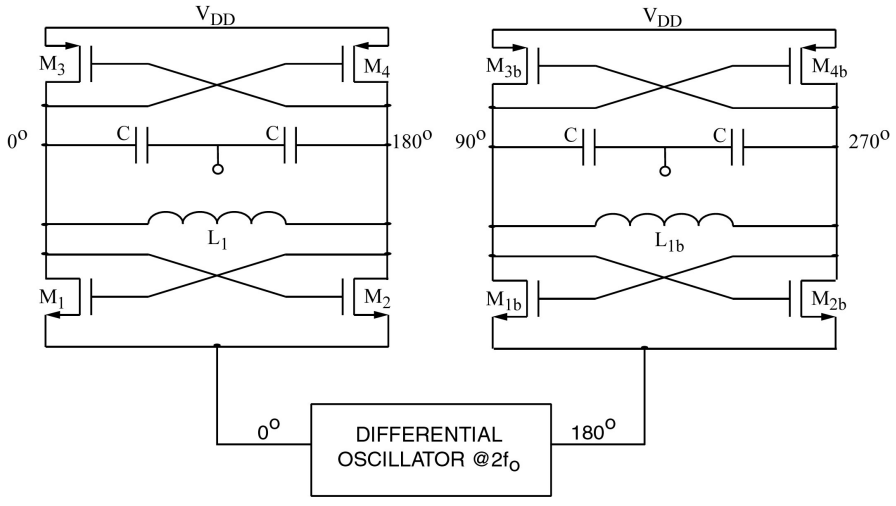


Figure 3-12. Quadrature oscillator based on the injection of a differential second harmonic

3.4. Coupled Oscillators

The dynamics associated to coupled oscillators is inherently non-linear and has a rich set of possible states, ranging from the chaotic behavior to the mutual synchronization or locking. The conduct of the coupled system depends basically on the coupling network (the tendency to lock increases with increased coupling strength) rather than on the detailed description of each individual oscillator [15,16]. This fact explains why many different kinds of oscillators, when coupled, show a similar behavior.

Thus, to analyze the dynamics of two coupled oscillators, a simple oscillator model consisting in a parallel RLC resonator and a non-linear device that restores the energy dissipated in the tank can be used. Analogous results can be obtained using a series resonator model [17].

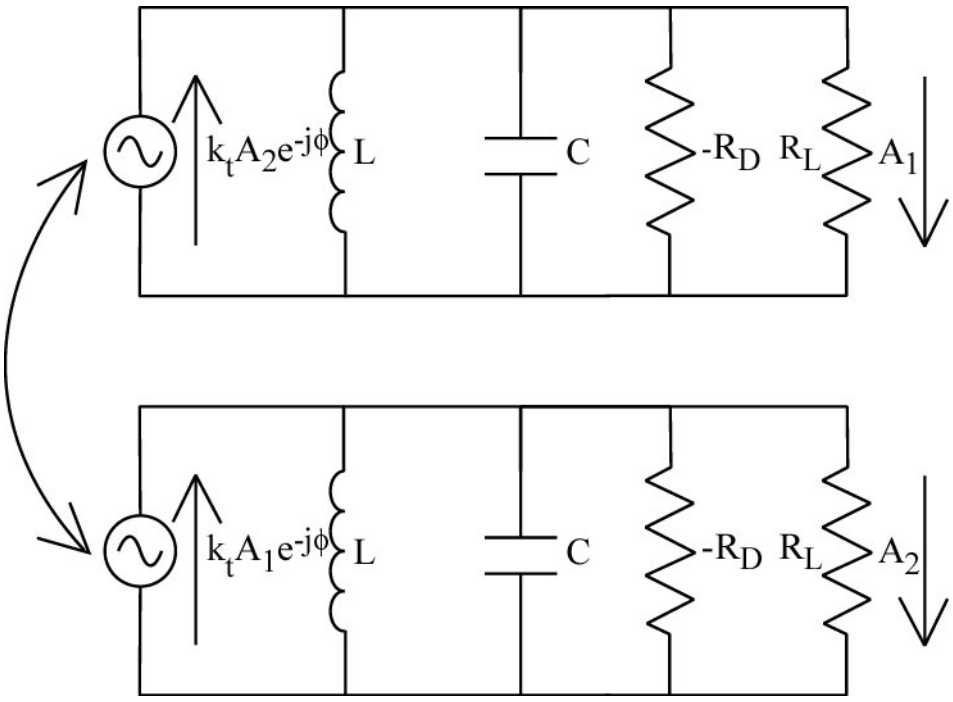


Figure 3-13. Oscillator model used in the analysis of coupled oscillators

Assuming an output current given by:

$$I(t) = A(t)e^{j\theta(t)} \tag{3.19}$$

and applying the KCL to a single oscillator equivalent circuit, where I_{inj} takes into account any injected signal, the following independent differential equations for the amplitude and phase dynamics are obtained:

$$\frac{dA}{dt} = -\frac{\omega_o}{2Q} A\left(1 - \frac{R_D}{R_L}\right) + \frac{\omega_o}{2Q} \mathrm{Re}\left\{\frac{I_{inj}}{I}\right\}$$
$$\frac{d\theta}{dt} = \omega_o + \frac{\omega_o}{2Q} \mathrm{Im}\left\{\frac{I_{inj}}{I}\right\} \quad \textbf{(3.20)}$$

where I is the current phasor, ω_o is the resonant frequency of the tank and Q is its quality factor. The quality factor Q has been defined in terms of the phase slope as in (2.13) and for a parallel resonator can be written as $\omega_o RC = \frac{R}{L\omega_o}$. Moreover, it has been assumed that the quality factor is high enough so that the oscillator frequency remains close to ω_o and therefore, the changes in the current phasor amplitude and phase will be small in a single period. For low level injected signals, the oscillation amplitude also remains close to its free-running value and the system is basically governed by the differential equation for the phase variables.

If the injected current is written as:

$$I_{inj} = A_{inj} e^{j\theta_{inj}} \quad \textbf{(3.21)}$$

the previous phase equation becomes:

$$\frac{d\theta}{dt} = \omega_o + \frac{\omega_o}{2Q} \frac{A_{inj}}{A} \sin\left(\theta_{inj} - \theta\right) \quad \textbf{(3.22)}$$

which is a general form of the famous Adler equation deduced previously (3.16 and 3.17) for injection locked oscillators (ILO's). However, it should be noted that the analysis of injection locking performed in the previous section is a steady-state analysis (equivalent to a harmonic balance analysis). This equation is more general since it can predict the dynamics of the system (not just the steady-state solution) provided the assumptions realized in its deduction are valid.

Consider now two identical oscillators coupled through a passive circuit with a coupling factor given by $k_t e^{j\Phi}$. Since coupled oscillators can be seen as mutually injected oscillators, the equations 3.20 are still valid. Moreover, if k_t is <<1, the amplitudes of the oscillators will then remain close to their free running amplitudes and the system dynamics will be described predominantly by the coupled phase equations [18].

But even if the coupling modifies the amplitude of the oscillators, it should be noticed that the phase equations are independent on the amplitude provided both oscillators

have the same amplitude. The eventual modification of the free-running amplitude (and even the frequency) caused by the coupling could be then considered by modifying the different elements L, C and R of the oscillator model. Nevertheless, at this point, we are interested exclusively in the phase dynamics of the coupled oscillators that is given by the following coupled equations:

$$\begin{aligned}\frac{d\theta_1}{dt} &= \omega_1 + \frac{k_t\omega_1}{2Q}\frac{A_2}{A_1}\sin(\theta_2-\theta_1-\Phi)\\ \frac{d\theta_2}{dt} &= \omega_2 + \frac{k_t\omega_2}{2Q}\frac{A_1}{A_2}\sin(\theta_1-\theta_2-\Phi)\end{aligned} \qquad \textbf{(3.23)}$$

where θ_1,θ_2 and ω_1,ω_2 are the phases and frequencies of oscillators 1 and 2. Subtracting these equations results in:

$$\frac{d\psi}{dt} = \Omega - 2\alpha\cos\Phi\sin\psi \qquad \textbf{(3.24)}$$

where $\Omega = \omega_1-\omega_2$, $\psi=\theta_1-\theta_2$ and $\alpha = \frac{k_t\omega_1}{2Q} \approx \frac{k_t\omega_2}{2Q}$. This expression can be seen as a generalization of Adler equation for coupled oscillators. Integrating (3.24) it is possible to obtain a general solution for the phase difference between both oscillators:

$$dt = \frac{d\psi}{\Omega - 2\alpha\cos\Phi\sin\psi} \quad with \quad |\Omega| < 2\alpha|\cos\Phi| \qquad \textbf{(3.25)}$$

resulting in:

$$\tan\frac{\psi}{2} = \frac{2\alpha\cos\Phi}{\Omega} - \frac{\sqrt{4\alpha^2\cos^2\Phi-\Omega^2}}{\Omega}\tanh\left[\frac{\sqrt{4\alpha^2\cos^2\Phi-\Omega^2}}{2}(t-t_0)\right] \qquad \textbf{(3.26)}$$

where t_o determines the initial phase at t=0. Notice that this solution is just valid if $|\Omega| < 2\alpha|\cos\Phi|$, that is, if the locking is possible. Actually, in the locked state, it should be verified that $\frac{d\psi}{dt} = 0$ and hence (3.24) can be directly solved resulting in:

$$\psi_1 = \sin^{-1}\frac{Q\Omega}{k_t\omega_0\cos\Phi} \qquad \textbf{(3.27)}$$

There are two possible solutions for (3.27), ψ_1 or π-ψ_1. In the general case of N-coupled oscillators, 2^{N-1} different phase distributions may be possible. However, not all of them are stable states. The coupled system will be stable if a small perturbation in the phase difference decays with the time. Thus, the following stability condition can be established:

$$\frac{d^2\psi}{dt^2} = -2\alpha\cos\Phi\cos\psi > 0 \qquad \textbf{(3.28)}$$

$\cos\Phi\cos\psi > 0$

Let us suppose a real coupling factor ($\Phi=\pi$ and $\Phi=0$) as it is found for many coupling networks (resistors based, transformers, etc). In these cases, the stable phase difference will tend to π for $\Phi=\pi$ and to 0 for $\Phi=0$ (both natural configurations for two coupled oscillators) as the frequency difference tends to zero:

$$\begin{aligned}\psi\big|_{\Phi=\pi} &\approx \sin^{-1}\left(\frac{Q\Omega}{k_t\omega_o\cos\Phi}\right)\rightarrow\pi \\ \psi\big|_{\Phi=0} &\approx \sin^{-1}\left(\frac{Q\Omega}{k_t\omega_o\cos\Phi}\right)\rightarrow 0\end{aligned} \qquad \textbf{(3.29)}$$

Identical results would be obtained from (3.26) taking into account that the hyperbolic tangent tends to 1 when its argument (time) tends to infinitum and applying the stability conditions.

For completeness, we can also find the common locking frequency $\omega_L = \frac{d\theta_1}{dt} = \frac{d\theta_2}{dt}$ as:

$$\omega_L = \frac{\omega_1+\omega_2}{2} - \alpha\sin\Phi\cos\psi = \frac{\omega_1+\omega_2}{2} \pm \alpha\sin\Phi\sqrt{1-\left(\frac{\Omega}{2\alpha\cos\Phi}\right)^2} \qquad \textbf{(3.30)}$$

Once again, the appropriate sign in (3.30) is determined by the stability condition.

(3.27) plays a fundamental role in the design of the presented quadrature topology since it shows the dependence of the steady-state phase shift (at the second harmonic) in terms of different design/circuit parameters (frequency, frequency mismatch, coupling factor and quality factor). Thus, two oscillators with the same natural frequency coupled at the second harmonic with a coupling network with $\Phi=\pi$ (as an inverter transformer) will result in a perfect quadrature at the fundamental frequency. As a consequence, the differential oscillator at 2f shown in fig. 3-12 can be substituted by an integrated transformer with important saving in area and power consumption. Mismatches between the natural frequencies of the coupled oscillators will result in departures from the quadrature.

3.5. Design Considerations for Quadrature Oscillators

In this section we will revise the hypothesis and results of the analysis performed in the previous sections and will apply them to the design of a quadrature oscillator. Also, we will identify the different phenomena (parasitic coupling, oscillator mismatches) that degrade the oscillator performance and point out the design parameters that affect directly the accuracy of the quadrature. In sake of simplicity, this discussion will be mainly focused on the oscillator shown in fig. 3-16 but could be also applicable to other oscillator topologies.

In section 3.4 we have assumed that the dynamics of the coupled oscillators was governed by the phase equations, i.e, that the signal amplitudes were lightly affected by the oscillator coupling. Since the coupling is established at the second harmonic, this hypothesis is very reasonable for the first harmonic, the stronger signal in the circuit that drives the transistor non-linearities. Nevertheless, this assumption on the second harmonic amplitude at the sources of the cross-pair has to be revised because the coupling affects the impedance attached to this node.
In the uncoupled situation, this impedance is the inductance L of the primary (or the secondary) of the transformer if the transistors parasitics are neglected. When coupled, this impedance becomes L-M, since the transformer is working in its differential mode (in any of the stable conditions). Thus, for coupling factors of 0.7-0.8, the inductance attached to the sources node is reduced to 0.2-0.3L. This could cause a considerable reduction of the voltage V_2 of this node if it is assumed that this node is driven by a constant current at 2f generated by the 'rectification' of first harmonic voltage. To analyze this fact, an isolated oscillator has simulated for different values of inductance ranging from 1nH to 10 nH attached to the sources node as long as the voltage V_2 has changed exclusively from 250 to 480 mV. This fact corroborates the observations performed in the deduction of (3.15), that points out that V_2 does not increase linearly with the impedance attached to the sources node (Z_{2f}) amplitude and has a strong dependence with $\phi=\varphi_2-2\theta_1$.

Still an additional argument can be invoked to justify the relevance of the phase over the amplitude dynamics. Since the second harmonic is much smaller than the fundamental

(few hundreds of mV compared to few volts), the non-linearities present in the circuit (basically the I-V characteristic of MOS devices) are mainly driven by the fundamental harmonic. Thus, the dynamics for the second harmonic amplitude will be quasi-linear around the periodic-state solution of the free-running oscillator. Such a linear dynamics can not handle the phenomena of mutual synchronization between oscillators.

In the analysis of coupled oscillators the following expressions have been obtained for the steady state phases:

$$\psi\Big|_{\Phi=\pi} \approx \sin^{-1}\left(\frac{Q\Omega}{k\omega_o \cos\Phi}\right)\rightarrow\pi$$
$$\psi\Big|_{\Phi=0} \approx \sin^{-1}\left(\frac{Q\Omega}{k\omega_o \cos\Phi}\right)\rightarrow 0 \qquad \textbf{(3.31)}$$

However, some comments have to be made in order to apply this analysis to our design. First of all, the LCR model used for each oscillator could be deduced straightly for our circuit if the coupling had been established at the first harmonic. However, in our design there is no resonator at the coupling frequency (2f), so what is the meaning of the quality factor in the previous equations? To answer this question we should remember that the phase of the first and second harmonic are related by $\phi=2\theta_1-\varphi_2$ (with ϕ constant in the locked state) and that in the locked state the oscillator works as an argument divider for the injected signal. Thus, applying the definition of Q:

$$Q_{2f} = -\frac{\omega_{2f}}{2}\frac{d\varphi_2}{d\omega}\bigg|_{\omega=\omega_{2f}} = \omega_0\left[\frac{d\phi}{d\omega} - \frac{2d\theta_1}{d\omega}\right]_{\omega=\omega_0} \qquad \textbf{(3.32)}$$

(3.17) gives us the dependence of ϕ with the frequency for small values of ϕ. Thus, substituting (3.17) in (3.32) results in:

$$Q_{2f} = Q\left(2-\frac{4}{kZ_0V_2}\right) = 2Q - \frac{4Q}{kZ_0V_2} \qquad \textbf{(3.33)}$$

It is noteworthy that according to (3.33) the value of Q_{2f} depends not just on the specific properties of a component but also on the operating conditions of the circuit, and in particular, on the second harmonic amplitude. Thus, in order to determine its value, the circuit has to be previously solved. To shown the actual dependence of the phase deviation from the quadrature with Q_{2f} (i.e, with Q), two coupled oscillators with small mismatches in their resonant frequencies have been simulated for two different values of the resonator quality factor Q. The results obtained for the circuit shown in fig. 3-16.

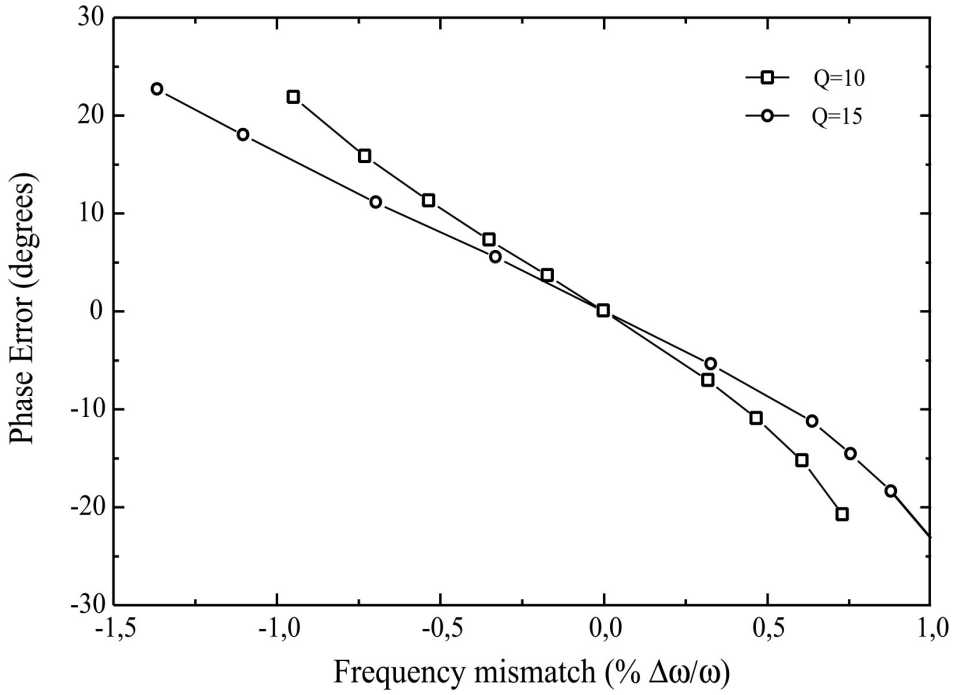


Figure 3-14. Deviation from the quadrature vs. the mismatch frequency between the coupled oscillators

The preceding equations constitute the basic design equations for the presented quadrature oscillator, pointing out the different parameters involved in the accuracy of the quadrature. In particular the matching between the free running frequencies of both coupled oscillators has been identified as the factor limiting the accuracy of the quadrature as it also occurs in ring or cross-coupled oscillators.

If the effects of the parasitic elements on the resonant frequencies of the oscillators are neglected, the mismatching between the capacitors and inductors constituting the resonant tanks will be responsible for the mismatch of the oscillator free running frequencies. Thus:

$$\left|\frac{d\omega_0}{\omega_0}\right| = \frac{1}{2}\omega_0^2(CdL + LdC) \qquad \textbf{(3.34)}$$

and if the same error in terms of percentage is assumed for inductors and capacitors, (dL=εL=dC=εC) the previous equation becomes:

$$\left|\frac{d\omega_0}{\omega_0}\right| = \varepsilon \qquad \textbf{(3.35)}$$

The discussion on coupled oscillators has also pointed out the role of the transformer in our circuit. It establishes a strong coupling between both oscillators (the stronger the better) and synchronizes their frequencies (injection locking) even if there is some mismatch between the resonant frequencies of the independent tanks. Moreover, the configuration of the transformer, inverter or non-inverter, has direct influence on the relative steady phase between oscillators. Thus, an inverter transformer forces the required phase-shift of 180 degrees between the second harmonics at the sources of NMOS transistors in order to obtain the quadrature at the fundamental. Instead, a transformer in a non-inverting configuration results in the oscillators coupled in the on-phase-state, and in-phase outputs at the fundamental frequency. It is also remarkable that the phase shift of practical inverter transformers separates from the ideal 180 degrees when the frequency increases, due mainly to the parasitic capacitances. But still, according to (3.31) it could result in a quadrature oscillator, provided both coupled oscillators are well matched.

Besides having a high coupling factor, the transformer should be also as symmetric as possible in order to keep the matching between the coupled oscillators. Thus, a layout as the one proposed in the fig. 3-15 is strongly recommended for this application.

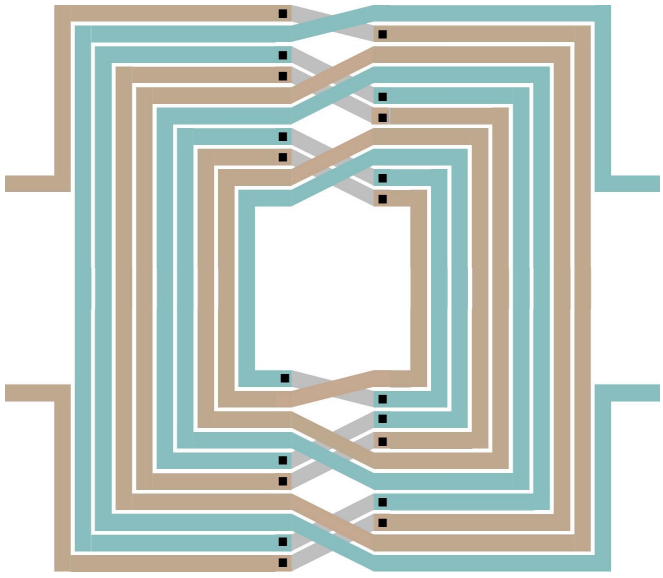


Figure 3-15. Transformer layout used to couple the oscillators in the QO.

We have also seen that there are two possible stationary phases for the coupled system (ideally, on-phase and with opposite phases) depending on the configuration of the

transformer. Thus, if the coupling between oscillators is set up at the fundamental frequency, no quadrature will be obtained. Instead the oscillators would be forced to the on-phase-state (or off-phase-state) at the fundamental frequency. Therefore, any parasitic coupling at the fundamental frequency should be avoided. This coupling can be established through the silicon substrate or via magnetic interaction between the inductors of the resonant tanks.

EM simulations of closely-spaced inductors have been carried out using Momemtum to analyze the magnetic coupling between the two planar inductors constituting the tank. Results show that for the inductor spacing used in our layout, 250 μm, the coupling is lower than -25 dB. In spite of this apparent high isolation, the power coupled directly at the first harmonic could not be negligible when compared to the injected contributions due to the second harmonics, since the fundamental harmonic is much stronger than the second one. Thus, the minimization of the coupling at the fundamental frequency should be considered as a main goal during the realization of the layout.

Different solutions can be applied to combat the effects of this parasitic coupling:
1. Increase the voltage of the second harmonic as suggested by (3.17). Although we have already show that V_2 does not increase linearly with the (inductive) impedance attached to the sources node, it is still possible to optimize this impedance to maximize V_2. Also simulations show that using a resonator tank at 2f (adding capacitors at the primary and secondary of the transformer), near to quadrature oscillations can be observed with coupling factors at the fundamental frequency as high as 0.1.
2. Minimize the coupling between the tank inductors through a proper layout (inductor area reduction, use of coupled inductors in differential designs instead of single isolated inductors, proper relative placing/orientation).

Another eventual problem is that the fundamental frequency could appear on the transformer terminals (on the sources) due to transistor mismatches. However, injection off odd harmonics in the node at the sources of the cross-pair is not efficient and this effect can be reasonably neglected.

3.6. Quadrature Oscillator Design and Test

A simplified schematic of a 900 MHz quadrature oscillator based on the differential coupling of the second harmonics and implemented in the Conexant 0.35μm BiCMOS process [19] is shown in fig. 3-16a. It consists of two complementary cross-pair CMOS oscillators (although the proposed design method is applicable to any other differential topology) coupled through an integrated transformer. The standard complementary CMOS cross-pair topology has been used since it reduces the up-conversion of the 1/f noise due to symmetry properties of the resulting periodic waveform [20]. In this first prototype we have used fixed capacitors rather than varactors in order to increase the simplicity of the design and test of the circuit. Nevertheless, the inclusion of varactors seems to be straightforward and would allow us to analyze experimentally the phase deviation from the quadrature in terms of the frequency mismatch between the oscillators.

The inverter transformer establishing the oscillator coupling is connected between the common-mode nodes at the sources of NMOS transistors and ground and substitutes the current source typically found at this node. Omitting the current source reduces the bias voltage required by the oscillator and removes an important noise source at the expense of an increased sensitivity to power supply changes (frequency pushing). However, if required, it is straightforward to include a NMOS or PMOS current source in this design.

The integrated transformer used consists of two closely-coupled loops of six turns with a metal width of 8 μm, a turn-to-turn spacing of 2 μm and an outer dimension of 250 μm (fig. 3-15) resulting in a coupling factor of 0.83. It was implemented using the top metal with a sheet resistance of 10 mΩ/sq, and is separated from a 10 Ω-cm silicon substrate by a silicon-dioxide layer of 3 μm. Each inductor constituting the transformer has an inductance of 5.5 nH and a Q of 9 at 1.8 GHz.

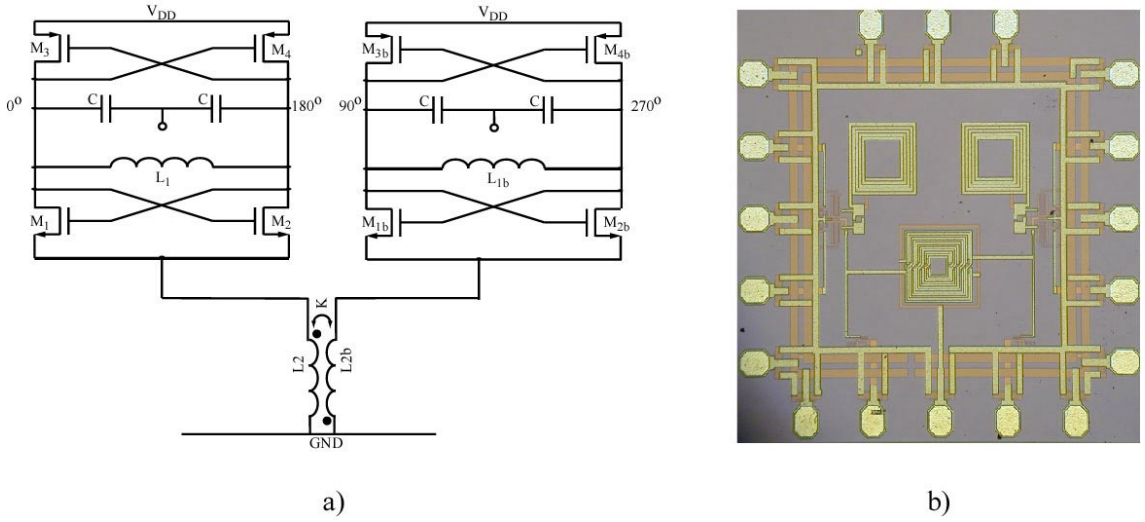


Figure 3-16. Quadrature oscillator schematic and layout

Spectre RF (Cadence) simulator was used during the design process in order to obtain the optimum sizes and bias conditions for minimum phase noise as long as a reliable startup was guaranteed for a voltage supply of 1.8V. Transistors with minimum channel length (0.35 μm) were used to minimize the parasitic capacitances. Two common-drain differential amplifier stages, biased at 5 mA per stage, and each adding around 50 fF to the resonant tanks, were used as output buffers to drive the 50 Ω measurement system.

During the layout process, special care was taken to keep the inherent symmetry of the circuit. Both NMOS and PMOS transistors were laid out as multi-finger structures in order to minimize the gate resistance. The layout of the circuit is shown in fig. 3-16b.

The VCO core consumes 3 mA (both oscillators) from a 1.8 V supply. The chip dimensions, 1250 x 1250 μm, were defined by the size of the differential probes available for on-wafer test. The outputs were measured differentially using a probe (G-S-G-S-G) from Picoprobe and then converted to single-ended signal using a 0-180° power-combiner (or directional coupler). The resulting output power was -9 dBm per oscillator at 900 MHz.

The time domain outputs were measured at Agere Systems using a 26 Gsamples oscilloscope in order to observe the quadrature conditions. The setup used to realize this measurement is shown in fig. 3-17. It includes 180-deg. couplers, power splitters and cables so it could not be perfectly matched. Therefore, some departure from the

quadrature should be associated to the measurement setup. The overall losses of this path were around 5 dB (4.3 dB due to the power splitter used to generate the trigger signal). The obtained quadrature outputs are shown in fig. 3-18. This measurement method is not suitable to measure the accuracy of the quadrature due to the mismatches between the different elements shown in fig. 3-17. A more accurate measurement could be based on the down-conversion on chip of the quadrature outputs and would require the integration on the same chip of additional elements. Also an indirect measurement could be performed using the quadrature oscillator to drive an image rejection mixer and defining the quadrature accuracy in terms of the image rejection.

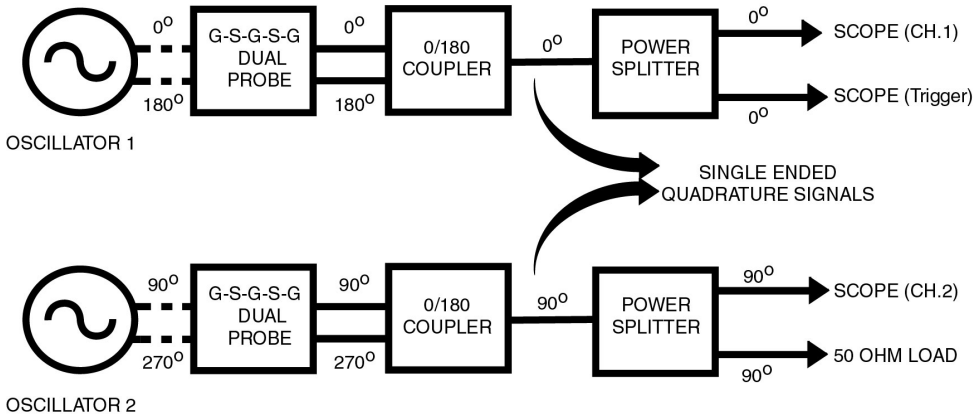


Figure 3-17. Experimental setup to measure the quadrature oscillator in the time domain

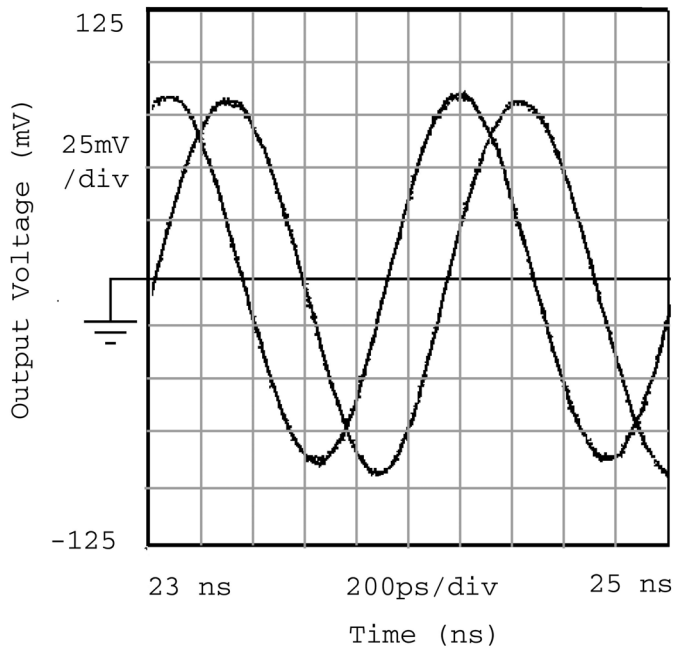


Figure 3-18. Quadrature signals in the time domain

The oscillator phase-noise was also measured in Agere Systems using the Agilent E5500 phase noise measurement system with the FM discrimination method. The delay line used in our setup introduced 27 ns of delay, establishing a trade-off between the noise floor and the maximum offset frequency measurable accurately (around 3 MHz in our case). The phase noise, shown in fig. 3-19, resulted in –116, –133 and –138 dBc/Hz at 100 KHz, 600 KHz and 1 MHz from the carrier, respectively.

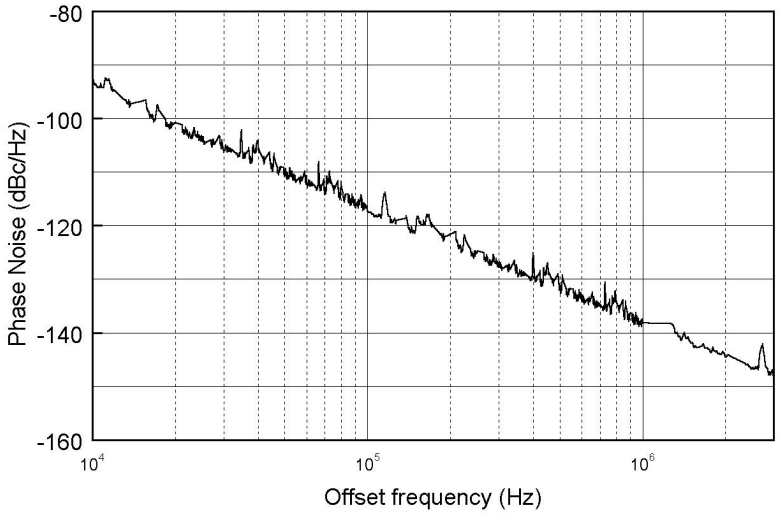


Figure 3-19. Phase Noise Measurement of the Quadrature Oscillator

3.7. Hybrid Implementation of Quadrature Oscillators

Finally, in order to illustrate the broad range of possibilities and the robustness of the presented method to generate quadrature signals, two additional circuits in a hybrid implementation have been designed.

The first circuit shown in fig. 3-20 consists in two coupled oscillators based on a single cross-pair of packaged bipolar transistors. In this case, the transformer (also packaged) that establishes the coupling between both oscillators is connected between the common mode node at the center tap of the oscillator inductors and V_{CC}. The operating frequency of this circuit was chosen around 150 MHz in order to facilitate the measurement of the quadrature signals in the time domain. These signals are shown in fig. 3-21.

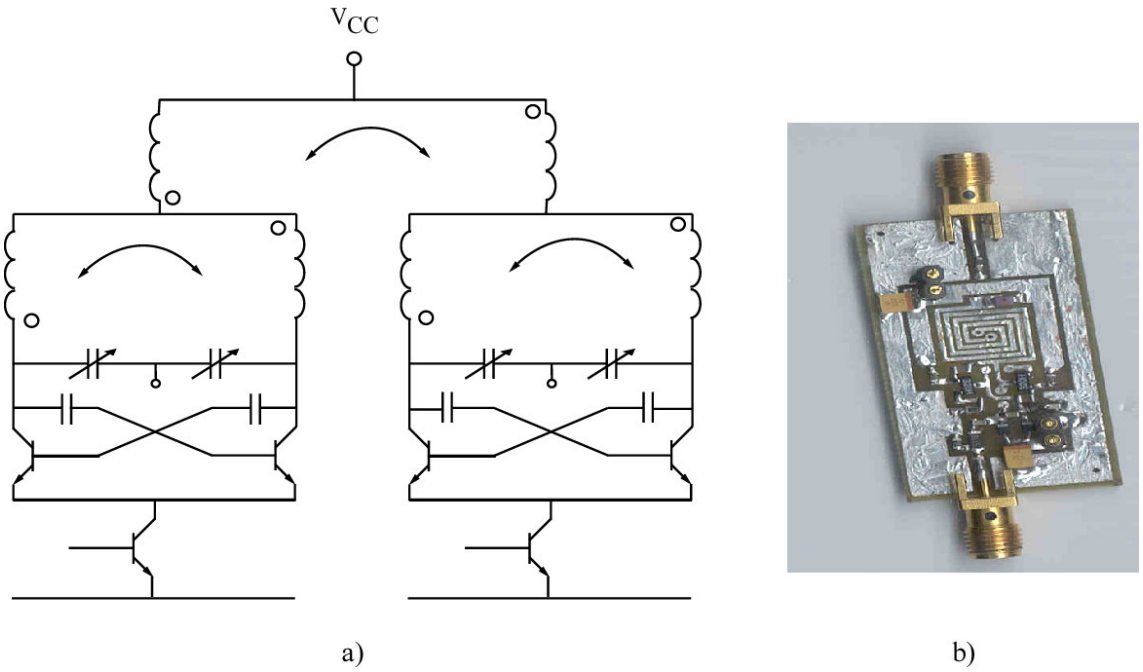


Figure 3-20. Quadrature oscillator based on a single cross-pair of packaged bipolar transistor and its hybrid implementation in a PCB board

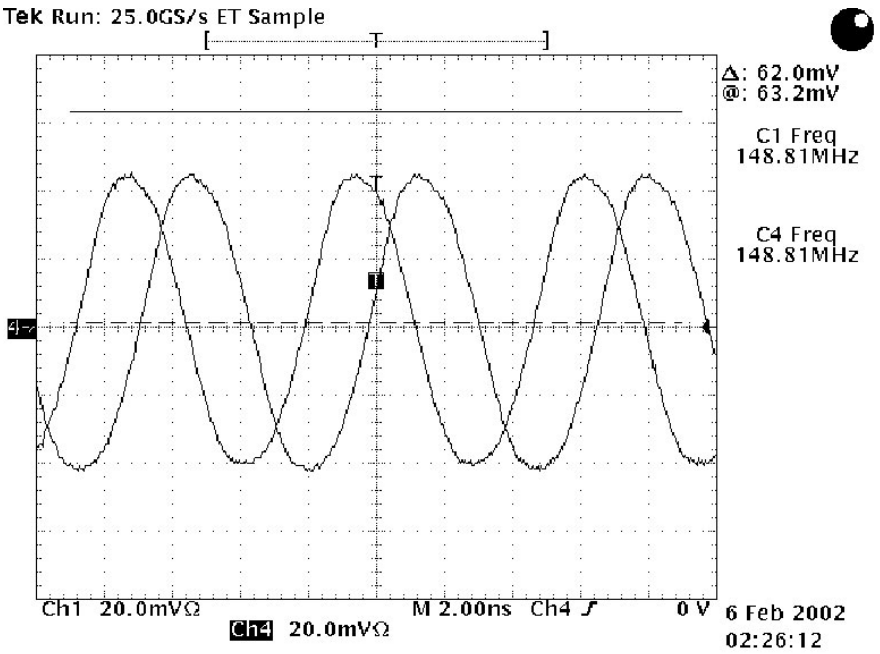
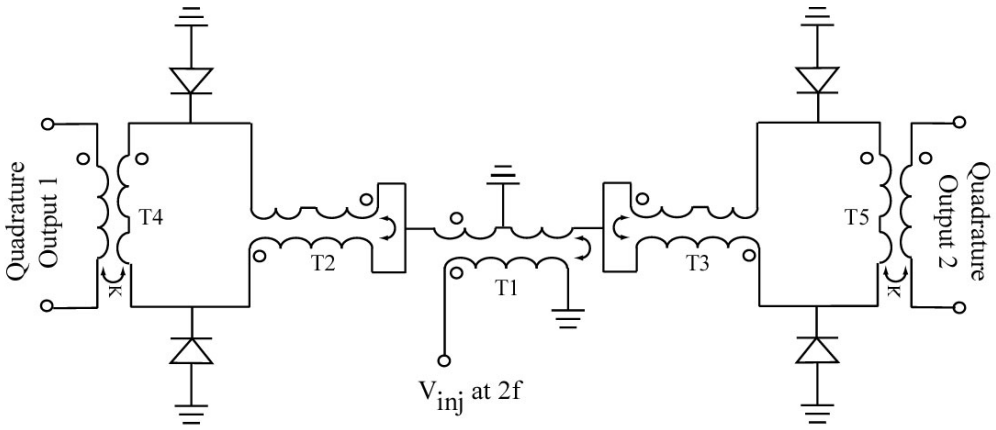


Figure 3-21. Measured quadrature outputs for the oscillator shown in fig. 3-20

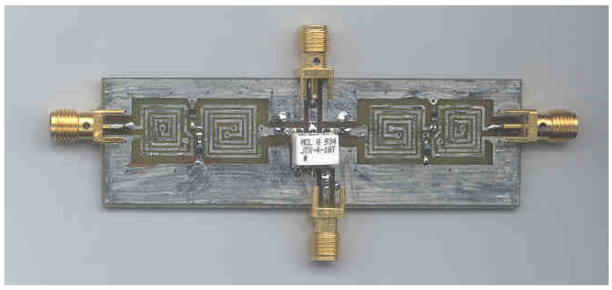
The second circuit consists in a quadrature generator (not oscillator) also implemented as a hybrid circuit [21]. In this circuit a second harmonic is injected and signals in quadrature are obtained at the fundamental harmonic as in the previous designs.

However, it has an important difference with the previous designs: in absence of the injected signal at 2f, there is no oscillation since the injected signal is used to compensate the resonator losses. Thus, the only active devices present in the circuit are the varactors used in the resonator. The schematic and layout of this quadrature generator are shown in fig. 3-22.

In spite of the large number of transformers used (proving once again their usefulness), this circuit can be easily analyzed. The transformer T1 acts as a balun generating the both phases of the second harmonic (0 and 180 degrees) that are then applied to T2 and T3. T2 and T3 have a dual function. They constitute along as with the capacitance of the varactors a resonant tank at the fundamental frequency. However, no oscillation can start up since in absence of injected signal there is no element to compensate the tank losses. Instead, for the second harmonic T2 and T3 act as short-circuits so ideally the second harmonic is applied directly to the varactors. Due to the non-linearities of the varactors, it can been seen that appears a negative resistance at the fundamental frequency proportional to the injected signal. When this negative resistor can compensate the resonator losses an oscillation starts up at half the frequency of the injected signal. Finally, transformers T4 and T5 are used as impedance adapters in order to reduce the load of the measurement system on the resonator tanks. The resulting quadrature outputs are shown in fig. 3-23.



a)



b)

Figure 3-22. Quadrature generator and its hybrid implementation

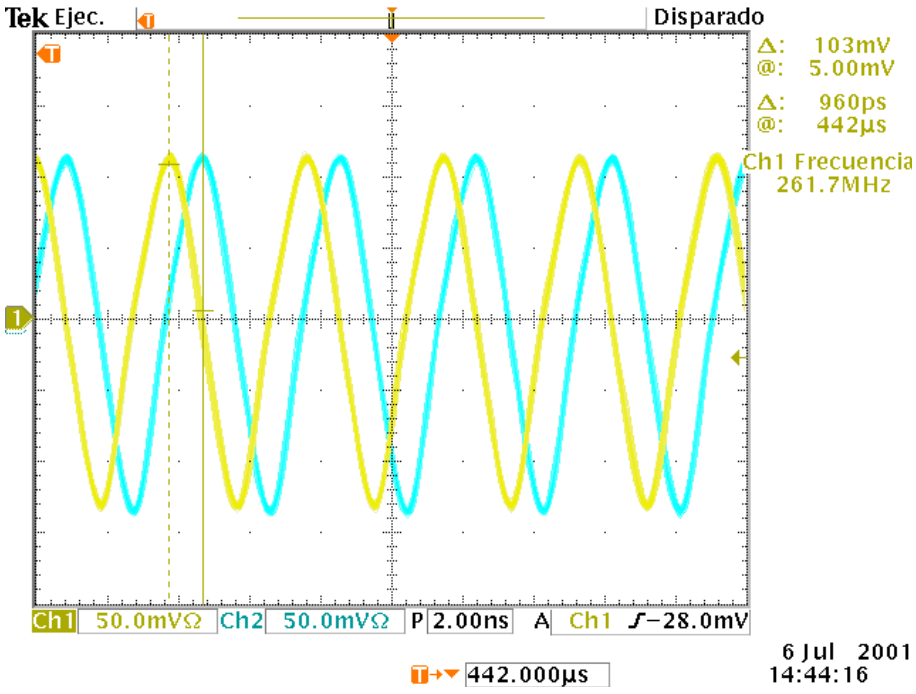


Figure 3-23. Measured output signals of the quadrature generator

Acknowledgements

I would like to thank the RFIC design group at Conexant Systems, Newport Beach, CA for fabricating the circuit and to Madhukar Reddy in special for his help at Conexant. Also I wish to acknowledge the assistance of Dr. Jenshan Lin at Agere Systems in the measurement of the oscillator phase-noise.

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CONCLUSIONS

During last ten years RF integrated circuits have evolved from their infancy to the maturity. Many items have contributed to this evolution (or more probably, revolution): advances in Silicon Technologies, the development of accurate non-linear CAD tools, improved circuit design techniques and architectures, etc. The result of this evolution has been the cellular phone. But, far from the saturation, still there are many potential applications for RF circuits (specially, in short range low power communications), whose proliferation is limited due to cost reasons. Thus, most of the design efforts on RF circuits are currently dedicated to lowering their cost by using CMOS processes. The direct-conversion architectures play also a relevant role in this trend since they favour the integration of the system.

This thesis has addressed issues related to the direct conversion architecture from the circuit design point of view. On the contrary than their digital counterparts, RF circuits are apparently simple (in terms of the number of transistors) and make an intensive use of passive devices and in particular, inductors and transformers. Besides, these passive devices have a noticeable effect on the circuit performance. Therefore, we have set up the analysis of these components (mainly transformers) as the starting point of this thesis with the aim of fully exploit their properties or skip their limitations when they are embedded in a circuit.

Thus, chapter 1 performs a deep analysis of the integrated transformers, revising their electrical properties as well as the several topologies suitable for its integrated

implementation. Besides the ohmic losses associated to thin metals used to build the coils, integrated transformers also suffer from magnetically induced losses (associated to eddy currents). In spite of the geometric or layout similarities with integrated inductors, eddy currents present a much more complex behavior for integrated transformers. In this thesis a special insight has been dedicated to their analysis and it has been pointed out for the first time some important considerations that affect directly to the modeling of the component, as a consequence, to the circuit design. These results can be summarized in the following items:

1) Eddy currents depend on the currents flowing in both the primary and in the secondary and hence can not be estimated independently on the load attached to the secondary. Therefore, a frequency dependent resistor (but independent on the secondary load) as the used in the modeling of the series resistance of integrated inductors can not reproduce the series resistance of the transformer coils for a general case.
2) Eddy currents are minimized when the transformer operates in its differential mode as long as they reach a maximum in the common mode where the transformer is equivalent to an inductor.

This analysis has also showed that the optimization of the transformer is strongly dependent on the application. Thus, when the transformer acts as a power transferer or balun (i.e, it works in its differential mode) the reduction of the component losses can be achieved increasing the strip width (reducing the ohmic losses) since eddy currents are considerably low. Instead, in applications where the transformer acts in its common mode (such as matching or transforming impedance networks, resonators) losses related to eddy currents are significant and should be minimized. This fact has been intensively exploited in chapter 2.

Finally, this chapter finishes with the design of a double balanced mixer that uses two differential transformers to increase the isolation between ports. It is demonstrated that a differential driving minimizes the effects of the parasitic capacitances and increases noticeably the LO-RF isolation, a key parameter when the mixer is intended for direct conversion since minimizes the self-mixing. It is also shown that the etching of the silicon underneath of the integrated transformers that reduces these parasitic

capacitances also increases this isolation (even when a single-ended excitation is applied).

Chapters 2 and 3 take profit of the deep understanding of integrated transformers previously achieved in order to exploit their potential in different circuit applications. Thus, in chapter 2 we have introduced a novel transformer (parallel)-based resonator that exploits the magnetic coupling between different resonators in order to increase its effective quality factor (defined from the phase slope around the resonance). We have also shortly discussed the extension of the transformer-based resonator (N=2) to the general case of N-parallel resonators. Circuit analysis predicted that N coupled inductors will show quality factor N times higher than a single uncoupled inductor.

Then we have performed an exhaustive EM analysis to understand the properties/limitations of the presented resonator and to compare its performance with the standard inductor-based resonator. As a result, eddy currents have been identified as the main cause that prevents or limits the expected improvement in the effective quality factor for the transformer-based resonator. However, this apparent limitation can be partially overcome through an optimized layout of the component.

This optimization algorithm, previously reported in the literature and applied initially to integrated inductors, basically trades losses due to eddy currents (that increase with the strip width) and ohmic losses (that decrease with the strip width) and establishes the optimum strip width (for each inductor turn) that minimizes the overall losses. In this work we have extended this technique to the optimization of integrated transformers. Combining a 3-parallel resonator and an optimized layout, an equivalent inductor of 11 nH with an effective quality factor as high as 25 at 1.7 GHz has been obtained. This value overcomes clearly the quality factor achievable with standard inductor layouts.

The design of oscillators based on N-parallel resonators is also discussed. As summary, the advantages of the N-parallel resonators over their inductor-based counterpart can be synthesized in the following items:

1) N-parallel resonators can achieve higher effective quality factors usually with lower peak impedances. These lower peak impedances allow an increment of the tail current (before reaching the voltage-limited region) leading to an additional

reduction of the phase noise. Of course, this improvement does not increase the oscillator figure of merit since it is achieved at expenses of higher power consumption. However, this method may result interesting if an absolute (or specified) value of phase noise is desired.

2) Since the center tap of secondary/ies is grounded to bias properly the varactors it acts as a short circuit for the common mode harmonics. Thus, no second harmonics can appear across the varactors in the secondary/ies, avoiding the noise down-conversion associated to the varactor non-linearities.
3) Finally, the use of a higher capacitance in the transformer-based resonator results in an extended tunning-range increasing its figure of merit.

To demonstrate this novel topology of resonator, an oscillator prototype at 1.7 GHz was designed, built and tested using the Conexant BC035 CMOS process. The VCO core consumed 4.5 mA of current from a 2.5 V supply, and resulted in a phase noise of -137, –142 and –152 dBc/Hz at 600K, 1 MHz and 3 MHz from the carrier, respectively. Thus, this oscillator features one of the lowest phase-noise achieved in CMOS technologies. The tuning range was 107 MHz for a tuning voltage range of 0-2.5V.

Quadrature oscillators play also a relevant role in the modern communications systems, and mainly in direct conversion architectures that require quadrature oscillators at the RF frequencies. Thus, in chapter 3 we have presented a novel method for designing quadrature oscillators based on the differential coupling at the second harmonic of two separated differential oscillators. As in the previous design, an integrated transformer plays a key role in the circuit, being used to establish the desired coupling between the oscillators. This design is intended to show a better phase noise performance and lower power consumption than the currently existing quadrature oscillators. Also, this method is especially applicable at 2.5-5 GHz and above where the power associated with building a 5-10 GHz differential oscillator followed by a digital divider becomes too high.

Due to the novelty of the presented design, a deep theoretical work has been performed in order to identify the physical mechanism responsible of its properties. In particular, we have revised the theory on injected (or forced) and coupled oscillators. This analysis has pointed out the influence of different design parameters (resonator quality factor,

transformer coupling factor, frequency mismatch between coupled oscillators) in the quadrature accuracy and sets up the basis for a future design optimization.

Finally, to prove the feasibility of this new topology of quadrature oscillator we have designed and tested a prototype of quadrature oscillator at 900 MHz based on double CMOS cross-pair topology. However, the proposed design methodology is also applicable to other any differential topologies, such as the Colpitts oscillator, or the cross-coupled BJT or SiGe oscillator. The circuit was implemented in the BC35 (0.35 μm BiCMOS) Conexant process. It featured a power consumption of 5 mW and an output power of –9 dBm, resulting in phase noise of –116, -133 and –138 dBc/Hz at 100 KHz, 600 KHz and 1 MHz from the carrier respectively.

Moreover, to illustrate the broad range of possibilities and the applicability of the presented method to generate quadrature signals, two additional circuits in a hybrid implementation have been presented. The first circuit consisted in a hybrid implementation of a quadrature oscillator at 150 MHz realized on a PCB board and employed packaged transistors and printed transformers. The main advantage of this approach (compared to the integrated design) is its versatility, since changes in the topology or in the components can be easily done, becoming a useful tool for the analysis and test of the new topology. The second circuit consisted in a quadrature generator also implemented as a hybrid circuit. In this circuit, a second harmonic was injected and signals in quadrature were obtained at the fundamental harmonic as in the previous designs. However, it showed an important difference with the previous designs: in absence of the injected signal at 2f, there is no oscillation since the injected signal is used to compensate the resonator losses. Thus, the only active devices present in the circuit are the varactors used in the resonator.

The work presented in this thesis is a clear example of the potential application of integrated transformers as key components for the design of RFIC's. It has been demonstrated that they allow new circuit topologies, which are worth being considered. Further analysis should be performed to fully exploit the capabilities of these components.