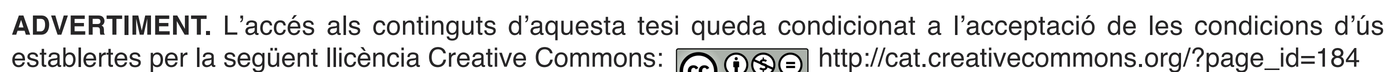
ADVERTIMENT. L'accés als continguts d'aquesta tesi queda condicionat a l'acceptació de les condicions d'ús establertes per la següent llicència Creative Commons:  http://cat.creativecommons.org/?page_id=184

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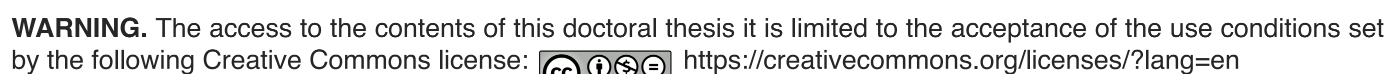
WARNING. The access to the contents of this doctoral thesis it is limited to the acceptance of the use conditions set by the following Creative Commons license:  https://creativecommons.org/licenses/?lang=en

Analysis of the Resistive Switching phenomenon in MOS devices for memory and logic applications

Ph. D. Thesis written by

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Under the supervision of

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Reliability of Electron device and Circuits

Bellaterra (Cerdanyola del Vallès), May 2017

The undersigned, Dra, **Rosana Rodríguez Martínez**, professor of the Electronic Engineering Department (Engineering School) of the *Universitat Autònoma de Barcelona*,

CERTIFY:

That the thesis entitled "*Analysis of the Resistive Switching phenomenon in MOS devices for memory and logic applications*" has been written by the Ph. D. candidate **Marcos Maestro Izquierdo** under her supervision, in fulfillment of the requirements for the PhD degree of Electrical and Telecommunication Engineering.

And hereby to acknowledge the above, sign the present.

Rosana Rodríguez Martínez

Marcos Maestro Izquierdo

Bellaterra (Cerdanyola del vallès), May 2017

"...The show must go on
Inside my heart is breaking
My make-up may be flaking
But my smile still stays on..."

The show must go on, Queen

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Acronyms

Abbreviation	Explanation
CDF	Cumulative Distribution Function
CF	Conductive Filament
CLCU	Current Limit Control Unit
ECM	Electro-Chemical Mechanism
HRS	High Resistance State
IMPLY	Material Implication
Log IVC	Logarithmic current-Voltage Converter
LRS	Low Resistance State
MIM	Metal-Insulator-Metal
MIS	Metal-Insulator-Semiconductor
RRAM	Resistive Random Access Memory
RS	Resistive Switching
RTN	Random Telegraph Noise
SD	Selector Device
SMU	Source Measurement Unit
SPA	Semiconductor Parameter Analyzer
TCM	Thermochemical Mechanism
TLP	Time Lag Plot
TS	Threshold Switching
VCM	Valence Change Mechanisms
VRS	Voltage Ramp Speed
W-TLP	Weighted-Time Lag Plot
NVM	Non Volatile Memory

Preface

In general, the continuous evolution, and improvement, of the technology has led to face new emerging challenges. Regarding the electronic field, one of the most relevant has been the Moore's law which postulates "the number of transistors in a dense integrated circuit doubles approximately every two years". To accomplish this postulate, the solution has been reducing the device dimensions. However, in last decades, physical limitations have been reached since device dimensions are in the atomic range. Moreover, problems originated from the device scaling such as short channel effects in MOSFETs have been observed. Consequently, the focus of the scientific community has turned into the exploration of alternative device materials and structures or different phenomena that would overcome the different issues owing to the scaling.

Concerning alternative phenomena, one of the most relevant has been the **Resistive Switching** (RS) phenomenon which has shown promising features to be implemented in many applications. This phenomenon is based on the capability of a dielectric layer to change its resistance (or conductivity) between two or more values, which show a non-volatile behavior, under the action of an electric field. Overall, these characteristics makes this phenomenon very suitable and promising for its application in digital logic where a new paradigm of computation based on this phenomenon is emerging, in the development of artificial neural networks emulating the behavior of the neuron part known as synapse, and in memory like the next generation of non-volatile memories.

Resistive switching (RS) was firstly reported by T. W. Hickmott (1962) and later by J. G. Simmons and R. R. Verderber (1967) where such a phenomenon was observed in different metal-oxide-metal sandwiches whose dielectric layer was based on silicon, aluminum, titanium, tantalum, or zirconium. Initially, the phenomenon was not defined like resistive switching, authors talked about changes in the resistance of the dielectric layer by observing large current densities inside of that layer. During the 1960s and 1970s, multiples studies about RS were performed due to the great interest the phenomenon caused. Many dielectric materials were observed exhibiting those resistance changes and different physical mechanisms were proposed to explain the origin of that resistance change. However, one of the most important contribution was in the applicability of the phenomenon. Devices exhibiting resistance changes were originally proposed to be implemented like non-volatile memories.

The interest in RS phenomenon decreased significantly in the 1980s and 1990s. The most likely reasons were the slow progress in the physical understanding of the

phenomenon, the difficulty in controlling it for a specific application and the enormous prosperity of silicon-based electronics. However, in the very beginning of 2000s, the interest in RS phenomenon suffered a revival. Zhuang, et al. in 2002 reported a fabricated resistive switching-based device to act like non-volatile memory element and Baek, et al. in 2004 showed the first RS behavior in binary transition metal oxides (TMO). From these years to date, a vast number of works about RS have been published extending the materials showing RS characteristics (binary and ternary oxides, nitrides or even organics materials); proposing new physical mechanisms or completing the existing ones to better describe RS phenomenon in the different dielectric materials (based on ion migration, thermochemical reaction or changes in the dielectric morphology). Additionally, much more works have been released where the applicability of RS-based devices as non-volatile memories, in the implementation of logic gates or in unconventional computing has been verified.

Despite the great efforts of the scientific community in last half a century, there are several hot topics, such as the deeper RS understanding, the analysis of reliability issues affecting RS behavior or the thorough investigation on new applications of RS-based devices in which much more work must be done. In this way, the goal of this thesis is focused on increasing the RS phenomenon knowledge and studying its feasibility for different applications. Hence, RS phenomenon has been study both at device level, to analyze the phenomenon itself, and at circuit level, to analyze its application in memory and digital fields. The results have been presented in relevant publications and conferences related to this subject. All these results are thoroughly explained in this thesis which is structured as follow:

Initially, in the first chapter, resistive switching phenomenon is widely defined, describing the main parameters that characterize it. The different modes in which the phenomenon can operate and the physical mechanisms explaining the origin of the resistance changes are described. Furthermore, the main applications where RS phenomenon can be implemented are numbered as well as the typical devices structures in which the phenomenon is observed. Eventually, a brief description of the principal reliability issues affecting the phenomenon performance is included.

In the second chapter, the RS phenomenon is experimentally studied on MOSFET transistors analyzing the effect on the dielectric resistance change of the voltage polarity applied to provoke RS. Furthermore, due to the localized character of the phenomenon, the different current contributions involved in the conduction through the dielectric and the control of those current contributions are analyzed.

In the third chapter, RS is studied on memristors with a dielectric layer based on HfO_2. Here, the phenomenon is studied applying fast voltage ramps to provoke the resistance changes in order to analyze the influence of the voltage ramp speed on the

RS parameters. In addition, in this chapter, enhanced experimental setups and characterization methods are proposed to analyze the RTN associated to RS.

In the fourth chapter, memristors with a SiO-based dielectric layer are investigated as memory and selector devices. Different DC and pulsed analysis are included to corroborate the feasibility of such devices for these applications.

Finally, the fifth chapter is dedicated to the application of memristors in the digital field. Memristors are used as the main element to design logic gates, specifically, to implement material implication-based (IMPLY) and NAND gates. In this chapter, the experimental working demonstration of both memristor-based logic gates (IMPLY and NAND) is presented. In addition, the transient behaviors of memristors involved in the IMPLY gate are experimentally studied in order to analyze what happens to memristors during IMPLY operation.

PREFACIO

La continua evolución de la tecnología ha llevado a afrontar nuevos retos. Concretamente en el campo de la electrónica, uno de los más relevantes ha sido la Ley de Moore que postula que "el número de transistores in un circuito integrado se duplicará aproximadamente cada dos años". Por ello, para cumplir con dicho ley, la solución ha sido reducir las dimensiones de los dispositivos. Sin embargo, en las últimas décadas, la reducción de estas dimensiones ha alcanzado limitaciones físicas ya que actualmente se está llegando al rango atómico. Además, se han observado diversos problemas, como por ejemplo efectos de canal corto en MOSFETs, originados por el escalado de los dispositivos. Como consecuencia, la comunidad científica se ha focalizado en la exploración de nuevos materiales, en el desarrollo de estructuras alternativas o en el estudio de diferentes fenómenos para solucionar los problemas derivados del escalado.

Con respecto a fenómenos físicos alternativos, uno de los más relevantes ha sido el fenómeno de ***Resistive Switching*** (RS) el cuál ha mostrado prometedoras características para ser implementado en diversas aplicaciones. Este fenómeno se basa en la capacidad de una capa de dieléctrico para cambiar su resistencia (o conductividad) entre dos o más valores que muestran un comportamiento no volátil bajo la acción de un campo eléctrico. En general, estas características permiten que este fenómeno sea muy apropiado y prometedor para su aplicación en lógica digital, donde un nuevo paradigma de computación basado en este fenómeno está surgiendo, en el desarrollo de redes neuronales artificiales, emulando el comportamiento de una parte de la neurona conocida como sinapsis, y en memorias como la siguiente generación de memorias no volátiles.

Resistive switching fue citado por primera vez por T. W. Hickmott (1962) y más tarde por J. G. Simmons and R. R. Verderber (1967) donde dicho fenómeno fue observado en diferentes estructuras metal-óxido-metal cuya capa dieléctrica estaba basada en silicio, aluminio, titanio, tantalo o zirconio. Inicialmente, el fenómeno no fue definido como RS, los autores hablaban simplemente de cambios en la resistencia de la capa de dieléctrico observando grandes densidades de corriente a través de dicha capa. Durante los años 60 y los 70, se llevaron a cabo multiples estudios sobre RS debido al gran interés que suscitó el fenómeno. Se observaron muchos materiales dieléctricos mostrando los sucesivos cambios de resistencia y se proposieron diferentes mecanismos físicos que pretendían explicar el origen de esos cambios resistivos. Sin embargo, una de las contribuciones más importantes fue en la aplicabilidad del

fenómeno. Dispositivos exhibiendo cambios resistivos fueron originalmente propuestos para ser implementados como memorias no volátiles.

El interés sobre el fenómeno RS disminuyó significativamente en las decadas de los 80 y 90. La razón más probable fue el lento progreso en el entendimiento físico del fenómeno, en la dificultad de controlarlo para aplicaciones más especificas y a la enorme prosperidad de la electrónica basada en silicio. Sin embargo, al comienzo de los 2000, el interés sobre el fenómeno RS sufrio un nuevo auge, principalmente debido a que. Zhuang, et al. en 2002 reportaron un dispositivo experimental basado en resistive switching que podía actuar como un elemento de memoria no volátil y Baek, et al. en 2004 mostraron el primer comportamiento de RS en óxidos metálicos binarios de transición (TMO). Desde aquellos años hasta la fecha, se han publicado un vasto número de trabajos sobre RS donde se ha aumentado el número de materiales que experimentan características RS (óxidos binarios y ternarios, nitruroso incluso material orgánicos); se han propuesto nuevos mecanismos físicos o se han completado los ya existentes para describir mejor el fenómeno RS en los diferentes materiales dieléctricos (basados en migración de iones, reacciones termoquímicas o en cambios en la morfología del dieléctrico). Adicionalmente, se han publicado numerosos trabajos donde se ha demonstrado la aplicabilidad de dispositivos basados en RS como memorias no volatiles, in la implemtación de puestas lógicas o en computación no convencional.

A pesar de los grandes esfuerzos por parte de la comunidad científica en la última mitad de siglo, hay varios temas candentes en los que aún queda mucho trabajo por hacer. Algunos de estos temas son entender más profundamente el fenómeno RS, analizar los problemas de fiabilidad que afectan al comportamiento RS o la investigación minuciosa de nuevas aplicaciones de dispositivos basados en RS. Por tanto, el fenómeno RS ha sido estudiado tanto a nivel de dispositivo, para analizar el fenómeno en sí mismo, como a nivel de circuito, para analizar sus aplicaciones en memorias y en lógica digital. Los resultados han sido presentados en publicaciones y conferencias relevantes en el tema donde la tesis está enmarcada. Todos estos resultados son detalladamente explicados en esta tesis que se ha estructurado como sigue:

Inicialmente, en el primer capítulo se explica ampliamente el fenómeno de RS, describiendo los principales parámetros que lo caracterizan. Se definen los diferentes modos en los que el fenómeno puede operar así como los mecanismos físicos que explican el origen de los cambios resistivos. También, se listan las principales aplicaciones donde el fenómeno RS puede ser implementado además de las estructuras típicas en las cuales el fenómeno es observado. Finalmente, se incluye una breve descripción de los problemas de fiabilidad más relevantes que afectan al rendimiento del fenómeno.

En el segundo capítulo, el fenómeno RS se estudia experimentalmente en transistores MOSFETs analizando el efecto de la polaridad del voltaje aplicado para provocar RS sobre el cambio resistivo del dieléctrico. Además, debido al carácter localizado del fenómeno, se analizan las diferentes contribuciones de corriente involucradas en la conducción a través del dieléctrico y el control de dichas contribuciones.

En el tercer capítulo, RS se estudia en memristores con una capa de dieléctrico basada en HfO_2. Aquí, el fenómeno se estudia aplicando rampas de voltajes más rápidas para provocar los cambios resistivos con el fin de analizar la influencia de la velocidad de la rampa sobre los parámetros RS. También, en este capítulo, se proponen montajes experimentales y métodos de caracterización mejorados para analizar el *random telegraph noise* (RTN) asociado al RS.

En el cuarto capítulo, se investigan memristores con una capa de dieléctrico basada en SiO para su aplicación como dispositivos de memoria y selección. Se han incluido diferentes análisis tanto en DC como AC para corroborar la viabilidad de dichos dispositivos en esas aplicaciones.

Finalmente, el quinto capítulo está dedicado a la aplicación de memristores en el campo de la lógica digital. Se han usado memristores como el elemento principal para diseñar puertas lógicas, específicamente para implementar puertas IMPLY y NAND. En este capítulo, se presenta la demostración experimental del funcionamiento de dichas puertas basadas en memristores así como el estudio experimental de la evolución temporal de los memristores involucrados en la puerta IMPLY con el fin de analizar que ocurre durante la operación lógica.

PREFACI

La contínua evolució de la tecnologia ha portat a afrontar nous reptes. Concretament en el camp de l'electrònica, un dels més rellevants ha estat la Llei de Moore que postula que "el nombre de transistors en un circuit integrat es duplicarà aproximadament cada dos anys". Per això, per complir aquest raonament, la solució ha estat reduir les dimensions dels dispositius. No obstant això, en les últimes dècades, la reducció d'aquestes dimensions ha arribat a limitacions físiques ja que actualment s'està arribant al rang atòmic. A més, s'han observat diversos problemes, com ara efectes de canal curt en MOSFETs, originats per l'escalat dels dispositius. Com a conseqüència, la comunitat científica s'ha focalitzat en l'exploració de materials i estructures de dispositius alternatives o en diferents fenòmens que ajudarien a solucionar els problemes derivats de l'escalat.

Pel que fa a fenòmens físics alternatius, un dels més rellevants ha estat el fenomen de Resistive Switching (RS) el quin ha mostrat prometedores característiques per ser implementat en diverses aplicacions. Aquest fenomen es basa en la capacitat d'una capa de dielèctric per canviar la seva resistència (o conductivitat) entre dos o més valors que mostren un comportament no volàtil sota l'acció d'un camp elèctric. En general, aquestes característiques permeten que aquest fenomen sigui molt apropiat i prometedor per a la seva aplicació en lògica digital, on un nou paradigma de computació basat en aquest fenomen està sorgint, en el desenvolupament de xarxes neuronals artificials, emulant el comportament d'una part de la neurona coneguda com sinapsis, i en memòries com la següent generació de memòries no volàtils.

Resistive switching va ser citat per primera vegada per T. W. Hickmott (1962) i més tard per J. G. Simmons and R. R. Verderber (1967) on aquest fenomen va ser observat en diferents estructures metall-òxid-metall la capa dielèctrica estava basat en silici, alumini, titani, tantalo o zirconi. Inicialment, el fenomen no va ser definit com RS, els autors parlaven simplement de canvis en la resistència de la capa de dielèctric observant grans densitats de corrent a través d'aquesta capa. Durant els anys 60 i els 70, es van dur múltiples estudis sobre RS a causa del gran interès que va suscitar el fenomen. Molts materials dielèctrics van ser observats mostrant aquells canvis de la seva resistència i diferents mecanismes físics van ser proposats per explicar l'origen d'aquest fenomen. No obstant això, una de les contribucions més importants va ser l'aplicabilitat del fenomen. Dispositius exhibint canvis resistius van ser originalment proposats per a ser implementats com memòries no volàtils.

L'interès sobre el fenomen RS va disminuir significativament en les dècades dels 80 i 90. La raó més probable va ser el lent progrés en l'enteniment físic del fenomen, en la dificultat de controlar-lo per a aplicacions més específiques i l'enorme prosperitat de l'electrònica basada en silici. No obstant això, a començaments dels anys 2000, l'interès sobre el fenomen RS va patir un ressorgiment. Zhuang, et al. al 2002 van reportar un dispositiu experimental basat en Resistive switching que podia actuar com un element de memòria no volàtil i Baek, et al. al 2004 van mostrar el primer comportament de RS en òxids metàl · lics binaris de transició (TMO). Des d'aquests anys fins a la data, s'han publicat un vast nombre de treballs sobre RS on s'ha augmentat el nombre de materials que experimenten característiques RS (òxids binaris i ternaris, nitrurs fins i tot materials orgànics); s'han proposat nous mecanismes físics o s'han completat els ja existents per descriure millor el fenomen RS en els diferents materials dielèctrics (basats en migració d'ions, reaccions termoquímiques o en canvis en la morfologia del dielèctric). Addicionalment, s'han publicat molts més treballs on s'ha demostrat l'aplicabilitat de dispositius basats en RS com memòries no volàtils, en la implantació de postes lògiques o en computació no convencional han estat publicats.

Malgrat els grans esforços per part de la comunitat científica en l'última meitat de segle, hi ha diversos temes candents en què encara queda molta feina per fer. Alguns d'aquests temes són entendre més profundament el fenomen RS, analitzar els problemes de fiabilitat que afecten al comportament RS o la investigació minuciosa de noves aplicacions de dispositius basats en RS. Per tant, el fenomen RS ha estat estudiat tant a nivell de dispositiu, per analitzar el fenomen en si mateix, com a nivell de circuit, per analitzar les seves aplicacions en memòries i en lògica digital. Els resultats han estat presentats en publicacions i conferències rellevants en el tema on la tesi està emmarcada. Tots aquests resultats són detalladament explicats en aquesta tesi que s'ha estructurat com segueix:

Inicialment, en el primer capítol, el fenomen de RS és àmpliament definit, descrivint els principals paràmetres que el caracteritzen. Els diferents maneres en què el fenomen pot operar així com els mecanismes físics que expliquen l'origen dels canvis resistius són descrits. També, es llisten les principals aplicacions on el fenomen RS pot ser implementat a més de les estructures típiques en les quals el fenomen és observat. Finalment, s'inclou una breu descripció dels problemes de fiabilitat més rellevants que afecten el rendiment del fenomen.

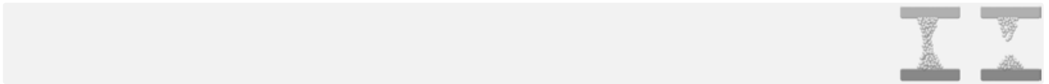
En el segon capítol, el fenomen RS s'estudia experimentalment en transistors MOSFETs analitzant l'efecte de la polaritat del voltatge aplicat per provocar RS sobre el canvi resistiu del dielèctric. A més, a causa del caràcter localitzat del fenomen, s'analitzen les diferents contribucions de corrent involucrades en la conducció a través del dielèctric i el control d'aquestes contribucions.

En el tercer capítol, RS s'estudia en memristors amb una capa de dielèctric basada en HfO2. Aquí, el fenomen s'estudia aplicant rampes de voltatges més ràpides per provocar els canvis resistius per tal d'analitzar la influència de la velocitat de la rampa sobre els paràmetres RS. També, en aquest capítol, es proposen muntatges experimentals i mètodes de caracterització millorats per analitzar el *random telegraph noise* (RTN) associat a l'RS

En el quart capítol, s'investiguen memristors amb una capa de dielèctric basada en SiO per a la seva aplicació com a dispositius de memòria i selecció. Diferents anàlisis tant en DC com AC s'han inclòs per corroborar la viabilitat d'aquesta dispositius en aquestes aplicacions.

Finalment, el cinquè capítol està dedicat a l'aplicació de memristors en el camp digital. Els memristors són usats com l'element principal per dissenyar portes lògiques, específicament per implementar portes IMPLY i NAND. En aquest capítol, es presenta la demostració experimental del funcionament d'aquestes portes basades en memristors. A més, s'ha estudiat experimentalment l'evolució temporal dels memristors involucrats en la porta IMPLY per tal d'analitzar com es comporten aquests memristors durant l'operació lògica.

1. INTRODUCTION



Many alternatives have been proposed along the years in order to improve technology and make it more competitive particularly in the electronic field. As indicated in the preface, the scaling of device dimensions, was one of those alternatives which successfully allowed accomplishing Moore`s law. However, as the scaling increased, different issues related to physical limitations or the wrong-operations of devices have been appearing. In order to solve them, different device materials and structures and other physical phenomena have been studied. In this latter regard, a new phenomenon, known as *Resistive Switching* (RS), has emerged as an alternative physical mechanism to be implemented in many different applications like logic, memory, artificial neural networks and computing.

Due to *Resistive Switching* is the focus of this thesis, an overview of the phenomenon is presented in this introductory chapter. First, the description of the phenomenon is detailed, explaining the basis of RS operation, the different modes in which the phenomenon can operate regarding the polarity of the applied electric field and the main physical mechanisms that explain the behavior of RS. Second, the foremost reliability issues related to the phenomenon are also introduced indicating how they affect to RS functionality, the different studies performed about them and, if possible, the proposed solutions to overcome them. Third, relevant applications where RS has been implemented are presented explaining their performance and including some examples that demonstrate the functionality of RS phenomenon in the application. Eventually, a description of the equipment used along the thesis as well as measurement and data analysis procedures is included at the end of the chapter.

1.1. Resistive switching phenomenon

In this section, resistive switching phenomenon will be described. Initially, a detailed phenomenon definition, indicating its characteristic processes and parameters, will be presented as well as the devices where such a phenomenon has been observed. Then, the different operation modes in addition with the most relevant physical mechanisms that describe the phenomenon will be explained.

1.1.1. What is Resistive Switching?

Resistive switching consists in successive resistance changes of a thin dielectric layer by applying an external electric field. Figure 1-1 shows two typical experimental current-voltage (IV) curves of the phenomenon. One IV-curve corresponds to the first resistive change for positive applied voltages whereas the subsequent resistive change is depicted for negative voltages, although other combinations of voltage polarities can take place. The resistance changes of the dielectric layer commonly occur between two well-differentiated states, which are usually separated by several orders of magnitude, although dielectrics with more than two resistance values are also possible allowing multistate RS. Those two dielectric resistance states are extensively recognized as high resistance state, HRS, and low resistance state, LRS, which show a non-volatile behavior, i.e. they are remained for a retention time after the electric field has been removed. Due to the relation between resistance and current (Ohm's law), at LRS state the current flowing through the dielectric is quite large; however, at HRS the flow of the current is almost suppressed (in Figure 1-1

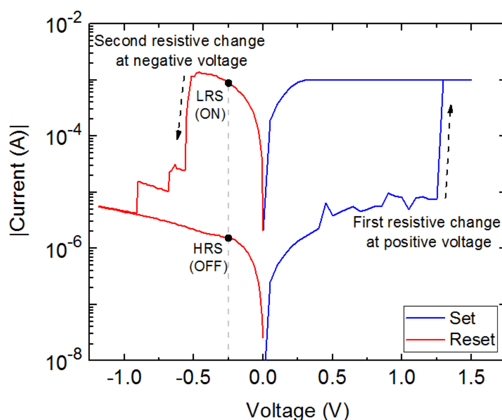
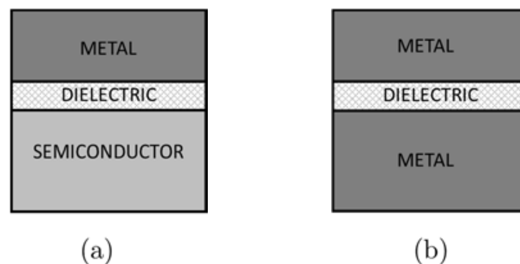


Figure 1-1: Typical experimental IV-curves of a memristive device showing resistive switching phenomenon.

indicated LRS and HRS show a current difference of approximately three decades). LRS and HRS resistance states can be also identified as ON (current flowing) and OFF (not current flowing) states, respectively. Moreover, following digital nomenclature, they can be considered as the “1” and “0” Boolean values for memory and digital applications.

Those devices where RS phenomenon takes place are frequently known as *memristive devices*. The most used and important memristive device is the *memristor* (contraction of memory and resistor). Firstly predicted by Leon Chua in 1971 as one of the four fundamental two-terminal circuit elements [1], and later experimentally demonstrated by D. Strukov and et al. in 2008 [2], memristors have become in a reality during the last decades. Structurally, a memristor consists in a three-layer structure formed by a top electrode, a bottom electrode and a dielectric layer sandwiched in between those electrodes. Two different memristor structures are mainly found: metal-insulator-metal (MIM) and metal-insulator-semiconductor (MIS) which are schematically presented in Figure 1-2(a) and (b), respectively. The dielectric layer corresponds to that layer whose resistance can be successively changed and, therefore, where the RS phenomenon takes places. However, the observation of such a phenomenon strongly depends on the electrodes and dielectric materials, not all the materials can experience RS phenomenon. Both, MIS and MIS-structured memristors have been used along this thesis to study different applications of the RS phenomenon.

From memristive point of view, a MOSFET transistor can be considered as a memristor because it is based on a MIS structure where two additional regions (drain and source) have been added, as shown in Figure 1-3. Essentially, MOSFET can act as a memristive device when a voltage difference is applied between gate and substrate electrodes, while drain and source terminals are grounded. Consequently, a resistance state change takes place in the dielectric (or oxide) layer. Such description of MOSFET operation could suggest that drain and source regions are



gure 1-2: Schematic of (a) a metal-insulator-semiconductor (MIS) and (b) a metal-insulator-metal (MI structures.

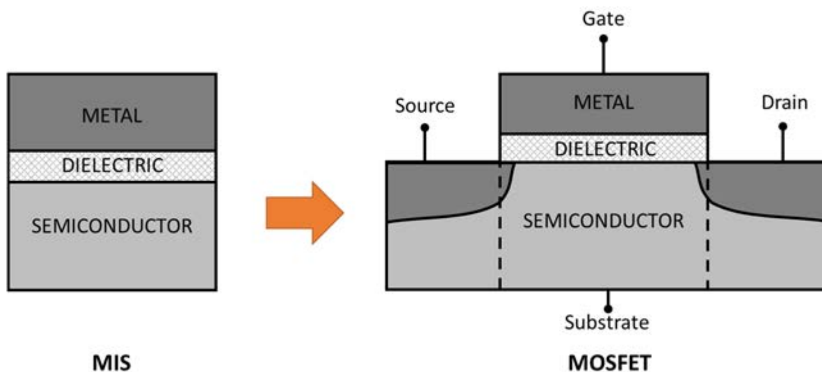


Figure 1-3: Schematic of a MOSFET where all the electrodes are indicated: gate, substrate, drain and source. RS phenomenon takes place in the dielectric layer located between the gate and substrate electrodes. Hence, a MOSFET can be considered as a memristive device.

useless since they are grounded all the time. Contrarily, these two terminals have allowed characterizing more deeply the resistance change behavior and postulating and demonstrating the existence of a kind of MOSFETs where resistive switching phenomenon and typical transistor operations can alternatively occur in the same device. This multifunction transistor has been called memFET (memory field effect transistor), [3]–[6], due to its functionality like memory, by provoking RS phenomenon, and like a typical transistor by modulating the current flowing between source and drain through the electric field applied between gate and substrate. More studies in the literature have also devoted to the analysis of the resistive switching in transistors [7].

Successive dielectric resistance changes in memristors are accomplished by performing different electrical processes that are mainly known like forming, set and reset. In Figure 1-4, very schematic representations of the three processes involved in RS operation as well as its characteristic parameters are depicted.

Forming process is usually the very first process occurring in a device where RS phenomenon is observed. Although it is not necessary in all the devices, in most of dielectric materials in which RS is observed, this process is required to observe subsequently the RS behavior. The forming process provokes the change of the dielectric resistance value from a pristine state to a LRS (top in Figure 1-4) by applying an external voltage. The exact voltage value at which this resistance change takes place is usually known as forming voltage, $V_{FORMING}$. An important condition to take into account during the forming process, although not mandatory depending on the dielectric material, is the use of a limit in the current flowing through the dielectric to avoid a complete dielectric breakdown which is an irreversible phenomenon. This parameter is commonly named compliance or current limit (I_C).

After forming, the device can be switched from LRS to HRS and vice versa successively by applying external voltages again. The first resistance change (from LRS to HRS) where dielectric resistance value increases is identified as *reset* process and the voltage at which the change occurs is defined as reset voltage, V_{RESET} (center in Figure 1-4). On the other hand, the process to perform the decrease of the dielectric resistance (from HRS to LRS) is called *set* process whose characteristic voltage, i.e. the voltage at which resistance change occurs, is labeled as set voltage, V_{SET} (bottom in Figure 1-4). Like in the forming process, during set process it is usually necessary to establish a current limit to avert an irreversible damage in the dielectric and to observe successive dielectric resistance changes.

Regarding the polarity of the applied voltage to provoke the different processes, RS phenomenon can be classified into different operation-mode categories depending on the polarity combination of voltages applied to perform set and reset processes.

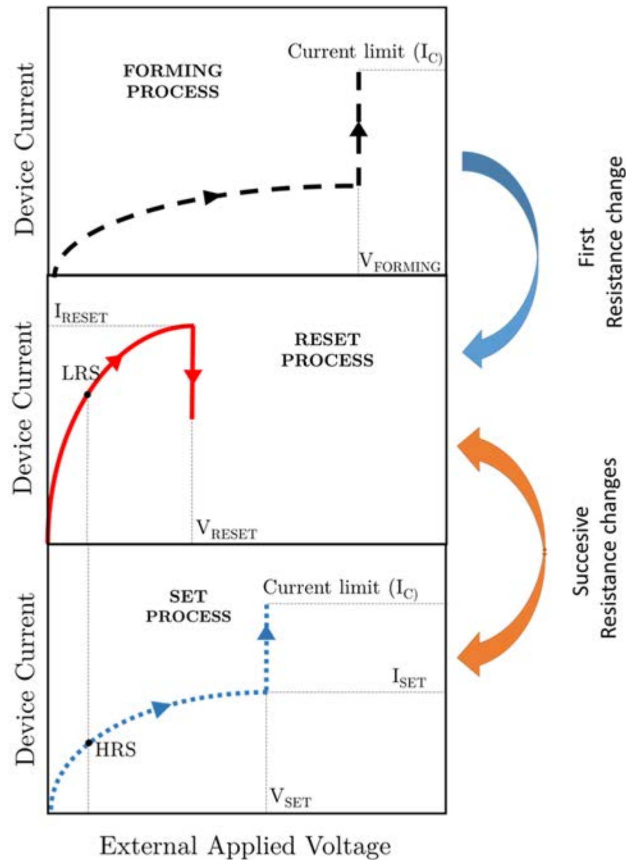


Figure 1-4: Schematic of forming (top), reset (center) and set (bottom) processes. Characteristic voltages ($V_{FORMING}$, V_{RESET} and V_{SET}), resistance states (LRS and HRS) and characteristic currents (I_{SET} and I_{RESET}) are also indicated in each process.

1.1.2. Operation modes

The main operation modes of the phenomenon are: *bipolar* and *unipolar resistive switching*. There is a third operation mode, not related to voltage polarity actually, known as *threshold switching*. This last operation mode differs from the previous ones in the volatile behavior or the LRS, because when the applied voltage is removed memristive device comes back to HRS.

1.1.2.1. Bipolar resistive switching

Bipolar RS takes place when the voltages applied to perform set and reset processes have opposite polarities. This is the most common voltage polarity combination used to observe the RS phenomenon. Schematic I-V curves for both possible bipolar switching modes are sketched in Figure 1-5(a) and (b), where the absolute value of the current is plotted in a logarithmic scale. In both figures, dotted blue curve corresponds to the change from HRS to LRS, i.e. the set process (the current limit, I_C, usually needed to avoid the whole dielectric breakdown is also indicated) whereas solid red curve shows the transition from LRS to HRS, i.e. when reset process takes place. First bipolar switching mode (Figure 1-5(a)) is called, in some works, as “figure-of-eight” bipolar switching due to 8-shape of the curves when they are plotted in linear scales. In this case, set process takes place when positive voltages are applied while reset process occurs for negative voltages. On the contrary, owing to the inversion of polarities, the second bipolar switching mode, where set and reset processes are provoked when negative and positive voltages are applied respectively (Figure 1-5(b)), is called “counter-figure-of-eight” bipolar switching.

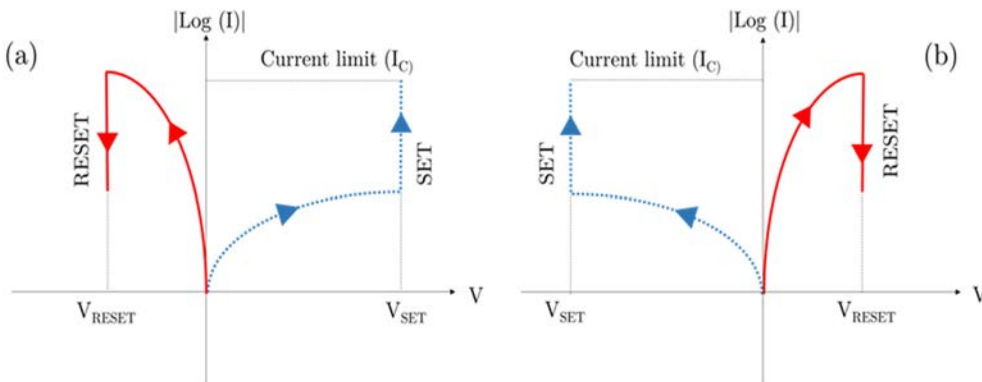


Figure 1-5: Sketch of typical I-V characteristics for (a) bipolar RS, where applied voltages to set and reset the device are positive and negative respectively, and (b) bipolar RS where set and reset processes are provoked applying negative and positive voltages, respectively.

Many materials have been reported in the literature showing bipolar RS such as TiO_2, TaO_X, HfO_X, Al_2O_3, Cr_2O_3, SiN, $BaTiO_3$ or graphene oxide amongst many others [8], [9]. Majority of the materials show only one kind of the bipolar voltage polarity combination (the one presented in Figure 1-5(a) or (b)). However, in some dielectric materials as for example WO_X [10], [11] both bipolar RS modes have been observed.

1.1.2.2. Unipolar resistive switching

Contrarily to the previous switching mode, unipolar resistive switching occurs when the voltage polarities applied to provoke set and reset processes are the same. Because of the two different voltage polarities, unipolar switching can be sub-classified into two types: negative and positive. In Figure 1-6, both negative (left hand side) and positive (right hand side) unipolar resistive switching are schematically shown (y-axis corresponds to absolute value of the current in logarithmic scale). Here, dashed line corresponds to the resistance transition from HRS to LRS, the set process. On the contrary, solid line represents the LRS-HRS transition, where reset process occurs. Current limit (I_C), although not always necessary, is also included during set process.

Many works have demonstrated the existence of many different dielectric materials showing negative, TiO_2 [12], positive, SiO_X [13], Nb_2O_5 [14] or even both unipolar RS modes HfO_2 [15], NiO [16], [17]. On the other hand, not only unipolar or bipolar operation modes can be observed in the same material, some other works have shown

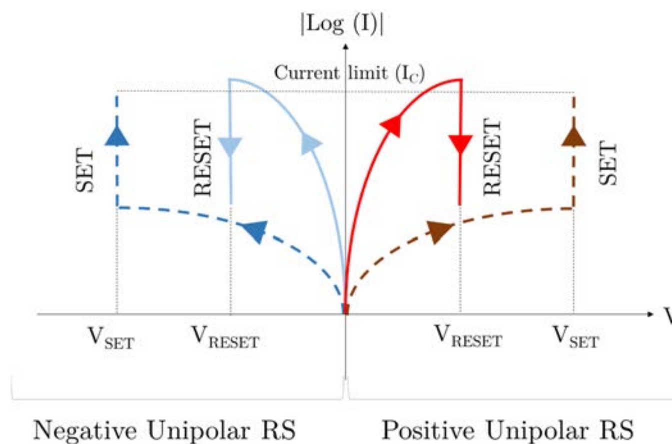


Figure 1-6: Sketch of typical I-V characteristics for both unipolar RS modes, (left) negative unipolar RS and (right) positive unipolar RS. In each mode, the applied voltages to provoke set and reset processes have the same polarity.

the coexistence of both resistive switching modes (bipolar and unipolar) occurring in the same device with a dielectric layer based on TiO_2 [18], NiO [19] or HfO_2 [20].

1.1.2.3. Threshold switching

Although it is also based on RS phenomenon, threshold switching (TS) is not strictly a resistive switching mode as far as voltage polarity and state volatility is concerned. However, as some results of this thesis are related to this type of switching, a brief introduction about TS is included.

Figure 1-7 shows a sketch of I-V curves for positive (solid red line) and negative (dotted blue line) threshold switching behavior. Initially, by applying a voltage ramp, TS consists in a set-like switching process which occurs at a certain voltage called threshold voltage, V_T. During the process, a current limit is also necessary to avoid a complete dielectric breakdown and reach the low resistance state as in the case of the set process. Contrarily to RS, the reached resistance state shows a volatile behavior; therefore, when voltage is removed back to zero an inverse switching takes place at a voltage named holding voltage, V_H. Then, a device showing TS only has one stable resistance state which is related with a HRS state in RS and whose current, measured to identify such a state, is labeled I_{OFF} as it is shown in Figure 1-7. The other resistance state reached after threshold switching, related to LRS state, is only stable in a short voltage range (between V_T and V_H). Due to the volatile behavior, threshold switching lacked of interest in memory or digital applications where two stable states are required. However, TS mode has been very attractive to develop select devices in crossbar memories [21], [22] as will be shown in section 1.3.

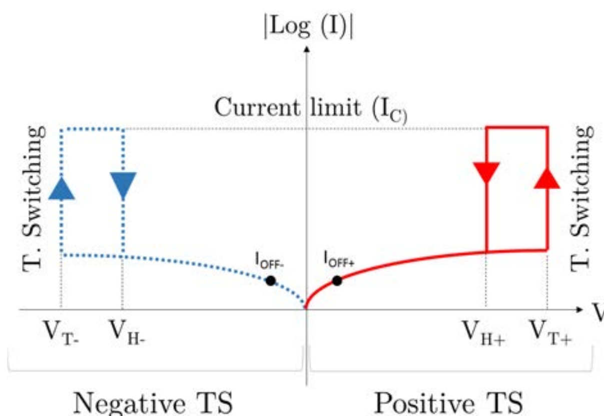


Figure 1-7: Sketch of typical I-V curves of positive (solid red lines) and negative (dotted blue lines) threshold switching behavior when positive and negative voltages are respectively applied. A current limit (I_C), needed in TS, is also indicated.

Once the different RS operation modes have been introduced, another important matter related to the RS phenomenon is the explanation of how set and reset processes physically occur. Different physical mechanisms explaining the nature of the resistance change behavior in a dielectric material have been proposed in the literature. In the following subsection, those physical mechanisms related to the RS phenomenon observed in this thesis are briefly presented.

1.1.3. Physical RS mechanisms

Numerous research groups have focused their efforts on finding the physical mechanisms that governs the set and reset processes to explain the RS behavior. [23]–[32]. Furthermore, those physical mechanisms specifically allow explaining the different operation modes of RS. Figure 1-8 shows a classification of different mechanisms according to how the resistance change physically occurs [24]. From all of them, only the three mechanisms occurring in the devices used along this thesis will be described. These three mechanisms (valence change, electromechanical metallization and thermochemical reaction) are very similar since the resistance changes of the dielectric are owing to the creation/dissolution of a conductive filament (CF) along the dielectric that connects top and bottom electrodes. The difference between these three mechanisms is in the physical process performed to create and disrupt the conductive filament. These processes depend on the materials of dielectric layer and the electrodes as well as the polarity of applied voltages to provoke the RS.

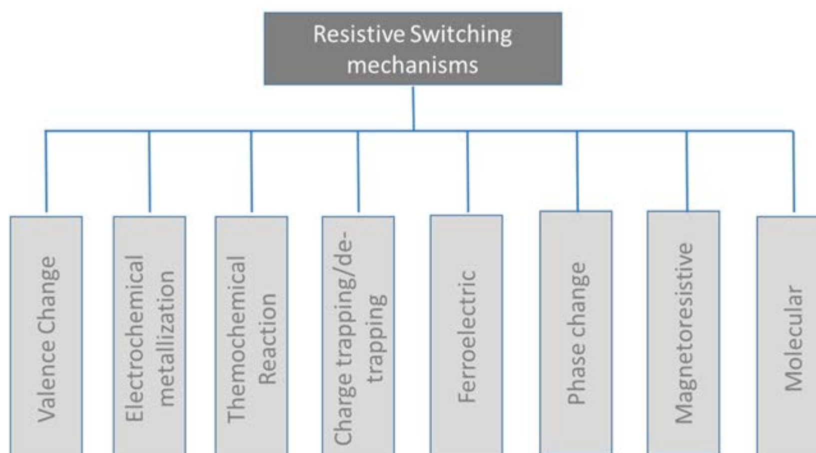


Figure 1-8: Classification of different physical mechanisms explaining the dielectric resistance change depending on how the resistance change physically occurs [24].

1.1.3.1. Valence change

Valence change mechanism (VCM) typically occurs in metal oxides such as HfO_X [33], NiO_X [34], TaO_X[35], or TiO_X [25], where a migration of ions takes place, specifically, a migration of anions. Actually, the mechanism is described by the "migration" of the positively charged counterparts, known as oxygen vacancies (V_Os), of those anions. The accumulation/depletion of V_Os causes changes in the resistance of the oxide. The accumulation of vacancies can be associated to the creation of a conductive filament formed of such vacancies. On the other hand, the depletion can be related to the dissolution or disruption of the conductive filament. In Figure 1-9, a schematic of valence change process is depicted. Initially, (a) the device in a pristine state has a uniform distribution of oxygen vacancies. Then, when a positive voltage bias is applied to the top electrode (TE), with the bottom electrode (BE) grounded, an accumulation of oxygen vacancies is induced at the interface between BE and oxide layer (b). If enough positive voltage is applied, the forming process is finally provoked creating a V_Os-based conductive filament connecting TE and BE (c) and reaching the LRS. After the forming, the device has reached the LRS state. Owing to the nature of the mechanism, V_Os-based filaments are typically considered conical shaped whose thinnest part is located at the interface between TE and oxide.

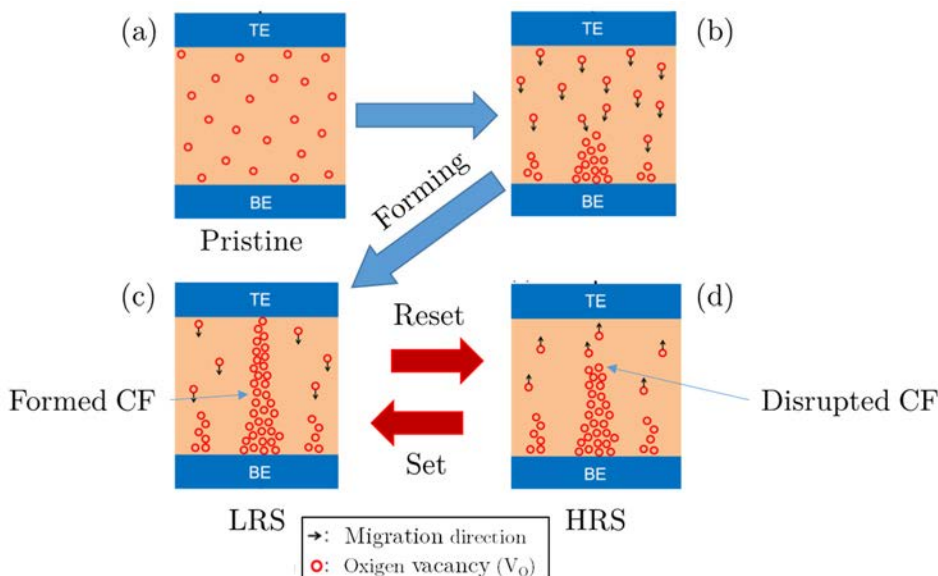


Figure 1-9: Schematic of VCM mechanism. (a) Initial state with a uniform distribution of oxygen vacancies. (b) Accumulation of oxygen vacancies starting at the interface between BE and the oxide layer. (c) Device at LRS when set (or forming) process has been performed by applying positive voltage bias. (d) HRS state of the device reached after a negative voltage bias was applied provoking reset process. Readapted from [8].

Once conductive filament is created, the device can be switched to HRS by means of the reset process. To do so, a negative voltage bias is applied provoking the totally or partially disruption of the filament (d) what is caused mainly by the V_Os-migration-induced redox reaction. Applying a positive voltage bias again, the device can be switched to LRS state performing the set process and a re-creation of the filament is done (c). Applying successively positive and negative voltage biases, subsequent set and reset processes are performed originating the re-creation and disruption of the V_Os-based conductive filament.

Regarding operation modes, VCM is closely related to bipolar RS. However, it is not clear which polarity of bipolar mode predominates. In general, the polarity of the voltages at which bipolar RS is observed depends on many factors related to the material used for the electrodes, such as the work function or the formation of interface layers [24].

1.1.3.2. Electrochemical metallization

As the valence change mechanism, electrochemical metallization (ECM) is based on ion migration. In this case, metal cations migrate back and forth between an electrochemically active metal (AM) and an electrochemically inert counter electrode (CE) creating and dissolving the metallic conductive filament along a dielectric layer located between both electrodes. Figure 1-10 shows an I-V characteristic of a structure with Ag as active metal, Pt as inert metal and Ge-Se as the dielectric [36]. Some sketches ((a)-(d)) of the structure at important curve points are included.

Initially, when no voltage bias is applied the device is at a pristine (or HRS) state (sketch (a)) and no metal ions migrate from the AM electrode into the dielectric layer. Later, by applying a positive voltage bias to Ag-electrode, metal ions are electrochemically dissolved (sketch (b)) to migrate subsequently through the dielectric being, then, deposited on the surface of CE (sketch (c)) due to reduction and electro-crystallization processes. When a sufficient positive voltage is applied and an adequate number of metal ions have been migrated and deposited, the metal-ion-based conductive filament is created (sketch (d)), forming process has been accomplished at the first step and the device has been switched to LRS state. Now, a negative voltage bias is applied to the device to switch it to HRS state and, therefore, performing the reset process. The resistance change occurs due to an electrochemical dissolution of the metal CF (sketch (e)) helped by Joule heating at the thinnest parts of the filament. When CF has been dissolved completely, the device comes back to LRS state by applying positive voltages again what performs the set process. Applying successively positive and negative voltages, the device can be switched to HRS and LRS, and vice versa, thanks to the creation and dissolution of a metallic filament.

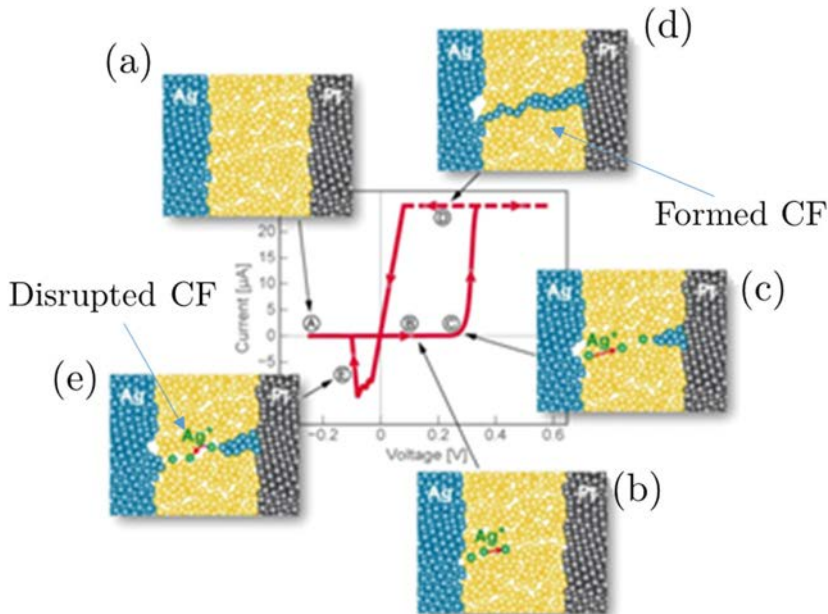


Figure 1-10: Typical I-V characteristic of a Ag/Ge-Se/Pt structure and a complete RS process. (a) Device in pristine state, (b)-(d) creation of the metallic CF by forming process (or set process for subseqent cycles) and (e) dissolution of the CF by reset process [36].

Many works have demonstrated the existence of a metallic CF created and dissolved by ECM mechanism in different materials such as TiO_2, SiO_2 or ZrO_2 [9]. Likewise, metals like Ag, Cu, Ni or Au have been used as AM [8]. In all of them, repeating the process of applying subsequently positive and negative voltage bias, the device can be switched successively from HRS to LRS (set) and from LRS to HRS (reset) performing a RS cycling. This polarity combination to perform set/reset cycles suggest that the predominant operation mode is the figure-of-eight bipolar mode shown in Figure 1-5(a). A positive voltage is needed to be applied to AM while CE is grounded to provoke the electromigration of the metal cations during set. On the contrary, a negative voltage applied to AM is necessary to provoke the dissolution of the cations during reset process. Therefore, bipolar resistive switching can be explained by VCM and ECM mechanisms. Depending on the dielectric materials and electrodes material either vacancy-based or metallic-based mechanism can illustrate set and reset processes under bipolar RS.

1.1.3.3. Thermochemical reaction

From the works presented by Wun-Cheng Luo et al. in [37] and Xing Wu et al. in [38], thermochemical mechanism (TCM) might be considered as a combination of ECM and VCM. Depending on the polarity of the applied voltage during forming

process the filament can be based on metal ions (ECM) or V_Os (VCM). Consequently, the set process is governed by the diffusion of metal ions or by the migration of V_Os. However, for the reset process, the rupture of the conductive filament is considered to be governed by thermally diffusion instead of ion dissolution.

In Figure 1-11, a schematic of a complete RS cycle is depicted for a Ni/NfO_2/Si MIS-structure. Initially, the device at a pristine state has a random distribution of oxygen vacancies and no metal ions have migrated yet (a). By applying a positive voltage to TE, the migration of metal (Ni) ions and V_Os begins due to the ECM and VCM mechanisms, respectively. Initially, oxygen vacancies are forced to reorganize as explained in VCM. However, when the applied voltage increases sufficiently, metal ions from TE are able to migrate through the oxide (b) and to be deposited in BE-oxide interface as voltage, and consequently the metal-ion migration, increases [38], [39]. When enough positive voltage is applied, the device reaches the LRS state (c) due to the formation of a conductive filament constituted by V_Os and metal cations where metallic conduction predominates. Once the CF is created, the forming process

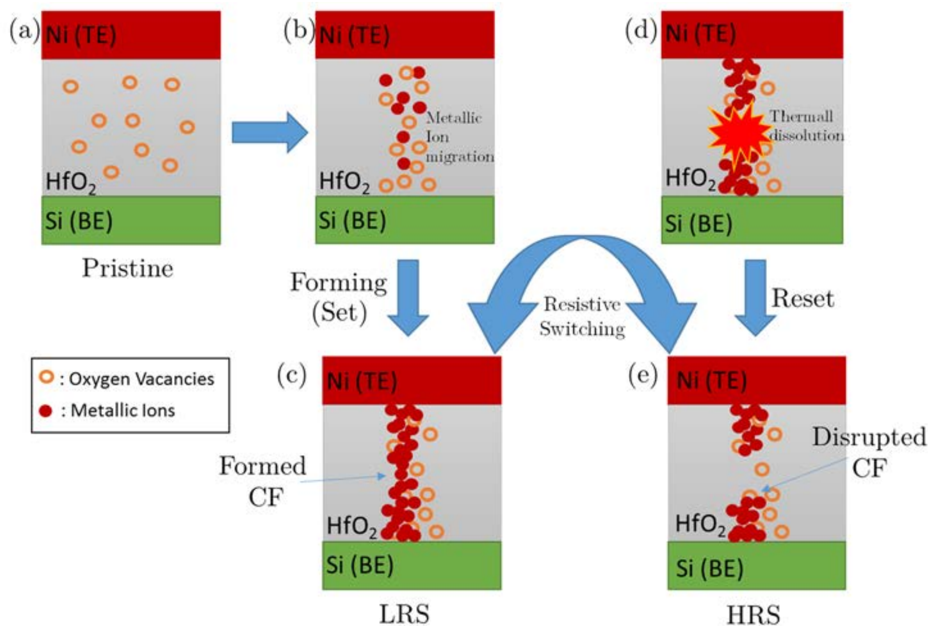


Figure 1-11: Schematic of metallic filament formation and rupture in a TCM device. (a) Initial state of the device before none voltage is applied yet. (b) Metallic ion and vacancies migration when positive voltage is applied to the TE. (c) Device at LRS state when filament is completely formed. (d) Rupture of the filament due to joule heating when positive voltage is applied. (e) Device at HRS state when filament is partially disrupted.

has been performed. With device at LRS state, if a positive voltage bias is applied again to the TE, contrarily to ECM and VCM, conductive filament can be ruptured switching the device to HRS state. As voltage increases, more metal ions (and also oxygen vacancies) migrate increasing the current through the filament. A self-accelerated mechanism occurs producing the increase of temperature, controlled by the applied voltage and current, by Joule heating [40], [41], in the narrowest parts of the filament. At a certain temperature, CF is ruptured by thermal dissolution of the ions that was forming the CF (d). After that, the device reaches the HRS state (e). Applying positive voltages successively over the top electrode, set/reset cycles can be performed.

Therefore, TCM mainly allows explaining the unipolar RS operation mode. However, in a device showing unipolar RS, the bipolar operation mode can be also observed due to the coexistence of V_Os and metallic ions in the CF.

Unlike the mechanism governing set process, which seems well known in all the cases introduced so far, there are still some unsolved questions about the mechanism governing reset process in TCM, such as: does the rupture of the filament occur over the entire CF or just at a certain point? How does the CF shape affect to the process? Or how much amount of power is needed to trigger the process? Some of these questions are partially answered in [42] or [43]. Regarding the latter question related to the power, the work done during this thesis contributes with the analysis of the energies needed to trigger set and reset processes which have been observed to be critical RS parameters (chapter 3).

1.2. Reliability issues in resistive switching

As pointed out in the introduction, there are reliability issues affecting the RS functionality. The most concerning are state retention, endurance, variability and random telegraph noise. In this section, a brief overview of them will be included focusing more on the impact of random telegraph noise on RS devices because it has been covered in this thesis.

1.2.1. Variability

Variability is understood as those fluctuations of RS operation parameters such as forming, set and reset voltages or resistance states (or related currents). Fluctuations refer to any change in the value of a parameter appearing due to the stochasticity of the RS operations mechanisms. They can be observed between different devices (device-to-device), known as spatial variability, or in a single device between the

subsequent set/reset cycles (cycle-to-cycle), known as temporal variability. Another reason for the RS parameters variability is the impact of fixed parameters such as current limit (I_C) which can provoke fluctuations in operation parameters when its value is varied. For memristive devices, two kind of variability are differentiated: intrinsic (that variability due to the device itself) and extrinsic (related to the effects originated because of the combination of the memristor with external current limiter devices like a transistor, selector or resistor).

Some examples about RS variability are shown in Figure 1-12(a), where LRS and HRS resistance cumulative distributions of MIM memristors are depicted for different current limits (from 500 µA to 2 µA) [44]. A resistance variability increase is observed as current limit decreases. In LRS, for I_C = 500 µA the median value, µ, of the resistance is 10^3 Ω while for I_C = 2 µA, the median value has suffered a shift to ~10^6 Ω. In addition, a cycle-to-cycle variability is observed when current limit decreases. When I_C varies from 500 µA to 2 µA, cycle-to-cycle variability, identified as the deviation (σ_R) of the distribution, increases from practically zero to a half of a decade. Similar behavior is observed for HRS resistance.

On the other hand, in Figure 1-12(b) set and reset voltages, extracted from cycling measurements in a MIS-structure memristor, are depicted as a function of the number of cycles [45]. Cycle-to-cycle variability is observed in both set and reset voltages, which authors in [45] attribute to the random creation and dissolution of the metallic conductive filament. Furthermore, they have found that both voltages are statistically correlated by means of the Pearson coefficient as the inset in

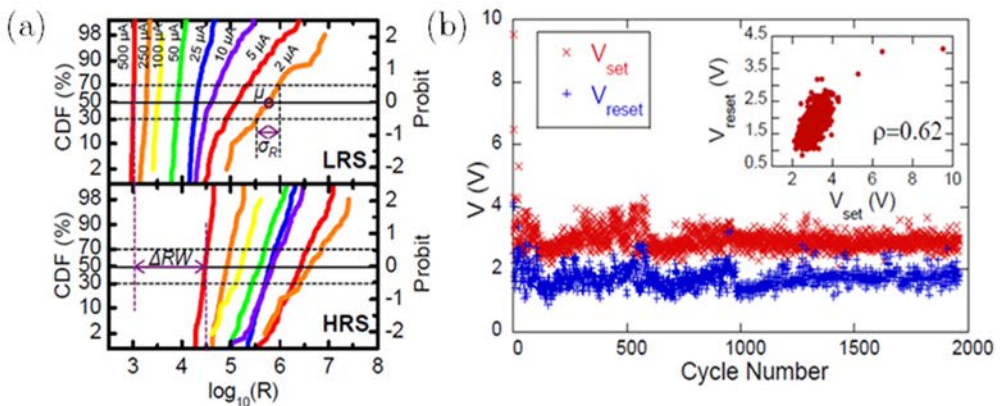


Figure 1-12: (a) LRS and HRS resistances cumulative distribution for different current limits. Mean value (µ); deviation value (σ_R) and resistance window (ΔRW) are indicated [44]. (b) Set and Reset voltages evolution along RS cycling. Inset shows the relation between both set and reset voltages which are correlated by the Pearson coefficiente (ρ) [45].

Figure 1-12(b) shows. Regarding dispersion, set voltage shows a range of values between ~3 V and ~4 V whereas for reset voltage the range is comprised between ~1 V and ~3 V. Such a set/reset voltage variability provokes an overlap in the operations voltages what can cause malfunction of the device when it is used, for instance, in memory or logic applications.

1.2.2. Retention

Memristive devices are mainly characterized by the non-volatile behavior of their states. However, the retention of those states is not boundless. The increase of the temperature, the operation time or simply the aging can provoke variations on HRS and LRS resistances which originates the retention failure.

Diverse experimental and simulation studies have been carried out to analyze the behavior of HRS and LRS resistances under different unfavorable conditions. For instance, in [48]–[50], authors have observed a retention failure of HRS state with time. Moreover, they have observed that the resistance at LRS tends to increase with temperature whereas HRS resistance decreases when increasing temperature. A time retention failure example is shown in Figure 1-13(a), where HRS and LRS resistances of devices are measured every 1s under a constant temperature of 180 °C [46]. Until time t_1 both states follow the projected device lifetime of ten years. However, between that time and time t_2, a retention failure is observed due to a sudden decrease of the HRS resistance. On the other hand, in Figure 1-13(b), a state retention test increasing the temperature is shown. Here, HRS and LRS memristor resistances are

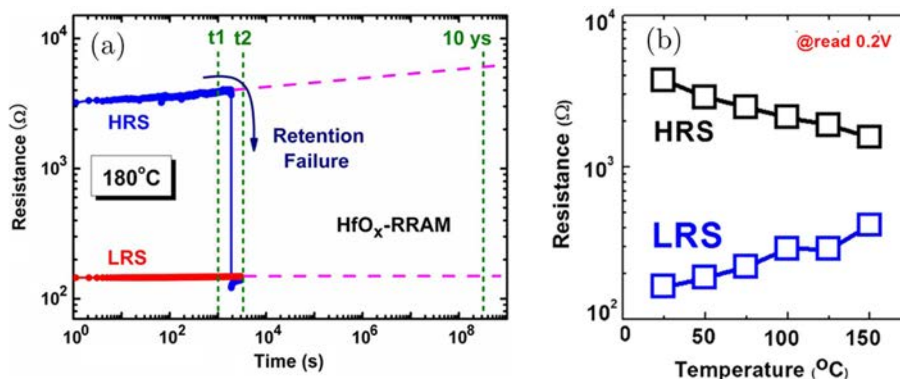


Figure 1-13: (a) HRS and LRS resistances measured every 1 s at 180 °C. After time t_1 the failure of HRS state is observed while LRS state is kept. Modified from [46]. (b) Temperature dependence of HRS and LRS resistances as temperature increases [47] where a resistance window decrease takes place as temperature increases.

measured at different temperatures [47]. Instead of the abrupt retention failure of any resistance state, a progressive degradation of memristor resistance at LRS (increasing) and HRS (decreasing) states is observed.

1.2.3. Endurance

Conceptually, endurance refers to the maximum number of switching cycles performed by a device until the decrease of the resistance window to an inacceptable value or to its complete closure, mostly related to the final failure of the device. Figure 1-14 shows an example of an endurance test of the resistance window for a HfO_2-based device [51]. As cycling increases, the resistance window decreases and it is completely closed after 10^8 cycles due to the decrease of HRS resistance while LRS remains almost constant. In other studies, the closure of the resistance window has been also observed because of LRS resistance degradation while HRS stays barely unchanged [52] or because of the degradation of both HRS and LRS states [53].

Along the years, endurance has been highly enhanced achieving up to 10^{12} cycles in bipolar RS operation mode [28], [54]. However, that large endurance is difficult to reproduce due to the lack of an absolute control on the stochastic resistance changes. In this way, RS research works have been focused on understanding what provokes the endurance failure in the different devices. For example in [55], authors found that the cause of the endurance failure in HfO_X-based devices is due to an irreversible set which occurs during the procedure to provoke the reset process.

Endurance and retention failures seems to be a very important reliability issues that are closely related due to their effect on resistance states. Due to that relation, optimizing one might have consequences on the other, so many times a trade-off

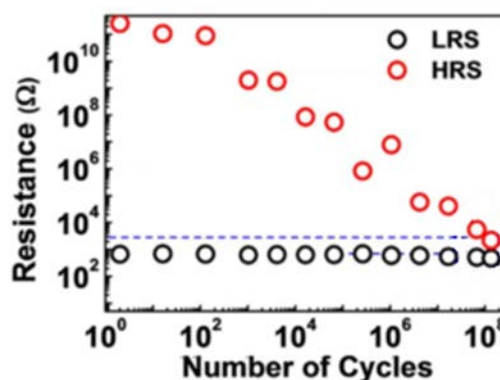


Figure 1-14: Resistance window evolution along RS cycling. After 10^8 cycles, a complete closure of the window is observed due to the degradation of HRS resistance, modified from [51].

between both reliability issues is necessary. The works performed in [56], [57], show studies on the endurance/retention trade-off on HfO_2-based and Ta_2O_5-based memristors, where authors demonstrate relevant improvements in endurance or retention at the cost of slightly getting worse other performance features such as resistance window.

1.2.4. Random Telegraph Noise

Random Telegraph Noise (RTN) observed in memristive devices consists in random dielectric current fluctuations between two or more discrete states when a constant voltage is applied to the memristor Figure 1-15. Those current fluctuations occur because the electrons flowing through the dielectric (mainly through the conductive filament) can be captured and emitted by existing defects (traps) in the dielectric (Figure 1-15(a)). Furthermore, higher current fluctuations can be observed in RTN signals originated by disturbances in the CF since ions (oxygen vacancies, metal ions), whose nature depends on the RS switching mechanism (VCM, ECM), are added or removed [58], [59] (Figure 1-15(b)). However, these higher fluctuations provoke morphological changes in the CF being more difficult to analyze with standard RTN characterization methods. In Figure 1-16, the two possible scenarios where RTN can appear are depicted for a memristive device (a) at LRS, (CF is completely formed with large current flowing through it) and (b) at HRS (when CF is partially disrupted and the current is typically several orders of magnitude smaller than at LRS state). Considering that most of the current through the dielectric is owing to CF contribution, current contributions can be produced by defects (empty

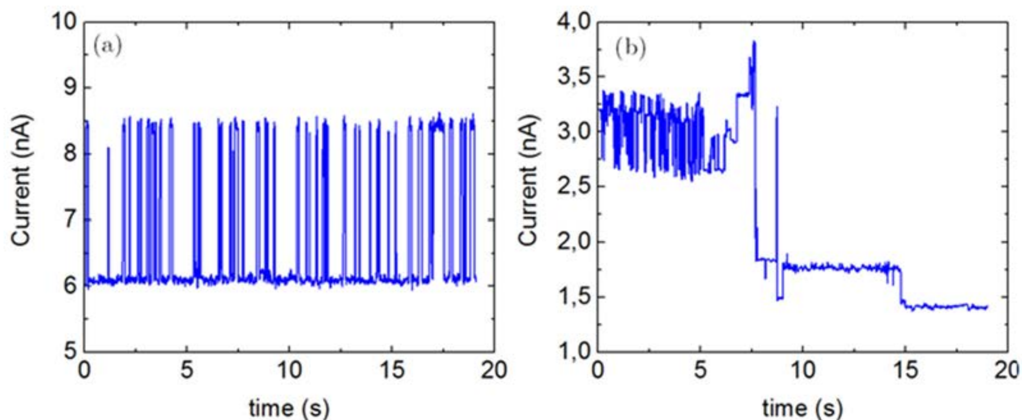


Figure 1-15: (a) RTN signal where stable current fluctuations between two current levels are observed due to one trap. (b) RTN signal with higher current fluctuations caused by addition or removal of ions to the filament [58].

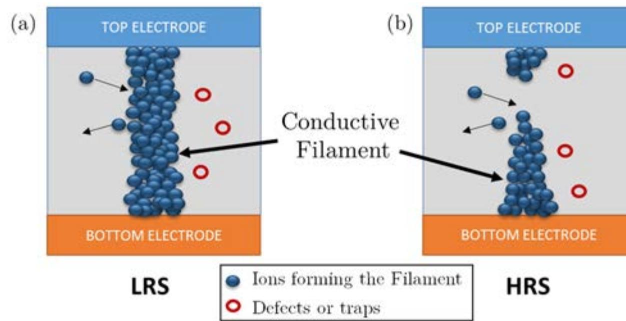


Figure 1-16: Metal-insulator-semiconductor structure at both (a) HRS and (b) LRS resistances states of RS phenomenon. In both scenarios, defects or traps responsible of RTN fluctuations are placed around conductive filament (red empty circles). Moreover, the addition and removal of ions (solid blue circles) causing higher current fluctuations are indicated by arrows.

red circles) located near the filament (where electrons can be captured or emitted) or by the addition or removal of ions (solid blue circles, the addition or removal is indicated by the arrows) to the filament. As extracted from the previous figure, the RTN impact on filament current is slightly different at LRS than at HRS. In the first one, considering a well-formed filament, current fluctuations are hardly observed since the current is quite large. On the contrary, at HRS the current is much lower and current jumps are easier of being observed. This is the reason why most of the works study RTN at HRS state, although the observation of RTN at LRS has also been reported [59], [60]. Overall, in memristive devices, the presence of RTN can cause a large spread in the distribution of the HRS and LRS resistances and induce errors, for instance, reading the wrong memory state stored in the memristor if the memory window is relatively small.

RTN characterization

Just regarding current fluctuations due to traps, detection of RTN signals can also serves as a tool to determine the number of traps, the characteristic times of the trap (as the emission (τ_e) and capture (τ_C) times), the spatial trap location from dielectric-electrode interface and the trap energy depth below conduction band of dielectric [61], [62]. Nevertheless, before identifying trap properties, RTN signal must be properly characterized. The simplest way to analyze those signals is plotting every point of the current of a RTN trace in a histogram which is quite feasible when the fluctuations are only between two levels as shown in Figure 1-17. However, as the complexity of the RTN signal increases either due to the enlargement of the background noise or the rising of number of traps, analysis methods must be enhanced. Different methods to analyze and characterize RTN have been developed [63] but those based on that proposed in [62] have become the most common. In [62]

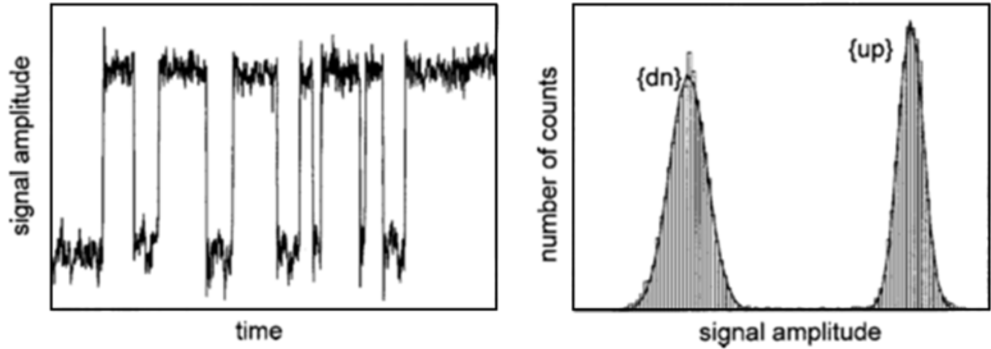


Figure 1-17: An experimental random telegraph signal showing two current levels. The histogram plot of the previous RTN signal. Two amplitude histograms (dn and up) corresponding to the current levels appear well differentiate without overlapping [64].

authors presented a method to study RTN signals which uses a Time Lag Plot (TLP). Figure 1-18 shows an explanation to get such a plot. The (i+1)-th current points of a RTN signal (left) are plotted against i-th current points of the same RTN signal to obtain the individual points shown in Figure 1-18 (right). In this plot, points located along the diagonal of the plot correspond to the current levels (points 1 and 4) whereas points outside the diagonal indicate the transitions occurred between those levels (points 2 and 3).

As an example, Figure 1-19(a) shows a current trace corresponding to a simulated one-defect RTN signal, what means that only two current levels exist. Applying the previous method, the TLP depicted in Figure 1-19(b) is obtained revealing four point clusters. Those located at the diagonal of the plot indicate the current levels of the RTN signal, identified as high (I_H) and small (I_L) current. On the contrary, the other two point clusters outside of the diagonal reflect the transitions between currents

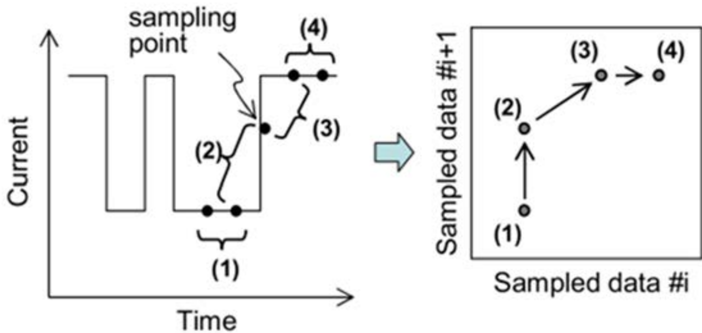


Figure 1-18: Explanation of how to create a time lag plot (TLP) from a current trace [62].

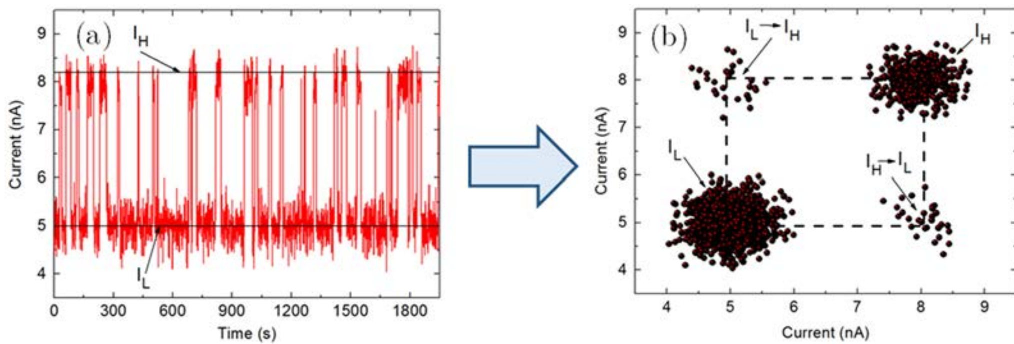


Figure 1-19: (a) Simulated RTN signal caused by a single defect. (b) The corresponding time-lag plot: two populated clusters on the main diagonal indicate the two levels. Other clusters of points outside the diagonal correspond to transition between levels.

levels (from I_L to I_H and from I_H to I_L). Note that a one-defect RTN signal creates a square in whose vertexes those clusters are located. Based on the number of clusters placed along the diagonal, that is, the number of RTN current levels, authors in [62] proposed a way to determine the number of detectable traps. Considering that $2^{(n-1)} < \text{(current levels)} \leq 2^n$, then the number of detectable traps originating current fluctuations corresponds to n.

Despite the fact that TLP method is very useful when the RTN current fluctuations are well defined, it becomes limited when the background noise is more relevant or when multilevel RTN signals are measured since different clusters can overlap each other. To overcome those limitations, in [65], an enhanced RTN characterization method named Weighted Time Lag (W-TL) is proposed. The method mainly improves TLP-based method minimizing the effect of the background noise in a RTN signal. The W-TLP method calculates a weighted function, which is based on a normal bivariate distribution of i-th point and (i+1)-th point, on each dot in TLP. Then, the weighted function is plotted as a contour plot where x and y-axes correspond to the current of i-th and (i+1)-th points, respectively (Figure 1-20(c)). On the other hand, the color map of the figure represents the weighted function (in arbitrary units) being 0 (red) the value of most populated region of the plot and -3 (blue) the value of empty region.

Figure 1-20(a) shows an experimental multilevel RTN signal of a pMOS transistor. Applying TLP and W-TLP methods to the signal the plots shown in Figure 1-20(b) and (c) are respectively obtained. In both TLP and W-TLP graphs, the diagonal of the plot is clearly identifiable but with the conventional TLP (Figure 1-20(b)) the levels are more difficult to identify. Those located at the corners of the different originated squares are the only ones that can be barely distinguished. However, some levels remain unclear due to either point overlapping or the small quantity of dots.

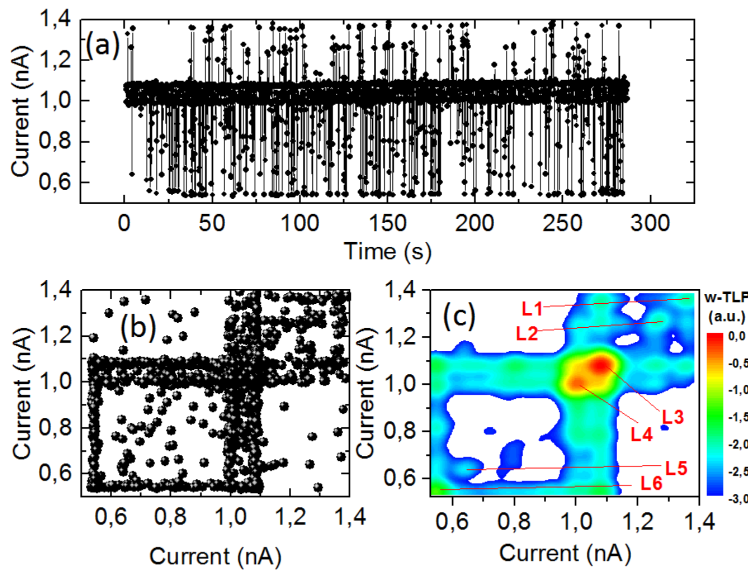


Figure 1-20: (a) Experimental multilevel RTN in the gate current of a pMOS transistor. (b) Conventional TLP and (c) W-TLP both obtained from the RTN signal presented in (a) [65].

On the contrary, using W-TLP, some levels that are not visible using conventional RTN characterization methods can be detected as corroborated by analyzing the Figure 1-20(c) where six different current levels have been encountered and labeled from L1 to L6.

The W-TL method also allows extracting the peak profile of the W-LTP diagonal corresponding to the different current levels of the RTN signal. Figure 1-21 shows the diagonal peak profile of the W-TLP shown in Figure 1-20(c). Apart from the six levels identified before as different red or soft blue-colored spots, two additional

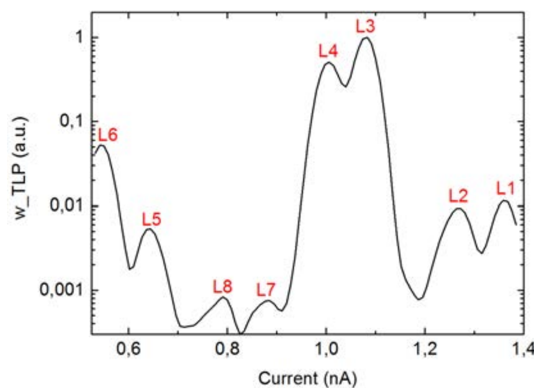


Figure 1-21: Peaks of the diagonal of the W-TLP shown in Figure 1-20(c). 8 peaks, i.e. 8 current levels are encountered instead of the 6 levels from W-TLP.

current levels (L7 at ~ 0.88 nA and L8 at ~ 0.8 nA) are distinguished. Just considering the first six encountered current levels and taking into account the parameter extraction procedure of the TLP-based method, three traps are detectable ($2^{(n-1)} < 6$ current levels $\leq 2^n$ what means n = 3). These two additional levels (L7 and L8) are consistent with the total number of current levels that should exist ($2^{3\ traps} = 8$ levels).

The characterization of RTN signals is more accurate using the W-TLP method, so it will be used to analyze the RTN signals measured by an enhanced setup, described in chapter 3, developed to register RTN signals in more detail.

1.3. Applications of resistive switching phenomenon

Memristive devices have been proposed to be implemented in many applications such as memory, logic computation, selectivity, artificial neural networks or novel computing based on randomness. Therefore, in this section, these applications will be described a bit more extensively, presenting some innovative works performed to date.

1.3.1. Memory applications

Most studied application of memristive devices in the last decades has been like memory device. As resistance is the active variable of such devices, memristive memories are widely known as Resistive Random Access Memories (RRAMs or ReRAMs).

A memory device consists in an element capable of storing information as a bit ("0" and "1"), which has been stored traditionally by generating and removing charges, respectively, in a MOSFET transistor. Nevertheless, as a memory element, a memristive device allows storing that bit information by its resistance levels (referred to as HRS and LRS). As known, LRS and HRS states can be related to "0" and "1" digital values. For instance, to write a "1" bit, the memristive device must be switched to LRS state by applying the required voltage to provoke the set process. On the contrary, to write a "0" bit, a voltage to provoke the reset process must be applied to the memristive device to switch it to HRS state ("0"). On the other hand, read operation can be performed by applying very small voltages (to avoid causing a state change) to know the resistance state (and therefore, the bit information) of the memory element.

Beyond their suitability for storing bit information, memristive devices or RRAMs have shown excellent operation properties desirable to become in the next generation

of specific non-volatile memories (NVM). Figure 1-22 shows some representative figures with relevant features observed in RRAMs such as:

(a) Great scalability. This figure represents a transmission electron microscopy (TEM) of the cross section of a RRAM with a width of 10 nm [66].

(b) Very large endurance. The figure shows consecutive resistance state changes for 10^{12} cycles [28].

(c) Excellent state retention. In [67] no experimental failure of HRS and LRS resistances for nine months at room temperature (RT) was observed.

(d)-(e) Ultra-fast switching speed. Both figures show the voltage across the device as a function of time when pulses of 100 ps are applied to provoke set and reset processes [68], [69], respectively. A very fast set and reset transitions take place.

Until now, these excellent properties have been observed separately in many different

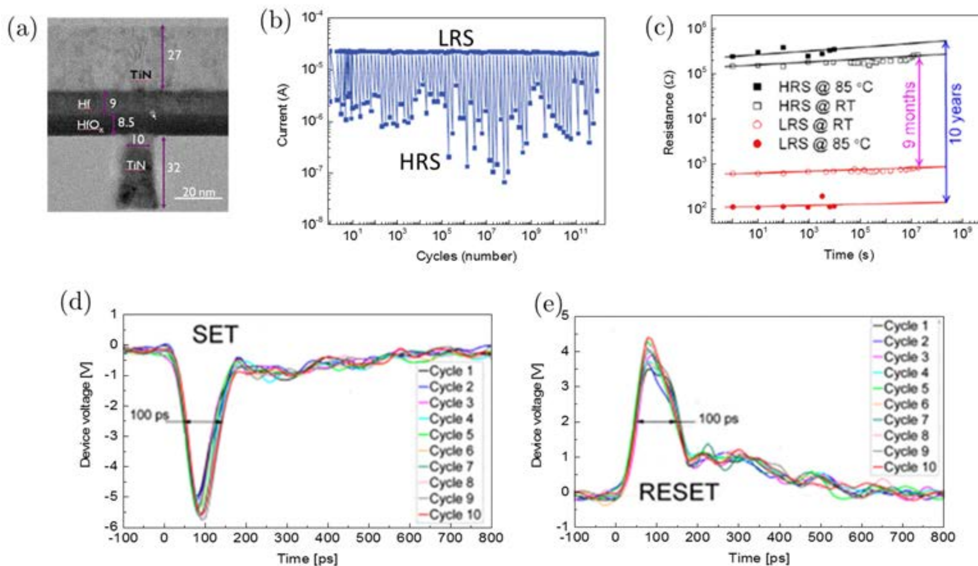


Figure 1-22: Some examples of the great features exhibited by different RRAM devices. (a) TEM image of the cross section of a RRAM showing a device size below 10 nm [66]. (b) HRS and LRS currents, registered to analyse the device endurance propierties, showing an adequate resistance window up to 10^{12} cycles [28]. (c) Experimental retention of nine months for both resistance states at room temperature (RT) [67]. (d)-(e) Voltage across the device during set and reset processes, respectively, while pulses of 100 ps are applied [69].

materials and combining them into only one device is still awkward. Although such a "universal" structure has not been discovered yet, many studies, analysis, experiments and simulations have been done in the way. In recent years, for example, scientific community has studied the impact of the voltage ramp speed on the conduction mechanisms [70]; compact models for RRAM depending on the filament's shape have been also presented [71] or new materials have been explored for RRAM implementation like in [72] where authors present a two dimensional material based on hexagonal boron nitride showing low set/reset voltages. In this sense, in this thesis, critical parameters such as the required voltages to provoke set and reset processes or necessary energies to perform these processes have been performed.

Regarding RRAM implementation, the most typical architecture to organize single memory elements to form a macroscale memory (such as USB, micro-SD, SSD and so on) is the well-known crossbar array association, which is formed by different word lines and bit lines connected by a cross-point where memory element is located. Figure 1-23 shows a memory crossbar array where one device can be accessed to be read or written by applying voltages to both word and bit lines. The zoom in the figure shows the activated device, i.e. the memory element where the bit will be stored, which would correspond to the location of the memristive device. During many years, 2D crossbar array, as that shown in Figure 1-23, has been the most typical structure for the organization of memory elements. However, to increase the integration density, 3D crossbar array solutions have been proposed recently to implement similar applications than 2D [73]–[75].

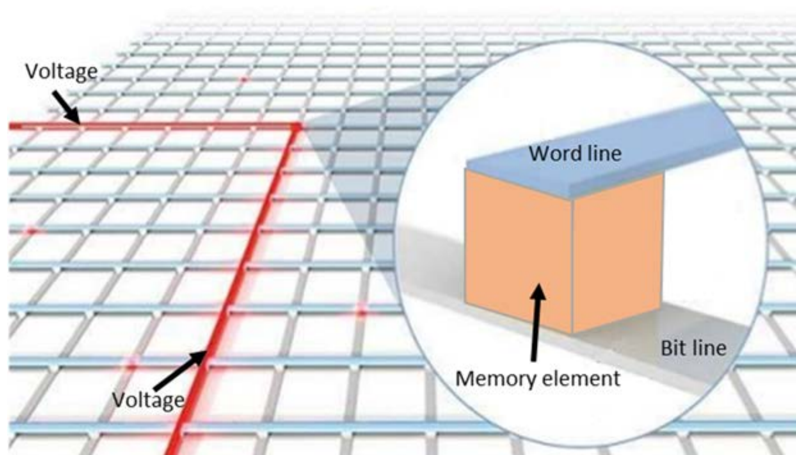


Figure 1-23: Crossbar array where one memory element is selected by applying adequate voltage to both word and bit lines. A zoom of the cross point where memory element is indicated. Readapted from http://www.slideshare.net/Jeevanvas/jeevan-memristor.

1.3.2. Digital applications

Use of memristors in digital applications may allow a new paradigm of computation since these devices can operate as a memory element and implement logic operations. Therefore, the memory and processing unit, separated in conventional computing systems, may exist in a module containing both of them. In this way, several works have demonstrated the proposal of using memristive devices as logic gates. Authors in [76] demonstrate the functionality of logic gates based on memristive devices, specifically by using MIM structures based on GeS_2 as resistive switching active layer. In Figure 1-24 a schematic of the four cases of a AND gate based on memristive devices is shown. From the figure, it is observed that the structure proposed to implement the different logic gates are made up with two memristive devices connected in series, which can be accessed individually for writing or reading operations. Contrarily, to perform the logic operation, both devices must be biased together by applying a unique voltage at the top electrode of the upper device and grounded the bottom electrode of lower device.

More designs have been proposed for the implementation of memristive-based logic gates. More recently, based on their previous work in [77], authors presented in [78] a new methodology to help in the development of logic gates, where the memristor resistance is used as a logic value. The design proposed by the authors, called MAGIC (memristor-aided logic), include at least three memristors, two of them acting as the inputs and the third one as the output of the gate, unlike previous presented structure. Authors demonstrated the functionality of NOR, NAND, OR, AND and NOT logic operations by using the MAGIC structure and described the procedure to be followed for future designs of logic gates based on memristors.

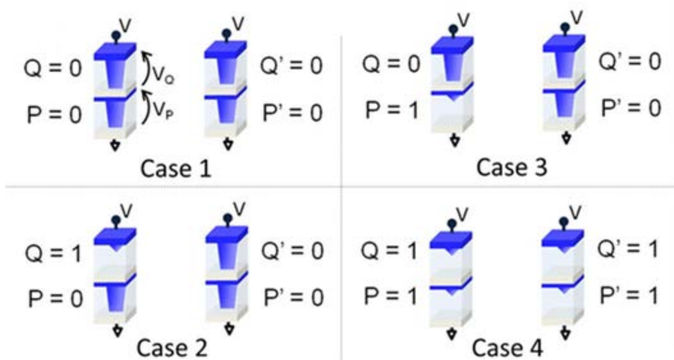
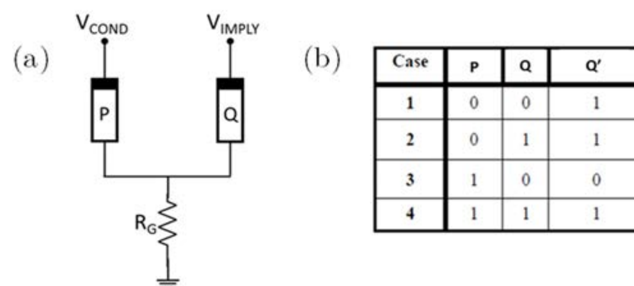


Figure 1-24: Schematic of the four cases of a memristive-based AND gate. On each case, at left side, the intial (inputs) states and at right sied the final (output) states of the meristive device forming the gate [76].

Another concept called material implication (IMP), which leads to a new logic gate labeled as IMPLY, has been proposed to be developed using memristors. Implication logic operation was initially studied in [79] and experimentally demonstrated in [80]. Figure 1-25 shows (a) the schematic of the circuit to implement such a novel logic gate and (b) its associated truth table. An IMPLY gate is formed by two memristive devices (P and Q) whose bottom parts are connected to a series resistor (R_G) as shown in Figure 1-25(a). The initial resistance states of RS-devices P and Q are the inputs of the gate whereas the resistance state of memristor Q after the IMPLY operation (Q') corresponds to the output (Figure 1-25(b)). By applying adequate voltages to memristors P (V_{COND}) and Q (V_{IMPLY}), IMPLY operations can be performed accomplishing the truth table included in Figure 1-25.

In addition, IMPLY can be considered as a fundamental Boolean logic gate of two inputs, P and Q, and an output whose operation can be described as '*if P is true then output follows Q otherwise it is true*' or simpler '*if P implies Q' or 'if P then Q'*.

During the last years, the research about IMPLY has been focused in modeling and simulating IMPLY behavior or in exploring different device configurations to become in a competitive logic gate [81]–[84]. For example, in [81] authors showed for the first time, a modified logic gate based on IMPLY operations by using four memristors. They show the reliable multi-cycle operation of such a modified logic gate and their use to developed gates like NAND in a three-dimensional stack of memristors as shown in Figure 1-26. This figure includes: (a) the equivalent circuit of the structure. (b) A drawing of the device cross section with related materials used in every layer. (c) NAND gate symbol with input (B1 and B2) and output (T1) memristors indicated. (d) Truth table and operation procedure to perform such a NAND gate and (e) finally, experimental results of the case 1 of previous gate where 80 operation cycles were performed with a 93% of success.



Case	P	Q	Q'
1	0	0	1
2	0	1	1
3	1	0	0
4	1	1	1

Figure 1-25: IMPLY (a) gate schematic circuit consisted in two memristors (P and Q) and a series resistance (R_G). V_{COND} and V_{IMPLY} correspond to the voltages applied on P and Q to perform the IMPLY operations. (c) Truth table of the IMPLY gate.

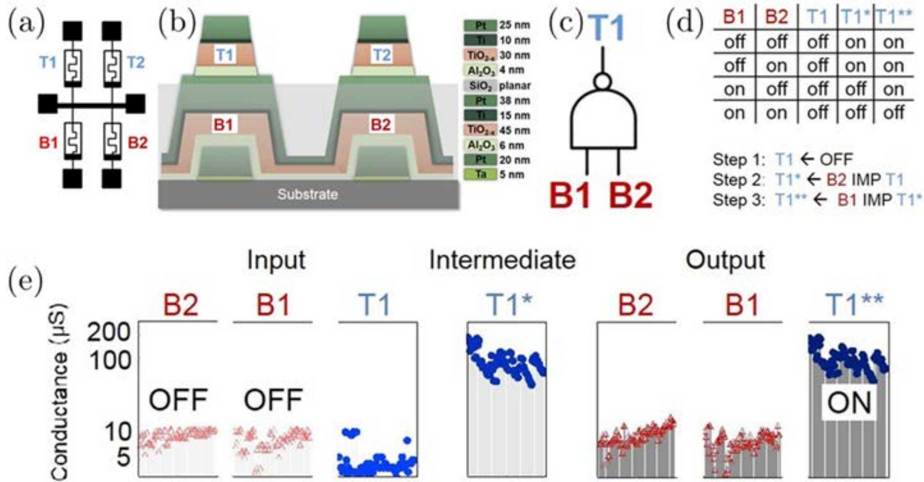


Figure 1-26: Details of the three dimensional IMPLY demonstrated in [81] (a) Equivalent circuit with four memristive devices where one is not used depending on the logic operation. (b) A drawing of the device cross section and the materials of each layer. (c) Schematic of a NAND gate based on IMPLY. (d) Truth table and operation procedure of previous gate. (e) Experimental resuls of the case 1 of the NAND gate where 80 operation cycles were performed. The intial and final states of the inputs and output, the intermediate states of the output are also included. Pictures extracted from [81].

Despite the different contributions previously commented, barely a few works have been focused on studying experimentally what happens on each memristor of the IMPLY gate when voltages are applied. For example, in [82] memristor current evolution is shown as a function of applied voltage, however, such evolution is not presented along the time in order to study the transient of memristors behaviour. In this sense, in this thesis, apart from demonstrating experimentally the IMPLY functionality with HfO_2-based memristive devices, the transient of the memristors states has been also studied in all IMPLY cases.

1.3.3. As selector element

As pointed out in memory application, the most typical organization of memristive devices is in a crossbar array due to their high integration density. Ideally, the memory operation in a crossbar should takes place only on the selected cell, without affecting the surrounding cells and with no current leakage contributions. However, reality, leakage currents due to unselected cells contribute to the current through the selected cell inducing memory operation errors. The use of a selector device in series with the memory cell, is an alternative solution to that leakage issue. The leakage

current is suppressed because the selector device shows very low current conduction at small voltages, at which unselected cells are biased when performing memory operations. That leakage current is shown in Figure 1-27 [85] as the sneak-path current. In a read operation when the selected element is at HRS (center element in red in the figure) and the neighboring elements are at LRS, undesired leakage current (I_{sneak}) can flow through the unselected elements contributing to the read current (I_{read}) which should only be formed by the current flowing through the selected element ($I_{element}$). This extra contribution to I_{READ} provokes an increase of the power consumption, a reduction in the read-out sense margin and a limitation in the array size [8]. To solve this problem, different methods mainly based on adding an extra element to the memory device have been proposed: one MOSFET-one resistor (1T1R), one bipolar junction transistor-one resistor (1BJT1R), one diode-one resistor (1D1R) or one selector-one resistor (1S1R). The last one, which has been analyzed in this thesis, will be described with more detail.

Selector elements are based on the prior explained threshold switching mode operation (subsection 1.1.2.3). The role of a selector element in crossbar arrays is to select the addressed memory element and to isolate electrically the non-addressed elements. Figure 1-28 shows a crossbar array cell (a) with a memory device and (b) with the memory plus the selector device. To better show the operation of a selector device in a crossbar array cell, in Figure 1-29 an example of a read operation with and without selector device is depicted. Briefly, a selector device changes from HRS to LRS when applied voltage is larger than the threshold voltage, V_T (and smaller than - V_T for bidirectional selectors and negative voltages). However, it comes back to HRS when applied voltage is decreased below to a specific voltage, V_H, as shown in Figure 1-7. To analyze the selector behavior in a crossbar array, the worst read scenario where all the cells (the selected one and the unselected nearby) are at LRS is supposed (Figure 1-29(a)). If the word and bit lines are biased as indicated in the

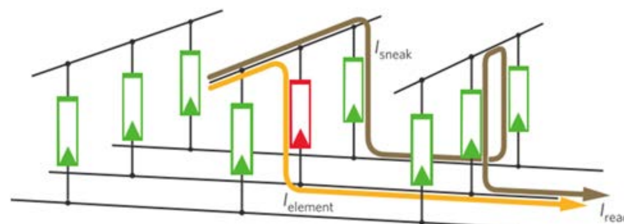


Figure 1-27: Sneak-path problem. The selected element is in the center (in red) at HRS whereas all surrounding elements are at LRS (in green). When reading the state of selected element, the current flowing through it ($I_{element}$) and a relevant current flowing through near elements (I_{sneak}) contributed to the current read by bit line (I_{read}) [85].

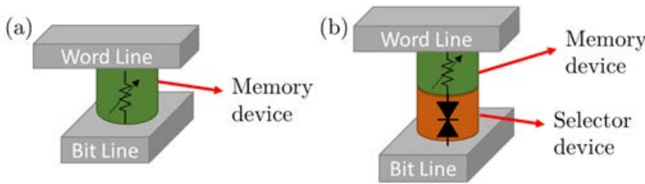


Figure 1-28: Crossbar array cell with (a) only a memory device and (b) a selector device placed in series with the memory device.

figure to perform the read operation, selected cell (big red square) is biased at V_{READ} while unselected cells (small blue squares) at ½ V_{READ}. Considering an array cell with just a memory device, the states of both selected and unselected cells will be those indicated in Figure 1-29(b) where the I-V curve to measure memristor states is depicted. Unselected cell state is very close to selected one what affects to the read measurement by increasing the expected read value. On the contrary, if an array cell is considered as the combination of a memory (Figure 1-29(b)) and a selector (Figure 1-29(c)) device, the I-V curve in Figure 1-29(d) is obtained. Now, the read value is not affected by unselected cell state because of the selector behavior. The unselected state is much lower at ½ V_{READ} than the selected at V_{READ}.

Although, selectors based on threshold switching have been only described here, more types of selector devices are currently investigated like those based on Si, metal-oxide

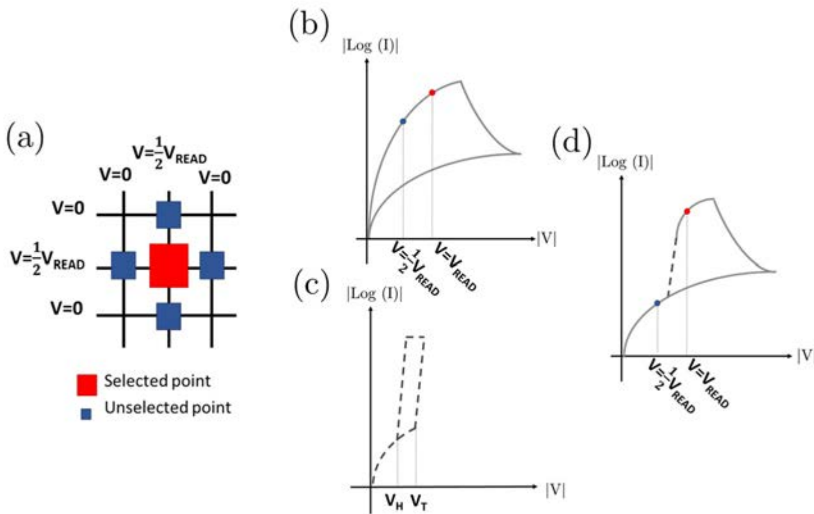


Figure 1-29: (a) Schematic of a crossbar array with a selected cell and four surrounding array cells. (b) I-V curve of a memory device where its state is read. At V_{READ}, the state of the selected cell is measured whereas at $1/2V_{READ}$ the unselected cell state is obtained. (c) I-V curve of a selector device. (d) I-V curve,where memory state is measured, of an array cell formed by a memory and selector device (1S1R).

or mixed ionic-electronic conduction to accomplish the requirements to be successfully implemented in crossbar arrays [86].

1.3.4. Neuromorphic applications

Although not covered in this thesis, another great application of RS phenomenon is to implement artificial neural networks. The interest in such a field, and particularly in the use of memristive devices as synapses, has increased hugely during last years thanks to the excellent memristor features like large scalability, very low power consumption, great endurance, fast switching speed and the multilevel switching behavior recently observed in some devices.

Very briefly, a neuron mainly consists of: a *cell body* (or soma), which contains specialized organelles where the computation is performed; *dendrites*, which are branched extensions arising from the cell body that receive signals from other neurons; an *axon*, a long cellular extension that transmits the signal to other cells and the synapses. Connecting the axon end and the dendrites, a synapse is encountered as a small gap (20-40 nm) junction that acts as a very complex interconnection network among neurons. Synapses allow passing electrical or chemical signals, depending on the type of synapse, from a presynaptic neuron to a postsynaptic neuron (Figure 1-30). To do this, the synapse changes its connection strength (known as synaptic plasticity) because of neuronal activity. It is in this process, where memristive devices have been proposed to develop synapse-like electronic devices. A memristive device may act as a synapse owing to its tunable resistance state (resistance plasticity), which can be related to the synaptic weight, and to the large connectivity that memristive devices can offer, what could reproduce the massive neuron interconnection.

Figure 1-31(a) shows an experimental example of the controllability of the resistance state of an HfO_X-based memristive device. The resistance can be continuously changed by performing continuous set (potentiation), with different current limits, and then continuous reset (depression) increasing the voltage at which reset process is stopped. Furthermore, in Figure 1-31(b), a schematic of a simple artificial neural network consisting in ten inputs (V_i) and three outputs (f_j) connected by 30 synaptic weights (W_{ij}), which are electronically implemented by the continuous resistance states of a memristive device, is depicted.

Therefore, the idea of reproducing the information processing occurring in the brain by means of computation and computer science theories has led the research community to investigate neuromorphic computing during decades. Most of the software simulations and hardware implementations performed in the artificial neural network field have been based on CMOS technology. However, the recent advances

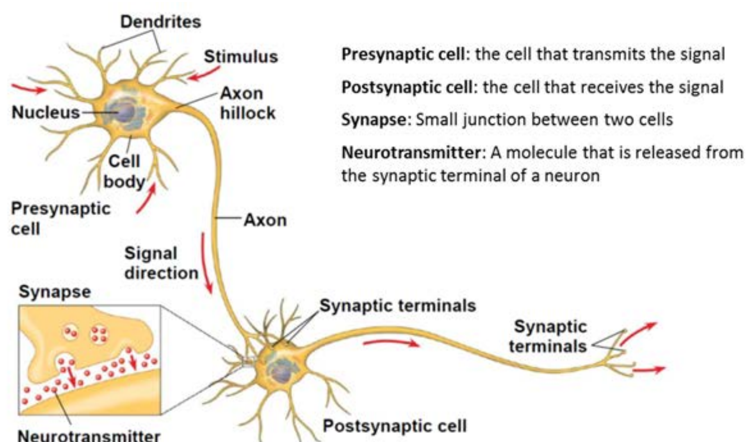


Figure 1-30: The major parts of a neruon in communication with another cell. Synapse is the most interesting part from memristive device application point of view [87].

in nanodevices has provoked a change in the neuromorphic approach. Different device systems with the property of change their resistance such as phase change memory (PCM), conductive bridge type memory (CBRAM) and resistive change memory (RRAM), among others, have been investigated in this field.

Focusing on RRAMs, many different RS materials such as TiO_X [88], HfO_X [89], WO_X [90] or AlO_X [91] have been studied to implement synaptic devices. They have been used to demonstrate the feasibility of an individual memristive device as artificial synapse [88], [92] or to implement more complex neural networks [93]–[95] as for example, for visual pattern recognition. Currently, neuromorphic works are focused on fully implement a neural network. For instance, in [93], authors experimentally demonstrate the implementation of a neural network using memristor in a transistor-free crossbar. Typically, the learning of a neural network is a

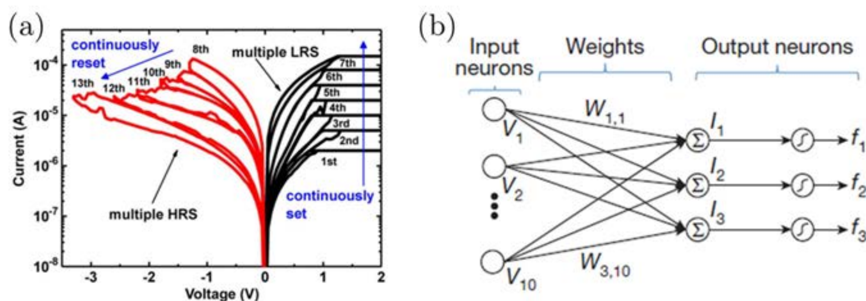


Figure 1-31: (a) I–V characteristics of metal oxide-based synapse device where the resistances are continuously changed, and multiple states are obtained [89]. (b) Schematic of a neural network with ten inputs and three outputs fully connected each other by 30 synaptics weights [93]

supervised process in which the response of the circuit is corroborated externally. However, unsupervised learning is even more attractive. Thus, current works are focusing on that as in [96] where authors demonstrate neural networks with CMOS/RRAM synapses capable of unsupervised learning.

1.3.5. Stochastic computing and security

As mentioned, one of the most relevant reliability issues is the spatiotemporal variability that memristive devices suffer. Switching parameters can vary from device to device (spatial variability), for example, due to irregularities in the dielectric film thickness and from cycle to cycle (temporal variability) in the same device, mainly because of the stochastic nature of the filament that dominates the switching of the devices. Temporal variability has been one of the main blockage for implementing memristive devices in manufacturing and commercialization. During the study and improvement of temporal variability, it has been observed that the stochasticity of the switching can be well characterized and controlled (the switching process follows a Poissonian distribution). This fact suggests that devices exhibiting such a randomness can be used for non-deterministic applications like stochastic computing instead of forcing them to be implemented in deterministic application like digital memory storage.

An example of the stochasticity application is demonstrated in [97], where authors show how the randomness inherent in memristive devices can be predictable making it useful for producing bit streams. Based on their work in [98], they explain a stochastic operation using a numerical representation that involves bit streams. Stochastic computing considers the probability that the bit in a given bit stream is equal to one as the number operation, i.e. if M is a bit stream of fifty bits where 20 are ones and 30 are zeros, the number is represented as m = 0.4 (0.4 is the probability that a randomly chosen bit is one). This example is experimentally presented in Figure 1-32 where the current of a device initially at HRS has been measured after applying consecutive pulses of 2.5 V of amplitude and 300 ms of width time. Randomly, the device switches to “1” or remains to “0” on each attempt, generating a bit stream whose related number is 0.4. [97].

Memristor resistance dispersion can be also applicable in low-cost authentication and key generation fields. Specifically, in developing physical unclonable functions (PUFs) [99] where randomness is a desirable property. PUFs are a promising technology to replace current nonvolatile memories in authentication and secret key storage because they are easy to fabricate, consume less power and allow more device density. Moreover, they do not require expensive cryptographic hardware or key encryption algorithm since PUFs operation is based on the physical characteristics

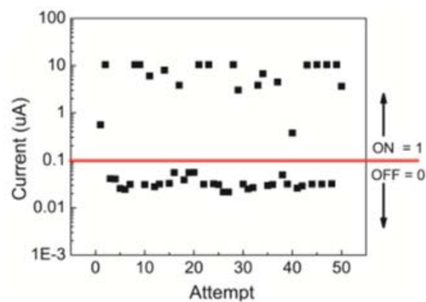


Figure 1-32: Current measured after repeated application of a single 2.5 V, 300 ms pulse in order to switch the device from HRS to LRS [98].

of the circuit. Among different architectures to implement PUFs like optical-based [100] or arbiter(silicon-based) [101], recently those based on memristive devices (mrPUF) have gain a lot of interest because the memristive devices cover most of the characteristics required for PUF applications [102]. More recently, some works have also shown the applicability of memristive devices in security as in [103], [104].

1.4. Experimental and analysis equipment

Eventually, since this thesis has been thoroughly experimental, in this section the equipment used in this work and the procedure to control such equipment will be presented. In addition, the software used to control and perform the measurements as well as to analyze collected data will be shown.

1.4.1. Experimental equipment

The main instruments used during this thesis to perform the different measurements have been:

Two kind of probes to place the device and contact it, one with a manual controlled chuck and another one with a remote-controlled chuck which also would allow carrying on temperature measurements.

Two semiconductor parameter analyzers (SPAs), the *Agilent 4156C* and the *Keithley 4200SCS* which include a source measure unit or source-measurement unit (SMU), which allows the SPA simultaneously to apply voltage (or current) and measure current (or voltage) from a device under test. Voltage (or current) sweeps or constant voltage (or current) can be applied with these equipments.

Furthermore, a pulse generator *Agilent 81101A 50 MHz* has been used to apply square pulses and an arbitrary waveform generator *TTi TGA12104* to apply pulses

with a specific waveform. In order to register data in the time domain, digital oscilloscopes *Tektronix TDS 210* and *LeCroy waverunner XI series* have been mainly used in pulsed measurements.

Finally, a current input preamplifier *Signal Recovery 5182* has been used to convert current into voltage, a programmable DC power supply *Keysight E3631A* to apply constant voltages and a heating oven *Binder APT.line™ ED* for temperature measurements when devices need to be baked.

1.4.2. Instrument control by GPIB communication

Briefly, GPIB (General Purpose Interface Bus) is a short-range digital communications 8-bit parallel multi-master interface bus specification which makes possible the instrument communication. A basic GPIB instrument control system consists of four parts:

1. PC (which is in charge of controlling all GPIB-connected instruments)
2. GPIB controller (A module included in the PC to connect it with other instruments which also has such a module)
3. GPIB cable (allows to connect the instruments among each other)
4. GPIB instrument (all the instruments controlled by PC)

Although control and data transfer might be relatively slow, GPIB allows controlling different instruments at the same time. A sketch of a GPIB instrument control system with a computer and several controlled instruments is shown in Figure 1-33. Communications functions are logically separated; a controller can address one device as a “talker” and one or more instruments as “listeners” without having to participate in the data transfer. Furthermore, it is possible for multiple controllers to share the same bus; but only one can be the main controller at a time. By means of GPIB commands an individual instrument can be controlled by a GPIB-controlled computer which may either perform a set operation (e.g. enabling instrument output or stablishing an instrument parameter value) or a query operation (e.g. reading voltages or asking for some instrument information). Hardware interface available in the instrument that allows the communication with a single host is made by the different manufacturers; therefore, GPIB commands are not usually standards for all the manufacturers, which may use different commands for the same function. To avoid misunderstandings, Standard Commands for Programmable Instruments

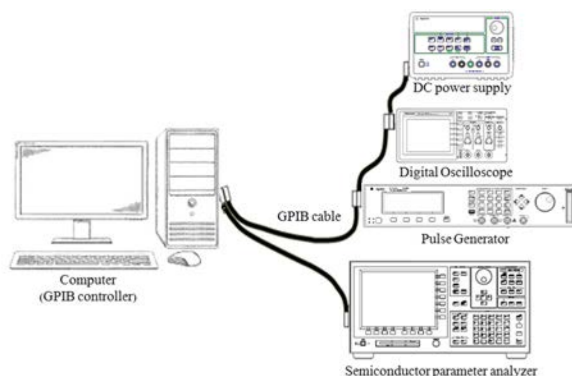


Figure 1-33: Sketch of a GPIB communication example between a computer as the GPIB controller and a semiconductor parameter analyzer, a pulse generator, a digital oscilloscope and a programmable DC power supply.

(SCPI) was developed in 1990. They consist in a more intuitive set of commands that allow the same set and query operations as GPIB commands, although, not all the instruments have been designed to use SCPI commands. Both commands have been used during the thesis depending on the requirements of the measurement. Following, an example of a set operation to establish a voltage source value of 5 V on the SMU number 1 in the SPA Agilent 4156C is shown by using GPIB commands and SCPI commands:

GPIB Commands “DV chnum (SMU number), range, voltage”

“DV 1, 0, 5”

SCPI commands “:PAGE:MEAS:CONS:SMU<num> voltage”

“:PAGE:MEASure:CONStnat:SMU1 5”

1.4.3. Software for instrument control and data analysis

The commands present just before are sent from the computer to the instruments by means of a software. Most of the instrument manufacturers provide to customers with commercial software, which are capable of sending instructions to the instrument and receive required information. However, these software have some restrictions to perform specific measurements required by the costumer. The most typical limitations are: the lacking of commands to implement required operations such as stopping the measurement when certain conditions is reached and the difficulty to program a complex measurement procedures where, for example, operation conditions are changes while the measurement is executed. Thus,

MATLAB software has been used in this thesis for that purpose by creating different scripts in which set and query operations are performed. This has permitted carrying on very laborious measurements when several instruments has been controlling at the same time. GPIB communication by using MATLAB scripts is based on creating an interface object (similar to create a file in c-programming language), then beginning the communication (like opening the file) and finally, writing and reading data, which would correspond to set and query operations. To recover instrument control, the communication must be disconnected (by closing the object). In Figure 1-34, a simple MATLAB script where a voltage is applied through a SMU and a current datum is read from the same SMU is shown.

The use of GPIB communication and MATLAB software has allowed performing smartly RS measurements by stopping the measurement when current reaches the current limit during the set process or reset process. In RS measurements, one of the most critical concerns is related to define the final voltage value when a voltage ramp is applied to provoke the reset process. If this voltage value is large enough an irreversible set process can takes place. Due to the variability of the voltage at which RS processes occur, it results very difficult to establish an adequate voltage sweep to perform the reset process and not provoke the subsequent set process. By using GPIB and MATLAB to perform the measurements, it has been possible to register the current point by point in order to make decisions while measurement is running.

The combination of GPIB and MATLAB in measuring has also permitted register current signals by different instruments. For example, in RTN measurement a constant voltage is typically applied by a SPA, which also registers the current. However, using GPIB, MATLAB and a specific circuit, RTN signals have been registered both by a SPA and by an oscilloscope. The same setup has been used to perform RS measurements where set and reset processes have been registered in the time domain thanks to the oscilloscope.

```
ag=gpib('ni',0,1);  % GPIB object creation whose GPIB address is 1
fopen(ag);          % Instrument communication is open

fprintf(ag,'CN 1'); % SMU 1 is enabled

fprintf(ag,'DV 1,0,1'); % 1 V is forced through SMU 1
fprintf(ag,'TI? 1,0');  % Query to ask for the measured current in SMU 1
I=fscanf(ag,'%f');      % Measured current point is stored in matrix I

fclose(ag)          % Instrument communication is closed
```

Figure 1-34: Example of a MATLAB script where GPIB object is created, then instrument communication is open, a SMU is enabled and 1 V is forced through that SMU. Then, measured current is asked to the SMU and stored in a matrix. Finally, GPIB instrument communications is closed.

On the other hand, the control of the setup with MATLAB software allows modifying instrument parameters and measurement conditions. For instance, under pulsed conditions, changing the pulse parameters is very common to observe the device behavior or the influence of such parameters on the device operation. Without GPIB commands, the change of the studied parameter must be performed manually. However, by using those commands and the MATLAB software, parameters can be automatically changed what allows carrying out long measurements faster.

Regarding data analysis, MATLAB software has been also used to analyze all the data registered during every performed measurement. The main advantage of using MATLAB is that the registered data from all instruments has been collected by means of the same software. Therefore, all data are perfectly prepared to be analyzed by MATLAB. Using the standard syntax of MATLAB, different scripts have been developed to perform data analysis tasks such as I-V recreation, parameter extraction or statistical analysis.

2. Analysis of Resistive Switching in MOSFET

As concisely indicated in the introduction chapter, the observation of resistive switching phenomenon in MOSFETs allows a deep phenomenon study. Specifically, taking advantage of the source and drain regions, the location of the conductive filament along the transistor dielectric length can be approximately identified. The identification of this location is a feature of the RS phenomenon more difficult to analyze in simpler structures as memristors. On the other hand, the access to all the transistor terminals opens the possibility to control the filament location along the transistor channel, depending on the voltages applied to the transistor terminals. The feasibility to manage the creation and disruption of the conductive filament in different locations could be potentially used to implement multi-state memories or switches. In this regard, it is necessary to explore the possibility to control the filament location in the transistor dielectric.

In this chapter, an initial characterization of resistive switching phenomenon in MOSFETs is firstly presented applying different voltage conditions. Then, the conductive filament location is intended to be controlled is described showing the obtained results. Finally, taking advantage of measurements where the location of the conductive filament is well-know, a method to calculate separately the different current contributions on transistor's gate current flowing through the dielectric is proposed: the one related to the conduction through the formed conductive filament and the other one related to the conduction through whole area of the dielectric.

2.1. MOSFET samples description

Samples used in all the experiments presented in this section have been supplied by the Interuniversity MicroElectronics Center (IMEC) of Leuven, Belgium. Samples, schematically shown in Figure 2-1, have been strained pMOSFET transistors with Ni-rich Fully Silicide (FUSI) gate electrode. Their dielectric gate stack consists of two layers: 1 nm-thickness of SiO_2 and 2.6 nm-thickness of HfSiON (with a Hf concentration of 60%). Therefore, this stack has an equivalent oxide thickness (EOT), i.e. the thickness of a silicon oxide layer needed to produce the same effect as the previous dielectric stack, equal to 1.4 nm. Finally, transistor bulk is compound by Si-n^+ what provokes an inversion channel formed by positive carriers. The size of the samples above described has been a width (W) of 0.15 µm and two different lengths (L) of 0.145 µm and 0.25 µm.

The strained MOSFETs consist in a source and drain regions where Ge atoms have been included during fabrication process to provoke a mechanical stress over the channel by compressing it. This modification on the source and drain regions would enhance the carrier mobility along the channel.

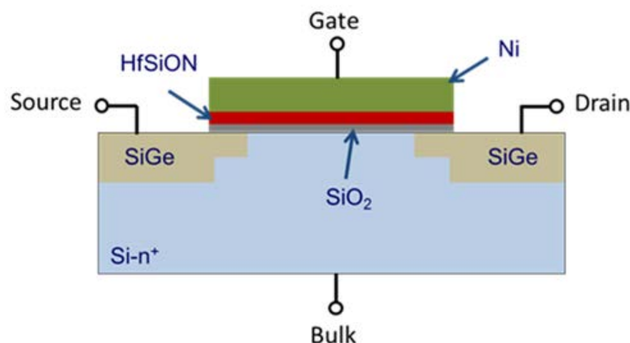


Figure 2-1: Schematic of the MOSFET samples. Materials of the different regions have been also indicated.

2.2. Resistive switching characterization

In chapter 1, where different RS operation modes have been described, it was indicated that such operation modes can individually occur or coexist in the same device. It is necessary to distinguish which one takes place and know which the best operation mode is in terms of endurance if both operation modes can be observed. Furthermore, recognizing the operation mode occurring in a device may help in

identifying the physical mechanism involved in RS performance. In this way, initial experimental resistive switching measurements have been performed on the described transistors. Previous RS studies carried out on similar samples [6] analyze voltage conditions to observe the RS. Following these studies, a more detailed RS analysis has been done under bipolar (negative and positive voltages to provoke set and reset processes respectively) and negative unipolar (negative voltages to provoke both set and reset processes) conditions. The voltages have been applied by the semiconductor parameter analyzer Keithley 4200SCS.

2.2.1. Device operation under bipolar RS

To observe bipolar resistive switching, a negative voltage ramp has been applied to gate terminal with the rest of the transistor terminals grounded in order to provoke set process. On the other hand, a positive voltage ramp has been applied to gate terminal while others grounded for reset process. In both cases, the gate current has been registered and analyzed. These voltages have been successively applied performing bipolar RS measurements in more than 50 samples. Mention that in all those RS measurements, a current limit of 500 µA has been chosen during set process to avoid a large degradation of the gate dielectric, supported by previous works in [105] where switching between two resistance states is observed in similar devices for current limits of this order of magnitude.

In Figure 2-2, some I_G-V_G characteristics for a 128-cycle measurement in the same transistor are depicted. From the figure, dispersion in the RS parameters (set and reset voltages and currents) are observed. To better observe voltage and current

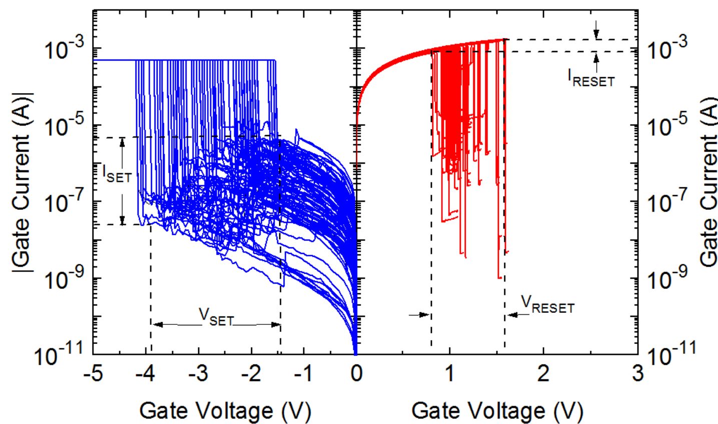


Figure 2-2: Typical I_G-V_G curves of bipolar Resistive Switching observed in the analyzed transistors.

variabilities, the cumulative distribution functions (CDFs) of the set and reset voltages and currents have been obtained. Figure 2-3(a) and (b) show the cumulative distribution functions of set and reset voltages and currents, respectively, for the previous 128 performed RS cycles. Figure 2-3(a) shows that set voltage (solid black circles) presents larger variability, with values varying in the range from -4 V to -2 V, than reset voltage (empty red circles), with a variation between 0.75 V and 1.5 V. On the other hand, in Figure 2-3(b), set current (solid black circles) exhibits a much larger variability (set currents are contained in 3 orders of magnitude) than that of reset (empty red circles) whose distribution is comprised in less than one order of magnitude.

The larger set parameters variability may be explained according to the physical RS mechanism occurring in the samples. According to [40], reset process seems to be governed by Joule heating phenomenon, which has a stochastic/random behavior. Therefore, the disruption of the conductive filament through the dielectric during reset process depends on how this Joule heating phenomenon has occurred. If reset process occurs abruptly, it will originate a filament largely disrupted what prevents a relevant current flowing through it. Consequently, a very high HRS resistance (greater than 1 GΩ) will be reached after the reset process. To switch the device to LRS state, a higher voltage will be necessary because of the higher HRS resistance achieved. Therefore, the stronger the reset process (the higher the HRS resistance reached) the larger the set voltage necessary to provoke the corresponding process. Because of HRS resistance reached after every reset process is significantly different, set voltages are also different provoking the large variability. Consequently, set current also shows a dependence on reset process, generally decreasing when resistance state reached after reset event increases. Overall, set parameters variability

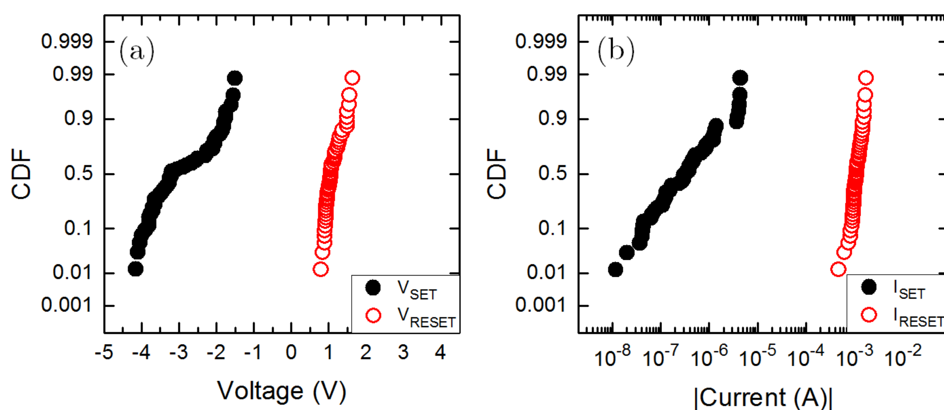


Figure 2-3: Cumulative distribution funcctions of (a) voltages and (b) currents of set (solid black circles) and reset (empty red circles) processes for a bipolar RS operation mode.

may be related to how abrupt the previous reset process was originated, i.e. the HRS resistance reached.

Dispersion of set and reset voltages are desired to be as low as possible in order to have a better control of the switching processes, but unfortunately, variability is always observed in those parameters.

2.2.2. Device operation under unipolar RS

For unipolar resistive switching, negative voltage ramps have been applied to the gate terminal with the rest of the transistor terminals grounded to provoke both set and reset processes. In this case, unipolar RS measurements have been performed on only 12 samples since their endurance hardly reached 20 cycles. The most endurable has been a measurement of 23 cycles, whose I_G-V_G characteristics are shown in Figure 2-4, until resistive switching cycling was not possible to be observed anymore due to large damage on dielectric stack. In addition, the current limit has been here reduced to 10 µA because RS phenomenon was barely observed at higher compliances.

As in bipolar case, cumulative distribution functions of the set and reset voltages and currents, shown in Figure 2-5(a) and (b) respectively, have been obtained for a better study of the parameters variability. Set parameters show larger variability than reset ones although the variability of later ones has increased in comparison to that in bipolar case. Set voltage (solid black circles) shows a very large variability of more than 2V-range (between -2.5 V to -4.75 V). On the contrary, reset voltage (empty red circles) is comprised in 1V-range (between -1 V and -2 V). Likewise, set current (solid black circles) shows a very large dispersion of almost two decades (minimum and maximum values at ~4x10^{-8} A and ~3x10^{-6} A, respectively). Unlike

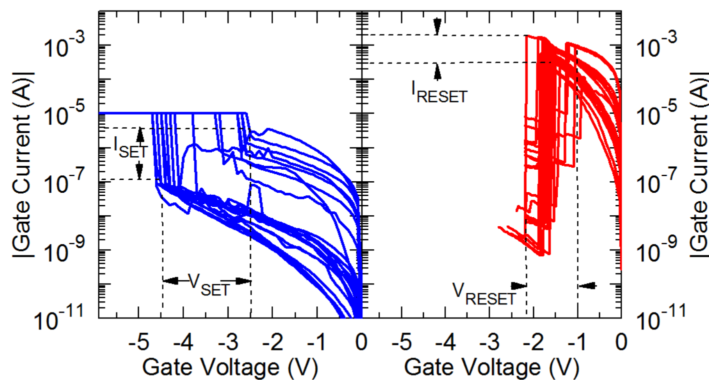


Figure 2-4: Typical I_G-V_G curves of unipolar Resistive Switching on the analyzed transistors.

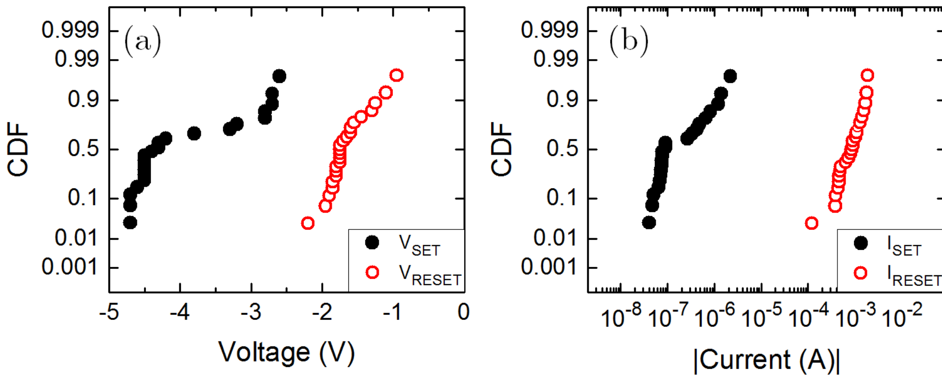


Figure 2-5: Cumulative distributions functions of (a) voltages and (b) currents of set (solid black circles) and reset (empty red circles) processes for a unipolar RS operation mode in the studied transistors.

the bipolar case, reset current (empty red circles) has a relevant variability showing a minimum value at around $4x10^{-4}$ A and a maximum value at $\sim 2x10^{-3}$ A, which indicate almost a decade of dispersion.

For a better comparison between the variability of the RS parameters observed for unipolar and bipolar operation modes, CDF parameters such as μ (mean of the normal distribution) and σ (standard deviation of normal distribution) for both modes are summarized in Table 2-I. Regarding voltages, although μ values in bipolar RS are smaller than in unipolar (a 1V-difference between set voltages), the dispersions are quite similar between RS modes. However, the variability is noticeably higher in set voltages than reset ones. As in bipolar case, the large set voltage variability might be due to different HRS resistance reached after every reset process. Similar behavior is observed in the currents, the μ values are even closer between bipolar and unipolar RS as well as the deviations for the set process. However, the reset current deviation is smaller in bipolar than in unipolar RS, what indicates less variability of such a current when bipolar RS.

Table 2-I: CDF parameters (μ and σ) for bipolar and unipolar RS parameters.

		BIPOLAR RS		UNIPOLAR RS	
		μ	σ	μ	σ
Voltage(V)	**Set**	-2.9	0.83	-3.9	0.79
	Reset	1.1	0.22	-1.65	0.28
Log(I) (A)	**Set**	-6.5	0.65	-6.8	0.55
	Reset	-3.0	0.11	-3.1	0.28

Overall, these samples show a large variability mainly on set parameters independently of the analyzed RS operation mode what indicates that it is more difficult to control at which voltage set process occurs. Despite the set variability disadvantage, bipolar RS has resulted as the most appropriate operation mode to observe large RS cycling since more measurement with large number of cycles have been possible to perform. Besides, reset current variability appears reduced at this operation mode. For these reasons, bipolar RS (with negative and positive voltages for set and reset processes, respectively) have been considered for all the subsequent measurements.

2.3. Filament location in MOSFET

As explained in chapter 1, RS phenomenon is associated to the generation of a conductive filament that can be (partially) disrupted or formed through the dielectric depending on the applied voltage to the device. In previous studies about dielectric breakdown (BD), the loss of the insulator properties is also associated to the creation of a conductive path through dielectric [106], [107]. The location of this breakdown path along the transistor dielectric length has been studied in transistors [108]–[110]. In [108] authors propose a method to determine the breakdown path location along the dielectric length of a transistor by means of measuring drain and source currents. The method allows determining the conductive path location calculating a parameter, labeled α, by the following equation [108]:

$$\alpha = \frac{I_D}{I_D + I_S} \quad \text{2-1}$$

where I_D and I_S are the drain and source currents respectively. They are extracted from the I_G-V_G characteristics after dielectric breakdown at a certain value of V_G within the accumulation region of the transistor [110]. Values of α close to 1 (>0.99) means that the breakdown path is mainly located near the drain region. On the contrary, when this value is close to 0 (<0.01) then the path location is near the source region. Values differing from these two numbers indicate breakdown path located along the transistor dielectric length.

Due to the similarities between the conductive localized path through the dielectric associated to the RS and BD phenomena, RS can be understood as a dielectric breakdown that can be reversible depending on the applied bias [105]. Therefore, the use of transistors instead of MIM/MIS structures allows obtaining the location of the conductive filament associated to RS by applying the previous method. The control of the filament location along the dielectric length has a lot of interest since it might allow individually creating different filaments in a controllable way. Hence, an

experiment to try to control the filament location along the length of transistor's dielectric stack has been performed and detailed in the following section.

2.3.1. Control of filament location

The experiment to control filament location has been carried out by using the setups sketched in Figure 2-6. The measurement procedure has consisted in performing a sequence of 15 cycles of set and reset events successively by applying voltages ramps according to bipolar RS mode (since in section 2.2.1 this operation mode shown the best endurance) with a current limit of 300 µA and following the sequence specified in Table 2-II to force filament location. In the table, D and S mean the expected location must be close to drain or source, respectively. For this purpose, the setup sketched in Figure 2-6(a) has been used. This setup shows the configuration to force the filament location near drain terminal. To do this, voltage ramps (from 0 V to -6 V to provoke set process and from 0 V to a positive voltage just after reset event occurs) are applied to the gate while the drain terminal is grounded and other terminals (source and bulk) are floating. With this bias configuration, a larger potential difference between grounded terminal (drain) and gate terminal than between floating terminal (source) and gate terminal is established. Consequently, the conductive filament is expected to be located near grounded (drain) terminal region. To locate filament close to source region, drain and source terminals must be exchanged; then, the source terminal must be now grounded and drain floating.

The RS I_G-V_G characteristic (set and reset process) registered for each performed cycle by using the setup in Figure 2-6(a) is plotted in Figure 2-7 just to show that the resistive switching phenomenon has been performed and the processes has been

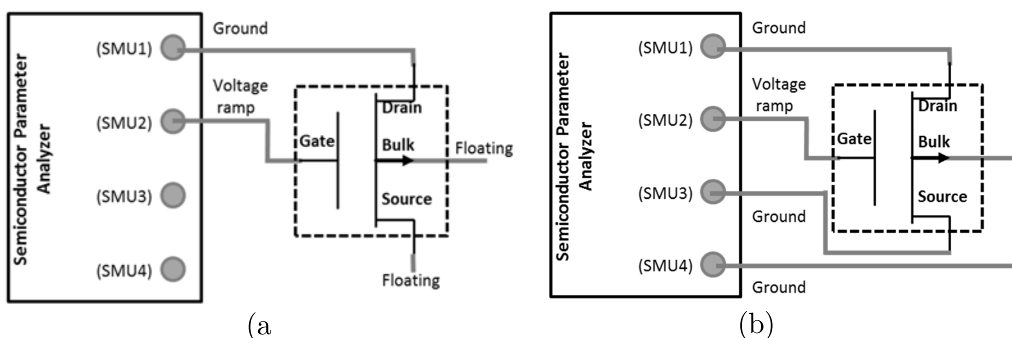


Figure 2-6: Schematic setup to study the location of the conductive filament (a) when filament location is desired to be controlled close to either drain or source (in this case configuration for filament location near drain is shown) and (b) without concontrolling filament location.

Table 2-II. Predefined definition of the conductive filament location with cycling. Forced filament location indicates where filament has been intended to be forced.

Cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Forced filament location	D	S	S	D	D	D	S	S	S	D	D	D	D	D	S

provoked, disrupting and re-creating a filament. As in previous analysis, a large variability of set and reset voltages and currents is observed. Note in this case that the current at LRS shows different behaviors (indicated in Figure 2-7) what might be associated to a size modification of the unique existing filament with cycling or to the creation of new different filaments contributing to the current or substituting the previous one [2], [8]-[10].

To verify if the location of the conductive filament is the expected, the α-parameter method explained at the beginning of the section 2.3 was applied. To do it, after each set and reset process, I_G-V_G transistor characteristics have been obtained using the setup schematized in Figure 2-6(b). A low voltage ramp, from 0.8 V to -0.8 V, to avoid extra degradation on dielectric layer or provoking a subsequent event is applied to the gate terminal while the rest of the terminals are grounded, registering the current through all the four terminals. This configuration is the typical used when filament location is not forced. This potential difference between gate and source terminals and between gate and drain terminals are almost equal what would originate a filament randomly located.

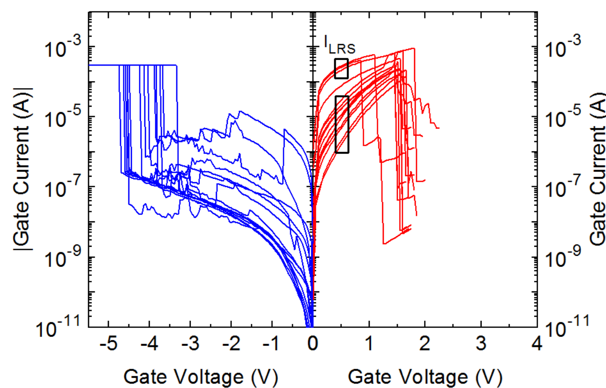


Figure 2-7: RS I_G-V_G characteristics of 15 performed cycles in which location of the filament has been forced eithter close to drain or close to source regarding sequence in Table 2-II.

In Figure 2-8(a) and (b), the currents corresponding to the fifth RS cycle and registered after set and reset processes, respectively, are depicted as a function of gate voltage. After set process, drain current (dashed blue line) is completely overlapping gate current (solid black squares) and they are larger than source current (solid red line) which indicates a filament located close to drain. On the contrary, after reset process, filament location is not so clear since the gate current is very low because the conductive filament is partially, or completely, disrupted. On the other hand, drain (dashed blue line) and source (solid red line) currents are small and comparable among them indicating that the currents through both terminals are nearly similar and, therefore, there is not filament current contribution close to any of the regions. Here, gate current is mainly due to current through the whole dielectric itself, being the filament current contribution less relevant.

To corroborate the location of the filament, α-parameters have been calculated, at V_G = +0.8 V, from I_G-V_G transistor characteristics measured after set and reset processes (at LRS and HRS states, respectively). The α-parameter values at LRS are depicted along the cycling in Figure 2-9(a). For the first cycles, filament location follows the predefined location in Table 2-II since α-parameter values correspond to filament location close to drain (α~1) or source (α~0). However, after cycle number 6 filament placement has started to be undefined since the α-parameter values differ from 1 (close to drain) or 0 (close to source) so the control of filament location has not been possible anymore. Values of the α-parameter differing from 1 or 0 would suggest that the filament is placed along the dielectric length or the generation of more conductive filaments along the dielectric what would add more current contributions.

In addition, in Figure 2-9(b) α-parameter values calculated at HRS are also depicted

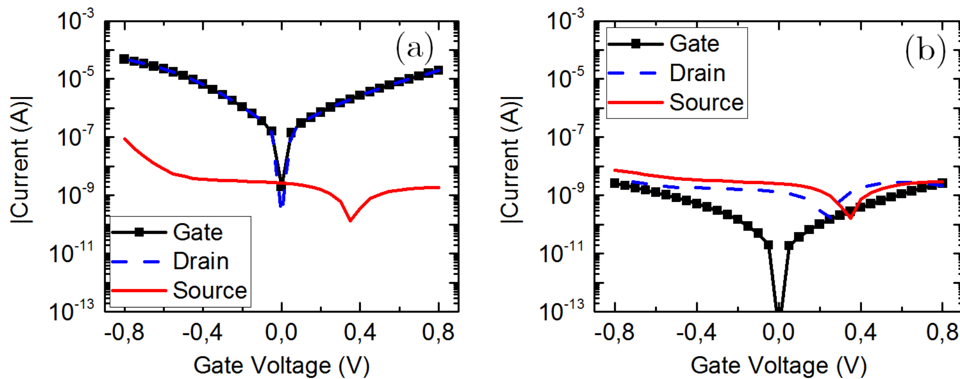


Figure 2-8: Gate, Drain and Source currents after (a) set process and (b) reset process both as a function of gate voltage to obtain filament location by means of α-parameter.

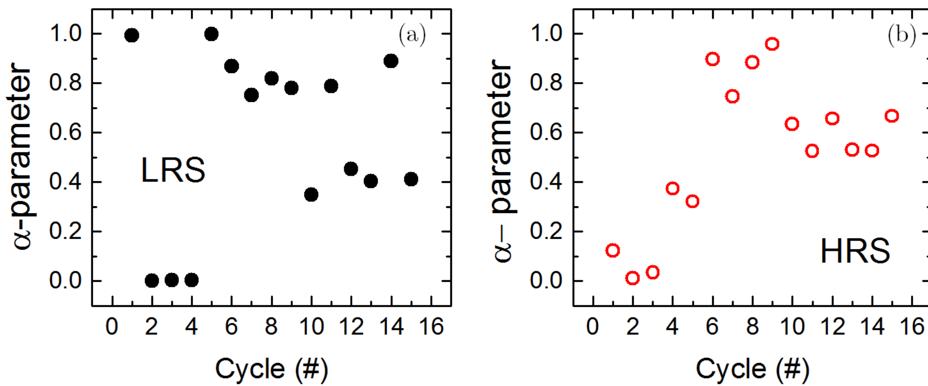


Figure 2-9: α-parameter calculated at V_G=0.8 V when device is at (a) LRS and (b) HRS for each RS cycle.

along cycling. In this case, location of the conductive filament is not so clear and barely matches the predefined filament location of Table 2-II. In this situation, the filament is disrupted and no relevant current flows through it. Consequently, most of the conduction is due to tunnel current flowing through the whole dielectric.

The previous explained measurement has been carried out on different devices changing the filament forced location sequence but in all the experiments, it has been very difficult to control the filament's placement along dielectric layer.

2.4. Method to discriminate gate current contributions

When resistive samples are at LRS, the conduction through the dielectric is mostly due to the current flowing through a conductive filament created during set process and whose position along dielectric length can be easily determinable by using α-parameter method, as previously shown. On the contrary, after reset process, the filament is partially or completely disrupted provoking a decrease of the current through the filament. This current is so reduced that can reach levels of the same order as the current that flows through the whole dielectric area (from now on known as non-localized current) due to other possible conduction mechanisms. Thus, it may be difficult to distinguish between the CF conduction and the non-localized current contribution. These currents are illustrated in Figure 2-10 where a RS transistor at LRS state with a filament located close to the source (blue) is sketch. The current flowing through this filament (I_{CF}), indicated with a blue arrow, and the flow of a non-localized current through the dielectric (I_{NLC}), represented with red arrows, are the mentioned two components of the gate current (I_G).

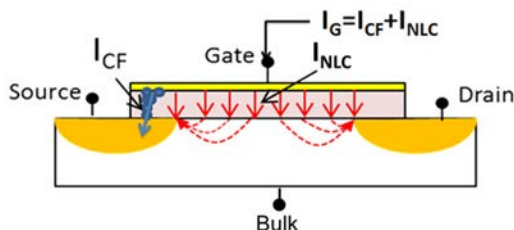


Figure 2-10: Schematic of dielectric conduction in a MOSFET with a CF located close to the source terminal. Localized current through the filament I_{CF} (blue), and non-localized current due to the whole area conduction I_{NLC} (red).

In this section, a new method to separate the localized current through the conductive filament from the non-localized gate area current for the low conductivity state (HRS) will be proposed. Actually, two similar methods are proposed depending on filament location is near source or drain. These methods allow analyzing the role of the non-localized current conduction across the whole dielectric area as well as its relevance in comparison to the current that flows through the local CF.

2.4.1. Experimental Procedure

To analyze the different dielectric current contributions at HRS, samples have been subjected to a repetitive measurement sequence whose scheme is shown in Figure 2-11. First, the fresh transistor characteristics (I_D-V_G, I_D-V_D, I_G-V_G) have been registered in order to characterize the transistor. To continue, successive set and reset processes have been performed under bipolar conditions (negative and positive voltages to provoke set and reset processes, respectively) with a current limit of 500 μA. Then, a voltage ramp limited in current has been applied to the gate terminal with the rest of terminals grounded to provoke the set process. Subsequently, another voltage ramp without current limit has been applied to perform reset process. After both set and reset processes, transistor characteristics of the sample have also been registered, thus, post-set and post-reset transistor

Figure 2-11: Stress-measurement sequence designed to analyze the the gate current contribution at HRS in MOSFETs.

characteristics have been obtained. From the whole transistor characteristics after both processes, especially the I_G-V_G, it is possible to evaluate the transistor damage and calculate α-parameter from which not only filament's location can be determined but also the gate current contributions. This sequence has been repeated as many RS cycles as possible, finishing when the RS performance has not been correctly observed or until reaching the maximum number of sequentially cycles allowed in the same measurement by the semiconductor characterization system Keithley 4200SCS, which is 128.

Previously described experiment has been performed in more than 20 samples until finding the filament location close to drain or source along cycling.

2.4.2. Methods to separate gate current components based on filament location.

2.4.2.1. Filament located close to the source

As an example of the first method, a measurement of 128 RS cycles where filament location was located near source has been used. In Figure 2-12(a) I_G-V_G characteristic after reaching the LRS, where gate current is mainly controlled by the filament current (I_{CF}), are shown. Drain (dashed blue curves) and source (solid red curves) currents have been included in the figure as well. As can be noted, the majority of the source curves overlaps the gate current curves (solid black squares) what indicates filament is likely located close to the source. This has been corroborated by calculating α-parameter from the I-V curves of Figure 2-12(a), at V_G = 0.8 V, (Figure 2-12(b)). The α-parameter values are very close to 0 indicating that the filament is indeed located near the source [108] for the all RS cycles.

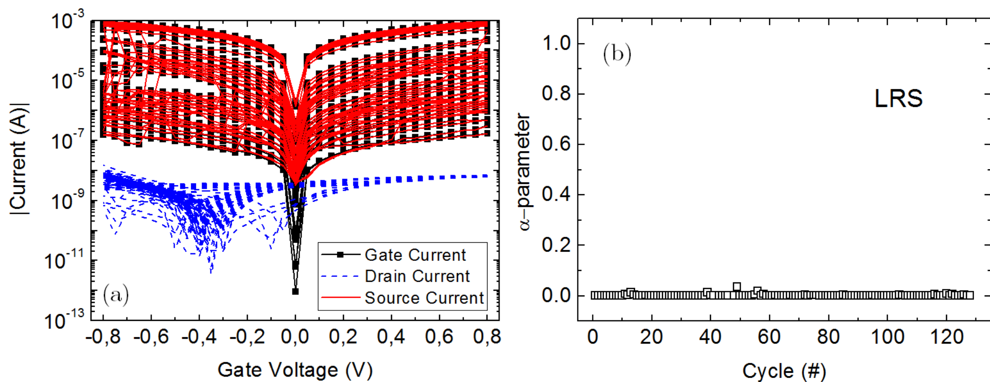


Figure 2-12: (a) Typical I_G-V_G characteristics after set process. (b) Experimental α-parameter during cycling at LRS when CF is located close to the source (α ~ 0).

After reaching HRS state, α-parameter has been also obtained for every cycle [105], at $V_G = 0.8$ V, and its values are depicted in Figure 2-13 (a) as a function of I_G to observe the relation between both parameters. For larger I_G values, α-parameter is very close to 0. However, lower I_G values correspond to α-parameter values closer to 0.5. When the filament conduction is relevant (larger I_G values), I_{CF} dominates and I_{NLC} becomes negligible, which explains values of α-parameter close to 0 for the HRS. However, for lower values of I_G, filament current flow can be considered completely disrupted and I_{NLC} becomes more relevant. As I_{NLC} is distributed through the whole transistor area, the portion of this current that is collected at the drain and source terminals tends to be the same, which explains the shift of α-parameter towards values larger than 0 (Figure 2-13 (a)). These data have been fitted to get the behavior of α-parameter with gate current (I_G). In Figure 2-13(a) the resulted fitting curve (blue line), which is described by equation 2-2, has been also plotted.

$$\alpha = \frac{0.5 \cdot I_{NLC}}{I_G} \qquad \text{2-2}$$

In this formula, I_{NLC} is a fixed parameter that has been obtained by least squares. To do this, calculated α-parameter is depicted versus the inverse of I_G as shown in Figure 2-14. Then, plotted data are linearly fitted (red line) by means of a linear regression whose slope is compared with the term 0.5 I_{NLC} to extract the fixed parameter I_{NLC}.

Coming back to Figure 2-13, α-parameter data are perfectly fitted by the curve governed by equation 2-2. Considering that gate current can be separated into two components, $I_G=I_{CF}+I_{NLC}$, then equation 2-2 can be rewritten as:

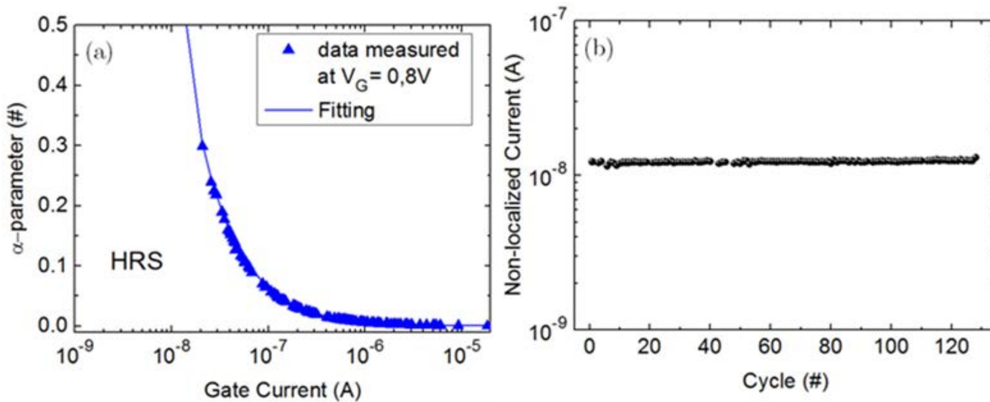


Figure 2-13: (a) Experimental α-parameter at HRS for the different cycles as a function of I_G (symbols). Fitting curve obtained from equation 2-2 (blue line). (b) I_{NLC} as a function of the number of RS cycles.

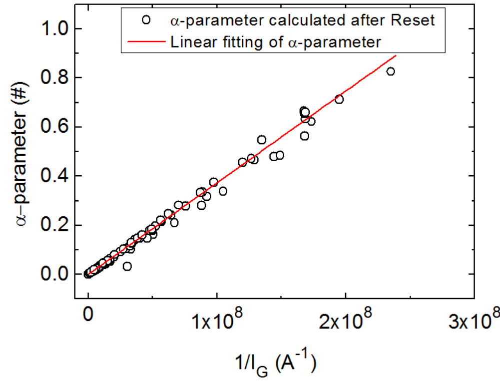


Figure 2-14: α-parameter as a funciton of the inverse of I_G and the fitting of those data which allows calculating the I_{NLC} parameter in equation 2-2.

$$\alpha = \frac{0.5 \cdot I_{NLC}}{I_{CF} + I_{NLC}} \qquad 2\text{-}3$$

From equations 2-2 and 2-3, I_{NLC} and I_{CF} can be extracted separately as a function of I_G by equations 2-4 and 2-5 consequently obtaining with more accuracy I_{CF} for the HRS.

$$I_{NLC} = \frac{\alpha \cdot I_G}{0.5} \qquad 2\text{-}4$$

$$I_{CF} = \frac{0.5 - \alpha}{\alpha} \cdot I_{NLC} = \frac{0.5 - \alpha}{0.5} \cdot I_G \qquad 2\text{-}5$$

From equations 2-4 and 2-5, it is possible to get the non-localized and conductive filament currents, respectively, for every RS cycle. In Figure 2-13(b) calculated I_{NLC} is plotted as a function of RS cycle number to study its behavior along cycling. I_{NLC} has been observed to be almost constant indicating that non-localized degradation is less relevant along cycling. The re-creation and disruption of the conductive filament mainly governs the gate current value.

So far, a method to separate filament and non-localized dielectric current contributions when filament is located close to source along cycling has been proposed. Furthermore, an analysis of the influence of the V_G value chosen to calculate α-parameter on the discrimination of I_{CF} and I_{NLC} has been also performed. To do that, I_{CF} and I_{NLC} have been obtained at different gate voltages (ranged between 0.1 V and 0.8 V) by using the previous method. Figure 2-15 shows the behavior of the total gate current (I_G, black triangles), filament current (I_{CF}, red circles) and non-localized current (I_{NLC}, orange squares) as a function of V_G for a certain cycle of the RS measurement. In the figure, I_{NLC} becomes more relevant, at

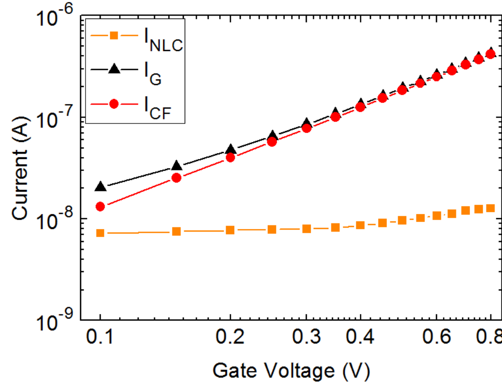


Figure 2-15: Dependenceon V_G of experimental I_G (Black triangles) and extracted I_{CF} (Red Circles) and I_{NLC} (Orange squares) by using equation 2-3.

lower V_G values, reaching similar values than I_{CF}. Contrarily, when V_G increases, I_{CF} becomes more relevant than I_{NLC}. Therefore, at $V_G = 0.8$ V filament and non-localized currents are clearly distinguished.

2.4.2.2. Filament located close to Drain

To illustrate the method to obtain separately I_{CF} and I_{NLC} when the filament is located close to drain, a measurement of 90 RS cycles has been used. The I_G-V_G transistor characteristics during LRS have been also obtained and are displayed in Figure 2-16(a) where drain and source currents have been also included. As it can be observed, most of the drain curves (dashed blue lines) completely overlaps gate curves (solid black squares) indicating in this case the existence of a conductive filament near the drain. Following with the analysis, α-parameter has been calculated when the sample is at LRS along the cycles (Figure 2-16(b)) which has corroborated that the filament is located near the drain (α-parameter close to 1). Unlike previous method, where filament has been located near source, a change on α-parameter trend was observed. Looking at Figure 2-16(b), α-parameter value is practically equal to 1 for several tens of cycles. However, at cycle 45 its value slightly changes from 1 indicating that something has happened in either filament location or dielectric stack conduction.

After knowing the filament is clearly located close to drain, at least for the first 45 cycles, α-parameter has been obtained after the reset event along the cycling and it is represented as a function of I_G in Figure 2-17(a). Not all α-parameter values have followed the same trend. There is a slight shift between the first cycles (From cycle 1 to 45, black squares) and last cycles (from cycle 46 up to the last one, red circles). In general, both groups of cycles have presented the same behavior: for the larger I_G, α-parameter at HRS is close to 1 and for lower I_G, α-parameter tends to 0.5. This

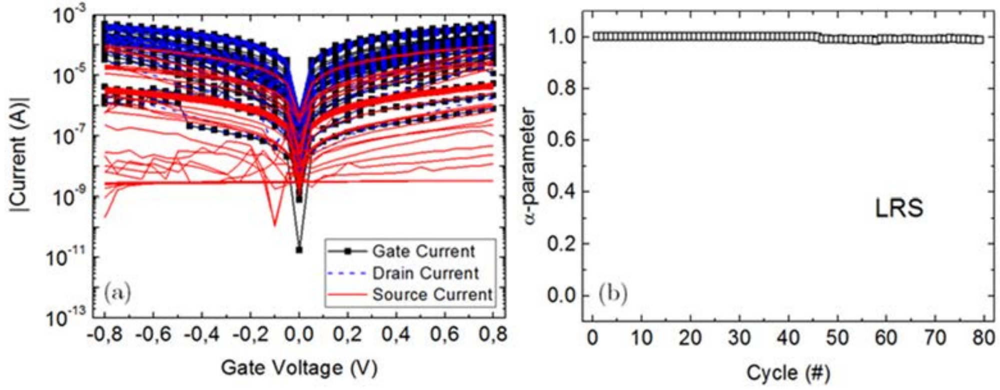


Figure 2-16: (a) Typical I_G-V_G characteristics after set process. (b) Experimental α-parameter during cycling at LRS when CF is located close to drain (α ~ 1).

behavior is still in agreement with the values of α–parameter obtained at LRS. Considering again I_G formed by two components, I_{CF} and I_{NLC}, at larger I_G values, I_{CF} is more relevant and I_{NLC} is negligible resulting in α-parameter values near 1. However, at lower I_G values, I_{CF} is so low that I_{NLC} becomes the relevant component. As I_{NLC} is a non-localized current, it has been collected in the same proportion by the drain and source, which explains α-parameter values closer to 0.5 when I_G decreases. In this situation, the formula to fit both groups of experimental data in Figure 2-17(a) is given by equation 2-6 following the expression:

$$\alpha = \frac{I_G - 0.5 \cdot I_{NLC}}{I_G} \qquad 2\text{-}6$$

I_{NLC} is the fixed parameter obtained by least squares as in the section 2.4.2.1. Since there are two behaviors of α-parameter as a function of I_G with cycling, now there are two fixed I_{NLC} parameters, one for the first 45 cycles and the other one for the rest of the cycles. In Figure 2-17(a), the fitting curves for each group of cycles are also graphed. Considering I_G=I_{CF}+I_{NLC}, equation 2-6 can be rewritten as:

$$\alpha = \frac{I_{CF} + 0.5 \cdot I_{NLC}}{I_{CF} + I_{NLC}} \qquad 2\text{-}7$$

Therefore, by solving equations 2-6 and 2-7, the filament and non-localized current contributions from the total gate current, during the HRS, can be obtained from equations 2-8 and 2-9:

$$I_{NLC} = \frac{1 - \alpha}{0.5} \cdot I_G \qquad 2\text{-}8$$

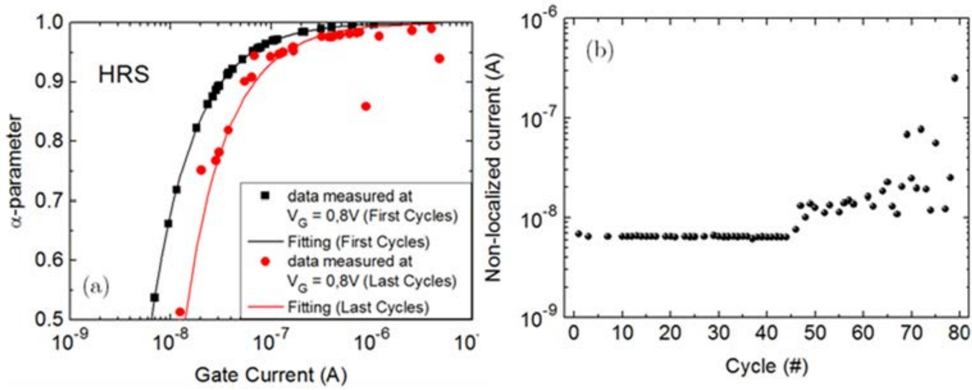


Figure 2-17: (a) Experimental α-parameter at HRS for the different cycles as a function of I_G (symbols). Fitting curves obtained from equation 2-7 (black and red lines). (b) I_{NLC} as a function of the number of RS cycles.

$$I_{CF} = \frac{0.5-\alpha}{\alpha-1} \cdot I_{NLC} = \frac{\alpha-0.5}{0.5} \cdot I_G \qquad 2\text{-}9$$

To demonstrate the increase of the non-localized dielectric degradation along the cycling, I_{NLC} is depicted in Figure 2-17(b) as a function of cycling. I_{NLC} is practically constant up to cycle 45 but from this cycle onwards, this current increases. This behavior indicates that the current through the whole dielectric area increases what could be due to an increase of the degradation of the dielectric area.

Finally, apart from the developed method, the influence on I_G, I_{CF} and I_{NLC} of the V_G at which α-parameter is calculated has been also analyzed. In Figure 2-18, where these currents are depicted as a function of V_G, it can be observed that at larger V_G, I_{CF} is predominant, whereas for lower V_G the I_{NLC} contribution increases and becomes

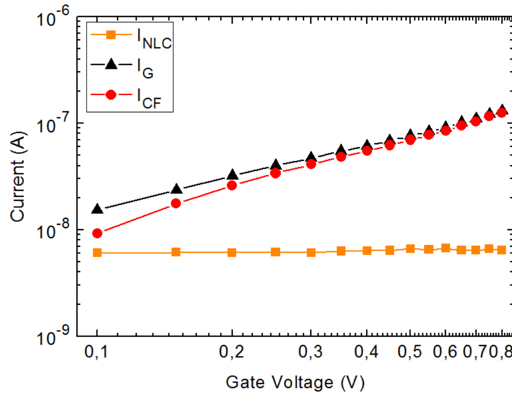


Figure 2-18: Dependence of experimental I_G and extracted I_{CF} and I_{NLC} (using 2-8 and 2-9 equations respectively) on V_G.

more relevant, reaching similar values than I_{CF}. Although developed methods are slightly different, the behavior of I_{CF} and I_{NLC} with V_G has been found to be independent on filament location.

2.5. Conclusions

Firstly, from the characterization of resistive switching phenomenon in transistors with a dielectric layer of HfSiON and a Ni-rich fully silicide gate electrode, bipolar voltage polarity (bipolar RS) conditions have been demonstrated to be the best polarity combination to perform large RS cycling in comparison with the negative unipolar voltage polarity (unipolar RS) conditions. Moreover, a large variability on set parameters has been observed independently of polarity conditions what makes more difficult to control when set process is going to be performed.

Then, it has been observed that forcing the location of the conducive filament close to drain or source is not controllable for this kind of transistors. The placement of the filament has been controlled for a very few initial cycles, but, after some cycles, location is not controllable anymore. In both cases, when device is at LRS and HRS, this might occur because the conductive filament is placed along the dielectric length or the appearance of more filaments as cycling increasing, making difficult to distinguish where every filament is located. Furthermore, when the device is at HRS, the control of the conductive filament location becomes more difficult from the beginning likely due to the conductive filament is not completely formed and, therefore, the conduction is due to tunnel current flowing through the whole dielectric area.

Finally, a new method to separate the localized current through the conductive filament (I_{CF}) from the non-localized gate current due to the whole dielectric degradation (I_{NLC}) when the dielectric is at the HRS has been proposed. The method has been based on the determination of the conductive filament location along the transistor channel by means of α-parameter when at HRS. Actually, the method must be adapted taking into account if filament is located close to drain or source.

3. Analysis of Resistive switching in memristors

RS phenomenon has been studied in MOSFET transistors in the last chapter. However, transistors are typically larger than memristors and their use in memory implementation might be an issue since for memory applications, the larger the information stored in less space, the better. According to this, memristors have gain more interest instead of transistors especially for memory applications. Nevertheless, the memristors functionality as well as the possible reliability problems such as the RTN current fluctuations [59], [114]–[117], as shown in chapter 1, should be completely understood and controlled. Up to date, these two goals have not been entirely achieved yet.

In this chapter, studies about the previous topics performed in memristors are presented. On the one hand, since fast switching is required to memristors to be implemented commercially, a study of RS processes under fast bias conditions is included. In particular, a study of the voltage ramp speed effect on RS parameters, such as the voltages and the energies required to provoke set and reset events, is introduced. On the other hand, a new RTN characterization method, which combines the improvement of the time resolution in comparison with that provided by standard SPAs with the W-TL method explained in chapter 1, is proposed. The method allows measuring RTN current events, not possible to register when a lower time resolution equipment is used. The procedure allows obtaining a more complete RTN characterization in comparison to standard techniques.

3.1. Memristors samples and measurement setup description

Memristors used in the experiments shown in this chapter have been supplied by the Institute of Microelectronics of Barcelona within Microelectronics National Center (IMB-CNM) from Barcelona, Spain. The fabrication process is detailed as follows. A schematic cross-section of the final device structure is depicted in Figure 3-1. Memristors are Ni/HfO_2/Si structures which were fabricated on (100) n-type Czochralski (CZ) silicon wafers with resistivity between 0.007 Ωcm and 0.013 Ωcm [45]. After standard wafer cleaning, a wet thermal oxidation process was done at 1100 °C leading to a 200 nm-thick SiO_2 layer. This field oxide was patterned by photolithography and wet etching. Prior to the high-k deposition, a cleaning in H_2O_2/H_2SO_4 and a dip in HF (5%) were performed. Subsequently, a 20 nm-thick HfO_2 layer was grown by atomic layer deposition (ALD) using tetrakis(dimethylamido)-hafnium (TDMAH) and H_2O as precursors, and N_2 as carrier and purge gas. The deposition temperature was 225 °C. The top metal electrode, consisting of a 200 nm-thick Ni layer, was deposited by magnetron sputtering. The resulting structures are square cells of 5x5 μm^2.

In Figure 3-2, an example of a typical IV-curve cycling of such samples is presented. HRS and LRS states as well as set process, i.e. the transition from HRS to LRS (blue curves) and the reset process, i.e. the change from LRS to HRS (red curves) are indicated. Although these samples have shown both unipolar and bipolar resistive switching [118], unipolar RS has been considered because that polarity combination results in the best performance of the samples [45], [119].

The results presented in this chapter have been carried out thanks to an experimental setup, developed in the REDEC research group of the UAB [120], that mainly allows registering current events with more time resolution (up to ns range using adequate circuit components) than standard semiconductor parameter analyzers; SPA, (with a typical time resolution within ms range). Furthermore, for the analysis of the RS phenomenon, the setup allows applying and tuning the current limit necessary during

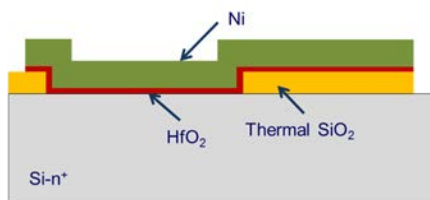


Figure 3-1: Cross-section of memristors, where the different materials are indicated.

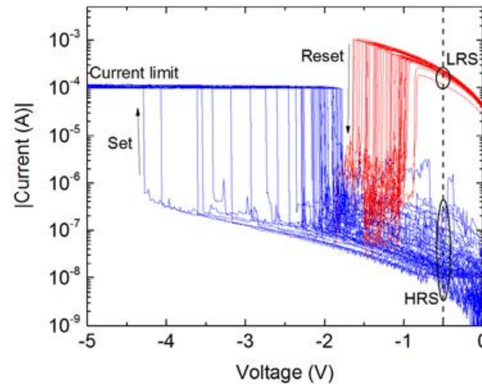


Figure 3-2: Typical RS IV-curves after succesive cycling of the samples previously described.

the set process in a wide range of currents, from 100 nA to 10 mA.

The setup mainly consists in three different parts depicted in Figure 3-3. The first part (block 1) is formed by an instrument capable of applying voltage bias that is connected to the top terminal of the memristor. A high impedance buffer, connected to the bottom terminal of the memristor, is also included to measure the voltage at this terminal allowing to know the actual voltage drop across the memristor. Afterward, to measure the current through the memristor, the bottom terminal is connected to the second stage of the setup (Block 2). This stage is formed by an in-house designed circuit that converts logarithmically the current from the memristor (I_{INPUT}) into voltage (V_{OUT}) by means of the Log-IVC module shown in Figure 3-3. Furthermore, it permits applying and selecting a specific current limit by the CLCU module shown in Figure 3-3. Finally, the output of the circuit is connected to an oscilloscope that constitutes the last stage of the setup (Block 3). Additionally, the output of the bias instrument can be connected to other channel of the oscilloscope to be registered as a function of time and with the same resolution that the output of the second stage of the setup. The use of the oscilloscope Tektronix

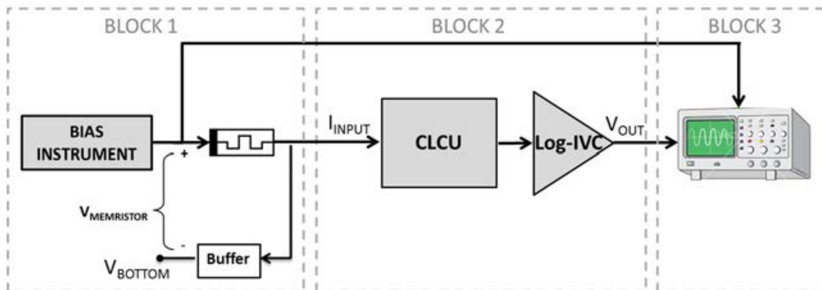


Figure 3-3: Block diagram of the setup. The CLCU will only be required when a current-limiting transistor is not integrated in the memory cell.

TDS 220 has allowed increasing the measurement time resolution due to its large sampling rate (1 GS/s) compared to the approximately 200 Samples/s of the SPA Agilent 4156C utilized in previous RS measurements [121].

Figure 3-4 shows a photograph of the circuit conforming the block 2 where all the components are visible. Regarding connectors, the one labeled as +/- corresponds to ±15 V supply voltage; V_{OUT} is the output of the circuit that is connected to the oscilloscope; V_{BOTTOM} is the connection between the bottom terminal of the memristors and the circuit; finally, V_C is an input voltage that allows stablishing the current limit, if necessary.

In more detail, the designed circuit of the second stage of the setup consists of two main modules. The first one is in charge of applying the current limit that must be applied to control the set process. This module is named Current Limit Control Unit (CLCU) and its operation is based on a MOSFET transistor working in the saturation region [120]. Therefore, different current limits can be switched by varying the transistor gate voltage. This module could be disabled if required, for instance, when the current limit is applied by others methods (by an on-chip select transistor fabricated in series with the device [122]) or during RTN measurements when a current limit is not needed since the large current values that can damage the device will not be reached. The second module is a logarithmic current–voltage converter (Log-IVC), which allows measuring current events when connected to an oscilloscope. The logarithmic conversion also permits to register the current in a six-orders-of-magnitude window, from nA to mA, without losing relevant information in the low current range as would be the case if linear conversion was used.

The converted memristor current measured as voltage by the oscilloscope at different time resolutions, must be converted from that registered voltage to actual current. To do that, the calibration curve of the circuit, shown in Figure 3-5 as the solid black

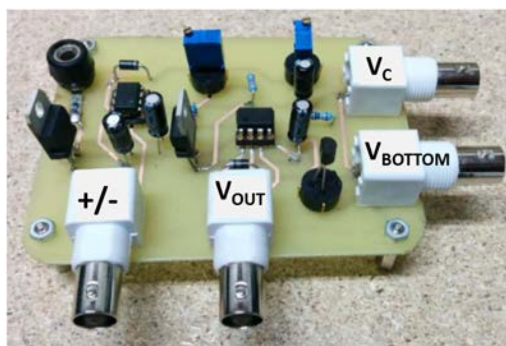


Figure 3-4: Picture of the circuit conforming block 2 to characterize the RS phenomenon.

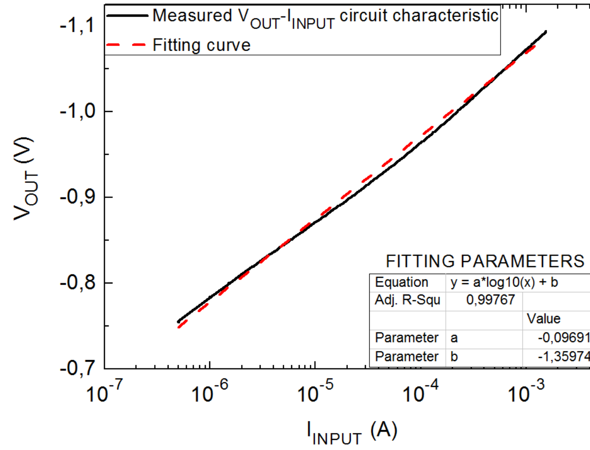


Figure 3-5: Circuit calibration curve where output voltage of the circuit (V_{OUT}) is measured for different currents applied to the circuit (I_{INPUT}).

line, has to be fitted by the mathematical equation (3-1) that relates logarithmically current and voltage and whose parameters *a* and *b* are obtained from the V_{OUT}-I_{INPUT} calibration curve of the circuit.

$$V = a\log(I) + b \tag{3-1}$$

Though the oscilloscope can allow higher time resolutions, there would be a limitation in the acquisition time coming from the bandwidth of Log-IVC designed circuit.

The applicability of the setup is quite broad. It can be used to register the current through a two-terminal device in a wide range and with more precision than, for instance, a SPA. In this thesis, the proposed setup has been used for two purposes: the first one, to measure the abrupt change in the current during set and reset processes in the previously explained memristors in order to analyze RS parameters when faster voltage ramps are applied. The second one, to measure and analyze RTN signals with a higher resolution than with standard equipment.

3.2. Analysis of set and reset mechanisms under fast voltage ramps

As commented in the introduction, the operation of memristors under fast conditions is a requisite for commercial purposes. Therefore, the dependence of RS phenomenon performance on the fast bias conditions is necessary to be studied. In particular, in this section, the influence on the RS set/reset parameters of the rise voltage ramp of a square pulse is analyzed. Specifically, the dependences of set and reset voltages and the energies associated to both processes on the voltage ramp speed are studied.

3.2.1. Experimental setup

Figure 3-6 shows the schematics of the complete used setup for RS measurements under fast bias condition where both the applied voltage ramp and the current through the memristor can be registered. The bias instrument is a pulse generator Agilent 81101A that has allowed the application of a much larger voltage ramp speed (VRS) range than the one provided by a SPA, which barely offers a voltage ramp speed of approximately 0.2 V/s [123]. The pulse amplitudes have been a fix value of -8 V to provoke the set process while for reset process a variable value ranged from -3.5 V to -6 V has been configured to provoke the process. Latter amplitude has been gradually increase to avoid an irreversible set process in the memristor that makes it not suffering RS cycling anymore. The rise time of a generated pulse (Figure 3-7) has been ranged from 7 ms to 100 ms. Lower values of the rise time range was not used because of the sampling rate limitation of the design Log-IVC circuit. The ramp speeds are calculated dividing the configured amplitude by the rise time of the pulse. As an example, a VRS of ~1143 V/s is obtained dividing the absolute value of the pulse amplitude -8 V by a rise time of 7 ms. Combining both ranges of amplitudes and rise times, a voltage ramp speed range from 35 V/s up to 1143 V/s has been achieved.

Voltage ramps with different speeds have been applied to the top terminal of the memristor by the pulse generator. Since memristors described in section 3.1 need an external system to control the current through them during set process, the CLCU module connected to the bottom terminal of the memristor has been enabled during this process and tuned to apply a current limit of 80 μA. During reset process, this module has been switched off to not to apply any current limit because a limitation in the current is not needed. Then, current through the memristor has been logarithmically converted to voltage by Log-IVC module connected subsequent the

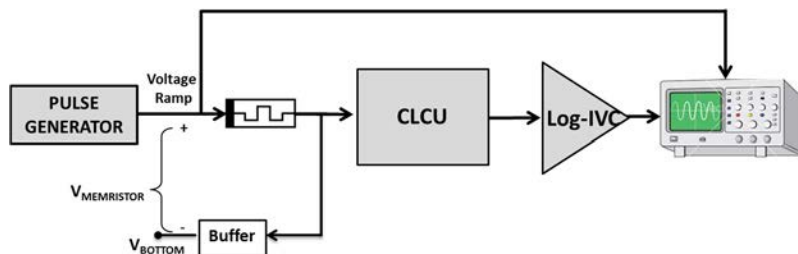


Figure 3-6: Schematics of the experimental setup developed to perform RS measurements under dynamic conditions applied by a pulse generator. $V_{MEMRISTOR}$ is the voltage drop across the memristor measured thanks to the buffer. In this case, CLCU unit is included since memristor itself has not got an integrated current limiter transistor.

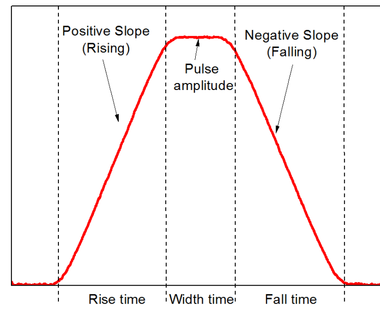


Figure 3-7: Sketch of a square pulse where different parts and times of the pulse are indicated.

CLCU. Finally, to measure set and reset processes, the output of the Log-IVC is connected to one of the channels of the oscilloscope (Tektronix TDS 220 with a bandwidth of 100 MHz and a maximum sample rate of 1 GS/s). The output of the pulse generator has been also connected to the other oscilloscope channel to register the generated voltage ramp. The experimental setup has been controlled using GPIB communication programmed with a specific MATLAB software script to register all data automatically.

An example of the oscilloscope capture of set and reset processes is shown in Figure 3-8 (a) and (b), respectively, where the red solid curves correspond to the converted currents of RS processes as a function of time and the dotted blue curves to the voltage pulses applied to provoke both processes. Note that only the first half of the pulse is shown since this is the pulse region of interest (rising region) because it is where set and reset processes occur. During the second half (falling region) no effects on the current have been observed. Simultaneous oscilloscope measurements

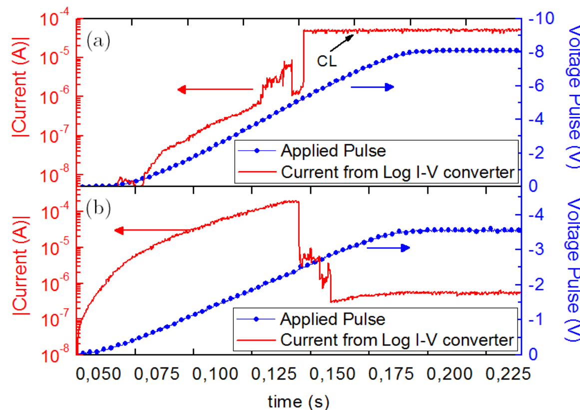


Figure 3-8: Applied voltage ramps and current registered during a set (a) and a reset (b) processes using the setup shown in Figure 3-6. The CLCU is configured to limit the current to ~80 μ A during set. In this case, a VRS of 80V/s for set and VRS of 35V/s for reset have been used.

of the applied voltage ramp and current events allow reconstructing the standard I-V characteristics of every RS cycle to obtain the RS parameters.

3.2.2. Measurement procedure

Measurement process for each memristor has consisted in, initially, an electroforming step applying a voltage ramp up to -10 V using a SPA Agilent 4156C. Then, around twenty RS cycles have been performed also using the SPA to get a stable RS cycling. After that, several set and reset processes have been sequentially induced on the same memristor at different voltage ramp speeds (Table 3-I) using the setup described in Figure 3-6. The current limit established during the set process in all the applied VRS was 80 µA. Beginning from the slowest VRS (rise time of 100 ms), the speed of the applied voltage ramp has been sequentially increased performing 5 consecutive cycles, comprising both set and reset processes, for each VRS. Up to seven different VRSs (corresponding to rise times from 100 ms to 7 ms) have been achieved for the same memristor. Note that the VRS is smaller during reset process than set process for every cycle performed with the pulse generator. This is because the pulse amplitude to provoke reset process has been always smaller than the pulse amplitude for the set process, while the rise time has been the same for both processes.

In Figure 3-9, reconstructed I-V characteristics of consecutive set and reset processes obtained from the previous measurement procedure are shown. Solid green squares correspond to the reconstructed I-V characteristics measured under the slowest VRS of 80 V/s for set process and 35 V/s for reset process. On the other hand, reconstructed I-V characteristic depicted with empty red triangles have been measured by applying the fastest VRS of 1143 V/s and 629 V/s for set and reset

Table 3-I. Voltage ramp speeds applied to the memristors and the corresponding predetermined amplitude and rise time of the pulse.

SET			**RESET**		
Amplitude (V)	Rise time (ms)	**VRS (V/s)**	Amplitude (V)	Rise time (ms)	**VRS (V/s)**
8	100	**80**	3.5	100	**35**
8	80	**100**	3.7	80	**46**
8	60	**133**	3.9	60	**65**
8	40	**200**	4.1	40	**103**
8	20	**400**	4.2	20	**210**
8	9	**888.9**	4.3	9	**478**
8	7	**1143**	4.4	7	**629**

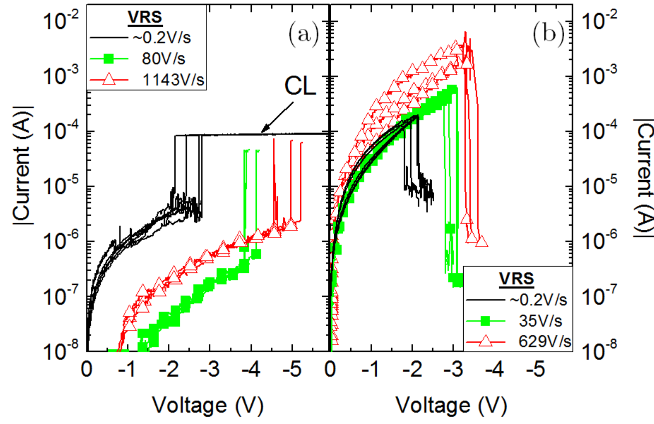


Figure 3-9: I-V characteristics for set (a) and reset (b) processes for different applied VRS. The x-axis shows the actual memristor voltage drop. Measurements with a typical SPA, which allows slower ramp speeds (~0.2 V/s) than those available with the developed setup, are included for comparison.

processes, respectively. I-V curves in solid black lines correspond to those measured initially by the SPA with an estimated voltage ramp speed of approximately 0.2 V/s. The inclusion of I-V curves from SPA measurements allows increasing the VRS range of study towards slower voltage ramp speeds. From that figure, it can be observed that the set and reset processes seem to occur at higher voltages when VRS increases. To continue, a thorough analysis of the RS parameters have been performed to study their behavior with VRS.

3.2.3. RS parameters analysis

A fast and accurate way to extract RS parameters has been possible thanks to the analysis scripts designed with MATLAB software which has allowed getting the voltage and current of the set and reset processes (V_{SET}, V_{RESET}, I_{SET} and I_{RESET}) as well as the current values at LRS and HRS states (I_{LRS} and I_{HRS}). Figure 3-10 shows the mean values of the extracted set and reset voltages plotted for the full range of studied VRS in the same memristor. Clearly, V_{SET} and V_{RESET} exponentially (x-axis is in logarithmic scale) increase with VRS, which seems to be consistent with similar experimental results showed in [124], [125] where the influence of the sweep rate (or voltage ramp speed as here defined) on set voltages is studied for MIM-structure memristors. To corroborate this agreement, both V_{SET} and V_{RESET} data have been fitted to the equation:

$$V_{SET} = a \cdot \ln(\mathrm{VRS}) + \mathrm{b} \tag{3-2}$$

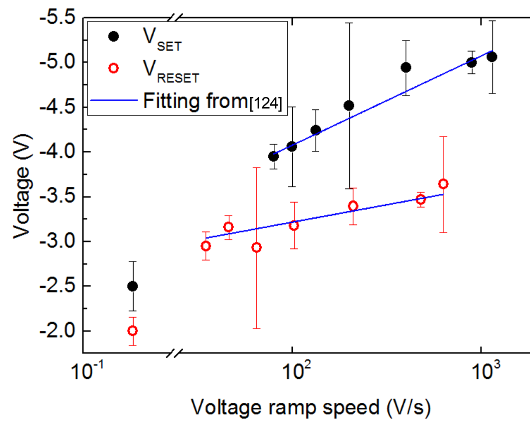


Figure 3-10: V_{SET} (solid black circles) and V_{RESET} (empty circles) as a function of VRS.

where *a* and *b* are fitting parameters. This equation has been derived from the logarithmic relation between V_{SET} and VRS proposed in [124] where, together with [126] and [127], authors postulate that the faster the voltage ramp, the higher the voltage required to form or dissolve the conductive filament through the dielectric. These results are also in agreement with those in [40], where the increase of reset voltage and current while VRS increases is related to the thermally driven CF dissolution kinetics.

The strong dependence of RS voltages on the VRS has suggested the existence of a critical energy required to trigger the corresponding set and reset processes. To corroborate this hypothesis, the energies required to provoke the set (ε_{SET}) and reset (ε_{RESET}) events, i.e. the energy necessary to reach the beginning of the processes, have been calculated. To do this, the voltage and current through the memristor have been registered as a function of time (as the traces shown in Figure 3-8). Then, the power consumed just until the RS processes occur has been calculated as the product of voltage by current. Finally, set and reset energies have been calculated integrating previous powers over the time.

Examples of the power evolution as a function of time during a whole RS cycle, calculated until the reset/set process begins, are represented in Figure 3-11. The set and reset powers/energies are those powers/energies consumed from the beginning of bias application until set and reset processes occur with the sample at HRS and LRS, respectively. In Figure 3-11, the reset power (empty red circles) is larger than the set power (solid black circles) which is consistent with the fact that at LRS more current is passing through the device compared to the current flowing at HRS.

In Figure 3-12, the mean values of set and reset energies calculated for the studied range of VRS are plotted as a function of the VRS. Energies tend to maintain almost constant when VRS increases so no dependence of the energies on VRS is observed.

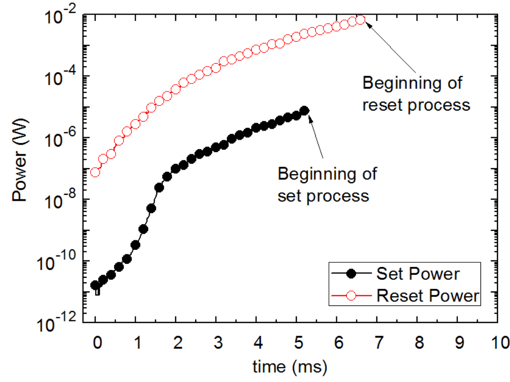


Figure 3-11: Example of reset power (empty red circles) and set power (solid black circles) for VRS=628.6V/s and VRS=1143V/s respectively. Reset power is greater than set power.

This result suggests that the energy supplied to the memristor controls the set and reset processes. On the one hand, ε_{SET} should be considered as the required energy to fully forms the filament [128]. On the other hand, ε_{RESET} should be interpreted as the energy required to heat, by joule effect, the CF locally until the critical temperature that triggers the filament disruption is reached [40]. The results in Figure 3-12 seem to indicate that ε_{SET} and ε_{RESET} are two critical parameters that determine the occurrence of the set or reset events, independently of the biasing conditions used to trigger them.

Finally, although the dependence of RS currents (I_{HRS} and I_{LRS}) on VRS has been also studied, no significant results have been observed for all the analyzed measurements. Figure 3-13 shows an example of the currents at HRS, I_{HRS}, (solid black circles) and at LRS, I_{LRS}, (empty red circles) for a VRS range comprising

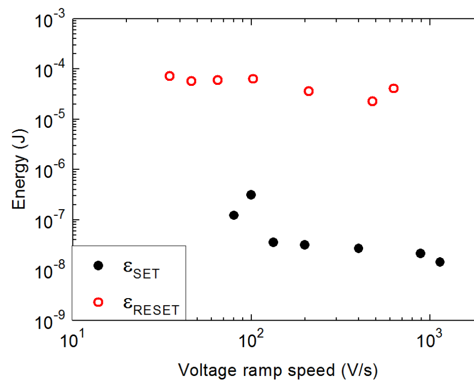


Figure 3-12: Energy required to trigger set and reset processes as a function of VRS. Both energies remain constant with VRS indicating that ε_{SET} and ε_{RESET} are critical parameters to provoke the RS phenomenon.

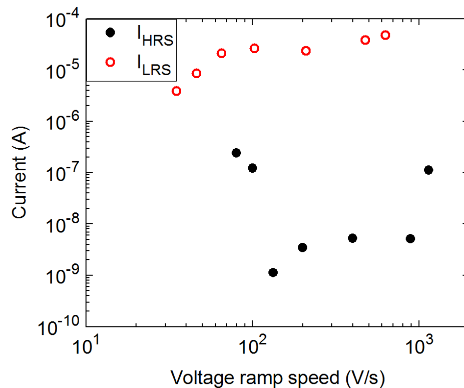


Figure 3-13: I_{HRS} and I_{LRS} extracted at -0.5 V from the reconstructed I-V curves considering the VRS range from 80 V/s to 1143 V/s for set (where I_{HRS} was extracted) and from 35 V/s to 629 V/s for reset (where I_{LRS} was extracted).

between 80 V/s and 1143 V/s for set process and between 35 V/s and 629 V/s for reset. While I_{HRS} clearly shows random values as VRS increases, I_{LRS} seems to have a slightly increasing behavior with VRS. This behavior might be likely caused by the stability of the CF, i.e. after the set process, the filament seems to be equally formed independently of the VRSs applied as extracted from Figure 3-9(b) where the current at low voltages (from 0 V to -1 V) is almost the same for all VRSs. Although not included here, set and reset currents (I_{SET} and I_{RESET}) also showed no dependence with VRS.

3.3. High resolution RTN characterization procedure

In this section, an accurate RTN characterization method for memristors is presented. The procedure allows obtaining a more complete RTN characterization in comparison to standard techniques. This method combines a setup based on the one presented in section 3.1 with the W-TL method explained in chapter 1.

3.3.1. Measurement and data analysis procedure

The setup used to perform RTN measurements is shown in Figure 3-14 which is based on the one shown in Figure 3-3. A semiconductor parameter analyzer (SPA) Agilent 4156C has been used as bias instrument to apply the voltage to the top terminal of the memristor and register the current through it by means of the SMUs described in chapter 1. Recording RTN signals by using the SPA would only offer a default measuring time resolution of the order of ms. This resolution is not large enough to characterize as much as possible current fluctuations. In this way, the

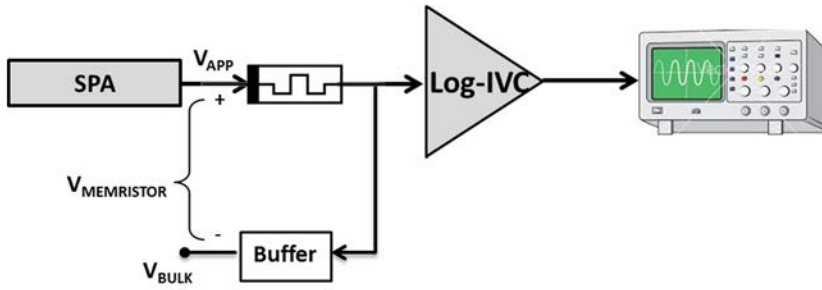


Figure 3-14: Schematic of the experimental setup developed to measure RTN signals with large time resolution. V_{APP} is the voltage applied by the semiconductor parameter analyzer (SPA) and $V_{MEMRISTOR}$ is the voltage drop across the memristor measured thanks to the included buffer. In this case, CLCU unit is not included since a current limit is not needed for RTN measurements.

memristor RTN current is registered, after the LOG-IV converter, with an oscilloscope, which has a resolution time between measurements larger than the SPA. In this case, CLCU unit has been disabled in the setup shown in Figure 3-3 since for RTN measurements a current limit is not necessary. This setup has allowed registering the whole RTN trace measured by the SPA and those signals captured by the oscilloscope which correspond to zoom measurements of the SPA trace. In this way, SPA and oscilloscope time resolutions can be compared for the same registered RTN trace.

Once the setup has been introduced, the measurement procedure is going to be detailed. Initially, memristors have been subjected to several resistive switching cycles (including the first cycle which corresponds to the forming process [129]) applying voltage ramps with an SPA to provoke the successive changes of the dielectric conductivity between a high and a low resistance state. The desired current limit when switching to the LRS has also been applied by the SPA. The purpose of this initial cycling has been to get a stable and well-created conductive filament through the dielectric layer. After this initial cycling, memristors have been switched to HRS in order to study RTN in this state. Then, the measurement procedure has followed the flux diagram presented in Figure 3-15. Since RTN fluctuations are not observed for any voltage, firstly, several attempts applying different constant voltages to the memristor have been performed with the SPA. When RTN has been observed at a certain voltage, RTN measurements have been carried out using the complete presented setup. Applying that suitable constant voltage V_{APP} by the SPA, the current trace through the memristor at HRS has been registered as a function of time by the SPA. At the same time, during the application of the constant voltage with the SPA, several oscilloscope captures have been registered varying the available time scales of the oscilloscope. Once SPA measurement has finished, the explained sequence started again performing another complete RTN measurement at the same

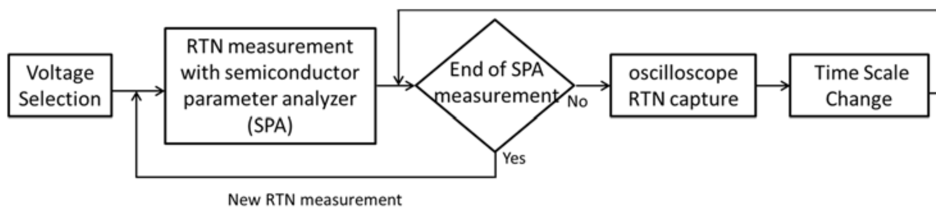


Figure 3-15: Flux of the RTN measurement process once a RTN signal has been detected at a particular voltage. RTN signals are simultaneously measured with the SPA and the developed setup. The time scale of the oscilloscope is changed during the measurement.

V_{APP}. Both instruments, SPA and oscilloscope, have been controlled by GPIB communication and a proper script to perform the required measurement procedure using MATLAB software was developed.

Once desired RTN measurement has been performed using the previous procedure, RTN traces can be analyzed by using different characterization methods such as histogram-based or TLP-based (described in section 1.2). As demonstrated in chapter 1, W-TLP improves TLP method allowing obtaining more RTN information. Then, combining the measurement procedure previously explained and the data analysis based on W-TLP method, a high-resolution RTN characterization procedure is proposed. Following, the applicability of this characterization method will be demonstrated with experimental results.

3.3.2. Applicability of the high-resolution method

Prior to RTN measurement, memristors have been initially subjected to 30 resistive switching cycles with an established current limit of 10 µA during HRS-LRS transition. In Figure 3-16, some of these initial RS cycles consisting in a set process, i.e. the transition from HRS to LRS (blue curves) and the reset process, i.e. the change from LRS to HRS (red curves) have been depicted. Once memristor has been switched to HRS, RTN fluctuations have been induced by applying a constant voltage bias, V_{APP}, equal to 1.25 V. During RTN measurement by using SPA, several oscilloscope captures have been registered varying available time scales from 0.1 s/div to 5 ns/div (i.e. varying time resolution from 400 µs to 0.02 ns). The measurement procedure explained in 3.3.1 has been carried out obtaining around 325 SPA measurements and 21 oscilloscope captures for each SPA trace. Not all SPA traces and oscilloscope captures have shown RTN fluctuations although the same V_{APP} has been applied in all the cases. The presented results correspond to a measurement in which a multilevel RTN signal has been observed.

Mention that only some parts of the SPA trace have been captured by the

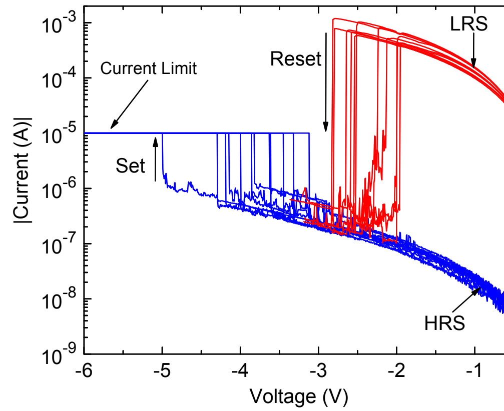


Figure 3-16: Initial RS cycling to form a stable conductive filament in memristor. Transition from HRS to LRS (blue lines) with a current limit of 10 µA and transition from LRS to HRS (red lines). X axis corresponds to the voltage drop across the memristor, so that it does not start at 0.

oscilloscope. This limitation is due to the GPIB communication since storing the oscilloscope data in the computer requires a specific time during which is not possible capturing more oscilloscope traces. However, the amount of the registered data is enough for the analysis of RTN.

An example of the RTN signal measured by the semiconductor parameter analyzer is depicted in Figure 3-17(a). Analyzing at naked eye directly the signal, around 5 or 6 different current levels can be distinguished what indicates there could be 3 defects provoking current fluctuations ($2^{\text{number of defects}}$ = number of current states, as indicated in chapter 1). On the other hand, from the 21 oscilloscope captures registered at different time resolutions, the three ones showing interesting current fluctuations are depicted for three different time resolutions, 40 µs (Figure 3-17(b)), 20 µs (Figure 3-17(c)) and 1 µs (Figure 3-17(b)). Each oscilloscope capture corresponds to different time slots of SPA current trace, approximately at around 8.4 s, 10.9 s and 20.7 s, respectively. Some fluctuations observed in the oscilloscope traces, which also correspond to some trapping and detrapping events in/from defects responsible for the RTN signal, appear with emission/capture times lower than 6 ms, which was the time resolution of SPA. These fast fluctuations of the current have not been detected with the SPA. Therefore, oscilloscope captures are giving additional information about RTN signal. Examining current fluctuations detected in Figure 3-17(b), (c) and (d) and looking at their current values, some current levels are coincident with those in Figure 3-17(a). However, in Figure 3-17(c) and Figure 3-17(d) a new current level (indicated in the figure as *), at around 200 nA, seems to be revealed. One possible explanation is that the defect emission and capture times related to this level (1.84 ms and 200 µs) are smaller than the SPA time resolution and therefore the level is undistinguished in that trace.

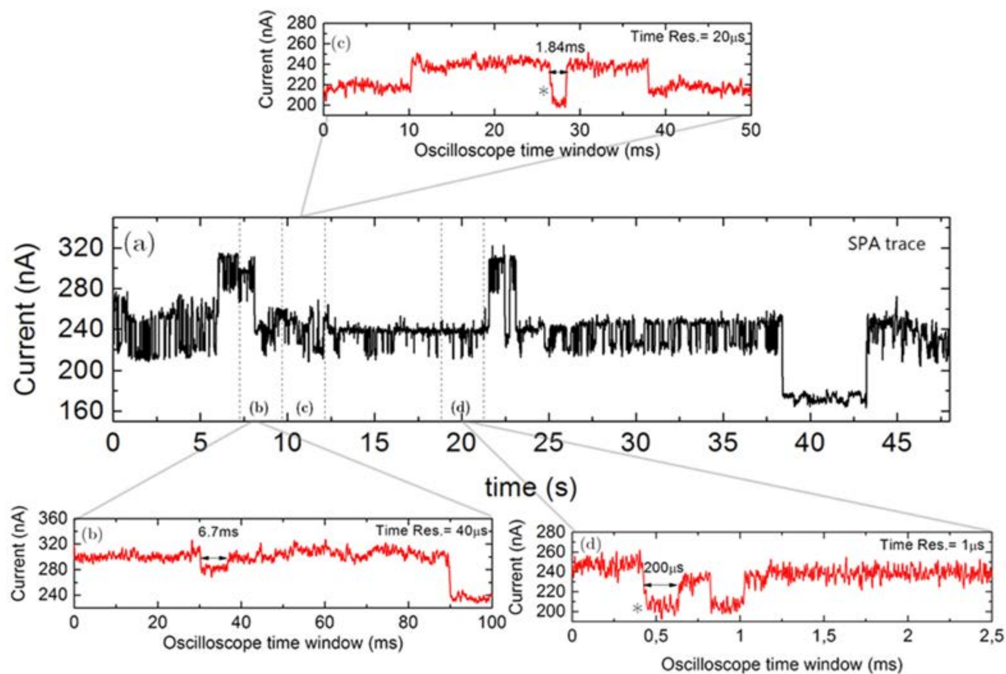


Figure 3-17: RTN signal measured by SPA (a) and oscilloscope traces captured within the intervals of: (b) 7.2–9.6 s, with 40 µs time resolution, (c) 9.6–12.1 s, with a time resolution of 20 µs and (d) 19.5–21.9 s with a time resolution of 1 µs.

Continuing with the analysis in order to find more information about the current levels of the RTN trace shown in Figure 3-17(a), the W-TLP method has been used for all RTN traces. First, the W-TL plots have been obtained from the SPA measurement and from the three captures of the oscilloscope, which are shown in Figure 3-18. Then, evaluating the diagonal of the plots and extracting the maxima of that diagonal, different levels in the RTN signals have been determined (and labeled) since each of those maxima corresponds to a current (defect) level of the signal. Separately, Figure 3-18(a) shows the W-TL plot of the whole RTN signal measured with the SPA and presented in Figure 3-17(a). On the other hand, Figure 3-18(b), (c) and (d) show the W-TL plots of the oscilloscope captures represented in Figure 3-17. As in the case of Figure 3-18(a), the existing current levels (again corresponding to defect levels) have been identified. Comparing these three figures with Figure 3-18(a), the same levels 2, 3, 5, 6 and 7 have been recognized as those red or yellow spots along the diagonal (keep in mind that red spots correspond to the maximum value and blue to the minimum in a rainbow palette).

Moreover, from Figure 3-18(c) and (d), a new current level at around 200 nA, labelled as L10, is also identified in the W-TL plot. This latter level, which has showed capture/emission times between 200 µs and 2 ms, has not appeared in the SPA measurement because of the lower instrument time resolution. However, the larger

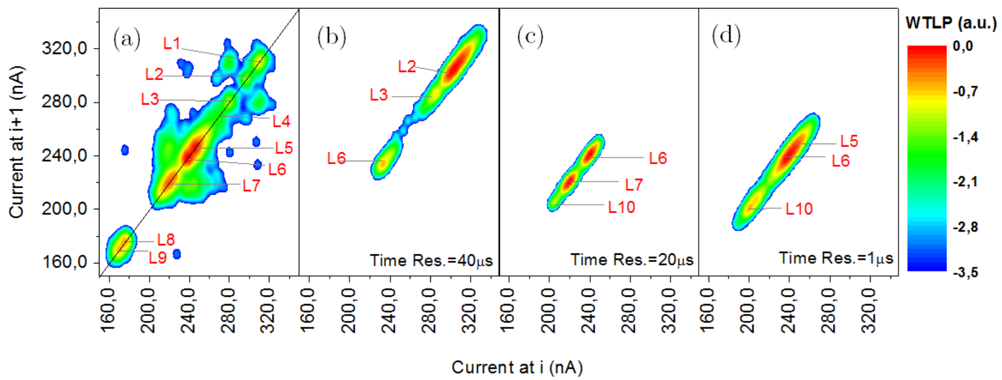


Figure 3-18: W-TL method applied to (a) the RTN measured by the SPA (Figure 3-17(a)). The line shows the diagonal of the plot, whose maximums correspond to the RTN current levels. 9 trap levels are detected; (b) oscilloscope capture with a time resolution of 40 µs (Figure 3-17(a)), 3 trap levels appear; (c) oscilloscope capture with time resolution of 20 µs with 3 trap levels (Figure 3-17(b); (d)) oscilloscope capture at the larger time resolution (1 µs), showing 3 trap levels (Figure 3-17(c)).

time resolution of the developed setup highlights its presence and it can be clearly visualized in the corresponding W-TL plots. The presence of this 10th current level is completely consistent with the expected number of current levels which can be at maximum 16. According to what explained in chapter 1, since there are 4 defects (more than 8 levels were detected in Figure 3-18(a)), up to 16 current levels should exist ($2^{4\ \text{defects}} = 16$ levels). From W-TL plot of the current trace obtained by SPA up to nine current levels have been detected plus the hidden level 10, which has been identified using the proposed method. Despite that, six levels would be still hidden and they have not been observed during the measurement. This might be because their probability of occurrence is too small or their emission and capture times are smaller than the minimum time resolution.

Finally, to complete the study of the RTN signal and corroborate the previous results, the diagonal of the different W-TL plots in Figure 3-18 have been analyzed (Figure 3-19). From the diagonal analysis of the W-TL plot of Figure 3-18(a), nine peaks and therefore nine current levels (labelled as L1-L9) have been obtained (Figure 3-19(b)). Remember that the number of current levels determined by the W-TL method is larger than that encountered at first sight only looking at the RTN signal. Likewise, the diagonal analysis of Figure 3-18(b), (c) and (d) allows obtaining the profiles of the oscilloscope captures with 40 µs, 20 µs and 1 µs time resolution shown in Figure 3-19(b), (c) and (d), respectively. Assessing Figure 3-19(b), (c) and (d), all the different peaks are indeed found as expected from the previous plots. For a time resolution of 40 µs (Figure 3-19(b)), three peaks have been encountered corresponding to current levels identified as the levels L2, L3 and L6. For 20 µs time resolution, these levels are L6, L7 and L10 (Figure 3-19(c)) and for 1 µs time

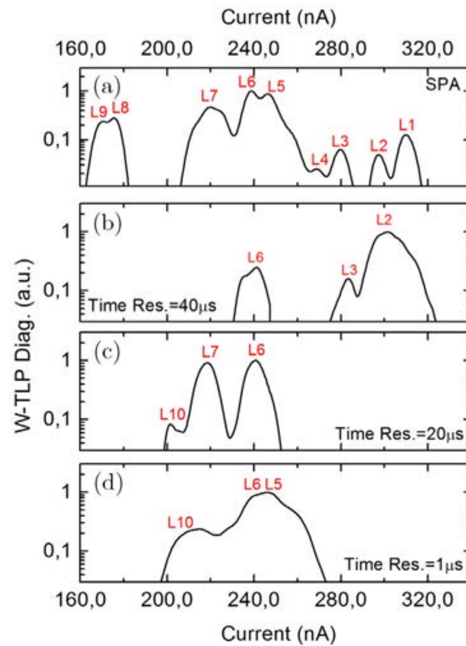


Figure 3-19: Profiles of the W-TLP diagonal for (a) SPA measurement, where 9 peaks were encountered and for oscilloscope captures with time resolution of (b) 40 µs, with peaks corresponding to levels 6, 3 and 2, (c) 20 µs, with levels 6, 7 and 10 and (d) 1 µs, with levels 5, 6 and 10.

resolution, L5, L6 and L10 (Figure 3-19(d)). All the peaks (i.e. current levels) encountered in these three plots have been well correlated with those in Figure 3-19(a) except for L10. The peak corresponding to this level appears at around 200 nA in Figure 3-19(c) and (d) whereas in the diagonal profile of the SPA measurement no peak for current values around 200 nA is found. This observation indicates, once more, that this current level has not been possible to be measured with SPA due to its lower time resolution. Although in this case the analysis of diagonal profiles has not given additional information as that extracted from W-TL plots, it is a useful tool for the RTN characterization to be considered, as demonstrated for the experimental multilevel RTN signal in chapter 1.

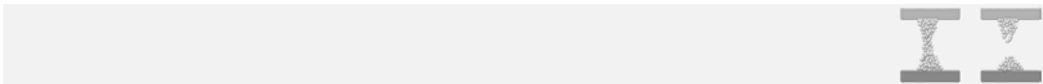
3.4. Conclusions

From the study of resistive switching (RS) phenomenon in the time domain (with a large time resolution) by means of the proposed experimental setup, a strong dependence of set and reset voltages on the speed of the applied voltage ramps to observe the RS phenomenon has been observed. Results have demonstrated that set and reset voltages increase with the increase of the voltage ramp speed. On the other hand, from the same analysis, it has been observed that the energies employed to

trigger set and reset processes are independent of the biasing conditions, specifically of the voltage ramp speed, suggesting that energy is an intrinsic parameter of the RS mechanism.

Regarding the RTN study, a new experimental setup that provides a larger time resolution than standard equipment has been presented to measure and analyze RTN signals. The obtained results have demonstrated that some RTN fluctuations can be undetectable if standard RTN characterization instruments, as semiconductor parameters analyzers with lower time resolution, are used. The analysis of RTN signals and, therefore, the identification of those hidden current levels have been performed with the W-TL method. Thus, a complete RTN characterization methodology, which combines high time resolution equipment and accurate parameters extraction method (W-TL), has been proposed to obtain an improved characterization of RTN signals and to study its impact on memristors performance.

4. SiO_X-BASED MEMRISTORS AS MEMORY/SELECTOR DEVICES



Concerning resistive switching memories (RRAMs), they are widely considered as one of the most promising technologies for nonvolatile memory (NVM). However, their feasibility as memory mainly requires a large on/off ratio, good endurance and high state retention occurring in the same memory device. On the other hand, memory cells are typically organized in crossbar arrays to be accessed through bit and word lines. Due to these lines are shared between several cells, some errors in the read/write operations can appear. Most common solution have been adding to the memory cell an extra element such as a selector device (SD). However, the availability of a robust selector element is still required for their integration. So, a new RRAM and a compatible SD structures must be investigated in order to improve existing commercial NVMs and SDs.

Hence, in this chapter, a study of different materials for the top electrode and the dielectric layer of a memristor device are combining and tested in order to find the most suitable combination for memory and selector applications. For the test process, continuous and pulsed operation conditions have been applied to found the most suitable operation conditions for a good resistance window and to study the endurance and retention of the devices. The work has been performed during a four-month abroad scholarship done in the *Dipartimento di Elettronica, Informazione e Bioingegneria* (DEIB) belonging to *Poitecnico di Milano,* (Italy) whose main topic focuses on the study of new materials for memory, selector and neuromorphic applications.

4.1. Memory and selector devices

Different materials for the top electrode and dielectric layer such as Cu, Ti, Ag and Nb_2O_5, SiO_X, respectively, have been studied to develop memory and selector devices. For memory purposes, the combination that has shown the best features is shown in Figure 4-1(a). RRAM devices consist of a SiO_X ($x \approx 1$) switching layer, with a thickness around 3 nm, and a Ti top electrode (TE) both deposited by electron beam (EB) evaporation. On the other hand, Figure 4-1(b) shows the material structure for a selector device with a switching layer of SiO_X ($x \approx 1$) with a relatively larger thickness of 5 nm. TE is formed by Ag also deposited by EB evaporation. In both memory and selector structures, top electrode and dielectric layer are located on a confined carbon bottom electrode, C(BE), which is connected by a W plug to a select transistor to control the current limit, I_C, during set with negligible parasitic capacitance [127]. Wafers, which initially consisted in an integrated select transistor, the W plug and the confined carbon BE, were supplied by Intel/Micron company. Then, memory and selector structures were finished in *the micro and nano technology center of the Politecnico di Milano (PoliFAB).*

As shown Figure 4-2, the whole devices used in all the experiments have been 1T1R structures consisting in one MOSFET transistor, which allows controlling the current limit, and a memristor (acting as the resistor). To perform RS measurements, the top electrode of the memristor is biased by V_{TE} while source terminal of the transistor (located at the bottom side of the wafer) is grounded. On the other hand, gate terminal of the transistor is biased with V_G to fix the desired current limit.

As indicated, the dielectric layer and the top electrode of the memristor have been fabricated over the provided INTEL wafers. Thus, the good control on material growth and especially in the dielectric growth which is quite relevant for a good performance of RS phenomenon is verified. In Figure 4-3(a) a piece of the structures

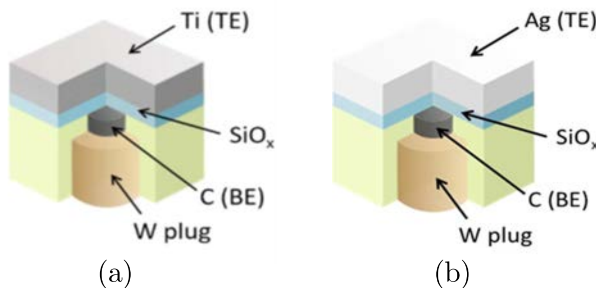


Figure 4-1: Schematic illustration of the (a) Ti/SiOx/C RRAM stack and (b) Ag/SiOx/C SD stack.

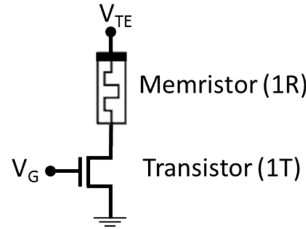


Figure 4-2: Sketch of a 1T1R structure where R is a memristor. V_{TE} corresponds to the voltage applied to the top electrode of the memristors whereas V_G corresponds to voltage applied to the gate electrode of the transistor in order to fix the desired current limit value through the structure.

presented in Figure 4-1, corresponding to the interface between C(BE) and dielectric layer, is sketched. Over this extracted structure, an atomic force microscopy (AFM) topography map has been obtained (Figure 4-3(b)) to show the difference between the grown dielectric layer and the C(BE). In addition, the profile along the step is also included in Figure 4-3(c) which shows that the SiO_X thickness has been indeed kept below 3 nm as expected. Furthermore, to show the good control on dielectric growth and suitability of SiO_X as RS active layer, the influence of dielectric thickness on forming voltage (V_{FORM}) has been analyzed for RRAM devices. Figure 4-4 shows V_{FORM} measured in four different devices where their dielectric thicknesses have been 2, 3, 7 and 11 nm, approximately. V_{FORM} shows a linear dependence on dielectric thickness which is in complete agreement with other works using SiO_2 [125]. Therefore, the understanding of RS in SiO_X is compatible with the already-known physical mechanisms explained in chapter 1.

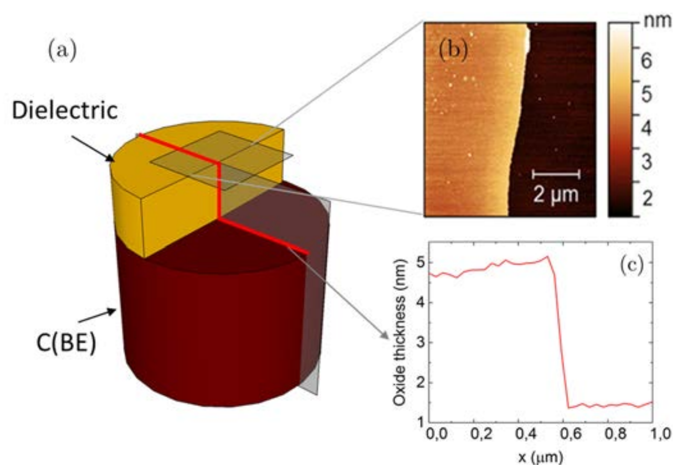


Figure 4-3: (a) Sketch of the interface between dielectric layer and C(BE). (b) Atomic force microscopy (AFM) topography map. (c) Profile along the step indicating a SiO_X thickness of approximately 3 nm.

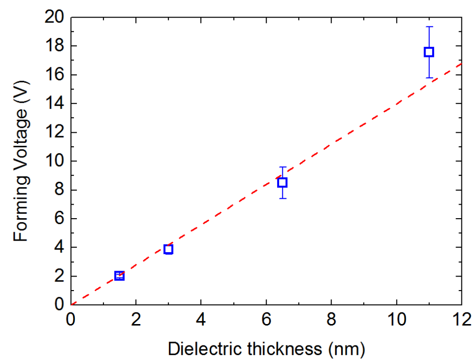


Figure 4-4: Forming voltage (V_{FORM}) showing a linear dependence on dielectric thickness.

4.2. Ti/SiO_X memory characteristics

Initially, Figure 4-5 shows an experimental I-V characteristic of previous memristor structure where relevant parameters are indicated for the bipolar RS shown by the memristor. For the set process (positive voltages), the voltage at which set process is produced, labeled as V_{SET}, as well as the current limit are shown. For the reset process (negative voltages), two characteristic voltages are considered since in these devices reset process occurs progressively: the voltage at which reset process begins, V_{RESET}, and the maximum voltage applied to stop the process, V_{STOP}, necessary to control when ion-based filament dissolution stops [125], [130]. Finally, the resistance window between HRS and LRS states, measured at the negative voltage V_{READ}, is indicated.

Then, for the study of Ti/SiO_X structure as memory device, several characteristics have been analyzed. First, the device behavior under DC conditions, i.e. applying very slow voltage ramps, has been studied in order to found the best operation conditions to achieve mainly the greatest resistance window. To do that, measurement where one of the parameter previously indicated is varied have been performed. Once the most suitable DC operation voltages have been found, the device working as memory has been corroborated under pulsed conditions. Voltage pulses have been applied to provoke both set and reset processes and perform the different resistance switches in order to find the most suitable voltage amplitude and time parameters of the applied pulse. Additionally, a very large endurance measurement has been performed under pulsed conditions to demonstrate the great durability (number of device switching cycles for an acceptable resistance window) of those devices since the endurance is one the most crucial aspect in memory applications. Another aspect to take into account for memory application is the retentions of the states under adverse conditions as for example high temperature.

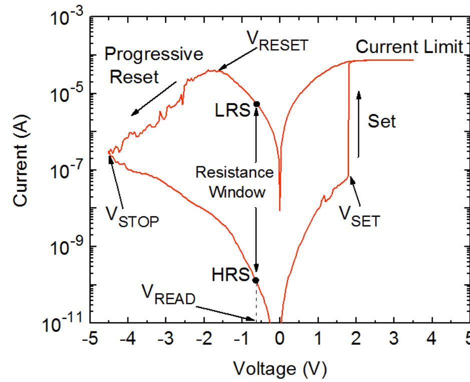


Figure 4-5: Experimental I-V characteristics of the Ti/SiO_X structure studied as a RRAM device.

Thus, a study of the retention of the both resistance states (HRS and LRS) with temperature has been also performed.

4.2.1. DC characteristics

To perform the DC characterization of the memristors, the schematic setup shown in Figure 4-6 has been used. Top electrode of the memristor and the gate terminal of the select transistor have been biased, with a semiconductor parameter analyzer Agilent 4156C, to provoke memristor resistance changes and to adjust the required current limit, respectively. At once, source (and bulk) transistor terminal has been directly grounded through the bottom side of the wafer.

Two types of measurements have been performed: one to find the most suitable V_{STOP}, which allows a large resistance window, and the other one to test the resistance window retention along the cycling at that V_{STOP}. First measurement has consisted in varying V_{STOP} in a range between -2.5 V and -4.5 V and performing 20 RS cycles for each voltage while the maximum positive voltage applied to provoke set process

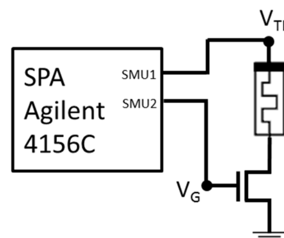


Figure 4-6: Sketch of bias connection from the SPA to the gate terminal of the transistor and to the top electrode of memristor.

has been 3.5 V. The transistor gate voltage has been adjusted to fix a current limit of 70 µA. In Figure 4-7, a representative I-V curve representing the general behavior of the 20 cycles is shown for each V_{STOP}. At first sight, it becomes appreciable that the resistance value of HRS state as well as V_{SET} increase as V_{STOP} increases. The increment of the HRS resistance implies that the resistance window increases since LRS resistance is almost constant. This increase indicates conductive filament dissolution is larger as V_{STOP} increases provoking that a larger V_{SET} is necessary to re-form the filament. That suggests the resistance window can be controllable by varying V_{STOP}, although more voltage is required to trigger the set process since V_{SET} also increases.

To better show previous increasing behaviors, HRS and LRS resistances and V_{SET}, all of them extracted from all the previous I-V curves, are depicted in Figure 4-8(a) and (b) , respectively, as a function of V_{STOP}. Graphs correspond to box plots where square horizontal sides indicate 75th (top side) and 25th (bottom side) quartiles, the line inside the square is the median value of data and finally outer lines correspond to maximum and minimum values of the data set. Figure 4-8(a), where resistance values of LRS and HRS measured at V_{READ} = -0.5 V are depicted, shows how the resistance window increases with V_{STOP} reaching a maximum value of approximately 4 decades for V_{STOP}= -4.5 V. This occurs because HRS resistance increases with V_{STOP} (from $2x10^6$ Ω to $8x10^9$ Ω) whereas LRS resistance remains almost constant at around 10^5 Ω. On the other hand, in Figure 4-8(b), where set voltages are also box plotted, a relevant influence of V_{STOP} on V_{SET} is observed. Set voltage rises when reset process duration is increased (larger V_{STOP}). This result might be explained according to the bipolar-RS mechanisms, considering that the larger the voltage to migrate metallic atoms back to the top electrode during reset process, the larger the voltage necessary to re-create metallic filament in the subsequent set process [131]–[133].

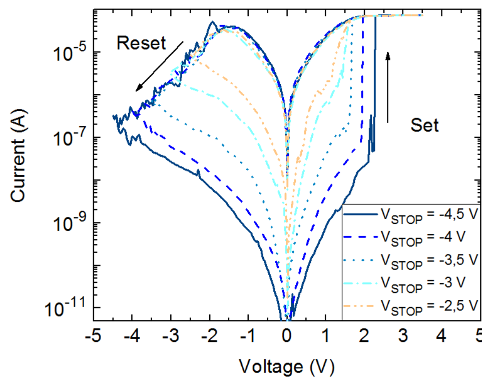


Figure 4-7: Representative measured I-V curves for the 1T1R RRAM devices under DC conditions at I_C = 70 µA for different V_{STOP} (from -2.5 V to -4.5 V).

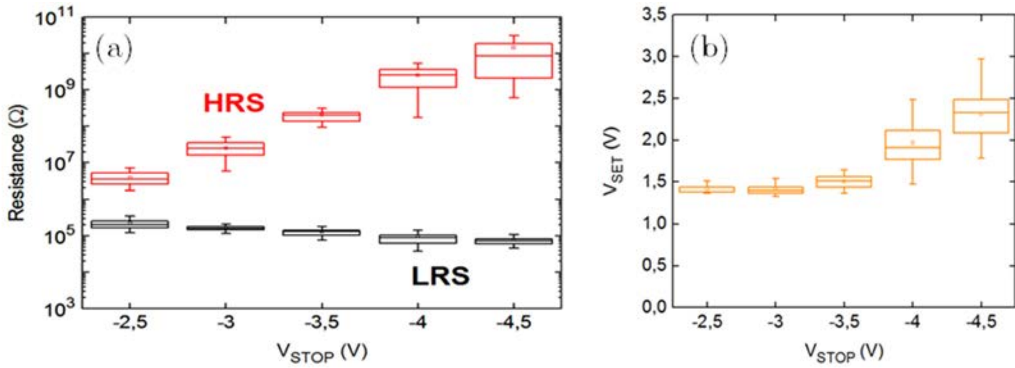


Figure 4-8: (a) Resistance values of HRS and LRS measured at V_{READ} = -0.5 V and (b) V_{SET} as a function of V_{STOP}.

On the other hand, to test the retention of resistance window values along cycling, a DC measurement of 400 RS cycles has been carried out under the operation conditions previously found. Therefore, V_{STOP} has been -4.5 V to get the maximum resistance window, which has been approximately of 10^4, a current limit of ~70 µA and a maximum positive voltage of 3.5 V. A few measured I-V curves are depicted in Figure 4-9 where resistance window is indeed showing a four-decade-of-magnitude value. Furthermore, V_{SET} and V_{RESET} show a quite stable behavior, as expected. Abrupt set transition occurs approximately at V_{SET} = 2.5 V whereas gradual reset transition is overall initiated at V_{RESET} = -1.5 V.

Taking advantage of the relatively large cycling measurement, resistances at HRS and LRS have been statistically analyzed. Figure 4-10 shows the cumulative distribution functions of both resistances along those 400 cycles. These resistances show a small cycle-to-cycle variability what indicates a good state stability. Besides,

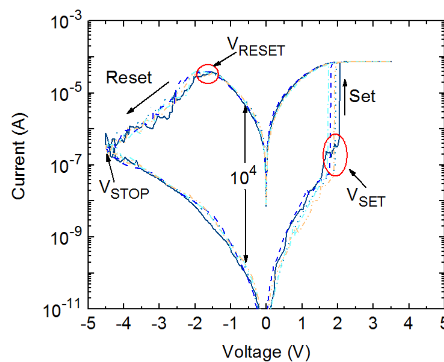


Figure 4-9: Representative measured I-V curves from the DC endurance measurement for the 1T1R RRAM devices at I_C = 70 µA and V_{STOP} = -4.5 V, showing a stable resistance window of four orders of magnitude.

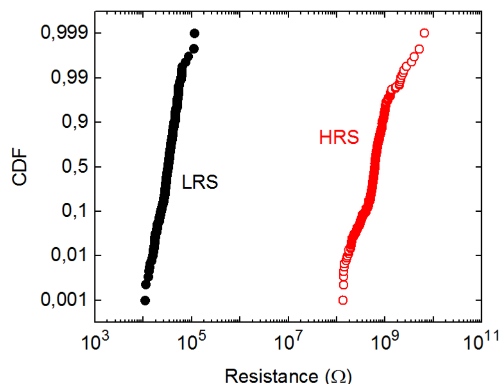


Figure 4-10: Cumulative distributions of LRS and HRS resistances for a cycling of 400 RS cycles with a V_{STOP} =- 4.5 V and I_C = 70 µA.

a large resistance window of approximately 4 decades is observed along cycling, indicating a good retention of such a window. Such a large resistance window and excellent resistances uniformity are promising characteristics to overcome the noise issues affecting the RRAM performance as indicated in [134]. One of them is current fluctuations at HRS and LRS states due to RTN, which was presented in chapter 3.

4.2.2. Pulsed characteristics

After DC measurements, which have allowed determining the operation voltages, RS measurements have been performed applying pulses. The reason of applying pulses is to characterize the behavior of the devices under the most similar conditions as those in commercial devices.

Pulsed measurements have been performed using an arbitrary waveform generator to apply the pulses and an oscilloscope to register all the events and also the applied voltage pulse. To register the current through the device, the input oscilloscope impedance is previously adjusted to 50 Ω what allows measuring the voltage drop across such an impedance which is directly related to the current through the device (Figure 4-11). The device current is finally obtained converting the registered voltage drop into current by Ohm's law. Thus, I-V characteristics of the device can be reconstructed to extract the RS parameters such as V_{SET}, V_{RESET} and/or HRS and LRS resistances.

However, measuring HRS from reconstructed I-V curves can give erroneous values if the current through the device is too small. In this case, the voltage corresponding to that current is also small, being more difficult to register due to the limited voltage resolution of the oscilloscope, which must be large enough to register the whole set and reset processes.

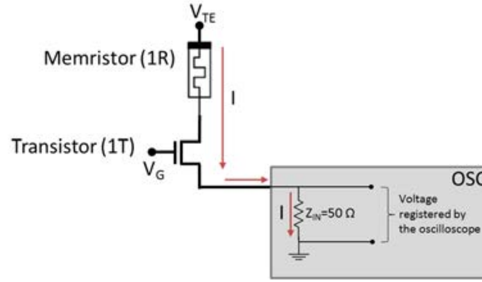


Figure 4-11: Schematic of the setup configuration to register current adjusting input impedance of the oscilloscope to 50 Ω and measuring the voltage drop across it.

To give more information about actual resistance states of the device, the experimental setup shown in Figure 4-12 has been used to get those resistance states also under DC conditions. Therefore, HRS and LRS resistances can be extracted from both DC and pulsed measurements. The setup includes an arbitrary waveform generator TTi AWG TGA 12102 to apply bursts of positive and negative voltage pulses to provoke set and reset processes respectively. This waveform generator also applies the corresponding bursts of pulses to the gate of select transistor to adjust the current limit. An oscilloscope LeCroy WaveRunner XI series to monitor the voltage pulse applied to the device voltage and the current through it previously converted into voltage by the low input impedance of 50 Ω and a SPA Agilent 4156C to perform DC measurements are also included in the setup. Finally, to switch between pulsed and DC measurements a developed board mainly consisting in two switches has been also used in the setup.

The whole setup has been controlled by GPIB connection, using MATLAB software to define and execute the measurement sequence that is described as follows:

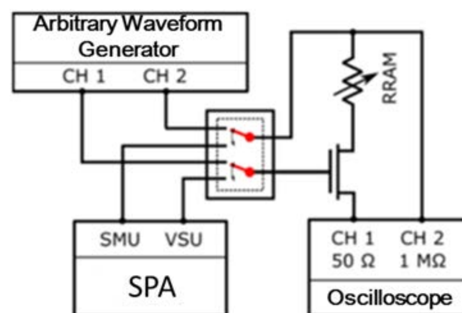


Figure 4-12: Experimental setup for the 1T1R structures. A switch matrix was used to change from DC to pulsed characterization schemes.

Measurement sequence:

1. With board switches at pulsed mode, a determined number of bursts of triangular voltage pulses are applied by the waveform generator to the memristor to provoke set and reset processes sequentially.
2. Board switches are changed to DC mode by applying a square pulse. Then, because the last pulse of the bursts was applied to provoke the reset process, the HRS resistance is measured by applying a low-voltage ramp by the SPA.
3. Board switches are changed to pulsed mode again. Then a single positive pulse is applied by the waveform generator to provoke the set process.
4. Now, because the device is at LRS, its resistance is measured under DC conditions applying a low-voltage ramp by the SPA after changing board switches to DC mode.
5. Finally, board switches are changed to pulsed mode again to repeat the sequence as many times as required.

Figure 4-13 shows the applied voltage pulse (dashed blue line) to perform a single set/reset sequence and the current (solid red line) through the memristor showing set and reset transitions. Clearly, set and reset events are observed during the rise time of both pulses. Therefore, the experiment to study RS pulsed characteristics of the devices has consisted in applying bursts made up by a triangular positive voltage pulse with a 5.5 V amplitude to provoke set event and a triangular negative voltage pulse to provoke the reset event. The amplitude of reset pulse (equivalent to V_{STOP} in DC measurements) has been varied every 100 cycles in a range between -2.5 V and -4 V to observe the V_{STOP} influence. The pulse width for both set and reset pulses has been always 5 µs. Following the measurement sequence previously explained,

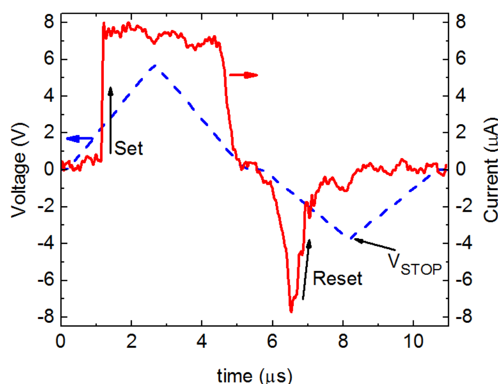


Figure 4-13: Measured voltage and current during a pulsed set/reset sequence.

after-set and after-reset I-V curves have been measured under DC conditions at cycle number 50 of every set of 100 cycles to obtain afterward HRS and LRS resistance. As indicated, before performing the pulsed or DC measurement, the proper signal is applied to the switch board just to change its state and allow the instrument (waveform generator or SPA) to apply the corresponding bias.

From the measured voltage and current traces shown in Figure 4-13, the typical I-V characteristics can be reconstructed. Figure 4-14(a) and (b) show two examples of those curves when V_{STOP} is -2.5 V and -4 V, respectively. In both cases, set and reset events are indicated as well as the reached V_{STOP}. Although less clear than in DC measurements, set and reset voltages and HRS and LRS states are also identifiable. It can be observed that resistance window increases as V_{STOP} increases, corroborating the resistance window control by the V_{STOP} parameter as seen in DC characteristics. It is also observed that V_{SET} and HRS resistance increase when V_{STOP} increases; a similar behavior than that observed under DC condition in Figure 4-8. Thus, the devices operate quite similar under both DC and AC conditions.

To better support the previous results, Figure 4-15 shows HRS and LRS resistances (empty red and solid black circles, respectively) extracted at V_{READ} = -0.5 V from the reconstructed I-V curves during the cycling experiment where V_{STOP} has been increased every 100 cycles. Moreover, HRS and LRS resistances extracted also at V_{READ} = -0.5 V from I-V curves measured under DC conditions after the 50th set/reset pulsed cycle of every V_{STOP} are also included (empty red and solid black squares). HRS shows larger values at higher V_{STOP} whereas LRS remains barely unchanged what corroborates the good control of the resistance window by varying V_{STOP} under pulsed conditions. From resistances measured under DC conditions after 50 pulsed cycles in every V_{STOP}, resistance window reaches a value of ~3.5 decades at V_{STOP} = -4 V what is quite in agreement with DC characteristics in Figure 4-8.

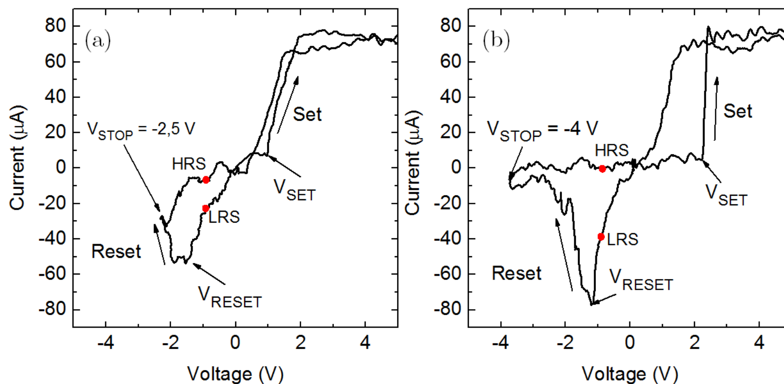


Figure 4-14: Reconstructed pulsed I-V curves for (a) V_{STOP} = -2.5 V (b) and V_{STOP} = -4 V.

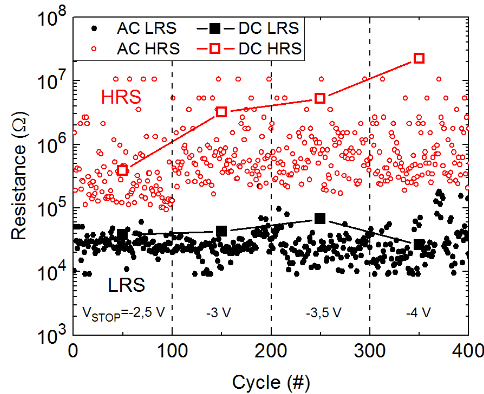


Figure 4-15: LRS and HRS resistances extracted from pulsed I-V curves as a function of cycles, where V_{STOP} was increased every 100 cycles. LRS and HRS resistances extracted from DC I-V curves were measured in the middle of each set of 100 cycles.

Contrarily, a lower resistance window is obtained under pulsed conditions because extracted HRS resistance is lower due to the limited voltage resolution of the oscilloscope.

4.2.3. Endurance characteristics

To show the feasibility of the analyzed memristor as memory, good endurance results would be needed. To analyze the maximum endurance achievable is these devices, the experimental setup shown in Figure 4-12 has been used to apply consecutive set and reset pulses bursts and measuring HRS and LRS states (under DC conditions) three times within every decade of applied pulses. Experimental pulsed conditions have been also a positive triangular pulse with an amplitude of 5.5 V, a negative triangular pulse of -4 V of amplitude, corresponding to V_{STOP} and a pulse width time of 5 µs for both positive and negative pulses. The value of V_{STOP} has been slightly reduced in comparison with the value found under DC conditions to maximize the endurance following the results observed in [55] where the impact of V_{STOP} on the maximum number of cycles achievable before device failure is analyzed in an endurance measurement on HfO_X-based memristors.

Unlike in Figure 4-15, in Figure 4-16 only HRS and LRS resistances extracted from I-V characteristics measured under DC conditions are depicted to better show endurance results. From the figure, a constant resistance window larger than 1 decade for at least $5x10^7$ cycles is observed. Then, after 10^8 cycles, the closure of the window occurs what means that the device is not cycling anymore. An endurance of almost 10^8 cycles is a starting quite promising result for SiO_X-based memristors to be considered as the next non-volatile memories.

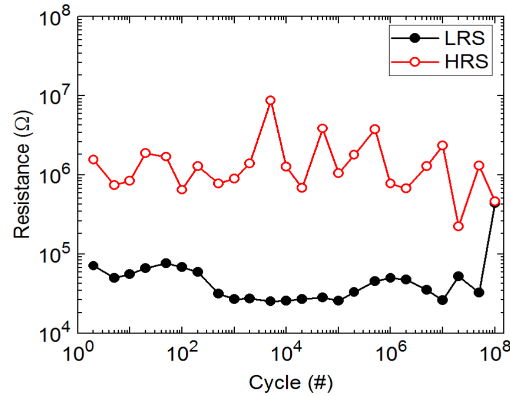


Figure 4-16: Cycling of HRS and LRS resistances extracted from the I-V characteristics measured under DC conditions three times in every decade of cycles.

Although not depicted in the previous figure, resistances of HRS and LRS states were also extracted from the I-V curves reconstructed from the pulsed measurements what have allowed performing a statistical analysis. In Figure 4-17(a) and (b) the cumulative distribution functions of those resistances are shown after 10^4 cycles and 10^7 cycles, respectively. In both cases, a proper separation between states is observed suggesting a good resistance window retention along cycling. The low sensitivity of the voltage (corresponding to the converted current through the memristor) registered by the oscilloscope at HRS (mentioned in subsection 4.2.2) slightly affects to obtain accurate current values and, therefore, accurate and actual HRS values. This is observed in the great dispersion of HRS cumulative distribution function which comprises two decades. Overall, this effect provokes a decreasing in HRS resistance value in comparison with that obtained from I-V curves under DC

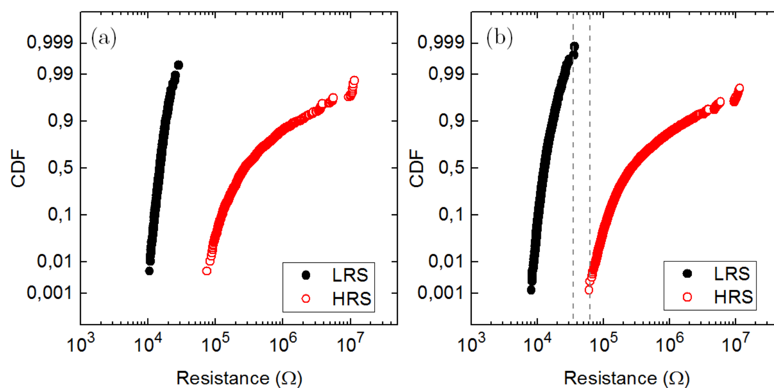


Figure 4-17: Cumulative distributions of HRS and LRS resistances after (a) 10^4 cycles (b) and 10^7 cycles showing an adequate resistance window even in the wort case (dashed lines).

conditions. Cumulative distributions after 10^7 cycles present also a suitable resistance window even in the worst case (dashed lines in Figure 4-17(b)).

4.2.4. Retention characteristics

Another important characteristic to be analyzed, to test the suitability of a new material structure for memory application, is the dependence of the state retention on temperature to observe how the devices behave under unfavorable conditions like device heating. To characterize retention behavior, devices have been firstly programmed under DC conditions to HRS establishing different V_{STOP} (-2.5 V, -3.5 V and -4.5V) with a fixed I_C of 100 µA; and to LRS by tuning different I_C (~ 21 µA, 64 µA and 135 µA) for a fixed V_{STOP} = -4.5 V. Then, the six devices have been subjected to annealings of one hour duration at different temperatures (from 120 °C to 260 °C). After each annealing, resistance state of every device has been verified applying low voltages under DC conditions and at room temperature (25 °C).

Figure 4-18(a) shows the evolution (or retention) of measured HRS and LRS resistances with annealing temperature. Data depicted there indicate a strong stability with less than 1-decade loss for HRS and a negligible resistance change for LRS within the studied temperature range. I-V curves at the beginning of the experiment and after every annealing have been registered (Figure 4-18(b)). Both I-V curves before (dashed blue line) and after (solid red line) the annealing are depicted for a device switched to LRS (I_C = 100 µA and V_{STOP} = -4.5 V) to show indeed a full set/reset functionality displayed by the memristor. This behavior has been observed also for the devices at HRS.

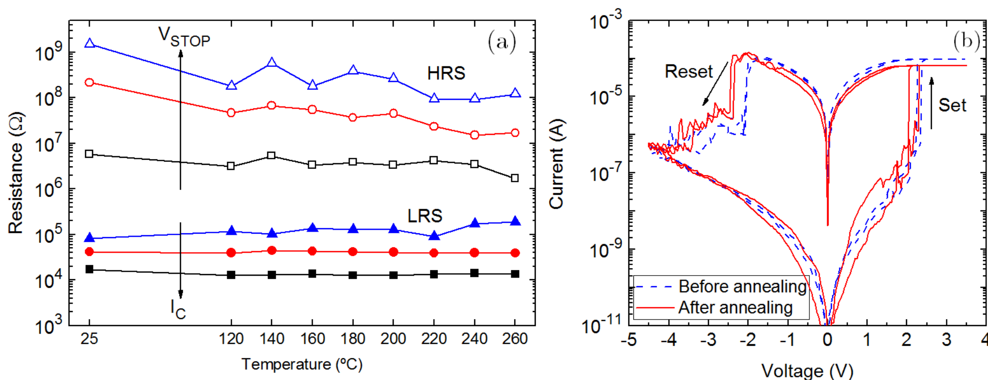


Figure 4-18: (a) Measured HRS and LRS resistances as a function of annealing temperature and (b) I-V curves before and after the annealing experiments. HRS resistance decreases by less than a factor of 10 within the studied temperature range.

4.3. Ag/SiO_X selector device characteristics

The feasibility of Ag/SiO_x structure to behave as a selector device (SD), which is based on the threshold switching mode presented in chapter 1, has been studied. To do this, both DC and pulsed characteristics have been analyzed by performing proper experiments. On the one hand, threshold switching has been carried out under DC conditions to determine the voltage at which switching takes place (threshold voltage, V_T) and the voltage at which filament dissolution spontaneously occurs (holding voltage, V_H). Then, the influence of the current limit on the volatile or nonvolatile behavior of the resistance state has been also analyzed under DC conditions. The importance of an initial positive forming in the bidirectional performance of Ag-based memristor as SD has been also studied. On the other hand, a study of the influence of pulsed conditions on the threshold switching behavior of these memristors has been performed. Specifically, the influence of the width time of the applied pulse has been studied on the voltage V_T. In addition, the retention time of the conductive filament have been studied for different pulse width times.

4.3.1. DC characteristics

First experiment performed under DC conditions has consisted in applying DC voltage ramps in both directions, positives and negatives voltages, up to 2.5 V and –1 V, respectively, establishing a current limit of I_C ~ 20 µA to observe the threshold switching behavior in the devices. Consequently, devices have displayed volatile bidirectional threshold switching as shown in Figure 4-19 where I-V curves are depicted. In this figure, characteristic voltages of a selector device are pointed out: positive threshold voltage V_{T+}, negative threshold voltage V_{T-}, at which set event occurs, and positive and negative holding voltages, V_{H+} and V_{H-} respectively, at which filament spontaneous dissolution takes place. Additionally, the I_{OFF} current, measured to check if the whole TS cycle has successfully occurred, is also indicated at 0.5 V (I_{OFF+}) and -0.2 V (I_{OFF-}) for positive and negative TS, respectively.

Bidirectional threshold switching cycling, at the abovementioned conditions, has been performed obtaining more than 120 cycles. In Figure 4-20(a), threshold and holding voltages, extracted from the I-V curves, are graphed as a function of the number of cycles. Voltages show a stable behavior under cycling being V_{T+} ~ 2 V, V_{T-} ~ -0.5 V, V_{H+} ~ 1.5 V and V_{H-} ~ -0.4 V. Additionally, Figure 4-20(b) represents the I_{OFF} current which shows a value of ≈ 1 pA. This value corroborates that device has performed a whole threshold switching cycle since low resistance state has not been retained when bias voltage has been reduced to zero.

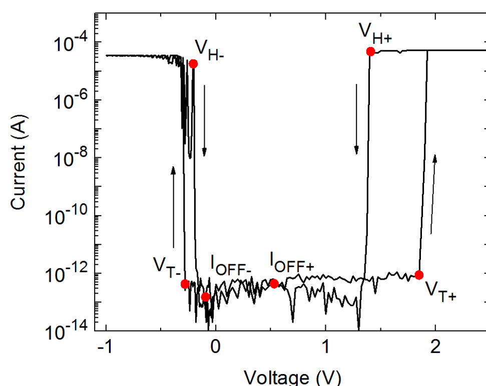


Figure 4-19: Measured I-V curves of the SD. The threshold (V_{T+}, V_{T-}) and hold voltages (V_{H+}, V_{H-}) as well as the current at off state for both positive and negative voltages are indicated.

To analyze the impact of the current limit on the SD performance, a second experiment where the current limit has been increased every 20 cycles in a range from 3 µA to 100 µA has been performed. Figure 4-21(a) shows the extracted voltages V_{T+}, V_{T-}, V_{H+} and V_{H-} for the different I_C as a function of the number of cycles. For small current limits ($I_C \leq 80$ µA), bidirectional threshold switching is observed, however, at higher I_C, threshold switching is not observed anymore with $V_H \sim 0$. This is probably due to the formation of a permanent filament as Figure 4-21(b) suggests, where an I-V curve for $I_C = 50$ µA (solid black line) and $I_C = 100$ µA (dashed blue line) are depicted. When $I_C = 50$ µA, volatile behavior of filament and, therefore, a complete TS cycle, is clearly observed whereas when $I_C = 100$ µA the switching is not observed either for positive or negative voltages because the filament is permanently formed and no disruption occurs. These results suggest that SiO_X-based

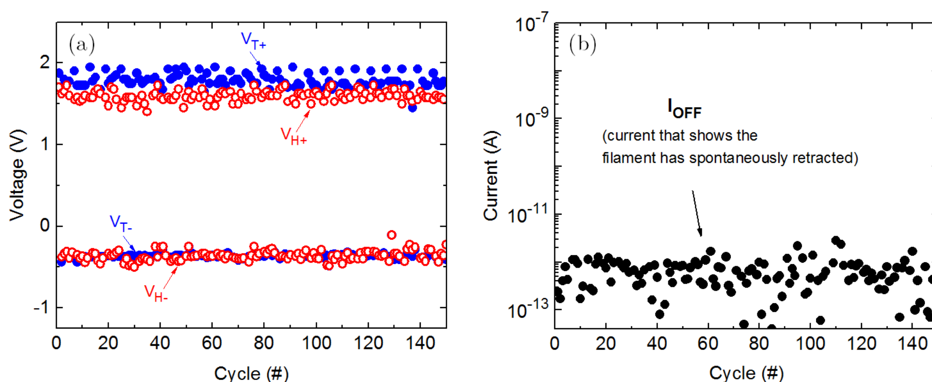


Figure 4-20: (a) SD voltages as a function of number of cycles showing a good stability over repeated threshold switching cycles. (b) I_{OFF} current with values of the order of pA to show the volatile behavior of the device resistance state.

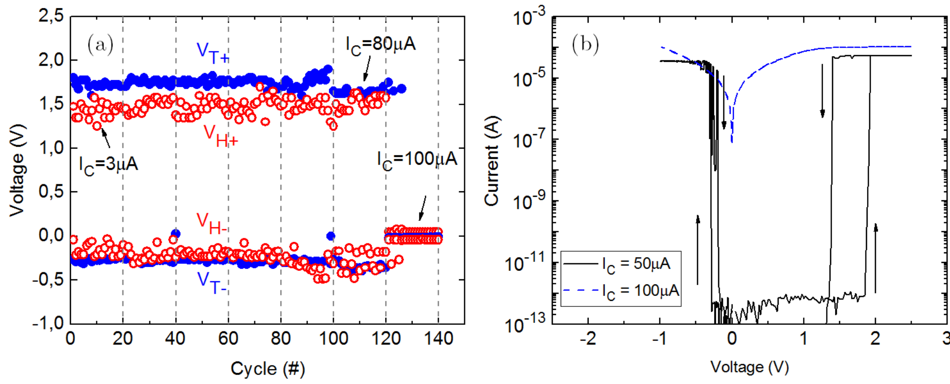


Figure 4-21: (a) Measured threshold voltages, V_{T+}, V_{T-}, and hold voltages, V_{H+}, V_{H-}, with increasing I_C as a function of the number of cycles. (b) I-V curves for I_C = 50 µA and I_C = 100 µA showing volatile and nonvolatile switching respectively.

memristors can be used as SD only for relatively low $I_C \leq 80$ µA.

Another remarkable result observed for these selector devices is related to their bidirectional behavior. Threshold switching is mainly initiated by performing a positive forming process. Typically, applying a positive sweep the forming process is caused as shown in Figure 4-22(a) (at V_{FORM} = 3 V). Then, subsequent negative and positive threshold switching cycles are observed successively. However, the possibility of performing TS cycling after a negative forming process has been also analyzed. Contrarily, applying a negative voltage sweep on a pristine device, where positive forming has not been previously performed, no switching has been observed even when a large voltage as -12 V is applied. Consequently, no threshold switching has been observed. This suggests the necessity of a positive forming process before performing bidirectional TS cycling. Overall, the mechanisms governing threshold switching can be attributed to voltage-induced migration of cations from the TE to

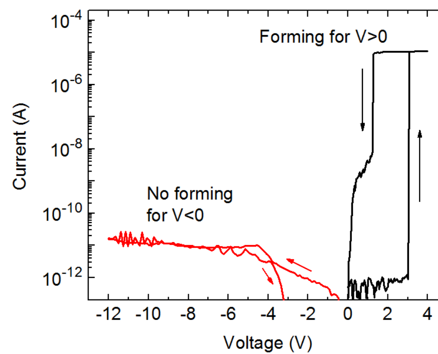


Figure 4-22: I-V characteristics showing forming process for positive voltages whereas no forming process is observed for negative voltages.

create the conductive filament. Therefore, the TS bidirectional cycling, observed only if a positive forming process is carried out, might be due to an accumulation of migrated ions in the interface between C(BE) and the dielectric layer during the forming. The threshold switching would occur if a conductive filament is formed/disrupted between Ag top electrode and the region with accumulated metallic ions.

4.3.2. Pulsed characteristics and retention time

Continuing with the study of the Ag/SiO_X-structure memristors suitability for SD application, pulsed measurements have been performed. During the first experiment, the waveform shown in Figure 4-23(a) consisting in semi-triangular positive and negative pulses with the same duration time (t_P) has been applied to provoke the bidirectional threshold switching. The measurement has consisted in varying the duration time of the semi-triangular pulse registering simultaneously the current through the device as shown in Figure 4-23(b). Now, the current through the memristor is previously converted to voltage using a commercial I-to-V converter to be registered by the oscilloscope (with high input impedance). Then, current is obtained by using the I-V ratio conversion of the commercial converter. As in other pulsed measurements, monitoring voltage and current traces allows reconstructing the I-V curves to obtain more easily the threshold switching parameters. Figure 4-23(c) shows the reconstructed I-V from the traces represented in Figure 4-23(a) and (b) where only positive and negative switching are observed. The spontaneous disruption of the conductive filament is not observed because it is expected to occur when pulse abruptly decreases to 0 V due to the volatility of the

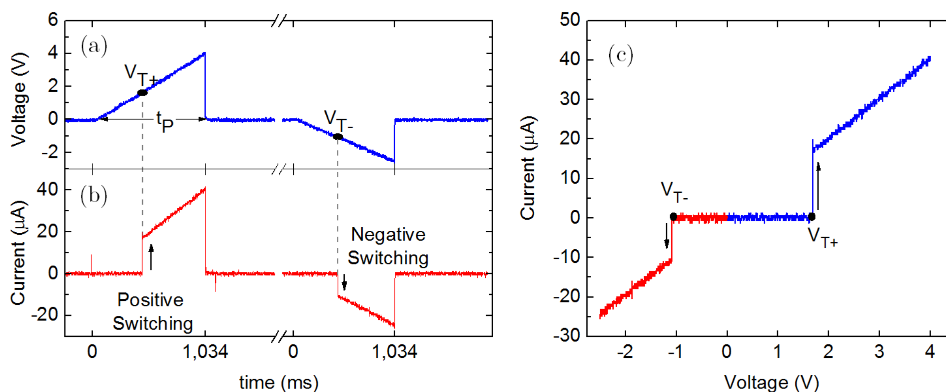


Figure 4-23: Measured (a) voltage and (b) current during a positive/negative switching sequence. (c) Corresponding I-V curves.

process. Therefore, only threshold voltages can be extracted for the different established duration times. In Figure 4-24, V_{T+} and V_{T-} extracted from the bidirectional switching sequence are box plotted as a function of t_P. Both threshold voltages show an increasing behavior when t_P decreases what indicates that the voltage needed to perform the switching at positive and negative polarities increases for faster pulses. This behavior might be due to the acceleration of Ag-cation migration from metallic electrodes as the speed of the pulse increases as suggested in [135] where authors observed an increase of the threshold voltage when sweep rate was increased on a Ag/TiO_2-based memristors acting as selector devices.

The influence of pulse duration on the retention time of the volatile state (the time needed for the spontaneous filament dissolution when voltage is swept back to zero) has been studied. Thus, the second experiment has consisted in applying several pulses as those shown in Figure 4-25(a) and (c) and registering the current through the devices to analyze positive and negative threshold switching, respectively, for different pulse duration times, t_P. To provoke the switching, triangular pulses of 3.5 V and -2.5 V are applied. Subsequently, a long square pulse whose amplitude is 0.2 V and -0.2 V for positive and negative polarities is applied to measure the retention time. The retention time, t_{RET}, has been evaluated by monitoring the current during triangular-square positive and negative pulses as shown in Figure 4-25(b) and (d). The retention time is obtained by measuring the time between the moment when voltage is abruptly decreased to zero and the moment when the current goes down and therefore filament dissolution takes place (Figure 4-25(b) and (d)). To perform such a measurement, the time of the square pulse has been 10 times longer than the switching pulse width t_P, which has been varied between 10 µs and 10 ms.

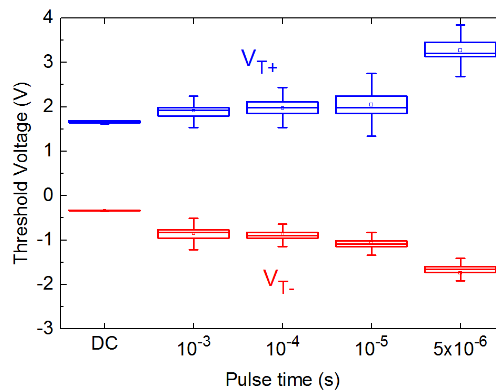


Figure 4-24: Threshold voltages (V_{T+} and V_{T-}) at different pulse times (t_P). Voltages increase when t_P decreases, i.e. pulses are faster.

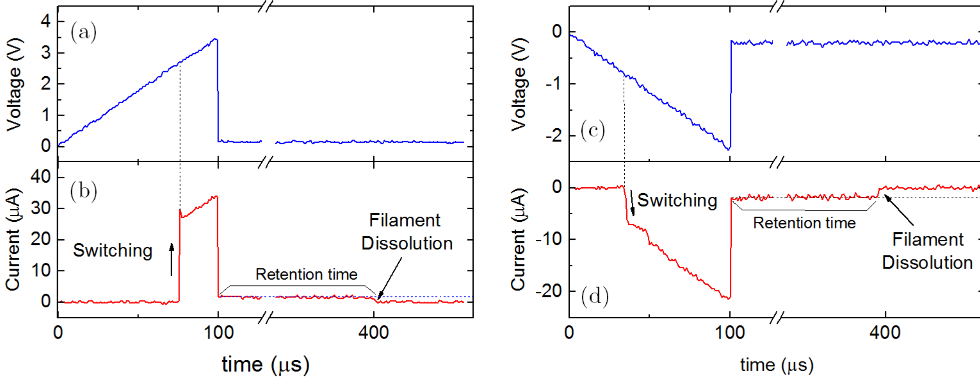


Figure 4-25: Measured voltage and current during (a), (b) positive and (c), (d) negative switching/read sequence for measuring t_{RET}.

After performing more than 100 complete (positive and negative) pulse cycles in every t_P, the cumulative distribution functions of t_{RET} have been calculated. In Figure 4-26, those distributions are depicted for the positive (a) and negative (b) threshold switching showing a large statistical spread on each cumulative distribution function. Note that all positive and negative cumulative distribution functions appear truncated at both ends. Data at the end at smaller values of t_{RET} correspond to the resolution of the oscilloscope so below that value accurate information is not obtained. On the other hand, the end at higher values corresponds to those retention times equal to the maximum time length of the square pulse indicating filament has not spontaneously disrupted during that time. To easy observe the behavior of the cumulative distribution functions, median values of t_{RET} have been extracted from previous distributions and are depicted as a function of t_P in Figure 4-26(c). For both positive and negative switching, t_{RET} slightly increases between 10 μs and 100 μs with

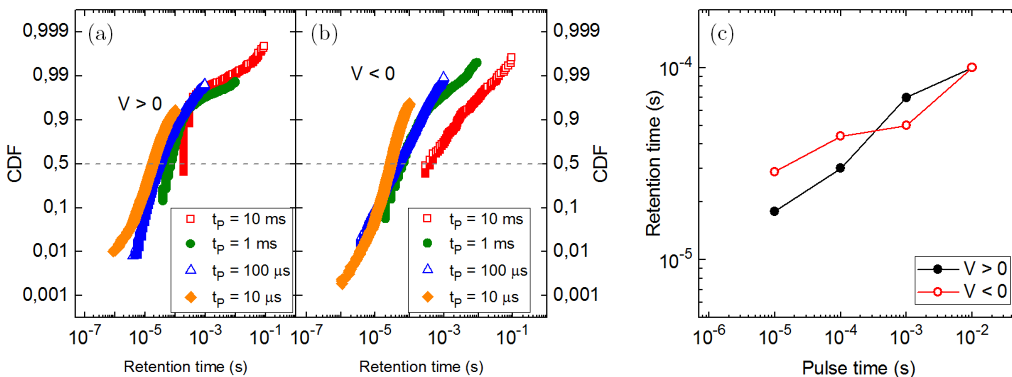


Figure 4-26: Cumulative distributions of t_{RET} for (a) V > 0 and (b) V < 0. (c) t_{RET} taken from cumulative distributions at 50 % as a function of t_P.

t_P. So far, SD behavior has been demonstrated in Ag/SiO_X-structure memristors; however, under pulsed conditions the performance is not as expected due to the large retention times observed, so reducing t_{RET} would be necessary to improve SD performance in the future.

4.4. Memory-selector one device

In spite of the issue of large retention times in previous SD devices, the performance of the combination of a SiO_X-based selector device with a SiO_X-based memory device has been demonstrated. Figure 4-27 shows a sketch of the mentioned combination formed by one-selector one-resistor (1S1R) structure. Additionally, a transistor (1T) is also included in the whole 1S1R device to control the limit of the current through the device. The functionality of the structure is shown in Figure 4-28 where experimental I-V curves are depicted. When a positive voltage is applied over the 1S1R structure, the switching of the selector is provoked first (1). With the selector at LRS state and therefore allowing the pass of current, the set process of the memory device (2), reaching the current limit (I_C = 5 μA), is provoked while applied voltage is still increased. Now, both the selector and memory devices are at LRS. If the applied voltage is gradually decreased to zero, the selector switching to HRS occurs (3) whereas memory device remains at LRS state. Subsequently, if negative voltage is applied, the switching of the selector is also provoked (4), followed by a rapid increase of the current because of the memory device is at LRS. After that, the gradual reset process of the memory device starts (5). Finally, after reset process ends, the applied voltage is reduced to zero observing again the switching to HRS of the selector device (6).

In brief, the addition of a selector device in a memory cell allows having a memristor compatible switch to avoid, for instance, write/read errors in crossbar arrays. Below a certain voltage (~ V_T), the selector does not allow the current to flow through the

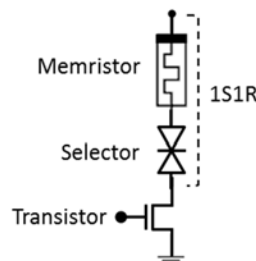


Figure 4-27: Schematic illustration of the 1S1R structure under study.

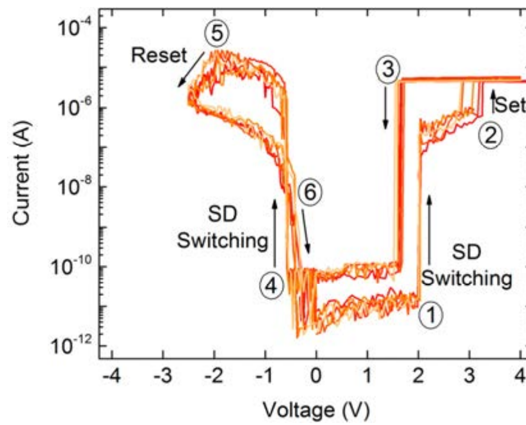


Figure 4-28 Measured I-V curves indicating separate biderectional threshold switching of SD and bipoalr resistive switching of RRAM.

structure, consequently the set/reset process of the memory device cannot take place. However, when the applied voltage is larger than that certain voltage, the selector at LRS allows the current to flow through the whole 1S1R structure. Increasing the applied voltage, set/reset process of memory device can occur.

4.5. Conclusions

Along this chapter, the feasibility in memory (RRAM) and selector (SD) applications of SiO_x-based dielectrics in combination with different top electrodes have been studied.

As memory, the Ti/SiO_X–based structure, with a dielectric thickness of 3 nm, has exhibited the best performance. On the one hand, DC characteristics have been analyzed observing a set voltage below 3 V and a resistance window controllable by V_{STOP} of four orders of magnitude for V_{STOP} = -4.5 V and I_C > 10 µA. On the other hand, studying pulsed characteristics, devices have also shown a controllable resistance window by varying V_{STOP} and a large endurance with more than 10^7 cycles where resistance window has been above one decade. Finally, by annealing the devices for an hour at increasing temperatures, devices have shown good state retention in the temperature range between 120 °C and 260 °C.

For selector application, Ag/SiO_X-based structure has shown great features such as a volatile switching with an on/off ratio larger than 10^7, bidirectional operation and stable threshold and holding voltages, everything under DC conditions. The necessity of a positive forming to observe bidirectional threshold switching in those devices has been also observed. Additionally, it has been studied the influence of I_C on SD

working concluding that for current limits below 80 µA volatile switching is achieved whereas for larger current limits nonvolatile switching is observed. Threshold switching has been also analyzed under pulsed conditions observing an increase of both positive and negative threshold voltages with t_P as well as the increase of the filament retention time also with t_P.

Eventually, the operation of SiO_X-based RRAM and SD combination, forming the 1S1R structure, has been demonstrated for a few cycles of bidirectional threshold switching and bipolar resistive switching.

5. Memristors in logic circuit applications

One of the most innovative and interesting application, in which the use of memristors has been also proposed, is in data computing. Memristors introduce a new paradigm to implement logic computing, not based on the traditional Von Neumann architecture where the data are separately stored in memory and processed in a processor, but combining both tasks in the same structure.

In this framework, the use of material implication (IMP) has been proposed to implement adders, multipliers [84], [136], [137] and other type of logic circuits such as the IMPLY gate, mentioned in the introduction chapter, [82], [138]. Despite that, a few of those works have been related with experimental measurements using real memristor devices with the consequent lack of experimental demonstrations observed in the literature. Furthermore, very few works have barely covered what happens in the memristors of the IMPLY gate during operation [18]. Therefore, a thorough experimental investigation of the gate transient is necessary to better know the behavior of IMPLY gate. This study would allow improving material implication performance.

In this chapter, an experimental verification of the IMPLY gate is demonstrated by using HfO_2-based manufactured devices. In addition, since NAND gate can be implemented by IMPLY operations, as commented in the introduction chapter, an IMPLY-based NAND gate is also experimentally demonstrated. Operation of NAND gate is typically based on two IMPLY operation steps, however a different procedure to perform the NAND gate operation consisting in one IMPLY operation step is proposed and experimentally demonstrated. In addition, an analysis of the transient of the IMPLY operation in all the gate cases is eventually carried out in this chapter.

5.1. Description of IMPLY and IMPLY-based NAND gates

In this section, IMPLY and IMPLY-based NAND gates will be briefly described by means of their equivalent circuit and truth tables.

5.1.1. IMPLY gate

Although an introduction to the IMPLY gate was done in chapter 1, here a more complete description will be presented. Equivalent circuit of the IMPLY gate is shown in Figure 5-1. Such a gate is formed by two memristors, P and Q and a series resistor (R_G) connected between ground and the bottom electrodes of both memristors. According to [80] the value of this resistor must be in between the two resistance state values of the memristors, i.e. LRS<R_G<HRS. The use of two memristors with two resistance states allows performing four digital operations as indicated in the IMPLY truth table (Table 5-I). In this table, the initial states of P and Q, as digital states, correspond to the inputs of the gate while the final state of Q (Q(out)) represents the output of the gate. From the four IMPLY cases, a change of Q state is only observed in case 1, which is initially at “0” and after IMPLY operation the memristor must be at “1”. On the contrary, in the rest of the cases the final state of Q is the same than the initial. Although not included in the table, the final state of P must be equal to its initial state in all the cases.

To perform IMPLY operations, memristors P and Q are biased by V_P and V_Q voltages, respectively. Applying adequate voltage values to V_P and V_Q, all the truth table can be accomplished. The voltage value applied to V_Q, named V_{IMPLY}, must be typically $V_{IMPLY} > V_{SET}$ to carry out the Q state change in case 1 and at the same time keep the initial state of such a memristor in other cases. On the other hand, the

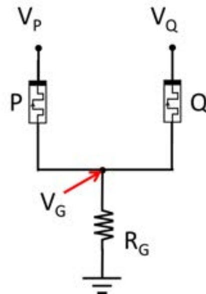


Figure 5-1: Schematic circuit of IMPLY gate. Two memristors (P and Q) and a resistance (R_G) form such a gate.

Table 5-I: IMPLY truth table

CASE	P	Q	Q (out)
1	0	0	1
2	0	1	1
3	1	0	0
4	1	1	1

voltage value of V_P, named V_{COND}, must be $V_{COND} << V_{SET}$ to not provoke any change on the state of P. These two voltages values are exactly the same to perform all the four IMPLY cases. Mention that V_{IMPLY} and V_{COND} values will depend on the memristors used to implement the IMPLY gate.

The common procedure to carry out an IMPLY case consists of an initialization step where memristors are switched to required initial states. Then, applying V_{IMPLY} and V_{COND} to memristors Q and P, respectively, the IMPLY operation is performed. Eventually, the final memristors states are checked to corroborate the well-working of the gate. Memristors states can be measured because of the voltage at the node where memristors and R_G are connected (labeled as V_G) is monitored to calculate the actual voltage drop across every memristor.

As an example, to perform the case 1, both devices must be initially at “0” logic state, i.e. at HRS, then, corresponding RS processes are provoked. Once at required states, applying proper voltages V_{COND} and V_{IMPLY}, Q state is changed to “1” (LRS) because the voltage drop across it is enough to provoke the required resistance change (concerning RS phenomenon, a set process is provoked). On the contrary, P remains unaltered keeping “0” logic state since its voltage drop is below the voltage necessary to originate a resistance state change. Regarding other three cases of the IMPLY, no state change is provoked in any of the memristors. However, applying the same operational voltage values (V_{COND} and V_{IMPLY}) in all the cases, the IMPLY truth table (Table 5-I) is perfectly accomplished.

5.1.2. IMPLY-based NAND gate

Apart from being a logic gate itself, IMPLY gate is also a basic gate which allows implementing other logic gates as NAND gate for instance. Figure 5-2 shows the equivalent circuit of such a gate based on the IMPLY gate. Its structure is similar to the IMPLY gate with a third memristor (named S), biased with V_S, added to P and Q involved in the IMPLY gate [138]. In this case, the inputs of the gate are the states of P and Q whereas the output is stored in the state of S.

As IMPLY gate, the combination of two inputs with two possible logic values (“0”

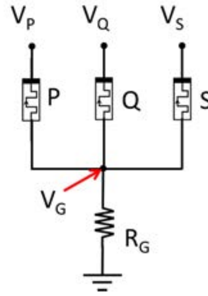


Figure 5-2: Schematic circuit of an IMPLY-based NAND gate. Now three memristors are used (P, Q and S) and therefore three voltages (V_P, V_Q and V_S) are applied to perform every NAND case.

and "1") leads to a four different NAND cases which are shown in the truth table of the NAND gate in Table 5-II. To carry out a NAND case, first of all, memristor S must be always initialized to "0" logic state. Then, P and Q are initialized as required in each case. Once the three memristors are initialized, NAND operations can be performed by applying the adequate V_P, V_Q and V_S. Unlike IMPLY gate, every case of this NAND gate is performed in two IMPLY operation steps because three memristor are involved. First IMPLY operation step takes place between P and S. Then, the second IMPLY operation steps occurs between Q and S. Finally, memristor states, where the final state of S corresponds to the output of the gate, are checked. Again, the voltage at the connection node, V_G, is also monitored to calculate the actual voltage drop across memristors and to obtain their resistance states.

Figure 5-3 shows the schematic of the sequence followed to accomplish every NAND case. As an example, in case 2, after the first initialization of S to "0", P is initialized to "0" state whereas Q is initialized at "1" state. Then, the first IMPLY operation step takes places between P and S applying the required voltages. Under these conditions, S state changes from "0" to "1" while P state remains unchanged. Therefore, the case 1 of IMPLY gate has been initially accomplished between P and S (see Table 5-I). Now, the new state of S (called S') is used together with Q state to perform the second IMPLY operation step. Since initial states are now "1" for both memristors, Q and S', the case 4 of an IMPLY gate (see Table 5-I), where the

Table 5-II: IMPLY-based NAND truth table.

CASE	P	Q	S	S (out)
1	0	0	0	1
2	0	1	0	1
3	1	0	0	1
4	1	1	0	0

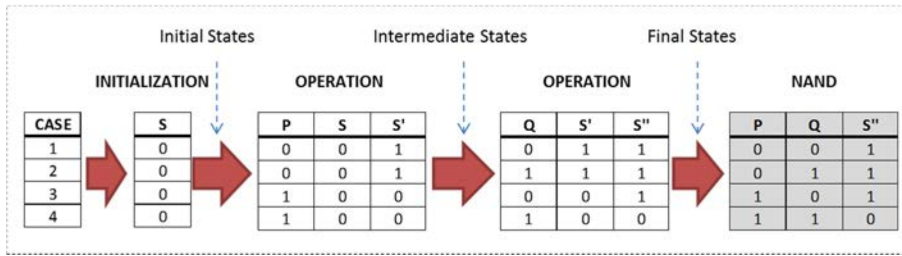


Figure 5-3: Schematic sequence flow for NAND cases performin where two IMPLY operation steps are involved. Initial, intermediate and final states steps indicate where memristors states are checked.

output is the state of S (called now S''), is now carried out. Eventually, the final state S'', which is the "1" logic state, corresponds to the output of the IMPLY-based NAND gate what indeed verifies that the case 2 of such a gate has been performed.

5.2. Memristor as digital element

To analyze the use of memristors for logic applications, the same devices as those presented in chapter 3 has been used. They are MIS structures with a Ni top electrode layer with a thickness of 200 nm, a 20 nm-thick high-k dielectric HfO_2 and a semiconductor bottom electrode of Si ($Ni/HfO_2/Si$). The area of such structures has been 5x5 μm^2. A schematic cross-section of an individual memristor structure is shown in Figure 5-4.

Relation between RS parameters and typical logic parameters is explained by the Figure 5-5, where typical I-V characteristics of the memristors used to implement IMPLY gate are depicted. Common RS parameters such as voltages at which samples change from HRS to LRS (V_{SET}) and from LRS to HRS (V_{RESET}) and currents at LRS (I_{LRS}) and at HRS (I_{HRS}) are indicated. A memristor can switch between two different resistance states (HRS and LRS) repeatedly. Considering HRS and LRS as

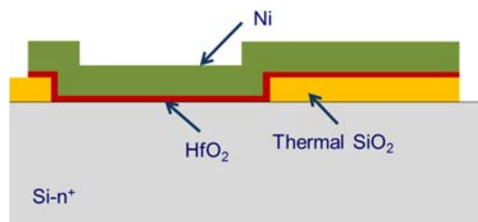


Figure 5-4: Cross-section of the memristor device used in this work.

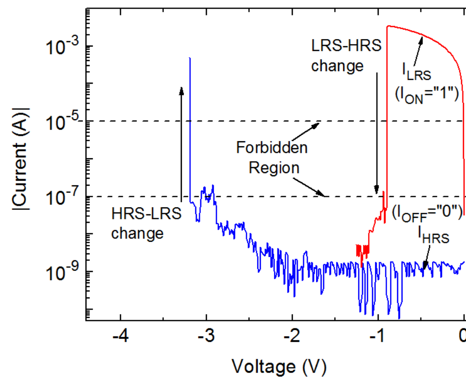


Figure 5-5: Typical I-V characteristic of the memristors used in this chapter. Voltage polarity to provoke Set and Reset processes is negative.

the logic states “0” and “1”, respectively, the resistance of the memristor can be considered as the physical variable to perform digital operation instead of voltages. When memristor is at HRS (see Figure 5-5), the conductive filament connecting bottom and top electrodes is partially (or completely) disrupted, so low (or no) current is flowing. In this situation memristor is operating in a cutoff-like region, current in this state is labeled as I_{OFF} and this state can be, then, associated to the “0” Boolean value. On the contrary, when memristor is at LRS (Figure 5-5) a significant current flow is allowed since the conductive filament is formed and connects both electrodes. Now the current in this states is relabeled as I_{ON}. Consequently, this state can be associated to the Boolean value “1”. Despite resistance states of the memristors have been initially associated to digital Boolean values, in this work, the values of I_{OFF} and I_{ON} currents have been considered as the “0” and “1” logic states, respectively, for simplicity. Finally, to perfectly separate I_{ON} and I_{OFF} states a forbidden region of two orders of magnitude (below 10^{-7} A memristor is at I_{OFF} and above 10^{-5} A it is at I_{ON}) has been defined as shown in Figure 5-5.

5.3. Experimental verification of the IMPLY and NAND gates based on HfO_2 devices

Experimental verification of the IMPLY and IMPLY-based NAND gates will be presented as well as a cycling measurement of more than 500 cycles of NAND cases.

5.3.1. Experimental procedure conditions

Initially, the memristors have been subjected to approximately 20 initial RS cycles, consisting in a first forming set (where the filament is firstly created). Then, the

successive changes between LRS and HRS have been performed in order to achieve a stable behavior of the conductive filament in its creation/disruption process. To carry out the RS measurements, only negative voltages has been used to trigger set and reset processes since, in these devices, negative unipolar operation gives the best endurance results of the RS phenomenon as demonstrated in [118], [119]. More than 3000 cycles of negative switching can be reached [118].

To perform both IMPLY and IMPLY-based NAND, a constant voltage has been applied to each memristor. To check the memristor state, the current through the device has been registered by applying a small voltage ramp from 0 V to -0.8V over the top electrode and grounding the bottom. The state is determined by obtaining the current at a certain voltage value. A SPA Agilent 4156C has been used to apply the required voltages and also to register the current through samples thanks to the use of SMUs. The current limit, which has been 250 µA during IMPLY and NAND operation, has also been applied by the SPA. To perform all the measurements, a script for every specific experiment has been developed in MATLAB software environment using GPIB commands communication.

5.3.2. IMPLY gate

For the IMPLY experimental verification, the circuit shown in Figure 5-1 has been implemented using the memristors presented in section 5.2 and a resistor $R_G = 1$ MΩ. Firstly, one of the cases from 1 to 4 of the truth table (Table 5-I) has been chosen. Then, memristors P and Q have been initialized to the states corresponding to the selected case, that is “0” (memristor at HRS) or “1” (memristor at LRS). Once memristors have been correctly initialized, IMPLY operation step has been performed so required voltages (V_P and V_Q) have been applied to change Q state (for case 1) or to keep the initial Q state (for other cases). Operational voltages applied to memristors do not depend on the considered case i.e. they must be the same whatever the case. For these devices, voltage applied to P has been $V_P = V_{COND} = -2$ V and that applied to Q was $V_Q = V_{IMPLY} = -4$ V. Checking initial and final memristors states has been carried out before and after the operation step, respectively.

Figure 5-6 shows the experimental verification of the four IMPLY cases, where memristors currents at initial and final states are depicted (from top to bottom, case 1 to case 4). Logic state “0” and “1” are indicated in every current state for an easier identification. As initially indicated, the states of memristors P and Q, before (initial states) and after (final states) operation step, are shown in terms of the current flowing through them (their resistances states can be obtained by Ohms law) in order to facilitate the interpretation of “0” (low current) and “1” (high current)

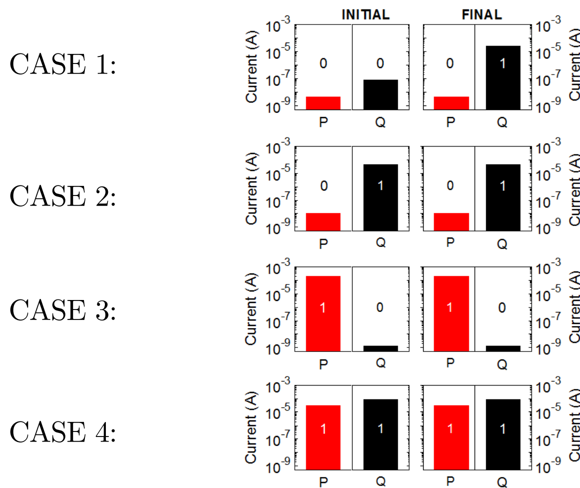


Figure 5-6: Experimental verification of IMPLY gate where initial and final states of memristors P and Q involved in the IMPLY logic gate are shown. Q final state corresponds to the output of the gate.

logic states. The figure shows a perfect accomplishment of the whole IMPLY truth table (Table 5-I). After applying V_P and V_Q voltages to the memristors in the initial state, Q state changes correctly from “0” initial state (HRS) to “1” final state (LRS) in case 1 and remains at the initial logic state for the rest of the cases. The final state of P is also included to corroborate that this input is kept unchanged as it should and the IMPLY operation has been performed completely.

5.3.3. IMPLY-based NAND gate

For the experimental verification of IMPLY-based NAND gate, the circuit shown in Figure 5-2 has been used with $R_G = 1$ MΩ. Following the measurement procedure shown in Figure 5-3, the three memristors conforming the NAND gate have been properly initialized. Then, to perform the first IMPLY operation step between P and S, operation voltages $V_P = V_{COND} =$ -2 V and $V_S = V_{IMPLY} =$-4 V have been applied. Once the required S state is reached (S’), subsequently, the second IMPLY operation step between Q and S (at S’ state) has been carried out by applying the same voltages values as in the previous step $V_Q = V_{COND} =$ -2 V and $V_S = V_{IMPLY} =$ -4 V. Latter step has led S to reach the final state S’’ which corresponds to the output of NAND gate. Experimental verification of the four NAND cases is shown in Figure 5-7 where initial and final states are depicted for each memristor (corresponding logic states, “0” and “1”, are also indicated to facilitate the comparison with truth table). The final state of S, after the first operation step, i.e. S’ (intermediate), is included to

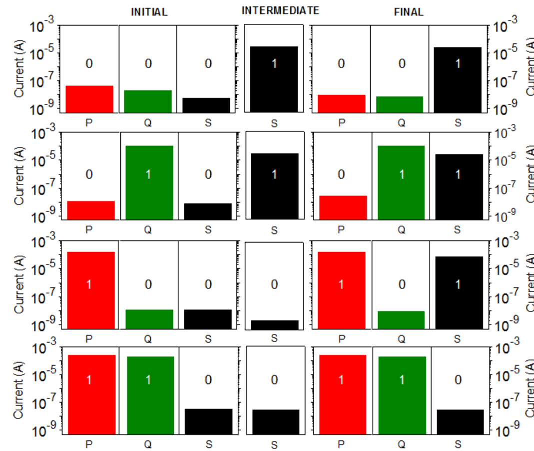


Figure 5-7: NAND implementation with two IMPLY operation steps. The first one is between memristors P and S with the output state stored in S (S'). The second IMPLY operation is between Q and S, being the initial state of S the output of the previous IMPLY operation. S state (S') after the first step is included to verify that the first IMPLY operation is well-performed. Final state of S (S'') is the output of NAND gate.

confirm that this first IMPLY operation step between P and S has been successfully performed. Comparing the experimental results in that figure with the NAND truth table (Table 5-II), the experimental verification of an IMPLY-based NAND gate is effectively accomplished.

In addition to the experimental verification of the single NAND cases, sequential repetitive measurements of the four NAND cases have also been performed in order to analyze if a NAND gate consisting of the memristors described in section 5.2 can perform a cycling of digital operations. To do that, a specific developed measurement script has been used. Firstly, a random selection of the case number has been performed. Then the same measurement procedure presented in Figure 5-3 has been followed: the initialization of memristors, both IMPLY operations applying exactly the same operations voltages and the checking of the final states. Once individual case has been accomplished, a new NAND case has been randomly chosen and the experimental procedure just mentioned has been followed again. The cycling measurement has been performed until one of the memristors did not work anymore due to its complete dielectric breakdown. Figure 5-8 shows the results obtained from a measurement of almost 500 cycles overall which are distributed to each NAND case since every cycle corresponds to one gate case. As in previous figures, initial and final states of the memristors P, Q and S are shown for successful cycles of each of the four NAND cases. As in Figure 5-7, intermediate S state (S') is included to corroborate that the first IMPLY operation step occurs successfully. In this cycling measurement, a cycle-to-cycle variability on the device states is observed. However,

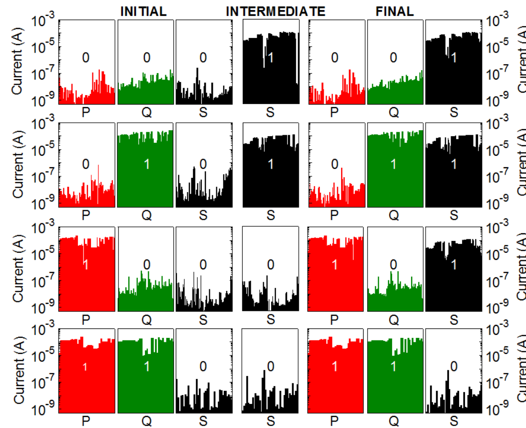


Figure 5-8: Cycling of all the NAND cases with two IMPLY operation steps. Intermediate state of S is included to show that the first operation step was made correctly.

the operation is still valid since currents when "0" are mostly below 10^{-7} A and currents when "1" are above 10^{-5} A what indicates that the forbidden region margins have been complied.

So far, IMPLY and IMPLY-based NAND logic gates have been experimentally demonstrated using HfO_2-based memristors and following standard procedures [138]. Furthermore, random cycling measurement of NAND cases has been also performed. In the next section, the measurement sequence for NAND gate is modified by reducing the number of operation steps to only one which might have some advantages, as for instance, reducing the operation time.

5.4. A modified NAND procedure operation

A modified NAND operation procedure is propose in this section. Initially, a circuit analysis is done to demonstrate the feasibility of one-operation step NAND based on memristors. To do that, the voltage at the connection node, V_G, is calculated analytically for each case what allows evaluating voltage drop across every memristor. Then, the functionality of this proposed procedure is proved experimentally performing all the four cases of the NAND gate.

To perform all the measurements, the proposed one-operation step sequence is graphically shown in Figure 5-9. Firstly, all memristors are initialized to the states indicated in the truth table (Table 5-II). Later, the unique operation step is carried out for each NAND case by applying adequate V_P, V_Q and V_S simultaneously. Note that one-operation step NAND gate is not strictly an IMPLY-based gate since an IMPLY case between only two memristor does not take place but a semi-IMPLY

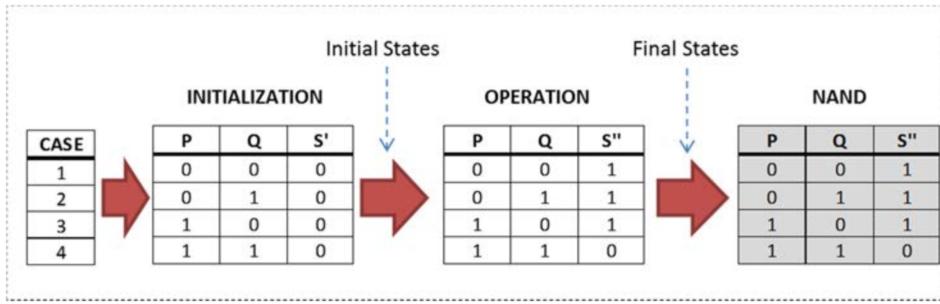


Figure 5-9: Schematic flow sequenceof the procudure to perform the IMPLY-based NAND logic gate. In this procedure, only one operation step is needed.

case involving three memristors is performed in almost all the cases for the proposed gate. For instance, in cases 1 and 3 the IMPLY case 1 is performed between Q and S although P is also involved in the operation. However, in case 2 the same IMPLY case 1 is carried out between P and S instead. On the contrary, in case 4 none IMPLY case is accomplished during operation. Unlike IMPLY-based NAND experiments, an additional operation voltage value is involved since all the memristors must be biased at the time. Now, the operation voltages are V_{COND1}, V_{IMPLY} and the new included V_{COND2} which is related to other voltages as $V_{COND2}>V_{COND1}$ and $V_{IMPLY}>V_{COND2}$.

5.4.1. Circuit analysis and feasibility

Considering the circuit shown in Figure 5-2, every memristor behaves as an individual resistance with two different values. These two values are labeled as R_{OFF} (related to I_{OFF} indicated in Figure 5-5) when memristor has a high resistance value, which means “0” logic state, and R_{ON} (related to I_{ON} indicated in Figure 5-5) when memristor has a low resistance value corresponding to “1” logic state. Then, considering the three memristors as the resistances R_P, R_Q and R_S, the voltage at the node, V_G, can be described by equation 5-1 by applying Kirchhoff's current law to the circuit.

$$V_G = \frac{R_G \cdot R_Q \cdot R_S \cdot V_P + R_G \cdot R_P \cdot R_S \cdot V_Q + R_G \cdot R_P \cdot R_Q \cdot V_S}{R_P \cdot R_Q \cdot (R_S + R_G) + R_G \cdot R_Q \cdot (R_S + R_P)} \qquad 5\text{-}1$$

In the equation, V_P, V_Q and V_S correspond to the voltages applied to P, Q and S, respectively, and to the series resistor R_G. Equation 5-1 is a general expression, so as to know V_G expression for a specific case, resistances R_P, R_Q and R_S must be substituted by R_{OFF} or R_{ON} values depending on the initial states indicated in

Table 5-II. Following, the expression of V_G will be calculated for every NAND case as well as suitable values of V_P, V_Q and V_S that allow implementing the NAND case in only one operation step.

CASE 1

In the case 1, NAND truth table (Table 5-II) indicates that the initial resistance values of memristors P, Q and S must be R_{OFF} ("0" logic state). At the end, NAND operation requires S resistance must change to R_{ON} whereas resistance of P and Q must remain unchanged. Then, applying the voltage V_{COND1} to P and Q V_{IMPLY} to S, only S should change its resistance state since $V_{IMPLY}>V_{COND1}$. Considering initial resistance values and applied voltages values just mentioned, substituting this values in the expression 5-1 and simplifying, the equation 5-2 is obtained. Considering that the value of R_G should be $R_{ON}<R_G<R_{OFF}$ with at least one order of magnitude difference between R_{ON} and R_G and between R_G and R_{OFF}, V_G would be negligible.

$$V_G = \frac{R_G \cdot V_{IMPLY} + 2 \cdot R_G \cdot V_{COND1}}{R_{OFF} + 3 \cdot R_G} \approx 0 \qquad \text{5-2}$$

Since $V_G \sim 0$ and voltage drop across memristors P, Q and S can be calculated as V_X-V_G (being V_X the applied voltage at the top electrode of each memristor), the voltage drop across P and Q would be approximately the applied voltage V_{COND1}, and across S almost V_{IMPLY}. This provokes the S resistance change from R_{OFF} ("0") to R_{ON} ("1"), while P and Q remain at R_{OFF} ("0").

CASE 2

Now, resistances of P, Q and S must be R_{OFF}, R_{ON} and R_{OFF} respectively and, as in case 1, S resistance must change to R_{ON}. Now, applying the voltage V_{COND2} to P and Q and V_{IMPLY} to S, again only latter memristor should change its state. As in previous case, initial resistance values of the three memristors as well as the applied voltages values are introduced in equation 5-1 to obtain V_G in this particular scenario. Equation 5-3 gives the V_G expression for this case. Taking into account the relation between memristor resistance values ($R_G<R_{OFF}$ and $R_{ON}<< R_{OFF}$), V_G would be also negligible. Thus, voltage drops through P, Q and S are V_{COND2}, V_{COND2} and V_{IMPLY}, respectively, (with $V_{IMPLY}>V_{COND2}$) only provoking the change of the S memristor resistance from R_{OFF} to R_{ON} and getting the expected gate output. As expected, P and Q would remain at the same initial state because V_{COND2} is not enough to provoke any state change.

$$V_G = \frac{R_G \cdot R_{ON} \cdot V_{IMPLY} + (\mathrm{R}_G \cdot \mathrm{R}_{ON} + \mathrm{R}_G \cdot \mathrm{R}_{OFF}) \cdot \mathrm{V}_{COND2}}{(R_{OFF} + 2 \cdot R_G) \cdot \mathrm{R}_{ON} + \mathrm{R}_G \cdot \mathrm{R}_{OFF}} \approx 0 \qquad \text{5-3}$$

CASE 3

Similar scenario occurs in case 3. Memristors P and Q are supposed to be interchangeable since they are always the inputs and never the output of the gate. Therefore, considering now initial states as $R_P = R_{ON}$, $R_Q = R_{OFF}$ and $R_S = R_{OFF}$, V_G has the same expression than the equation 5-3. Evaluating in the same way, voltage drops across memristors, considering $V_P = V_Q = V_{COND2}$ and $V_S = V_{IMPLY}$, are the same as in case 2, reaching the required final state of S (R_{ON}) and keeping final states of P and Q unchanged (R_{OFF}).

CASE 4

Finally, in case 4, initial states of P, Q and S must be equal to R_{ON}, R_{ON} and R_{OFF}, respectively. In this case, the state of S must not change, therefore, despite applying V_{IMPLY} voltage, S should remain at R_{OFF}. Here, the voltage applied to P and Q should be V_{COND1} and V_{IMPLY} to S. Then, substituting resistance and voltage values in equation 5-1 and, subsequently, simplifying that equation V_G would be described by the expression in equation 5-4.

$$V_G = \frac{R_G \cdot R_{ON} \cdot V_{IMPLY} + 2 \cdot R_G \cdot R_{OFF} \cdot V_{COND1}}{(\mathrm{R}_{OFF} + \mathrm{R}_G) \cdot \mathrm{R}_{ON} + 2 \cdot \mathrm{R}_G \cdot \mathrm{R}_{OFF}} \approx V_{COND1} \qquad \text{5-4}$$

In this case, voltage drops at the memristors differ from the rest of cases. In both memristors, P and Q, the voltage across them are zero, while across S is V_{IMPLY}-V_{COND1}<V_{IMPLY} what should not change the state of S. Hence, under this situation all memristors maintain its initial state value and case 4 is accomplished.

From the circuit analysis, the NAND truth table (Table 5-II) can be obtained in a single operation step by choosing the adequate applied voltages values. In the following section the experimental demonstration is presented.

5.4.2. Experimental verification

To perform experimentally the one-step NAND gate, the operation voltages V_{COND1}, V_{COND2} and V_{IMPLY} must be selected. After individually performing each case of NAND gate under different applied voltages, finally, the values that allow successfully performing all the NAND cases have been 0 V, -2 V and -4 V for V_{COND1}, V_{COND2} and V_{IMPLY}, respectively. The combination of these voltages for each case of NAND gate is shown in Table 5-III where voltages applied to memristor P, Q and S are indicated. As aforementioned, the three voltages are applied simultaneously to the memristors in order to perform the corresponding cases. Note that a third operational voltage is required in comparison to the IMPLY or IMPLY-based NAND gates, but the value

Table 5-III: Experimental voltages applied simultaneously to the nand circuit to provoke the different cases of the nand output in only one operation step.

CASE	V_P (V)	V_Q (V)	V_S (V)
1	-2	-2	-4
2	0	0	-4
3	0	0	-4
4	-2	-2	-4

of this additional voltage (0 V) can be considered as ground.

To perform the experimental verification of NAND gate with only one operation state the circuit shown in Figure 5-2 has been used with the same value of R_G (1 MΩ) as in the IMPLY and the IMPLY-based NAND cases. After applying the voltage values included in Table 5-III, experimental NAND results are presented in Figure 5-10. In the figure, initial and final memristor current states are depicted for all NAND cases. Note that the intermediate S state (shown when two sequential steps were required, Figure 5-7) are not included. These results indeed demonstrate that memristor-based NAND operation is possible using just one step. For all the cases, initial and final states are well accomplished as truth table (Table 5-II) requires.

A cycling measurement has also been done consisting in performing a random cycling case measurement of the one-operation step NAND gate. Figure 5-11 shows initial and final memristors states for all NAND cases after more than 200 successful cycles.

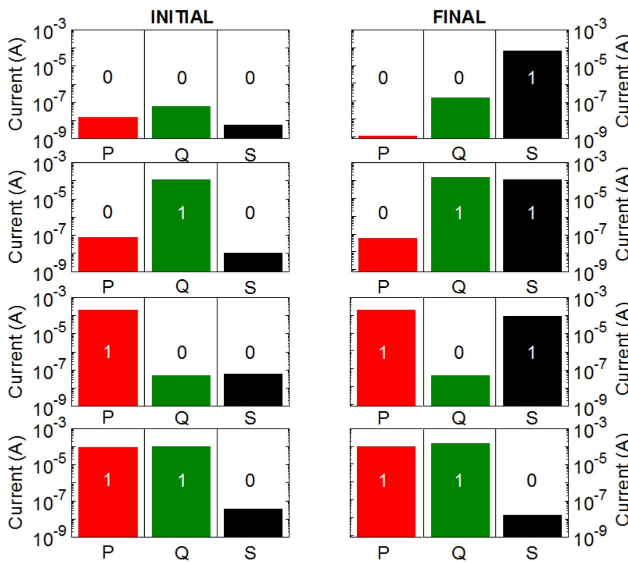


Figure 5-10: NAND implementation with only one operation step.

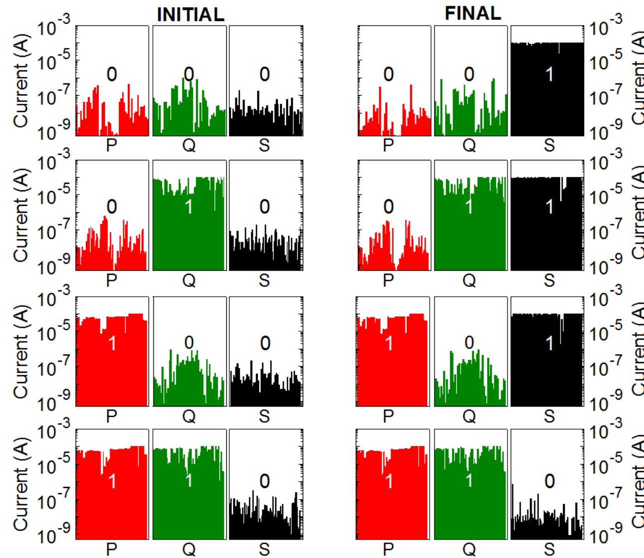


Figure 5-11: Random cycling cases of NAND gate with only one operation step.

Despite current state variability is observed in all the cases, sequential working of NAND gate with only one operation step is well achieved.

5.5. Analysis of the transient response of the memristors during IMPLY operation step

A thorough study of what happens in the memristors of the IMPLY gate during the gate operation ca be helpful for a better understanding of the IMPLY gate behavior. However, a very few works have been interested in studying the evolution of memristors state while operation voltages are applied as for example in [82] where the evolution of SiO_X-based memristors currents are presented. Consequently, a transient analysis of the IMPLY gate showing the time evolution of the currents and voltage drops across both memristors, P and Q, is presented. Furthermore, the impact of R_G on the gate functionality is discussed.

5.5.1. Experimental procedure conditions

Similarly to section 5.3, the experimental procedure has consisted in a first measurement where the memristors have been subjected to approximately 20 initial RS cycles applying negative voltages. Afterward, every IMPLY case has been performed by initializing the memristors to required initial state, then, carrying out the IMPLY operation applying the corresponding voltage values and finally

measuring the final state of the memristors. To measure both initial and final memristor states, a small voltage ramp from 0 V to -0.8 V has been applied to the top electrode of the memristor with the bottom grounded. In order to perform the IMPLY operations and measure memristors behavior during IMPLY operation, simultaneous voltage ramps, from 0 V to -2 V and from 0V to -4 V, have been applied to P and Q, respectively. At the same time, the current through both memristors has been registered by the SPA using the SMUs. In addition, the voltage V_G has also been monitored to obtain the actual voltage drop across the memristors. A current limit of 50 µA has also been applied by the SPA. Mention that the registered time has been estimated by the software used to perform the measurements.

5.5.2. Memristors behaviour for each IMPLY case

Transient analysis of the four IMPLY cases is presented in this section. Specifically, the behavior along time of the current through memristors and the voltage drop across them have been analyzed for every case of the IMPLY gate individually.

CASE 1

Case 1 is, probably, the most interesting case because it is the only one where a memristor state change occurs during operation step. In Figure 5-12, initial and final memristors states as well as the transient of the currents are shown. To perform this case, both memristors, P and Q, must be initialized to “0” logic state, so the current through them must be lower to 0.1 µA. Figure 5-12(a) and (d) show initial current states of Q and P, respectively. As observed, both states present current values below 0.1 µA, which indeed corroborates memristors have been well initialized to “0” state.

Once initialization has been done, the operation step is carried out by applying the corresponding voltage ramps to the memristors. Under this conditions, Q should change from “0” to “1” logic state while P should keep the same state, “0”, as truth table (Table 5-I) indicates. This means that the memristor Q should change its resistance to lower values, allowing larger current values than 10 µA, as defined previously. Figure 5-12(b) shows the transient response of the current through Q. After certain time (~ 38 s) applying the voltages, current through this memristor suffers an abrupt increase (in absolute values) reaching the established current limit. As indicated, another voltage ramp has been applied simultaneously to memristor P, while its current is also registered. Figure 5-12(e) shows the current through this memristor as a function of time. It is observed that the current barely suffers variations what keeps the initial memristor state unchanged. Initially, P is at “0” ($I < 0.1$ µA) and this state has been kept even though the increase of the applied

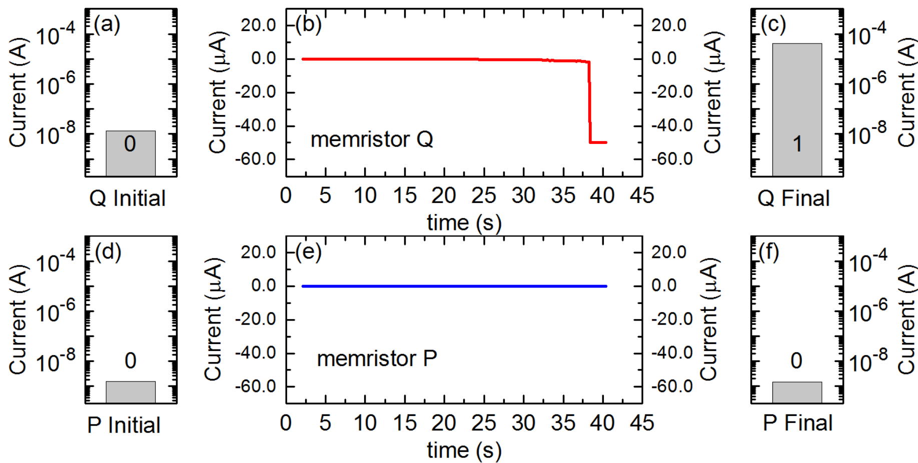


Figure 5-12: Transition between initial and final states for case 1 of the IMPLY gate, showing (from left to right) the initial (input) states of Q at "0" logic state (a) and P also at "0" logic state (d); current evolutions as a function of time of Q memristor (b) and P memristor (e) and final states of Q (output) at "1" logic state (c) and P remained at "0" logic state (f). Initial and final states were measured at -0.5 V.

voltage ramp. In the final scenario, memristors Q and P are at "1" and "0", respectively, verifying the IMPLY truth table. This is corroborated in Figure 5-12(c), and (f) where final states of Q, showing a current larger than 10 µA, and P, with a current below 0.1 µA, are depicted, respectively.

For a better understanding of current behaviors, in Figure 5-13(a) the actual voltage ramps applied to memristors P and Q (solid blue and dashed red lines, respectively) as well as V_G (solid black circles) are depicted. Programmed voltage ramps (empty blue squares and empty red circles for P and Q, respectively) are also depicted to show the difference with the actual voltage ramps due to the applied current limit. When the current through memristor Q reaches the current limit value, SPA reduces the actual applied voltage to keep the current through the memristor at the established limit value whereas the programmed voltage remains increasing up to the maximum. This behavior also affects to V_G evolution provoking this voltage also increases abruptly. These changes provokes the increase of the Q current ($I > 10$ µA) which originates a decrease of the resistance value of the memristor. Consequently, Q memristor is at "1" logic state. On the contrary, since P is initially at 0 state, its resistance is so large that almost no current can flow (I_{OFF}) and, therefore, no state change is provoked. Resistance of Q is much larger in comparison to that of the memristor P what provokes all the current from Q flows through R_G. Consequently, the IMPLY circuit shown in Figure 5-1 can be considered as a voltage divider between Q or and R_G, what makes V_G proportional to V_Q. This is the reason why after reaching the current limit V_G evolution follows the behavior of V_Q.

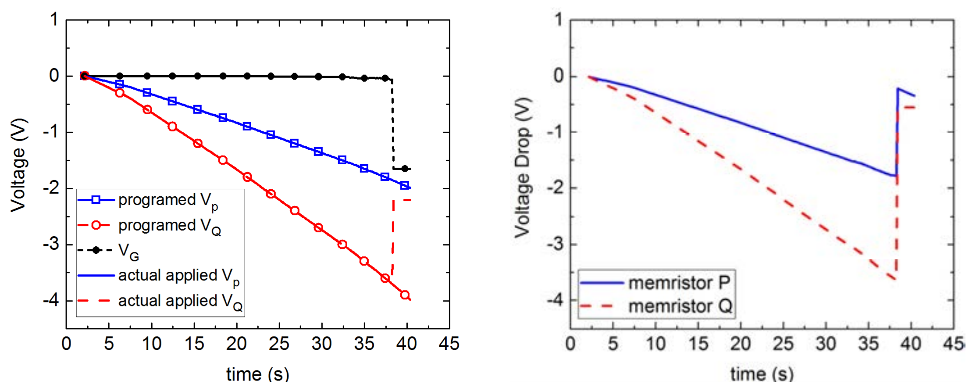


Figure 5-13: Actual voltages, applied in case 1, to P and Q top electrodes (solid blue and dashed red lines respectively), V_G (solid black circles) and programmed voltages of P and Q (empty blue squares and empty red circles respectively). All these voltages are depicted as a function of time. (b) Voltage drops at P (solid blue line) and Q (dashed red line) memristors as a function of time.

Measuring V_G allows getting the voltage drops across both memristors, P and Q, as V_X-V_G, where V_X is the actual applied voltage and X indicates P or Q. In Figure 5-13(b), those voltage drops calculated from the voltages in Figure 5-13(a) are depicted along the time. Initially, voltages drops are equal to the actual applied, then, once the Q state changes and also because of V_G changes, they decrease. At this point, P voltage drop is lower than previously to the state change and, therefore, current through P is still at low levels not altering its state. On the other hand, voltage drop across memristor Q has been forced to reach this value by the current limit applied by the SPA. So, a constant behavior is observed in V_Q after the state change.

CASE 2

For the second IMPLY case, the initial situation is different from case 1, memristor P must be initialized at “0” (I_{OFF}) whereas Q at “1” (I_{ON}). Figure 5-14(a) and (d) show the initialized current state of Q (I > 10 µA) and P (I < 0.1 µA), respectively. Unlike case 1, neither Q state nor P state should change when the voltage ramps are applied to them. Figure 5-14 (b) and (e) show the transient response of the current through the Q and P, respectively. As the voltage ramp is applied to Q, the current through it quickly increases (the memristor Q is at “1” state) until, finally, reaching the defined current limit. Due to the current limit and the maximum value of the voltage ramp, Q has maintained its state at “1” as demonstrated in Figure 5-14(c) where final Q current state is depicted. At the same time, a current below nanoamperes range is flowing through memristor P, when the corresponding voltage ramp is applied. From the transient response of the current shown in Figure 5-14(e), no current changes are observed what indicates the state of this memristors have not

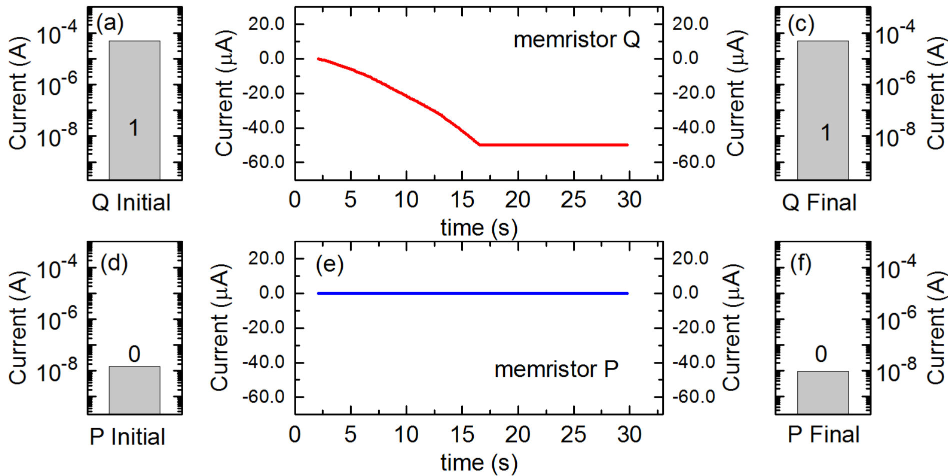


Figure 5-14: Transition between initial and final states for case 2 of the IMPLY gate showing (from left to right) the initial (input) states of Q at “1” logic state (a) and P at “0” logic state (d); current evolutions as a function of time of Q memristor (b) and P memristor (e) and final states of Q (output) at “1” logic state (c) and P at “0” logic state (f). Initial and final state currents were measured at -0.5 V.

changed. This is corroborated in Figure 5-14(f) where final P current value below 0.1 µA is observed verifying the memristor is still at “0”.

All the voltages have also been registered along the time. Figure 5-15(a) shows the actual voltage applied to P and Q (continuous blue and dashed red lines), the programmed voltages (empty blue squares and empty red circles) and the monitored V_G (solid black circles). The difference between applied and programmed voltages in Q is now more noticeable. Although an abrupt reduction of the applied voltage is not observed because Q does not change its resistance, V_Q is varied when current limit is reached (after ~ 15 seconds) being constant at approximately -2.3 V to control the current flowing through Q memristor. Now, the situation is similar to the one after the abrupt current change of Q current in case 1 when the current limit was reached. Due to the divider circuit configuration, V_G follows V_Q behavior again whereas V_P has not suffered any variation since the current through P is very low.

Different behavior is observed in the voltage drops across memristors depicted in Figure 5-15(b). Voltage drop across memristor Q (dashed red line) remains almost constant since V_G and V_Q has similar transient evolution. However, the voltage drop across P (solid blue line) changes its polarity a couple of times because V_G crosses V_P at time 3 s and 25 s. The inset in Figure 5-15 corresponds to a zoom of the first 7 seconds and has been included to better distinguish the first polarity change. Despite these changes, absolute value of P-current value is always below 0.1 µA since the voltage drop is kept low, independently of the polarity.

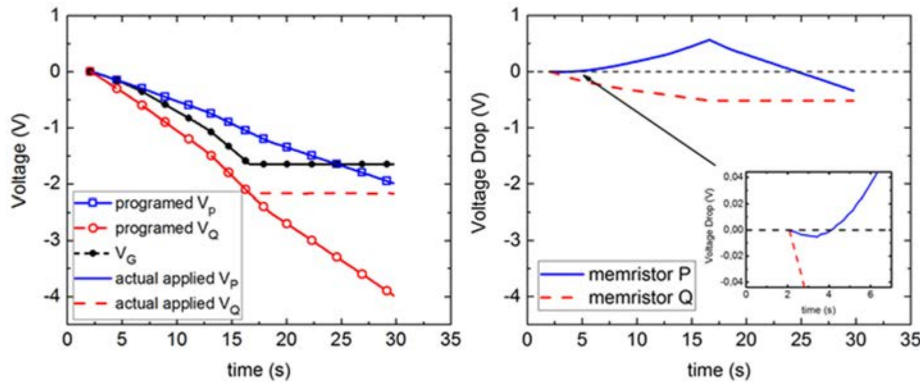


Figure 5-15: (a) Actual voltages applied to P (continuous blue line) and Q (dashed red line) top electrodes, V_G (solid black circles) and programmed voltages of P (empty blue squares) and Q (empty red circles) memristors depicted as a function of time. (b) Voltage drops across P (solid blue line) and Q (dashed red line) as a function of time. Inset is a zoom of the region pointed out by the arrow where the polarity of P voltage drop changes.

CASE 3

Case 3 seems quite similar to case 2, with one memristor at "0" and the other at "1". Here memristor P is at "1" while memristor Q is at "0" as shown in Figure 5-16(a) and (d), respectively. The main difference between both cases is the larger voltage ramp is applied to the memristor at "0". Despite that, no effect on the case performance is observed. In Figure 5-16(b) and (e) the transient of the currents are

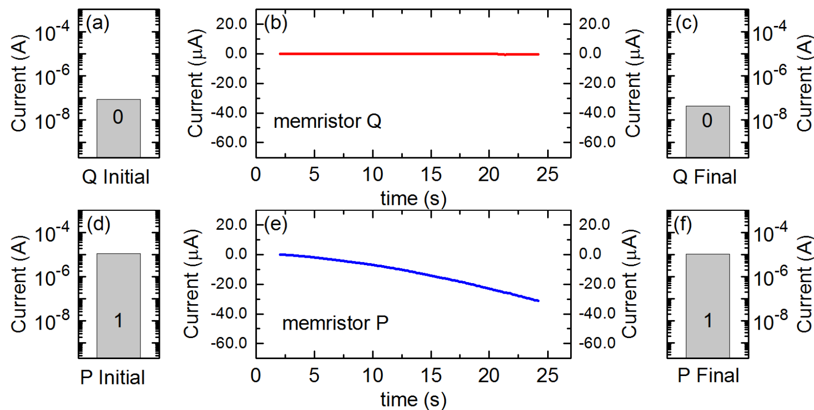


Figure 5-16: Transition between initial and final states for case 3 of the IMPLY gate showing (from left to right) the initial (input) states of Q at "0" logic state (a) and P at "1" logic state (d); current evolutions as a function of time of Q memristor (b) and P memristor (e) and final states of Q (output) at "0" logic state (c) and P at "1" logic state (f). Initial and final states were measured at -0.5 V.

depicted for Q and P, respectively. Now, the current flowing through Q is always low (< 0.1 µA) what indicates memristor Q will keep its I_{OFF} state as Figure 5-16(c) demonstrates. Despite the voltage ramp applied to Q memristor increases up to -4 V, the voltage drop across the memristors is not enough to provoke a state change due to V_G also increases. On the other hand, as voltage ramp is applied to memristor P, its current increases until high current levels since the low value of P resistance. The current never reaches the current limit due to the maximum voltage ramp value is not enough to achieve that current level. Figure 5-16(f), where final state of P is depicted, corroborates P is kept at "1" since the current at that state is I_{ON} (>0.1 µA).

To understand the transient response of P-current, in Figure 5-17(a) the actual voltages applied to P and Q (continuous blue and dashed red lines), the programmed voltage ramps (empty blue squares and empty red circles) and V_G (dashed line plus solid black circles) are depicted as a function of time. In addition, Figure 5-17(b) shows the voltage drops across P (solid blue line) and Q (dashed red line).

In Figure 5-17(a), it is observed the applied and programmed voltages of memristor P completely coincide, because the current limit value has not been reached. This probably occurs because the voltage drop across P is not enough to reach the current limit value since the voltage ramp only increases up to -1 V Furthermore, the resistance value achieved in the initialization step, more voltage would be needed to reach that current limit according Ohm's law. Regarding the voltages of Q, even though voltage drop across Q is larger (at maximum values $V_Q - V_G = -4\text{ V} - (-1\text{ V}) = -3\text{ V}$), the resistance value of Q is higher enough to keep

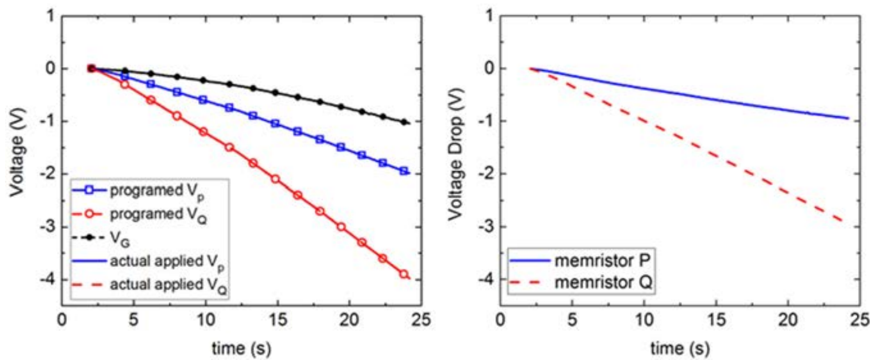


Figure 5-17: (a) Actual voltages, applied in case 3, to P and Q top electrodes (continuous blue and dashed red lines respectively), V_G (solid black circles) and programmed voltages of P and Q (empty blue squares and empty red circles) depicted as a function of time. As I_C is not reached, applied and programmed voltages completely overlap. (b) Voltage drops across P and Q (continuous blue and dashed red lines) as a function of time.

the current at low levels (I_{OFF}) maintaining Q at required "0" state. Contrarily to case 2, the resistance value of Q is much larger than that of P what produces the voltage divider configuration between memristor P and R_G and, therefore, V_G tends to follow V_P behavior (Figure 5-17(a)).

In spite of different voltage behaviors, both memristors, Q and P, reach the correct final states (Figure 5-16(c) and (d)) applying the same voltage ramps as in previous cases, accomplishing the case 3 as indicated in the IMPLY truth table (Table 5-I).

CASE 4

Now, the initial states of P and Q, shown in Figure 5-18(a) and (d) respectively, must be "1" for both memristors what means high currents values ($I > 10$ µA). Likewise cases 2 and 3, a memristor state changes is not expected neither Q nor P memristors after voltage ramps are applied. Figure 5-18(b) and (e) show the transient response of the currents through Q and P when the voltage ramps from 0 V to -4 V and from 0 V to -2 V are respectively applied. Initially, both memristors currents are expected to reach the current limit since both memristor are at "1" state, their resistances values are very low. However, only memristor Q achieves the current limit mainly due to the applied voltage ramp is larger than that applied to P. Therefore, the current evolution of Q memristor is similar to that observed in case 2 for the same memristor. The current quickly increases with voltage until the established current limit kept by the SPA is reached. This effect is observed in Figure 5-19(a) where actual applied, programmed voltages and V_G are depicted for

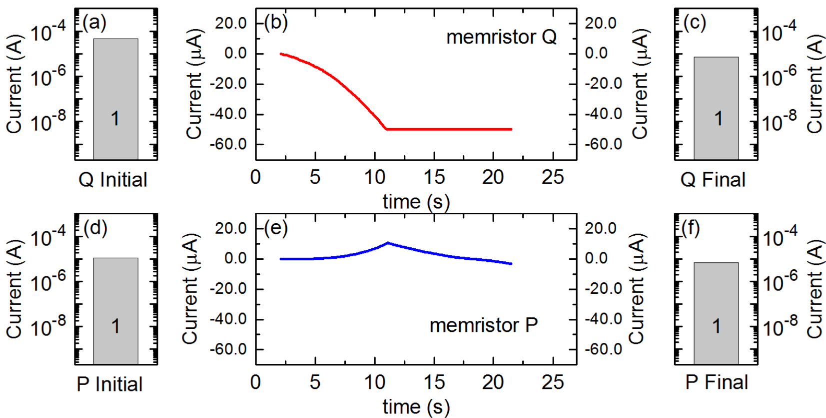


Figure 5-18: Transition between initial and final states for case 4 of the IMPLY gate showing (from left to right) the initial (inputs) states of Q at "1" logic state (a) and P also at "1" logic state (d); current evolutions as a function of time of Q memristor (b) and P memristor (e) and final states of Q (output) at "1" logic state (c) and P at "1" logic state (f). Initial and final states were measured at -0.5 V.

both memristors, P and Q.

Initially, applied voltage V_Q (dashed red line) follows programed V_Q (empty red circles), but when current limit is reached, the SPA automatically varies the increasing speed of the voltage to control the current flowing through the memristor and to avoid current larger than the current limit. Furthermore, V_G (solid black circles) also appears following applied voltage V_Q. The reason of such a behavior is owing to the initial states reached by the memristors are not exactly equal. Memristor Q has reach a larger current value that memristor P has, almost an order of magnitude of difference as observed from Figure 5-18(a) and (d). Consequently, the resistance value of Q is approximately on order of magnitude lower than the resistance value of P. Due to that difference between the resistance values, the contribution of V_Q to V_G expression becomes more relevant than that of V_P provoking the evolution of V_G is led mainly by V_Q. Note that after reaching current limit V_Q is not completely constant. This might be due to the influence of V_P, whose increasing also affects to V_G value and, consequently, to V_Q too. Therefore, no voltage divider behavior is observed between one memristor and R_G, as in the previous cases. This provokes the voltage drop across Q (dashed red line in Figure 5-19(b)) barely increases up to reach a constant value of -0.5 V.

Regarding the transient response of the current through P (Figure 5-18(e)), two unexpected behaviors are observed. First, current never reaches the expected current limit level what may be due to the low voltage drop across P (solid blue line in Figure 5-19(b)) is not sufficient to reach that value. Moreover, P current changes its direction twice because, in Figure 5-19(a), V_G surpasses applied V_P (solid blue line

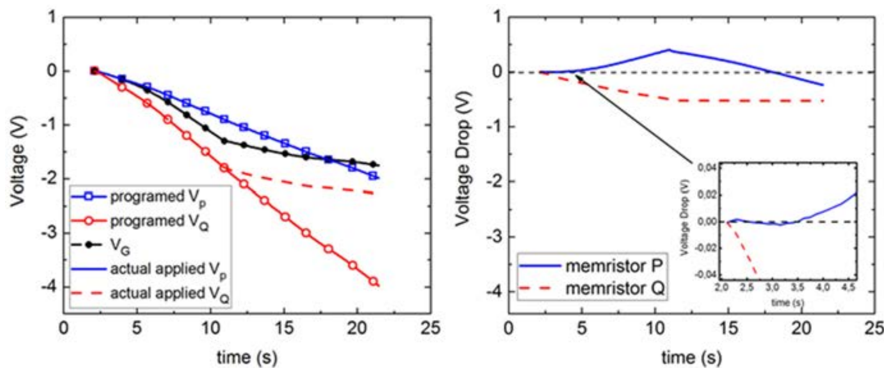


Figure 5-19: (a) Actual voltages, applied in case 4, to P and Q top electrodes (continuous blue and dashed red lines respectively), V_G (solid black circles) and programmed voltages of P and Q (empty blue squares and empty red circles). (b) Voltage drops across memristor P (continuous blue line) and Q (dashed red line). Inset is a zoom of the part pointed out by the arrow where the polarity of P voltage drop changes.

in Figure 5-19(a)) at around 5 and 17 seconds. This behavior is explained by the voltage drop across P depicted in Figure 5-19(b). This voltage drop (solid blue line) changes its polarity twice. The inset in Figure 5-19(b) show more in detail the first polarity change of the voltage drop across P. In spite of low voltage drop and polarity changes the current flowing through memristor does not affect the state and therefore memristor P maintains its “1” state as Figure 5-18(f) corroborates.

In short, the case 4 of the IMPLY is successfully accomplished although different memristors behaviors are observed.

5.5.3. The effect of the series resistor on IMPLY operation

As notice, the foremost component in an IMPLY gate are the memristors since their resistance states are the inputs and outputs of the gate. However, another component involved in the performance of the gate operation is the resistor R_G. R_G is overall defined as a resistor whose value must be in between of the two possible resistance values of the memristors, LRS and at HRS, [80], to successfully perform the IMPLY operation. However, in this work, such a resistor has shown an influence on the transient evolution affecting the current limit controlled by the SPA. Hence, a study of the R_G effect on current limit value has been performed.

The study has been carried out on the case 2 since the larger voltage ramp is applied to the memristor at “1” logic state and the current limit is easier to reach. For the measurement, voltage ramps applied to memristors Q and P have been from 0 V to -4 V and from 0 to -2 V, respectively. A relatively high current limit of 300 µA has been established in order to clearly observe the differences between the current limit applied by the SPA and the influence of R_G. Different values of R_G have been used to show its impact depending on the desired current limit. To compare RG values with memristor resistance states, LRS and HRS have been considered to be around 10 kΩ and 50 MΩ, respectively.

In case 2, one of the memristors is at “0” (or HRS) and the other memristor at “1” or (LRS). Because the resistance value at HRS is really large in comparison with that at LRS, the current flowing through the corresponding memristor can be neglected. Therefore, that branch in the equivalent circuit of IMPLY gate can be suppressed as Figure 5-20(a) shows. The equivalent circuit now may be considered as a voltage divider between the branches of the memristor at “1” (LRS) and the resistor R_G as depicted in Figure 5-20(b).

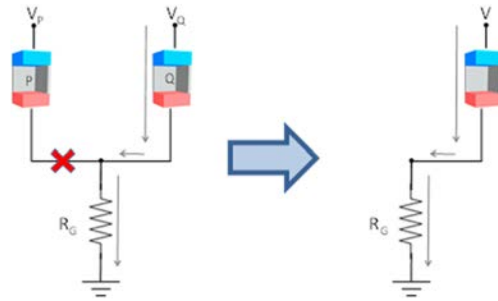


Figure 5-20: Equivalent IMPLY circuit when one of the memristor is at “0” state, and therefore, its resistance is very large in comparison to R_G and that of the other memristor.

Current flowing through the memristor conforming the voltage divider is the same current that flows through R_G. Therefore, the current flowing through the whole branch is controlled by R_G following the Ohm’s law. Depending on the voltage applied to the memristor R_G might act as current limiter instead of the SPA because R_G value and voltage drop across it is not enough to reach the current limit value.

To experimentally show the R_G effect on the achieved current limit value, in Figure 5-21 the transient evolution of the currents through the memristor P and Q (I_P and I_Q respectively) are depicted for 5 different values of R_G (1 kΩ, 33 kΩ, 155 kΩ, 566 kΩ and 956 kΩ). As memristor P is at “0”, the current through it (I_P) is indeed below 0.1 µA. On the other hand, as memristor Q is at “1”, the current I_Q reached values above 10 µA. Note that the different chosen values of R_G accomplish the condition HRS > R_G > LRS with the exception of 1 kΩ which has been included to show the situation when the current limit is applied by the

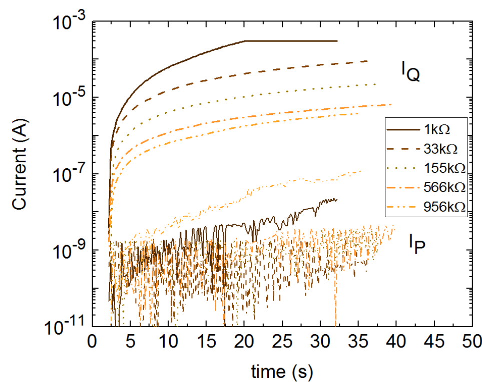


Figure 5-21: Currents through memristors P and Q for different values of R_G (1 kΩ, 33 kΩ, 156 kΩ, 566 kΩ, 960 kΩ). As the value of R_G increases, the current limit is imposed by the resistor instead of the semiconductor parameter analyzer.

SPA. Focusing on the current through memristor Q (I_Q), initially, when R_G is 1 kΩ current through such a resistor is larger than the selected current limit (for applied voltage, V_Q, larger than -2 V), therefore, when the current flowing through the voltage divider reaches the limit, SPA is acting as the current limiter, what can be identified by the flat part of the curve (solid line in Figure 5-21). However, as R_G increases the current through the resistor becomes lower for the same applied voltages due to Ohm's law, therefore, the larger R_G, the lower the current flowing through Q. As a consequence, when the voltage drop across R_G is not enough to reach the current limit value, the maximum allowed current through the branch is that flowing through the resistor, what provokes R_G control the current limit.

This is corroborated in Figure 5-22 where voltage drops across memristor Q (continuous red line) and R_G (dashed black line) are depicted for the different values of R_G ((a) 1 kΩ, (b) 33 kΩ, (c) 156 kΩ, (d) 566 kΩ and (e) 956 kΩ). For the lowest value of R_G (1 kΩ), the voltage drop across R_G (black dashed line in Figure 5-22(a)) is almost negligible and barely affects the current conduction through Q. Voltage drops across the memristor (continuous red line in Figure 5-22(a)) is almost the voltage applied to it. Thus, the current through the

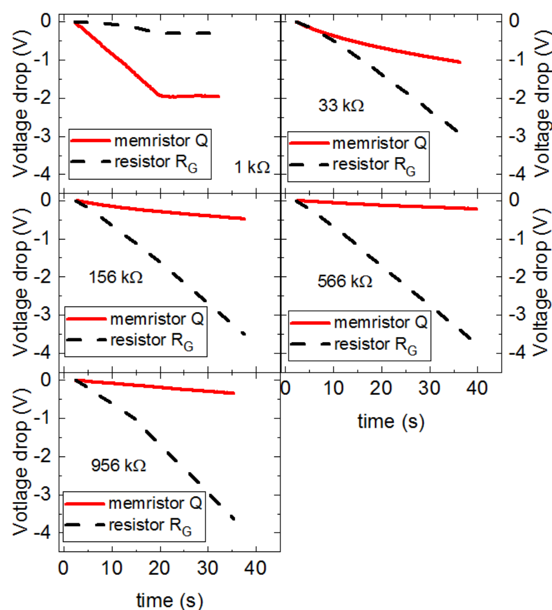


Figure 5-22: Voltage drops across memristor Q and R_G in case 2 for different values of R_G, (a) 1 kΩ, (b) 33 kΩ, (c) 156 kΩ, (d) 566 kΩ, and (e) 956 kΩ). As R_G increases, voltage drop through R_G also increases until almost reaching the values of the voltage applied to Q.

branch is mainly controlled by the SPA which keeps a constant applied voltage to fix the current at the limit value. On the contrary, as R_G increases, its voltage drop also increases provoking that the voltage drop across Q decreases. Consequently, the current through R_G, and hence through memristor Q, is now controlled by Ohm's law on R_G. As an example, looking at the Figure 5-22(b) when R_G = 33 kΩ, if the maximum value of applied voltage ramp is -4 V, a current of 121 µA should flow along the branch, according to Ohm's law. This value of the current is more than a half of the established current limit which is 300 µA. Therefore, R_G is limiting the current that can flow through the whole branch and consequently through memristor Q. This effect is increased when R_G value also increases because the current flowing through the divider branch decreases since the voltage ramp is always applied from 0 V to -4 V range. Although, this effect would allow accomplishing IMPLY truth table, if low current limit values were required, the final state reached for memristor Q could not be a well-defined state.

5.6. Conclusions

Initially, memristor-based IMPLY and IMPLY-based NAND logic gates have been experimentally demonstrated using HfO_2-based memristor. Sequential NAND measurement, where the four cases randomly chosen were performed, have been also successfully demonstrated. Additionally, a modified procedure to operate the NAND gate has been proposed. This procedure suggests reducing NAND operation from two steps to only one which might reduce the computing time. Despite this technique requires a third operational voltage for the NAND structure, in the shown case this additional voltage is grounded.

Secondly, a detailed study of the electrical transient response of the two memristors involved in the IMPLY gate has been performed for each IMPLY case. The transient evolution of the currents and the voltage drops of memristors have been analyzed during operation gate. Different behaviors have been observed, such as polarity changes in some of the transient-implicated memristors voltage drops and changes in the increasing speed of the applied voltage ramps. Finally, the impact of the resistor R_G also involved in the design of the IMPLY gate and located in series with the memristors has been analyzed. The results have shown that R_G can act as the current limiter instead of the SPA although it might have no effect on the gate performance.

6. Conclusions

Scientific community have been focused continuously on improving the technology. In particular, in the electronic field, great advances have been performed along decades. However, as the time goes by, the innovative technology of yesterday becomes obsolete today what provokes continuous research, for instance, on new materials, new structures of the devices or new phenomena. In the later topic, **Resistive Switching** constitutes one of the most relevance phenomenon in the improvement of the current electronic technology. This phenomenon shows a good versatility to be implemented in many different applications such as memories, logic gates, artificial neural networks or stochastic computing.

This thesis, which has been focused on the characterization of resistive switching phenomenon and its application in different areas. The results have allowed coming to the following conclusions:

First, during the analysis of the resistive switching in transistors, it has been intended to control the localization of the conductive filament, which connects the gate and bottom transistor terminals through the dielectric layer, near the other two terminals of the transistor, the source and the drain. Initially, it was observed a relatively good control of that location, however after a very few cycles of RS that location become more difficult to control. Therefore, the complete control of the location of the conductive filament was not possible for the transistors used in this work. On the other hand, from the characterization of resistive switching phenomenon in transistors, a new method to separate the two contributions of the current through the dielectric layer (localized current through the conductive filament, I_{CF}, and non-localized gate current due to the whole dielectric degradation I_{NLC}) has been proposed. The method has been based on the determination of the location of the filament along the transistor channel when at HRS. Actually, the method must be adapted taking into account if filament is located close to drain or source.

Continuing with the characterization of the phenomenon, in this case over memristors, a study of such a phenomenon in the time domain (with a large time resolution) by means of the proposed experimental setup has been performed. This

study has shown that set and reset voltages has a strong dependence on the speed of the applied voltage ramps to provoke both set and reset processes. Results have demonstrated that set and reset voltages increase with the increase of voltage ramp speed. On the contrary, from the same study, it has been observed that the energies employed to trigger set and reset processes are independent of the biasing conditions, specifically of the voltage ramp speed, suggesting that energy is an intrinsic parameter of the RS mechanism. Furthermore, a new experimental setup that provides a larger time resolution than standard equipment has been presented to analyze RTN fluctuations which affects resistive switching performance. The obtained results have demonstrated that some RTN fluctuations can be undetectable if standard RTN characterization instruments, as semiconductor parameters analyzers with lower time resolution, are used. Therefore, a complete RTN characterization methodology, which combines a high time resolution equipment and an accurate parameters extraction method (W-TL), has been proposed to obtain a more complete information about RTN signals. In addition, this methodology allows studying the RTN impact in memristors working as well as the cause of those RTN fluctuations.

Regarding the applications of resistive switching, new material combinations based on SiO_x as dielectric layer in combination with different top electrodes have been studied to demonstrate their feasibility in memory and selector applications. On the one hand, as memory device, Ti/SiO_X-based structure has exhibited the best performance. Under DC conditions the devices have shown a low set voltage (below 3 V) and a resistance window controllable by V_{STOP} parameter. This behavior has been also observed under pulsed conditions as well as a very large endurance (with more than 10^7 cycles where resistance window has been above 10). Finally, these devices have shown good state retention in the temperature range from 120 °C to 260 °C. On the other hand, for selector applications, Ag/SiO_X-based structure has shown great features such as a volatile switching with larger on/off ratio ($>10^7$), a bidirectional operation and stable threshold and holding voltages, everything under DC conditions. It has been also studied the influence of I_C on the device operation concluding that for low current limits the volatile switching is achieved whereas for larger current limits nonvolatile switching is observed. Moreover, threshold switching has been also analyzed under pulsed conditions discovering an increase of both positive and negative threshold voltages with the time of the applied pulse as well as an increasing of the filament retention time also with such a time. Eventually, the operation of SiO_X-based memory and selector devices in combination, forming the 1S1R structure, has been demonstrated for a few cycles of bidirectional threshold switching and bipolar resistive switching.

Finally, the use of memristors in logic application has been studied. Specifically,

memristor-based IMPLY and IMPLY-based NAND logic gates have been experimentally demonstrated using HfO_2-based memristors. Additionally, sequential NAND measurement have been also successfully demonstrated. A modified procedure to operate the NAND gate has been proposed where only one operation step is required. This fact might reduce the computing time when compared to previous IMPLY-based NAND implementations which require two operation steps. Furthermore, a detailed study of the electrical transient response of the two memristors involved in the IMPLY gate has been performed for each IMPLY input-output case. The transient evolution of the currents and the voltage drops of memristors have been analyzed, describing how these parameters behave during the operation gate. Polarity changes in some of the transient-implicated memristors voltage drops have been observed during the IMPLY gate performance. Finally, the impact of the resistor R_G also involved in the design of the IMPLY gate has been analyzed. The results have shown that R_G can act as the current limiter instead of the SPA when large current limits are established.

Overall, the work developed in this thesis provides new characterization techniques for the study of resistive switching and reliability issues such as RTN fluctuations in both transistors and memristors. Moreover, the use of memristors as memory and selector devices as well as to develop logic gates have been studied and demonstrated. Most of the results included in this manuscript have been disserted in specialized journals and international conferences

PUBLICATIONS

JOURNAL PAPERS

Maestro, M., Martin-Martinez, J., Crespo-Yepes, A., Escudero, M., Rodriguez, R., Nafria, M., Aymerich, X. and Rubio, A. "*Transient performance of memristors in an IMPLY gate: an experimental study*". Trans. Electron Devices. (Sent for publication).

Maestro, M., Martin-Martinez, J., Crespo-Yepes, A., Escudero, M., Rodriguez, R., Nafria, M., Aymerich, X. and Rubio, A. "*Experimental verification of memristor-based material implication NAND operation*". Trans. Emerging Topics in Computing (Sent for publication).

Maestro, M., Diaz, J., Crespo-Yepes, A., Gonzalez, M. B., Martin-Martinez, J., Rodriguez, R., Nafria, Campabadal, F. and M., Aymerich, X. "*A new high resolution Random Telegraph Noise (RTN) characterization method for resistive RAM*". Solid-State Electronics, vol.115, pp. 140–145, 2016.

Maestro, M., Martin-Martinez, J., Diaz, J., Crespo-Yepes, A., Gonzalez, M. B., Rodriguez, R., Campabadal, F., Nafria, M. and Aymerich, X. "*Analysis of Set and Reset mechanisms in Ni/HfO2-based RRAM with fast ramped voltages*". Microelectronic Engineering, vol. 147, pp. 176–179, 2015.

Diaz-Fortuny, J. **Maestro**, **M.** Martin-Martinez, J. Crespo-Yepes, A. Rodriguez, R., M. Nafria, and X. Aymerich, "Current-limiting and ultrafast system for the characterization of resistive random access memories," *Rev. Sci. Instrum.*, vol. 87, no. 6, p. 064705, Jun. 2016.

Gonzalez, M. B. Martin-Martinez, J. **Maestro, M**. Acero, M. C. Nafria, M. and Campabadal, F. "*Investigation of Filamentary Current Fluctuations Features in the High-Resistance State of Ni/HfO_2-Based RRAM*," IEEE Trans. Electron Devices, vol. 63, no. 8, pp. 3116–3122, 2016.

Claramunt, S., Wu, Q., **Maestro, M.,** Porti, M., Gonzalez, M. B., Martin-Martinez, J., Campabadal, F., Nafría, M. "*Non-homogeneous conduction of conductive filaments in Ni/HfO2/Si resistive switching structures observed with CAFM*". Microelectronic Engineering, vol. 147, pp. 335-338, 2015.

CONFERENCE PAPERS

Maestro, **M.** Martin-Martinez, J. Crespo-Yepes, A. Escudero, M. Rodriguez, R. Nafria, M. Aymerich, X. Rubio, A. "*Transient analysis of an experimentally-verified memristor-based IMPLY gate.*" (ORAL) "International Conference on Memristive Materials, Devices & Systems" (MEMRISYS 2017).

Maestro, **M.** Martin-Martinez, J. Diaz, J. Crespo-Yepes, A. Gonzalez, M. B. Rodriguez, R. Campabadal, F. Nafria, M. Aymerich, X. "*Analysis of Set and Reset mechanisms in Ni/HfO2-based RRAM with fast ramped voltages.*" (POSTER) 19th Conference of "Insulating Films on Semiconductors" (INFOS 2015).

Maestro, M., Crespo-Yepes, A., Martin-Martinez, J., Claramunt, S., Rodriguez, R., Nafria, M., and Aymerich, X., "*Distinguishing conductive filament and non-localized gate conduction in resistive switching devices*". (POSTER) IEEE 10th Spanish Conference on Electron Devices, pp. 1–4, (CDE 2015).

Maestro, **M.** Diaz, J. Crespo-Yepes, A. Gonzalez, M.B. Martin-Martinez, J. Rodriguez, R. Nafria, M. Campabadal, F. and Aymerich, X. "*A new high resolution Random Telegraph Noise (RTN) characterization method for Resistive RAM.*" (ORAL) Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (ULIS), pp. 133-136, (EUROSOI-ULIS 2015).

Maestro, **M.** Crespo-Yepes, A. Martin-Martinez, J. Rodriguez, R. Nafria, M. Aymerich, X. "*New method to discriminate between the conductive filament and the non-localized gate current conduction in resistive switching devices.*" (POSTER) 18th Workshop on Dielectrics in Microelectronics (WoDiM 2014).

Claramunt, S. Wu, Q. **Maestro**, **M.** Porti, M. Gonzalez, M.B. Martin-Martinez, J. Campabadal, F. Nafria, M. "*Non-homogeneous conduction of conductive filaments in Ni/HfO2/Si resistive switching structures observed with CAFM.*" (POSTER) 19th Conference of "Insulating Films on Semiconductors" (INFOS 2015).

Crespo-Yepes, A. Martin-Martinez, J. Rama, I. **Maestro**, **M.** Rodriguez, R. Gonzalez, M.B. Campabadal, F. Nafria, M. Aymerich, X. "*Intra-device statistical parameters in variability-aware modelling of Resistive Switching devices*" (ORAL) International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS 2016).

Bricalli, A. Ambrosi, E. Laudato, M. **Maestro, M.** Rodriguez, R. and Ielmini, D. "*SiO_X-based resistive switching memory (RRAM) for crossbar storage/select elements with high on/off ratio.*" (ORAL) 62nd IEEE-International Electronic Device Meeting (IEDM 2016).

REFERENCES

[1] L. O. Chua, “Memristor—The Missing Circuit Element,” IEEE Trans. Circuit Theory, vol. 18, no. 5, pp. 507–519, 1971.

[2] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, “The missing memristor found.,” Nature, vol. 453, no. 7191, pp. 80–3, 2008.

[3] C. Garcia Almudever, A. Rubio Sola, A. Crespo-Yepes, M. Nafria Maqueda, and R. Rodriguez Martinez, “Method for operating a transistor, reconfigurable porcessing architecture and use of a multiple mode operation,” European Patent Office 10016028.2-2210, 2012.

[4] J. Martin-Martinez, A. Crespo-Yepes, R. Rodriguez, M. Nafria, C. G. Almudever, and A. Rubio, “memFET: From gate dielectric breakdown to system reconfigurability,” in 2013 IEEE International Reliability Physics Symposium (IRPS), 2013, p. ER.2.1-ER.2.6.

[5] C. G. Almudever, A. Rubio, J. Martin-Martinez, A. Crespo-Yepes, R. Rodriguez, and M. Nafria, “Shape-shifting digital hardware concept: Towards a new adaptive computing system,” in 2012 NASA/ESA Conference on Adaptive Hardware and Systems (AHS), 2012, pp. 167–173.

[6] Albert Crespo, “Estudio de la reversibilidad de la ruptura dieléctrica en dispositivos MOS con dieléctrico de puerta high-k ultra delgado,” Ph. D. dissertation, Electrical Engineering Department, Autonomous University of Barcelona, 2012.

[7] Shih-Chieh Wu, Chieh Lo, and Tuo-Hung Hou, “Logic/resistive-switching hybrid transistor for two-bit-per-cell storage,” in Proceedings of the International Symposium on VLSI Technology, System and Application, 2012, pp. 1–2.

[8] F. Pan, S. Gao, C. Chen, C. Song, and F. Zeng, “Recent progress in resistive random access memories: Materials, switching mechanisms, and performance,” Mater. Sci. Eng. R Reports, vol. 83, pp. 1–59, Sep. 2014.

[9] J. S. Lee, S. Lee, and T. W. Noh, "Resistive switching phenomena," Appl. Phys. Rev., vol. 2, no. 3, p. 31303, Sep. 2015.

[10] Seonghyun Kim, K. P. Biju, Minseok Jo, Seungjae Jung, Jubong Park, Joonmyoung Lee, Wootae Lee, Jungho Shin, Sangsu Park, and Hyunsang Hwang, "Effect of Scaling WOx-Based RRAMs on Their Resistive Switching Characteristics," IEEE Electron Device Lett., vol. 32, no. 5, pp. 671–673, May 2011.

[11] D. S. Shang, L. Shi, J. R. Sun, B. G. Shen, F. Zhuge, R. W. Li, and Y. G. Zhao, "Improvement of reproducible resistance switching in polycrystalline tungsten oxide films by in situ oxygen annealing," Appl. Phys. Lett., vol. 96, no. 7, p. 72103, Feb. 2010.

[12] B. J. Choi, D. S. Jeong, S. K. Kim, C. Rohde, S. Choi, J. H. Oh, H. J. Kim, C. S. Hwang, K. Szot, R. Waser, B. Reichenberg, and S. Tiedke, "Resistive switching mechanism of TiO2 thin films grown by atomic-layer deposition," J. Appl. Phys., vol. 98, no. 3, p. 33715, Aug. 2005.

[13] J. Yao, Z. Sun, L. Zhong, D. Natelson, and J. M. Tour, "Resistive Switches and Memories from Silicon Oxide," Nano Lett., vol. 10, no. 10, pp. 4105–4110, Oct. 2010.

[14] S. Spiga, A. Lamperti, C. Wiemer, M. Perego, E. Cianci, G. Tallarida, H. L. Lu, M. Alia, F. G. Volpe, and M. Fanciulli, "Resistance switching in amorphous and crystalline binary oxides grown by electron beam evaporation and atomic layer deposition," Microelectron. Eng., vol. 85, no. 12, pp. 2414–2419, 2008.

[15] Y. Yin Chen, G. Pourtois, C. Adelmann, L. Goux, B. Govoreanu, R. Degreave, M. Jurczak, J. A. Kittl, G. Groeseneken, and D. J. Wouters, "Insights into Ni-filament formation in unipolar-switching Ni/HfO2/TiN resistive random access memory device," Appl. Phys. Lett., vol. 100, no. 11, p. 113513, Mar. 2012.

[16] I. G. Baek, M. S. Lee, S. Sco, M. J. Lee, D. H. Seo, D.-S. Suh, J. C. Park, S. O. Park, H. S. Kim, I. K. Yoo, U.-I. Chung, and J. T. Moon, "Highly scalable non-volatile resistive memory using simple binary oxide driven by

asymmetric unipolar voltage pulses," in IEEE International Electron Devices Meeting IEDM Technical Digest, 2004., pp. 587–590.

[17] D. Ielmini, F. Nardi, and C. Cagli, "Physical models of size-dependent nanofilament formation and rupture in NiO resistive switching memories," Nanotechnology, vol. 22, no. 25, p. 254022, Jun. 2011.

[18] D. S. Jeong, H. Schroeder, and R. Waser, "Coexistence of Bipolar and Unipolar Resistive Switching Behaviors in a Pt/TiO2/Pt Stack," Electrochem. Solid-State Lett., vol. 10, no. 8, p. G51, 2007.

[19] L. Goux, J. G. Lisoni, M. Jurczak, D. J. Wouters, L. Courtade, and C. Muller, "Coexistence of the bipolar and unipolar resistive-switching modes in NiO cells made by thermal oxidation of Ni layers," J. Appl. Phys., vol. 107, no. 2, p. 24512, Jan. 2010.

[20] L. Goux, Y.-Y. Chen, L. Pantisano, X.-P. Wang, G. Groeseneken, M. Jurczak, and D. J. Wouters, "On the Gradual Unipolar and Bipolar Resistive Switching of TiN\HfO2\Pt Memory Systems," Electrochem. Solid-State Lett., vol. 13, no. 6, p. G54, 2010.

[21] S. H. Chang, S. B. Lee, D. Y. Jeon, S. J. Park, G. T. Kim, S. M. Yang, S. C. Chae, H. K. Yoo, B. S. Kang, M.-J. Lee, and T. W. Noh, "Oxide Double-Layer Nanocrossbar for Ultrahigh-Density Bipolar Resistive Memory," Adv. Mater., vol. 23, no. 35, pp. 4063–4067, Sep. 2011.

[22] M.-J. Lee, Y. Park, D.-S. Suh, E.-H. Lee, S. Seo, D.-C. Kim, R. Jung, B.-S. Kang, S.-E. Ahn, C. B. Lee, D. H. Seo, Y.-K. Cha, I.-K. Yoo, J.-S. Kim, and B. H. Park, "Two Series Oxide Resistors Applicable to High Speed and High Density Nonvolatile Memory," Adv. Mater., vol. 19, no. 22, pp. 3919–3923, Nov. 2007.

[23] R. Waser and M. Aono, "Nanoionics-based resistive switching memories," Nat. Mater., vol. 6, no. 11, pp. 833–840, Nov. 2007.

[24] R. Waser, R. Dittmann, G. Staikov, and K. Szot, "Redox-Based Resistive Switching Memories–Nanoionic Mechanisms, Prospects, and Challenges," Adv. Mater., vol. 21, no. 25–26, pp. 2632–2663, 2009.

[25] J. J. Yang, M. D. Pickett, X. Li, D. A. A. Ohlberg, D. R. Stewart, and R. S. Williams, "Memristive switching mechanism for metal/oxide/metal nanodevices," Nat. Nanotechnol., vol. 3, no. 7, pp. 429–433, Jul. 2008.

[26] T. Chang, Y. Yang, W. Lu, Ting Chang, Yuchao Yang, and Wei Lu, "Building neuromorphic circuits with memristive devices," IEEE Circuits Syst. Mag., vol. 13, no. 2, pp. 56–73, 2013.

[27] J. J. Yang, D. B. Strukov, and D. R. Stewart, "Memristive devices for computing," Nat. Nanotechnol., vol. 8, no. 1, pp. 13–24, Dec. 2012.

[28] M.-J. Lee, C. B. Lee, D. Lee, S. R. Lee, M. Chang, J. H. Hur, Y.-B. Kim, C.-J. Kim, D. H. Seo, S. Seo, U.-I. Chung, I.-K. Yoo, and K. Kim, "A fast, high-endurance and scalable non-volatile memory device made from asymmetric Ta2O5-x/TaO2-x bilayer structures," Nat. Mater., vol. 10, no. 8, pp. 625–630, Jul. 2011.

[29] D.-H. Kwon, K. M. Kim, J. H. Jang, J. M. Jeon, M. H. Lee, G. H. Kim, X.-S. Li, G.-S. Park, B. Lee, S. Han, M. Kim, and C. S. Hwang, "Atomic structure of conducting nanofilaments in TiO2 resistive switching memory," Nat. Nanotechnol., vol. 5, no. 2, pp. 148–153, Feb. 2010.

[30] Y. Yang, P. Gao, S. Gaba, T. Chang, X. Pan, and W. Lu, "Observation of conducting filament growth in nanoscale resistive memories," Nat. Commun., vol. 3, p. 732, Mar. 2012.

[31] F. Miao, J. P. Strachan, J. J. Yang, M.-X. Zhang, I. Goldfarb, A. C. Torrezan, P. Eschbach, R. D. Kelley, G. Medeiros-Ribeiro, and R. S. Williams, "Anatomy of a Nanoscale Conduction Channel Reveals the Mechanism of a High-Performance Memristor," Adv. Mater., vol. 23, no. 47, pp. 5633–5640, Dec. 2011.

[32] J. P. Strachan, M. D. Pickett, J. J. Yang, S. Aloni, A. L. David Kilcoyne, G. Medeiros-Ribeiro, and R. Stanley Williams, "Direct Identification of the Conducting Channels in a Functioning Memristive Device," Adv. Mater., vol. 22, no. 32, pp. 3573–3577, Aug. 2010.

[33] Y. S. Lin, F. Zeng, S. G. Tang, H. Y. Liu, C. Chen, S. Gao, Y. G. Wang, and F. Pan, "Resistive switching mechanisms relating to oxygen vacancies migration in both interfaces in Ti/HfOx/Pt memory devices," J. Appl. Phys., vol. 113, no. 6, p. 64510, Feb. 2013.

[34] C. Yoshida, K. Kinoshita, T. Yamasaki, and Y. Sugiyama, "Direct observation of oxygen movement during resistance switching in NiO/Pt film," Appl. Phys. Lett., vol. 93, no. 4, p. 42106, Jul. 2008.

[35] C. Chen, C. Song, J. Yang, F. Zeng, and F. Pan, "Oxygen migration induced resistive switching effect and its thermal stability in W/TaOx/Pt structure," Appl. Phys. Lett., vol. 100, no. 25, p. 253509, Jun. 2012.

[36] I. Valov, R. Waser, J. R. Jameson, and M. N. Kozicki, "Electrochemical metallization memories—fundamentals, applications, prospects," Nanotechnology, vol. 22, no. 25, p. 254003, Jun. 2011.

[37] W.-C. Luo, T.-H. Hou, K.-L. Lin, Y.-J. Lee, and T.-F. Lei, "Reversible transition of resistive switching induced by oxygen-vacancy and metal filaments in HfO2," Solid. State. Electron., vol. 89, pp. 167–170, Nov. 2013.

[38] X. Wu, D. Cha, M. Bosman, N. Raghavan, D. B. Migas, V. E. Borisenko, X.-X. X. Zhang, K. Li, and K.-L. L. Pey, "Intrinsic nanofilamentation in resistive switching," J. Appl. Phys., vol. 113, no. 11, p. 114503, Mar. 2013.

[39] K.-L. Lin, T.-H. Hou, J. Shieh, J.-H. Lin, C.-T. Chou, and Y.-J. Lee, "Electrode dependence of filament formation in HfO2 resistive-switching memory," J. Appl. Phys., vol. 109, no. 8, p. 84104, Apr. 2011.

[40] U. Russo, D. Ielmini, C. Cagli, and A. L. A. Lacaita, "Self-Accelerated Thermal Dissolution Model for Reset Programming in Unipolar Resistive-Switching Memory (RRAM) Devices," IEEE Trans. Electron Devices, vol. 56, no. 2, pp. 193–200, Feb. 2009.

[41] M. A. Villena, F. Jiménez-Molinos, J. B. Roldán, J. Suñé, S. Long, X. Lian, F. Gámiz, and M. Liu, "An in-depth simulation study of thermal reset transitions in resistive switching memories," J. Appl. Phys., vol. 114, no. 14, p. 144505, 2013.

[42] K. M. Kim, D. S. Jeong, and C. S. Hwang, "Nanofilamentary resistive switching in binary oxide system; a review on the present status and outlook," Nanotechnology, vol. 22, no. 25, p. 254002, Jun. 2011.

[43] D. Ielmini, F. Nardi, and C. Cagli, "Universal Reset Characteristics of Unipolar and Bipolar Metal-Oxide RRAM," IEEE Trans. Electron Devices, vol. 58, no. 10, pp. 3246–3253, Oct. 2011.

[44] A. Fantini, L. Goux, R. Degraeve, D. J. Wouters, N. Raghavan, G. Kar, A. Belmonte, Y. Y. Chen, B. Govoreanu, and M. Jurczak, "Intrinsic switching variability in HfO2 RRAM," 2013 5th IEEE Int. Mem. Work. IMW 2013, pp. 30–33, 2013.

[45] M. Gonzalez, J. Rafi, O. Beldarrain, M. Zabala, and F. Campabadal, "Analysis of the Switching Variability in Ni/HfO2-based RRAM Devices," IEEE Trans. Device Mater. Reliab., vol. 14, pp. 1–1, 2014.

[46] B. Gao, H. Zhang, B. Chen, L. Liu, X. Liu, R. Han, J. Kang, Z. Fang, H. Yu, B. Yu, and D.-L. Kwong, "Modeling of Retention Failure Behavior in Bipolar Oxide-Based Resistive Switching Memory," IEEE Electron Device Lett., vol. 32, no. 3, pp. 276–278, Mar. 2011.

[47] M. Kyu Yang, H. Ju, G. Hwan Kim, J.-K. Lee, and H.-C. Ryu, "Direct evidence on Ta-Metal Phases Igniting Resistive Switching in TaOx Thin Film," Sci. Rep., vol. 5, p. 14053, Sep. 2015.

[48] D. Ielmini, F. Nardi, C. Cagli, and A. L. Lacaita, "Size-Dependent Retention Time in NiO-Based Resistive-Switching Memories," IEEE Electron Device Lett., vol. 31, no. 4, pp. 353–355, Apr. 2010.

[49] Z. Wei, T. Takagi, Y. Kanzawa, Y. Katoh, T. Ninomiya, K. Kawai, S. Muraoka, S. Mitani, K. Katayama, S. Fujii, R. Miyanaga, Y. Kawashima, T. Mikawa, K. Shimakawa, and K. Aono, "Retention Model for High-Density ReRAM," in 2012 4th IEEE International Memory Workshop, 2012, pp. 1-4.

[50] S. Yu, Y. Yin Chen, X. Guan, H.-S. Philip Wong, and J. A. Kittl, "A Monte Carlo study of the low resistance state retention of HfOx-based resistive switching memory," Appl. Phys. Lett., vol. 100, no. 4, p. 43507, Jan. 2012.

[51] H. Lv, X. Xu, H. Liu, R. Liu, Q. Liu, W. Banerjee, H. Sun, S. Long, L. Li, and M. Liu, “Evolution of conductive filament and its impact on reliability issues in oxide-electrolyte based resistive random access memory,” Sci. Rep., vol. 5, p. 7764, Jan. 2015.

[52] Y. Y. Chen, B. Govoreanu, L. Goux, R. Degraeve, A. Fantini, G. S. Kar, D. J. Wouters, G. Groeseneken, J. A. Kittl, M. Jurczak, and L. Altimime, “Balancing SET/RESET Pulse for >1010 Endurance in HfO2/Hf 1T1R Bipolar RRAM,” IEEE Trans. Electron Devices, vol. 59, no. 12, pp. 3243–3249, Dec. 2012.

[53] S. Balatti, S. Ambrogio, Z.-Q. Wang, S. Sills, A. Calderoni, N. Ramaswamy, and D. Ielmini, “Pulsed cycling operation and endurance failure of metal-oxide resistive (RRAM),” in 2014 IEEE International Electron Devices Meeting, 2014, vol. 2015–Febru, no. February, p. 14.3.1-14.3.4.

[54] Y.-B. Kim, S. R. Lee, D. Lee, C. B. Lee, M. Chang, J. H. Hur, M.-J. Lee, G.-S. Park, C. J. Kim, U.-I. Chung, I.-K. Yoo, and K. Kim, “Bi-layered RRAM with unlimited endurance and extremely uniform switching,” Symp. VLSI Technol. - Dig. Tech. Pap., pp. 52–53, 2011.

[55] S. Balatti, S. Ambrogio, Z. Wang, S. Sills, A. Calderoni, N. Ramaswamy, and D. Ielmini, “Voltage-Controlled Cycling Endurance of HfOx-Based Resistive-Switching Memory,” IEEE Trans. Electron Devices, vol. 62, no. 10, pp. 3365–3372, Oct. 2015.

[56] M. Azzaz, E. Vianello, B. Sklenard, P. Blaise, A. Roule, C. Sabbione, S. Bernasconi, C. Charpin, C. Cagli, E. Jalaguier, S. Jeannot, S. Denorme, P. Candelier, M. Yu, L. Nistor, C. Fenouillet-Beranger, and L. Perniola, “Endurance/Retention Trade Off in HfO2 and TaOx Based RRAM,” in 2016 IEEE 8th International Memory Workshop (IMW), 2016, pp. 1–4.

[57] Y. Y. Chen, L. Goux, S. Clima, B. Govoreanu, R. Degraeve, G. S. Kar, A. Fantini, G. Groeseneken, D. J. Wouters, and M. Jurczak, “Endurance/Retention Trade-off on HfOx/Metal Cap 1T1R Bipolar RRAM,” IEEE Trans. Electron Devices, vol. 60, no. 3, pp. 1114–1121, Mar. 2013.

[58] M. B. Gonzalez, J. Martin-Martinez, M. Maestro, M. C. Acero, M. Nafria, and F. Campabadal, "Investigation of Filamentary Current Fluctuations Features in the High-Resistance State of Ni/HfO2 -Based RRAM," IEEE Trans. Electron Devices, vol. 63, no. 8, pp. 3116–3122, Aug. 2016.

[59] N. Raghavan, R. Degraeve, A. Fantini, L. Goux, S. Strangio, B. Govoreanu, D. J. J. Wouters, G. Groeseneken, and M. Jurczak, "Microscopic origin of random telegraph noise fluctuations in aggressively scaled RRAM and its impact on read disturb variability," in 2013 IEEE International Reliability Physics Symposium (IRPS), 2013, p. 5E.3.1-5E.3.7.

[60] F. M. Puglisi, P. Pavan, L. Larcher, and A. Padovani, "Analysis of RTN and cycling variability in HfO2 RRAM devices in LRS," 2014, pp. 246–249.

[61] K. Takeuchi, T. Nagumo, S. Yokogawa, K. Imai, and Y. Hayashi, "Single-charge-based modeling of transistor characteristics fluctuations based on statistical measurement of RTN amplitude - IEEE Xplore Document," in Symposium on VLSI technology, 2009, pp. 54–55.

[62] T. Nagumo, K. Takeuchi, S. Yokogawa, K. Imai, and Y. Hayashi, "New analysis methods for comprehensive understanding of Random Telegraph Noise," 2009, pp. 1–4.

[63] L. R. Rabiner, "A tutorial on hidden Markov models and selected applications in speech recognition," Proc. IEEE, vol. 77, no. 2, pp. 257–286, 1989.

[64] Y. Yuzhelevski, M. Yuzhelevski, and G. Jung, "Random telegraph noise analysis in time domain," Cit. Rev. Sci. Instruments Rev. Sci. Instruments Spectr. a Two-param. Random Signal Rev. Sci. Instruments, vol. 71, no. 10, 2000.

[65] J. Martin-Martinez, J. Diaz, R. Rodriguez, M. Nafria, and X. Aymerich, "New Weighted Time Lag Method for the Analysis of Random Telegraph Signals," IEEE Electron Device Lett., vol. 35, no. 4, pp. 479–481, Apr. 2014.

[66] B. Govoreanu, G. S. Kar, Y.-Y. Chen, V. Paraschiv, S. Kubicek, A. Fantini, I. P. Radu, L. Goux, S. Clima, R. Degraeve, N. Jossart, O. Richard, T.

Vandeweyer, K. Seo, P. Hendrickx, G. Pourtois, H. Bender, L. Altimime, D. J. Wouters, J. A. Kittl, M. Jurczak, "10×10nm2 Hf/HfOx crossbar resistive RAM with excellent performance, reliability and low-energy operation," in International Electron Devices Meeting, 2011, p. 31.6.1-31.6.4.

[67] S. Gao, F. Zeng, C. Chen, G. Tang, Y. Lin, Z. Zheng, C. Song, and F. Pan, "Conductance quantization in a Ag filament-based polymer resistive memory," Nanotechnology, vol. 24, no. 33, p. 335201, Aug. 2013.

[68] A. C. Torrezan, J. P. Strachan, G. Medeiros-Ribeiro, and R. S. Williams, "Sub-nanosecond switching of a tantalum oxide memristor.," Nanotechnology, vol. 22, no. 48, p. 485203, Dec. 2011.

[69] B. J. Choi, A. C. Torrezan, K. J. Norris, F. Miao, J. P. Strachan, M.-X. Zhang, D. A. A. Ohlberg, N. P. Kobayashi, J. J. Yang, and R. S. Williams, "Electrical performance and scalability of Pt dispersed SiO2 nanometallic resistance switch.," Nano Lett., vol. 13, no. 7, pp. 3213–7, Jul. 2013.

[70] E. Pérez, A. Grossi, C. Zambelli, P. Olivo, and C. Wenger, "Impact of the Incremental Programming Algorithm on the Filament Conduction in HfO2-Based RRAM Arrays," vol. 5, no. 1, 2017.

[71] G. González-Cordero, J. B. Roldan, and F. Jiménez-Molinos, "Simulation of RRAM memory circuits, a Verilog-A compact modeling approach," in XXXI edition of the Design of Circuits and Integrated Systems Conference, 2016.

[72] F. M. Puglisi, L. Larcher, C. Pan, N. Xiao, Y. Shi, F. Hui, and M. Lanza, "2D h -BN based RRAM devices," in IEEE international Electron Devices Meeting (IEDM), 2016, pp. 874–877.

[73] Y. Luo, W. Chen, M. Cheng, and W. Yin, "Electrothermal Characterization in 3-D Resistive Random Access Memory Arrays," IEEE Trans. Electron Devices, vol. 63, no. 12, pp. 4720–4728, 2016.

[74] G. C. Adam, B. D. Hoskins, M. Prezioso, F. Merrikh-Bayat, B. Chakrabarti, and D. B. Strukov, "3-D Memristor Crossbars for Analog and Neuromorphic Computing Applications," IEEE Trans. Electron Devices, vol. 64, no. 1, pp. 312–318, 2017.

[75] P. Y. Chen, Z. Li, and S. Yu, "Design Tradeoffs of Vertical RRAM-Based 3-D Cross-Point Array," IEEE Trans. Very Large Scale Integr. Syst., vol. 24, no. 12, pp. 3460–3467, 2016.

[76] S. Balatti, S. Ambrogio, and D. Ielmini, "Normally-off Logic Based on Resistive Switches — Part I : Logic Gates," IEEE Trans. Electron Devices, vol. 62, no. 6, pp. 1831–1838, 2015.

[77] S. Kvatinsky, D. Belousov, S. Liman, G. Satat, N. Wald, E. G. Friedman, A. Kolodny, and U. C. Weiser, "MAGIC - Memristor-aided logic," IEEE Trans. Circuits Syst. II Express Briefs, vol. 61, no. 11, pp. 895–899, 2014.

[78] N. Wald and S. Kvatinsky, "Design Methodology for Stateful Memristive Logic Gates," Proc. Int. Conf. Sci. Electr. Eng. - Press, 2016.

[79] E. Lehtonen and M. Laiho, "Stateful implication logic with memristors," in 2009 IEEE/ACM International Symposium on Nanoscale Architectures, 2009, pp. 33–36.

[80] J. Borghetti, G. S. Snider, P. J. Kuekes, J. J. Yang, D. R. Stewart, and R. S. Williams, "'Memristive' switches enable 'stateful' logic operations via material implication.," Nature, vol. 464, no. 7290, pp. 873–876, 2010.

[81] G. C. Adam, B. D. Hoskins, M. Prezioso, and D. B. Strukov, "Optimized stateful material implication logic for three- dimensional data manipulation," Nano Res., vol. 9, no. 12, pp. 3914–3923, 2016.

[82] F. Zhou, L. Guckert, Y.-F. Chang, E. E. Swartzlander, and J. Lee, "Bidirectional voltage biased implication operations using SiOx based unipolar memristors," Appl. Phys. Lett., vol. 107, no. 18, p. 183501, 2015.

[83] G. Sharma and L. Bhargava, "Imply logic based on TiO2 memristor model for computational circuits," IEEE Int. Conf. Circuit, Power Comput. Technol. ICCPCT 2015, 2015.

[84] M. Teimoory, A. Amirsoleimani, J. Shamsi, A. Ahmadi, S. Alirezaee, and M. Ahmadi, "Optimized implementation of memristor-based full adder by material implication logic," 2014 21st IEEE Int. Conf. Electron. Circuits Syst. ICECS 2014, pp. 562–565, 2015.

[85] E. Linn, R. Rosezin, C. Kügeler, and R. Waser, "Complementary resistive switches for passive nanocrossbar memories," Nat. Mater., vol. 9, no. 5, pp. 403–406, May 2010.

[86] R. Aluguri and T. Y. Tseng, "Overview of selector devices for 3-D stackable cross point RRAM arrays," IEEE J. Electron Devices Soc., vol. 4, no. 5, pp. 294–306, 2016.

[87] L. A. Urry, M. L. Cain, S. A. Wasserman, P. V. Minosky, R. B. Jackson, and jane B. Reece, Biology in Focus, 1st editio. Pearson, 2013.

[88] K. Seo, I. Kim, S. Jung, M. Jo, S. Park, J. Park, J. Shin, K. P. Biju, J. Kong, K. Lee, B. Lee, and H. Hwang, "Analog memory and spike-timing-dependent plasticity characteristics of a nanoscale titanium oxide bilayer resistive switching device," Nanotechnology, vol. 22, no. 25, p. 254023, 2011.

[89] S. Yu, Y. Wu, R. Jeyasingh, D. Kuzum, and H. S. P. Wong, "An electronic synapse device based on metal oxide resistive switching memory for neuromorphic computation," IEEE Trans. Electron Devices, vol. 58, no. 8, pp. 2729–2737, 2011.

[90] T. Chang, S. H. Jo, and W. Lu, "Short-term memory to long-term memory transition in a nanoscale memristor," ACS Nano, vol. 5, no. 9, pp. 7669–7676, 2011.

[91] Y. Wu, S. Yu, H. S. P. Wong, Y. S. Chen, H. Y. Lee, S. M. Wang, P. Y. Gu, F. Chen, and M. J. Tsai, "AlOx-based resistive switching device with gradual resistance modulation for neuromorphic device application," 4th IEEE Int. Mem. Work. IMW 2012, vol. 1, 2012.

[92] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, and W. Lu, "Nanoscale memristor device as synapse in neuromorphic systems," Nano Lett., vol. 10, no. 4, pp. 1297–1301, 2010.

[93] M. Prezioso, F. Merrikh-Bayat, B. D. Hoskins, G. C. Adam, K. K. Likharev, and D. B. Strukov, "Training and operation of an integrated neuromorphic network based on metal-oxide memristors," Nature, vol. 521, no. 7550, pp. 61–64, 2015.

[94] M. Chu, B. Kim, S. Park, H. Hwang, M. Jeon, B. H. Lee, and B. G. Lee, “Neuromorphic Hardware System for Visual Pattern Recognition with Memristor Array and CMOS Neuron,” IEEE Trans. Ind. Electron., vol. 62, no. 4, pp. 2410–2419, 2015.

[95] S. Yu, Z. Li, P. Chen, H. Wu, B. Gao, D. Wang, W. Wu, and H. Qian, “Binary Neural Network with 16 Mb RRAM Macro Chip for Classification and Online Training,” in IEEE International Electron Device Meeting (IEDM), 2016, pp. 416–419.

[96] V. Milo, G. Pedretti, R. Carboni, A. Calderoni, N. Ramaswamy, S. Ambrogio, and D. Ielmini, “Demonstration of hybrid CMOS/RRAM neural networks with spike time/rate-dependent plasticity,” in IEEE International Electron Device Meeting (IEDM), 2016, pp. 440–443.

[97] S. Gaba, P. Knag, Z. Zhang, and W. Lu, “Memristive devices for stochastic computing,” in IEEE International Symposium on Circuits and Systmes (ISCAS), 2014, pp. 2592–2595.

[98] S. Gaba, P. Sheridan, J. Zhou, S. Choi, and W. Lu, “Stochastic memristive devices for computing and neuromorphic applications,” Nanoscale, vol. 5, no. 13, p. 5872, 2013.

[99] C. Herder, M. D. Yu, F. Koushanfar, and S. Devadas, “Physical unclonable functions and applications: A tutorial,” Proc. IEEE, vol. 102, no. 8, pp. 1126–1141, 2014.

[100] R. Pappu, B. Recht, J. Taylor, and N. Gershenfeld, “Physical One-Way Functions,” Science (80-.)., vol. 297, no. 5589, pp. 2026–2030, Sep. 2002.

[101] B. Gassend, D. Clarke, M. Van Dijk, and S. Devadas, “Silicon Physical Random Functions,” in Proceeding of the 9th conference on Computer and communications security, 2002, pp. 148–160.

[102] Y. Gao, D. C. Ranasinghe, S. F. Al-Sarawi, O. Kavehei, and D. Abbott, “Memristive crypto primitive for building highly secure physical unclonable functions.,” Sci. Rep., pp. 1–14, 2015.

[103] H. Abunahla, D. Shehada, C. Y. Yeun, B. Mohammad, and M. A. Jaoude, "Novel secret key generation techniques using memristor devices," AIP Adv., vol. 6, no. 2, 2016.

[104] D. Arumí, S. Manich, R. Rodríguez-Montañés, and M. Pehl, "RRAM Based Random Bit Generation for Hardware Security Applications," in IEEE International Verification and Security Workshop, 2016.

[105] A. Crespo-Yepes, J. Martin-Martinez, R. Rodriguez, M. Nafria, X. Aymerich, and A. Rothschild, "Resistive switching-like behaviour of the dielectric breakdown in ultra-thin Hf based gate stacks in mosfets," in Proceedings of the European Solid State Device Research Conference, 2010, pp. 138–141.

[106] J. Suñé, I. Placencia, N. Barniol, E. Farrés, F. Martín, and X. Aymerich, "On the breakdown statistics of very thin SiO2 films," Thin Solid Films, vol. 185, no. 2, pp. 347–362, Mar. 1990.

[107] E. Miranda, J. Sune, R. Rodriguez, M. Nafria, X. Aymerich, L. Fonseca, and F. Campabadal, "Soft breakdown conduction in ultrathin (3-5 nm) gate dielectrics," IEEE Trans. Electron Devices, vol. 47, no. 1, pp. 82–89, 2000.

[108] R. Degraeve, B. Kaczer, A. De Keersgieter, and G. Groeseneken, "Relation between breakdown mode and location in short-channel nMOSFETs and its impact on reliability specifications," IEEE Trans. Device Mater. Reliab., vol. 1, no. 3, pp. 163–169, 2001.

[109] B. Kaczer, R. Degraeve, A. De Keersgieter, K. Van de Mieroop, V. Simons, and G. Groeseneken, "Consistent model for short-channel nMOSFET after hard gate oxide breakdown," IEEE Trans. Electron Devices, vol. 49, no. 3, pp. 507–513, Mar. 2002.

[110] F. Crupi, B. Kaczer, R. Degraeve, A. De Keersgieter, and G. Groeseneken, "Location and hardness of the oxide breakdown in short channel n- and p-MOSFETs," in IEEE International Reliability Physics Symposium. Proceedings. 40th Annual (Cat. No.02CH37320), 2002, pp. 55–59.

[111] U. Russo, D. Ielmini, C. Cagli, A. L. L. Lacaita, S. Spiga, C. Wiemer, M. Perego, and M. Fanciulli, "Conductive-filament switching analysis and self-

accelerated thermal dissolution model for reset in NiO-based RRAM," in IEEE International Electron Devices Meeting, 2007, pp. 775–778.

[112] B. Chen, J. F. Kang, P. Huang, Y. X. Deng, B. Gao, R. Liu, F. F. Zhang, L. F. Liu, X. Y. Liu, X. A. Tran, and H. Y. Yu, "Multi-level resistive switching characteristics correlated with microscopic filament geometry in TMO-RRAM," in International Symposium on VLSI Technology, Systems and Application (VLSI-TSA), 2013, pp. 1–2.

[113] S. Larentis, F. Nardi, S. Balatti, D. C. Gilmer, D. Ielmini, S. Larentis, S. Balatti, D. C. Gilmer, and D. Ielmini, "Resistive Switching by Voltage-Driven Ion Migration in Bipolar RRAM—Part I: Experimental Study," IEEE Trans. Electron Devices, vol. 59, no. 9, pp. 2468–2475, Sep. 2012.

[114] N. Raghavan, R. Degraeve, L. Goux, A. Fantini, D. J. Wouters, G. Groeseneken, and M. Jurczak, "RTN insight to filamentary instability and disturb immunity in ultra-low power switching HfOx and AlOx RRAM," in Symposium on VLSI Technology Digest of Technical Papers, 2013, pp. T164–T165.

[115] S. Ambrogio, S. Balatti, A. Cubeta, A. Calderoni, N. Ramaswamy, and D. Ielmini, "Statistical Fluctuations in HfOx Resistive-Switchi," IEEE Trans. Electron Devices, vol. 61, no. 8, pp. 2920–2927, Aug. 2014.

[116] S. Balatti, S. Ambrogio, A. Cubeta, A. Calderoni, N. Ramaswamy, and D. Ielmini, "Voltage-dependent random telegraph noise (RTN) in HfOx resistive RAM," IEEE Int. Reliab. Phys. Symp., p. MY.4.1-MY.4.6, Jun. 2014.

[117] C. M. Compagnoni, R. Gusmeroli, A. S. Spinelli, and A. Visconti, "RTN VT Instability From the Stationary Trap-Filling Condition: An Analytical Spectroscopic Investigation," IEEE Trans. Electron Devices, vol. 55, no. 2, pp. 655–661, Feb. 2008.

[118] M. B. B. Gonzalez, M. C. C. Acero, O. Beldarrain, M. Zabala, and F. Campabadal, "Investigation of the resistive switching behavior in Ni/HfO2-based RRAM devices," in 10th Spanish Conference on Electron Devices (CDE), 2015, vol. 14, no. 2, pp. 1–3.

[119] A. Rodriguez, M. B. Gonzalez, E. Miranda, F. Campabadal, and J. Suñe, “Temperature and polarity dependence of the switching behavior of Ni/HfO2-based RRAM devices,” Microelectron. Eng., vol. 147, pp. 75–78, 2015.

[120] J. Diaz-Fortuny, M. Maestro, J. Martin-Martinez, A. Crespo-Yepes, R. Rodriguez, M. Nafria, and X. Aymerich, “Current-limiting and ultrafast system for the characterization of resistive random access memories,” Rev. Sci. Instrum., vol. 87, no. 6, p. 64705, Jun. 2016.

[121] M. Maestro, J. Diaz, A. Crespo-Yepes, M. B. Gonzalez, J. Martin-Martinez, R. Rodriguez, M. Nafria, F. Campabadal, and X. Aymerich, “A new high resolution Random Telegraph Noise (RTN) characterization method for resistive RAM,” in 2015 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon ULIS, 2015, pp. 133–136.

[122] A. Chen, “Current overshoot during set and reset operations of resistive switching memories,” in IEEE International Reliability Physics Symposium (IRPS), 2012, p. MY.2.1-MY.2.4.

[123] Agilent Technologies, “Agilent 4155C Semiconductor Parameter Analyzer Agilent 4156C Precision Semiconductor Parameter Analyzer User ’ s Guide : Measurement and Analysis,” 2008.

[124] C. Cagli, D. Ielmini, F. Nardi, and A. L. Lacaita, “Evidence for threshold switching in the set process of NiO-based RRAM and physical modeling for set, reset, retention and disturb prediction,” in IEEE International Electron Devices Meeting, 2008, pp. 1–4.

[125] C. Schindler, G. Staikov, and R. Waser, “Electrode kinetics of Cu–SiO2-based resistive switching cells: Overcoming the voltage-time dilemma of electrochemical metallization memories,” Appl. Phys. Lett., vol. 94, no. 7, p. 72109, 2009.

[126] L. Vandelli, A. Padovani, L. Larcher, G. Bersuker, D. Gilmer, and P. Pavan, “Modeling of the Forming Operation in HfO2-Based Resistive Switching

Memories," in 3rd IEEE International Memory Workshop (IMW), 2011, pp. 1–4.

[127] D. Ielmini, "Modeling the Universal Set/Reset Characteristics of Bipolar RRAM by Field- and Temperature-Driven Filament Growth," IEEE Trans. Electron Devices, vol. 58, no. 12, pp. 4309–4317, Dec. 2011.

[128] S. Long, X. Lian, C. Cagli, L. Perniola, E. Miranda, D. Jimenez, H. Lv, Q. Liu, L. Li, Z. Huo, M. Liu, and J. Sune, "Compact analytical models for the SET and RESET switching statistics of RRAM inspired in the cell-based percolation model of gate dielectric breakdown," in IEEE International Reliability Physics Symposium (IRPS), 2013, p. 5A.6.1-5A.6.8.

[129] H.-S. P. Wong, H.-Y. Lee, S. Yu, Y.-S. Chen, Y. Wu, P.-S. Chen, B. Lee, F. T. Chen, and M.-J. Tsai, "Metal-Oxide RRAM," Proc. IEEE, vol. 100, no. 6, pp. 1951–1970, Jun. 2012.

[130] P. Peng, D. Xie, Y. Yang, Y. Zang, X. Gao, C. Zhou, T. Feng, H. Tian, T. Ren, and X. Zhang, "Resistive switching behavior in diamond-like carbon films grown by pulsed laser deposition for resistance switching random access memory application," J. Appl. Phys., vol. 111, no. 8, p. 84501, 2012.

[131] F. M. Puglisi, L. Larcher, G. Bersuker, A. Padovani, and P. Pavan, "An Empirical Model for RRAM Resistance in Low- and High-Resistance States," IEEE Electron Device Lett., vol. 34, no. 3, pp. 387–389, Mar. 2013.

[132] Y. Nishi, K. Fleck, U. Bottger, R. Waser, and S. Menzel, "Effect of RESET Voltage on Distribution of SET Switching Time of Bipolar Resistive Switching in a Tantalum Oxide Thin Film," IEEE Trans. Electron Devices, vol. 62, no. 5, pp. 1561–1567, May 2015.

[133] F. M. Puglisi, L. Larcher, A. Padovani, and P. Pavan, "Bipolar Resistive RAM Based on HfO2: Physics, Compact Modeling, and Variability Control," IEEE J. Emerg. Sel. Top. Circuits Syst., vol. 6, no. 2, pp. 171–184, Jun. 2016.

[134] S. Ambrogio, S. Balatti, V. McCaffrey, D. C. Wang, and D. Ielmini, "Noise-Induced Resistance Broadening in Resistive Switching Memory—Part II:

Array Statistics," IEEE Trans. Electron Devices, vol. 62, no. 11, pp. 3812–3819, Nov. 2015.

[135] Jeonghwan Song, Jiyong Woo, A. Prakash, Daeseok Lee, and Hyunsang Hwang, "Threshold Selector With High Selectivity and Steep Slope for Cross-Point Memory Array," IEEE Electron Device Lett., vol. 36, no. 7, pp. 681–683, Jul. 2015.

[136] K. Bickerstaff and E. E. Swartzlander, "Memristor-based arithmetic," in Conference Record of the Forty Fourth Asilomar Conference on Signals, Systems and Computers, 2010, pp. 1173–1177.

[137] D. Mahajan, M. Musaddiq, and E. E. Swartzlander, "Memristor based adders," in 48th Asilomar Conference on Signals, Systems and Computers, 2014, pp. 1256–1260.

[138] S. Kvatinsky, G. Satat, N. Wald, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Very Large Scale Integration (VLSI) Systems, IEEE ," IEEE Trans. Very Large Scale Integr. Syst., vol. 22, no. 10, pp. 2054–2066, Oct. 2014.