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TESI DOCTORAL

Contributions to the Modulation and Closed-Loop Control of Multilevel Dual-Active-Bridge Dc-Dc Converters

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Tesis doctoral presentada per accedir al grau de Doctor per la Universitat Politècnica de Catalunya, dins del Programa de Doctorat en Enginyeria Electrònica

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“There are things known and there are things unknown, and in between are the doors of perception.”

Aldous Huxley

Agraïments

En primera instancia vull agrair al meu director de tesi, Sergi Busquets, l'oportunitat de realitzar la tesi doctoral en l'apassionant tema dels convertidors multinivell. El seu guiatge i els coneixements que m'ha transmès, han estat una gran ajuda en aquest llarg camí i m'han permès créixer com a enginyer i investigador. També vull agrair a en Josep Bordonau, director del Grup en Electrònica de Potència (GREP), l'oferta que em va proposar, ara fa sis anys, de treballar en aquest grup de recerca, que tot i ser petit, compta d'un gran potencial humà. A en Joan Nicolás, Alejandro Calle, Salvador Alepuz i resta de companys del GREP, els hi reconec el seu inestimable suport i els consells que m'han brindat en moments crucials. Als companys del departament, en especial a l'Álvaro Gómez, els dono les gràcies per donar-me un cop de mà quan els ho he demanat i per les conversacions disteses i amb gran sentit de l'humor (digne de la "Commedia") de l'hora del cafè.

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CONTENTS

ABSTRACT

Galvanically-isolated bidirectional dc-dc converters (IBDCs) have recently received more attention due to its increasing use in systems requiring energy transfer between two dc networks in both directions, requiring galvanic isolation and a high voltage gain. Some of these systems are energy storage systems, vehicle-to-grid power interfaces, fuel cell energy systems, uninterruptable power supplies, high-voltage dc links for electric-energy transmission, and solid-state transformers.

The most prominent IBDC, thanks to its good performance, is the dual-active-bridge (DAB) converter. It features a high power density, a wide dc-voltage gain working range, a low count of passive components, and an exceptional transformer utilization. Nevertheless, the DAB converter suffers from a significant performance deterioration when operating at conditions different from its nominal design working point. This problem has been alleviated by designing complex modulation schemes, which require a high computational effort and are highly dependent on the parasitic-component values.

On the other hand, as DAB converters have been lately introduced in high-power applications, higher voltages are needed in the dc links in order to achieve reasonable efficiency values. This has led to the use of multilevel topologies on the DAB converters, mainly multilevel neutral-point-clamped (NPC) topologies. However, the little and recent literature in this topic have not fully explored the operational capabilities and performance benefits of multilevel DAB converters.

The aim of this thesis is to study the viability of multilevel NPC DAB (ML-DAB) converters, where the major faced challenge is the dc-link capacitors voltage balancing. First, three particular ML-DAB converters are studied, with the same number of levels on each side; the three-level, four-level, and five-level topologies (3L-DAB, 4L-DAB, and 5L-DAB, respectively). Suitable switching sequences, modulation schemes, and control schemes are designed for the proposed ML-DAB converters. The converter switching and conduction losses are studied with three figures of merit, resulting in a set of practical solutions that define the modulation parameters and achieve satisfactory converter-performance figures. These results are then generalized to the *N*-level topology (*N*L-DAB). Finally, the feasibility of ML-DAB converters with an asymmetric number of levels is also demonstrated.

NOMENCLATURE

Acronyms and Abbreviations

IBDC	Galvanically-isolated bidirectional dc-dc converter.
HF	High frequency.
DAB	Dual-active-bridge (converter).
DFB	Dual-full-bridge converter.
FB-DAB	Full-bridge two-level single-phase DAB converter.
HB-DAB	Half-bridge two-level single-phase DAB converter.
ZVS	Zero-voltage switching.
ZCS	Zero-current switching.
PSM	Phase-shift modulation.
TRM	Triangular current modulation.
TZM	Trapezoidal current modulation.
DoF	Degree of freedom.
NPC	Neutral-point clamped.
MAC	Multilevel active clamped.
MOSFET	Metal-oxide-semiconductor field-effect transistor.
IGBT	Isolated gate bipolar transistors.
THD	Total harmonic distortion.
rms	Root mean square.
ML	Multilevel.
3L	Three level.
4L	Four level.
5L	Five level.
ML-DAB	Multilevel DAB converter employing NPC phase legs.
3L-DAB	Full-bridge single-phase DAB converter employing 3L-NPC phase legs.

4L-DAB	Full-bridge single-phase DAB converter employing 4L-NPC phase legs.
5L-DAB	Full-bridge single-phase DAB converter employing 5L-NPC phase legs.
NL-DAB	Full-bridge single-phase DAB converter employing NL-NPC phase legs.
N_aL-N_bL-DAB	Full-bridge single-phase DAB converter employing N_aL-NPC phase legs on side a and N_bL-NPC phase legs on side b.

Symbols

Converter topology parameters

$z \in \{\mathrm{a}, \mathrm{b}\}$	Side of the converter.
N	Number of levels of both sides dc-links.
M	Number of capacitors on both sides dc-link. Also, number of α_{zk}, α_{zik}, or α_{zok} switching angles per side.
N_z	Number of levels of z-side dc-link (on asymmetric ML-DAB).
m_z	z-side dc-link point m.
z_1, z_2	z-side phase legs or outputs of the phase legs.
n	Transformer-secondary number of turns per turn on the primary side.
d	a-side referred converter dc-voltage gain.

Passive values

L	a-side referred transformer leakage inductance.
C_z	Capacitance of the z-side dc-link capacitors.

Voltages

v_{Czk}, $k \in \{1,2,\ldots,M\}$	z-side dc-link capacitor number k voltage.
V_Z	z-side dc-link voltage.
v_{z1}, v_{z2}	z-side phase legs z_1 and z_2 voltages, respectively, with respect to voltage level connection point 1_z.
v_z	z-side transformer-windings voltage.
$v_{z,1}$	Fundamental component of v_z.
V_o^*	Output voltage control setpoint value.

Currents and charges

i_Z	z-side dc-link port current.
i_{mz}	m_z dc-link connection point current.
i_z	z-side transformer current.
$i_{z,1}$	Fundamental component of i_z.
$i_{z,h}$	h^{th} harmonic of i_z.
$i_{z,1}^{\text{p}}$	In-phase component, with respect to $v_{z,1}$, of $i_{z,1}$.
$i_{z,1}^{\text{q}}$	In-quadrature component, with respect to $v_{z,1}$, of $i_{z,1}$.
$i_{z,h}^{\text{p}}$	In-phase component, with respect to v_z h^{th} harmonic, of $i_{z,\text{h}}$.
$i_{z,h}^{\text{q}}$	In-quadrature component, with respect to v_z h^{th} harmonic, of $i_{z,h}$
$I_{\text{a,rms}}$	i_{a} rms value over a switching period.
$I_{\text{sw,I}}$, $I_{\text{sw,II}}$	Phase leg instantaneous switching current of Type I and Type II switching transitions, respectively.
q_{mz}	Electrical charge provided to m_z inner dc-link point.

Power and energy

P	Converter transferred power.
E_{sw}	Energy lost in a lossy switching transition.

Modulation parameters

φ	Phase shift between v_a and v_b.
α_{zk}, $k \in \{1,2,\ldots,M\}$	z-side switching angles defining v_z with quarter-wave symmetry.
$\alpha_{zik}, \alpha_{zok}$ $k \in \{1,2,\ldots,M\}$	z-side inner and outer switching angles, respectively, defining v_z with odd symmetry.
Δ_{zr}, $r \in \left\{1,2,\ldots,\left\lfloor \frac{M}{2}-1 \right\rfloor\right\}$	Difference between $\alpha_{z(r+1)}$ and α_{zr} sines and between $\alpha_{z(M-r+1)}$ and $\alpha_{z(M-r)}$ sines, on side z.

Control parameters

y_{zm}, $m \in \{2,3,\ldots,M\}$	Unbalance variable related to inner dc-link point m_z.
y^*_{zm}	y_{zm} control objective value.
e_{zm}	Error between y^*_{zm} and y_{zm}.
u_{zm}	Control variable of the control loop regulating y_{zm}.
$H_{filt}(s)$	Low-pass filter transfer function to filter the capacitor voltages.
$G_{zm}(s)$	Controller transfer function of the control loop regulating y_{zm}.
$k_{P,zm}$ $T_{I,zm}$	Proportional-integral regulator constants.

Time and frequency

f_s	Switching frequency of the converter.
T_s	Switching cycle time. Inverse of f_s.
$t_{b,z}$	Blanking time left between voltage-level switching transitions on side z.

CHAPTER 1.

INTRODUCTION

Abstract — This opening chapter presents a review, from its inception to the current state of the art, of galvanically-isolated bidirectional dc-dc converters (IBDCs) most common structures and modulation strategies. First, two-level IBDCs topologies are reviewed. Then, an overview of the typical multilevel dc-ac topologies is introduced. Finally, a survey of the current state of the art of multilevel IBDCs is introduced. This chapter concludes with the selection of a best case study and the definition of the thesis objective and the thesis outline.

Galvanically-isolated bidirectional dc-dc converters (IBDCs) can be classified according to the number of supply/sinking power ports and the number of stages that form them. For the present study of the state of the art, only two-port single-stage IBDCs are considered, as these are the most common. Other types of IBDCs are out of the scope of the thesis.

1.1. Two-port single-stage IBDCs common structure

Two-port single-stage IBDCs present the common structure shown in Fig. 1.1. Two subcircuits (a and b) are identified at both sides of the high frequency (HF) transformer. Each subcircuit has on one of its ends a dc port, with the capability of either sourcing or sinking power. Both subcircuits are composed of three blocks. The structure is symmetrical at both sides of the HF transformer. The circuit topology of the corresponding blocks at both sides does not necessarily need to be the same; hence, the symmetry might only exist at the block-structure level.

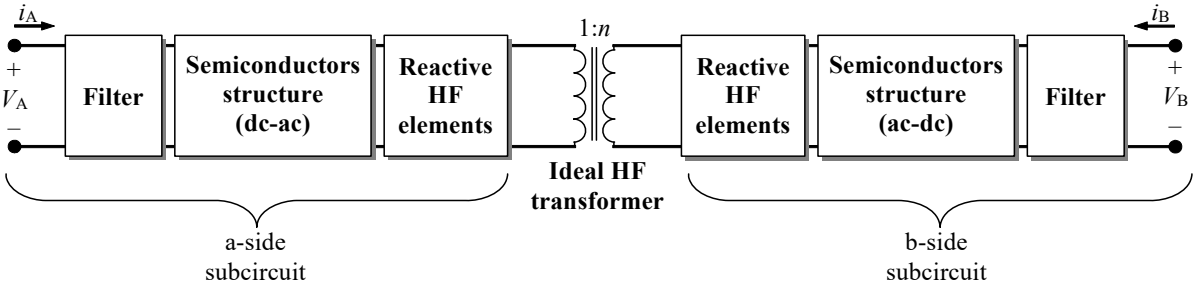


Fig. 1.1. Blocks composing the common structure of two-port single-stage IBDCs.

The blocks are:

- **Filter**: They deliver a smooth (ideally constant) current or voltage at the ports of the IBDC. At least a capacitor (for a voltage-sourced port) or an inductor (for a current-sourced port) must be employed on each filter. However, the present study will only

consider IBDCs with filters that present a voltage source at the converter dc port; i.e., voltage-sourced converters.

- **Semiconductors structure**: The dc-ac and ac-dc semiconductor structure blocks consist of a set of semiconductors properly interconnected to control the power flow between ports a and b by providing/receiving ac power through the HF transformer. To achieve power transmission from a to b and vice versa, these semiconductor blocks must be capable of bidirectional power flow.
- **Reactive HF elements**: Permit the storage of energy in order to transfer power between both sides, as well as shaping the switch currents properly in order to achieve low switching losses. These are always implicitly present due to the parasitic and nonideal components of the HF transformer (stray and magnetizing inductances and parasitic capacitances).
- **HF transformer**: Mandatory to achieve galvanic isolation. Its turn ratio can be designed properly in order to achieve the desired voltage and current ratios between the converter ports. As opposite to line-frequency transformers, HF transformers are smaller and have a reduced cost.

1.2. Types of non-multilevel two-port single-stage IBDCs

This section presents a brief description of the operation, advantages, and drawbacks of the different converters in the non-multilevel two-port single-stage IBDCs family.

1.2.1. Low switch-count converters

IBDCs with a low number of switches (both active and passive) can be represented by three main topologies: The bidirectional flyback converter (BF) ([1], [2], Fig. 1.2(a)), the bidirectional forward-flyback converter (BFF) ([3], [4], Fig. 1.2(b)) and the bidirectional isolated Ćuk converter (BIC) ([5], [6], Fig. 1.2(c)). These topologies present a capacitor as a filter on each side, while the reactive HF elements are the transformer magnetizing inductance(s) reflected on each side of the transformer(s). Low switch-count IBDCs are restricted to low- and medium-power applications (less than 2 kW), due to the stresses induced in the switches, caused by large current and voltage spikes. All of them present the main advantages of being simple circuits and having a low number of switches, although the switches are operated with hard-switching transitions and active clamping is required to improve efficiency, which increases the number of switches and discrete devices ([6] requires two switches, four diodes, two capacitors, and two inductors for the active snubber circuits). The BIC has a better HF transformer utilization (defined as P/S_T, where P is the converter output

power and S_T is the transformer VA rating) compared to the BF and BFF, although the BIC requires two extra inductors and two extra capacitors, all four components rated at the full transformer current.

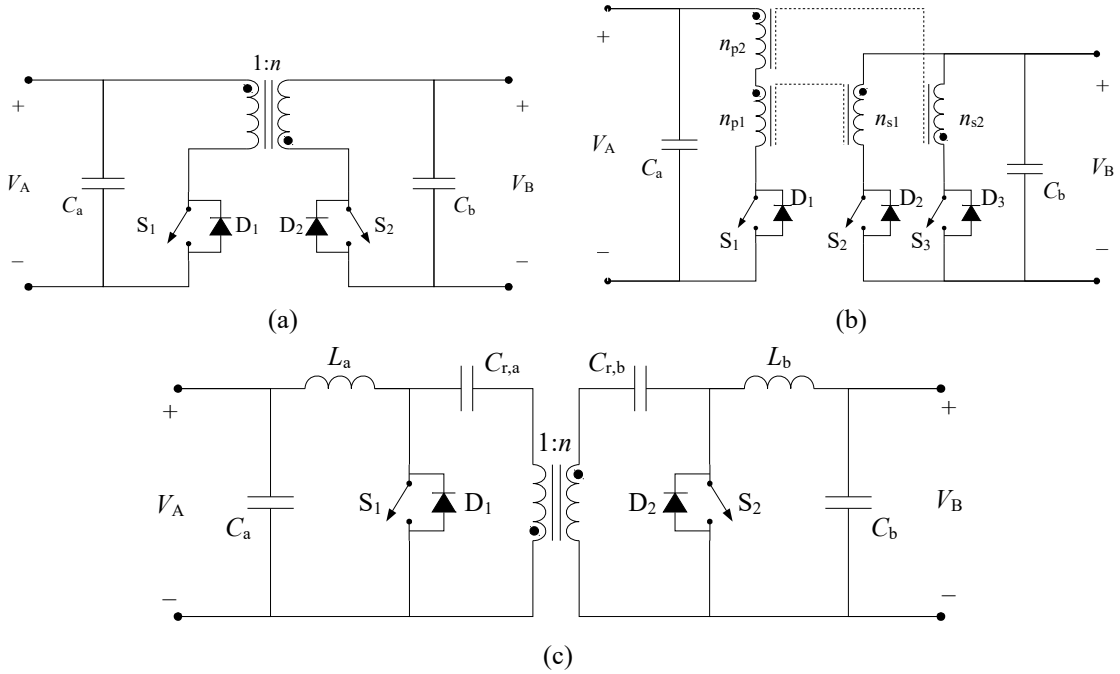


Fig. 1.2. Three types of low switch count IBDCs. (a) BF. (b) BFF. (c) BIC.

1.2.2. High switch-count converters

In high switch-count IBDCs, each semiconductor structure block (Fig. 1.1) is composed by topologies comprising two or more switches, primarily bridge type topologies, while the reactive HF elements present a non-resonant configuration [7]–[9]. Two types of converters are defined depending on the role of its reactive HF element (usually determined by the transformer leakage inductance): the dual-active-bridge (DAB) converters, where the HF elements are employed as the power-transferring element, and the dual-bridge converters, where the HF elements do not alter the transferred power capability (in fact, it may become a nuisance, due to the eventual series connection of them with an external inductance). Compared with the low switch-count converters, the high switch-count converters can achieve greater transferred-power levels, realize soft-switching transitions, present a lower number of passive components, and have greater HF transformer utilization, therefore leading to higher power-density values.

1.2.2.1. Single-phase dual-bridge converters

The conventional (unidirectional) isolated buck converter [10] (Fig. 1.3) can be extended to a bidirectional converter by parallelizing a switch (diode) to existing diodes (switches), as seen in Fig.

1.4. Such converter is named dual-full-bridge converter (DFB), and was first proposed in [11] and improved in [12]–[14]. Both converter ports are voltage sourced, with a capacitor on the a-side filter and an LC network on the b-side filter. This configures the semiconductor structures as a voltage-sourced full bridge on side a and a current-sourced full bridge on side b. The a-side referred L_B inductance has a higher value than the leakage inductance of the transformer (L). The turns ratio of the transformer is limited to $n > V_{B,max}/V_{A,min}$, where $V_{A,min}$ and $V_{B,max}$ are V_A minimum value and V_B maximum value, respectively, on its specified working range. This leads to the need of special circuitry for the start-up process [13].

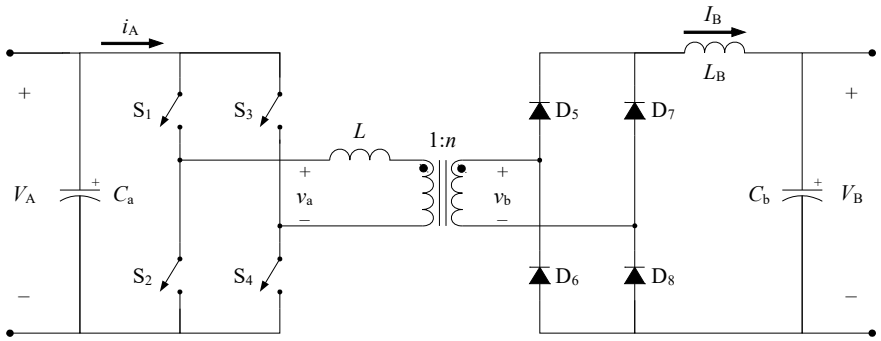


Fig. 1.3. Unidirectional isolated buck converter.

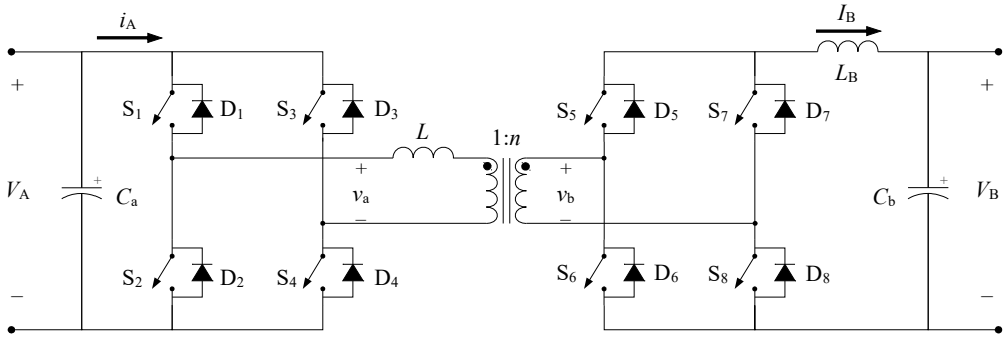


Fig. 1.4. Bidirectional isolated DFB.

The modulation employed in the DFB varies depending on the power flow direction. When power goes from a-side to b-side, the a-side bridge synthetizes voltage v_a across the primary transformer winding, while the b-side full-bridge actively rectifies reflected voltage v_b, and the second order filter, formed by inductor L_B and capacitor C_b, filters it. When power is transferred from b-side to a-side, the b-side bridge forces I_B into the secondary transformer winding, which is later rectified by the a-side full bridge, and filtered by capacitor C_a.

The DFB enables zero-voltage switching (ZVS) transitions on the a-side bridge and zero-current switching (ZCS) transitions on the b-side bridge, which together with a high switching frequency, permits to achieve a high power density [7], [9], [12]–[14]. Capacitor C_b can be smaller than C_a, thanks to the smooth current that flows through L_B, but the volume that this inductor adds should be considered. A great disadvantage of the DFB, is the need of snubber circuitry to mitigate the voltage spikes caused by the repeated connection/disconnection in series of L with L_B [7], [9].

1.2.2.2. Single-phase DAB converters

The single-phase DAB (2L-DAB) converter is the most prominent topology among the two-port single-stage IBDCs. It can be built with different types of switching and filter networks. However, the most known and first of its kind is the full-bridge DAB converter [FB-DAB, Fig. 1.5(a)], first introduced in 1988 [15], later developed in 1991 [16], and patented in 1994 [17]. The half-bridge DAB converter [HB-DAB, Fig. 1.5(b)], introduced in 1992 [18] is also a common topology, mostly employed in low-power applications [19].

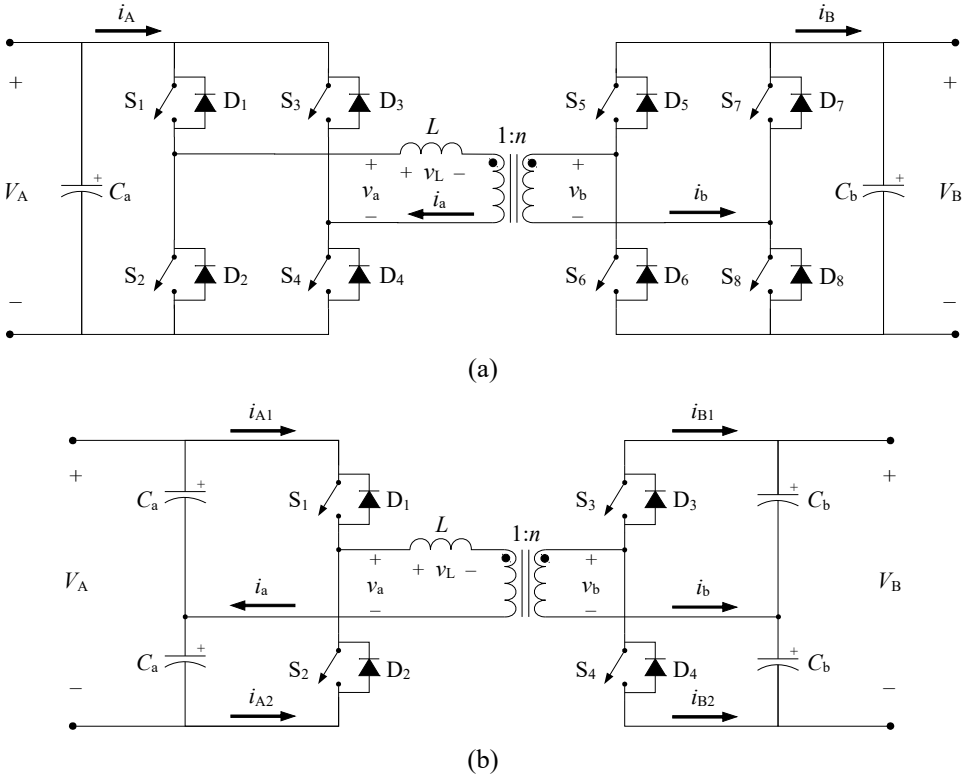


Fig. 1.5. Single-phase DAB converters. (a) FB-DAB. (b) HB-DAB.

The HB-DAB requires half the number of switches of the FB-DAB, but each switch on the HB-DAB must have a VA rating two times the VA rating of each switch on the FB-DAB [20]. Nevertheless, both converters present lower switch VA ratings and do not require snubber circuit

networks, compared to the DFB. For the same transformer cross-sectional area, the HB-DAB presents half of the transformer flux swing compared to the full-bridge version [21], which results in less core losses. However, the rms transformer current is doubled in the half-bridge version [20], which increases considerably the conduction losses. All the comparisons are made assuming the same converter power level. Moreover, both present the advantages of having a lower number of passive components and a better transformer utilization compared to the dual-bridge converters, having a symmetric structure, an even distribution of the current within the switches, an inherent soft-switching capability, and a higher power density [16], [18].

The key component of the single-phase DAB converters is inductance L (either the transformer leakage inductance or the sum of an external inductance plus the transformer leakage inductance), as it is used to transfer power between both sides. Various modulation strategies exist that define the switching patterns for the FB-DAB and HB-DAB bridges in order to achieve a proper power transfer. The simplest is the conventional phase-shift modulation (PSM) [16], also called rectangular modulation. This modulation presents the same working principle for either the FB-DAB and the HB-DAB, and it consists on applying a square-wave ac voltage (v_a and v_b) on each side of the HF transformer, synthesizing leakage inductance voltage $v_L = v_a - v_b/n$. Voltages v_a and v_b are phase-shifted φ degrees, hence building i_a ac current upon the inductance. This current is rectified by both sides bridges, generating currents i_A and i_B in the FB-DAB, and currents i_{A1}, i_{A2}, i_{B1} and i_{B2} (the currents of the four switches) in the HB-DAB, which contain a dc component plus a ripple. Hence, phase shift φ is used to control the power transferred between both sides. Moreover, when $\varphi > 0$, power is transferred from a-side to b-side, and when $\varphi < 0$, power is transferred from b-side to a-side. Relevant voltage and current waveforms are presented in Fig. 1.6(a) for the FB-DAB and in Fig. 1.6(b) for the HB-DAB.

The equations defining the FB-DAB and HB-DAB average transferred power with the PSM are

$$P_{FB} = \frac{V_A^2}{2\pi \cdot f_s \cdot L_{s,a}} \cdot d \cdot \varphi \left(1 - \frac{|\varphi|}{\pi}\right) \tag{1.1}$$

and

$$P_{HB} = \frac{V_A^2}{8\pi \cdot f_s \cdot L_{s,a}} \cdot d \cdot \varphi \left(1 - \frac{|\varphi|}{\pi}\right) \tag{1.2}$$

respectively, where, $d = V_B/(n \cdot V_A)$ is the a-side-referred voltage gain of the converter, f_s is the switching frequency of the converter (in Hz), and φ is in radians.

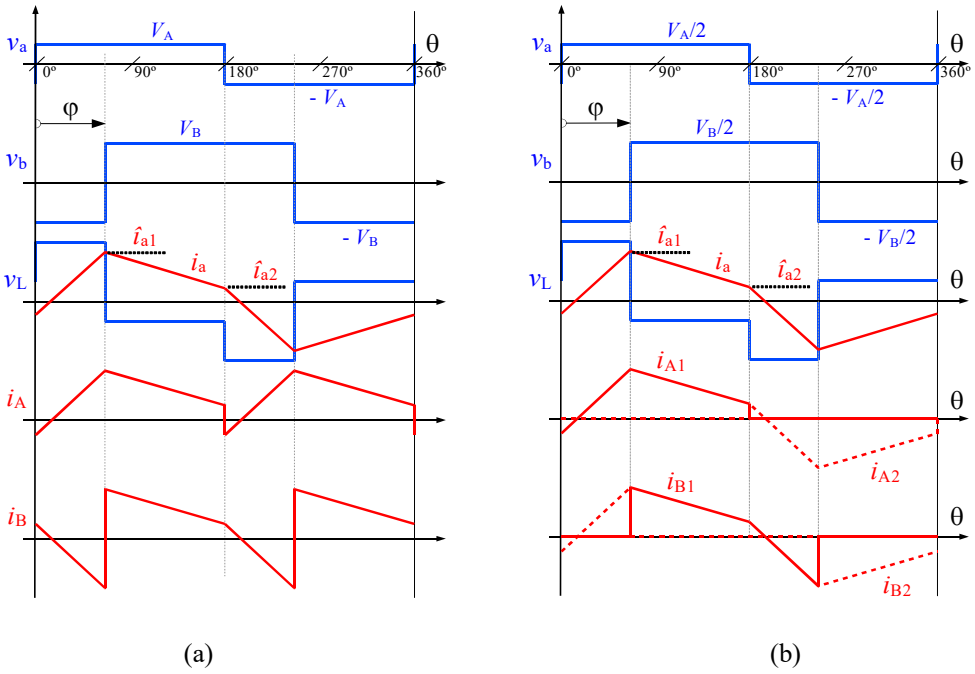


Fig. 1.6. Time-dependent waveforms related to the presented single-phase DAB converters when employing the PSM and $V_A < V_B/n$. (a) FB-DAB. (b) HB-DAB.

It can be observed that for the same converter port voltages, L value, turns ratio, and switching frequency, the maximum transferred power achievable by the HB-DAB is one fourth of that of the FB-DAB. Fig. 1.7(a) shows the plot of (1.1) in per-units [base power equal to $P_{base} = V_A^2/(2\pi \cdot f_s \cdot L)$]. It can be seen that the maximum transferred power is achieved when $|\varphi| = 90º$. Negative power values imply that power is transferred from side b to side a.

One of the main advantages of the DAB converters operated with the PSM is that switching losses are reduced thanks to the achievement of soft-switching transitions (more precisely, ZVS turn-on switching transitions). This is only achieved when current levels $\hat{\imath}_{a1}$ and $\hat{\imath}_{a2}$ (Fig. 1.6) are of equal sign. This condition is only met for a given value range of d and φ, corresponding to the cyan-shaded area in Fig. 1.7(a).

Due to the phase between v_a and i_a and between v_b and i_b, part of the power delivered to the load is returned to the power source; i.e., reactive power is present. Since neither the transformer voltages nor currents are sinusoidal, the reactive power cannot be computed as in pure-sinusoidal conditions. Moreover, there is no consensus on which is the best method to compute the reactive power in such condition [22]. One of these methods, employed to specifically compute the FB-DAB

reactive power, is proposed in [23]. In it, reactive power is defined with two terms; the reactive power defined by the voltage and current components with the same frequency plus the reactive power defined by the voltage and current components with different frequency. For the PSM, that is

$$Q = \sqrt{\sum_{h=1,3,5,\ldots} Q_h^2 + \sum_{g\neq h=1,3,5,\ldots} Q_{g\neq h}^2} \tag{1.3}$$

where

$$\begin{aligned} Q_h &= \frac{4V_A^2}{\pi^3 h^3 \cdot f_s \cdot L}\left[1 - d\cdot\cos\left(h\cdot\varphi\right)\right] \\ Q_{g\neq h} &= \frac{4V_A^2}{\pi^3 h^2 \cdot g \cdot f_s \cdot L}\sqrt{\left(d\cdot\cos\left(h\cdot\varphi\right)-1\right)^2 + \left(d\cdot\sin\left(h\cdot\varphi\right)\right)^2}. \end{aligned} \tag{1.4}$$

Fig. 1.7(b) presents the per-unit values of Q [using the same base power as in Fig. 1.7(a)]. A high reactive power value implies that high circulating currents are present on the converter; i.e., high transformer and dc-link capacitors rms currents [24]. This relation is manifested when comparing Fig. 1.7(b) with the transformer rms current ($I_{a,rms}$), shown in Fig. 1.7(c). Moreover, significant Q and $I_{a,rms}$ values are present at low-power levels when $d \neq 1$, hence reducing drastically the efficiency of the converter, due to high conduction losses and high switching losses (soft switching is lost at those working points). For $90^o \leq |\varphi| \leq 180^o$, although soft switching is achieved for the whole range of d, high conduction losses exist, turning this operating range ineffective. Hence, if reasonable efficiency values must be ensured when employing the PSM, the phase-shift value corresponding to the desired maximum transferred power should be close to $\varphi = 60^o$, or, as an alternative, the operating range must be confined close to the nominal operating point ($d = 1$).

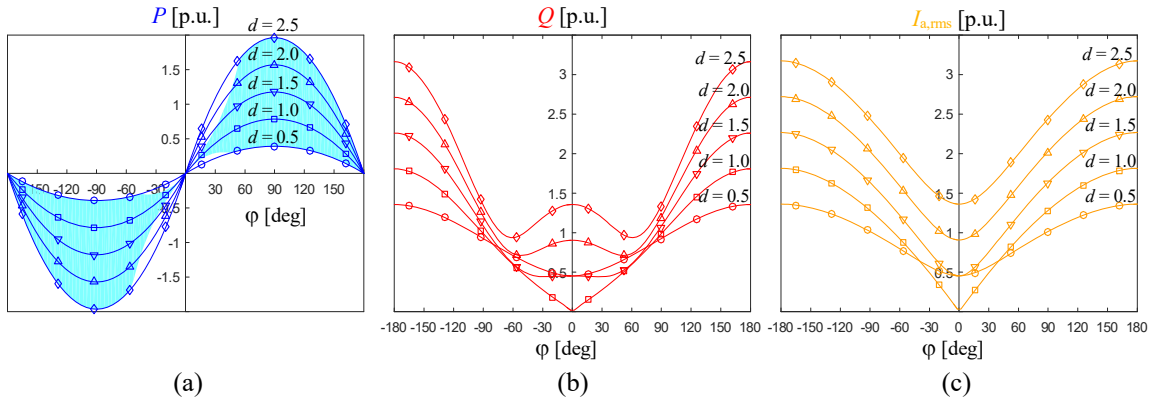


Fig. 1.7. Plots of relevant single-phase DAB converter figures when employing the PSM. (a) Per-unit transferred active power. The cyan-shaded area indicates the region where the converter has soft-switching capability. (b) Per-unit reactive power. (c) Per-unit transformer rms current [$I_{base} = V_A/(2\pi f_s \cdot L)$].

To overcome the drawbacks of the PSM when $d \neq 1$, various studies have proposed new modulation schemes that take advantage of the degrees of freedom (DoF) implicit in the FB-DAB and HB-DAB topologies. It should be noted that the PSM only employs one DoF; i.e., the phase shift.

Regarding the FB-DAB, most alternative modulations are focused on the DoF derived from the FB-DAB capability to generate zero voltage across both bridges, hence synthesizing three-level voltage waveforms across the transformer windings. Moreover, such voltage waveforms present quarter-wave symmetry with dwell times defined by duty-cycle variables D_a and D_b (Fig. 1.8). Both duty cycles plus the phase shift sum up to three available DoF.

References [24]–[29] present modulation strategies using only two of the above mentioned DoF. References [24], [27], [29] define $D_a = D_b$, while in [25], [26], [28], $D_a = 1 \wedge D_b \in [0,1]$ when $d > 1$ and $D_a \in [0,1] \wedge D_b = 1$ when $d < 1$. On the other hand, modulation strategies from [23], [30]–[40] employ the three DoF.

The majority of the aforementioned modulations focus on reducing the conduction losses by minimizing an objective function, equivalent to the converter reactive power [23], [24], [27], [28] or to the transformer rms current [27], [33], [34], [36]. Such modulations, however, cannot achieve soft switching over the whole d and P ranges.

Other modulations are focused on reducing the switching losses by either minimizing the current stress on the switches; i.e., the maximum absolute transformer current value [27], [29], [38], or by actively shaping the transformer current in order to achieve ZVS or ZCS transitions over the whole d and P ranges. The second strategy was first devised in [25] and later evolved to the triangular current modulation (TRM) and trapezoidal current modulation (TZM) [30], [31], [39], and its further improved variants [32], [35], [40]. The typical voltage and current waveforms of the TRM and TZM can be seen in Fig. 1.8. The TRM is only feasible when $V_A << V_B/n$ or $V_A >> V_B/n$, has a lower maximum-power-transfer capability than the TZM and the PSM, while the TZM builds the current waveform without zero-current intervals, and its maximum-power-transfer capability is higher than the TRM but lower than the PSM. Nevertheless, both modulations present high rms currents at medium and high power levels and an uneven sharing of the switching losses between the switches. It should be noted that [34] optimum results minimizing $I_{a,rms}$, reveal that the optimum modulation strategy tends to the TRM for low powers and PSM for high powers. For medium powers, an optimal transitional modulation is defined.

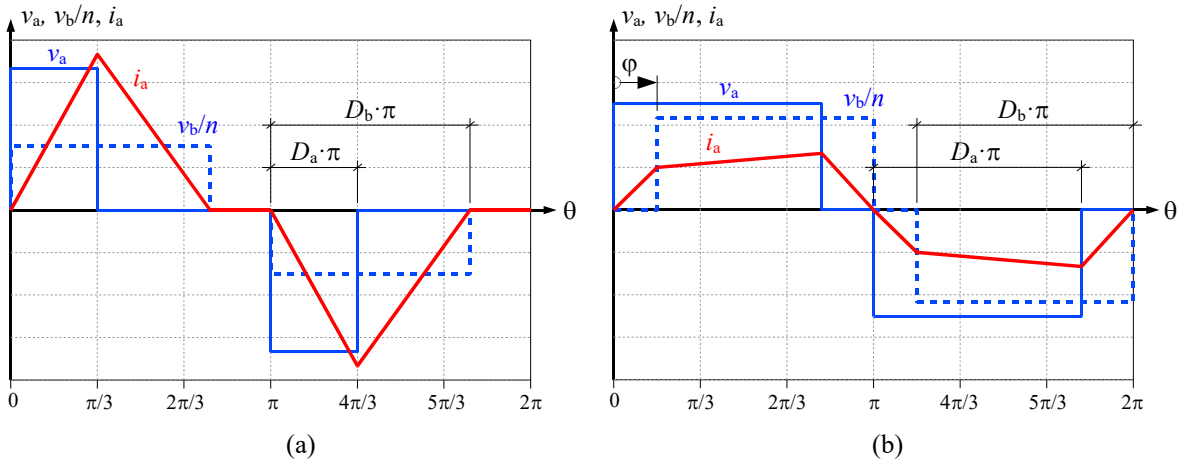


Fig. 1.8. Transformer current (i_a) and voltages (v_a, v_b) for two types of modulations. (a) TRM. (b) TZM.

Modulations presented in [26], [35] minimize an objective function defined as the sum of the overall converter losses (conduction, switching and core losses). Although such modulations obtain closed-form expressions defining the optimal modulation parameters, these expressions are complex, require a high computational effort (although a look-up table implementation is possible), and make the converter performance strongly dependent to the unpredictable values of the parasitic components.

Finally, references [41], [42] make use of an additional DoF present in the modulation parameters; i.e., the switching frequency. Reference [41] finds the optimum D_a or D_b and φ values plus an optimum set of f_s discrete values, to achieve minimum $I_{a,rms}$ and ZVS transitions for the desired transferred power value. On the other hand, [42] adjusts f_s and φ in order to minimize the converter reactive power.

As for other DAB topology variants, the HB-DAB can be operated with asymmetric transformer voltage waveforms [19]; i.e., v_a and v_b present unequal dwell times for the positive and negative pulses. Therefore, three DoF are present in the HB-DAB, which are the duty cycles defining the positive pulses of v_a and v_b plus the phase shift. Such asymmetrical operation leads to unbalance of the dc-link capacitors [43], although this is not an issue since the switches blocking voltage is the whole dc-link voltage in any case. Reference [19] employs two DoF from the three above defined, particularly φ and the transformer voltages duty cycles, equal on both sides. The proposed modulation scheme achieves minimum transformer rms current, although with loss of ZVS at light loads and $d \neq 1$. A second modulation scheme is proposed that achieves ZVS, but with greater transformer rms currents.

As a side note, the asymmetrical operation of the transformer voltages on the FB-DAB would not be wise. The presence of a transformer-voltage dc component on either side of the transformer,

would cause a steady-state transformer dc current due to the transformer magnetizing inductance and winding resistances, leading to higher conduction, switching, and core losses, and the risk of transformer saturation [19], [44], [45]. Although this is also true for the HB-DAB, such dc current is blocked by the dc-link capacitors in steady-state regime.

Overall, all the presented alternative modulations achieve greater converter efficiency figures than those obtained with the PSM when $d \neq 1$, particularly at medium and high transferred power values.

1.2.2.3. Three-phase DAB converter

The three-phase DAB converter was first presented in its voltage-sourced version in [16] (Fig. 1.9), together with the single-phase FB-DAB [Fig. 1.5(a)]. Posterior studies can be found in [46]–[52]. Its semiconductor structure blocks consist of six half bridges (three on each side) and the reactive HF elements are formed by three HF transformers and its leakage (or independent) inductances (L), where the windings on each side are Y-connected, as seen in Fig. 1.9. A single three-phase HF transformer can also be employed. The modulation used in the three-phase DAB [16], [46] is similar to the PSM used in the single-phase DAB converter. On each side, each half bridge synthesizes a two-level square voltage waveform, each one consecutively shifted 120º from the other. Phase voltages $v_{p,a}$ and $v_{p,b}$ ($p \in \{1,2,3\}$) present five voltage levels, two more than what can be achieved in the single-phase FB-DAB converter. Consequently, the current waveform in each phase, in the input/output ports, and in the capacitors are smoother and with a lower rms value and harmonic content. The VA rating of the transformer and switches is also greatly reduced compared to the single-phase DAB converters, and hence high converter power densities can be achieved [16]. However, poor efficiency is achieved if operated at $d \neq 1$, and no alternative modulations are feasible (no zero-voltage intervals can be synthesized in the half-bridge voltages).

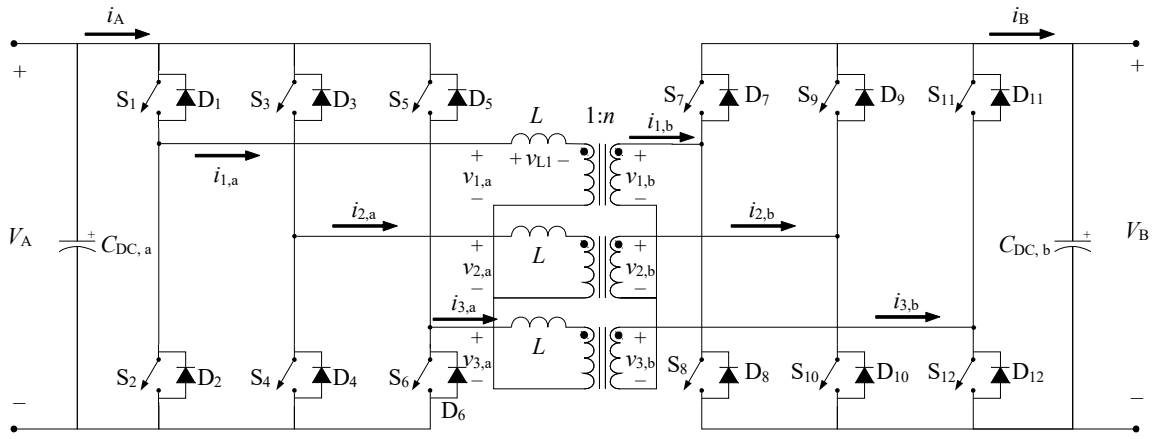


Fig. 1.9. Three-phase DAB converter.

By combining various primary and secondary transformer winding configurations (Y-Y, Y-Δ, and Δ-Δ), different performance levels can be achieved with the three-phase DAB converter, as shown in [49]. The study reveals that, for power levels between 50 % and 80 % of the maximum power, the Y-Δ configuration features a wider ZVS region and lower current stress on the switches, transformer, and capacitors.

Similar to [19] regarding the HB-DAB, [50], [51] propose a modulations where transformer asymmetrical voltage waveforms are generated, hence gaining two DoF with respect to the conventional PSM, which permit increasing the ZVS region [50] and decrease the transformer rms currents [51]. However, such modulation causes an increase of the dc-link capacitors rms current and an unequal power-loss distribution among the switches.

A variation of the three-phase DAB converter was presented in [52], where full-bridges are used on each phase of side a, making the transformer voltages independent one from another. This permits zero-voltage intervals on the a-side transformer voltages and increases the DoF, which, in the same manner to the alternative modulations of the single-phase DAB converters, can be used to reduce the reactive power, extend the soft-switching range, and overall, increase the efficiency, as demonstrated by [52].

1.3. Multilevel voltage-source topologies

Multilevel voltage-source topologies are characterized by the number of dc-voltage levels available to synthesize the output ac voltage, and can be classified in three basic families according to its topology [53]; flying capacitor, cascaded full bridges with separate dc sources, and neutral-point clamped (NPC).

1.3.1. Flying-capacitor topologies

Flying-capacitor topologies (also called capacitor-clamped topologies) were first introduced in [54]. Fig. 1.10 presents one leg of a three-level flying-capacitor converter. The number of switches employed is $2(N-1)$, where N is the number of available voltage levels. The problem of this topology is the high volume of capacitors needed, which compromises the converter power density, and the need of a controlled process to precharge these capacitors.

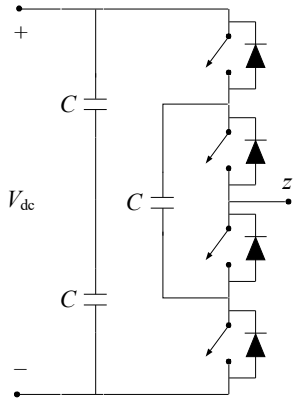


Fig. 1.10. Three-level flying-capacitor converter leg.

1.3.2. Cascaded full-bridge topologies

As its name indicates, the cascaded full bridge topology (originally introduced in [55]) is built upon the series connection of the outputs of single-phase full bridges, each one with a separate dc voltage source, and all of the same value. Fig. 1.11 shows one leg of a five-level cascaded full bridge converter. The number of voltage levels of v_o is equal to $2k + 1$, where k is the number of independent dc voltage sources.

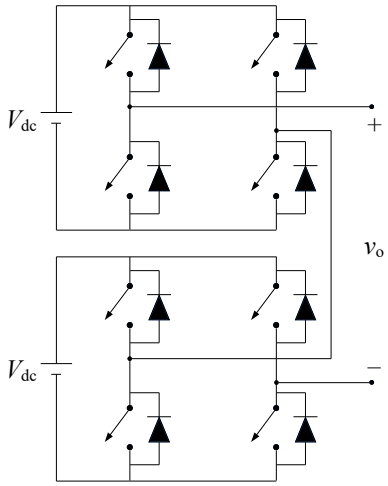


Fig. 1.11. Five-level cascaded full bridge topology.

Further variations of the cascaded full bridge topology are asymmetric configurations, which give different values to the adjacent dc-sources in order to increase the number of v_o voltage levels, while maintaining the same number of dc-sources. These variations are called the binary [56], the quasi-linear [57], and the trinary [58]. Each one can achieve a maximum number of voltage levels of

$2^{k+1}-1$, $2\cdot3^{k-1}$, and 3^k, respectively. The presented variations have greater advantages than the classic full bridge topology, but different voltage-rated switches and capacitors must be employed for every full bridge.

An advantage of the full bridge cascaded topologies is that a high number of voltage levels can be synthesized in the output voltage waveform with only a few dc voltage sources, but these sources need to be isolated one from another. This last condition may or not be a drawback, depending on the application where the topology is employed.

1.3.3. Neutral-point-clamped topologies

In NPC topologies, a single dc-bus is formed by the series connection of capacitors or voltage sources, which define the available voltage levels. The output of each converter leg is then connected to any of the voltage levels through a set of semiconductor devices. Each converter leg can be modeled as a single-pole *N*-throw switch (Fig. 1.12).

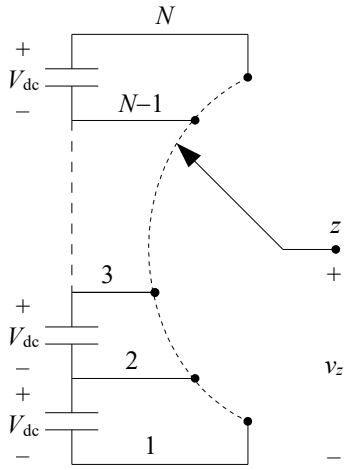


Fig. 1.12. Functional model of a dc-ac N-level NPC converter leg.

1.3.3.1. Diode-clamped topology

The diode-clamped topology is the most popular NPC topology, specially the three-level version (Fig. 1.13). It was first presented in [59] and a generalization to *N* levels was presented in [60], [61].

The diode-clamped topology has become the most used multilevel topology in industry, thanks to its implementation simplicity and its better performance, compared to other topologies. The number of switches and clamping diodes employed is $2(N-1)$ and $2(N-2)$, respectively.

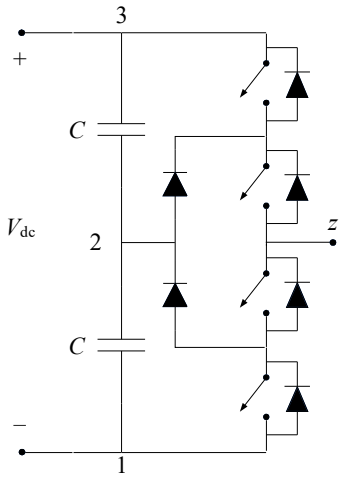


Fig. 1.13. Three-level diode-clamped converter leg.

One of the main drawbacks of this topology (and in general, of NPC topologies) is the capacitor voltage balancing [62]. To avoid device overvoltage, it is necessary to keep the voltages across the dc-link capacitors constant during the operation of the converter. Conventional modulations for line-frequency inverters do not guarantee voltage balancing over all the operating conditions and number of converter levels. Nevertheless, new modulations have been proposed to solve this problem. However, all of them are only oriented to line-frequency dc-ac conversion.

1.3.3.2. Three-level active-clamped topology

The first proposed active-clamped topology [63] (Fig. 1.14) is based on the three-level diode-clamped topology, where two switches with antiparallel diodes substitute the clamping diodes. With this modification, a better balance on loss distribution is achieved, as opposed to the classical diode-clamped topology. This allows increasing the output power rating or the switching frequency.

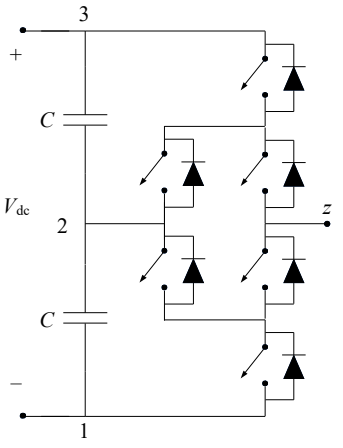


Fig. 1.14. Three-level active-clamped converter leg.

1.3.3.3. Multilevel active-clamped topology

The multilevel active-clamped (MAC) topology is an extension to any number of levels of the previous topology, derived from the generalized multilevel topology [64], where all capacitors are removed except for the ones on the dc link. The MAC topology is built upon a single cell, a half bridge composed by two switches and its anti-parallel diodes, which is replicated to form a pyramidal structure, as it can be seen in the four-level MAC (4L-MAC) converter of Fig. 1.15. It was first presented in [65], [66], and a proof of concept of a non-isolated buck-boost dc-dc converter using two legs of the MAC topology is carried out in [67]. The number of switches employed per converter leg is $N(N-1)$. To simplify, throughout the rest of the document, the three-level active-clamped topology is named as 3L-MAC.

The MAC topology operation principle aims to connect each one of the input voltage levels to the output through the maximum number of parallel paths, while at the same time, activating other non-used switches to set the blocking voltage of the remaining unused switches to $V_{dc}/(N-1)$. This leads, in one hand, to a minimization of the equivalent conduction resistance (if metal-oxide-semiconductor field-effect transistors (MOSFETs) are employed), and on the other hand, permits to build the topology around a single type of switch, which may reduce the cost of the converter. In addition, during transitions from one switching state to another, the switching losses can be distributed among the switches involved in the transition.

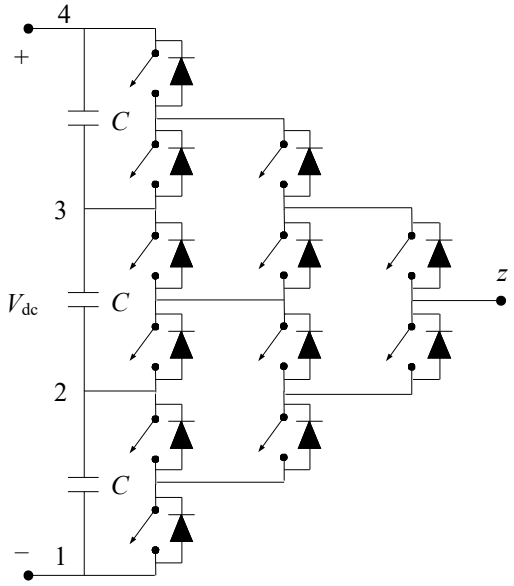


Fig. 1.15. 4L-MAC converter leg.

1.3.3.4. T-type topology

The T-type topology is a NPC topology where the connection of the inner dc-link points to the output is performed with single bidirectional switches, one for each inner dc-link point [68]–[71]. Fig. 1.16 shows a three-level T-type (3L-T-type) leg topology. The number of switches employed is $2(N-2)+2$, considering two switches per bidirectional switch.

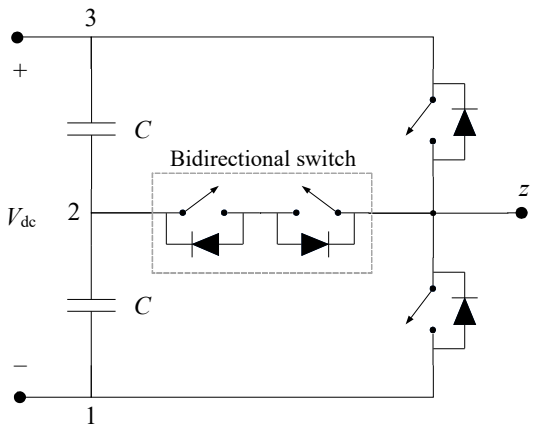


Fig. 1.16. 3L-T-type converter leg.

Unlike the diode-clamped and MAC topologies, the T-type topology switches connecting the output to the dc-link extremes have to withstand the full dc-link voltage, while the bidirectional switch have to withstand a portion of the dc-link voltage, which varies depending on its position. However, the T-type topology can generate voltage steps from non-contiguous voltage levels, e.g., it can transition directly from voltage level 1 to voltage level 3 (Fig. 1.16). This property provides added DoF to any modulation where the switching order pattern has a big influence on the converter performance.

1.4. Two-port single-stage multilevel IBDCs

The multilevel voltage-source topologies presented in Section 1.3, can offer improvements to IBDCs, compared to the performance achieved with the traditional two-level topologies. On one hand, for a given semiconductor technology, multilevel topologies allow reaching higher dc-voltage ratings (by a factor of N–1), which may allow increasing the conversion efficiency, for a given power rating, by reducing the current stress on the semiconductors and passive components. On the other hand, for a given dc-link voltage rating, they allow operating with lower-voltage-rated devices [by a factor of $1/(N-1)$] with better performance features and lower cost, reducing both switching and conduction losses, reducing the total harmonic distortion (THD) of voltage and current waveforms, and improving the converter fault-tolerance capacity. However, its disadvantages are the added

complexity of the control and modulation strategies, and the higher number of semiconductors and corresponding required gate circuits.

Few studies have been performed where the concepts of multilevel technology and IBDCs are merged.

1.4.1. Single-phase three-level DAB converter

A three-level DAB converter is presented in [72] (Fig. 1.17). It is based on HB-DAB [Fig. 1.5(b)], where the converter legs are substituted by a hybrid topology composed by a three-level diode-clamped leg (Fig. 1.13) with a flying capacitor ($C_{f,a}$, $C_{f,b}$) connected between the midpoints of the upper and lower switch pairs. Such converter is defined as a 3L-HB-DAB. Reference [72] does not explain the function of the $C_{f,a}$, $C_{f,b}$, but most probably these are used to guarantee a blocking voltage of the switches an diodes equal to half of the each-side dc link. It must be taken into account that using one three-level converter per side, only allows synthesizing three-level transformer ac voltages, just the same as with the FB-DAB [Fig. 1.5(a)]. In fact, [72] only uses two of the three available levels (no zero-voltage intervals are applied), so the converter is restricted to use the PSM. Hence, no novelty is being added, except for using a multilevel topology to reach higher dc-link voltages with a given semiconductor technology. Moreover, the capacitor-voltage-balancing issue is not discussed.

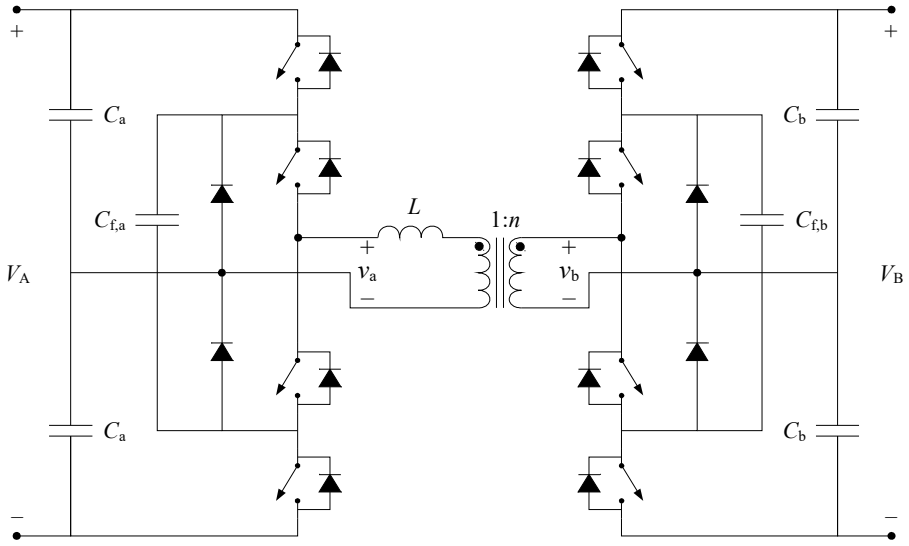


Fig. 1.17. 3L-HB-DAB converter employing 3L-NPC legs with added flying capacitors.

References [73]–[75] propose a similar DAB converter where a single 3L-NPC converter leg in half-bridge disposition is used on one side, while on the other side, a two-level full bridge is used,

hence defining a 3L-2L-HB-FB-DAB converter. For instance, [73] employs such topology to perform a benchmark of a novel variation of the TRM. On [74], an input-parallel output-series connection of four 3L-2L-HB-FB-DAB converters, is necessary to achieve up to 8 kV on the high-voltage dc link. Similarly, [75] employs the NPC topology to reduce the voltage stress of the high-voltage side switches. Moreover, the three studies do not propose any modulation that would take advantage of the three-level output voltage generated by the NPC leg (no zero-voltage sequence is generated). The capacitor-voltage-balancing issue is not discussed.

A third example of a multilevel DAB converter is presented in [76]–[78] (Fig. 1.18). In this case, two 3L-NPC legs are placed in a full-bridge disposition in order to synthesize a five-level transformer stepped voltage waveform. On the other side, a two-level full bridge is used, as in the FB-DAB [Fig. 1.5(a)], synthesizing a three-level transformer voltage waveform. Such converter is defined as a 3L-2L-FB-DAB. References [76] and [77] propose a modulation similar to the PSM, although it is not profusely studied. On the other hand, [78] characterizes the power transfer capability of the converter and its soft-switching regions, although no novel modulation is proposed. Compared to the conventional 2L-DAB, a smoother inductor current is achieved. The three-phase DAB (Fig. 1.9) attains a more sinusoidal current, while using the same number of switches, but four more windings on the transformer. No efficiency study is carried out. As in [72], [73], the capacitor-voltage-balancing issue is not discussed. Moreover, in [78] independent dc-voltage supplies are employed in the three-level side dc-link to generate the voltage levels.

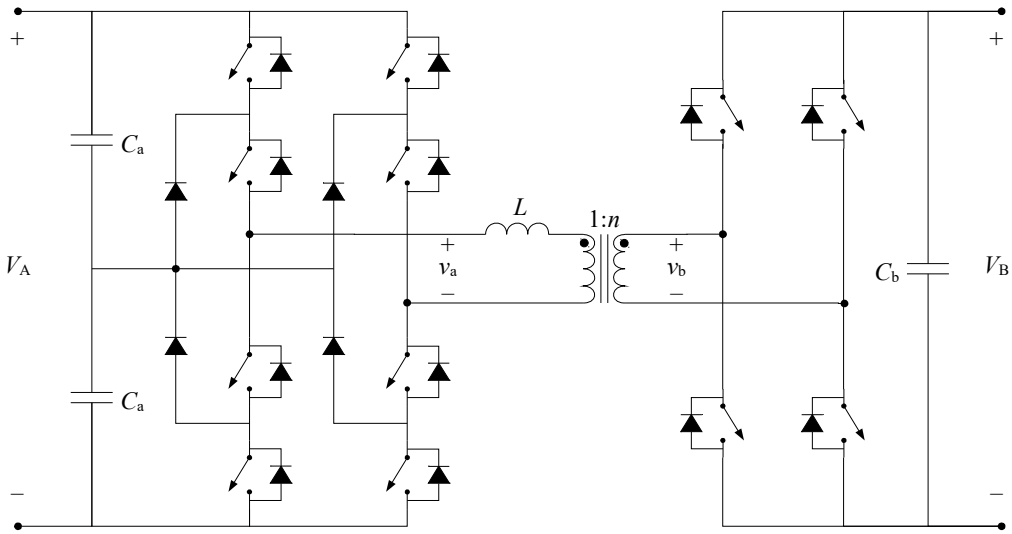


Fig. 1.18. 3L-2L-FB-DAB converter employing 3L-NPC legs.

References [79], [80] also employ Fig. 1.18 topology, in order to benchmark a 25 kW 700 V / 5 kV DAB converter working with 600 V isolated gate bipolar transistors (IGBTs) on the primary and five series connected 1.5 kV SiC junction field-effect transistors to implement each switch of the secondary side. Nevertheless, the PSM is employed (rectangular voltage waveforms are applied on each transformer side) and the capacitor voltage balancing is not discussed.

References [81]–[83] employ two 3L-T-type converter legs in a full-bridge disposition on one DAB converter side and a two-level full bridge on the other side, as shown in Fig. 1.19, again defining a 3L-2L-FB-DAB. Reference [81] proposes a modulation scheme that minimizes the transformer rms current, taking advantage of the T-type topology capability of generating transformer voltage waveforms with voltage steps transitioning directly from zero to $\pm V_A$, without the need to commutate to $\pm V_A/2$ intermediate voltage level in between. The efficiency values obtained with such modulation are compared with those obtained with an efficiency optimized FB-DAB [Fig. 1.5(a)]. The results demonstrate that the proposed 3L-2L-FB-DAB converter has better efficiency values in the high voltage regime. Nevertheless, the capacitor voltage balancing is not discussed. Reference [82] makes a similar and more comprehensive comparison of Fig. 1.5(a) and Fig. 1.19 topologies, both employing efficiency optimized modulation schemes, with Si MOSFETs and SiC MOSFETs. Such comparison shows that the conventional FB-DAB is superior in terms of efficiency, power density, and cost. Nevertheless, the higher power-density claim comes from the fact that the 3L-2L-FB-DAB requires higher dc-link capacitances to mitigate the capacitor voltage unbalance. By employing a modulation that offers the possibility to control the capacitor voltages, such issue could be overcome. On the other hand, the higher cost claim is derived from the need of a higher number of gate drivers. Still, the cost of such gate drivers could be greatly reduced if integrated gate-drive power supplies were employed [84].

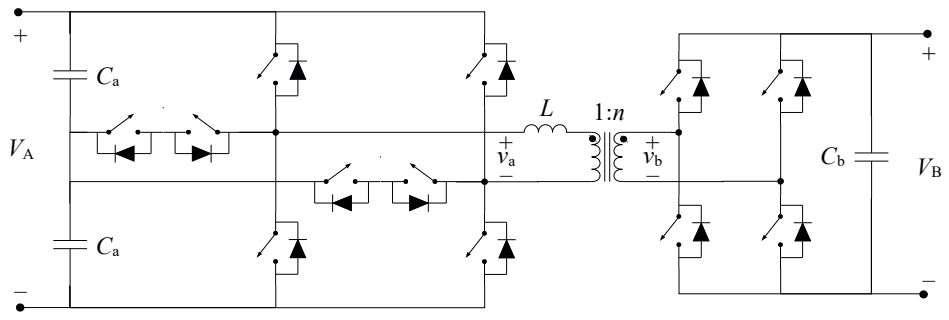


Fig. 1.19. 3L-2L-FB-DAB converter built upon 3L-T-type legs.

1.4.2. Three-phase three-level DAB converter

A three-level three-phase DAB is presented in [85], built-upon a generic single-pole triple-throw switch per phase, as seen in Fig. 1.20. A modulation is defined with three DoF, two duty cycles defining the phase voltages on each side plus the phase shift between each side phase voltages. With the defined modulation, the region of feasible ZVS is greatly expanded in comparison with the conventional (two-level) three-phase DAB. A numerical optimization of the transformer rms current, helps finding favorable patterns in the modulation parameters, with the result of a simplified modulation strategy (it employs only two DoF), while still achieving close-to-minimum transformer rms currents and soft-switching transitions. The capacitor-voltage-balancing issue is not discussed. Two independent voltage sourced power supplies are employed per side to generate the three voltage levels on each side.

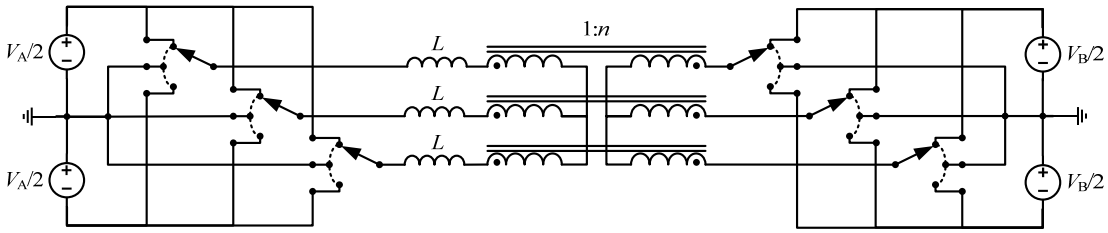


Fig. 1.20. Three-phase 3L-DAB converter with Y-Y transformer connections.

1.5. Thesis objective

The exposed state of the art reveals that the most promising IBDC in terms of performance, flexibility, and power density is the DAB converter. An extensive and heterogeneous number of studies in the literature are dedicated to the conventional two-level single-phase DAB converter, exploring several topology variants and multiple modulation schemes with heterogeneous strategies, with the principal objective of increasing the converter efficiency over a wide dc-voltage gain range. A natural step to further improve the converter performance is the inclusion of multilevel topologies on the DAB converter. Few studies have explored such venture, but the NPC topologies are promising, due to its high power density, better performance, and high reliability, while extending the available DoF and widening the DAB application profile to higher-voltages.

A first objective of the proposed thesis is to study the viability of multilevel DAB converters employing NPC topologies (ML-DAB converters). An important issue to determine the viability is the dc-link capacitor voltage balancing.

A second objective is to design suitable modulation strategies and closed-loop controls to maximize the performance features of ML-DAB converters (efficiency, power density, etc), and compare their performance to the conventional 2L-DAB converter performance.

1.6. Thesis outline

The thesis is organized as follows.

Chapter 2, Chapter 3, and Chapter 4 comprise the study of a three-level, four-level, and five-level (5L) NPC DAB converter, respectively. Such studies present the definition of novel modulation schemes, suitable capacitor-voltage-balancing closed-loop control strategies, and closed-form solutions for the modulation parameters based on the converter-losses optimization results. Its feasibility and performance are verified through simulations and experimental tests.

Chapter 5 presents an extension to N levels of the previously studied ML-DAB converters. A generalization of the modulation, capacitor-voltage-balancing control schemes, and closed-form modulation-parameter definitions are presented.

Chapter 6 studies the feasibility of ML-DAB converters with an asymmetric number of levels. Three different configurations (3L-2L, 4L-2L, and 4L-3L) are characterized and its feasibility and performance are verified through simulations and experimental tests.

Finally, Chapter 7 outlines the conclusions and proposes potential future research lines.

Appendix A presents the experimental equipment and converters used to perform the experimental tests.

Appendix B outlines the proposed algorithm to limit the modulation switching angles to its physical limits.

CHAPTER 2.

STUDY OF A THREE-LEVEL NEUTRAL-POINT-CLAMPED DUAL-ACTIVE-BRIDGE DC-DC CONVERTER

Abstract — This chapter presents the study of a three-level neutral-point-clamped (NPC) dual-active-bridge (DAB) dc-dc converter. A general modulation pattern is initially defined, the dc-link capacitor voltage balancing is analyzed in detail, and a proper balancing control is designed. Then, a set of decoupled optimization problems are formulated as a function of the available modulation degrees of freedom to minimize the predominant converter losses. Finally, a simple and practical specific modulation strategy is provided resembling the optimum solutions. The good performance of the proposed three-level NPC DAB converter operated with the proposed modulation strategy and capacitor-voltage-balancing control is verified through simulation and experiments. In addition, it is concluded that the multilevel topology provides benefits compared with the conventional (two-level) full-bridge DAB converter.

2.1. Introduction

This chapter introduces a DAB dc-dc converter built upon four 3L-NPC legs. A proper modulation strategy is proposed and characterized. The dc-link capacitor voltage balancing is analyzed, including the effect of the transformer current harmonics, and a closed-loop voltage-balancing control is proposed. By performing an optimization of the modulation strategy parameters values and studying the results, a set of simple and practical equations is proposed that minimizes the converter losses. Finally, simulation and experimental tests are done to verify the proposed capacitor-voltage-balancing control and the optimized modulation strategy.

This chapter is organized as follows. Section 2.2 presents the converter topology. Section 2.3 presents the fundamentals of the modulation strategy. Section 2.4 presents the study of the capacitor voltage balancing and defines a proper control scheme. Section 2.5 presents the performance optimization study and proposes a practical solution for the modulation strategy based on the results. Section 2.6 presents the simulation and experimental results to verify the modulation and control performance. Finally, Section 2.7 outlines the conclusions.

2.2. Topology

Fig. 2.1 presents the proposed 3L NPC DAB dc-dc (3L-DAB) converter topology. This converter, with a structure similar to the (two-level) FB-DAB, has two sides; i.e., a-side and b-side, delimited by a transformer with a turns ratio of 1/n. Each side has a voltage-sourced dc link, with a voltage of V_Z (where $Z \in \{\text{A, B}\}$). Three voltage levels, with connection points 1_z, 2_z, and 3_z (where

$z \in \{a, b\}$), are obtained from each dc-link by a capacitor voltage divider. Each side has two 3L-NPC legs (named as its output nodes z_1 and z_2) which synthesize v_{z1} and v_{z2} medium-to-high-frequency ac voltages, by connecting the output nodes to the available dc-link connection points. The full-bridge disposition of the NPC legs in each side of the converter, allows generating transformer voltages v_a and v_b. Power is transferred between both dc links by phase shifting voltages v_a and v_b, which induces an ac current (i_a) in inductance L. This inductance can be attained with an external inductor or with the transformer stray inductance.

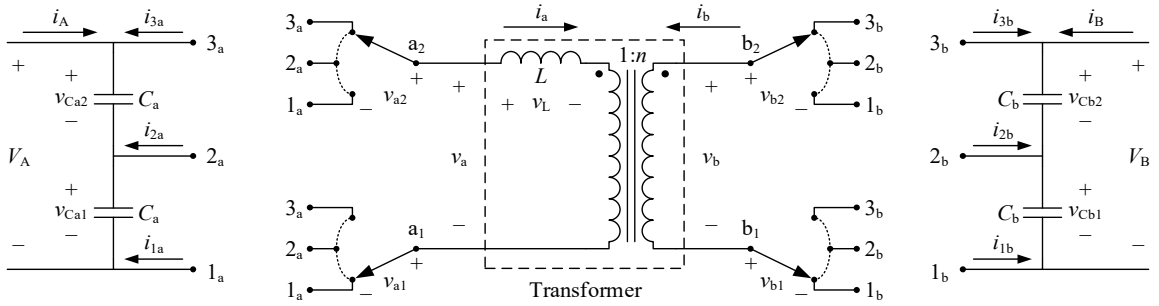


Fig. 2.1. Topology of the proposed 3L-DAB dc-dc converter with phase legs a_1, a_2, b_1, and b_2 depicted as single-pole triple-throw switches.

2.3. Modulation

Fig. 2.2 represents the two z-side leg voltages v_{z1} and v_{z2} in the most general case, assuming a staircase waveform with a single connection to the top and bottom voltage levels per switching cycle. In each converter full bridge 7 DoF, or independent variables, are available, which accounts to a total of 15 DoF if the phase shift between v_a and v_b is considered.

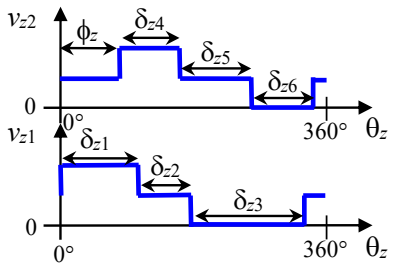


Fig. 2.2. Analysis of maximum DoF available in a 3L-DAB.

To reduce the risk of transformer-core saturation and prevent the rise of a steady-state dc component in i_a (increasing the converter conduction and switching losses), it is necessary to guarantee $\overline{v}_z = 0 \ \forall z$, or in other words, $\overline{v}_{z1} = \overline{v}_{z2} \ \forall z$. Hence, looking at Fig. 2.2, we can derive that

$$v_{Cz2} \cdot \delta_{z1} - v_{Cz1} \cdot \delta_{z3} = v_{Cz2} \cdot \delta_{z4} - v_{Cz1} \cdot \delta_{z6} \,. \tag{2.1}$$

This leaves us with 6 DoF in each converter full bridge (e.g., δ_{z1}, δ_{z2}, δ_{z3}, δ_{z4}, δ_{z5}, ϕ_z) leading to a total of 13 DoF in the full converter when considering the phase-shift between v_a and v_b.

Moreover, to impose odd symmetry on v_z, necessary for the capacitor voltage balancing (see Section 2.4.1) and force a symmetrical operation of both full-bridge legs, it is set (as shown in Fig. 2.3)

$$\begin{cases} \delta_{z4} = \delta_{z1} \\ \delta_{z5} = 360° - \left(\delta_{z1} + \delta_{z2} + \delta_{z3}\right) \\ \delta_{z6} = \delta_{z3}. \end{cases} \tag{2.2}$$

With this condition, 4 DoF remain in each converter full bridge (δ_{z1}, δ_{z2}, δ_{z3}, ϕ_z) leading to a total of 9 DoF in the full converter when considering the phase-shift between v_a and v_b. Additionally, (2.1) is always verified, which avoids a transformer current dc component.

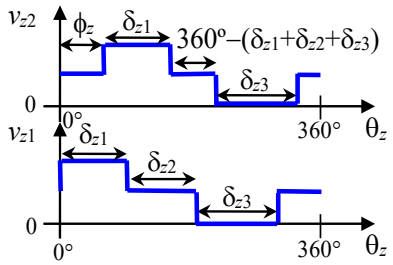


Fig. 2.3. Analysis of the available DoF when legs z_1 and z_2 operate symmetrically.

For convenience, the 9 DoF are represented by a new set of independent variables; i.e., eight switching angles (α_{ao1}, α_{ao2}, α_{ai1}, α_{ai2}, α_{bo1}, α_{bo2}, α_{bi1}, α_{bi2}) plus the phase shift (φ) between v_a and v_b, all depicted in Fig. 2.4. The relationship between the new set and Fig. 2.3 independent variables is

$$\begin{cases} \delta_{z1} = 180° + \alpha_{zi1} - \alpha_{zo2} \\ \delta_{z2} = \alpha_{zo2} - \alpha_{zo1} \\ \delta_{z3} = 180° + \alpha_{zo1} - \alpha_{zi2} \\ \phi_z = \alpha_{zi1} + \alpha_{zo2}. \end{cases} \tag{2.3}$$

The switching angles boundary values are

$$\begin{aligned} -90° \le \alpha_{zi1} \le \alpha_{zi2} \le 90° \\ -90° \le \alpha_{zo1} \le \alpha_{zo2} \le 90°. \end{aligned} \tag{2.4}$$

In Fig. 2.4, it is shown that with the proposed modulation scheme, v_z voltage waveform presents five voltage levels if capacitor voltages are balanced. Additionally, v_z has a fixed switching-state sequence (v_a switching-state sequence can be seen on top of Fig. 2.4). The switching states are represented as $(xy)_z$, where $x, y \in \{1,2,3\}$ indicate the z-side dc-link point to which nodes z_2 and z_1 are connected, respectively.

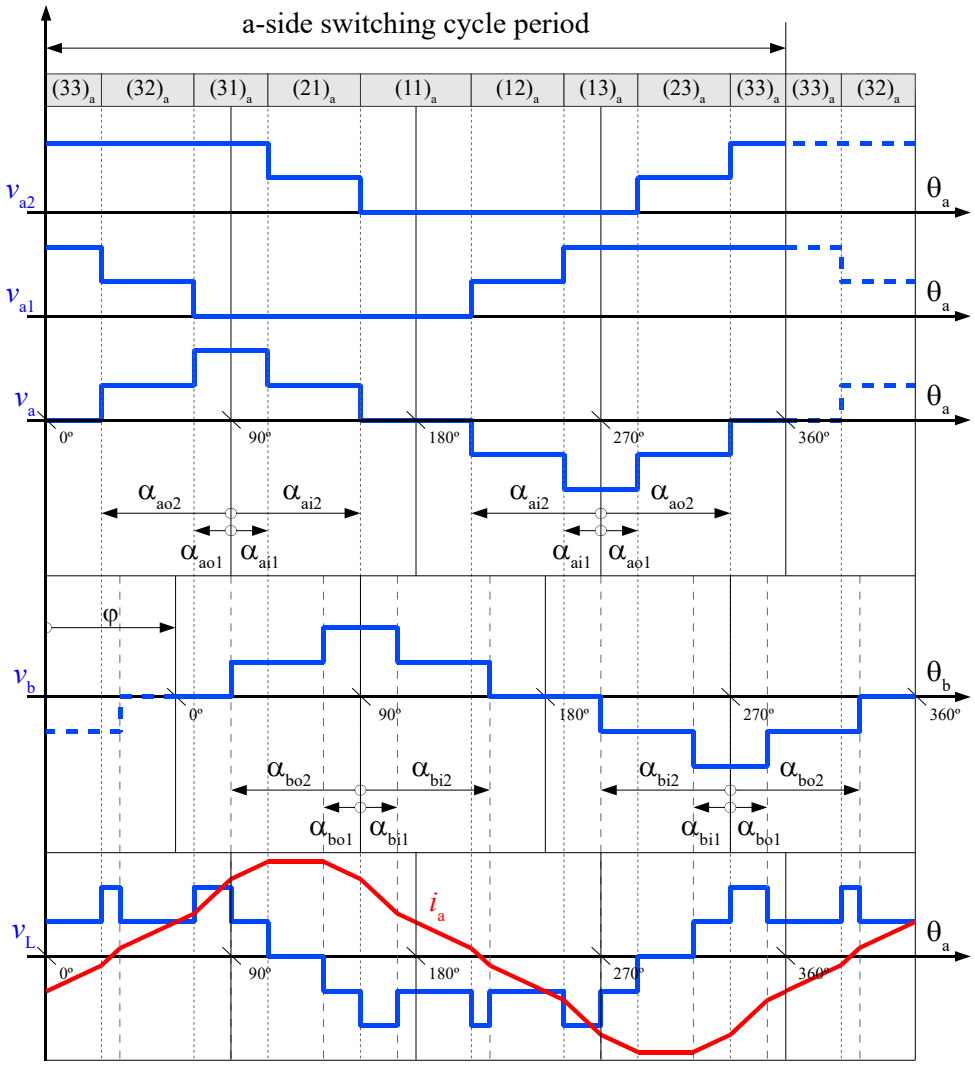


Fig. 2.4. Voltage waveforms v_{a1}, v_{a2}, v_b, and v_L, and current waveform i_a for the proposed three-level modulation. Switching states are shown on top of the figure. All waveforms are plotted assuming $V_A = V_B/n$ and $v_{C1} = v_{C2}$ $\forall z$.

Two out of the four DoF in each converter full bridge affect the capacitor voltage balancing and therefore have to be reserved for the capacitor-voltage-balancing control. They can be identified in terms of independent variables α_{zo1}, α_{zo2}, α_{zi1}, α_{zi2}, as

$$\begin{aligned}\psi_{z1} &= \alpha_{zi1} - \alpha_{zo1} \\ \psi_{z2} &= \alpha_{zi2} - \alpha_{zo2}.\end{aligned} \tag{2.5}$$

The remaining two DoF in each converter full bridge can be used to optimize the converter performance. They can be identified in terms of the four independent variables α_{zo1}, α_{zo2}, α_{zi1}, α_{zi2}, as

$$\begin{aligned}\psi_{z3} &= \frac{\alpha_{zi1} + \alpha_{zo1}}{2} = \alpha_{z1} \\ \psi_{z4} &= \frac{\alpha_{zi2} + \alpha_{zo2}}{2} = \alpha_{z2}.\end{aligned} \tag{2.6}$$

It should be noted the convenience of working with variables α_{zo1}, α_{zo2}, α_{zi1}, α_{zi2}: The DoF to achieve capacitor voltage balancing can be identified as their differential value and the remaining DoF, employed to optimize the converter performance, as their average value.

As in the 2L-DAB, the fundamental components of voltages v_a and v_b are phase shifted φ degrees, hence building current i_a in the leakage inductance L of the transformer. The magnitude of φ determines the amount of power being transferred, and the sign of φ determines the direction; i.e., for $\varphi > 0$, power flows from a-side to b-side, and for $\varphi < 0$, the power flows in the opposite direction.

It should be noted that, in any case, v_z voltage waveform has odd symmetry [$v_z(\theta_z) = -v_z(-\theta_z)$]. Assuming

$$\begin{aligned}\alpha_{zo1} &= \alpha_{zi1} = \alpha_{z1} \\ \alpha_{zo2} &= \alpha_{zi2} = \alpha_{z2}\end{aligned} \tag{2.7}$$

and that the capacitor voltages are balanced, v_z also presents half-wave symmetry, and even-order harmonics are eliminated in v_a, v_b, v_L, and i_a waveforms. Then, the transformer voltages and currents can be defined in terms of their different harmonics as

$$\begin{aligned}v_z &= \sum_{h\ \text{odd}} \left[\left\| \mathbf{V}_{z,h} \right\| \cdot \sin\left(h \cdot \theta_a + \arg\left(\mathbf{V}_{z,h} \right) \right) \right] \\ i_a &= -n \cdot i_b = \sum_{h\ \text{odd}} \left[\left\| \mathbf{I}_{a,h} \right\| \cdot \sin\left(h \cdot \theta_a + \arg\left(\mathbf{I}_{a,h} \right) \right) \right],\end{aligned} \tag{2.8}$$

where h is the harmonic number, $\mathbf{V}_{z,h}$ and $\mathbf{I}_{a,h}$ are the voltage and current harmonic h phasors,

$$\begin{aligned}
&\mathbf{V}_{\mathrm{a},h} = V_{\mathrm{a},h} \cdot \left(\cos\left(h \cdot \varphi/2\right) + j \cdot \sin\left(h \cdot \varphi/2\right)\right) \\
&\mathbf{V}_{\mathrm{b},h} = V_{\mathrm{b},h} \cdot \left(\cos\left(h \cdot \varphi/2\right) - j \cdot \sin\left(h \cdot \varphi/2\right)\right) \\
&V_{z,h} = \frac{2V_Z}{\pi h} \cdot \left[\cos\left(h \cdot \left(90° - \alpha_{z1}\right)\right) + \cos\left(h \cdot \left(90° - \alpha_{z2}\right)\right)\right] \\
&\mathbf{I}_{\mathrm{a},h} = -\mathbf{I}_{\mathrm{b},h} = \frac{\mathbf{V}_{\mathrm{a},h} - \mathbf{V}_{\mathrm{b},h}/n}{\mathbf{X}_{\mathrm{L},h}} \\
&\mathbf{X}_{\mathrm{L},h} = j \cdot \left(2\pi \cdot h \cdot f_{\mathrm{s}} \cdot L\right),
\end{aligned} \tag{2.9}$$

$|V_{z,h}|$ is the peak value of the amplitude of harmonic $v_{z,h}$, and f_s is the switching frequency of the converter.

The transferred power considering a lossless system is

$$P = \frac{1}{2} \cdot \sum_{h\ \mathrm{odd}} \left[\left\|\mathbf{V}_{\mathrm{a},h}\right\| \cdot \left\|\mathbf{I}_{\mathrm{a},h}\right\| \cdot \cos\left(\arg\left(\mathbf{V}_{\mathrm{a},h}\right) - \arg\left(\mathbf{I}_{\mathrm{a},h}\right)\right)\right]. \tag{2.10}$$

If $P > 0$, then power is transferred from a-side to b-side and vice versa if $P < 0$.

The maximum power that can be transferred for a given V_A and V_B/n is defined by (2.10) when $\alpha_{z1} = \alpha_{z2} = 90^\circ\ \forall z$, and $\varphi = 90^\circ$. Setting $\alpha_{z1} = \alpha_{z2} = 90^\circ\ \forall z$ is equivalent to employing the PSM, hence, according to (1.1), the maximum transferred power is

$$P_{\max} = \frac{V_{\mathrm{A}}^2 d}{8 f_{\mathrm{s}} L}. \tag{2.11}$$

Equations (2.8)−(2.10) are used in Section 2.5, considering all harmonics up to order $h = 63$.

2.4. Capacitor voltage balancing

Fig. 2.5 shows an example of the capacitor voltage behavior under the absence of a closed-loop control. In this example, a small perturbation on both sides switching angles is introduced to account for switch and gate driver non-idealities (parameter dispersion, etc.). Such perturbation leads to unacceptable capacitor voltage oscillations over long periods of time and a permanent voltage unbalance that could destroy the devices due to an excessive blocking voltage, besides leading to nonoptimal operating conditions. Therefore, a closed-loop capacitor-voltage-balancing control is required.

Capacitor voltage unbalance in voltage-source multilevel converters is an important issue [53], and many solutions have been proposed for modulations with high switching-to-fundamental

frequency ratios. However, the proposed modulation does not fall into this category. Therefore, in this section, an analysis of the capacitor voltage balancing with the proposed modulation scheme is carried out, and a suitable control scheme to compensate any voltage unbalance is proposed.

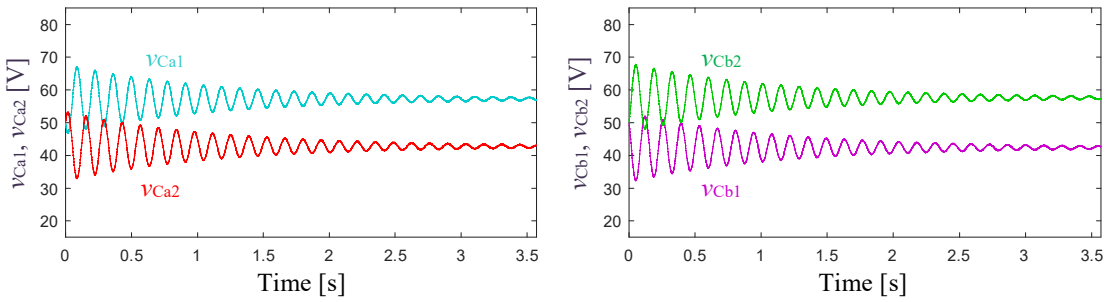


Fig. 2.5. Simulation results showing the transient response of v_{Ca1}, v_{Ca2}, v_{Cb1}, and v_{Cb2} voltages, from an initial balanced state, when a small perturbation in both sides switching angles ($\{\alpha_{ai1},\alpha_{ao1},\alpha_{ai2},\alpha_{ao2}\}$ = {22.5°,25°,67.5°,65°} and $\{\alpha_{bi1},\alpha_{bo1},\alpha_{bi2},\alpha_{bo2}\}$ = {22.5°,20°,67.5°,70°}) is introduced. Conditions: V_A = 100 V, V_B = 100 V, C_z = 100 μF, and φ = 60°. Transient response.

2.4.1. Control operating principle and control scheme

The current injected into or drawn from the neutral point of the dc-link alters the ratio between the two dc-link capacitor voltages. This current is

$$i_{2z} = S_{z12} \cdot i_z - S_{z22} \cdot i_z , \tag{2.12}$$

where S_{zj2} is equal to 1 when leg z_j is connected to dc-link point 2_z and 0 otherwise.

To preserve the capacitor balance, the total charge injected into the neutral point within a switching cycle has to be equal to zero.

Let us first consider the effect of the fundamental component of i_z ($i_{z,1}$), as its amplitude is greater than each of the harmonic amplitudes. Current $i_{z,1}$ can be decoupled into a $i^{p}_{z,1}$ component, in phase with $v_{z,1}$ (the fundamental component of v_z), and into $i^{q}_{z,1}$ component, in quadrature with $v_{z,1}$. This can be mathematically expressed as

$$\begin{aligned} v_{z,1} &= V_{z,1} \cdot \sin(\theta_z) \\ i_{z,1} &= i^{p}_{z,1} + i^{q}_{z,1} = I^{p}_{z,1} \cdot \sin(\theta_z) + I^{q}_{z,1} \cdot \cos(\theta_z). \end{aligned} \tag{2.13}$$

Currents $i^{p}_{z,1}$ and $i^{q}_{z,1}$ are depicted in Fig. 2.6, together with v_z. The shaded areas in Fig. 2.6 represent the electrical charge injected into (positive sign) or drawn from (negative sign) the z-side dc-link neutral point by these currents. If (2.7) is verified (there is quarter-wave symmetry), the total

charge injected into the neutral point by both currents is zero for a whole switching cycle. However, if a voltage unbalance needs to be corrected, the inner (α_{zi1}, α_{zi2}) and outer angles (α_{zo1}, α_{zo2}) can be modified in order to inject or draw a nonzero charge during a switching cycle. This charge will only be provided by $i^{p}_{z,1}$ since the total charge injected by $i^{q}_{z,1}$ is zero owing to the odd symmetry of v_z.

Employing the in-phase component of $i_{z,1}$ is advantageous since the in-quadrature component contributes to the reactive power of the converter, which ideally should be minimized to reduce the conduction losses.

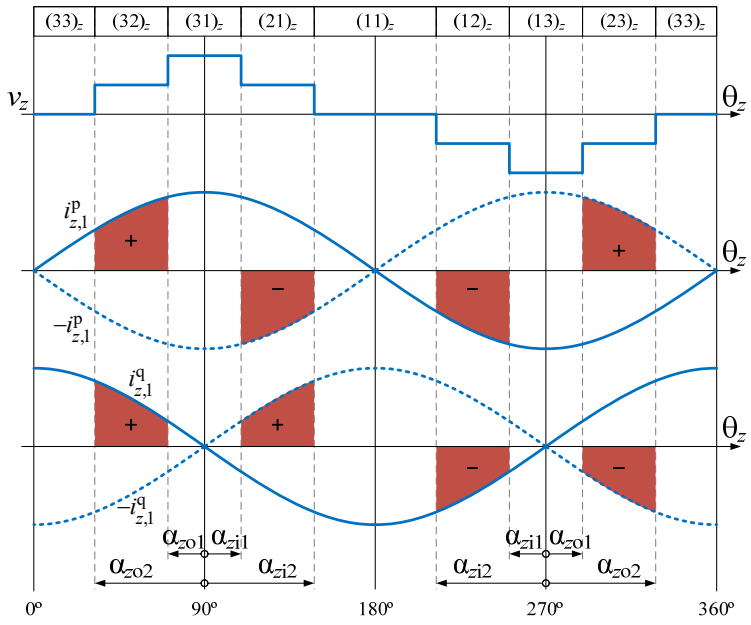


Fig. 2.6. Voltage v_z and the in-phase and in-quadrature components of i_z fundamental component ($i^{p}_{z,1}$ and $i^{q}_{z,1}$). The red areas depict the injected (+) or drawn (−) charge from the z-side dc-link neutral point by $i^{p}_{z,1}$ and $i^{q}_{z,1}$.

2.4.1.1. Full control scheme

Fig. 2.7 shows the proposed control scheme for the capacitor voltage balancing. This control scheme takes advantage of all the available switching angles shown in Fig. 2.4 to regulate any voltage unbalance, hence it is denominated as full control scheme. Variable y_{z2} captures the unbalance between both dc-link capacitor voltages, which are previously filtered through transfer functions matrix $\mathbf{H}_{filt}(s) = \text{diag}(H_{filt}(s), H_{filt}(s))$. Variable y^{*}_{z2} indicates the desired capacitor voltage unbalance, which is equal to zero when $v_{Cz1} = v_{Cz2}$ is required. The difference between y^{*}_{z2} and y_{z2} defines error variable e_{z2}. A value $e_{z2} > 0$ means that v_{Cz1} is below its desired value and v_{Cz2} is above its desired value. Therefore, a control action is needed that injects charge into 2_z in order to increase v_{Cz1} and decrease v_{Cz2}; i.e., increase y_{z2}.

Without loss of generality, let us assume that power is transferred from side a to side b. Then, the waveforms defined in Fig. 2.6 correspond to side a, while the waveforms of side b are the same except for the current, which has opposite sign ($i_b = -i_a$). In this case, any $e_{zm} \neq 0$ can be corrected by modifying switching angles α_{zo1}, α_{zo2}, α_{zi1}, and α_{zi2} according to Table 2.1. Obviously, if power is transferred from side b to side a, the required switching-angle-change directions shown in Table 2.1 are reversed. Control variable u_{z2}, generated by processing e_{z2} variable with compensator $G_{z2}(s)$, is responsible of performing the required control action. Variable u_{z2} modifies switching angles α_{zo1}, α_{zo2}, α_{zi1}, and α_{zi2} in a per-unit basis from the value of the initial switching angles α_{z1} and α_{z2}.

z	e_{z2}	**Charge sign to provide**	**{α_{zo1}, α_{zi2}}**	**{α_{zo2}, α_{zi1}}**
a	+ / –	+ / –	↓ / ↑	↑ / ↓
b	+ / –	+ / –	↑ / ↓	↓ / ↑

Table 2.1. Sign of the charge to be provided and switching angles change needed to correct a voltage unbalance at neutral point 2z, depending on the sign of e_{z2}, and according to Fig. 2.6.

Let us consider that $G_{z2}(s)$ compensator transfer function is a proportional-integral (PI) controller, defined in its standard form as

$$G_{zm}(s) = k_{P,zm} \cdot \left(1 + \frac{1}{T_{I,zm} \cdot s}\right) = k_{zm} \cdot \frac{T_{I,zm} \cdot s + 1}{s}, \tag{2.14}$$

where $m = 2$ for the present converter, $k_{P,zm}$ is the general gain of the controller, $T_{I,zm}$ is the integrator reset time, and $k_{zm} = k_{P,zm}/T_{I,zm}$.

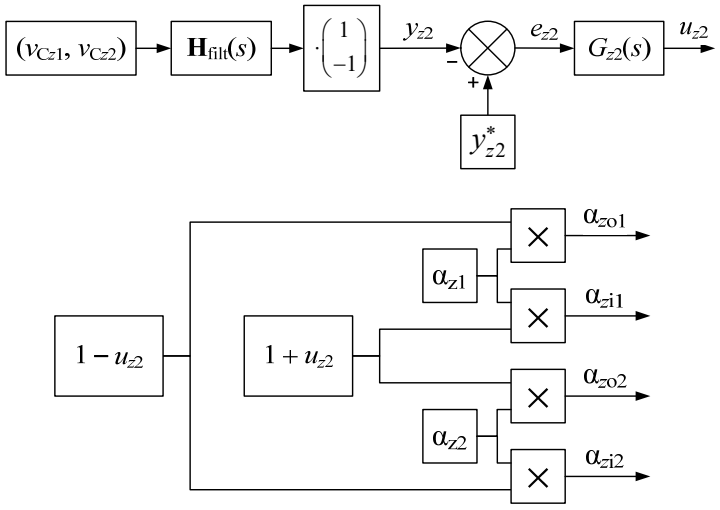


Fig. 2.7. Full control scheme for the z-side capacitor voltage balancing.

When power is transferred from side a to side b $k_{P,a2} > 0$. Regarding b-side, since $i_b = -i_a$, $k_{P,b2} < 0$. When power is transferred from side b to side a, the sign of $k_{P,z2}$ changes.

2.4.2. Influence of the transformer current harmonics and dc component on the capacitor voltage balancing

Current i_z will typically contain non-negligible harmonics and may contain a non-desired dc component. Their effect on the capacitor voltage balancing needs to be assessed.

As an example, Fig. 2.8 depicts the charge injected into or drawn from the neutral point by the in-phase and in-quadrature components of i_z third harmonic ($i^p_{z,3}$ and $i^q_{z,3}$, respectively), when v_z has quarter-wave symmetry.

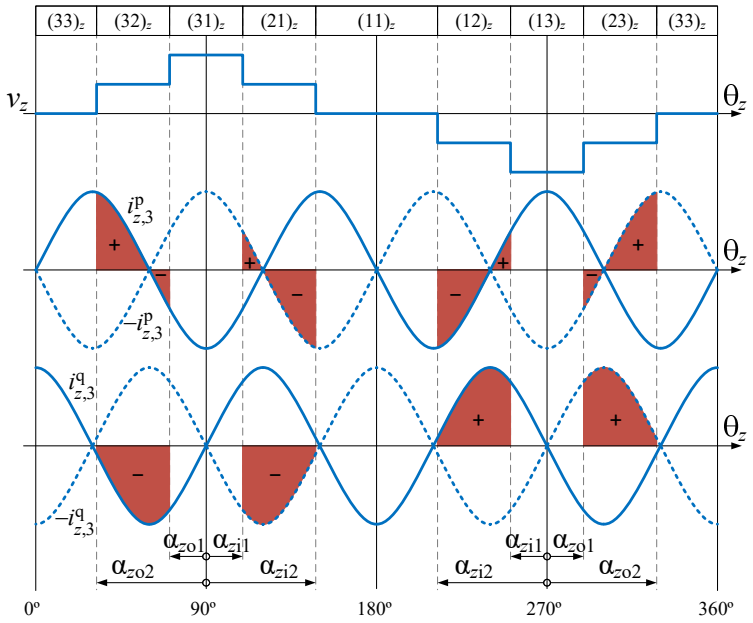


Fig. 2.8. Voltage v_z and the in-phase and in-quadrature components of i_z third harmonic ($i^p_{z,3}$ and $i^q_{z,3}$). The red areas depict the injected (+) or drawn (−) charge from the z-side dc-link neutral point by $i^p_{z,3}$ and $i^q_{z,3}$.

The odd symmetry of v_z guarantees that, for all harmonics, the in-quadrature component of the current ($i^q_{z,h}$), as well as any potential dc component present on i_z, do not affect the capacitor voltage balancing. On the other hand, the half-wave symmetry of v_z guarantees that, for all harmonics (in this case, only odd harmonics are present), the in-phase component of the current ($i^p_{z,h}$) does not affect the capacitor voltage balancing.

According to the modulation pattern presented in Fig. 2.4, voltage v_z will always present odd symmetry, even when the capacitor voltages are unbalanced. Therefore, $i^q_{z,h}$ will never affect the capacitor voltage balancing. If in addition to odd symmetry, voltage v_z presents half-wave symmetry (v_z presents quarter-wave symmetry), then neither the i_z fundamental component nor any harmonic

will affect the capacitor voltage balancing. This can be verified in the case of the third harmonic presented in Fig. 2.8. When the capacitor voltage balance is lost, the control action will force that v_z losses its half-wave symmetry, preserving only odd-symmetry. In this case, the in-phase fundamental component of i_z and the in-phase component of all i_z harmonics will introduce a non-zero charge into the neutral point, affecting the capacitor voltage balancing. However, since the fundamental component amplitude is typically much larger than the harmonic amplitudes, it can be reasonably assumed that the fundamental component effect will be larger than the joint effect of all other harmonic currents. The presented control is based on this assumption. As an example, Fig. 2.9 presents the amplitude of the first harmonics of i_a during a capacitor voltage balance recovery transient. All harmonic amplitudes always remain much lower than the fundamental component amplitude, and the proposed capacitor-voltage-balancing control operates well and is able to quickly recover the balance of a-side capacitor voltages without perturbing the balance of b-side capacitor voltages.

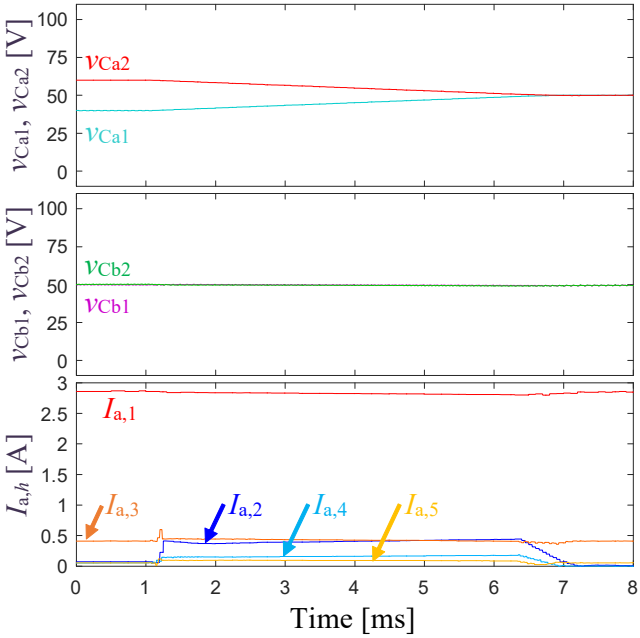


Fig. 2.9. Simulation results for v_{Ca1}, v_{Ca2}, v_{Cb1}, and v_{Cb2} and the amplitude of the first five harmonics of i_a during a capacitor-voltage-balance recovery transient starting at t = 1 ms. Conditions: α_{z1} = 60° and α_{z2} = 80° ∀z, V_A = 100 V, V_B = 100 V, R_B = 60 Ω, and steady-state φ= 26.4°.

2.5. Performance optimization

Five DoF are available to force the desired power transfer and optimize the converter performance: α_{a1}, α_{a2}, α_{b1}, α_{b2}, and φ. Variable φ is typically determined by the output voltage closed-loop control since it controls the power transfer. Therefore, simple closed-form expressions of α_{a1}, α_{a2}, α_{b1}, and α_{b2} as a function of φ that provided good performance in most cases would be highly desirable to define a general-purpose practical modulation strategy that takes advantage of the available DoF. The final goal of this section is to propose such modulation strategy.

The main performance figure of the DAB converter is the efficiency. As shown in [86], [87], transformer copper losses and switch conduction and switching losses on the 2L-DAB, represent an 80-90 % of the total losses. It seems reasonable to assume that these losses are also predominant on the presented 3L-DAB. Ideally, one would like to find out the values of the modulation parameters (α_{a1}, α_{a2}, α_{b1}, α_{b2}, and φ) that minimize the addition of all these losses on every converter working point, defined by $\{V_A^*, V_B^*, P^*\}$. However, this global optimum is strongly dependent on the constructive and operating parameters of the converter, which define different relative weights on the loss components.

In order to gain insight into the global optimization problem from a general perspective, let us decouple the global optimization problem into three simpler optimization problems. Three different objective functions are defined, which only depend on the transformer current. One objective function is associated to conduction losses, while the remaining two are associated to switching losses. Each of the three optimization problems leads to a different optimal solution. However, the analysis of their common features helps obtaining a set of practical closed-form expressions defining the modulation parameters for every operating point, with an overall good converter performance.

The proposed modulation and capacitor-voltage-balancing control can be applied with any NPC leg topology (Section 1.3.3) built upon any suitable set of semiconductor devices, operated at any voltage and current levels, and any switching frequency. However, for the sake of model simplicity and convenience in the experimental implementation, it will be assumed that legs a_1, a_2, b_1, and b_2 are implemented using 3L-MAC legs built upon MOSFETs (Fig. 2.10). The legs are operated according to [66], which guarantees a blocking voltage of $V_Z/2$ on each switch if capacitor voltages are balanced.

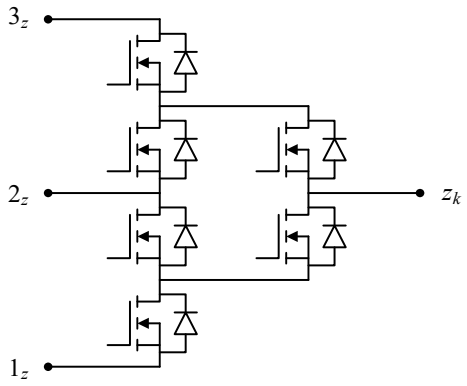


Fig. 2.10. MOSFET-based 3L-MAC leg used to implement legs a_1, a_2, b_1, and b_2.

2.5.1. Objective function associated to conduction losses

The conduction losses in the transformer windings and MOSFETs (mainly conducting through the MOSFET channel) are essentially proportional to the square of the transformer rms current ($I^2_{\mathrm{a,rms}}$). Hence, in order to minimize these losses, objective function

$$F_1 = I_{\mathrm{a,rms}} = \sqrt{\frac{1}{2} \cdot \sum_{h\ \mathrm{odd}} \left\| \mathbf{I}_{\mathrm{a},h} \right\|^2} \tag{2.15}$$

is defined.

2.5.2. Objective functions associated to switching losses

In the topology of Fig. 2.10, the leg output terminal is connected to one of the three dc-link terminals or levels. In the transition between adjacent levels, some switches turn off and some others turn on. The switching losses will be concentrated on the first switch turning on or the last switch turning off, depending on the leg output-current. Let us designate two types of transitions:

- Type I: Transitions where the losses are concentrated on a switch turning on (and on the associated turning-off diode), hence realizing a hard-switching transition.
- Type II: Transitions where the losses are concentrated on a switch turning off, hence realizing a soft-switching transition.

In a first approximation, let us consider the lossy switching transition waveforms shown in Fig. 2.11, where ideal (lossless) diodes and small parasitic drain-to-source capacitances are assumed. The energy lost in a transition between adjacent levels can be modelled as

$$E_{sw} = \frac{V_Z/(N-1)\cdot I_{sw}^2}{2\cdot s_i} + \frac{\left(V_Z/(N-1)\right)^2\cdot |I_{sw}|}{2\cdot s_v}, \tag{2.16}$$

where I_{sw} is the current being switched, N is the converter number of levels ($N = 3$ in the present chapter), and s_v and s_i are the voltage and current transition slopes, respectively, which are assumed to be constant during a transition and independent of I_{sw} and V_Z.

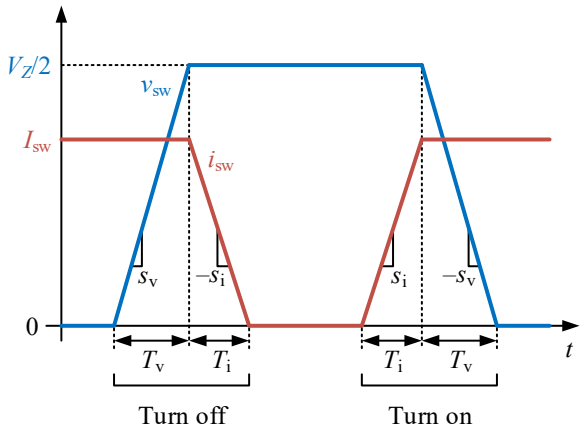


Fig. 2.11. MOSFET switch voltage and current simplified waveforms, for lossy turn-on and turn-off switching transitions on a 3L-MAC leg (Fig. 2.10). Variables $v_{sw}(t)$ and $i_{sw}(t)$ are the voltage across the switch and current through the switch.

With the previous assumptions, E_{sw} is obtained as the addition of $|I_{sw}|$ and I^2_{sw} with different weighting factors. These weighting factors are unknown because they depend on the specific device selection and other converter implementation details. Therefore, following the optimization problem decoupling approach explained previously, two different switching-loss-related objective functions can be proposed: one involving the addition of $|I_{sw}|$ for all leg level transitions within a switching cycle and another one involving the addition of I^2_{sw} for all leg level transitions within a switching cycle.

However, if real diodes are considered, the losses in Type I transitions increase due to diode reverse recovery. In addition, the losses in Type II transitions can be very small for small currents. Thus, this implies a higher penalty for Type I transitions compared to Type II. This is reflected in the final proposed objective functions associated to switching losses

$$F_2 = \sum_{T_s} \left| I_{\text{sw,I}} \right| + K \cdot \sum_{T_s} \left| I_{\text{sw,II}} \right|$$
$$F_3 = \sum_{T_s} I_{\text{sw,I}}^2 + K \cdot \sum_{T_s} I_{\text{sw,II}}^2, \tag{2.17}$$

where $I_{\text{sw,I}}$ and $I_{\text{sw,II}}$ are equal to the transition currents for Type I and Type II transitions, respectively, in each phase leg and within a switching cycle. Constant $K \in]0,1[$ is introduced in order to prioritize the minimization of Type I transitions losses in front of Type II transition losses. A value of $K = 0.1$ will be considered throughout this chapter.

2.5.3. Optimization process

Objective functions F_1, F_2, and F_3 are minimized independently using the numerical computation algorithms provided by MATLAB's Global Optimization Toolbox. The optimization problems are

$$\min\left(F_f\right) = F_f\left(X_f\right), \tag{2.18}$$

where $f \in \{1,2,3\}$ and $X_f = \{\alpha_{a1},\alpha_{a2},\alpha_{b1},\alpha_{b2},\varphi\}_f$ is F_f optimum solution at a given point defined by V_A^*, V_B^*, and P^*.

The constraint equations are

$$\begin{cases} 0° \le \alpha_{z1} \le \alpha_{z2} \le 90° \\ 0° \le \varphi \le 90° \qquad \forall z \\ P = P^*. \end{cases} \tag{2.19}$$

The optimum F_f switching angles, shown in Fig. 2.12, present certain patterns that are similar among all F_f. First, in each F_f, a symmetry can be identified between a- and b-side optimum switching angles, which can be expressed as $\{\alpha_{a1},\alpha_{a2}\}_f|_d = \{\alpha_{b1},\alpha_{b2}\}_f|_{(1/d)}$. Second, in all F_f solutions, for $d \neq 1$, α_{z1} begins at nearly 0° and increases, and α_{z2} begins at nearly 90° and decreases. Both angles present a trend change at approximately the same phase-shift value ($\varphi_{z,\text{th},f}$ in Fig. 2.12). Eventually, they both increase until reaching 90°. $\varphi_{z,\text{th},f}$ is equal to 0° when $d = 1$ and increases as d departs from 1. For $d > 1$, $\varphi_{a,\text{th},f} < \varphi_{b,\text{th},f}$, and for $d < 1$, $\varphi_{a,\text{th},f} > \varphi_{b,\text{th},f}$.

It is interesting to note that, for $d = 1$, the optimum solution for F_1 sets all switching angles to 90°, producing pure square voltage waveforms in v_a and v_b as with the PSM. This occurs because, in this case, for a given transferred power value, maximizing the amplitude of v_a and v_b fundamental

components minimizes the required transformer rms current value, therefore minimizing the conduction losses. This is consistent with previous studies on the 2L DAB case [34].

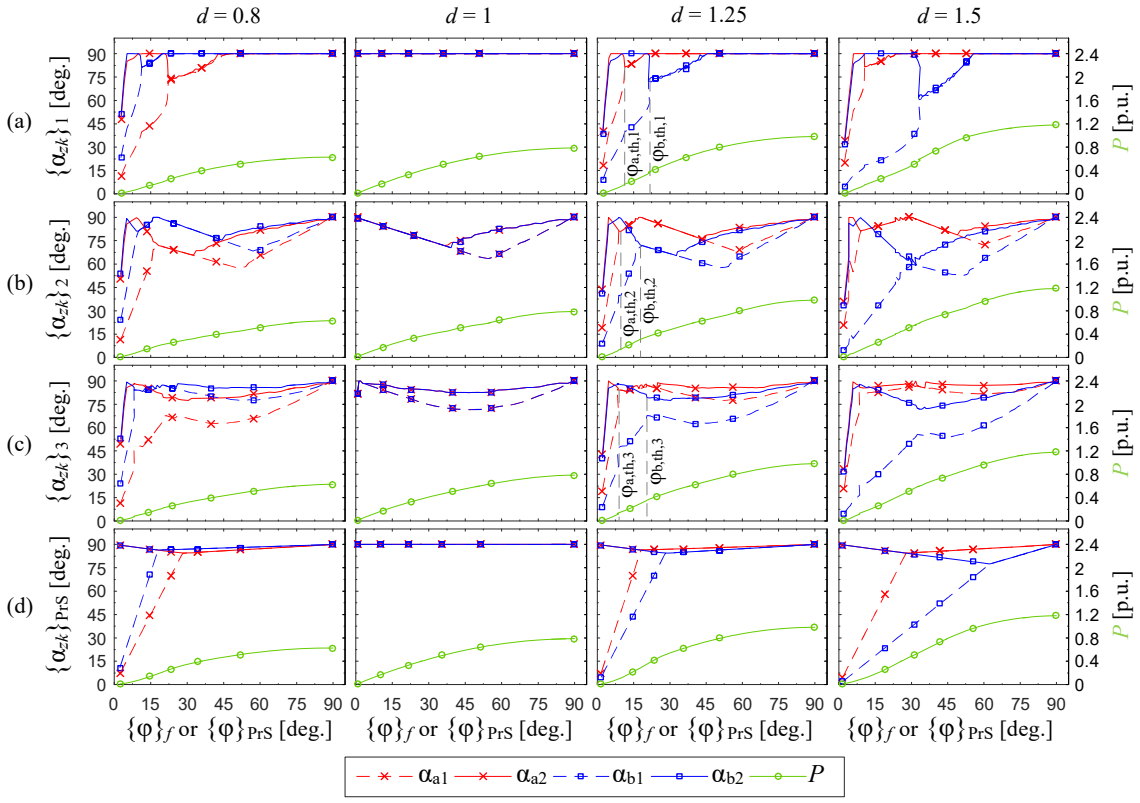


Fig. 2.12. Switching angle values (left axis on each subfigure) and transferred power (right axis) as a function of phase shift. (a) Solution that minimizes F_1. (b) Solution that minimizes F_2. (c) Solution that minimizes F_3. (d) Proposed practical solution.

It should be noted that negative switching angles are not allowed by the constraints. Optimization processes allowing negative angles have shown that F_1, F_2, and F_3 optimum results giving negative angles, only appear at very low powers, accompanied with high phase shift values. Hence, as power grows, phase shift would have a non-monotonic variation, which hinders the definition of a simple and practical modulation parameter solution inferred from the optimum results.

2.5.4. Practical solution

The optimal switching angles as a function of φ of the three formulated optimization problems shown in Fig. 2.12 present a common pattern, as discussed previously. Fig. 2.13 aims to reproduce this pattern through the plot of variables $\{\alpha_{z1},\alpha_{z2}\}_{\mathrm{PrS}}$. These are the switching angles defined by the proposed practical solution, which can be expressed as

$$\{\alpha_{z1}\}_{\text{PrS}} = \begin{cases} 0° + \dfrac{\alpha_{z,\text{th}}}{\varphi_{z,\text{th}}} \cdot \varphi, & \varphi < \varphi_{z,\text{th}} \\ \alpha_{z,\text{th}} + \dfrac{90° - \alpha_{z,\text{th}}}{90° - \varphi_{z,\text{th}}} \cdot (\varphi - \varphi_{z,\text{th}}), & \varphi \geq \varphi_{z,\text{th}} \end{cases}$$
$$\{\alpha_{z2}\}_{\text{PrS}} = \begin{cases} 90° - K_{\alpha,\text{th}} \cdot \varphi, & \varphi < \varphi_{z,\text{th}} \\ \alpha_{z,\text{th}} + \dfrac{90° - \alpha_{z,\text{th}}}{90° - \varphi_{z,\text{th}}} \cdot (\varphi - \varphi_{z,\text{th}}), & \varphi \geq \varphi_{z,\text{th}} \end{cases} \quad (2.20)$$

where

$$\begin{aligned} \varphi_{\text{a,th}} &= K_{\varphi,\text{th}} \cdot \left|1 - 1/d^2\right| \\ \varphi_{\text{b,th}} &= K_{\varphi,\text{th}} \cdot \left|1 - d^2\right| \\ \alpha_{z,\text{th}} &= 90° - K_{\alpha,\text{th}} \cdot \varphi_{z,\text{th}} \end{aligned} \quad (2.21)$$

and $K_{\varphi,\text{th}}$ is a constant that forces a $\varphi_{z,\text{th}}$ value close to $\varphi_{z,\text{th},f}$ in Fig. 2.12 for all of the considered d values in the optimization process. To guarantee the converter capability to transfer maximum power, $\varphi_{z,\text{th}}$ has to be limited to $\varphi_{\text{th,max}} < 90°$. From (2.21), it can be derived that for

$$d \in \left[\left(1 + \varphi_{\text{th,max}} / K_{\varphi,\text{th}}\right)^{-1/2}, \left(1 + \varphi_{\text{th,max}} / K_{\varphi,\text{th}}\right)^{1/2} \right] \quad (2.22)$$

then $\varphi_{z,\text{th}} \leq \varphi_{\text{th,max}}$. Otherwise, for d values outside this range, $\varphi_{z,\text{th}} = \varphi_{\text{th,max}}$ will have to be enforced. For instance, if $K_{\varphi,\text{th}} = 50°$, $K_{\alpha,\text{th}} = 0.2$, and $\varphi_{\text{th,max}} = 80°$, the range defined in (2.22) is $d \in [0.62, 1.61]$. Fig. 2.12(d) presents the practical angle values for the previous set of practical solution parameter values, which provide a good approximation of the optimum solutions.

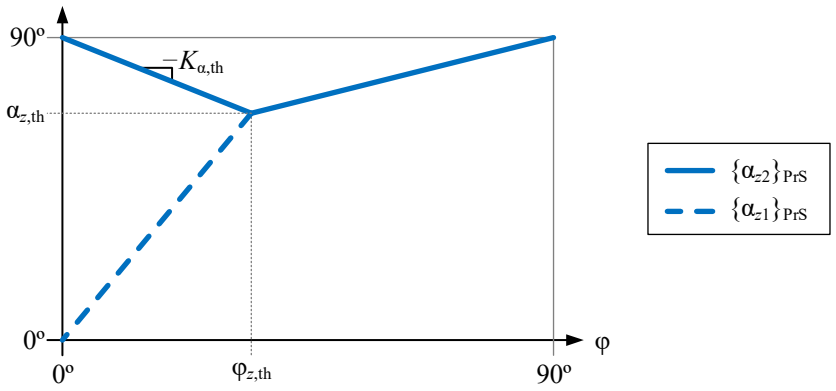


Fig. 2.13. Practical switching angles as a function of φ.

2.5.5. Comparison of the practical solution and F_1, F_2, and F_3 optimum solutions

To evaluate the suitability of the proposed practical solution, the value of the objective functions obtained with the practical solution, illustrated in Fig. 2.12(d) [$F_f(X_{PrS})$], are compared with the optimum values of the objective functions [$F_f(X_f)$] and with the values of the objective functions obtained when using the PSM in the present converter [$F_f(X_{PSM})$]. These results are presented in Fig. 2.14 as a function of P. Solution X_{PSM} $\forall d$ is the same as the practical solution for $d = 1$, shown in Fig. 2.12(d).

The base voltage, current, and power values are

$$\begin{aligned} V_{base} &= V_A \\ I_{base} &= \frac{V_A}{2\pi \cdot f_s \cdot L} \\ P_{base} &= \frac{V_A^2}{2\pi \cdot f_s \cdot L}. \end{aligned} \tag{2.23}$$

As it can be observed in Fig. 2.14(a), $F_1(X_{PrS})$ is very close to the minimum possible value [$F_1(X_1)$] and is lower than $F_1(X_{PSM})$, especially at low-to-medium powers. Only for very low powers, $F_1(X_{PrS})$ is not close to the minimum.

In Fig. 2.14(b), for low-to-medium powers and $d \neq 1$, $F_2(X_{PrS})$ is greater than the minimum [$F_2(X_2)$] but significantly lower than $F_2(X_{PSM})$. These differences increase for $d << 1$ and $d >> 1$.

In Fig. 2.14(c), $F_3(X_{PrS})$ is very close to the minimum [$F_3(X_3)$] for the whole d range, and lower than $F_3(X_{PSM})$ for $d \neq 1$ and low-to-medium powers.

In conclusion, the proposed practical solution is expected to achieve lower conduction and switching losses than PSM for low-to-medium powers when $d \neq 1$. Also, if in (2.16) I^2_{sw} influence is higher than $|I_{sw}|$ influence due to constructive parameters of the converter, then the switching losses will be very close to the minimum. At high powers and in all the power range for $d = 1$, both the practical and PSM solutions are close to or equal to the minimum possible conduction and switching losses.

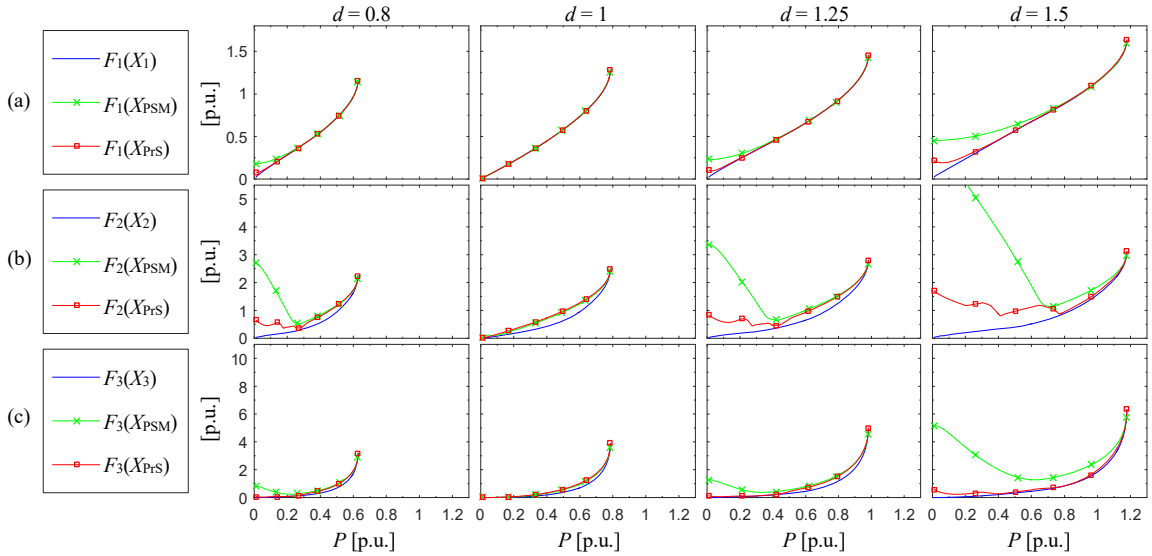


Fig. 2.14. Objective function values as a function of P for solutions X_f, X_{PrS}, and X_{PSM} (V_A = 1 p.u.). (a) F_1. (b) F_2. (c) F_3.

2.6. Simulation and experimental results

Simulation and experimental tests have been carried out to prove the effectiveness of the capacitor-voltage-balancing control and the proposed practical solution for the 3L-DAB. A MATLAB-Simulink lossless model of the converter in Fig. 2.1 is used to perform the simulations. All simulations assume $n = 1$, $C_z = 100$ μF, and $L = 300$ μH. The experimental test are performed with the converter prototype shown in Appendix A, Section A.1.1.

In all simulations and experiments, a dc voltage source with a low series resistance (10 mΩ) is connected across the a-side dc-link and a resistive load (R_B) across the b-side dc-link.

The converter is controlled at $f_s = 10$ kHz with the proposed practical solution presented in Section 2.5.4. The capacitor-voltage-balancing control scheme of Fig. 2.7 is employed, with a simple proportional compensator (with gain G_{z2}) as regulator. The switching angle values (α_{zok} and α_{zik}) outputted by the balancing control are processed by the algorithm presented in Appendix B, in order to limit its values to the defined boundaries ($\Delta\alpha_{z,\min} = 2.52^o$, corresponding to $t_{b,z} = 700$ ns $\forall z$).

The load voltage (V_B) is controlled by the regulator shown in Fig. 2.15. It is comprised of a pure integrator, a zero at frequency $f_{z,ps}$, and a pole at frequency $f_{p,ps}$. Reference value V_o^* is equal to the V_B defined in each working point. The output load resistor value (R_B) is adjusted so that the phase shift control settles on the desired φ and V_B defined in the working point.

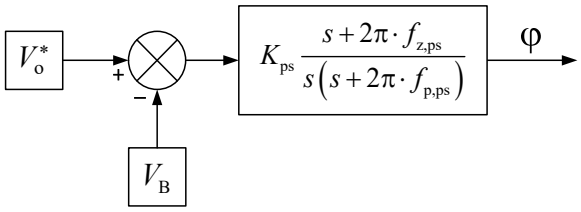


Fig. 2.15. Control scheme of the load-voltage regulator.

A low-pass filter, with a cut-off frequency of 1000 Hz, is employed to filter the capacitor voltages on both sides. Its transfer function is $H_{filt}(s) = 2\pi\cdot1000/(s + 2\pi\cdot1000)$.

All compensator parameters have been tuned through simulation and experiments to obtain an acceptable performance and stable behavior.

2.6.1. Steady state results

The steady-state behavior at two working points is analyzed:

- WP1: $d = 1$ ($V_A = 100$ V, $V_B = 100$ V) and $\varphi \approx 60^o$.
- WP2: $d = 1.5$ ($V_A = 80$ V, $V_B = 120$ V) and $\varphi \approx 30^o$.

The control parameters are $G_{a2} = -G_{b2} = 0.1$, $K_{PS} = 5000$, $f_{z,ps} = 50$ Hz, and $f_{p,ps} = 2500$ Hz. Fig. 2.16 presents the simulation results for the relevant voltage and current waveforms. It can be observed that both dc links have capacitor voltage balance, since v_a and v_b present voltage steps of equal amplitude. The red and green dots indicate when a transition is of Type I or Type II, respectively. Fig. 2.17 shows the experimental results for the same working points and conditions of Fig. 2.16. Both the simulation and experimental waveforms are in close agreement. Dc-link capacitor voltage balancing is also achieved.

Table 2.2 presents a comparison of the analytical, simulation, and experimental values of the three objective functions for both working points. The results are again fairly similar.

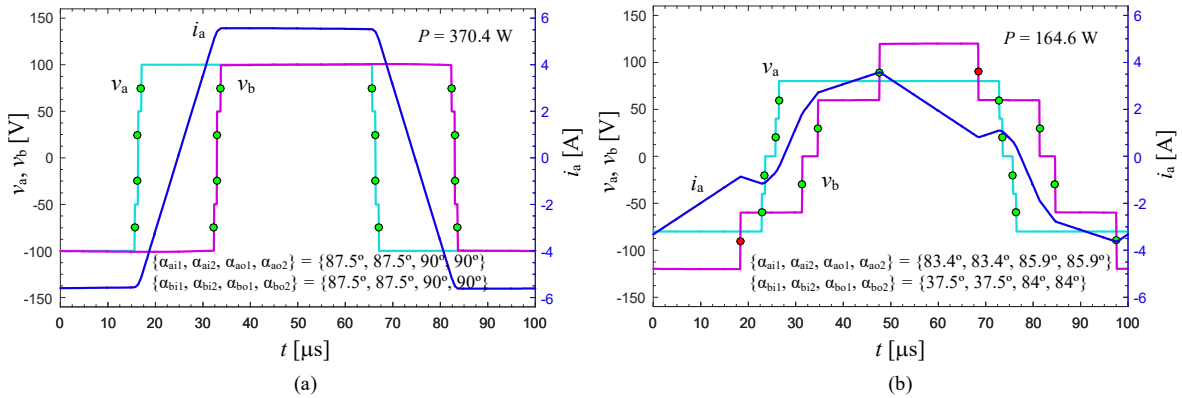


Fig. 2.16. Simulation results for v_a, v_b, and i_a, using the limited practical solution. (a) WP1. (b) WP2.

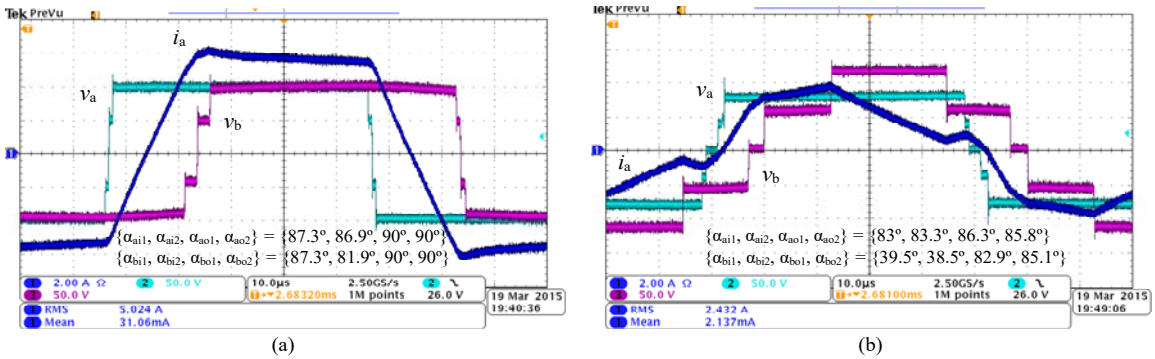


Fig. 2.17. Experimental results for v_a, v_b, and i_a, using the limited practical solution. (a) WP1. (b) WP2.

		F_1	F_2	F_3
WP1	**Analytic**	0.92 p.u.	1.62 p.u.	1.64 p.u.
	Simulation	0.93 p.u.	1.62 p.u.	1.65 p.u.
	Experimental	0.95 p.u.	1.67 p.u.	1.76 p.u.
WP2	**Analytic**	0.56 p.u.	0.94 p.u.	0.38 p.u.
	Simulation	0.56 p.u.	0.94 p.u.	0.38 p.u.
	Experimental	0.57 p.u.	0.81 p.u.	0.38 p.u.

Table 2.2. Comparison of the objective function values given with the proposed practical solution..

2.6.2. Transient results

Fig. 2.18 and Fig. 2.19 present the simulation and experimental results that demonstrate the performance of the system, with the load-voltage V_B control enabled (Fig. 2.15), under different transients: a step in V_B voltage reference [V_o^*; Fig. 2.18(a.1) and Fig. 2.18(a.2)], a step in the load [Fig. 2.18(b.1) and Fig. 2.18(b.2)], and a capacitor-voltage-balancing transient [Fig. 2.19 (a) and Fig. 2.19(b)].

In Fig. 2.18, the simulation and experimental results are similar. All controls perform satisfactorily, keeping the capacitor voltages balanced during the transients, with minor adjustments on the inner and outer switching angles.

In Fig. 2.19, an initial unbalance in v_{Cb1} and v_{Cb2} is forced by disabling the b-side capacitor-voltage-balancing control and loading the b-side capacitors with two different resistance values. Once the b-side balancing control is enabled, the capacitor voltage balance is quickly recovered. As shown in the simulation results [Fig. 2.19(a)], the b-side capacitor-voltage-balancing control takes action by diverging the values of the inner and outer angles (α_{zik}, α_{zok}) from its steady state values (approximately equal to α_{zk}), effectively correcting the existing unbalance. Although the switching angle values from the experimental values could not be obtained, it can be inferred that they are similar to the simulation values, due to the similarities between the simulation and experimental capacitor voltage waveforms.

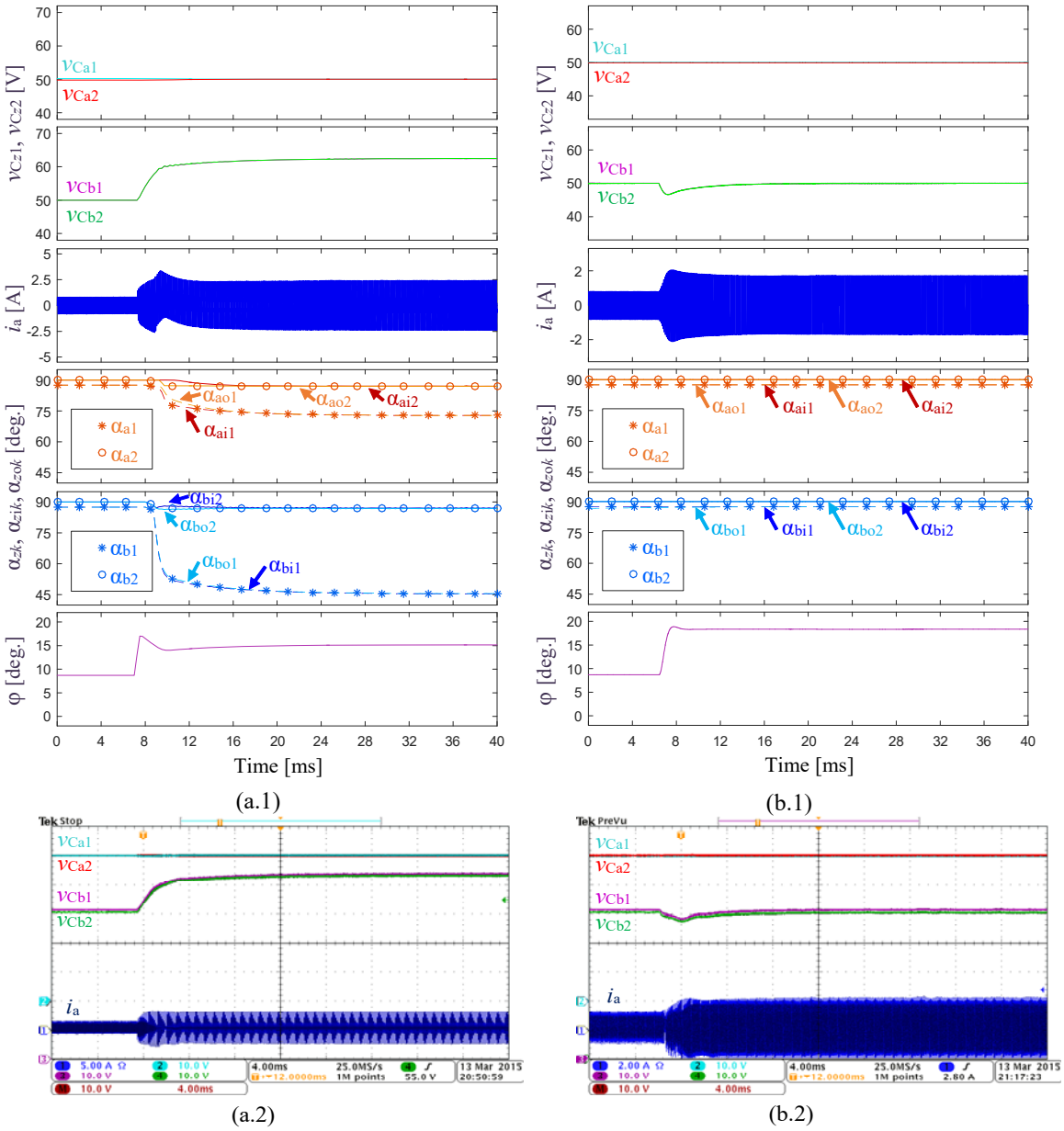


Fig. 2.18. Results of two types of transient responses for v_{Czk}, i_a, α_{zk}, α_{zik}, α_{zok}, and φ ($\forall z,k$) for the proposed practical solution modulation strategy under the following conditions: V_A = 100 V, capacitor-voltage-balancing control enabled, $|G_{z2}|$ = 0.1, $f_{z,ps}$ = 50 Hz, and $f_{p,ps}$ = 2500 Hz. (a) Simulation (a.1) and experimental (a.2) results for transient response under a V_o^* step change from 100 V to 125 V (R_B = 132 Ω, K_{ps} = 5000). (b) Simulation (b.1) and experimental (b.2) results of transient response under a R_B step change from 132 Ω to 66 Ω (V_o^* = 100 V, K_{ps} = 20000).

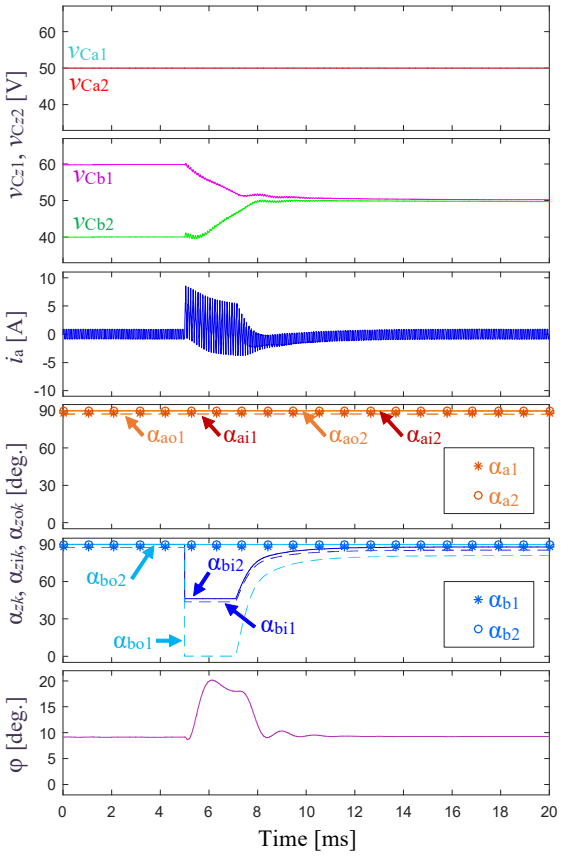


Fig. 2.19. Results for v_{Czk}, i_a, α_{zk}, α_{zik}, α_{zok}, and φ ($\forall z$, $\forall k$) under a capacitor voltage balancing recovery transient with the proposed modulation an the following conditions: V_A = 100 V, R_B = 132 Ω, a-side capacitor-voltage-balancing control enabled, $|G_{z2}|$ = 0.15, V_o^* = 100 V, K_{ps} = 50000, $f_{z,ps}$= 50 Hz, and $f_{p,ps}$= 2500 Hz. (a) Simulation results. (b) Experimental results.

2.7. Efficiency comparison

Fig. 2.20 compares the power loss (P_{loss}) and efficiency (η) of a 3L-DAB operated with 100 V MOSFETs (FDPF3860T, with ON resistance $R_{DS,on}$ = 30 mΩ) and the proposed modulation strategy (Section 2.5.4) and a (two-level) FB-DAB operated with 200 V MOSFETs (STF20NF20, $R_{DS,on}$ = 100 mΩ) and two possible modulation strategies (PSM and TRM-TZM [30], Fig. 1.8). Only semiconductor device losses (conduction and switching) are considered and a wide operating range at f_s = 100 kHz is explored. The comparison has been performed combining simulation and experimental data. The system is simulated in MATLAB-Simulink. Conduction losses are then calculated from the simulated semiconductor current values and the datasheet $R_{DS,on}$ value. Switching losses are calculated from the simulated current values and expression

$$E_{sw} = a \cdot I_{sw}^2 + b \cdot |I_{sw}| + c \ [\mu J], \tag{2.24}$$

where coefficients *a*, *b*, and *c* depend on the device, the type of switching transition, and the value of blocking voltage V_{DS}. A suitable set of coefficient values for each different case has been obtained from the switch and diode energy loss during switching transitions experimentally measured using a double pulse board (see Appendix A, Section A.6) at different blocking voltages V_{DS}, over the full current range up to 16 A, and with a gate resistance R_g = 6.6 Ω. For example, Table 2.3 presents the value of these coefficients for the nominal V_{DS} value that together with (2.24), approximate the experimentally measured losses (in both the switch and diode, at turn-on E_{on}) and turn-off (E_{off}) transitions, involving one or two diodes ("1d", "2d") with a coefficient of determination (R^2) higher than 90 % for the switch and higher than 70 % for the diode. Similar sets of coefficient values have been obtained for V_{DS} = {40,44.5,55,60} V for FDPF3860T and V_{DS} = {80,89,110,120} V for STF20NF20. For currents below 2 A, a simple linear regression has been applied to compute diode turn-off losses.

		FDPF3860T @ V_{DS} = 50 V			**STF20NF20 @ V_{DS} = 100 V**		
		a	***b***	***c***	***a***	***b***	***c***
Switch	$E_{on,1d}$	0	0.548	0	0	8.059	0
	$E_{on,2d}$	0	0.604	0	-	-	-
	$E_{off,1d}$	0.046	−0.192	0.398	0.088	0.053	0
	$E_{off,2d}$	0.04	−0.173	0.23	-	-	-
Diode	$E_{off,1d}$	0	0.131	2.366	0	2.466	16.55
	$E_{off,2d}$	0	0.145	2.984	-	-	-

Table 2.3. Switching loss coefficients.

It can be observed in Fig. 2.20 that both conduction and switching losses are lower in the 3L-DAB case, leading to a higher efficiency.

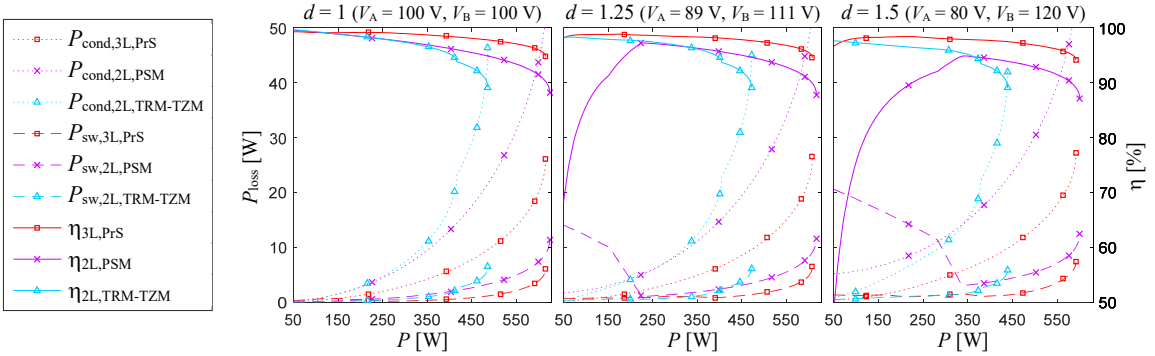


Fig. 2.20. Comparison of the losses and efficiency of a 3L-DAB operated with the proposed modulation and a 2L-DAB operated with PSM and TRM-TZM. Conditions: f_s = 100 kHz, L = 20 μH, $K_{\alpha,th}$ = 0.2, and $\Delta\alpha_{z,min}$ = 10.8° ∀z.

Table 2.4 presents a comparison of the practical solution (PrS) and a global optimum (GO) obtained through the minimization of a function defined by the addition of all the 3L-DAB converter semiconductor losses (conduction and switching) in the same conditions as in Fig. 2.20. The comparison is performed under nine working points. Although differences appear in some switching angles, the efficiency results are in general almost identical except for the cases with $d \neq 1$ and low power levels.

d	***P* [W]**		**α_{a1}**	**α_{a2}**	**α_{b1}**	**α_{b2}**	**η**
1	100	**PrS**	79.2º	90º	79.2º	90º	99.17 %
		GO	79.2º	90º	76.6º	87.4º	99.2 %
	300	**PrS**	79.2º	90º	79.2º	90º	98.95 %
		GO	79.2º	90º	79.2º	90º	98.95 %
	500	**PrS**	79.2º	90º	79.2º	90º	97.68 %
		GO	79.2º	90º	79.2º	90º	97.68 %
1.25	100	**PrS**	58.8º	87.6º	36.9º	87.6º	98.8 %
		GO	79.2º	90º	43.3º	86.8º	99.31 %
	300	**PrS**	79.2º	90º	77.3º	88.1º	98.45 %
		GO	79.2º	90º	66.2º	90º	98.58 %
	500	**PrS**	79.2º	90º	79.2º	90º	97.42 %
		GO	79.2º	90º	73.2º	90º	97.44 %
1.5	100	**PrS**	48.5º	86.8º	19.8º	86.8º	98.1 %
		GO	79.2º	90º	26º	83.1º	99.19 %
	300	**PrS**	79.2º	90º	43.8º	82.9º	98.02 %
		GO	79.2º	90º	54.4º	84.5º	98.09 %
	500	**PrS**	79.2º	90º	69.6º	80.4º	96.87 %
		GO	79.2º	90º	66.6º	90º	96.9 %

Table 2.4. Comparison of practical solution and global optimum.

2.8. Conclusion

This chapter constitutes a preliminary study to show the feasibility and potential advantages of replacing the two-level legs of the conventional (two-level) FB-DAB converter by three-level legs, in any application where this converter is of interest. A 3L-DAB converter employing 3L-NPC legs, has been proposed and studied. An effective modulation scheme with nine DoF has been first defined. Four DoF are employed to design a dc-link capacitor-voltage-balancing control. The remaining five DoF are employed to control the power flow and minimize the predominant converter losses. The pattern defined by the optimum values of these five DoF (represented as independent variables) has been explored through the analysis of three decoupled optimization problems, related to the converter conduction and switching losses. Finally, simple and practical closed-form expressions of these modulation parameters have been provided, representing this modulation strategy a good trade-off between pattern simplicity and accuracy of approximation to the three individual optimum solutions. Moreover, the proposed practical solution offers greater converter performance when compared with the conventional PSM.

From the analytical, simulation, and experimental results, it is concluded that it is feasible to implement a DAB dc-dc converter from 3L-NPC legs. In addition, the multilevel topology provides benefits compared with the conventional 2L-DAB converter; namely, an increase in the total dc-link voltage for a given semiconductor technology, the possibility of using lower-voltage-rated semiconductor devices with better performance figures for a given dc-link voltage, lower converter losses (especially for $d \neq 1$), and lower transformer-current harmonic distortion which leads to lower magnetic losses.

CHAPTER 3.

STUDY OF A FOUR-LEVEL NEUTRAL-POINT-CLAMPED DUAL-ACTIVE-BRIDGE DC-DC CONVERTER

Abstract — This chapter presents the study of a four-level NPC DAB dc-dc converter, following a structure similar to the three-level case. That is, a general modulation pattern is initially defined, the dc-link capacitor voltage balancing is analyzed in detail, and proper balancing control schemes are designed. Then a set of decoupled optimization problems related to the converter losses is formulated, and from its solutions, a simple and practical modulation strategy resembling these solutions is provided. The good performance of the proposed four-level NPC DAB converter operated with the proposed modulation strategy and capacitor-voltage-balancing control is verified through simulation and experiments.

3.1. Introduction

This chapter introduces a DAB dc-dc converter built upon four four-level NPC (4L-NPC) legs. A proper modulation strategy is proposed and characterized. The dc-link capacitor voltage balancing is analyzed and different closed-loop capacitor-voltage-balancing control schemes are proposed. By performing an optimization of the modulation strategy parameter values and studying the results, a set of simple and practical equations, similar to the solution proposed for the three-level case, is proposed, improving the converter performance. Finally, simulation and experimental tests are done to verify the proposed capacitor-voltage-balancing controls and the practical modulation strategy.

This chapter is organized as follows. Section 3.2 presents the converter topology. Section 3.3 presents the fundamentals of the modulation strategy. Section 3.4 presents the study of the capacitor voltage balancing and defines different control schemes. Section 3.5 presents the performance optimization study and proposes a practical solution for the modulation strategy based on the results. Section 3.6 presents the simulation and experimental results to verify the modulation and control performance. Finally, Section 3.7 outlines the conclusions.

3.2. Topology

Fig. 3.1 presents the proposed 4L-NPC DAB dc-dc converter (4L-DAB) topology, which is an extension to four levels of the 3L-DAB. In the 4L-DAB, compared to the 3L-DAB, each side dc-link has four voltage levels, with connection points 1_z, 2_z, 3_z, and 4_z, and two 4L-NPC legs (z_1 and z_2).

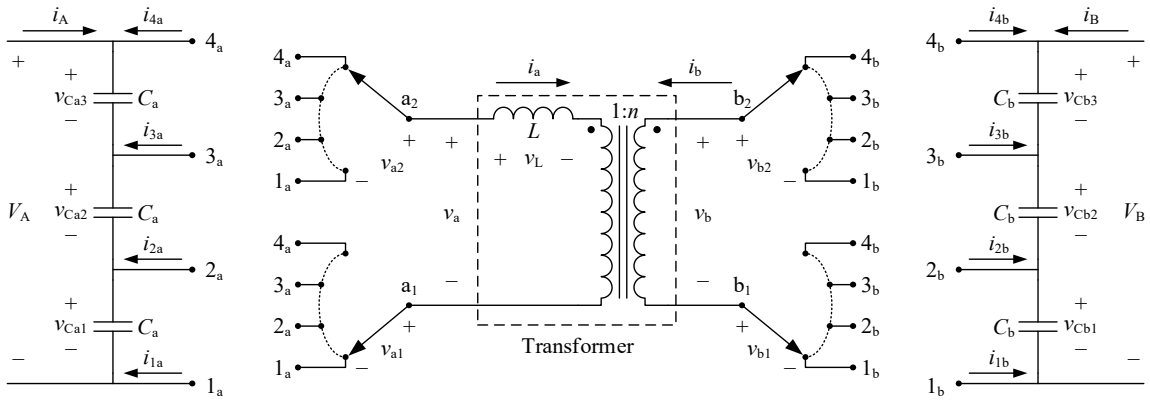


Fig. 3.1. Topology of the proposed 4L-DAB dc-dc converter with phase legs a_1, a_2, b_1, and b_2 depicted as single-pole quadruple-throw switches.

3.3. Modulation

Fig. 3.2 presents the modulation pattern for the 4L-DAB. The two four-level legs on each z-side are controlled to produce the four-level staircase waveforms v_{z1} and v_{z2}, to synthesize a v_z transformer voltage waveform with seven voltage levels (two more than the 3L-DAB). The 4L-DAB z-side switching-state sequence (shown in top of Fig. 3.2 for the a-side) is similar to the 3L-DAB case, with four additional switching states per switching cycle.

The dwell times of the 4L-DAB z-side switching states can be defined by six independent switching angles; i.e., α_{zi1}, α_{zi2}, α_{zi3}, α_{zo1}, α_{zo2}, and α_{zo3}, with

$$\begin{aligned} -90° \le \alpha_{zi1} \le \alpha_{zi2} \le \alpha_{zi3} \le 90° \\ -90° \le \alpha_{zo1} \le \alpha_{zo2} \le \alpha_{zo3} \le 90°. \end{aligned} \tag{3.1}$$

As in the 3L-DAB, the established definition of the switching-states dwell times with these switching angle variables allows maintaining $\overline{v}_z = 0, \forall z$, even when the dc-link capacitor voltages are not balanced. It also forces a symmetrical operation of both full-bridge legs. Odd symmetry is guaranteed in v_a, v_b, v_L, and i_a waveforms, which is convenient for the capacitor voltage balancing.

The six switching angles per side (α_{zi1}, α_{zi2}, α_{zi3}, α_{zo1}, α_{zo2}, and α_{zo3}) plus the phase shift (φ), sum up 13 DoF available to control the capacitor voltage balancing, the converter performance, and the power flow. If

$$\begin{aligned} \alpha_{zo1} &= \alpha_{zi1} = \alpha_{z1} \\ \alpha_{zo2} &= \alpha_{zi2} = \alpha_{z2} \\ \alpha_{zo3} &= \alpha_{zi3} = \alpha_{z3} \end{aligned} \tag{3.2}$$

and the dc-link capacitor voltages are balanced, then quarter-wave symmetry is guaranteed and even-order harmonics are eliminated in v_a, v_b, v_L, and i_a waveforms.

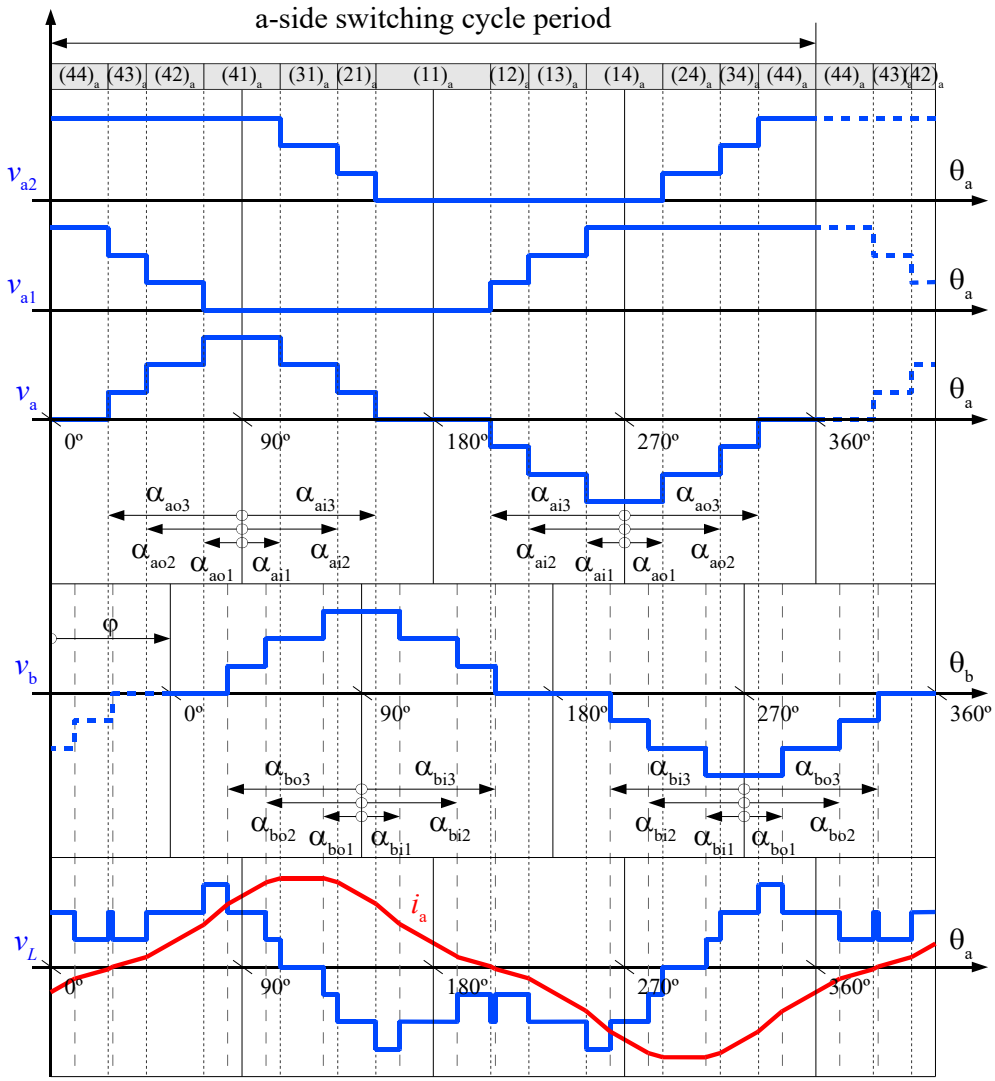


Fig. 3.2. Voltage waveforms v_{a1}, v_{a2}, v_a, v_b, and v_L, and current i_a for the proposed four-level modulation. Switching states for a-side are shown on top of the figure. All waveforms are plotted assuming $V_A = V_B/n$.

3.4. Capacitor voltage balancing

The capacitor-voltage-balancing issue for the 4L-DAB is more challenging than in the 3L-DAB, since it has an additional inner point in each dc link. The simulation results shown in Fig. 3.3(a) confirm this claim. These results show the capacitor voltages transient response under an initial balanced state, with an arbitrary set of switching angles defining v_a and v_b waveforms with equal-value dwell times, and under the absence of a closed-loop control. In less than 50 ms, the transient reaches a steady state with an unacceptable permanent capacitor voltage unbalance that could destroy the devices due to an excessive blocking voltage, besides leading to nonoptimal operating conditions. Therefore, a means to guarantee the capacitor voltage balancing is required.

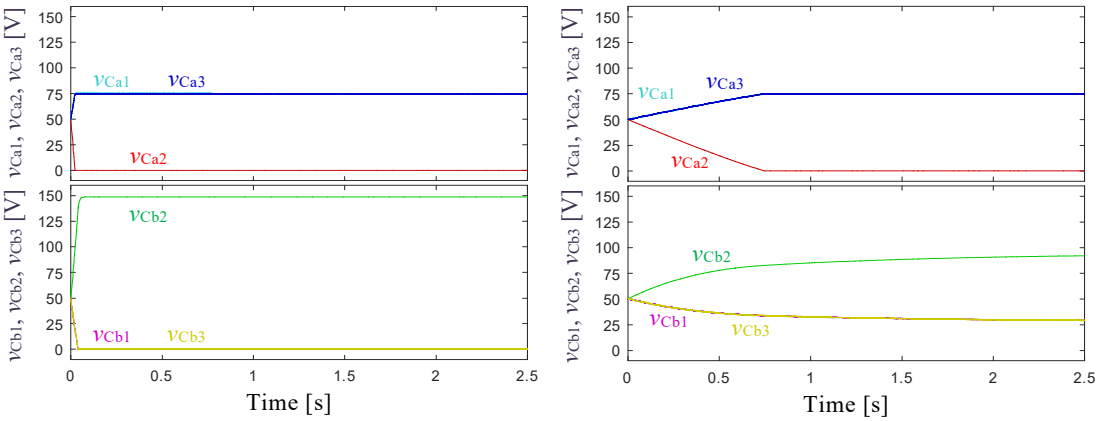


Fig. 3.3. Simulation results of a transient in the capacitor voltages during converter operation, under the following conditions: V_A = 150 V, C_z = 100 μF, φ = 60°. A resistive load (R_B) is present across the b-side output and its value is selected in order to set $V_B \approx 150$ V. (a) Simulation with arbitrary switching angles $\{\alpha_{z1},\alpha_{z2},\alpha_{z3}\} = \{15°,45°,75°\}$ $\forall z$ and R_B = 62 Ω. (b) Simulation with $\{\alpha_{z1},\alpha_{z2},\alpha_{z3}\} = \{15°,37.76°,75°\}$ $\forall z$, and R_B = 72.5 Ω. Switching angle α_{z2} is computed with (3.6) in order to lessen the capacitor voltage unbalance on both sides.

3.4.1. Control operating principle and control schemes

The currents injected into or drawn from the inner points of the dc-link (2_z, 3_z) alter the ratio between the three dc-link capacitor voltages. These currents are

$$\begin{aligned} i_{2z} &= S_{z12} \cdot i_z - S_{z22} \cdot i_z \\ i_{3z} &= S_{z13} \cdot i_z - S_{z23} \cdot i_z, \end{aligned} \tag{3.3}$$

where S_{zj2} and S_{zj3} are equal to 1 when leg z_j is connected to dc-link point 2_z and 3_z, respectively, and 0 otherwise.

Following the same procedure as in the three-level case (Section 2.4.1), let us consider the effect of the fundamental component of i_z ($i_{z,1}$), as its amplitude is greater than each of the harmonic amplitudes. Current $i_{z,1}$ can be decoupled into $i^{p}_{z,1}$ component, in phase with $v_{z,1}$ (the fundamental component of v_z), and into a $i^{q}_{z,1}$ component, in quadrature with $v_{z,1}$.

Currents $i^{p}_{z,1}$ and $i^{q}_{z,1}$ are depicted in Fig. 3.4, together with v_z. The shaded areas in Fig. 3.4 represent the electrical charge injected into (positive sign) or drawn from (negative sign) the z-side dc-link neutral points 2_z (red areas) and 3_z (blue areas) by these currents. To keep a preexisting capacitor voltage balance, the sum of the red areas must be zero and the sum of the blue areas must also be zero. The sum of $i^{q}_{z,1}$ red areas and the sum of $i^{q}_{z,1}$ blue areas are always zero, regardless of the values of the switching angles, thanks to v_z odd symmetry. Therefore, to keep a preexisting capacitor voltage balance, it is only necessary to cancel out the red and blue areas of $i^{p}_{z,1}$, or in other words, the charge provided by $i^{p}_{z,1}$ to each inner dc-link point within a switching cycle must be zero. To simplify, and thanks to the even symmetry of $i^{p}_{z,1}$ shaded areas along the switching period, let us only consider half of the switching period shown in Fig. 3.4. The per-unit charge provided to inner dc-link points 2_z and 3_z by $i^{p}_{z,1}$ during this period is

$$\begin{aligned} q_{2z} &= \sin\left(\alpha_{zo2}\right) - \sin\left(\alpha_{zo1}\right) - \left(\sin\left(\alpha_{zi3}\right) - \sin\left(\alpha_{zi2}\right)\right) \\ q_{3z} &= \sin\left(\alpha_{zo3}\right) - \sin\left(\alpha_{zo2}\right) - \left(\sin\left(\alpha_{zi2}\right) - \sin\left(\alpha_{zi1}\right)\right), \end{aligned} \tag{3.4}$$

respectively. If (3.2) is assumed for simplicity, then $q_{2z} = -q_{3z}$. Moreover, in order to force that $i^{p}_{z,1}$ provides a null charge to the inner dc-link points, let us set $q_{2z} = -q_{3z} = 0$, which results in

$$\sin\left(\alpha_{z1}\right) + \sin\left(\alpha_{z3}\right) - 2 \cdot \sin\left(\alpha_{z2}\right) = 0. \tag{3.5}$$

Isolating α_{z2} from (3.5)

$$\alpha_{z2} = \arcsin\left(\frac{\sin\left(\alpha_{z1}\right) + \sin\left(\alpha_{z3}\right)}{2}\right) \tag{3.6}$$

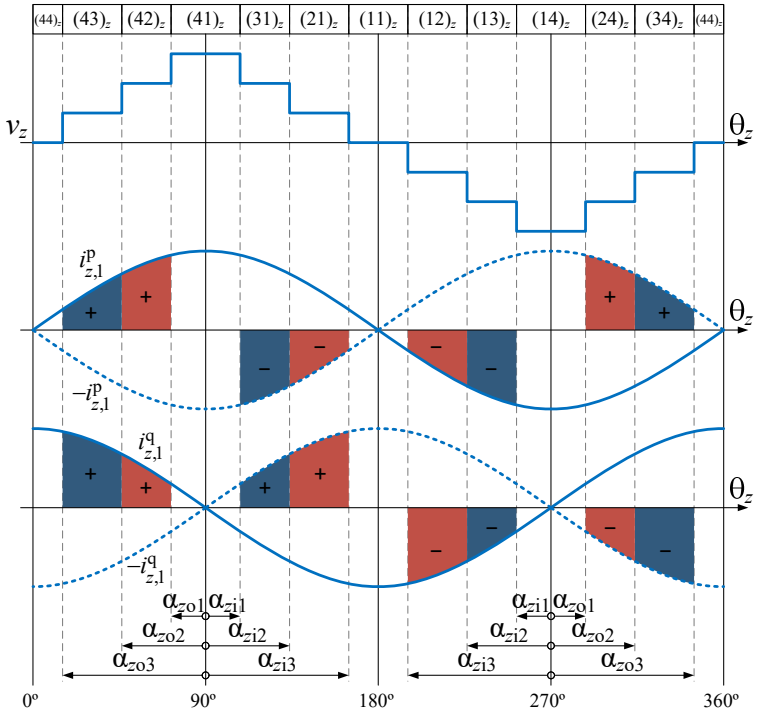


Fig. 3.4. Voltage v_z and the in-phase and in-quadrature components of i_z fundamental component ($i^p_{z,1}$ and $i^q_{z,1}$). The red and blue areas depict the charge injected into (+) or drawn from (–) dc-link neutral point 2_z and 3_z, respectively, by $i^p_{z,1}$ and $i^q_{z,1}$.

However, when all i_z harmonics are taken into consideration or when converter non-idealities exist, (3.6) does not guarantee maintaining a preexisting capacitor voltage balance. This fact is demonstrated with the simulation results shown in Fig. 3.3(b), where, even though the charge provided by $i_{z,1}$ to the dc-link neutral points is zero thanks to (3.6), the i_z harmonics provide a non-zero charge to the inner dc-link points, unbalancing the capacitor voltages to unacceptable values. It is worth noting, however, that the capacitor voltage unbalance transient is certainly slowed and lessened in comparison to the arbitrary-switching-angles simulation of Fig. 3.3(a).

Consequently, a control action is needed that modifies the values of the inner (α_{zi1}, α_{zi2}, α_{zi3}) and outer (α_{zo1}, α_{zo2}, α_{zo3}) angles in order to inject a non-zero charge during a switching cycle and, ultimately, correct any possible capacitor voltage unbalance. This charge will only be provided by $i^p_{z,h}$, $h \in \{1,2,3,\ldots,\infty\}$; i.e., the in-phase fundamental and harmonic components of i_z, since the total charge provided by $i^q_{z,h}$, $h \in \{1,2,3,\ldots,\infty\}$ is always zero, owing to the odd symmetry of v_z, as explained in Section 2.4.2. Moreover, most of the charge will be provided by $i^p_{z,1}$.

3.4.1.1. Basic control scheme

Fig. 3.5 shows a first design proposal for a control scheme. This control scheme corrects the capacitor voltage unbalances by only modifying α_{zi1}, α_{zi3}, α_{zo1}, and α_{zo3} switching angles, while α_{zi2} and α_{zo2} are set to α_{z2}. Variables

$$\begin{aligned} y_{z2} &= v_{\mathrm{Cz1,filt}} - \frac{v_{\mathrm{Cz2,filt}} + v_{\mathrm{Cz3,filt}}}{2} \\ y_{z3} &= \frac{v_{\mathrm{Cz1,filt}} + v_{\mathrm{Cz2,filt}}}{2} - v_{\mathrm{Cz3,filt}} \end{aligned} \tag{3.7}$$

capture the unbalance between the two normalized partial dc-link voltages associated to inner dc-link points 2_z and 3_z, respectively. They are designated as unbalance variables. Also, it should be noted that such variables are computed with the capacitor-voltage filtered values ($v_{\mathrm{Cz}k\mathrm{,filt}}$, $k \in \{1,2,3\}$), obtained with transfer function matrix $\mathbf{H}_{\mathrm{filt}}(s) = \mathrm{diag}(H_{\mathrm{filt}}(s), H_{\mathrm{filt}}(s), H_{\mathrm{filt}}(s))$. Variables y^*_{z2} and y^*_{z3} indicate the command values, which are typically zero.

The difference between y^*_{zm} and y_{zm} ($m \in \{2,3\}$) defines error variable e_{zm}. A value $e_{z2} > 0$ means that v_{Cz1} is below its desired value and the average value among v_{Cz2} and v_{Cz3} is above its desired value. Therefore, a control action is needed that injects charge into 2_z in order to increase v_{Cz1} and decrease v_{Cz2} and v_{Cz3}; i.e., increase y_{z2}. The same principle is applied to inner dc-link point 3_z; i.e., if $e_{z3} > 0$, a control action is needed that injects charge into 3_z in order to increase v_{Cz1} and v_{Cz2} and decrease v_{Cz3}; i.e., increase y_{z3}.

Without loss of generality, let us assume that power is transferred from side a to side b. Then, any $e_{zm} \neq 0$ can be corrected by modifying the switching angles as described in Table 3.1. Control variables u_{zm}, generated by processing e_{zm} variables with compensators $\mathrm{G}_{zm}(s)$, are responsible of performing the required control action. Variables u_{z2} and u_{z3} modify switching angles α_{zi1}, α_{zi3}, α_{zo1}, and α_{zo3} in a per-unit basis from the value of the initial switching angles α_{z1} and α_{z3}. Switching angle α_{z2} can be computed with (3.6) in order to minimize the voltage unbalance and control effort that the controllers must perform.

Regarding compensators $\mathrm{G}_{zm}(s)$, the sign of $k_{\mathrm{P},zm}$ is subject to the same rationale discussed for the 3L-DAB (Section 2.4.1.1).

z	m	e_{zm}	Charge sign to provide	$\{\alpha_{zo1}, \alpha_{zi3}\}$	$\{\alpha_{zo3}, \alpha_{zi1}\}$
a	2	+ / –	+ / –	↓ / ↑	
	3	+ / –	+ / –		↑ / ↓
b	2	+ / –	+ / –	↑ / ↓	
	3	+ / –	+ / –		↓ / ↑

Table 3.1. Sign of the charge to be provided and switching angles change needed to correct a voltage unbalance at inner dc-link point m_z, depending on the sign of e_{zm} and according to Fig. 3.4.

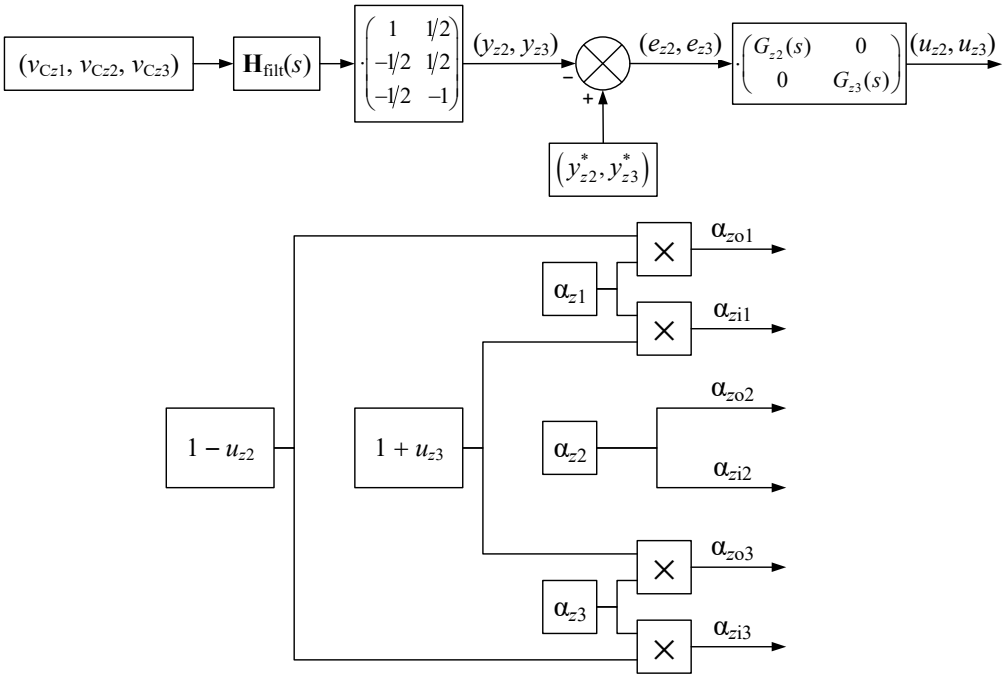


Fig. 3.5. Basic control scheme for the z-side capacitor voltage balancing.

3.4.1.2. Basic control scheme with decoupling

Let us assume that dc-link voltage V_Z is kept constant by means of a dc voltage source (with a series low resistance) connected across the dc link or, when a load is connected across the dc link, through a control loop that maintains V_Z constant by modifying φ. It is also assumed that all capacitors have the same capacitance and that switching angles α_{zk} remain constant during a switching period.

Considering the control scheme of Fig. 3.5, let us assume that in order to regulate y_{z2}, a control action u_{z2} is performed, which forces an injection of average current I_{2z} into inner dc-link point 2_z. As shown in Fig. 3.6, and with the assumptions previously described, current I_{2z} is distributed in two thirds flowing through the bottom capacitor and one third through the upper capacitors. Analogously, when u_{z3} is modified, an average current I_{3z} is injected into inner dc-link point 3_z, where one third of I_{3z} flows through the bottom capacitors and two thirds through the upper capacitor.

If it is considered that both currents are injected simultaneously, the capacitor voltages will vary

$$\begin{aligned}\Delta v_{Cz1} &= \frac{1}{s\cdot C_z}\cdot\left(\frac{2}{3}\cdot I_{2z}+\frac{1}{3}\cdot I_{3z}\right)\\ \Delta v_{Cz2} &= \frac{1}{s\cdot C_z}\cdot\left(-\frac{1}{3}\cdot I_{2z}+\frac{1}{3}\cdot I_{3z}\right)\\ \Delta v_{Cz3} &= \frac{1}{s\cdot C_z}\cdot\left(-\frac{1}{3}\cdot I_{2z}-\frac{2}{3}\cdot I_{3z}\right).\end{aligned} \tag{3.8}$$

The variation of the unbalance variables will be

$$\begin{aligned}\Delta y_{z2} &= \left(V_{Cz1}+\Delta v_{Cz1}-\frac{V_{Cz2}+\Delta v_{Cz2}+V_{Cz3}+\Delta v_{Cz3}}{2}\right)-\left(V_{Cz1}-\frac{V_{Cz2}+V_{Cz3}}{2}\right)\\ &= \frac{1}{s\cdot C_z}\cdot\left(I_{2z}+\frac{1}{2}\cdot I_{3z}\right)\\ \Delta y_{z3} &= \left(\frac{V_{Cz1}+\Delta v_{Cz1}+V_{Cz2}+\Delta v_{Cz2}}{2}-\left(V_{Cz3}+\Delta v_{Cz3}\right)\right)-\left(\frac{V_{Cz1}+V_{Cz2}}{2}-V_{Cz3}\right)\\ &= \frac{1}{s\cdot C_z}\cdot\left(\frac{1}{2}\cdot I_{2z}+I_{3z}\right).\end{aligned} \tag{3.9}$$

It can be observed that when the control loop related to inner point 2_z tries to correct an unbalance by modifying control variable u_{z2}, it also affects the unbalance of inner point 3_z, although in a smaller proportion. Because of the system symmetry, the control loop related to inner point 3_z will also affect both y_{z3} and y_{z2} in an analogous manner. It can be inferred that, although the control loops are decoupled, the plant is coupled, which may lead to a conflict between both control loops and cause a control inefficiency. Hence, a means to decouple the plant is convenient.

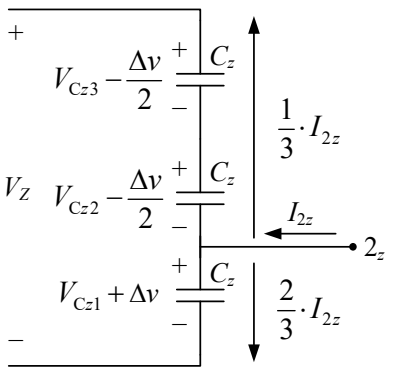


Fig. 3.6. Effect of current I_{2z} on the dc-link capacitor voltages when V_Z is kept constant.

The plant transfer function matrix can be defined as

$$\begin{pmatrix} y_{z2} \\ y_{z3} \end{pmatrix} = \frac{1}{C_z \cdot s} \cdot \mathbf{C_{4L}} \begin{pmatrix} I_{2z} \\ I_{3z} \end{pmatrix}, \tag{3.10}$$

where $\mathbf{C_{4L}}$ is the coupling matrix of the plant, which is derived from the analysis done in (3.9), and is equal to

$$\mathbf{C_{4L}} = \begin{pmatrix} 1 & 1/2 \\ 1/2 & 1 \end{pmatrix}. \tag{3.11}$$

However, having y_{zm} as a function of I_{mz} is not useful for the sake of the control decoupling analysis, since the outputs of the control scheme are u_{zm}. Therefore, the relation between I_{mz} and u_{zm} is needed. To ease the analysis, let us consider only the fundamental component of the transformer current. With the aid of Fig. 3.4, the average current provided to each inner dc-link point by $i_{z,1}$ during a switching cycle, can be computed as

$$\begin{aligned} I_{2z,1} &= \frac{1}{2\pi}\int_0^{2\pi} i_{2z,1}^{\mathrm{p}} = \frac{I_{z,1}^{\mathrm{p}}}{\pi}\left[\sin(\alpha_{zo2}) - \sin(\alpha_{zo1}) - \sin(\alpha_{zi3}) + \sin(\alpha_{zi2})\right] \\ I_{3z,1} &= \frac{1}{2\pi}\int_0^{2\pi} i_{3z,1}^{\mathrm{p}} = \frac{I_{z,1}^{\mathrm{p}}}{\pi}\left[\sin(\alpha_{zo3}) - \sin(\alpha_{zo2}) - \sin(\alpha_{zi2}) + \sin(\alpha_{zi1})\right]. \end{aligned} \tag{3.12}$$

Substituting the switching angles with its expressions defined in the control scheme of Fig. 3.5

$$\begin{aligned} I_{2z,1}(u_{z2}) &= \frac{I_{z,1}^{\mathrm{p}}}{\pi}\left[2\cdot\sin(\alpha_{z2}) - \sin(\alpha_{z1}\cdot(1-u_{z2})) - \sin(\alpha_{z3}\cdot(1-u_{z2}))\right] \\ I_{3z,1}(u_{z3}) &= \frac{I_{z,1}^{\mathrm{p}}}{\pi}\left[\sin(\alpha_{z3}\cdot(1+u_{z3})) + \sin(\alpha_{z1}\cdot(1+u_{z3})) - 2\cdot\sin(\alpha_{z2})\right]. \end{aligned} \tag{3.13}$$

As the control variables are inside sine functions, these expressions are nonlinear. Linearizing the expressions in (3.13) around $u_{zm} = 0$ results in

$$\begin{aligned} I_{2z,1}^{\mathrm{lin}}(u_{z2}) &= I_{2z,1}(0) + \left[\left.\frac{dI_{2z,1}}{du_{z2}}\right|_{u_{z2}=0}\right]\cdot u_{z2} = a_{4\mathrm{LB}}\cdot u_{z2} \\ I_{3z,1}^{\mathrm{lin}}(u_{z3}) &= I_{3z,1}(0) + \left[\left.\frac{dI_{3z,1}}{du_{z3}}\right|_{u_{z3}=0}\right]\cdot u_{z3} = a_{4\mathrm{LB}}\cdot u_{z3}, \end{aligned} \tag{3.14}$$

where

$$a_{4\mathrm{LB}} = \frac{I_{z,1}^{\mathrm{p}}}{\pi} \cdot \left[\alpha_{z1} \cdot \cos\left(\alpha_{z1}\right) + \alpha_{z3} \cdot \cos\left(\alpha_{z3}\right) \right], \tag{3.15}$$

switching angles are in radians, and $I_{2z,1}(0) = I_{3z,1}(0) = 0$ due to (3.6) being fulfilled for the sake of easing the capacitor voltage balancing.

Finally, the plant transfer function matrix, where the inputs are the control variables u_{zm} and the outputs are the unbalance variables y_{zm}, can be expressed as

$$\begin{pmatrix} y_{z2} \\ y_{z3} \end{pmatrix} = \frac{a_{4\mathrm{LB}}}{C_z \cdot s} \cdot \mathbf{C_{4L}} \begin{pmatrix} u_{z2} \\ u_{z3} \end{pmatrix}. \tag{3.16}$$

In order to decouple the plant, the control variables vector fed by the compensators has to be multiplied by the inverse of $\mathbf{C_{4L}}$, as demonstrated in [88], [89]. Then, the new controller-to-output plant transfer function becomes fully decoupled

$$\begin{pmatrix} y_{z2} \\ y_{z3} \end{pmatrix} = \frac{a_{4\mathrm{LB}}}{C_z \cdot s} \cdot \mathbf{C_{4L}} \cdot \mathbf{C_{4L}^{-1}} \begin{pmatrix} u'_{z2} \\ u'_{z3} \end{pmatrix} = \frac{a_{4\mathrm{LB}}}{C_z \cdot s} \cdot \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix} \begin{pmatrix} u'_{z2} \\ u'_{z3} \end{pmatrix}, \tag{3.17}$$

where

$$\mathbf{C_{4L}^{-1}} = \begin{pmatrix} 4/3 & -2/3 \\ -2/3 & 4/3 \end{pmatrix} \tag{3.18}$$

and u'_{zm} are the control variables outputted by the controller.

Consequently, the plant can be decoupled by introducing a decoupling matrix in the control scheme, which defines a new control scheme, shown in Fig. 3.7.

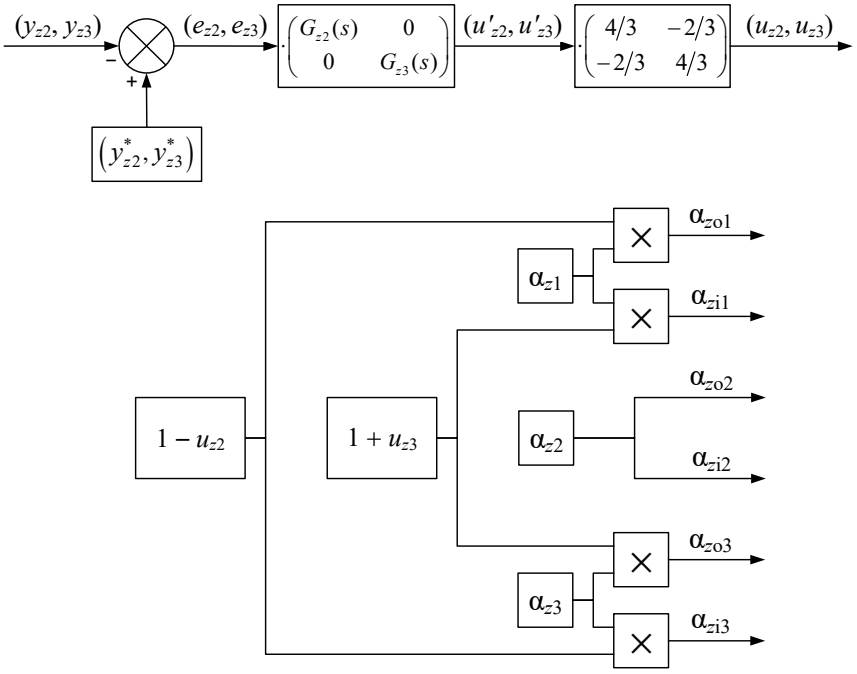


Fig. 3.7. Basic control scheme for the z-side capacitor voltage balancing with decoupling of the control loops that regulate y_{z2} and y_{z3}. The subscheme to compute y_{z2} and y_{z3} is the same of Fig. 3.5.

As a side note, the suitability of linearization performed to determine the coupling existing on the system transfer function is studied in Section 5.4.1.3.

3.4.1.3. Full control scheme

Fig. 3.8 shows an enhanced design of the control scheme proposed in Fig. 3.5. This control scheme takes advantage of all the available switching angles (α_{zi1}, α_{zi2}, α_{zi3}, α_{zo1}, α_{zo2}, and α_{zo3}) defined by the modulation, as opposed to the non-decoupled and decoupled basic control schemes of Fig. 3.5 and Fig. 3.7, respectively. Hence, it is named as full control scheme, as it employs all the DoF available to control the capacitor voltage balancing. Similar to Table 3.1, Table 3.2 shows how switching angles must be modified in order to correct any $e_{zm} \neq 0$ when power is transferred from side a to side b. In this case, all the available switching angles are taken into account.

z	*m*	e_{zm}	Charge sign to provide	{α_{zo1}, α_{zi3}}	{α_{zo2}, α_{zi2}}	{α_{zo3}, α_{zi1}}
a	2	+ / –	+ / –	↓ / ↑	↑ / ↓	
	3	+ / –	+ / –		↓ / ↑	↑ / ↓
b	2	+ / –	+ / –	↑ / ↓	↓ / ↑	
	3	+ / –	+ / –		↑ / ↓	↓ / ↑

Table 3.2. Sign of the charge to be provided and switching angles change needed to correct a voltage unbalance at inner dc-link point m_z, depending on the sign of e_{zm}, and according to Fig. 3.4.

Switching angles α_{zi1}, α_{zi3}, α_{zo1}, and α_{zo3} are modified using the same approach of the basic control scheme. Switching angles pair $\{\alpha_{zi2},\alpha_{zo2}\}$ modify the charge provided to both inner dc-link points simultaneously, as seen in Fig. 3.4 diagram and Table 3.2. This feature can be used to enhance the regulation of the unbalance variables by modifying α_{zi2} and α_{zo2} with the same control variables of the basic control scheme. Switching angles α_{zi2} and α_{zo2} can be defined according to Table 3.2, as

$$\alpha_{zi2} = \alpha_{zo2} = \alpha_{z2} \cdot \left(1 + u_{z2} - u_{z3}\right), \forall z. \tag{3.19}$$

Looking at Table 3.2, the most advantageous cases arise when $\text{sgn}(e_{z2}) \neq \text{sgn}(e_{z3})$, where the control must inject charge into 2_z and draw charge from 3_z, or draw charge from 2_z and inject charge into 3_z. In such cases, the resulting values of switching angles α_{zi2} and α_{zo2} given by (3.19), act in favor of correcting the voltage unbalance related to both inner dc-link points.

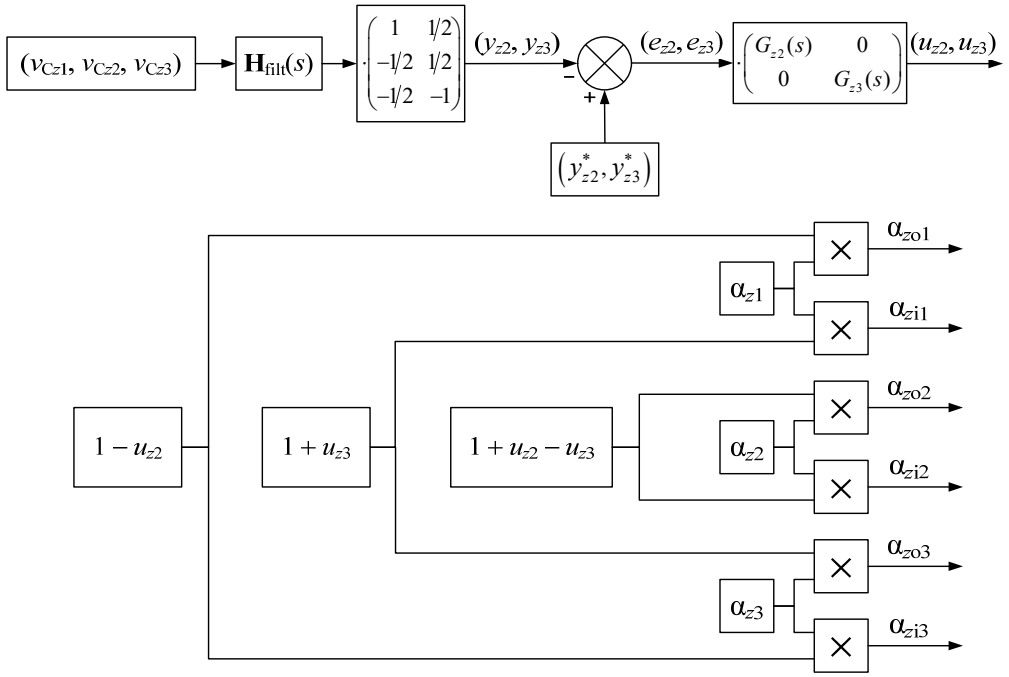


Fig. 3.8. Full control scheme for the z-side capacitor voltage balancing.

In the cases where $\text{sgn}(e_{z2}) = \text{sgn}(e_{z3})$, the control loops that regulate y_{z2} and y_{z3} act against each other when modifying α_{zi2} and α_{zo2} switching angles. The control loop with a bigger $|u_{zm}|$ value will turn the control action of $\{\alpha_{zi2},\alpha_{zo2}\}$ in its favor, while the other control loop (with a smaller $|u_{zm}|$ value) will be impaired by such control action. However, this impairment does not necessarily imply that the affected e_{zm} will grow away from zero during the transient. That is because switching angles pairs $\{\alpha_{zo1}, \alpha_{zi3}\}$ and $\{\alpha_{zo3}, \alpha_{zi1}\}$ (controlled independently by u_{z2} and u_{z3}, respectively) can counteract the adverse action of α_{zo2} or α_{zi2}.

Nevertheless, it can be noticed that the proposed full control scheme presents an additional degree of coupling with respect to the basic control scheme; The modification of α_{zi2} and α_{zo2} causes a coupling between the control loops regulating e_{z2} and e_{z3}. This coupling does not necessarily invalidate the control scheme of Fig. 3.8, but can be detrimental to its performance.

3.4.1.4. Full control scheme with decoupling

The full control scheme presented in Fig. 3.8 presents two degrees of coupling; First, the coupling described in Section 3.4.1.2, caused by the influence that the current provided to each inner dc-link point has among all the unbalance variables. Second, as described in Section 3.4.1.3, the coupling implicit in the full control scheme, where the regulation of y_{zm} with $\{\alpha_{zi2},\alpha_{zo2}\}$ alters simultaneously the charge provided to inner dc-link points 2_z and 3_z.

Therefore, as it has been done in Section 3.4.1.2, it is necessary to study the coupling matrix present in the transfer function, with the objective of finding a decoupling matrix. This decoupling matrix will allow having a control scheme where the control variables outputted by the controller (u'_{zm}) will only affect its corresponding unbalance variable; i.e., u'_{zm} will only affect y_{zm}.

For the present study, the same assumptions as in Section 3.4.1.2 are made; i.e., V_Z is kept constant, all capacitors are assumed to be of equal capacitance, and switching angles α_{zk} are considered to be constant during a switching cycle.

The plant transfer function, with I_{mz} as the inputs and y_{zm} as the outputs, is the same as the basic-control-scheme plant transfer function defined in (3.10), since the converter topology is the same. Considering only the fundamental component of i_z, currents $I_{mz,1}$ as a function of the control variables are defined as

$$\begin{aligned} I_{2z,1}\left(u_{z2},u_{z3}\right) &= \frac{I_{z,1}^{\mathrm{p}}}{\pi}\left[2\cdot\sin\left(\alpha_{z2}\cdot\left(1-u_{z3}+u_{z2}\right)\right)-\sin\left(\alpha_{z1}\cdot\left(1-u_{z2}\right)\right)-\sin\left(\alpha_{z3}\cdot\left(1-u_{z2}\right)\right)\right] \\ I_{3z,1}\left(u_{z2},u_{z3}\right) &= \frac{I_{z,1}^{\mathrm{p}}}{\pi}\left[\sin\left(\alpha_{z1}\cdot\left(1+u_{z3}\right)\right)+\sin\left(\alpha_{z1}\cdot\left(1+u_{z3}\right)\right)-2\cdot\sin\left(\alpha_{z2}\cdot\left(1-u_{z3}+u_{z2}\right)\right)\right] \end{aligned} \tag{3.20}$$

Following the same procedure of Section 3.4.1.2, let us linearize $I_{mz,1}(u_{z2},u_{z3})$ at $u_{zm} = 0$

$$
\begin{aligned}
I_{2z,1}^{\text{lin}}\left(u_{z2},u_{z3}\right) &= I_{2z,1}\left(0,0\right)+\left[\left.\frac{\partial I_{2z,1}}{\partial u_{z2}}\right|_{\substack{u_{z2}=0\\u_{z3}=0}}\right]\cdot u_{z2}+\left[\left.\frac{\partial I_{2z,1}}{\partial u_{z3}}\right|_{\substack{u_{z2}=0\\u_{z3}=0}}\right]\cdot u_{z3} \\
&= e_{4\text{LF}}\cdot\left[\left(a_{4\text{LF}}+b_{4\text{LF}}\right)\cdot u_{z2}-b_{4\text{LF}}\cdot u_{z3}\right] \\
I_{3z,1}^{\text{lin}}\left(u_{z2},u_{z3}\right) &= I_{3z,1}\left(0,0\right)+\left[\left.\frac{\partial I_{3z,1}}{\partial u_{z2}}\right|_{\substack{u_{z2}=0\\u_{z3}=0}}\right]\cdot u_{z2}+\left[\left.\frac{\partial I_{3z,1}}{\partial u_{z3}}\right|_{\substack{u_{z2}=0\\u_{z3}=0}}\right]\cdot u_{z3} \\
&= e_{4\text{LF}}\cdot\left[-b_{4\text{LF}}\cdot u_{z2}+\left(a_{4\text{LF}}+b_{4\text{LF}}\right)\cdot u_{z3}\right]
\end{aligned}
\tag{3.21}
$$

where

$$
\begin{aligned}
a_{4\text{LF}} &= \alpha_{z1}\cdot\cos\left(\alpha_{z1}\right)+\alpha_{z3}\cdot\cos\left(\alpha_{z3}\right) \\
b_{4\text{LF}} &= 2\alpha_{z2}\cdot\cos\left(\alpha_{z2}\right) \\
e_{4\text{LF}} &= \frac{I_{z,1}^{\text{p}}}{\pi},
\end{aligned}
\tag{3.22}
$$

switching angles are in radians, $I_{2z,1}(0,0) = I_{3z,1}(0,0) = 0$ due to (3.6) being fulfilled for the sake of easing the capacitor voltage balancing.

Finally, by substituting I_{mz} on (3.10) with $I^{\text{lin}}{}_{mz,1}$ in (3.21), the plant transfer function, where the inputs are control variables u_{zm} and the outputs are unbalance variables y_{zm}, can be obtained

$$
\begin{pmatrix} y_{z2} \\ y_{z3} \end{pmatrix} = \frac{e_{4\text{LF}}}{C_z\cdot s}\cdot\mathbf{E}_{4\text{L}}\begin{pmatrix} u_{z2} \\ u_{z3} \end{pmatrix}
\tag{3.23}
$$

where

$$
\mathbf{E}_{4\text{L}} = \mathbf{C}_{4\text{L}}\cdot\mathbf{D}_{4\text{L}} = \begin{pmatrix} 1 & 1/2 \\ 1/2 & 1 \end{pmatrix}\begin{pmatrix} a_{4\text{LF}}+b_{4\text{LF}} & -b_{4\text{LF}} \\ -b_{4\text{LF}} & a_{4\text{LF}}+b_{4\text{LF}} \end{pmatrix} = \begin{pmatrix} a_{4\text{LF}}-\dfrac{b_{4\text{LF}}}{2} & \dfrac{a_{4\text{LF}}-b_{4\text{LF}}}{2} \\ \dfrac{a_{4\text{LF}}-b_{4\text{LF}}}{2} & a_{4\text{LF}}-\dfrac{b_{4\text{LF}}}{2} \end{pmatrix},
\tag{3.24}
$$

$\mathbf{C}_{4\text{L}}$ is the coupling matrix due to the plant, and $\mathbf{D}_{4\text{L}}$ is the coupling matrix caused by the modification of α_{zo2} and α_{zi2}.

Hence, in order to decouple the plant, the control variables vector from the compensators (u'_{z2} and u'_{z3}) has to be multiplied by the inverse of coupling matrix $\mathbf{E}_{4\text{L}}$, defined as

$$\mathbf{E}_{4L}^{-1} = \frac{2}{3 \cdot a_{4LF}^2 + 6 \cdot a_{4LF} \cdot b_{4LF}} \cdot \begin{pmatrix} 2 \cdot a_{4LF} + b_{4LF} & b_{4LF} - a_{4LF} \\ b_{4LF} - a_{4LF} & 2 \cdot a_{4LF} + b_{4LF} \end{pmatrix} \tag{3.25}$$

Consequently, the plant can be decoupled by introducing a decoupling matrix in the control scheme, which defines a new control scheme, shown in Fig. 3.9.

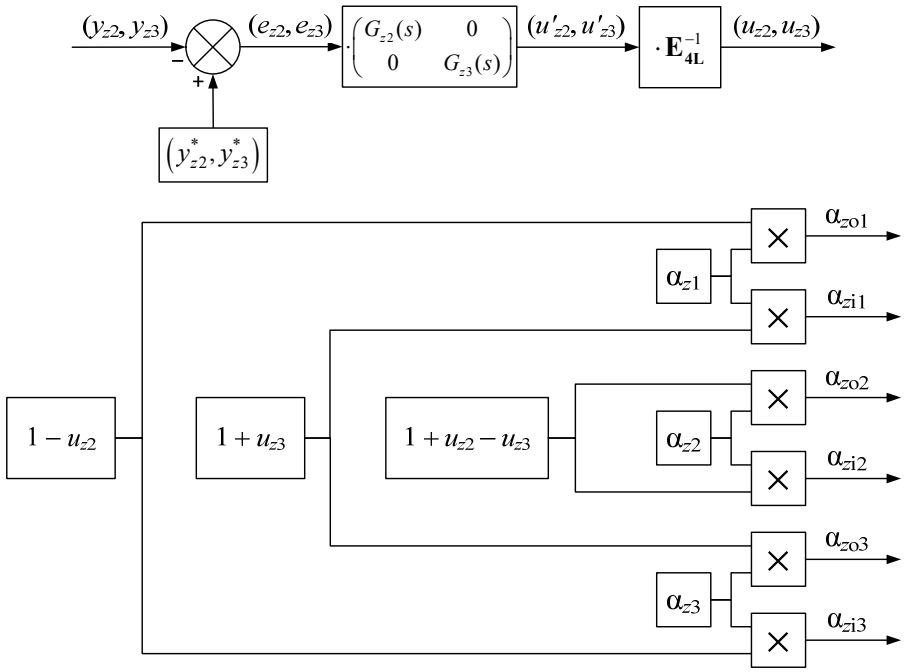


Fig. 3.9. Full control scheme for the z-side capacitor voltage balancing with decoupling of the plant and decoupling between u_{z2} and u_{z3}. The subscheme that computes y_{z2} and y_{z3} is the same of Fig. 3.5.

As a side note, the suitability of linearization performed to determine the coupling existing on the system transfer function is studied in Section 5.4.1.3.

3.5. Performance optimization

Following the same procedure as in the performance optimization study of the 3L-DAB (Section 2.5), this section proposes and solves a set of decoupled optimization problems, as a function of the available DoF, which are related to the 4L-DAB converter conduction and switching losses. Then, the results given by the optimization process are analyzed to find a common pattern, which can be defined by a set of simple and closed-form expressions, aiming to minimize the converter losses.

From the existing 13 DoF in the 4L-DAB, 5 DoF are available to force the desired power transfer and optimize the converter performance: α_{a1}, α_{a3}, α_{b1}, α_{b3}, and φ. It is assumed that legs a_1,

a_2, b_1, and b_2 are implemented using 4L MAC legs built upon MOSFET devices (Fig. 3.10). The legs are operated according to [66], which guarantees a blocking voltage of $V_Z/3$ on each switch if capacitor voltages are balanced, and that in each switching transition, switching losses are concentrated in a single device.

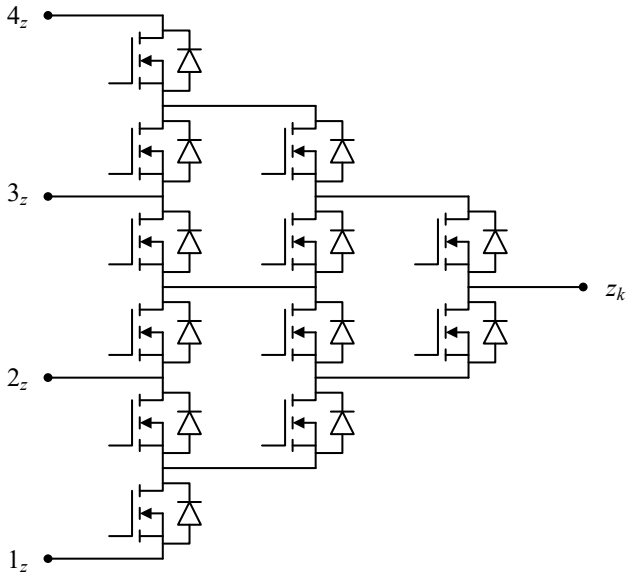


Fig. 3.10. MOSFET-based 4L MAC leg used to implement legs a_1, a_2, b_1, and b_2.

3.5.1. Objective functions

The objective functions to be optimized are the same as in the optimization process of the 3L-DAB, which are defined in Section 2.5. These functions are

$$\begin{aligned} F_1 &= I_{\mathrm{a,rms}} = \sqrt{\frac{1}{2}\cdot\sum_{h\ \mathrm{odd}}\left\|\mathbf{I}_{\mathrm{a},h}\right\|^2} \\ F_2 &= \sum_{T_\mathrm{s}}\left|I_{\mathrm{sw,I}}\right| + K\cdot\sum_{T_\mathrm{s}}\left|I_{\mathrm{sw,II}}\right| \\ F_3 &= \sum_{T_\mathrm{s}} I_{\mathrm{sw,I}}^2 + K\cdot\sum_{T_\mathrm{s}} I_{\mathrm{sw,II}}^2, \end{aligned} \tag{3.26}$$

where F_1 is related to the conduction losses and F_2 and F_3 are related to the switching losses. K is assumed to be 0.1 thorough the whole chapter.

3.5.2. Optimization process

Objective functions F_1, F_2, and F_3 are minimized independently using the numerical computation algorithms provided by MATLAB's Global Optimization Toolbox. The optimization problems are

$$\min\left(F_f\right) = F_f\left(X_f\right), \tag{3.27}$$

where $X_f = \{\alpha_{a1},\alpha_{a2},\alpha_{a3},\alpha_{b1},\alpha_{b2},\alpha_{b3},\varphi\}_f$ is F_f optimum solution at a given point defined by V_A^*, V_B^*, and P^*.

The constraint equations are

$$\begin{cases} 0° \le \alpha_{z1} \le \alpha_{z2} \le \alpha_{z3} \le 90° \\ 0° \le \varphi \le 90° \\ P = P^* \\ \int_{0°}^{360°} i_{mz} \cdot d\theta_z = 0. \end{cases} \qquad m \in \{2,3\},\ z \in \{a,b\} \tag{3.28}$$

It can be observed that the average current provided to each inner dc-link point within a switching cycle is forced to be null.

The optimum F_f switching angles are shown in Fig. 3.11. Comparing these results with the results of Fig. 2.12, it can be observed that switching angles $\{\alpha_{z1},\alpha_{z2}\}_f$ of the 3L-DAB optimum results are almost identical to $\{\alpha_{z1},\alpha_{z3}\}_f$ of the 4L-DAB optimum results.

Negative switching angles are not allowed by the constraints for the same reasons explained in the 3L-DAB optimization process (Section 2.5.3).

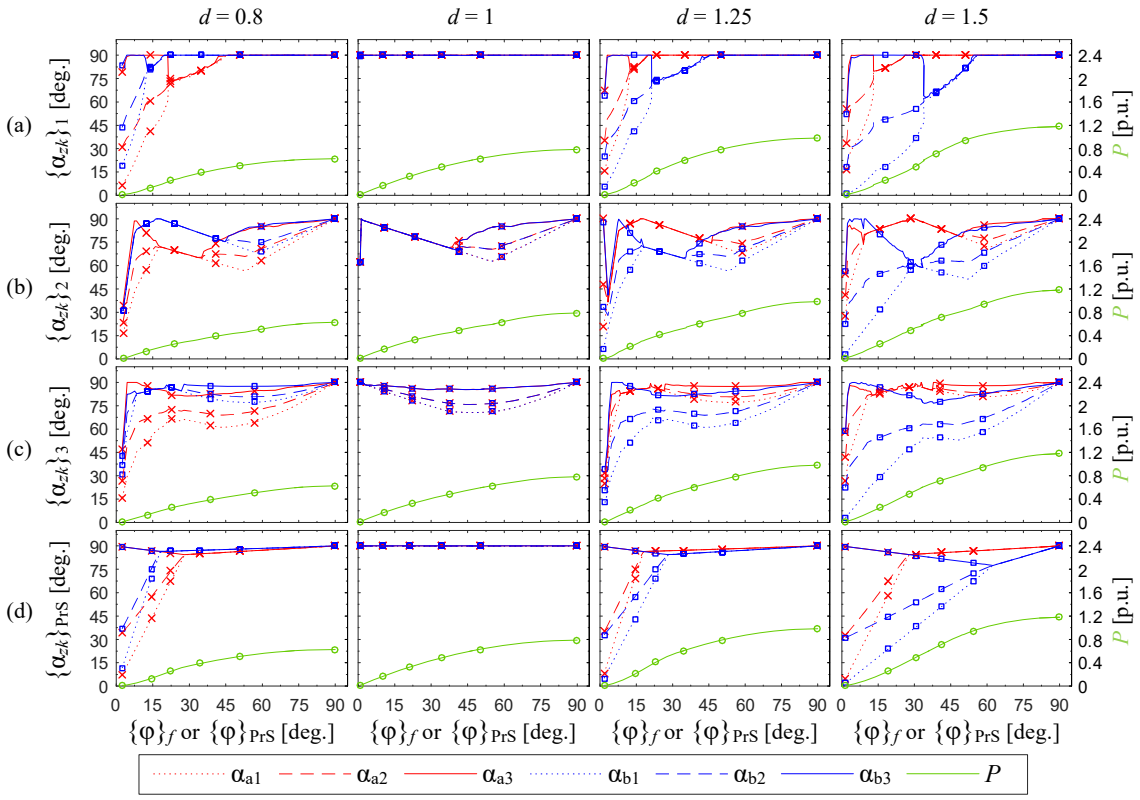


Fig. 3.11. Switching angle values (left axis on each subfigure) and transferred power (right axis) as a function of phase shift. (a) Solution that minimizes F_1. (b) Solution that minimizes F_2. (c) Solution that minimizes F_3. (d) Proposed practical solution.

3.5.3. Practical solution

The similarity between the optimum solutions computed for the 3L-DAB and the 4L-DAB, allows us to propose a practical solution for the 4L-DAB (Fig. 3.12) similar to the 3L-DAB practical solution. Particularly, switching angles α_{z1} and α_{z3} of the 4L-DAB practical solution will be equal to α_{z1} and α_{z2} of the 3L-DAB practical solution, respectively. Switching angle α_{z2} of the 4L-DAB practical solution is computed using (3.6). In summary,

$$\left\{\alpha_{z1}\right\}_{\mathrm{PrS}}=\begin{cases}0°+\dfrac{\alpha_{z,\mathrm{th}}}{\varphi_{z,\mathrm{th}}}\cdot\varphi, & \varphi<\varphi_{z,\mathrm{th}}\\ \alpha_{z,\mathrm{th}}+\dfrac{90°-\alpha_{z,\mathrm{th}}}{90°-\varphi_{z,\mathrm{th}}}\cdot\left(\varphi-\varphi_{z,\mathrm{th}}\right), & \varphi\geq\varphi_{z,\mathrm{th}}\end{cases}$$

$$\left\{\alpha_{z2}\right\}_{\mathrm{PrS}}=\arcsin\left(\frac{\sin\left(\alpha_{z1}\right)+\sin\left(\alpha_{z3}\right)}{2}\right), \tag{3.29}$$

$$\left\{\alpha_{z3}\right\}_{\mathrm{PrS}}=\begin{cases}90°-K_{\alpha,\mathrm{th}}\cdot\varphi, & \varphi<\varphi_{z,\mathrm{th}}\\ \alpha_{z,\mathrm{th}}+\dfrac{90°-\alpha_{z,\mathrm{th}}}{90°-\varphi_{z,\mathrm{th}}}\cdot\left(\varphi-\varphi_{z,\mathrm{th}}\right), & \varphi\geq\varphi_{z,\mathrm{th}}\end{cases}$$

As in the three-level case, the value of $\varphi_{z,\mathrm{th}}$ has to be limited to $\varphi_{\mathrm{th,max}} < 90^{\mathrm{o}}$ in order to guarantee the converter capability to transfer maximum power. This limitation will take place when d is outside the range defined in (2.22).

Fig. 3.11(d) presents the practical angle values for the following parameters values: $K_{\varphi,\mathrm{th}} = 50^{\mathrm{o}}$, $K_{\alpha,\mathrm{th}} = 0.2$, and $\varphi_{\mathrm{th,max}} = 80^{\mathrm{o}}$. These values provide a good approximation of the optimum solutions.

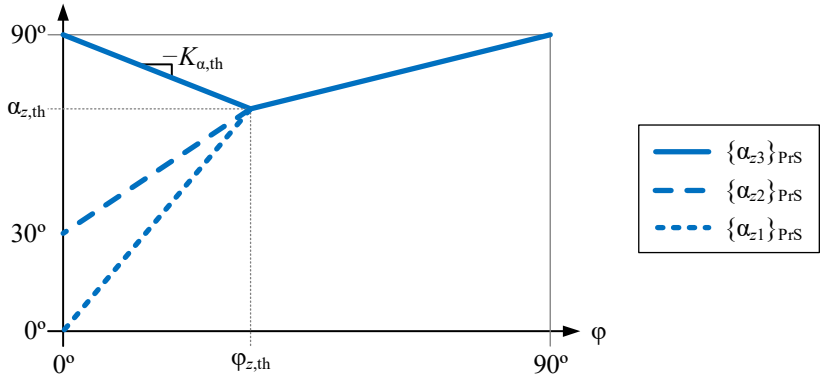


Fig. 3.12. Practical switching angles as a function of φ.

3.5.4. Comparison of the practical solution and F_1, F_2, and F_3 optimum solutions

Following the same procedure of the three-level case, to evaluate the suitability of the proposed practical solution, the value of the objective functions obtained with the practical solution, illustrated in Fig. 3.11(d) [$F_f(X_{\mathrm{PrS}})$], are compared with the objective function values given by the optimum results [$F_f(X_f)$], and with the objective function values obtained with the PSM in the present converter [$F_f(X_{\mathrm{PSM}})$]. These results are presented in Fig. 3.13 as a function of P. Solution X_{PSM} $\forall d$ is the same as the practical solution for $d = 1$, shown in Fig. 3.11(d). The base voltage, current, and power values are computed with (2.23).

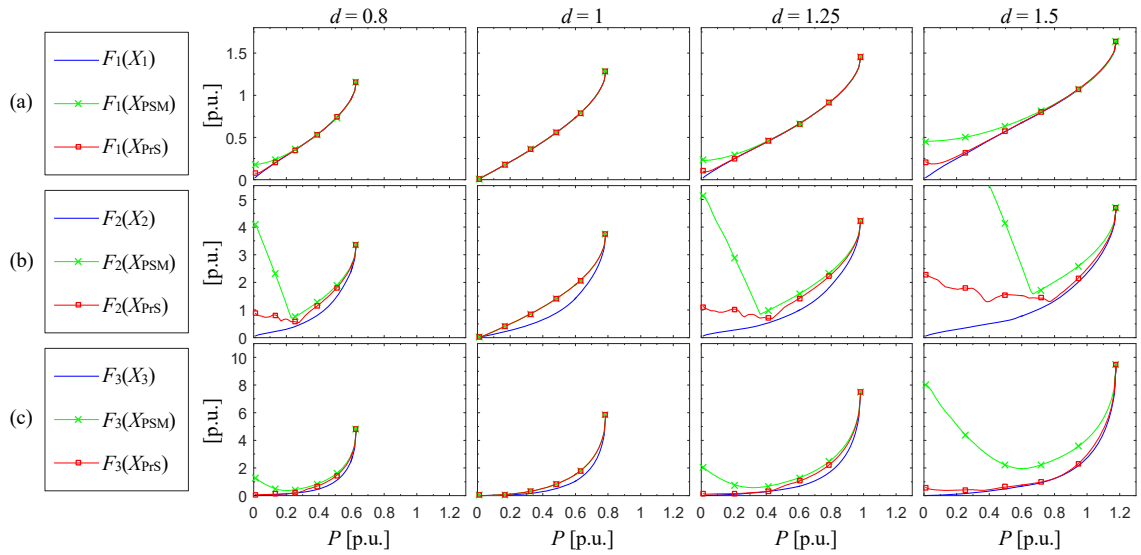


Fig. 3.13. Objective function values as a function of P for solutions X_f, X_{PrS}, and X_{PSM} (V_A = 1 p.u.). (a) F_1. (b) F_2. (c) F_3.

Since the 4L-DAB optimum results have similar patterns to the 3L-DAB optimum results, the values of its objective functions are also analogous. In fact, the values of F_1 for all X_f and X_{PrS} 4L-DAB solutions are practically identical (X_{PSM} is, in fact, identical) to its corresponding values on the 3L-DAB. On the other hand, F_2 and F_3 values are higher on all cases for the 4L-DAB solutions than for the 3L-DAB solutions, mainly because in the 4L-DAB four more switching transitions per switching cycle are performed.

In conclusion, the proposed practical solution is expected to achieve lower conduction and switching losses than PSM for low-to-medium powers when $d \neq 1$. Also, if in (3.26) I^2_{sw} influence is higher than $|I_{sw}|$ influence due to constructive parameters of the converter, then the switching losses will be very close to the minimum. At high powers and in all the power range for $d = 1$, both the practical and PSM solutions are close to or equal to the minimum possible conduction and switching losses.

3.6. Simulation and experimental results

Simulation and experimental tests have been carried out to demonstrate the effectiveness of the proposed 4L-DAB converter and capacitor-voltage-balancing controls. A MATLAB-Simulink lossless model of the converter in Fig. 3.1 is used to perform the simulations, where it is assumed $n = 1$, $C_z = 100$ µF, and $L = 300$ µH. The experimental tests are performed with the 4L-DAB converter prototype shown in Appendix A, Section A.1.2.

In all simulations and experiments, a dc voltage source with a low resistance (10 mΩ) in series is connected across the a-side dc-link and a resistive load (R_B) across the b-side dc-link.

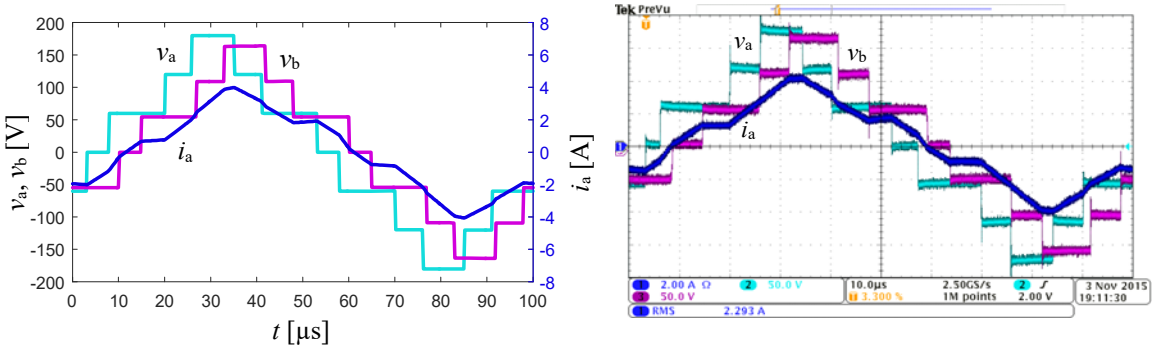
The non-decoupled basic capacitor-voltage-balancing control scheme (Fig. 3.5) is employed throughout the simulations and experimental tests, unless otherwise noted. Such control scheme is commanded by a proportional controller with $G_{am} = -G_{bm} = 0.6\ \forall m$, unless otherwise noted. Switching angles α_{zok} and α_{zik} values are limited by the algorithm presented in Appendix B. The low-pass-filter transfer function for the capacitor voltages is $H_{filt}(s) = 2\pi\cdot1000/(s + 2\pi\cdot1000)$.

The load voltage (V_B) is controlled by the regulator shown in Fig. 2.15, with $K_{PS} = 7500$, $f_{z,ps} = 50$ Hz, and $f_{p,ps} = 2500$ Hz. Reference value V_o^* is equal to the V_B defined in each working point. The output load resistor value (R_B) is adjusted so that the phase shift control settles on the desired φ and V_B defined in the working point.

All compensator parameters have been tuned through simulation and experiments to obtain an acceptable performance and stable behavior.

3.6.1. Steady-state results

Fig. 3.14 presents the simulation and experimental results for the relevant voltage and current waveforms. It can be observed that, in the simulation and experimental tests, a-side and b-side dc-links have capacitor voltage balance, since both v_a and v_b present voltage steps of equal magnitude.



(a) (b)

Fig. 3.14. Waveforms v_a, v_b, and i_a, in steady state with the capacitor-voltage-balancing control enabled on both sides. Conditions and parameter values: $f_s = 10$ kHz, $V_A = 180$ V, $V_B = 160$ V, $R_B = 132\ \Omega$, $\varphi \approx 25°$, $\{\alpha_{z1},\alpha_{z2},\alpha_{z3}\} = \{15°,37.76°,75°\}\ \forall z$, and $\Delta\alpha_{z,min} = 2.52°\ \forall z$ ($t_{b,z} = 700$ ns $\forall z$) (a) Simulation results. (b) Experimental results.

3.6.2. Transient results

The transient results help to analyze the behavior, performance, and suitability of the proposed control schemes.

A first set of tests, with simulation and experimental results, is presented in Fig. 3.15. In these tests, the same control scheme and controller from the steady-state results is employed. An initial unbalance in v_{Cb1}, v_{Cb2}, and v_{Cb3} is forced, disabling the b-side capacitor-voltage-balancing control and loading the b-side capacitors with three different resistance values. Once the b-side balancing control is enabled, the capacitor voltage balance is quickly recovered in both the simulation and experimental tests.

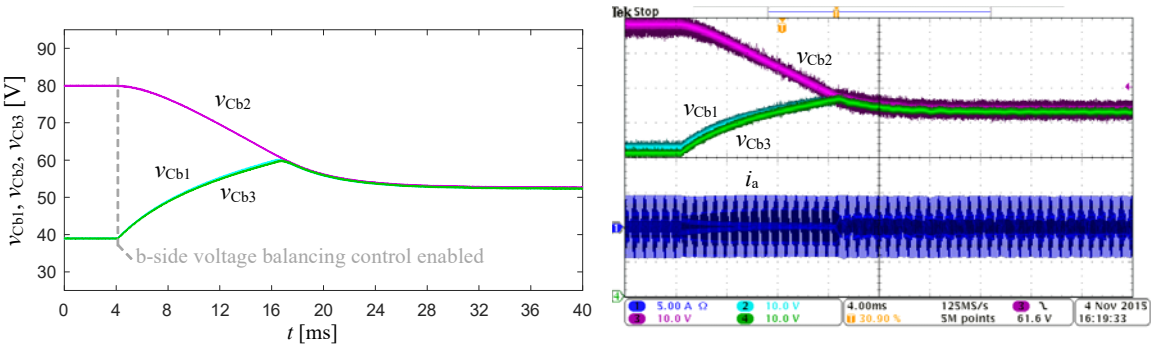


Fig. 3.15. Waveforms v_{Cb1}, v_{Cb2}, v_{Cb3}, and i_a under a b-side capacitor-voltage-balancing transient. The a-side capacitor-voltage-balancing control is all the time enabled, guaranteeing a-side capacitor voltage balancing. The b-side capacitor-voltage-balancing control is enabled at t = 4 ms. Conditions: f_s = 10 kHz, V_A = 180 V, V_B = 160 V, R_B = 132 Ω, $\varphi \approx 25°$, $\{\alpha_{z1},\alpha_{z2},\alpha_{z3}\} = \{15°,37.76°,75°\}$ $\forall z$, and $\Delta\alpha_{z,min} = 2.52°$ $\forall z$ ($t_{b,z}$ = 700 ns $\forall z$) (a) Simulation results. (b) Experimental results.

A second set of tests, with simulation results only, consist on performing a deliberate unbalance (starting from a balanced state) of the a-side dc-link capacitor voltages, by assigning a non-zero value to one of the unbalance commands (y^*_{a3}). After reaching a steady state, a second transient is performed by assigning $y^*_{a3} = 0$. Such test eases the analysis of the proposed non-decoupled and decoupled control schemes performance.

The capacitor-voltage-balancing control schemes are commanded by (2.14) PI controller. To fulfill the assumptions considered in the design of the decoupled control scheme, the chosen $k_{P,am}$ and $T_{I,am}$ $\forall m$ values guarantee that the switching angle values during the transient tests do not get limited by 90º, 0º, or by an adjacent switching angle, and the values of α_{zk} guarantee a null charge provided to the inner dc-link points by $i_{z,1}$ when $u_{zm} = 0$ $\forall m$.

Fig. 3.16 shows the simulations results when employing the non-decoupled basic control scheme and the decoupled basic control scheme. Fig. 3.17 shows the simulation results for the non-decoupled full control scheme and for the decoupled full control scheme. In Fig. 3.16 and Fig. 3.17, dark red and dark blue colors are associated to the variables involved in the regulation of inner dc-link points 2_a and 3_a voltages, respectively. Dark green color is associated to the switching angles involved in the simultaneous regulation of both inner dc-link point voltages.

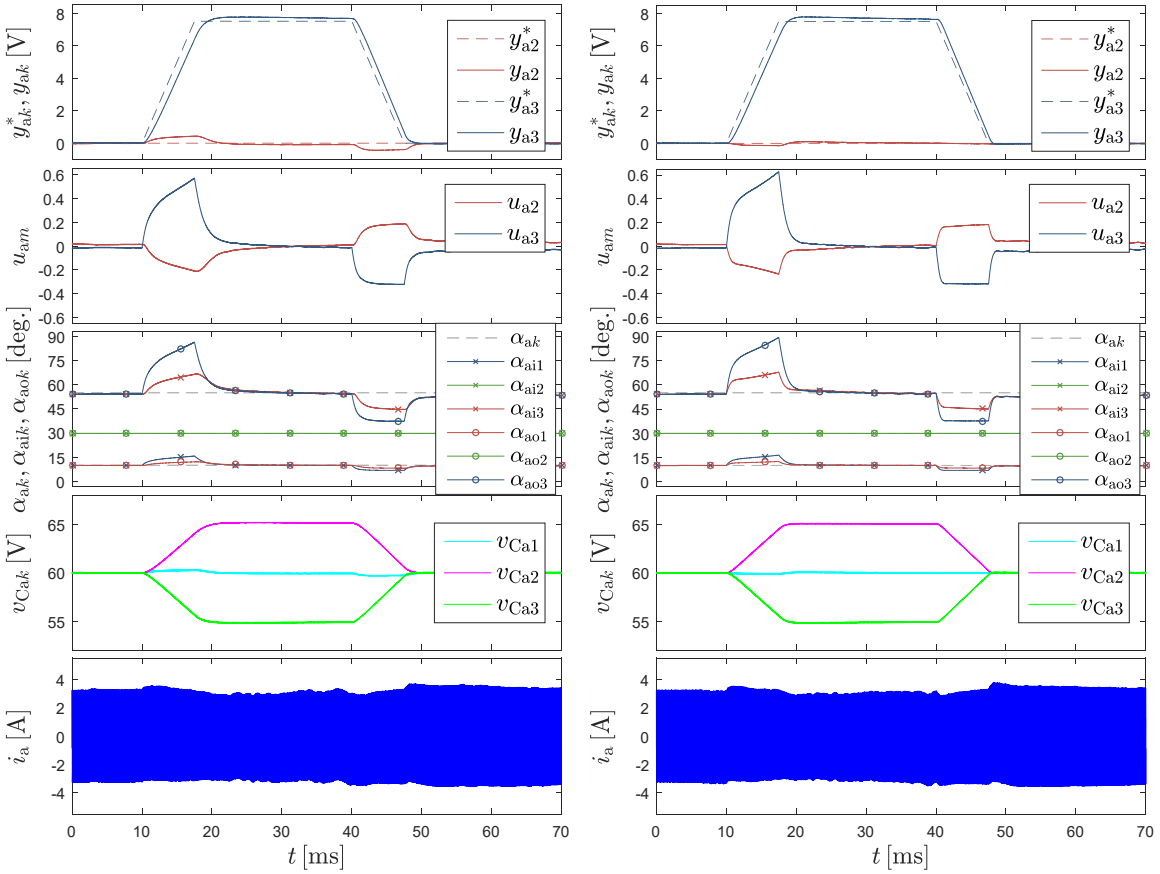
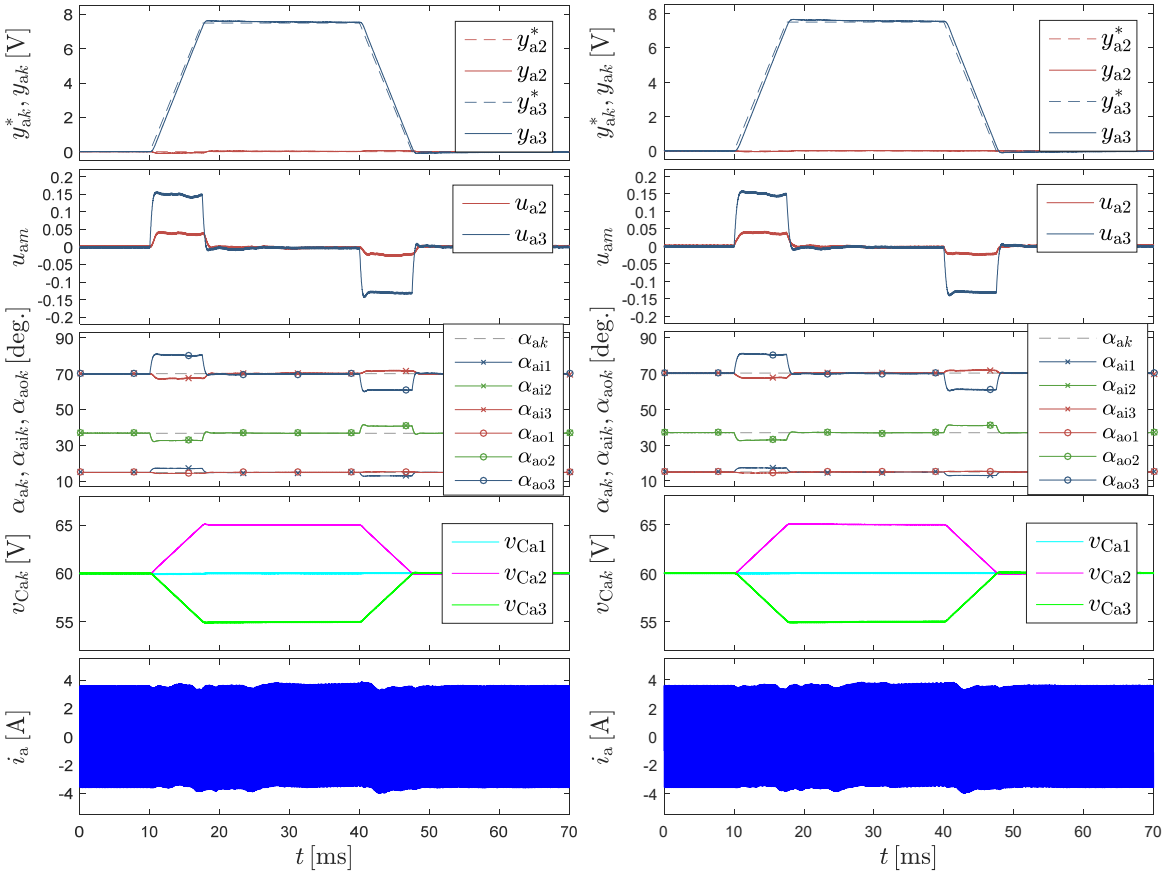


Fig. 3.16. Simulation results under ramp variations (±1 V/ms) of y^*_{a3} from 0 V to 7.5 V and vice versa. Conditions: f_s = 20 kHz, V_A = 180 V, V_B = 120 V, R_B = 145 Ω, $\varphi \approx 60°$, $\{\alpha_{z1},\alpha_{z2},\alpha_{z3}\} = \{10°,29.76°,55°\}$ $\forall z$, and a PI compensator with $k_{P,am} = -k_{P,bm} = 0.4$ and $T_{I,zm} = 20$ ms $\forall z,m$. (a) Results when employing the non-decoupled basic control scheme. (b) Results when employing the decoupled basic control scheme.

It can be observed that when employing the non-decoupled basic control scheme [Fig. 3.16(a)], y_{a2} is altered when y_{a3} is being regulated due to the existing plant coupling explained in Section 3.4.1.2. Control loop regulating y_{a2}, corrects such alteration a short after y_{a3} regulation begins. The alteration of y_{a2} could be worse if unfavorable conditions are met, such as when using a weak compensator ($k_{P,a2}$ smaller and/or $T_{I,a2}$ larger).

On the other hand, when the control with decoupling is employed [Fig. 3.16(b)], the induced alteration in y_{a2} is greatly diminished. With such control scheme, the decoupling is performed by letting y_{a3} control loop modify u_{a2} and u_{a3}, in order to counteract the induced alteration of y_{a2} and regulating y_{a3} (its main duty), respectively. The simultaneous modification of the control variables can be observed in Fig. 3.16(b), where u_{a2} and u_{a3} begin its modification at the same time.



(a) (b)

Fig. 3.17. Simulation results under the same conditions of Fig. 3.16 except for the switching angles, where $\{\alpha_{z1},\alpha_{z2},\alpha_{z3}\} = \{15°,36.82°,70°\}$ $\forall z$ and $R_B = 100\ \Omega$. (a) Results when employing the non-decoupled full control scheme of Fig. 3.8. (b) Results when employing the decoupled full control scheme of Fig. 3.9.

Fig. 3.17 shows the simulation results when employing the full control scheme with and without decoupling. When comparing these results with the basic control scheme results, it is patent that the full control scheme performs better (y_{a3} follows y^*_{a3} with a smaller stationary error) and regulates the unbalance variables with less control effort (u_{a2} and u_{a3} reach smaller maximum values).

Moreover, when employing the non-decoupled full control scheme [Fig. 3.17(a)], y_{a2} control loop is able to correct promptly the y_{a2} alteration, induced by the coupling issues explained in Section

3.4.1.2 and Section 3.4.1.4. Furthermore, such correction is accomplished with a performance similar to the one showed by the decoupled full control scheme [Fig. 3.17(b)].

Section 6.3.2 shows further simulation and experimental transient results employing the four proposed capacitor-voltage-balancing control schemes. The similarity between simulation and experimental results is confirmed.

3.7. Conclusion

This chapter has explored the possibility of implementing DAB dc-dc converters employing 4L-NPC legs. A suitable modulation strategy and two capacitor-voltage-balancing control schemes have been defined. A thorough analysis has revealed two coupling mechanisms that affect the regulation of each inner dc-link point voltage. As a result, a decoupled version of each control scheme has been proposed. Simulation and experimental results demonstrate the feasibility of such 4L-DAB dc-dc converter with the proposed modulation and the basic capacitor-voltage-balancing control scheme. Simulation results demonstrate the feasibility of the proposed decoupled capacitor-voltage-balancing basic and full control schemes. The system presents thirteen DoF. Eight of these DoF are used to guarantee capacitor voltage balancing and the remaining five DoF are used to control the power flow between both converter sides and improve the converter performance. The pattern defined by $\{\alpha_{a1}, \alpha_{a2}, \alpha_{a3}, \alpha_{b1}, \alpha_{b2}, \alpha_{b3}, \varphi\}$ optimum values has been explored through the analysis of three decoupled optimization problems, related with the converter conduction and switching losses. Finally, simple and practical closed-form expressions of these modulation parameters have been provided, representing this modulation a good trade-off between pattern simplicity and accuracy of approximation to the three individual optimum solutions. Moreover, the proposed practical solution offers greater converter performance when compared with the conventional PSM.

The proposed 4L-DAB topology presents several advantages compared to DAB topologies with two or three levels; namely, an increase in the total dc-link voltage for a given converter power rating and semiconductor-device voltage rating, resulting in better efficiency values, the possibility of using lower-voltage-rated semiconductor devices with better performance figures for a given dc-link voltage, lower converter losses, better converter loss distribution, and lower transformer-current harmonic distortion, which leads to lower magnetic losses.

CHAPTER 4.

STUDY OF A FIVE-LEVEL NEUTRAL-POINT-CLAMPED DUAL-ACTIVE-BRIDGE DC-DC CONVERTER

Abstract — This chapter presents the study of a five-level NPC DAB dc-dc converter. First, a general modulation pattern is defined, the dc-link capacitor voltage balancing is analyzed in detail, and proper balancing control schemes are designed. Then, a simple and practical specific modulation strategy is provided, resembling the practical modulation proposed for the three-level and four-level cases. The good performance of the proposed five-level NPC DAB converter operated with the proposed modulation strategy and capacitor-voltage-balancing control is verified through simulation.

4.1. Introduction

This chapter introduces a DAB dc-dc converter built upon four five-level (5L) NPC legs. A proper modulation strategy is proposed and characterized. The dc-link capacitor voltage balancing is analyzed and closed-loop capacitor-voltage-balancing control schemes are proposed. The modulation parameter values are determined with a set of simple and practical equations, based on the solutions proposed for the three-level and four-level case. Finally, simulation results are presented to verify the good performance of the proposed capacitor-voltage-balancing controls.

This chapter is organized as follows. Section 4.2 presents the converter topology. Section 4.3 presents the fundamentals of the modulation strategy. Section 4.4 presents the study of the capacitor voltage balancing and defines proper control schemes. Section 4.5 proposes a practical solution for the modulation strategy. Section 4.6 presents the simulation results to verify the modulation and control performance. Finally, Section 4.7 outlines the conclusions.

4.2. Topology

Fig. 4.1 presents the proposed five-level NPC DAB dc-dc converter (5L-DAB) topology, which is an extension to five levels of the 4L-DAB. In the 5L-DAB, each side dc-link has five voltage levels, with connection points 1_z, 2_z, 3_z, 4_z, and 5_z, and two five-level NPC legs (z_1 and z_2).

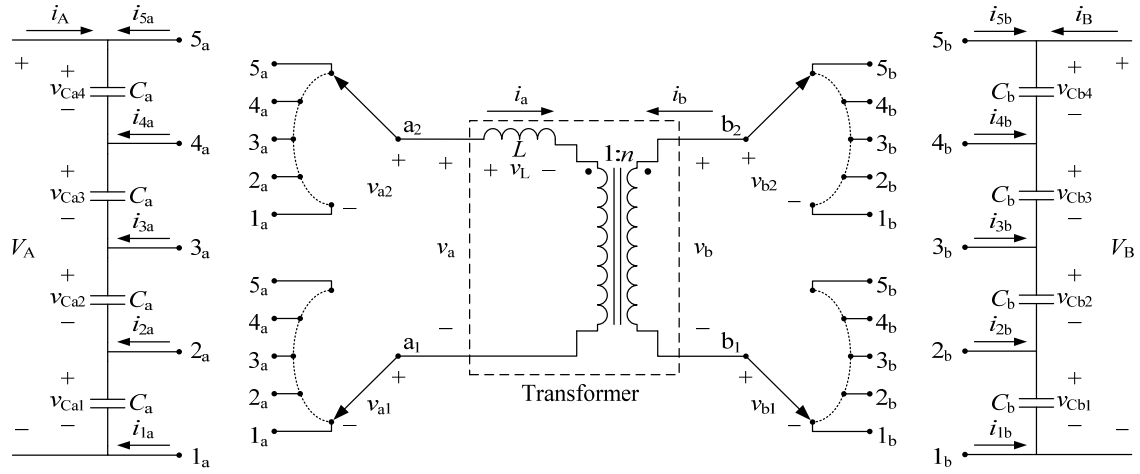


Fig. 4.1. Topology of the proposed 5L-DAB dc-dc converter with phase legs a_1, a_2, b_1, and b_2 depicted as single-pole quintuple-throw switches.

4.3. Modulation

Fig. 4.2 presents the modulation pattern for the 5L-DAB. The two five-level legs on side z are controlled to produce the five-level staircase waveforms v_{z1} and v_{z2}, so as to synthesize a v_z transformer voltage waveform with nine voltage levels (four more than the 3L-DAB and two more than the 4L-DAB). The 5L-DAB a-side switching-state sequence is shown on top of Fig. 4.2. The b-side switching-state sequence follows the same pattern.

The dwell times of the 5L-DAB z-side switching states can be defined by eight independent switching angles; i.e., α_{zi1}, α_{zi2}, α_{zi3}, α_{zi4}, α_{zo1}, α_{zo2}, α_{zo3}, and α_{zo4}, with

$$\begin{aligned} &-90° \le \alpha_{zi1} \le \alpha_{zi2} \le \alpha_{zi3} \le \alpha_{zi4} \le 90° \\ &-90° \le \alpha_{zo1} \le \alpha_{zo2} \le \alpha_{zo3} \le \alpha_{zo4} \le 90°. \end{aligned} \tag{4.1}$$

As in the 3L-DAB and 4L-DAB, the present modulation allows maintaining $\overline{v}_z = 0, \forall z,$ which guarantees the nonexistence of a transformer steady-state dc current and prevents the saturation of the transformer core, even when the dc-link capacitor voltages are not balanced. It also forces a symmetrical operation of both z-side full-bridge legs, as well as guaranteeing odd symmetry in v_a, v_b, v_L, and i_a waveforms, which is convenient for the capacitor voltage balancing.

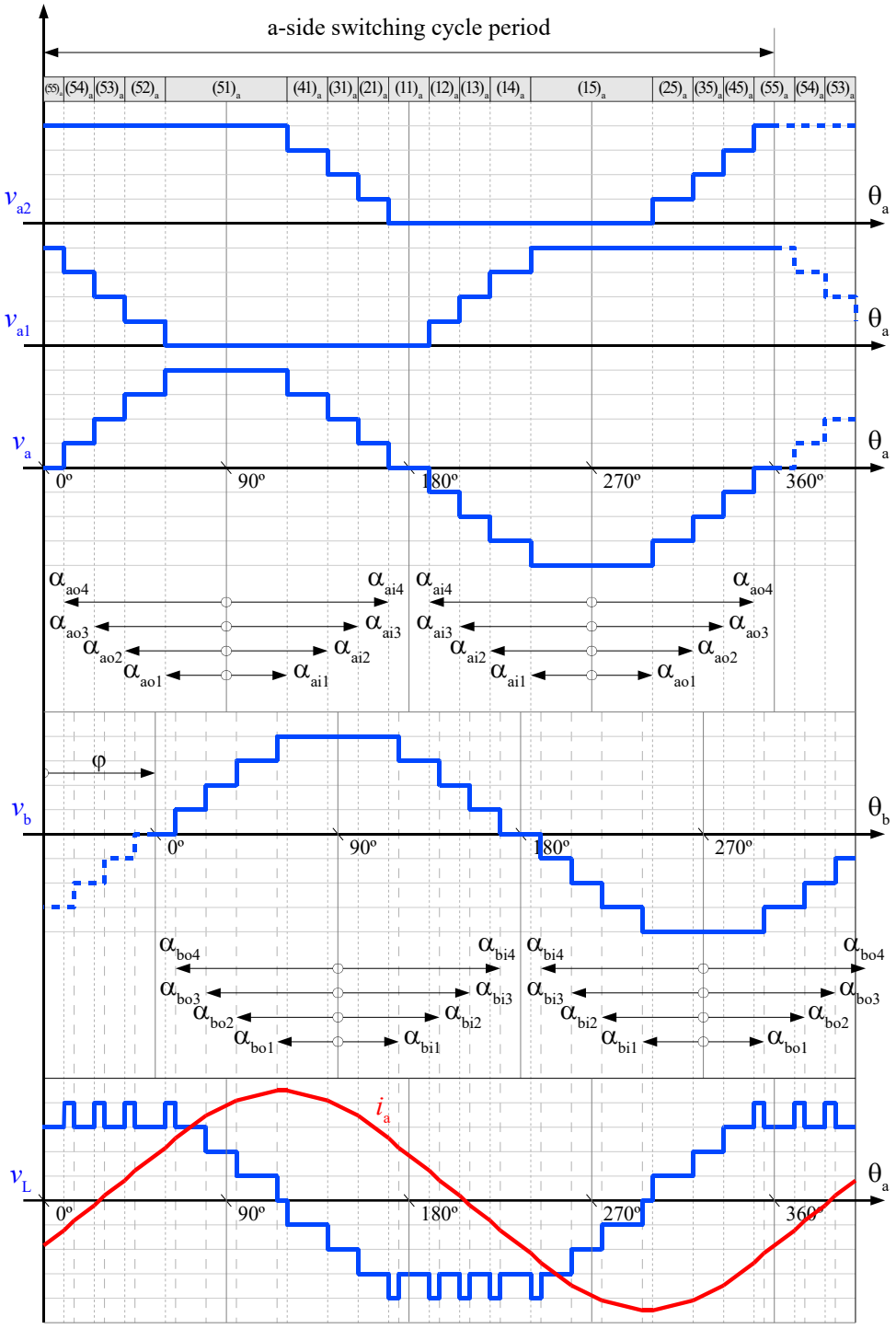


Fig. 4.2. Voltage waveforms v_{a1}, v_{a2}, v_a, v_b, and v_L, and current i_a for the proposed five-level modulation. Switching states for a-side are shown on top of the figure. All waveforms are plotted assuming $V_A = V_B/n$.

The eight switching angles per side (α_{zi1}, α_{zi2}, α_{zi3}, α_{zi4}, α_{zo1}, α_{zo2}, α_{zo3}, and α_{zo4}) plus the phase shift (φ), make a total of 17 DoF available to control the capacitor voltage balancing, the converter performance, and the power flow. If

$$\begin{aligned}\alpha_{zo1} &= \alpha_{zi1} = \alpha_{z1}\\ \alpha_{zo2} &= \alpha_{zi2} = \alpha_{z2}\\ \alpha_{zo3} &= \alpha_{zi3} = \alpha_{z3}\\ \alpha_{zo4} &= \alpha_{zi4} = \alpha_{z4}\end{aligned} \tag{4.2}$$

and the dc-link capacitor voltages are balanced, then quarter-wave symmetry is guaranteed and even-order harmonics are eliminated in v_a, v_b, v_L, and i_a waveforms.

4.4. Capacitor voltage balancing

As in the 3L-DAB and 4L-DAB cases, the 5L-DAB dc-dc converter also requires a means to guarantee the dc-link capacitor voltages balance, since these voltages naturally collapse or increase above the desired value. This phenomenon can be observed in the simulation results shown in Fig. 4.3(a). These results show the capacitor voltages transient response under an initial balanced state, with an arbitrary set of switching angles setting equal-value dwell times in v_a and v_b waveforms, and under the absence of a closed-loop control. After 80 ms, the transient reaches a steady state where the capacitor voltages have reached unacceptable levels, which could destroy the devices due to an excessive blocking voltage, besides leading to nonoptimal operating conditions. Therefore, a means to guarantee the capacitor voltage balancing is required.

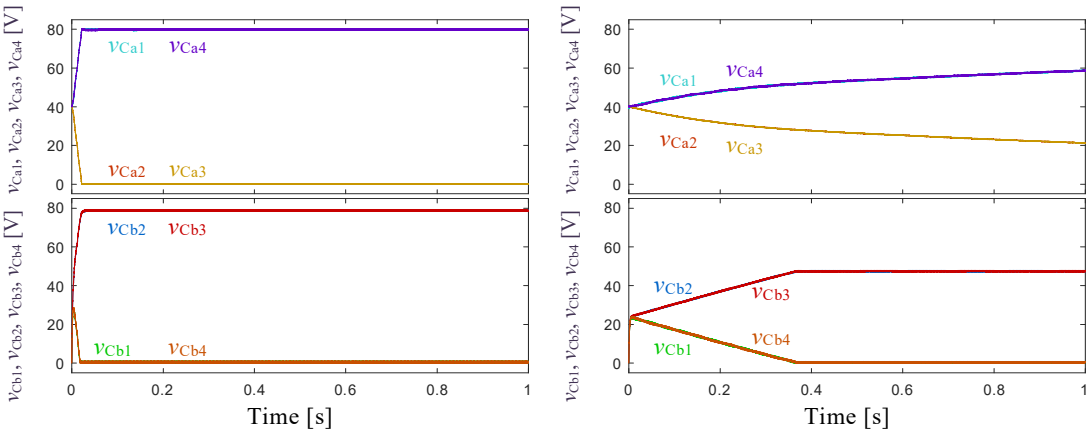


Fig. 4.3. Simulation results of a transient in the capacitor voltages during converter operation, under the following conditions: V_A = 160 V, C_z = 100 μF, φ = 60°. A resistor load (R_B) is present across the b-side output and its value is selected in order to set $V_B \approx 160$ V. (a) Simulation with arbitrary switching angles $\{\alpha_{z1},\alpha_{z2},\alpha_{z3},\alpha_{z4}\} = \{11.25°,33.75°,56.25°,78.75°\}$ ∀z and R_B = 65.4 Ω. (b) Simulation with $\{\alpha_{z1},\alpha_{z2},\alpha_{z3},\alpha_{z4}\} = \{10°,26.4°,45.6°,80°\}$ ∀z, and R_B = 47.9 Ω. Switching angles α_{z2} and α_{z3} are computed with (4.6) and (4.19) in order to lessen the capacitor voltage unbalance on both sides.

4.4.1. Control operating principle and control schemes

The currents injected into or drawn from the inner points of the dc-link (2_z, 3_z, 4_z) alter the ratio between the four dc-link capacitor voltages. These currents are

$$\begin{aligned} i_{2z} &= S_{z12} \cdot i_z - S_{z22} \cdot i_z \\ i_{3z} &= S_{z13} \cdot i_z - S_{z23} \cdot i_z \\ i_{4z} &= S_{z14} \cdot i_z - S_{z24} \cdot i_z, \end{aligned} \tag{4.3}$$

where S_{zj2}, S_{zj3}, and S_{zj4} are equal to 1 when leg z_j is connected to inner dc-link point 2_z, 3_z, and 4_z, respectively, and 0 otherwise.

Following the same procedure as in the three-level and four-level cases (Section 2.4.1 and Section 3.4.1, respectively), let us consider only the effect of the fundamental component of i_z ($i_{z,1}$), as its amplitude is greater than each i_z harmonic amplitudes. Current $i_{z,1}$ can be decoupled into $i^{p}_{z,1}$ component, in phase with $v_{z,1}$, and into a $i^{q}_{z,1}$ component, in quadrature with $v_{z,1}$.

Currents $i^{p}_{z,1}$ and $i^{q}_{z,1}$ are depicted in Fig. 4.4, together with v_z. The shaded areas in Fig. 4.4 represent the electrical charge injected into (positive sign) or drawn from (negative sign) the z-side inner dc-link points 2_z (red areas), 3_z (blue areas), and 4_z (green areas) by these currents. To keep a preexisting capacitor voltage balance, the sum of the red areas must be zero, the sum of the blue areas must be zero, and the sum of the green areas must also be zero. As in the previous cases, the sum of $i^{q}_{z,1}$ areas for each color is always zero, thanks to v_z odd symmetry. Therefore, to keep a preexisting capacitor voltage balance, it is only necessary to cancel the areas of $i^{p}_{z,1}$ for each color, or in other words, the charge provided by $i^{p}_{z,1}$ to each inner dc-link point within a switching cycle must be zero. To simplify, and thanks to the even symmetry of $i^{p}_{z,1}$ shaded areas along the switching period, let us only consider half of the switching period shown in Fig. 4.4. The per-unit charge provided to each inner dc-link point by $i^{p}_{z,1}$ during this period is

$$\begin{aligned} q_{2z} &= \sin\left(\alpha_{zo2}\right) - \sin\left(\alpha_{zo1}\right) - \left(\sin\left(\alpha_{zi4}\right) - \sin\left(\alpha_{zi3}\right)\right) \\ q_{3z} &= \sin\left(\alpha_{zo3}\right) - \sin\left(\alpha_{zo2}\right) - \left(\sin\left(\alpha_{zi3}\right) - \sin\left(\alpha_{zi2}\right)\right) \\ q_{4z} &= \sin\left(\alpha_{zo4}\right) - \sin\left(\alpha_{zo3}\right) - \left(\sin\left(\alpha_{zi2}\right) - \sin\left(\alpha_{zi1}\right)\right). \end{aligned} \tag{4.4}$$

If (4.2) is assumed for simplicity, then $q_{3z} = 0$ and $q_{2z} = -q_{4z}$. Forcing $q_{2z} = -q_{4z} = 0$ results in

$$\sin\left(\alpha_{z1}\right) - \sin\left(\alpha_{z2}\right) - \sin\left(\alpha_{z3}\right) + \sin\left(\alpha_{z4}\right) = 0. \tag{4.5}$$

One solution of (4.5) is to force

$$\begin{aligned}\sin(\alpha_{z2}) &= \sin(\alpha_{z1}) + \Delta_{z1} \\ \sin(\alpha_{z3}) &= \sin(\alpha_{z4}) - \Delta_{z1},\end{aligned} \tag{4.6}$$

where, to meet (4.1), it must be verified that

$$0 \le \Delta_{z1} \le \frac{\sin(\alpha_{z4}) - \sin(\alpha_{z1})}{2}. \tag{4.7}$$

However, as it happens in the previous cases, when considering all i_z harmonics, as well as converter non-idealities, verifying (4.5) is not enough to maintain a preexisting capacitor voltage balance, as demonstrated in the simulation results of Fig. 4.3(b).

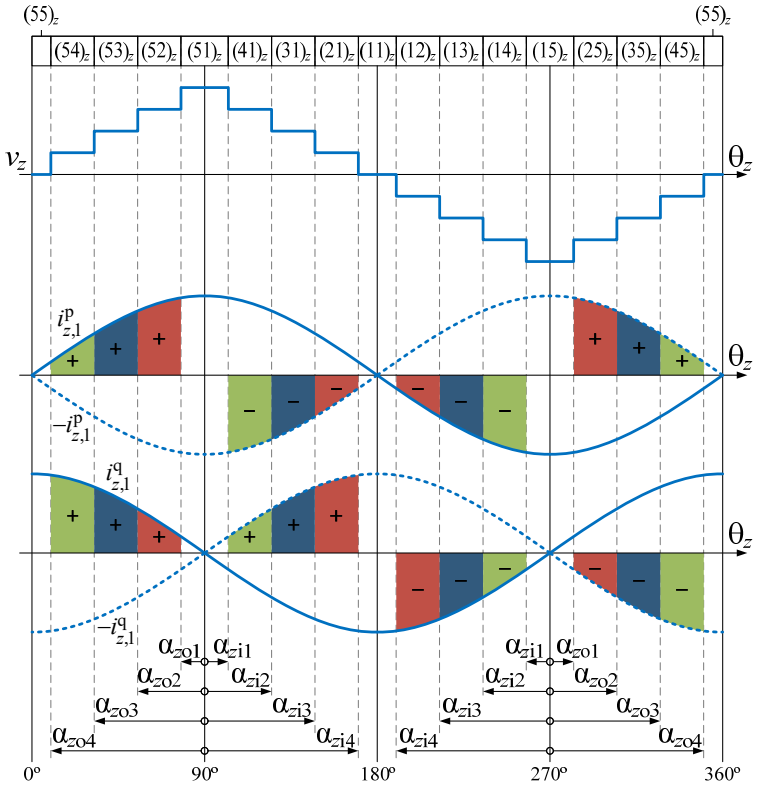


Fig. 4.4. Voltage v_z and the in-phase and in-quadrature components of i_z fundamental component ($i^p_{z,1}$ and $i^q_{z,1}$). The red, blue, and green areas depict the charge injected into (+) or drawn from (–) inner dc-link points 2_z, 3_z, and 4_z, respectively, by $i^p_{z,1}$ and $i^q_{z,1}$.

Consequently, a control action is needed which modifies the values of the inner (α_{zi1}, α_{zi2}, α_{zi3}, α_{zi4}) and outer (α_{zo1}, α_{zo2}, α_{zo3}, α_{zo4}) switching angles in order to provide a non-zero charge to the inner dc-link points during a switching cycle and, ultimately, correct any capacitor voltage unbalance. This charge will only be provided by $i^p_{z,h}$, $h \in \{1,2,3,\ldots,\infty\}$, since the total charge provided by $i^q_{z,h}$, $h \in$

{1,2,3,…,∞} is always zero, owing to the odd symmetry of v_z. Moreover, most of the charge will be provided by $i^{p}_{z,1}$.

4.4.1.1. Full control scheme

Fig. 4.5 shows the proposed full control scheme. This control scheme is an extension to five levels of the 4L-DAB full control scheme shown in Fig. 3.8. As in the 3L-DAB and 4L-DAB cases, unbalance variables (y_{zm}) are computed from the filtered capacitor voltages, and compared with the command values (y^{*}_{zm}) in order to obtain the error variables (e_{zm}). For instance, a value $e_{z2} > 0$ means that v_{Cz1} is below its desired value and the average value among v_{Cz2}, v_{Cz3}, and v_{Cz4} is above its desired value. Therefore, a control action is required that injects charge into 2_z in order to increase v_{Cz1} and decrease v_{Cz2}, v_{Cz3}, and v_{Cz4}; i.e., increase y_{z2}. The same principle is applied to inner dc-link points 3_z and 4_z.

Without loss of generality, let us assume that power is transferred from side a to side b. Then, any $e_{zm} \neq 0$ can be corrected by modifying the switching angles as described in Table 4.1. Control variables u_{zm}, generated by processing e_{zm} variables with compensators $G_{zm}(s)$, are responsible of performing the required control action. Switching angles α_{zi1}, α_{zi2}, α_{zi3}, α_{zi4}, α_{zo1}, α_{zo2}, α_{zo3}, and α_{zo4} are modified by u_{zm} variables in a per-unit basis from the value of the initial switching angles α_{z1}, α_{z2}, α_{z3}, and α_{z4}.

Regarding compensators $G_{zm}(s)$, the sign of $k_{P,zm}$ is subject to the same rationale discussed for the 3L-DAB (Section 2.4.1.1).

It is worth noting that the proposed control scheme takes advantage of all the available switching angles to correct any preexisting voltage unbalance.

z	*m*	e_{zm}	Charge sign to provide	{α_{zo1}, α_{zi4}}	{α_{zo2}, α_{zi3}}	{α_{zo3}, α_{zi2}}	{α_{zo4}, α_{zi1}}
a	2	+ / –	+ / –	↓ / ↑	↑ / ↓		
	3	+ / –	+ / –		↓ / ↑	↑ / ↓	
	4	+ / –	+ / –			↓ / ↑	↑ / ↓
b	2	+ / –	+ / –	↑ / ↓	↓ / ↑		
	3	+ / –	+ / –		↑ / ↓	↓ / ↑	
	4	+ / –	+ / –			↑ / ↓	↓ / ↑

Table 4.1. Sign of the charge to be provided and switching angles change needed to correct a voltage unbalance at inner dc-link point m_z, depending on the sign of e_{zm}, and according to Fig. 4.4.

From Table 4.1, it can also be observed that switching angles pair $\{\alpha_{zo2}, \alpha_{zi3}\}$ is modified by both u_{z2} and u_{z3}, and $\{\alpha_{zo3}, \alpha_{zi2}\}$ is modified by both u_{z3} and u_{z4}. If $G_{zm}(s)$ is defined as a proportional controller, it can be seen that in the case where $\text{sgn}(e_{z2}) = \text{sgn}(e_{z4}) \neq \text{sgn}(e_{z3})$, the three control variables modify $\{\alpha_{zo2}, \alpha_{zi3}\}$ and $\{\alpha_{zo3}, \alpha_{zi2}\}$ in the required directions to correct the three voltage unbalances. However, when $\text{sgn}(e_{z2}) = \text{sgn}(e_{z3})$, $\{\alpha_{zo2}, \alpha_{zi3}\}$ will be modified in favor of y_{z2} regulation when $|u_{z2}| > |u_{z3}|$, or in favor of y_{z3} when $|u_{z2}| < |u_{z3}|$. The same happens for $\{\alpha_{zo3}, \alpha_{zi2}\}$; When $\text{sgn}(e_{z3}) = \text{sgn}(e_{z4})$, these switching angles will be modified in favor of y_{z3} regulation when $|u_{z3}| > |u_{z4}|$, or in favor of y_{z4} when $|u_{z3}| < |u_{z4}|$.

Hence, the proposed full control scheme presents a coupling between the control loops that regulate y_{z2}, y_{z3}, and y_{z4}. This coupling can be detrimental to the control performance. Thus, a means to reverse such coupling would improve its performance.

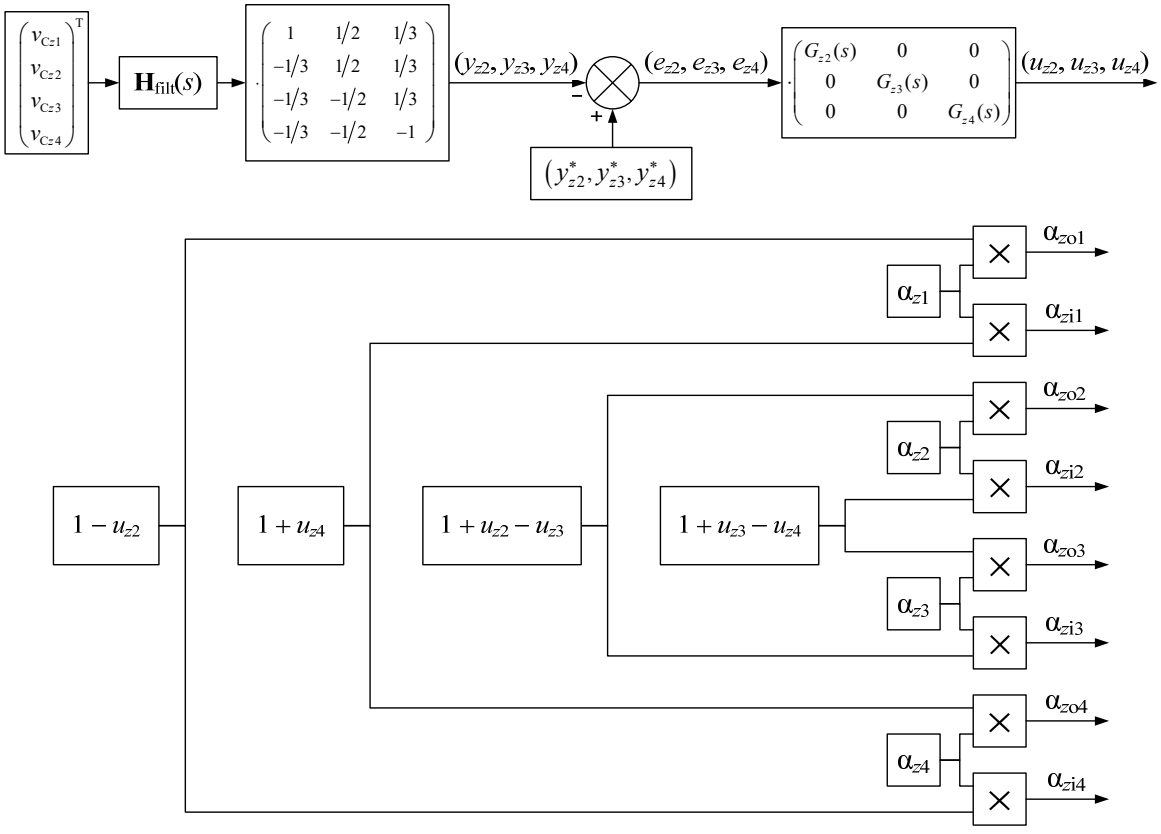


Fig. 4.5. Full control scheme for the z-side capacitor voltage balancing.

4.4.1.2. Full control scheme with decoupling

Analogous to the 4L-DAB, the 5L-DAB full control scheme presented in Fig. 4.5 presents two levels of coupling. First, the plant coupling described in Section 3.4.1.2. Second, as described in Section 4.4.1.1, the implicit coupling in the full control scheme, where the regulation of y_{zm} with $\{\alpha_{zo2}, \alpha_{zi3}\}$ or $\{\alpha_{zo3}, \alpha_{zi2}\}$ alters simultaneously the charge provided to inner dc-link points 2_z and 3_z or 3_z and 4_z, respectively.

Therefore, as it has been done in Section 3.4.1, it is necessary to derive the coupling matrix present in the transfer function, with the objective of determining a decoupling matrix. This decoupling matrix will allow having a control scheme where the control variables outputted by the controller (u'_{zm}) will only affect its corresponding unbalance variable; i.e., u'_{zm} will only affect y_{zm}.

For the present study, the same assumptions as in Section 3.4.1 are made; i.e., V_Z is kept constant, all capacitors are assumed to be of equal capacitance, and switching angles α_{zk} are considered to be constant during a switching cycle.

Let us suppose that a current I_{2z} is injected into inner dc-link point 2_z. Such current will be distributed in three quarters flowing through the bottom capacitor and one quarter flowing through the upper capacitors. For a current I_{3z} being injected into 3_z, one half will flow through the bottom capacitors and another one half through the upper capacitors. Analogously to 2_z, a current I_{4z} being injected into 4_z will be distributed in one quarter flowing through the bottom capacitors and three quarters through the upper capacitor.

If it is considered that the three currents are injected simultaneously, the capacitor voltages will vary

$$\begin{aligned}
\Delta v_{Cz1} &= \frac{1}{s \cdot C_z} \cdot \left(\frac{3}{4} \cdot I_{2z} + \frac{1}{2} \cdot I_{3z} + \frac{1}{4} \cdot I_{4z} \right) \\
\Delta v_{Cz2} &= \frac{1}{s \cdot C_z} \cdot \left(-\frac{1}{4} \cdot I_{2z} + \frac{1}{2} \cdot I_{3z} + \frac{1}{4} \cdot I_{4z} \right) \\
\Delta v_{Cz3} &= \frac{1}{s \cdot C_z} \cdot \left(-\frac{1}{4} \cdot I_{2z} - \frac{1}{2} \cdot I_{3z} + \frac{1}{4} \cdot I_{4z} \right) \\
\Delta v_{Cz4} &= \frac{1}{s \cdot C_z} \cdot \left(-\frac{1}{4} \cdot I_{2z} - \frac{1}{2} \cdot I_{3z} - \frac{3}{4} \cdot I_{4z} \right).
\end{aligned} \tag{4.8}$$

The variation of the unbalance variables will be

$$\begin{aligned}
\Delta y_{z2} &= \left(\Delta v_{Cz1} - \frac{\Delta v_{Cz2} + \Delta v_{Cz3} + \Delta v_{Cz4}}{3} \right) = \frac{1}{s \cdot C_z} \cdot \left(I_{2z} + \frac{2}{3} \cdot I_{3z} + \frac{1}{3} \cdot I_{4z} \right) \\
\Delta y_{z3} &= \left(\frac{\Delta v_{Cz1} + \Delta v_{Cz2}}{2} - \frac{\Delta v_{Cz3} + \Delta v_{Cz4}}{2} \right) = \frac{1}{s \cdot C_z} \cdot \left(\frac{1}{2} \cdot I_{2z} + I_{3z} + \frac{1}{2} \cdot I_{4z} \right) \\
\Delta y_{z4} &= \left(\frac{\Delta v_{Cz1} + \Delta v_{Cz2} + \Delta v_{Cz3}}{3} - \Delta v_{Cz4} \right) = \frac{1}{s \cdot C_z} \cdot \left(\frac{1}{3} \cdot I_{2z} + \frac{2}{3} \cdot I_{3z} + I_{4z} \right).
\end{aligned} \tag{4.9}$$

The plant transfer function, with I_{mz} as the inputs and y_{zm} as the outputs, can be defined as

$$\begin{pmatrix} y_{z2} \\ y_{z3} \\ y_{z4} \end{pmatrix} = \frac{1}{C_z \cdot s} \cdot \mathbf{C_{5L}} \begin{pmatrix} I_{2z} \\ I_{3z} \\ I_{4z} \end{pmatrix}, \tag{4.10}$$

where $\mathbf{C_{5L}}$ is the coupling matrix of the plant and is equal to

$$\mathbf{C_{5L}} = \begin{pmatrix} 1 & 2/3 & 1/3 \\ 1/2 & 1 & 1/2 \\ 1/3 & 2/3 & 1 \end{pmatrix}. \tag{4.11}$$

Considering only the fundamental component of i_z, the currents provided to the inner dc-link points, within a switching cycle, and as a function of the control variables, are defined as

$$\begin{aligned}
I_{2z,1}(u_{z2},u_{z3},u_{z4}) &= \frac{I_{z,1}^{\mathrm{p}}}{\pi} \cdot \Big[\sin\left(\alpha_{z2}\left(1+u_{z2}-u_{z3}\right)\right) - \sin\left(\alpha_{z1}\left(1-u_{z2}\right)\right) \\
&\qquad - \sin\left(\alpha_{z4}\left(1-u_{z2}\right)\right) + \sin\left(\alpha_{z3}\left(1+u_{z2}-u_{z3}\right)\right) \Big] \\
I_{3z,1}(u_{z2},u_{z3},u_{z4}) &= \frac{I_{z,1}^{\mathrm{p}}}{\pi} \cdot \Big[\sin\left(\alpha_{z3}\left(1+u_{z3}-u_{z4}\right)\right) - \sin\left(\alpha_{z2}\left(1+u_{z2}-u_{z3}\right)\right) \\
&\qquad - \sin\left(\alpha_{z3}\left(1+u_{z2}-u_{z3}\right)\right) + \sin\left(\alpha_{z2}\left(1+u_{z3}-u_{z4}\right)\right) \Big] \\
I_{4z,1}(u_{z2},u_{z3},u_{z4}) &= \frac{I_{z,1}^{\mathrm{p}}}{\pi} \cdot \Big[\sin\left(\alpha_{z4}\left(1+u_{z4}\right)\right) - \sin\left(\alpha_{z3}\left(1+u_{z3}-u_{z4}\right)\right) \\
&\qquad - \sin\left(\alpha_{z2}\left(1+u_{z3}-u_{z4}\right)\right) + \sin\left(\alpha_{z1}\left(1+-u_{z4}\right)\right) \Big].
\end{aligned} \tag{4.12}$$

Following the same procedure of Section 3.4.1, let us linearize $I_{mz,1}(u_{z2},u_{z3},u_{z4})$ at $u_{zm} = 0\ \forall m$

$$
\begin{aligned}
I_{2z,1}^{\text{lin}}\left(u_{z2},u_{z3},u_{z4}\right) &= I_{2z,1}\left(0,0,0\right)+\left[\frac{\delta I_{2z,1}}{\delta u_{z2}}\bigg|_{\substack{u_{z2}=0\\u_{z3}=0\\u_{z4}=0}}\right]\cdot u_{z2}+\left[\frac{\delta I_{2z,1}}{\delta u_{z3}}\bigg|_{\substack{u_{z2}=0\\u_{z3}=0\\u_{z4}=0}}\right]\cdot u_{z3}+\left[\frac{\delta I_{2z,1}}{\delta u_{z4}}\bigg|_{\substack{u_{z2}=0\\u_{z3}=0\\u_{z4}=0}}\right]\cdot u_{z4} \\
&= e_{5\text{LF}}\cdot\left[\left(a_{5\text{LF}}+b_{5\text{LF}}\right)\cdot u_{z2}-b_{5\text{LF}}\cdot u_{z3}\right] \\
I_{3z,1}^{\text{lin}}\left(u_{z2},u_{z3},u_{z4}\right) &= I_{3z,1}\left(0,0,0\right)+\left[\frac{\delta I_{3z,1}}{\delta u_{z2}}\bigg|_{\substack{u_{z2}=0\\u_{z3}=0\\u_{z4}=0}}\right]\cdot u_{z2}+\left[\frac{\delta I_{3z,1}}{\delta u_{z3}}\bigg|_{\substack{u_{z2}=0\\u_{z3}=0\\u_{z4}=0}}\right]\cdot u_{z3}+\left[\frac{\delta I_{3z,1}}{\delta u_{z4}}\bigg|_{\substack{u_{z2}=0\\u_{z3}=0\\u_{z4}=0}}\right]\cdot u_{z4} \\
&= e_{5\text{LF}}\cdot\left[-b_{5\text{LF}}\cdot u_{z2}+2\cdot b_{5\text{LF}}\cdot u_{z3}-b_{5\text{LF}}\cdot u_{z4}\right] \\
I_{4z,1}^{\text{lin}}\left(u_{z2},u_{z3},u_{z4}\right) &= I_{4z,1}\left(0,0,0\right)+\left[\frac{\delta I_{4z,1}}{\delta u_{z2}}\bigg|_{\substack{u_{z2}=0\\u_{z3}=0\\u_{z4}=0}}\right]\cdot u_{z2}+\left[\frac{\delta I_{4z,1}}{\delta u_{z3}}\bigg|_{\substack{u_{z2}=0\\u_{z3}=0\\u_{z4}=0}}\right]\cdot u_{z3}+\left[\frac{\delta I_{4z,1}}{\delta u_{z4}}\bigg|_{\substack{u_{z2}=0\\u_{z3}=0\\u_{z4}=0}}\right]\cdot u_{z4} \\
&= e_{5\text{LF}}\cdot\left[-b_{5\text{LF}}\cdot u_{z3}+\left(a_{5\text{LF}}+b_{5\text{LF}}\right)\cdot u_{z4}\right],
\end{aligned}
\tag{4.13}
$$

where

$$
\begin{aligned}
a_{5\text{LF}} &= \alpha_{z1}\cdot\cos\left(\alpha_{z1}\right)+\alpha_{z4}\cdot\cos\left(\alpha_{z4}\right) \\
b_{5\text{LF}} &= \alpha_{z2}\cdot\cos\left(\alpha_{z2}\right)+\alpha_{z3}\cdot\cos\left(\alpha_{z3}\right) \\
e_{5\text{LF}} &= \frac{I_{z,1}^{\text{p}}}{\pi},
\end{aligned}
\tag{4.14}
$$

switching angles are in radians, and $I_{2z,1}(0,0,0) = I_{3z,1}(0,0,0) = I_{4z,1}(0,0,0) = 0$ due to (4.5) being fulfilled for the sake of easing the capacitor voltage balancing.

Finally, by substituting I_{mz} on (4.10) with $I^{\text{lin}}{}_{mz,1}$ in (4.13), the plant transfer function, where the inputs are control variables u_{zm} and the outputs are unbalance variables y_{zm}, can be obtained

$$
\begin{pmatrix} y_{z2} \\ y_{z3} \\ y_{z4} \end{pmatrix} = \frac{e^{5\text{LF}}}{C_z\cdot s}\cdot\mathbf{E_{5L}}\begin{pmatrix} u_{z2} \\ u_{z3} \\ u_{z4} \end{pmatrix}
\tag{4.15}
$$

where

$$\mathbf{E_{5L}} = \mathbf{C_{5L}} \cdot \mathbf{D_{5L}} = \begin{pmatrix} 1 & 2/3 & 1/3 \\ 1/2 & 1 & 1/2 \\ 1/3 & 2/3 & 1 \end{pmatrix} \begin{pmatrix} a_{5LF} + b_{5LF} & -b_{5LF} & 0 \\ -b_{5LF} & 2 \cdot b_{5LF} & -b_{5LF} \\ 0 & -b_{5LF} & a_{5LF} + b_{5LF} \end{pmatrix}$$
$$= \begin{pmatrix} a_{5LF} + \dfrac{b_{5LF}}{3} & 0 & \dfrac{a_{5LF} - b_{5LF}}{3} \\ \dfrac{a_{5LF} - b_{5LF}}{2} & b_{5LF} & \dfrac{a_{5LF} - b_{5LF}}{2} \\ \dfrac{a_{5LF} - b_{5LF}}{2} & 0 & a_{5LF} + \dfrac{b_{5LF}}{3} \end{pmatrix}, \tag{4.16}$$

$\mathbf{C}_{5L}$ is the plant coupling matrix and $\mathbf{D}_{5L}$ is the coupling matrix of the control.

Hence, in order to decouple the system, the output vector of control commands provided by the compensators (u'_{z2}, u'_{z3}, u'_{z4}) has to be multiplied by the inverse of coupling matrix $\mathbf{E_{5L}}$, defined as

$$\mathbf{E_{5L}^{-1}} = \frac{1}{8} \cdot \begin{pmatrix} \dfrac{3\left(3 \cdot a_{5LF} + b_{5LF}\right)}{a_{5LF}^2 + a_{5LF} \cdot b_{5LF}} & 0 & \dfrac{-3\left(a_{5LF} - b_{5LF}\right)}{a_{5LF}^2 + a_{5LF} \cdot b_{5LF}} \\ \dfrac{-3\left(a_{5LF} - b_{5LF}\right)}{a_{5LF} \cdot b_{5LF}} & \dfrac{8}{b_{5LF}} & \dfrac{-3\left(a_{5LF} - b_{5LF}\right)}{a_{5LF} \cdot b_{5LF}} \\ \dfrac{-3\left(a_{5LF} - b_{5LF}\right)}{a_{5LF}^2 + a_{5LF} \cdot b_{5LF}} & 0 & \dfrac{3\left(3 \cdot a_{5LF} + b_{5LF}\right)}{a_{5LF}^2 + a_{5LF} \cdot b_{5LF}} \end{pmatrix} \tag{4.17}$$

The control scheme resulting from the introduction of the decoupling matrix is shown in Fig. 4.6.

As a side note, the suitability of linearization performed to determine the coupling existing on the system transfer function is studied in Section 5.4.1.3.

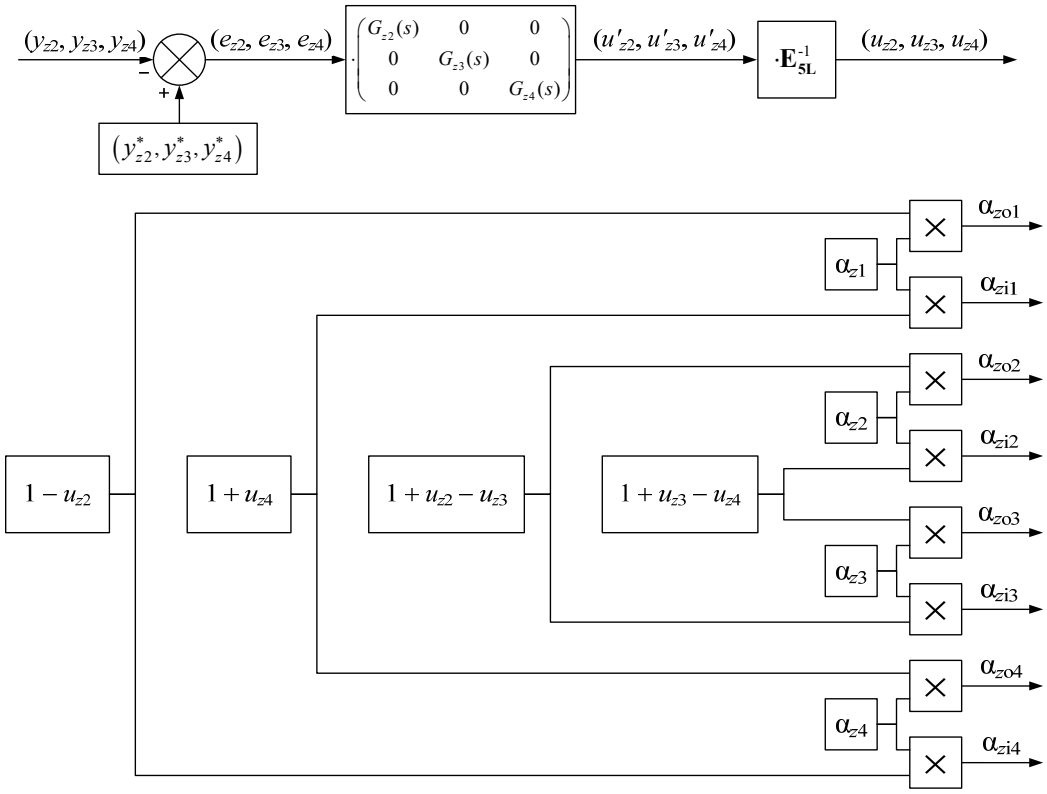


Fig. 4.6. Full control scheme for the z-side capacitor voltage balancing with decoupling. The subscheme that computes y_{zm} is the same of Fig. 4.5.

4.5. Definition of the modulation parameter values

Unlike as it has been previously done in the 3L-DAB and 4L-DAB chapters, this section does not actively pursue the performance optimization of the 5L-DAB. This is due to the great complexity of such endeavor, since it involves finding the optimum solution of a set of equations with nine independent variables (two more than in the 4L-DAB performance optimization), hence requiring a great computational effort. However, since the optimum solutions found for the 3L-DAB and 4L-DAB cases (Section 2.5.3 and Section 3.5.2, respectively) are quite similar, it is reasonable to assume that the optimum solutions for the 5L-DAB case would be of the same nature. It will be therefore assumed that a set of equations similar to the 3L-DAB and 4L-DAB practical solutions (Section 2.5.4 and Section 3.5.3, respectively) are also valid to determine a set of 5L-DAB modulation parameter values providing a good converter performance.

The practical solution for the 5L-DAB is defined as

$$\begin{aligned}
\{\alpha_{z1}\}_{\mathrm{PrS}} &= \begin{cases} 0° + \dfrac{\alpha_{z,\mathrm{th}}}{\varphi_{z,\mathrm{th}}} \cdot \varphi, & \varphi < \varphi_{z,\mathrm{th}} \\ \alpha_{z,\mathrm{th}} + \dfrac{90° - \alpha_{z,\mathrm{th}}}{90° - \varphi_{z,\mathrm{th}}} \cdot (\varphi - \varphi_{z,\mathrm{th}}), & \varphi \geq \varphi_{z,\mathrm{th}} \end{cases} \\
\{\alpha_{z2}\}_{\mathrm{PrS}} &= \arcsin\left(\sin(\alpha_{z1}) + \Delta_{z1}\right), \\
\{\alpha_{z3}\}_{\mathrm{PrS}} &= \arcsin\left(\sin(\alpha_{z4}) - \Delta_{z1}\right), \\
\{\alpha_{z4}\}_{\mathrm{PrS}} &= \begin{cases} 90° - K_{\alpha,\mathrm{th}} \cdot \varphi, & \varphi < \varphi_{z,\mathrm{th}} \\ \alpha_{z,\mathrm{th}} + \dfrac{90° - \alpha_{z,\mathrm{th}}}{90° - \varphi_{z,\mathrm{th}}} \cdot (\varphi - \varphi_{z,\mathrm{th}}), & \varphi \geq \varphi_{z,\mathrm{th}}, \end{cases}
\end{aligned} \tag{4.18}$$

Switching angles α_{z1} and α_{z4} are equal to α_{z1} and α_{z3}, respectively, of the 4L-DAB practical solution (also equal to α_{z1} and α_{z2} of the 3L-DAB practical solution). Intermediate switching angles α_{z2} and α_{z3} are computed using (4.6), which guarantees that the charge provided to the inner dc-link points within a switching cycle by $i_{z,1}$ is null. Variable Δ_{z1} can be defined, for example, as

$$\Delta_{z1} = \frac{\sin(\alpha_{z4}) - \sin(\alpha_{z1})}{3} \tag{4.19}$$

among other possibilities to guarantee (4.1).

Fig. 4.7 presents the switching angle values of this practical solution for the following parameter values: $K_{\varphi,\mathrm{th}} = 50°$, $K_{\alpha,\mathrm{th}} = 0.2$, and $\varphi_{\mathrm{th,max}} = 80°$.

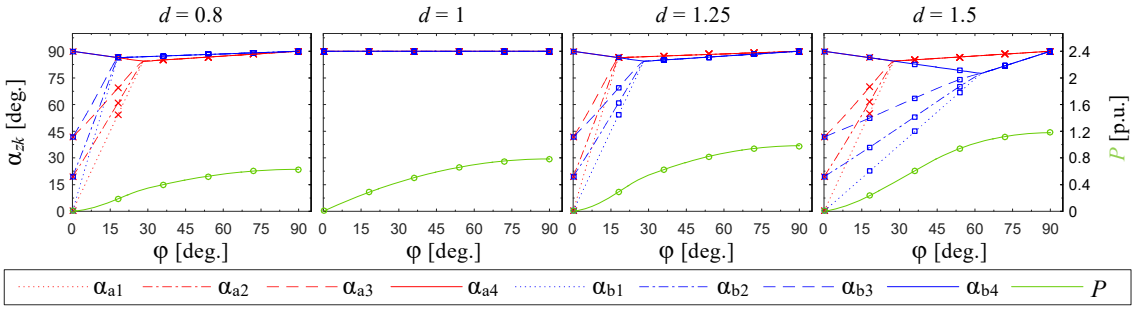


Fig. 4.7. Switching angle values and transferred-power values given by the 5L-DAB practical solution as a function of phase shift.

Fig. 4.8 presents the value of the objective functions (defined in Section 2.5), as a function of P, obtained with the practical solution of Fig. 4.7 [$F_f(X_{\mathrm{PrS}})$] and with the PSM [$F_f(X_{\mathrm{PSM}})$]. Solution X_{PSM} $\forall d$ is the same as the practical solution for $d = 1$. The base voltage, current, and power values are computed with (2.23).

Comparing the objective function values obtained with the practical solution and PSM on the 5L-DAB and 4L-DAB converters, it can be seen that equivalent patterns are present on both converters. Objective functions F_2 and F_3 present greater values in the 5L-DAB case, because four more switching transitions per switching cycle are performed. Due to the similarity with the 4L-DAB results, analogous conclusions can be drawn; the proposed practical solution is expected to achieve lower conduction and switching losses than PSM for low-to-medium powers when $d \neq 1$, while at high powers and for the full power range at $d = 1$, both the practical solutions and PSM present similar conduction and switching losses.

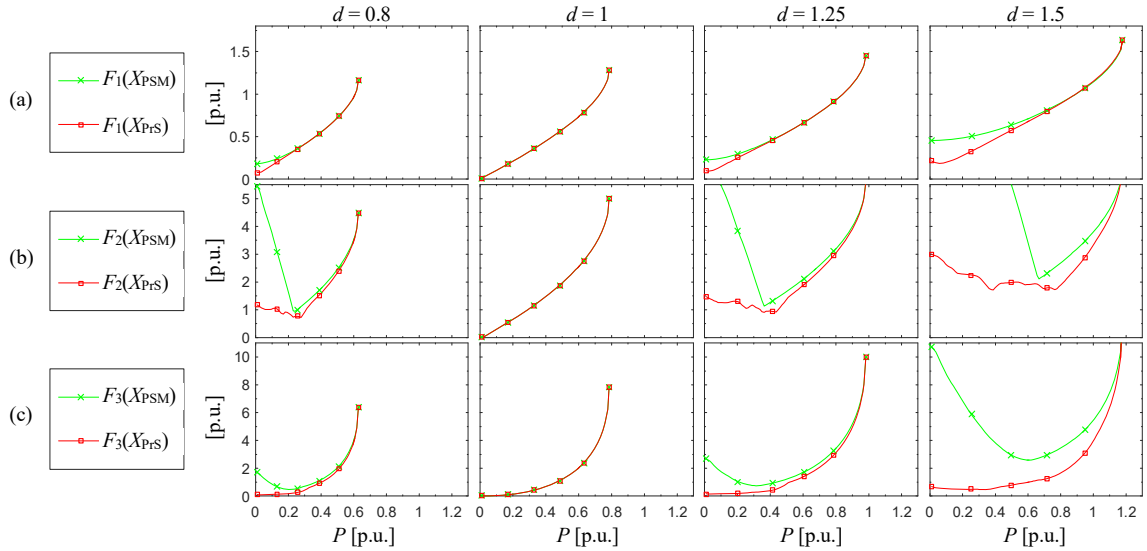


Fig. 4.8. Objective function values as a function of P for solutions X_{PrS} and X_{PSM} (V_A = 1 p.u.). (a) F_1. (b) F_2. (c) F_3.

4.6. Simulation results

Simulations have been carried out to demonstrate the effectiveness of the proposed 5L-DAB converter and capacitor-voltage-balancing control. A MATLAB-Simulink lossless model of the converter in Fig. 4.1 is used to perform the simulations, where it is assumed $n = 1$, $C_z = 100$ µF, $L = 300$ µH, $f_s = 20$ kHz, and $H_{filt}(s) = 2\pi \cdot 2000/(s + 2\pi \cdot 2000)$.

The capacitor-voltage-balancing control schemes employed in each test are handled by the PI compensator defined in (2.14). Switching angles α_{zok} and α_{zik} are processed by the limitation algorithm presented in Appendix B, in order to limit its values to the defined boundaries ($\Delta\alpha_{z,min} = 5.04^o$ $\forall z$, corresponding to $t_{b,z} = 700$ ns $\forall z$).

The voltage on the load (V_B) is controlled by the regulator defined in Fig. 2.15, with $K_{ps} = 7500$, $f_{z,ps} = 50$ Hz, $f_{p,ps} = 2500$ Hz, and V_o^* equal to the V_B defined in each working point. The output

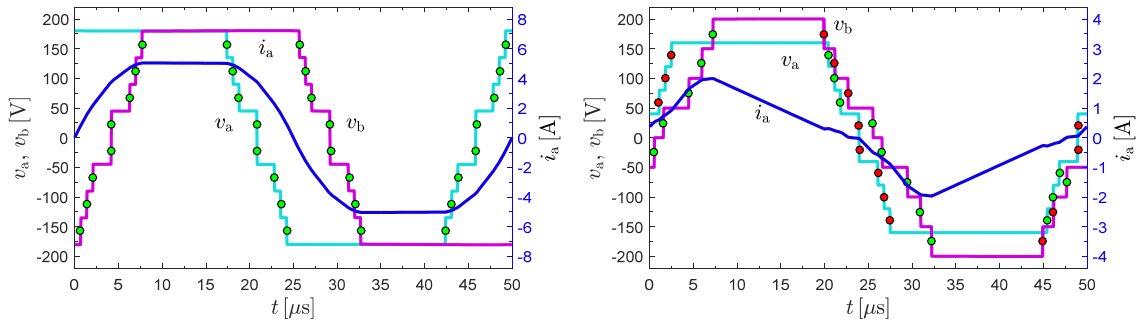
load resistor value (R_B) is adjusted so that the phase shift control settles on the desired φ and V_B defined in the working point.

4.6.1. Steady-state results

In all the simulations performed to obtain steady-state results, switching angles α_{zk} are defined with the practical solution proposed in Fig. 4.7, while the capacitor voltage balancing is performed by the decoupled full control scheme proposed in Section 4.4.1.2, with compensator parameter values $k_{P,am} = -k_{P,bm} = 0.4$ and $T_{I,zm} = 20$ ms $\forall z,m$. Two working points are analyzed:

- WP1: $d = 1$ ($V_A = 180$ V, $V_B = 180$ V) and $\varphi \approx 60º$.
- WP2: $d = 1.25$ ($V_A = 160$ V, $V_B = 200$ V) and $\varphi \approx 15º$.

Fig. 4.9 presents the steady-state results obtained for both working points. It can be observed that the a-side and b-side dc-link capacitor voltages are balanced, since both v_a and v_b present voltage steps of equal magnitude. As in previous chapters, Type I switching transitions (hard switching) are marked with a red dot, while Type II switching transitions (soft switching) are marked with a green dot. It can be observed that for WP1, all switching transitions are of soft-switching nature, while for WP2, most of the hard-switching transitions occur at low current values (less than a third of the maximum current).



(a) (b)

Fig. 4.9. Simulated v_a, v_b, and i_a in steady state and with the capacitor-voltage-balancing control enabled on both sides. (a) WP1, with $R_B = 59$ Ω, and $P = 549$ W. (b) WP2 with $R_B = 271$ Ω, and $P = 149$ W.

The switching angles characterizing v_a and v_b waveforms in Fig. 4.9 (α_{zok} and α_{zik}) are different from those obtained with the practical solution (α_{zk}). This is due to the control action performed by the capacitor-voltage-balancing control, as well as the limitation algorithm. Table 4.2 shows the value of such switching angles. It is worth noticing that, even when the values of $\{\alpha_{zo1}, \alpha_{zo2}, \alpha_{zo3}\}$ and $\{\alpha_{zi1}, \alpha_{zi2}, \alpha_{zi3}\}$ are forced by the limitation algorithm, the balancing control manages to perform the proper control action to achieve capacitor voltage balancing on both sides.

	z	a				b			
	k	1	2	3	4	1	2	3	4
WP1	α_{zk}	90º	90º	90º	90º	90º	90º	90º	90º
	α_{zok}	65.39º	70.43º	75.47º	90º	64.75º	69.79º	74.83º	90º
	α_{zik}	65.39º	70.43º	75.47º	90º	64.75º	69.79º	74.83º	90º
WP2	α_{zk}	71.50º	76.50º	80.22º	86.94º	46.02º	54.35º	64.9º	86.94º
	α_{zok}	64.60º	69.64º	74.68º	90º	45.70º	54.81º	65.42º	86.10º
	α_{zik}	64.56º	69.60º	74.64º	90º	45.57º	54.78º	65.46º	86.33º

Table 4.2. Switching angles obtained in steady state with the practical solution (α_{zk}) and with the capacitor-voltage-balancing control after being processed by the limitation algorithm (α_{zok} and α_{zik}).

4.6.2. Transient results

Simulations to obtain transient results help demonstrating the behavior, performance, and suitability of the proposed control schemes. Two sets of simulations are performed.

The first set of simulations consists on forcing an unbalance of the a-side dc-link capacitor voltages, by assigning a non-zero value to the command unbalance variables. The performed action will force the increase of v_{Ca1} and the decrease of v_{Ca4}, while v_{Ca2} and v_{Ca3} remain constant. This is accomplished by imposing $y^*_{a2}/y^*_{a3} = y^*_{a4}/y^*_{a3} = 4/3$. Fig. 4.10 shows the simulation results, where in dark red, dark blue, and dark green, are represented variables y_{am}, u_{am}, α_{aik}, and α_{aok} involved in the regulation of inner dc-link points 2_a, 3_a, and 4_a voltages, respectively. In light blue are represented variables α_{aik} and α_{aok} involved in the simultaneous regulation of y_{a2} and y_{a3}, while purple represents the variables corresponding to the simultaneous regulation of y_{a3} and y_{a4}. To fulfill the assumptions considered in the design of the decoupled control scheme, the chosen values for the PI regulator parameters ($k_{P,am} = -k_{P,bm} = 0.3$ and $T_{I,zm} = 20$ ms $\forall z,m$) guarantee that the switching angle values during the transient tests do not get limited by 90º, 0º, or by an adjacent switching angle, and the values of α_{zk} guarantee a null charge provided to the inner dc-link points by $i_{z,1}$ when $u_{zm} = 0$ $\forall m$.

Fig. 4.10(a) shows the simulation results when employing the non-decoupled full control scheme. It can be observed that v_{Ca2} and v_{Ca3} voltages do not behave as desired; i.e., they are altered due to the coupling of the plant and the control loops. On the other hand, when the decoupled control scheme is employed [Fig. 4.10(b)], v_{Ca2} and v_{Ca3} voltages do remain constant (as expected).

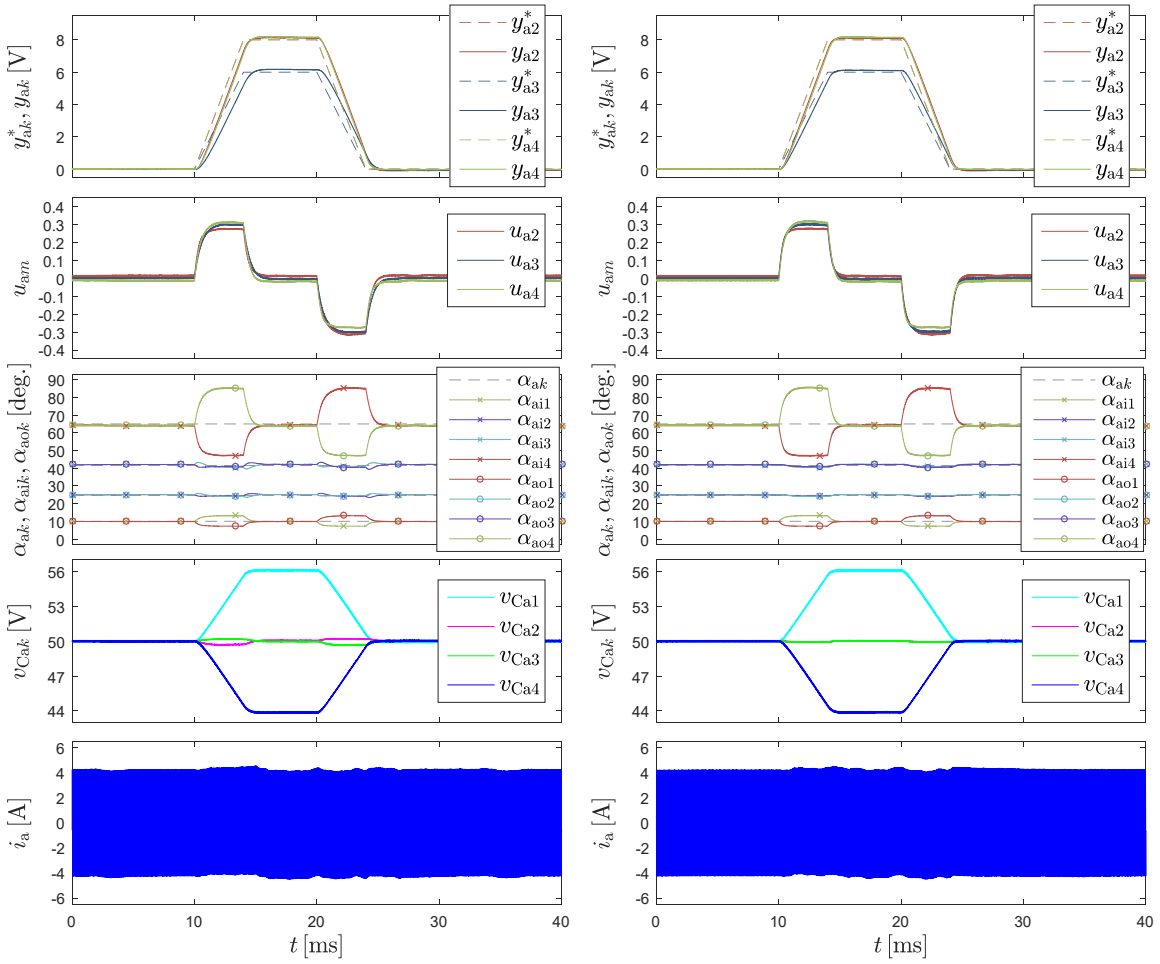


Fig. 4.10. Simulation results under ramp variations of ±2 V/ms for y^*_{a2} and y^*_{a4}, and ±1.5 V/ms for y^*_{a3}. Conditions: V_A = 200 V, V_B = 160 V, R_B = 142 Ω, $\varphi \approx 65°$, and $\{\alpha_{z1},\alpha_{z2},\alpha_{z3},\alpha_{z4}\} = \{10°,24.7°,41.5°,65°\}$ ∀z. (a) Results when employing the non-decoupled full control scheme of Fig. 4.5. (b) Results when employing the decoupled full control scheme of Fig. 4.6.

A second set of simulation results is presented in Fig. 4.11. An initial unbalance is forced in v_{Cb1}, v_{Cb2}, v_{Cb3}, and v_{Cb4} by disabling the b-side capacitor-voltage-balancing control and loading each b-side capacitor with a resistor in parallel. The values of these resistors are 175 Ω, 375 Ω, 375 Ω, and 175 Ω for each of the four dc-link capacitors, from top to bottom (Fig. 4.1), which set initial voltages $\{v_{Cb1},v_{Cb2},v_{Cb3},v_{Cb4}\}$ = {25,55,55,25} V. Once the b-side balancing control is enabled, the capacitor voltage balance is quickly recovered, although there is a sag of V_B voltage due to the decrease of α_{bik} and α_{bok} ($k \in \{1,2,3\}$), which reduces the transferred power. This sag is compensated by the load-voltage control by incrementing φ. It is worth noticing that the balancing control is able to maintain the capacitor voltages balanced with little effort (α_{bik} and α_{bok} are close to α_{bk} when a steady state is reached), considering the high unbalanced load applied to the dc-link capacitors.

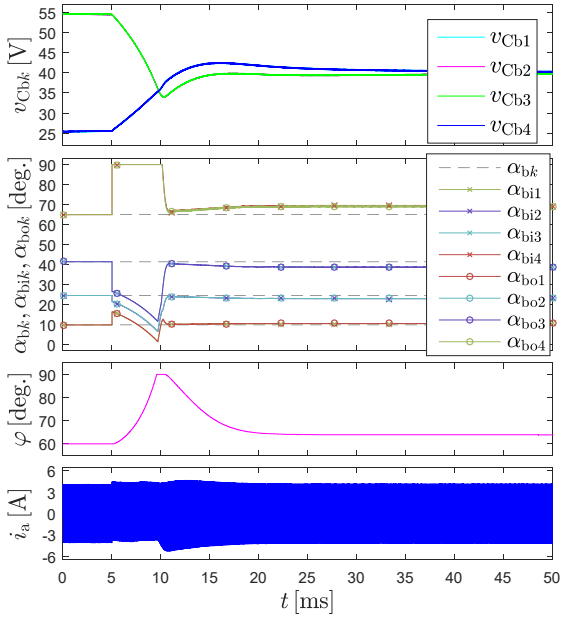


Fig. 4.11. Waveforms v_{Cb1}, v_{Cb2}, v_{Cb3}, v_{Cb4}, and i_a under a b-side capacitor-voltage-balancing transient. The a-side capacitor-voltage-balancing control is all the time enabled, guaranteeing the a-side capacitor voltage balancing. The b-side capacitor-voltage-balancing control is enabled at t = 5 ms. Conditions: V_A = 200 V, V_B = 160 V, R_B = 170 Ω, $\{\alpha_{z1},\alpha_{z2},\alpha_{z3},\alpha_{z4}\} = \{10°,24.7°,41.5°,65°\}$ $\forall z$, and K_{ps} = 20000.

4.7. Conclusion

This chapter has explored the possibility of implementing DAB dc-dc converters employing five-level NPC legs. A suitable modulation strategy and a first capacitor-voltage-balancing control scheme have been defined. A thorough analysis has revealed two coupling mechanisms that affect the regulation of each inner dc-link point voltage. As a result, a decoupled version of the first control scheme has been proposed. Simulation results demonstrate the feasibility of the proposed modulation and of both capacitor-voltage-balancing control schemes. Moreover, the comparison between both control schemes shows that the decoupled control scheme offers a slightly sharper control action.

The modulation offers seventeen DoF. Ten of these DoF are used to guarantee capacitor voltage balancing and the remaining seven DoF are used to control the power flow between both converter sides and improve the converter performance. This is accomplished by defining α_{zk} as a function of φ and Δ_{z1} with a set of closed-form expressions (the so-called practical solution) based on the 3L-DAB and 4L-DAB practical solutions. Moreover, the proposed practical solution offers greater converter performance when compared with the conventional PSM.

Compared to the proposed 3L-DAB and 4L-DAB topologies, the proposed 5L-DAB topology presents several advantages; namely, an increase in the total dc-link voltage for a given

semiconductor-device voltage rating, the possibility of using lower-voltage-rated semiconductor devices with better performance figures for a given dc-link voltage, lower converter losses, better converter loss distribution, and lower transformer-current harmonic distortion, which leads to lower magnetic losses.

CHAPTER 5.

STUDY OF AN *N*-LEVEL NEUTRAL-POINT-CLAMPED DUAL-ACTIVE-BRIDGE DC-DC CONVERTER

Abstract — This chapter studies the general case of a multilevel DAB dc-dc converter with two N-level NPC legs on each side. A modulation pattern is proposed, which is inferred from the previously proposed modulations. The capacitor voltage balancing is analyzed, leading to a set of equations that guarantees null charge provided to the inner dc-link points with the transformer current fundamental component. Two closed-loop control schemes are proposed, which allow correcting any existing voltage unbalance. Closed-form generalized expressions defining the modulation parameters are inferred from the previously defined practical solutions.

5.1. Introduction

This chapter presents an extension to N levels of a DAB dc-dc converter built upon four N-level (NL) NPC legs. A generalized modulation strategy is proposed and characterized. The dc-link capacitor voltage balancing is analyzed and two generalized closed-loop voltage-balancing controls are proposed. The working range of the capacitor-voltage-balancing control is analyzed, and an alternative modulation and control scheme are proposed, in order to employ them when working outside the safe working range. The modulation parameter values are determined with a generalized set of simple and practical equations.

This chapter is organized as follows. Section 5.2 presents the converter topology. Section 5.3 presents the modulation strategy. Section 5.4 presents the extension to N levels of the capacitor-voltage-balancing strategy, defines two generalized control schemes, and studies the suitability of the system linearization performed to obtain a decoupled control scheme. The working range of such controls is also analyzed and an alternative modulation and control scheme are proposed. Section 5.5 proposes a practical solution for the modulation strategy based on the results of Chapter 2, Chapter 3, and Chapter 4. Finally, Section 5.6 outlines the conclusions.

5.2. Topology

Fig. 5.1 presents the proposed N-level NPC DAB dc-dc (NL-DAB) converter topology, which is an extension to an arbitrary number of levels of the previously studied 3L-DAB, 4L-DAB, and 5L-DAB. In the NL-DAB each dc-link has N voltage levels, obtained with a capacitor voltage divider composed by $M = N - 1$ capacitors, with connection points 1_z, 2_z, …, N_z and two NL-NPC legs (z_1 and z_2). As in the previous cases, phase legs z_1 and z_2 synthesize ac voltages v_{z1} and v_{z2}, respectively,

in order to generate transformer voltages v_z, and consequently, transfer power between both sides with i_z.

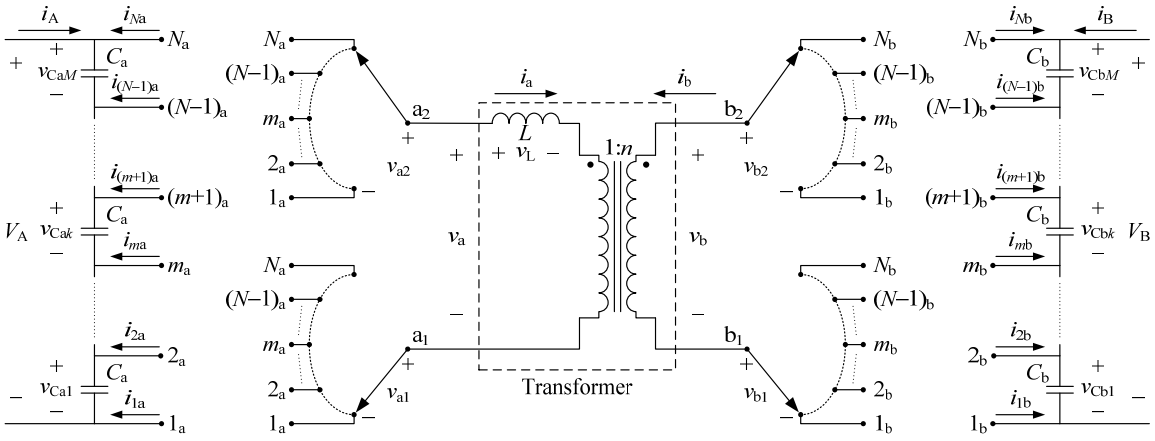


Fig. 5.1. Topology of the proposed NL-DAB dc-dc converter with phase legs a_1, a_2, b_1, and b_2 depicted as single-pole N-throw switches.

5.3. Modulation

Fig. 5.2 presents the modulation pattern for the *N*L-DAB. The two *N*-level legs of each *z*-side are controlled to produce the *N*-level staircase waveforms v_{z1} and v_{z2}, in order to synthesize a v_z transformer voltage waveform with $2N - 1$ voltage levels. The *N*L-DAB a-side switching-state sequence is shown in top of Fig. 5.2. The b-side switching-state sequence follows the same pattern.

The dwell times of the *N*L-DAB *z*-side switching states can be defined by $2M$ independent switching angles; i.e., α_{zi1}, α_{zi2}, …, α_{ziM}, and α_{zo1}, α_{zo2}, …, α_{zoM}, with

$$\begin{aligned} &-90° \le \alpha_{zi1} \le \alpha_{zi2} \le \ldots \le \alpha_{ziM} \le 90° \\ &-90° \le \alpha_{zo1} \le \alpha_{zo2} \le \ldots \le \alpha_{zoM} \le 90°. \end{aligned} \tag{5.1}$$

The present modulation allows maintaining $\overline{v}_z = 0, \forall z$, which guarantees a null steady-state transformer dc current and prevents the saturation of the transformer core, even when the dc-link capacitor voltages are not balanced. It also forces a symmetrical operation of both *z*-side full-bridge legs, as well as guaranteeing odd symmetry in v_a, v_b, v_L, and i_a waveforms, which is convenient for the capacitor voltage balancing.

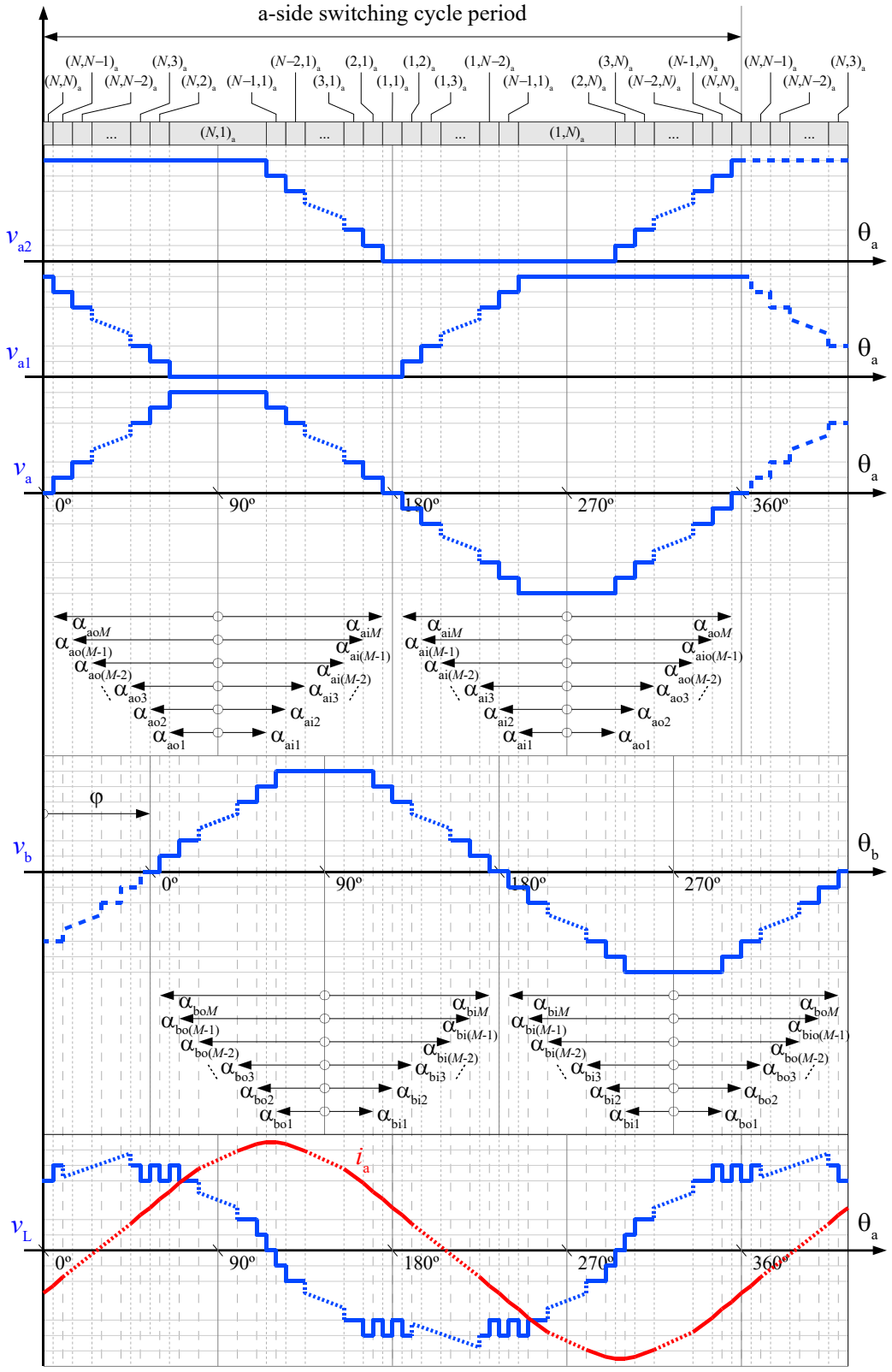


Fig. 5.2. Voltage waveforms v_{a1}, v_{a2}, v_a, v_b, and v_L, and current i_a for the generalized N-level modulation. Switching states for a-side are shown on top of the figure. All waveforms are plotted assuming $V_A = V_B/n$.

The $2M$ switching angles per side plus the phase shift, sum up to a total of $4M + 1$ DoF available to control the capacitor voltage balancing, the converter performance, and the power flow. If

$$\begin{aligned} \alpha_{zo1} &= \alpha_{zi1} = \alpha_{z1} \\ \alpha_{zo2} &= \alpha_{zi2} = \alpha_{z2} \\ &\vdots \\ \alpha_{zoM} &= \alpha_{ziM} = \alpha_{zM} \end{aligned} \tag{5.2}$$

and the dc-link capacitor voltages are balanced, then quarter-wave symmetry is guaranteed and even-order harmonics are eliminated in v_a, v_b, v_L, and i_a waveforms.

5.4. Capacitor voltage balancing

As demonstrated for the 3L-DAB, 4L-DAB, and 5L-DAB, a ML-DAB converter requires a means to guarantee the dc-link capacitor voltage balance, since these voltages typically collapse or reach values higher than intended. This section presents the generalization to an arbitrary number of levels of the constraints and control schemes needed to preserve the desired capacitor voltage balancing.

5.4.1. Control operating principle and control schemes

The currents injected into or drawn from the inner dc-link points of the dc-link (2_z, 3_z, …, M_z) alter the ratio between the M dc-link capacitor voltages. These currents are

$$\begin{aligned} i_{2z} &= S_{z12} \cdot i_z - S_{z22} \cdot i_z \\ i_{3z} &= S_{z13} \cdot i_z - S_{z23} \cdot i_z \\ &\vdots \\ i_{Mz} &= S_{z1M} \cdot i_z - S_{z2M} \cdot i_z, \end{aligned} \tag{5.3}$$

where S_{zjm} is equal to 1 when leg z_j is connected to inner dc-link point m_z and 0 otherwise.

Let us consider the effect of the fundamental component of i_z ($i_{z,1}$), as its amplitude is greater than each of the harmonic amplitudes. As done in previous chapters, $i_{z,1}$ is decoupled into $i^{p}_{z,1}$ and $i^{q}_{z,1}$ components, shown in Fig. 5.3 together with v_z. The shaded areas in Fig. 5.3 represent the electrical charge injected into (positive sign) or drawn from (negative sign) the z-side inner dc-link points by these currents, where each color refers to an inner dc-link point. Thanks to v_z odd symmetry, the sum of $i^{q}_{z,1}$ areas for each point is always zero. Hence, only $i^{p}_{z,1}$ can provide charge to the inner dc-link points. Moreover, thanks to the even symmetry of $i^{p}_{z,1}$ shaded areas along the switching

period, let us only consider half of this switching period. The per-unit charge provided to each inner dc-link point by $i^{p}_{z,1}$ during this period is

$$\begin{aligned} q_{2z} &= \sin(\alpha_{zo2}) - \sin(\alpha_{zo1}) - \left(\sin(\alpha_{ziM}) - \sin(\alpha_{zi(M-1)})\right) \\ q_{3z} &= \sin(\alpha_{zo3}) - \sin(\alpha_{zo2}) - \left(\sin(\alpha_{zi(M-1)}) - \sin(\alpha_{zi(M-2)})\right) \\ &\vdots \\ q_{Mz} &= \sin(\alpha_{zoM}) - \sin(\alpha_{zo(M-1)}) - \left(\sin(\alpha_{zi2}) - \sin(\alpha_{zi1})\right). \end{aligned} \tag{5.4}$$

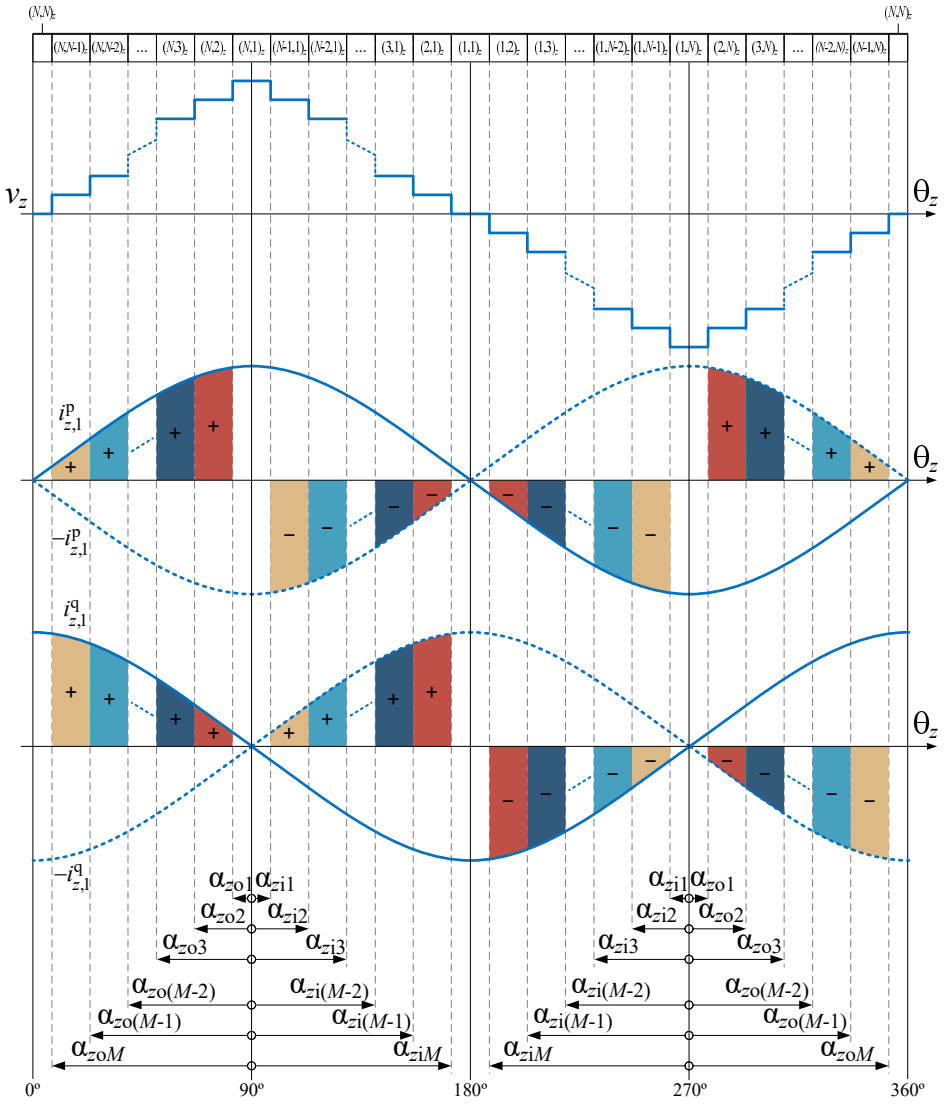


Fig. 5.3. Voltage v_z and the in-phase and in-quadrature components of i_z fundamental component ($i^{p}_{z,1}$ and $i^{q}_{z,1}$). The colored areas depict the charge injected into (+) or drawn from (–) inner dc-link points 2_z, 3_z, …, and M_z by $i^{p}_{z,1}$ and $i^{q}_{z,1}$.

Equation (5.4) can be expressed as

$$q_{(k+1)z} = \sin\left(\alpha_{zo(k+1)}\right) - \sin\left(\alpha_{zok}\right) - \left(\sin\left(\alpha_{zi(M+1-k)}\right) - \sin\left(\alpha_{zi(M-k)}\right)\right) \quad k \in \{1,2,\ldots,M-1\}. \tag{5.5}$$

If (5.2) is assumed for simplicity, then (5.4) verifies that $q_{2z} = -q_{Mz}$, $q_{3z} = -q_{(M-1)z}$, and so on, or, in a compact form, $q_{(k+1)z} = -q_{(M-k+1)z}\ \forall k$. Hence, when (5.2) is assumed, (5.5) results in

$$q_{(k+1)z} = -q_{(M-k+1)z} = \sin\left(\alpha_{z(k+1)}\right) - \sin\left(\alpha_{zk}\right) - \left(\sin\left(\alpha_{z(M-k+1)}\right) - \sin\left(\alpha_{z(M-k)}\right)\right) \quad k \in \left\{1,2,\ldots,\left\lfloor \frac{M}{2} \right\rfloor\right\}. \tag{5.6}$$

In order to keep a preexisting capacitor voltage balance, the charge provided by $i^{p}_{z,1}$ to each inner dc-link point must be zero. Hence, let us set (5.6) to zero, which results in

$$\sin\left(\alpha_{z(k+1)}\right) - \sin\left(\alpha_{zk}\right) - \sin\left(\alpha_{z(M-k+1)}\right) + \sin\left(\alpha_{z(M-k)}\right) = 0 \quad k \in \left\{1,2,\ldots,\left\lfloor \frac{M}{2} \right\rfloor\right\}. \tag{5.7}$$

In order to fulfill (5.7), we can proceed as in Chapter 4 and force

$$\begin{cases} \sin\left(\alpha_{z(r+1)}\right) = \sin\left(\alpha_{zr}\right) + \Delta_{zr} \\ \sin\left(\alpha_{z(M-r)}\right) = \sin\left(\alpha_{z(M-r+1)}\right) - \Delta_{zr} \end{cases} \qquad r \in \left\{1,2,\ldots,\left\lfloor \frac{M}{2} - 1 \right\rfloor\right\}, \tag{5.8}$$

where, in order to fulfill (5.1),

$$\begin{aligned} &\Delta_{zr} \geq 0 \quad \forall r \\ &\sum_{r=1}^{\left\lfloor \frac{M}{2}-1 \right\rfloor} \Delta_{zr} \leq \frac{\sin\left(\alpha_{zM}\right) - \sin\left(\alpha_{z1}\right)}{2}. \end{aligned} \tag{5.9}$$

With (5.8), the sines of the switching angles are defined as shown in Fig. 5.4, with two different patterns depending on N being odd [Fig. 5.4(a)] or even [Fig. 5.4(b)]. Fig. 5.4 shows that Δ_{zr} differences are distributed symmetrically with respect to $y = [\sin(\alpha_{z1}) + \sin(\alpha_{zM})]/2$.

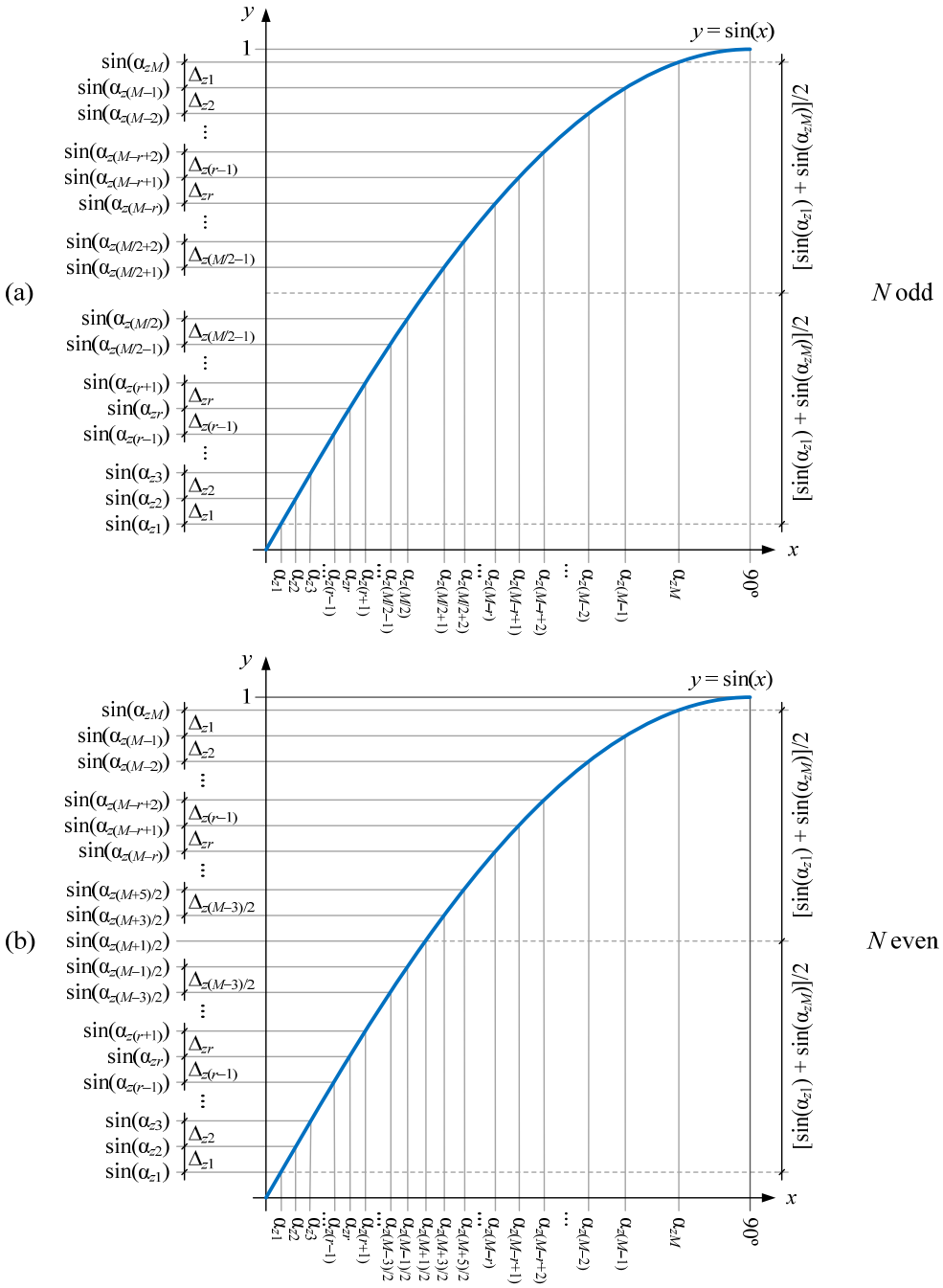


Fig. 5.4. Distribution of the sinus of the switching angles according to Δ_{zr}*. (a) Odd N. (b) Even N.*

It is noticeable that the maximum value that r takes in (5.8) is one unit less than k in (5.6) and (5.7), for the same value of M. This is because two especial cases arise when $k = \lfloor M/2 \rfloor$, where it is not necessary to define Δ_{zr}. The first case is when N is odd (even M) and $k = \lfloor M/2 \rfloor = M/2$, where (5.6) becomes

$$q_{\left(\frac{M}{2}+1\right)z} = \sin\left(\alpha_{z\left(\frac{M}{2}+1\right)}\right) - \sin\left(\alpha_{z\left(\frac{M}{2}\right)}\right) - \left(\sin\left(\alpha_{z\left(\frac{M}{2}+1\right)}\right) - \sin\left(\alpha_{z\left(\frac{M}{2}\right)}\right)\right) = 0, \tag{5.10}$$

meaning that the charge provided to the middle dc-link point is always null, regardless of the switching angle values. On the other hand, when N is even (odd M) and $k = \lfloor M/2 \rfloor = (M-1)/2$, then (5.7) becomes

$$2 \cdot \sin\left(\alpha_{z\left(\frac{M+1}{2}\right)}\right) - \sin\left(\alpha_{z\left(\frac{M-1}{2}\right)}\right) - \sin\left(\alpha_{z\left(\frac{M+3}{2}\right)}\right) = 0. \tag{5.11}$$

Therefore, similarly to the strategy followed in the 4L-DAB (even N), switching angle $\alpha_{z(M+1)/2}$ can be defined as a function of its two contiguous switching angles. Hence, difference Δ_{zr} for $r = \lfloor M/2 \rfloor$ is not necessary in both cases.

The difference between the number of variables and equations present in (5.8) (together with (5.11) when N is even), determines the number of existing independent variables. Such independent variables are DoF available to improve the performance of the converter. Table 5.1 shows the number of variables, equations, and independent variables in (5.8) and (5.11), as a function of N. Let us consider that variables Δ_{zr} are chosen to be part of the available independent variables. With such assumption, only two independent variables remain to be selected in all cases. These two remaining variables are selected to be α_{z1} and α_{zM}, following the same strategy than in the 4L-DAB and 5L-DAB practical solutions.

N	**Number of α_{zk} variables**		**Number of Δ_{zr} variables**		**Number of equations**		**Number of independent variables**
3	2		0		0		2
4	3		0		1		2
5	4		1		2		3
6	5		1		3		3
7	6		2		4		4
8	7	+	2	−	5	=	4
9	8		3		6		5
10	9		3		7		5
…	…		…		…		…
***N* odd**	M		$M/2 - 1$		$M - 2$		$M/2 + 1$
***N* even**	M		$(M - 3)/2$		$M - 2$		$M/2 + 1/2$

Table 5.1. Number of variables, equations, and independent variables, available for side z, as a function of N, derived from the expressions necessary to guarantee a null charge into z-side inner dc-link points with $i_{z,1}$.

In summary, in order to guarantee that a null charge is provided to the inner dc-link points within a switching cycle by $i_{z,1}$, expressions

$$\begin{cases} \sin\left(\alpha_{z(r+1)}\right) = \sin\left(\alpha_{zr}\right) + \Delta_{zr} \\ \sin\left(\alpha_{z(M-k)r}\right) = \sin\left(\alpha_{z(M-r+1)}\right) - \Delta_{zr} \end{cases} \quad \text{odd } N, \quad r \in \left\{1,2,\ldots,\frac{M}{2}-1\right\}$$

$$\begin{cases} \sin\left(\alpha_{z(r+1)}\right) = \sin\left(\alpha_{zr}\right) + \Delta_{zr} \\ \sin\left(\alpha_{z(M-r)}\right) = \sin\left(\alpha_{z(M-r+1)}\right) - \Delta_{zr} \\ \sin\left(\alpha_{z\left(\frac{M+1}{2}\right)}\right) = \frac{1}{2}\left(\sin\left(\alpha_{z\left(\frac{M-1}{2}\right)}\right) + \sin\left(\alpha_{z\left(\frac{M+3}{2}\right)}\right)\right) \end{cases} \quad \text{eveb } N, \ r \in \left\{1,2,\ldots,\frac{M-3}{2}\right\} \tag{5.12}$$

can be used for $N > 3$, where α_{z1}, α_{zM}, and Δ_{zr} $\forall r$ are independent variables that need to be previously defined. Also, (5.9) must be fulfilled.

However, when considering all i_z harmonics, as well as converter non-idealities, verifying (5.12) is not enough to maintain a preexisting capacitor voltage balance.

Consequently, a control action is needed which modifies the values of the inner and outer switching angles in order to inject a non-zero charge during a switching cycle and, ultimately, correct any capacitor voltage unbalance. This charge will only be provided by $i^{p}_{z,h}$, $h \in \{1,2,3,\ldots,\infty\}$, since the total charge provided by $i^{q}_{z,h}$, $h \in \{1,2,3,\ldots,\infty\}$ is always zero, owing to the odd symmetry of v_z. Moreover, most of the charge will be provided by $i^{p}_{z,1}$.

5.4.1.1. Full control scheme

Fig. 5.5 shows the generalization to N levels of the non-decoupled full control schemes proposed in previous chapters. The capacitor voltages, included in vector $\mathbf{v}_{Cz} = (v_{Cz1}, v_{Cz2}, \ldots, v_{CzM})^{T}$, are filtered by means of transfer function $\mathbf{H}_{filt}(s) = \text{diag}(H_{filt}(s), \ldots, H_{filt}(s))$. The filtered voltages vector is multiplied by matrix $\mathbf{Y}$ in order to obtain the unbalance variables, which indicate how much the voltage of an inner dc-link point has departed from its balanced value (when all capacitor voltages are equal). The unbalance variables are included in vector $\mathbf{y}_z = (y_{z2}, y_{z3}, \ldots, y_{zM})^{T}$. Matrix $\mathbf{Y}$, with an $(M-1) \times M$ size, is defined as

$$\mathbf{Y}=\begin{pmatrix} 1 & -\frac{1}{M-1} & & \cdots & & -\frac{1}{M-1} \\ \frac{1}{2} & \frac{1}{2} & -\frac{1}{M-2} & & \cdots & -\frac{1}{M-2} \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & -\frac{1}{M-3} & \cdots & -\frac{1}{M-3} \\ \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ \frac{1}{M-1} & & \cdots & & \frac{1}{M-1} & -1 \end{pmatrix}. \tag{5.13}$$

Vector $\mathbf{y}_z$ is subtracted from the vector of command values ($\mathbf{y}^*_z$) in order to obtain the error vector ($\mathbf{e}_z$). A value $e_{zm} > 0$ means that the average value among v_{Cz1}, …, $v_{Cz(m-1)}$ is below its desired value and the average value among v_{Czm}, …, v_{CzM} is above its desired value. Therefore, a control action is required that injects charge into m_z in order to increase v_{Cz1}, …, $v_{Cz(m-1)}$ and decrease v_{Czm}, …, v_{CzM}; i.e., increase y_{zm}.

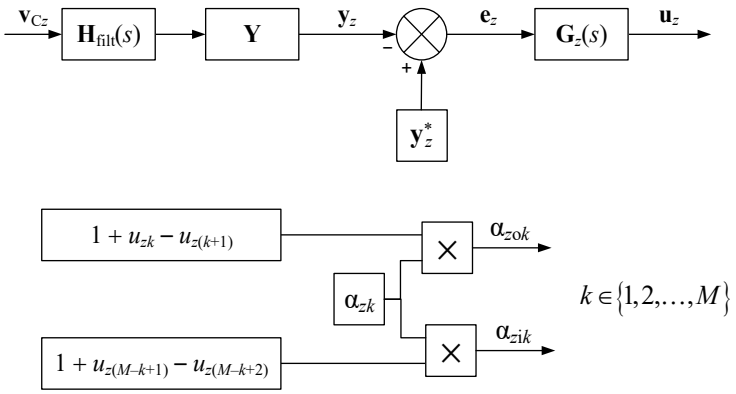


Fig. 5.5. Full control scheme for the NL-DAB z-side capacitor voltage balancing. Note that $u_{z1} = u_{z(M+1)} = 0$.

Without loss of generality, let us assume that power is transferred from side a to side b, thus Fig. 5.6 waveforms correspond to side a. In such case, $e_{zm} \neq 0$ can be corrected by modifying the switching angles as described in Table 5.2. The rationale of Table 5.2 can be better understood by looking at Fig. 5.6, which shows the charge provided to inner dc-link points $(m-1)_z$, m_z, and $(m+1)_z$, as well as the switching angles that modify such charges. For example, when $e_{am} > 0$, an average positive charge has to be injected into m_a, which is accomplished by decreasing switching angles pair $\{\alpha_{ao(m-1)}, \alpha_{ai(M-m+2)}\}$ and increasing $\{\alpha_{aom}, \alpha_{ai(M-m+1)}\}$. This control action is determined by control variable u_{am}. Each control variable, contained in vector $\mathbf{u}_z$, is obtained by multiplying $\mathbf{e}_z$ with matrix $\mathbf{G}_z(s) = \text{diag}(G_{z2}(s), G_{z3}(s), \ldots, G_{zM}(s))$, the compensator transfer function matrix.

z	*m*	e_{zm}	Chrg. sign to prov.	$\{\alpha_{zo1}, \alpha_{ziM}\}$	$\{\alpha_{zo2}, \alpha_{zi(M-1)}\}$	$\{\alpha_{zo3}, \alpha_{zi(M-2)}\}$	…	$\{\alpha_{zo(m-2)}, \alpha_{zi(M-m+3)}\}$	$\{\alpha_{zo(m-1)}, \alpha_{zi(M-m+2)}\}$	$\{\alpha_{zom}, \alpha_{zi(M-m+1)}\}$	$\{\alpha_{zo(m+1)}, \alpha_{zi(M-m)}\}$	…	$\{\alpha_{zo(M-2)}, \alpha_{zi3}\}$	$\{\alpha_{zo(M-1)}, \alpha_{zi2}\}$	$\{\alpha_{zoM}, \alpha_{zi1}\}$
a	2	+ / –	+ / –	↓ / ↑	↑ / ↓										
	3	+ / –	+ / –		↓ / ↑	↑ / ↓									
	⋮	⋮	⋮			⋮	⋱								
	$m-1$	+ / –	+ / –					↓ / ↑	↑ / ↓						
	m	+ / –	+ / –						↓ / ↑	↑ / ↓					
	$m+1$	+ / –	+ / –							↓ / ↑	↑ / ↓				
	⋮	⋮	⋮								⋮	⋱			
	$M-1$	+ / –	+ / –										↓ / ↑	↑ / ↓	
	M	+ / –	+ / –											↓ / ↑	↑ / ↓
b	2	+ / –	+ / –	↑ / ↓	↓ / ↑										
	3	+ / –	+ / –		↑ / ↓	↓ / ↑									
	⋮	⋮	⋮			⋮	⋱								
	$m-1$	+ / –	+ / –					↑ / ↓	↓ / ↑						
	m	+ / –	+ / –						↑ / ↓	↓ / ↑					
	$m+1$	+ / –	+ / –							↑ / ↓	↓ / ↑				
	⋮	⋮	⋮								⋮	⋱			
	$M-1$	+ / –	+ / –										↑ / ↓	↓ / ↑	
	M	+ / –	+ / –											↑ / ↓	↓ / ↑

Table 5.2. Switching angles change needed to correct a voltage unbalance on the a-side and b-side inner dc-link points, depending on the sign of the error variables, and according to Fig. 5.3 and Fig. 5.6.

In agreement with Table 5.2, each inner and outer switching is modified by the control variables according to

$$\begin{cases} \alpha_{zok} = \alpha_{zk}\left(1 + u_{zk} - u_{z(k+1)}\right) \\ \alpha_{zik} = \alpha_{zk}\left(1 + u_{z(M-k+1)} - u_{z(M-k+2)}\right) \end{cases} \qquad k \in \{1,2,\ldots,M\}, \quad u_{z1} = u_{z(M+1)} = 0. \tag{5.14}$$

Regarding compensators $G_{zm}(s)$, the sign of $k_{P,zm}$ is subject to the same rationale discussed for the 3L-DAB (Section 2.4.1.1). As in the individual cases of the 3L-DAB, 4L-DAB, and 5L-DAB full control schemes, the generalized case presented in Fig. 5.5 takes advantage of all the available switching angles to correct any preexisting voltage unbalance.

As seen in Table 5.2, all switching angles pairs, except for $\{\alpha_{ao1}, \alpha_{aiM}\}$ and $\{\alpha_{aoM}, \alpha_{ai1}\}$, are modified by two control variables. The reason is that each switching angle pair, when modified, alters simultaneously the charge provided to two contiguous inner dc-link points. Moreover, the charge

provided to both inner dc-link points is modified in opposite directions; i.e., increases while the other decreases.

Additionally, each control variable modifies two switching angles pairs, which in turn affect the charge provided to three inner dc-link points (as seen in Table 5.2 and Fig. 5.6). For example, u_{zm} modifies $\{\alpha_{zo(m-1)}, \alpha_{zi(M-m+2)}\}$ and $\{\alpha_{zom}, \alpha_{zi(M-m+1)}\}$ in order to regulate the charge provided to m_z, but simultaneously modifies the charge provided to $(m-1)_z$ and $(m+1)_z$, the inner dc-link points contiguous to m_z.

Hence, the proposed full control scheme presents a coupling between the control loops that regulate contiguous error variables. This coupling can be detrimental to the control performance. Thus, a means to reverse such coupling is of interest.

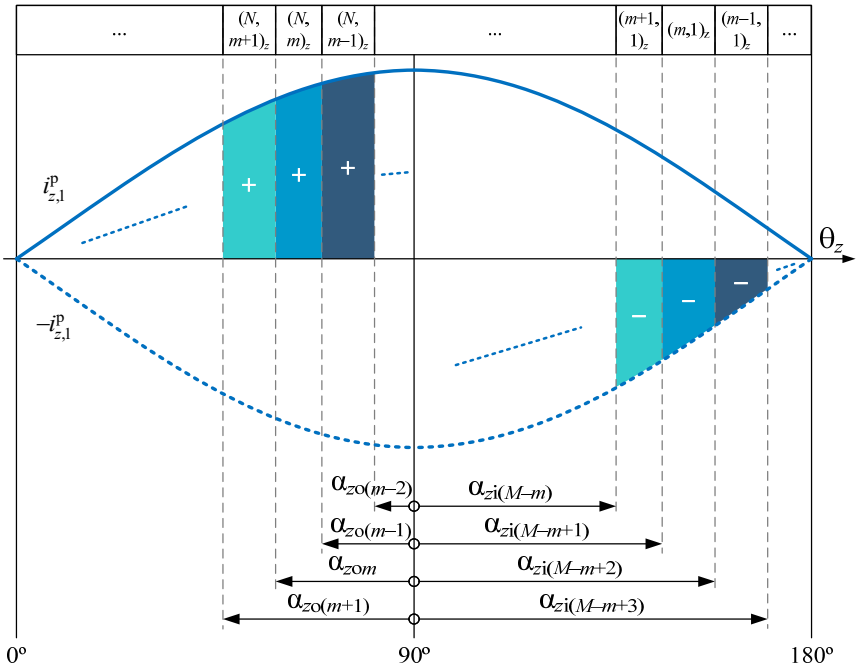


Fig. 5.6. Depiction of the charge (colored areas) provided by $i^p_{z,1}$ to inner dc-link points $(m-1)_z$, m_z, and $(m+1)_z$. Symbols + and – indicate if the charge is injected into or drawn from the inner dc-link points, respectively.

5.4.1.2. Full control scheme with decoupling

Analogous to the 4L-DAB and 5L-DAB full control schemes, the *N*L-DAB full control scheme of Fig. 5.5 presents two degrees of coupling; First, the coupling due to the distribution, among the dc-link capacitors, of the current injected into an arbitrary inner dc-link point (first described in Section 3.4.1.2). Second, as described in Section 5.4.1.1, the coupling inherent to the full control

scheme topology, where the regulation of a given inner dc-link point error variable alters simultaneously the charge provided to its contiguous inner dc-link points.

Therefore, it is necessary to derive the coupling matrix present in the transfer function, with the objective of decoupling the control problem. Applying a decoupling matrix will allow having a control scheme where the control variables outputted by the controller (u'_{zm}) only affect its corresponding unbalance variable; i.e., u'_{zm} will only affect y_{zm}.

For the present study, the same assumptions as in Section 3.4.1 are made; i.e., V_Z is kept constant, all capacitors are assumed to be of equal capacitance, and switching angles α_{zk} are considered to be constant during a switching cycle.

Let us suppose that a current I_{mz} is injected into inner dc-link point m_z. Such current will flow through the bottom capacitors with a proportion of $(M - m + 1)/M$ and through the upper capacitors with a proportion of $(m - 1)/M$. The capacitor voltages will vary as

$$\Delta v_{Czm} = \frac{1}{s \cdot C_z} \cdot \left[\sum_{j=m+1}^{M} I_{jz} \left(\frac{M-j+1}{M} \right) - \sum_{j=2}^{m} I_{jz} \left(\frac{j-1}{M} \right) \right] \quad m \in \{1,2,\ldots,M\}, \tag{5.15}$$

or in a matrix form

$$\Delta \mathbf{v}_{Cz} = \frac{1}{s \cdot C_z} \mathbf{A} \mathbf{i}_z, \tag{5.16}$$

where $\Delta \mathbf{v}_{Cz} = (\Delta v_{Cz1}, \Delta v_{Cz2}, \ldots, \Delta v_{CzM})^{\mathrm{T}}$, $\mathbf{i}_z = (I_{2z}, I_{3z}, \ldots, I_{Mz})^{\mathrm{T}}$, and $\mathbf{A}$ is an $M \times (M-1)$ matrix, defined as

$$\mathbf{A} = \begin{pmatrix} \frac{M-1}{M} & \frac{M-2}{M} & \frac{M-3}{M} & & \cdots & & & \frac{1}{M} \\ -\frac{1}{M} & \frac{M-2}{M} & \frac{M-3}{M} & & \cdots & & & \frac{1}{M} \\ -\frac{1}{M} & -\frac{2}{M} & \frac{M-3}{M} & & \cdots & & & \frac{1}{M} \\ \vdots & \vdots & \vdots & & & & & \vdots \\ -\frac{1}{M} & -\frac{2}{M} & -\frac{3}{M} & \cdots & -\frac{m-1}{M} & \frac{M-m}{M} & \frac{M-m-1}{M} & \cdots & \frac{1}{M} \\ \vdots & \vdots & \vdots & & & & & & \vdots \\ -\frac{1}{M} & -\frac{2}{M} & -\frac{3}{M} & & \cdots & & & -\frac{M-1}{M} \end{pmatrix}. \tag{5.17}$$

The variation of the unbalance variables can be computed with

$$\Delta \mathbf{y}_z = \frac{1}{s \cdot C_z} \mathbf{C}_{NL} \mathbf{i}_z, \tag{5.18}$$

where $\Delta \mathbf{y}_z = (\Delta y_{z2}, \Delta y_{z3}, \ldots, \Delta y_{zM})^{\mathrm{T}}$ and $\mathbf{C}_{NL}$ is the matrix, of size $(M-1) \times (M-1)$, that characterizes the coupling between the currents provided to the N-level dc-link inner points and the unbalance variables, and is defined as

$$\mathbf{C}_{NL} = \mathbf{YA} = \begin{pmatrix} 1 & \cdots & \frac{3}{M-1} & \frac{2}{M-1} & \frac{1}{M-1} \\ \frac{1}{2} & 1 & \vdots & \vdots & \vdots \\ \frac{1}{3} & \frac{2}{3} & \ddots & \frac{2}{3} & \frac{1}{3} \\ \vdots & \vdots & \vdots & 1 & \frac{1}{2} \\ \frac{1}{M-1} & \frac{2}{M-1} & \frac{3}{M-1} & \cdots & 1 \end{pmatrix}. \tag{5.19}$$

The plant transfer function, with $\mathbf{i}_z$ as input vector and $\boldsymbol{y}_z$ as output vector, is defined as

$$\mathbf{y}_z = \frac{1}{C_z \cdot s} \cdot \mathbf{C}_{NL} \mathbf{i}_z. \tag{5.20}$$

Considering only the fundamental component of i_z, the currents provided to the inner dc-link points, within a switching cycle, and as a function of the control variables, are defined as

$$\begin{aligned} & I_{mz,1}\left(u_{z(m-1)}, u_{zm}, u_{z(m+1)}\right) = \\ & = \frac{I_{z,1}^{\mathrm{p}}}{\pi}\left[\sin\left(\alpha_{zom}\right) - \sin\left(\alpha_{zo(m-1)}\right) - \sin\left(\alpha_{zi(M-m+2)}\right) + \sin\left(\alpha_{zi(M-m+1)}\right)\right] \\ & = \Big[\sin\left(\alpha_{zm}\left(1 + u_{zm} - u_{z(m+1)}\right)\right) - \sin\left(\alpha_{z(m-1)}\left(1 + u_{z(m-1)} - u_{zm}\right)\right) \\ & \quad - \sin\left(\alpha_{z(M-m+2)}\left(1 + u_{z(m-1)} - u_{zm}\right)\right) + \sin\left(\alpha_{z(M-m+1)}\left(1 + u_{zm} - u_{z(m+1)}\right)\right)\Big]. \end{aligned} \tag{5.21}$$

Following the same procedure of Section 3.4.1, let us linearize $I_{mz,1}(u_{z(m-1)},u_{zm},u_{z(m+1)})$ at $u_{z(m-1)} = u_{zm} = u_{z(m+1)} = 0$

$$
\begin{aligned}
&I_{mz,1}^{\text{lin}}\left(u_{z(m-1)},u_{zm},u_{z(m+1)}\right)= \\
&= I_{mz,1}\left(0,0,0\right)+\left[\left.\frac{\delta I_{mz,1}}{\delta u_{z(m-1)}}\right|_{\substack{u_{z(m-1)}=0\\u_{zm}=0\\u_{z(m+1)}=0}}\right]\cdot u_{z(m-1)}+\left[\left.\frac{\delta I_{mz,1}}{\delta u_{zm}}\right|_{\substack{u_{z(m-1)}=0\\u_{zm}=0\\u_{z(m+1)}=0}}\right]\cdot u_{zm}+\left[\left.\frac{\delta I_{mz,1}}{\delta u_{z(m+1)}}\right|_{\substack{u_{z(m-1)}=0\\u_{zm}=0\\u_{z(m+1)}=0}}\right]\cdot u_{z(m+1)} \\
&= I_{mz,1}\left(0,0,0\right)+e_{NL}\cdot\left[a_{NL}\left(m\right)\cdot u_{z(m-1)}+b_{NL}\left(m\right)\cdot u_{zm}+c_{NL}\left(m\right)\cdot u_{z(m+1)}\right]
\end{aligned}
\tag{5.22}
$$

where

$$
\begin{aligned}
a_{NL}\left(m\right)&=-\alpha_{z(m-1)}\cdot\cos\left(\alpha_{z(m-1)}\right)+\alpha_{z(M-m+2)}\cdot\cos\left(\alpha_{z(M-m+2)}\right) \\
b_{NL}\left(m\right)&=\alpha_{zm}\cdot\cos\left(\alpha_{zm}\right)+\alpha_{z(m-1)}\cdot\cos\left(\alpha_{z(m-1)}\right)+\alpha_{z(M-m+2)}\cdot\cos\left(\alpha_{z(M-m+2)}\right) \\
&\quad+\alpha_{z(M-m+1)}\cdot\cos\left(\alpha_{z(M-m+1)}\right) \\
c_{NL}\left(m\right)&=-\alpha_{zm}\cdot\cos\left(\alpha_{zm}\right)+\alpha_{z(M-m+1)}\cdot\cos\left(\alpha_{z(M-m+1)}\right) \\
e_{NL}&=\frac{I_{z,1}^{\text{p}}}{\pi},
\end{aligned}
\tag{5.23}
$$

switching angles are in radians, and $I_{mz,1}(0,0,0) = 0$ since (5.12) is fulfilled. Alternatively, in a matrix form

$$
\mathbf{i}_{z,1}^{\text{lin}}=e_{NL}\cdot\mathbf{D}_{NL}\mathbf{u}_z=e_{NL}\cdot\begin{pmatrix}
b_{NL}\left(2\right) & c_{NL}\left(2\right) & 0 & 0 & \cdots & 0 \\
a_{NL}\left(3\right) & b_{NL}\left(3\right) & c_{NL}\left(3\right) & 0 & \cdots & 0 \\
0 & a_{NL}\left(4\right) & b_{NL}\left(4\right) & c_{NL}\left(4\right) & \cdots & 0 \\
\vdots & \vdots & \vdots & \vdots & & \vdots \\
0 & 0 & 0 & 0 & a_{NL}\left(M\right) & b_{NL}\left(M\right)
\end{pmatrix}\mathbf{u}_z. \tag{5.24}
$$

Finally, by substituting $\mathbf{i}_z$ on (5.20) with $\mathbf{i}^{\text{lin}}{}_{z,1}$ in (5.24), the system transfer function, where $\mathbf{u}_z$ is the input vector and $\mathbf{y}_z$ is the output vector, can be obtained

$$
\mathbf{y}_z=\frac{e_{NL}}{C_z\cdot s}\cdot\mathbf{C}_{NL}\mathbf{D}_{NL}\mathbf{u}_z=\frac{e_{NL}}{C_z\cdot s}\cdot\mathbf{E}_{NL}\mathbf{u}_z, \tag{5.25}
$$

where $\mathbf{E}_{NL}$ is the coupling matrix.

With the coupling matrix, it is easy to decouple the control of the system by simply multiplying the vector of compensator output control variables ($\mathbf{u}'_z$) by the inverse of the coupling matrix; i.e., the decoupling matrix ($\mathbf{E}^{-1}{}_{NL}$). Fig. 5.7 shows the decoupled control scheme.

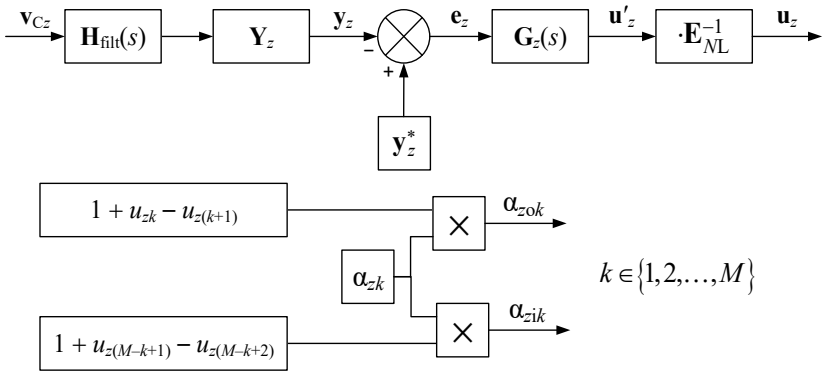


Fig. 5.7. Full control scheme for the NL-DAB z-side capacitor voltage balancing with decoupling. Note that $u_{z1} = u_{z(M+1)} = 0$.

5.4.1.3. *Linearity of the capacitor voltage balancing control system*

This section studies the suitability of the linearization of the equations defining the average currents provided to the inner dc-link points as a function of the control variables. Such linearization is performed to determine the existing coupling mechanism in the system transfer function.

To study the linearity of the plant, let us examine the graphic shown in Fig. 5.8. In this graphic, the red solid area illustrates the charge provided to an arbitrary inner dc-link point (m_z) by current $i^p_{z,1}$. This charge is defined by adjacent switching angles $\alpha_{z(k-1)}$ and α_{zk}. Let us consider that when the control scheme adjusts control variable u_{zm} to regulate the voltage at m_z, switching angle α_{zk} is modified from initial value $\alpha_{zk,i}$ to final value $\alpha_{zk,f} = \alpha_{zk,i} \cdot (1 + u_{zm})$.

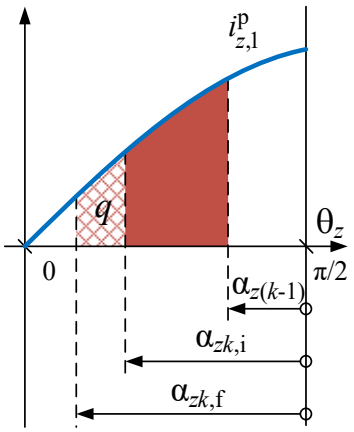


Fig. 5.8. First quarter wave period of current $i^p_{z,1}$. *The solid red area depicts the charge provided to a given inner dc-link point when no capacitor-voltage-balancing control action is performed. The red striped area depicts the additional charge provided to the same inner point when a control action is performed.*

The additional charge (q) provided to m_z in this control action is represented as a red striped area. The value of q, as a function of u_{zm}, is

$$q(u_{zm}) = \int_{\pi/2-\alpha_{zk,i}}^{\pi/2-\alpha_{zk,f}} I_{z,1}^{p} \cdot \sin(\theta_z)\, d\theta_z = I_{z,1}^{p} \cdot \left[\sin\left(\alpha_{zk,i} \cdot (1+u_{zm})\right) - \sin(\alpha_{zk,i})\right], \tag{5.26}$$

where $\alpha_{zk,i}$ is in radians, and $q(u_{zm})$ is represented in Fig. 5.9 for two different values of $\alpha_{zk,i}$ (u_{zm} span is defined such that $\alpha_{zk,f} = [-\pi/2,\pi/2]$). It can be easily observed that $q(u_{zm})$ is not a linear function as it is a sine function. As shown in previous chapters, to study the system transfer function coupling, $q(u_{zm})$ is linearized at $u_{zm} = 0$ (dashed lines in Fig. 5.9) for a given value of $\alpha_{zk,i}$. This linearized function is

$$q_{\text{lin}}(u_{zm}) = q(0) + u_{zm} \cdot \left.\frac{dq(u_{zm})}{du_{zm}}\right|_{u_{zm}=0} = I_{z,1}^{p} \cdot \alpha_{zk,i} \cdot \cos(\alpha_{zk,i}) \cdot u_{zm}\,. \tag{5.27}$$

The error defined by $q_{\text{lin}}(u_{zm})$ and $q(u_{zm})$ determines the suitability of the linearization; i.e., the less the error the better suitability. When u_{zm} departs from 0, or in other words, when $|\alpha_{zk,f} - \alpha_{zk,i}|$ increases, the error also increases. When $\alpha_{zk,i}$ is close to $\pi/2$ [Fig. 5.9(a)] or $-\pi/2$, the error is small for a small range of u_{zm}. When $\alpha_{zk,i}$ is close to 0 [Fig. 5.9(b)] the error is small for a more extended range.

Therefore, the linearization performed to determine the plant transfer function coupling has a better suitability for a large range of u_{zm} at $\alpha_{zk,i}$ values close to zero, and for a small range of u_{zm} at $\alpha_{zk,i}$ values close to 90º.

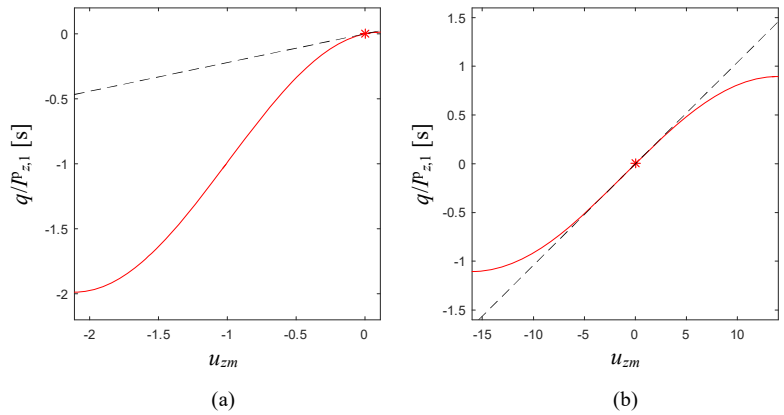


Fig. 5.9. Additional charge provided to inner dc-link point m_z divided by $I^{p}_{z,1}$ as a function of control variable u_{zm}. The striped line depicts the linearized function at $u_{sm} = 0$. (a) For $\alpha_{zk,i} = 9\pi/20$ (81º). (b) For $\alpha_{zk,i} = \pi/30$ (6º)

5.4.2. Effective working range of the capacitor-voltage-balancing control

The capacity to correct any capacitor voltage unbalance relies on $i^{p}_{z,1}$. There are cases where the charge provided by $i^{p}_{z,1}$ is not large enough to counteract the charge causing the unbalance, which may have its origin in converter non-idealities or in i_z harmonics. These cases occur when $I^{p}_{z,1}$ value is very low; i.e., when the phase shift between $v_{z,1}$ and $i_{z,1}$ (β_z) is close to ±90º.

The phasor diagrams of Fig. 5.10 show two examples where $|\beta_z| \approx 90º$. For instance, Fig. 5.10(a) depicts phasors $\mathbf{V}_{z,1}$ and $\mathbf{I}_{z,1}$ for d << 1 and at a low phase shift value. It can be observed that both β_a and β_b are close to -90º and 90º, respectively. Fig. 5.10(b) depicts the case where d << 1 and $\varphi = 90º$, resulting in $\beta_a \approx -90º$ and $\beta_b \approx -180º$. In this case, only the a-side capacitor-voltage-balancing control will face difficulties when regulating the capacitor voltages.

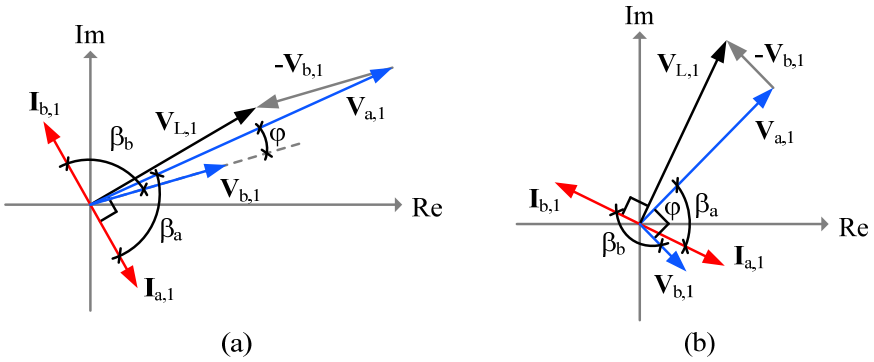


Fig. 5.10. Phasor diagrams showing the phase shift between each transformer side voltage and current fundamental components when d << 1. (a) φ = 8º. (b) φ = 90º.

A more comprehensive analysis can be done by plotting β_a and β_b as a function of φ and *d* (Fig. 5.11). It can be observed that the control of both sides will face difficulties when $\varphi \approx 0º$ $\forall d \neq 1$. At $\varphi > 0º$ only the control employed on the converter side with a greater V_Z will face difficulties, e.g., a-side control when d << 1 and b-side control when d >> 1.

Consequently, for a proper performance of the converter, extremely high and low *d* values should be avoided. In addition, a minimum phase shift value should be guaranteed. When changing the power direction flow (φ changes its sign), a fast enough transition should be realized, in order to avoid staying at low φ values for an extended time.

It should be mentioned, however, that during the experimental tests, the aforementioned adverse performance at $\varphi \approx 0º$ has not been observed. No experiments have been realized at $d << 1$ or $d >> 1$.

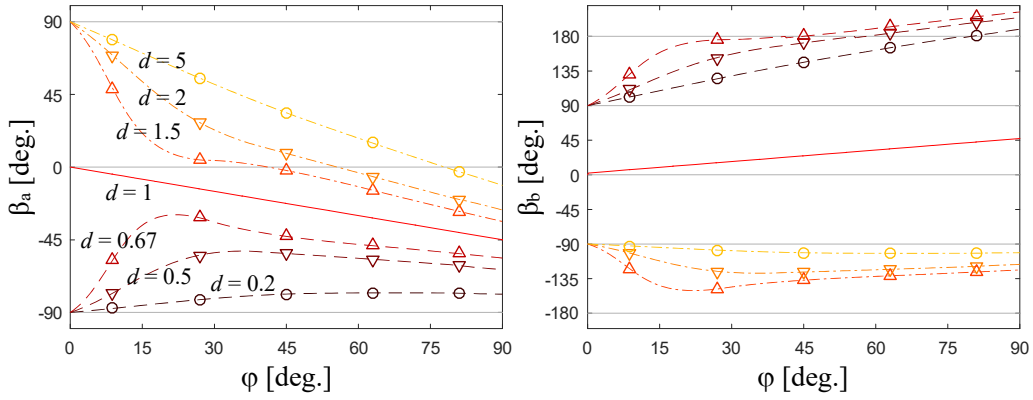


Fig. 5.11. Phase shift between $v_{a,1}$ and $i_{a,1}$ (β_a) and between $v_{b,1}$ and $i_{b,1}$ (β_b) as a function of φ, for different values of d, and employing the 3L-DAB practical solution of Fig. 2.12(d).

5.4.2.1. Alternative modulation and control scheme

A solution to regain the capability of controlling the capacitor voltage balancing when the described worst-case conditions are met, is to employ an alternative modulation and control scheme that allows regulating the charge provided to the inner dc-link points with the in-quadrature current, since $|I^{q}_{z,1}| >> |I^{p}_{z,1}|$ when operating outside of the effective working range of the regular control scheme. Fig. 5.12 shows the aforementioned alternative modulation scheme for the 5L-DAB case. The switching sequence is the same as the regular modulation scheme (Fig. 4.4), while eight new switching angle variables are introduced.

This new modulation scheme does not guarantee any kind of symmetry on v_z within a switching cycle. Therefore, to guarantee a null dc component on v_z,

$$v_{Cz1}\cdot\sigma_{z1}+v_{Cz2}\cdot\sigma_{z2}+v_{Cz3}\cdot\sigma_{z3}+v_{Cz4}\cdot\sigma_{z4}=0 \tag{5.28}$$

must be fulfilled, where

$$\begin{aligned}
\sigma_{z1}&=\alpha_{zlo1}+\alpha_{zli4}-\alpha_{zro1}-\alpha_{zri4}\\
\sigma_{z2}&=\alpha_{zlo2}+\alpha_{zli3}-\alpha_{zro2}-\alpha_{zri3}\\
\sigma_{z3}&=\alpha_{zlo3}+\alpha_{zli2}-\alpha_{zro3}-\alpha_{zri2}\\
\sigma_{z4}&=\alpha_{zlo4}+\alpha_{zli1}-\alpha_{zro4}-\alpha_{zri1}.
\end{aligned} \tag{5.29}$$

Nevertheless, quarter-wave symmetry can be guaranteed if

$$\begin{aligned}
\alpha_{z\mathrm{lo}1} &= \alpha_{z\mathrm{li}1} = \alpha_{z\mathrm{ro}1} = \alpha_{z\mathrm{ri}1} = \alpha_{z1} \\
\alpha_{z\mathrm{lo}2} &= \alpha_{z\mathrm{li}2} = \alpha_{z\mathrm{ro}2} = \alpha_{z\mathrm{ri}2} = \alpha_{z2} \\
\alpha_{z\mathrm{lo}3} &= \alpha_{z\mathrm{li}3} = \alpha_{z\mathrm{ro}3} = \alpha_{z\mathrm{ri}3} = \alpha_{z3} \\
\alpha_{z\mathrm{lo}4} &= \alpha_{z\mathrm{li}4} = \alpha_{z\mathrm{ro}4} = \alpha_{z\mathrm{ri}4} = \alpha_{z4}.
\end{aligned} \tag{5.30}$$

On Fig. 5.12, only $i^{\mathrm{q}}_{z,1}$ is depicted since it is considered that $I^{\mathrm{p}}_{z,1} \approx 0$. As in previous cases, each shaded area on Fig. 5.12 depicts the charge provided to the z-side inner dc-link points by $i^{\mathrm{q}}_{z,1}$. If (5.30) is met, then the total charge provided by $i^{\mathrm{q}}_{z,1}$ is zero. However, overriding v_z quarter-wave symmetry let us control the charge provided to individual inner dc-link points in order to correct any capacitor voltage unbalance.

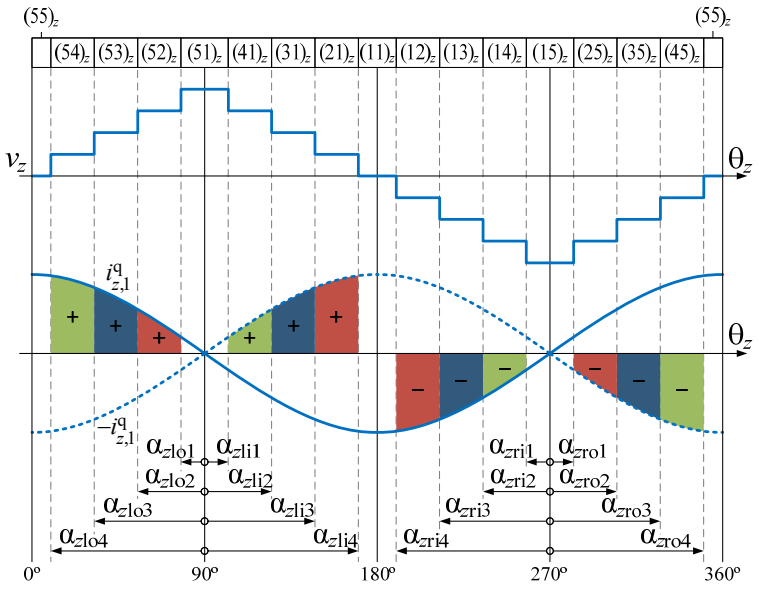


Fig. 5.12. Novel switching angle variables in the alternative modulation scheme. The red, blue, and green areas depict the charge injected into (+) or drawn from (–) inner dc-link points 2_z, 3_z, and 4_z, respectively, by $i^{q}_{z,1}$.

Without loss of generality, let us assume that power is transferred from side a to side b, and that variables y_{zm}, e_{zm}, and u_{zm} are computed as in the control scheme of Fig. 4.5. Then, any $e_{zm} \neq 0$ can be corrected by modifying the switching angle values according to Table 5.3. Different to the previous proposed control schemes, let us define each switching angle on Fig. 5.12 as the sum of its associated initial switching angle (α_{zk}) and required control variable(s), according to Table 5.3, resulting in

$$\begin{cases} \alpha_{zlo1} = \alpha_{z1} - u_{z2} \\ \alpha_{zro1} = \alpha_{z1} + u_{z2} \\ \alpha_{zli4} = \alpha_{z4} + u_{z2} \\ \alpha_{zri4} = \alpha_{z4} - u_{z2} \end{cases} \begin{cases} \alpha_{zlo2} = \alpha_{z2} + u_{z2} - u_{z3} \\ \alpha_{zro2} = \alpha_{z2} - u_{z2} + u_{z3} \\ \alpha_{zli3} = \alpha_{z3} - u_{z2} + u_{z3} \\ \alpha_{zri3} = \alpha_{z3} + u_{z2} - u_{z3} \end{cases} \begin{cases} \alpha_{zli2} = \alpha_{z2} - u_{z3} + u_{z4} \\ \alpha_{zri2} = \alpha_{z2} + u_{z3} - u_{z4} \\ \alpha_{zlo3} = \alpha_{z3} + u_{z3} - u_{z4} \\ \alpha_{zro3} = \alpha_{z3} - u_{z3} + u_{z4} \end{cases} \begin{cases} \alpha_{zli1} = \alpha_{z1} - u_{z4} \\ \alpha_{zri1} = \alpha_{z1} + u_{z4} \\ \alpha_{zlo4} = \alpha_{z4} + u_{z4} \\ \alpha_{zro4} = \alpha_{z4} - u_{z4} \end{cases}, \forall z. \quad (5.31)$$

If the compensator transfer function of (2.14) is employed to compute each u_{zm} from e_{zm}, then, when power is transferred from side a to side b, $k_{P,am} > 0$ $\forall m$ and $k_{P,bm} < 0$ $\forall m$. When power is transferred from side b to side a, the sign of each $k_{P,zm}$ is changed.

With such definitions, $\sigma_{zk} = 0$ $\forall z,k$ regardless of the initial switching angles and control variables values, and hence, a null v_z dc component is always guaranteed.

z	*m*	e_{zm}	Charge sign to provide	$\{\alpha_{zlo1}, \alpha_{zri4}\}$	$\{\alpha_{zli4}, \alpha_{zro1}\}$	$\{\alpha_{zlo2}, \alpha_{zri3}\}$	$\{\alpha_{zli3}, \alpha_{zro2}\}$	$\{\alpha_{zlo3}, \alpha_{zri2}\}$	$\{\alpha_{zli2}, \alpha_{zro3}\}$	$\{\alpha_{zlo4}, \alpha_{zri1}\}$	$\{\alpha_{zli1}, \alpha_{zro4}\}$
a	2	+ / –	+ / –	↓ / ↑	↑ / ↓	↑ / ↓	↓ / ↑				
	3	+ / –	+ / –			↓ / ↑	↑ / ↓	↑ / ↓	↓ / ↑		
	4	+ / –	+ / –					↓ / ↑	↑ / ↓	↑ / ↓	↓ / ↑
b	2	+ / –	+ / –	↑ / ↓	↓ / ↑	↓ / ↑	↑ / ↓				
	3	+ / –	+ / –			↑ / ↓	↓ / ↑	↓ / ↑	↑ / ↓		
	4	+ / –	+ / –					↑ / ↓	↓ / ↑	↓ / ↑	↑ / ↓

Table 5.3. Sign of the charge to be provided and switching angles change needed to correct a voltage unbalance at inner dc-link point m_z, depending on the sign of e_{zm}, and according to Fig. 5.12.

5.5. Definition of the modulation parameter values

This section presents a set of equations to define the *N*L-DAB modulation parameter values, specifically, switching angles α_{zk} $\forall z,k$ as a function of phase shift φ. In the 3L-DAB and 4L-DAB cases, the modulation parameter values are defined by a set of equations, the so-called practical solution, which are inferred from the optimization results (see Sections 2.5.3 and 3.5.2) of objective functions F_1, F_2, and F_3, a parameter-less representation of the conduction and switching losses. The practical solutions of both ML-DAB converters ensure a good converter performance over a wide power and voltage gain range.

As shown in Section 4.5, the similarity between the patterns defined by the optimum results of the 3L-DAB and 4L-DAB, leads to induce that such resemblance will also occur for the 5L-DAB optimum results, otherwise unfeasible to obtain due to the high computational effort required by the optimization process. Considering such assumption, Section 4.5 defines the 5L-DAB modulation

parameter values with the 3L-DAB practical solution together with the equations that ensure a null charge provided to the inner dc-link points by $i_{z,1}$ (Section 4.4.1).

Let us make the same assumptions for the general NL-DAB case. The first and last switching angles (α_{z1} and α_{zM}, respectively) are defined as in the 3L-DAB practical solution (2.20), while the intermediate switching angles (α_{z2} to $\alpha_{z(M-1)}$) are defined with (5.12), which guarantees a null charge provided to the inner dc-link points by $i_{z,1}$. In summary, the NL-DAB practical solution is defined by

$$
\begin{aligned}
\left\{\alpha_{z1}\right\}_{\mathrm{PrS}} &= \begin{cases} 0° + \dfrac{\alpha_{z,\mathrm{th}}}{\varphi_{z,\mathrm{th}}} \cdot \varphi, & \varphi < \varphi_{z,\mathrm{th}} \\ \alpha_{z,\mathrm{th}} + \dfrac{90° - \alpha_{z,\mathrm{th}}}{90° - \varphi_{z,\mathrm{th}}} \cdot \left(\varphi - \varphi_{z,\mathrm{th}}\right), & \varphi \geq \varphi_{z,\mathrm{th}} \end{cases} \\
\left\{\alpha_{z2}\right\}_{\mathrm{PrS}} &= \arcsin\left(\sin\left(\alpha_{z1}\right) + \Delta_{z1}\right) \\
\left\{\alpha_{z3}\right\}_{\mathrm{PrS}} &= \arcsin\left(\sin\left(\alpha_{z2}\right) + \Delta_{z2}\right) \\
&\vdots \\
\left\{\alpha_{z(r+1)}\right\}_{\mathrm{PrS}} &= \arcsin\left(\sin\left(\alpha_{zr}\right) + \Delta_{zr}\right) \\
&\vdots \\
\left\{\alpha_{z\frac{M}{2}}\right\}_{\mathrm{PrS}} &= \arcsin\left(\sin\left(\alpha_{z\left(\frac{M}{2}-1\right)}\right) + \Delta_{z\left(\frac{M}{2}-1\right)}\right) \\
\left\{\alpha_{z\left(\frac{M}{2}+1\right)}\right\}_{\mathrm{PrS}} &= \arcsin\left(\sin\left(\alpha_{z\left(\frac{M}{2}+2\right)}\right) - \Delta_{z\left(\frac{M}{2}-1\right)}\right) \\
&\vdots \\
\left\{\alpha_{z(M-k)r}\right\}_{\mathrm{PrS}} &= \arcsin\left(\sin\left(\alpha_{z(M-r+1)}\right) - \Delta_{zr}\right) \\
&\vdots \\
\left\{\alpha_{z(M-2)}\right\}_{\mathrm{PrS}} &= \arcsin\left(\sin\left(\alpha_{z(M-1)}\right) - \Delta_{z2}\right) \\
\left\{\alpha_{z(M-1)}\right\}_{\mathrm{PrS}} &= \arcsin\left(\sin\left(\alpha_{zM}\right) - \Delta_{z1}\right) \\
\left\{\alpha_{zM}\right\}_{\mathrm{PrS}} &= \begin{cases} 90° - K_{\alpha,\mathrm{th}} \cdot \varphi, & \varphi < \varphi_{z,\mathrm{th}} \\ \alpha_{z,\mathrm{th}} + \dfrac{90° - \alpha_{z,\mathrm{th}}}{90° - \varphi_{z,\mathrm{th}}} \cdot \left(\varphi - \varphi_{z,\mathrm{th}}\right), & \varphi \geq \varphi_{z,\mathrm{th}}, \end{cases}
\end{aligned}
\tag{5.32}
$$

for odd N, and by

$$
\begin{aligned}
\left\{\alpha_{z1}\right\}_{\mathrm{PrS}} &= \begin{cases} 0° + \dfrac{\alpha_{z,\mathrm{th}}}{\varphi_{z,\mathrm{th}}} \cdot \varphi, & \varphi < \varphi_{z,\mathrm{th}} \\ \alpha_{z,\mathrm{th}} + \dfrac{90° - \alpha_{z,\mathrm{th}}}{90° - \varphi_{z,\mathrm{th}}} \cdot \left(\varphi - \varphi_{z,\mathrm{th}}\right), & \varphi \geq \varphi_{z,\mathrm{th}} \end{cases} \\
\left\{\alpha_{z2}\right\}_{\mathrm{PrS}} &= \arcsin\left(\sin\left(\alpha_{z1}\right) + \Delta_{z1}\right) \\
\left\{\alpha_{z3}\right\}_{\mathrm{PrS}} &= \arcsin\left(\sin\left(\alpha_{z2}\right) + \Delta_{z2}\right) \\
&\vdots \\
\left\{\alpha_{z(r+1)}\right\}_{\mathrm{PrS}} &= \arcsin\left(\sin\left(\alpha_{zr}\right) + \Delta_{zr}\right) \\
&\vdots \\
\left\{\alpha_{z\left(\frac{M-1}{2}\right)}\right\}_{\mathrm{PrS}} &= \arcsin\left(\sin\left(\alpha_{z\left(\frac{M-3}{2}\right)}\right) + \Delta_{z\left(\frac{M-3}{2}\right)}\right) \\
\left\{\alpha_{z\left(\frac{M+1}{2}\right)}\right\}_{\mathrm{PrS}} &= \arcsin\left(\frac{\sin\left(\alpha_{z\left(\frac{M+3}{2}\right)}\right) + \sin\left(\alpha_{z\left(\frac{M-1}{2}\right)}\right)}{2}\right) \\
\left\{\alpha_{z\left(\frac{M+3}{2}\right)}\right\}_{\mathrm{PrS}} &= \arcsin\left(\sin\left(\alpha_{z\left(\frac{M+5}{2}\right)}\right) - \Delta_{z\left(\frac{M-3}{2}\right)}\right) \\
&\vdots \\
\left\{\alpha_{z(M-r)}\right\}_{\mathrm{PrS}} &= \arcsin\left(\sin\left(\alpha_{z(M-r+1)}\right) - \Delta_{zr}\right) \\
&\vdots \\
\left\{\alpha_{z(M-2)}\right\}_{\mathrm{PrS}} &= \arcsin\left(\sin\left(\alpha_{z(M-1)}\right) - \Delta_{z2}\right) \\
\left\{\alpha_{z(M-1)}\right\}_{\mathrm{PrS}} &= \arcsin\left(\sin\left(\alpha_{zM}\right) - \Delta_{z1}\right) \\
\left\{\alpha_{zM}\right\}_{\mathrm{PrS}} &= \begin{cases} 90° - K_{\alpha,\mathrm{th}} \cdot \varphi, & \varphi < \varphi_{z,\mathrm{th}} \\ \alpha_{z,\mathrm{th}} + \dfrac{90° - \alpha_{z,\mathrm{th}}}{90° - \varphi_{z,\mathrm{th}}} \cdot \left(\varphi - \varphi_{z,\mathrm{th}}\right), & \varphi \geq \varphi_{z,\mathrm{th}}, \end{cases}
\end{aligned}
\tag{5.33}
$$

for even N. Variables $\varphi_{z,\mathrm{th}}$ and $\alpha_{z,\mathrm{th}}$ are computed with (2.21). In addition, restriction (5.9) must be complied.

Variables Δ_{zr} $\forall z,r$, together with $K_{\varphi,\mathrm{th}}$ and $K_{\alpha,\mathrm{th}}$, sum up to a total of $N-1$ DoF when N is odd, and to a total of $N-2$ DoF when N is even. These DoF are available to adjust the performance of the converter. As an example, and in order to simplify (5.32) and (5.33), let us set that all the differences between the sine of contiguous switching angles are equal, resulting in

$$
\Delta_{zr} = \Delta_z = \frac{\sin\left(\alpha_{zM}\right) - \sin\left(\alpha_{z1}\right)}{M-1},\ \forall r. \tag{5.34}
$$

With (5.34), the practical solution equations can be rewritten as

$$
\begin{aligned}
\left\{\alpha_{z1}\right\}_{\mathrm{PrS}} &= \begin{cases} 0° + \dfrac{\alpha_{z,\mathrm{th}}}{\varphi_{z,\mathrm{th}}} \cdot \varphi, & \varphi < \varphi_{z,\mathrm{th}} \\ \alpha_{z,\mathrm{th}} + \dfrac{90° - \alpha_{z,\mathrm{th}}}{90° - \varphi_{z,\mathrm{th}}} \cdot \left(\varphi - \varphi_{z,\mathrm{th}}\right), & \varphi \geq \varphi_{z,\mathrm{th}} \end{cases} \\
\left\{\alpha_{z2}\right\}_{\mathrm{PrS}} &= \arcsin\left(\sin\left(\alpha_{z1}\right) + \Delta_z\right) \\
\left\{\alpha_{z3}\right\}_{\mathrm{PrS}} &= \arcsin\left(\sin\left(\alpha_{z1}\right) + 2\Delta_z\right) \\
&\vdots \\
\left\{\alpha_{z(r+1)}\right\}_{\mathrm{PrS}} &= \arcsin\left(\sin\left(\alpha_{z1}\right) + r\Delta_z\right) \\
&\vdots \\
\left\{\alpha_{z\frac{M}{2}}\right\}_{\mathrm{PrS}} &= \arcsin\left(\sin\left(\alpha_{z1}\right) + \left(\frac{M}{2} - 1\right)\Delta_z\right) \\
\left\{\alpha_{z\left(\frac{M}{2}+1\right)}\right\}_{\mathrm{PrS}} &= \arcsin\left(\sin\left(\alpha_{zM}\right) - \left(\frac{M}{2} - 1\right)\Delta_z\right) \\
&\vdots \\
\left\{\alpha_{z(M-r)}\right\}_{\mathrm{PrS}} &= \arcsin\left(\sin\left(\alpha_{zM}\right) - r\Delta_z\right) \\
&\vdots \\
\left\{\alpha_{z(M-2)}\right\}_{\mathrm{PrS}} &= \arcsin\left(\sin\left(\alpha_{zM}\right) - 2\Delta_z\right) \\
\left\{\alpha_{z(M-1)}\right\}_{\mathrm{PrS}} &= \arcsin\left(\sin\left(\alpha_{zM}\right) - \Delta_z\right) \\
\left\{\alpha_{zM}\right\}_{\mathrm{PrS}} &= \begin{cases} 90° - K_{\alpha,\mathrm{th}} \cdot \varphi, & \varphi < \varphi_{z,\mathrm{th}} \\ \alpha_{z,\mathrm{th}} + \dfrac{90° - \alpha_{z,\mathrm{th}}}{90° - \varphi_{z,\mathrm{th}}} \cdot \left(\varphi - \varphi_{z,\mathrm{th}}\right), & \varphi \geq \varphi_{z,\mathrm{th}}, \end{cases}
\end{aligned}
\tag{5.35}
$$

for odd N, and as

$$
\begin{aligned}
\left\{\alpha_{z1}\right\}_{\mathrm{PrS}} &= \begin{cases} 0^\circ + \dfrac{\alpha_{z,\mathrm{th}}}{\varphi_{z,\mathrm{th}}} \cdot \varphi, & \varphi < \varphi_{z,\mathrm{th}} \\ \alpha_{z,\mathrm{th}} + \dfrac{90^\circ - \alpha_{z,\mathrm{th}}}{90^\circ - \varphi_{z,\mathrm{th}}} \cdot \left(\varphi - \varphi_{z,\mathrm{th}}\right), & \varphi \geq \varphi_{z,\mathrm{th}} \end{cases} \\
\left\{\alpha_{z2}\right\}_{\mathrm{PrS}} &= \arcsin\left(\sin\left(\alpha_{z1}\right) + \Delta_z\right) \\
\left\{\alpha_{z3}\right\}_{\mathrm{PrS}} &= \arcsin\left(\sin\left(\alpha_{z1}\right) + 2\Delta_z\right) \\
&\vdots \\
\left\{\alpha_{z(r+1)}\right\}_{\mathrm{PrS}} &= \arcsin\left(\sin\left(\alpha_{z1}\right) + r\Delta_z\right) \\
&\vdots \\
\left\{\alpha_{z\left(\frac{M-1}{2}\right)}\right\}_{\mathrm{PrS}} &= \arcsin\left(\sin\left(\alpha_{z1}\right) + \left(\frac{M-3}{2}\right)\Delta_z\right) \\
\left\{\alpha_{z\left(\frac{M+1}{2}\right)}\right\}_{\mathrm{PrS}} &= \arcsin\left(\frac{\sin\left(\alpha_{z\left(\frac{M+3}{2}\right)}\right) + \sin\left(\alpha_{z\left(\frac{M-1}{2}\right)}\right)}{2}\right) \\
\left\{\alpha_{z\left(\frac{M+3}{2}\right)}\right\}_{\mathrm{PrS}} &= \arcsin\left(\sin\left(\alpha_{zM}\right) - \left(\frac{M-3}{2}\right)\Delta_z\right) \\
&\vdots \\
\left\{\alpha_{z(M-r)}\right\}_{\mathrm{PrS}} &= \arcsin\left(\sin\left(\alpha_{zM}\right) - r\Delta_z\right) \\
&\vdots \\
\left\{\alpha_{z(M-2)}\right\}_{\mathrm{PrS}} &= \arcsin\left(\sin\left(\alpha_{zM}\right) - 2\Delta_z\right) \\
\left\{\alpha_{z(M-1)}\right\}_{\mathrm{PrS}} &= \arcsin\left(\sin\left(\alpha_{zM}\right) - \Delta_z\right) \\
\left\{\alpha_{zM}\right\}_{\mathrm{PrS}} &= \begin{cases} 90^\circ - K_{\alpha,\mathrm{th}} \cdot \varphi, & \varphi < \varphi_{z,\mathrm{th}} \\ \alpha_{z,\mathrm{th}} + \dfrac{90^\circ - \alpha_{z,\mathrm{th}}}{90^\circ - \varphi_{z,\mathrm{th}}} \cdot \left(\varphi - \varphi_{z,\mathrm{th}}\right), & \varphi \geq \varphi_{z,\mathrm{th}}, \end{cases}
\end{aligned}
\tag{5.36}
$$

for even *N*.

Fig. 5.13 shows the switching angles pattern in the generalized case, defined with (5.35) [Fig. 5.13(a)] and (5.36) [Fig. 5.13(b)].

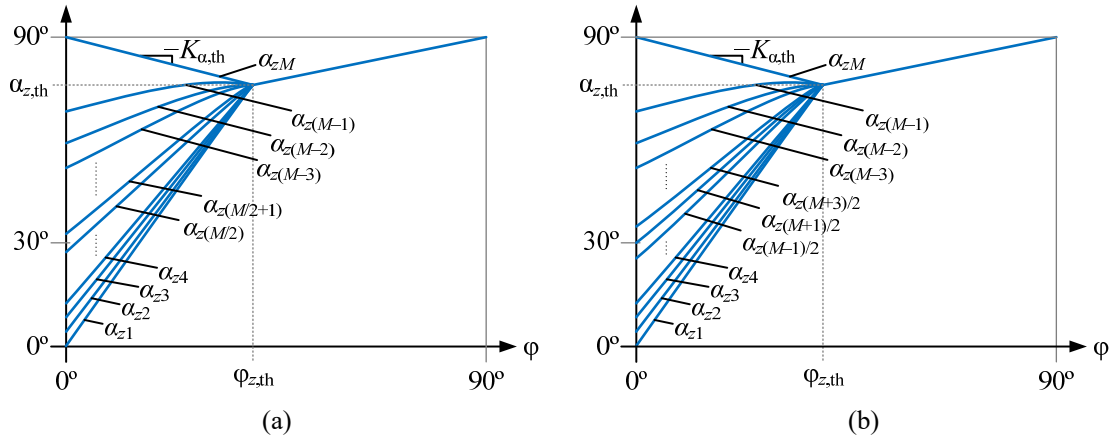


Fig. 5.13. Practical solutions defining the switching angles as a function of φ for the NL-DAB. (a) Odd N. (b) Even N.

5.6. Conclusion

This chapter has analyzed the *N*L-DAB case. The topology, modulation pattern, capacitor-voltage-balancing control schemes, and the practical solution defining the modulation parameter values, are inferred from the previously studied 3L-DAB, 4L-DAB, and 5L-DAB particular cases.

Switching angles α_{zik} and α_{zok} $\forall k,z$ and phase shift φ, defined in the modulation, sum up a total of $4N - 3$ DoF. These DoF form two groups; $N + 1$ (for even N) or $N + 2$ (for odd N) DoF are employed to control the power flow between both converter sides and optimize the converter performance, while $3N - 4$ (for even N) or $3N - 5$ (for odd N) DoF are employed for the capacitor voltage balancing. It is worth noting that each time the number of levels is increased to an odd number, two more DoF are available to optimize the converter performance and control the power flow.

Switching angles α_{zk} $\forall k,z$ are defined as a function of φ and Δ_{zr} $\forall r,z$, with a set of closed-form expressions inferred from the proposed 3L-DAB and 4L-DAB practical solutions. These practical solutions are formulated such that they resemble the patterns defined by the modulation parameter values that minimize the conduction and switching losses. Since the 3L-DAB and 4L-DAB optimum solution patterns are almost identical, it is reasonable to expect that the optimum solution patterns for greater number of levels will also be similar, and hence, the proposed *N*L-DAB practical solution will present a good converter efficiency.

Two aspects of the capacitor-voltage-balancing control are studied. Firstly, the suitability of the system linearization, performed to obtain a decoupled control scheme, is studied. Its suitability is confirmed for a large range of u_{zm} when switching angle values are close to zero, and for a small range of u_{zm} when switching angle values are close to 90º. Secondly, the effective working range of the capacitor-voltage-balancing control is analyzed. The theoretical analysis shows that extremely high and low d values should be avoided, and a minimum phase shift value should be guaranteed. However, the capacitor voltage balancing can be guaranteed in these conditions by employing an alternative modulation and control scheme, exemplified in this chapter for the 5L-DAB. Its basis is the control of the capacitor voltages with $i^{q}_{z,1}$ (the in-quadrature component), while the charge provided by $i^{p}_{z,1}$ is neglected, since $I^{p}_{z,1} \approx 0$ when the described conditions are met. A generalized alternative modulation scheme should be easy to infer, yet such study falls outside the scope of this thesis.

CHAPTER 6.

STUDY OF NEUTRAL-POINT-CLAMPED DUAL-ACTIVE-BRIDGE DC-DC CONVERTERS WITH ASYMMETRIC NUMBER OF LEVELS

Abstract —This chapter presents the study of multilevel NPC DAB dc-dc converters with an asymmetric number of levels; i.e., the a-side number of levels is different from the b-side number of levels. The modulation strategy, capacitor-voltage-balancing control, and modulation parameter values are based on the conventional 2L-DAB and the proposed (symmetric) 3L-DAB and 4L-DAB. The feasibility and good performance of the proposed asymmetric NPC DAB converters is verified through simulation and experimental tests.

6.1. Introduction

This chapter studies different ML-DAB converters built upon 2L legs, 3L NPC legs, and 4L NPC legs, whose common characteristic is that the number of levels on each dc-link is not equal; i.e., a ML-DAB converter with an asymmetric number of levels. Three different asymmetric DAB converters are considered:

- A DAB built upon two 3L-NPC legs on side a and two 2L legs on side b (3L-2L-DAB).
- A DAB built upon two 4L-NPC legs on side a and two 2L legs on side b (4L-2L-DAB).
- A DAB built upon two 4L-NPC legs on side a and two 3L-NPC legs on side b (4L-3L-DAB).

The modulation, capacitor-voltage-balancing control, and definition of the modulation parameters for each converter are based on the results obtained in previous chapters.

Simulation and experimental tests are done to verify the viability of the proposed asymmetric ML-DAB converters, and by extension, of a general N_aL-N_bL-DAB converter, where N_a and N_b are the a-side and b-side number of levels, respectively.

This chapter is organized as follows. Section 6.2 briefly presents the configuration of each converter, which embraces the topology, modulation, capacitor-voltage-balancing control, and the solutions to define the modulation parameters. Section 6.3 presents the simulation and experimental results that verify the good performance of the asymmetric converters. Finally, Section 6.4 outlines the conclusions.

6.2. Configuration overview

This section presents the topology, modulation, capacitor-voltage-balancing control, and definition of the modulation parameters of the proposed asymmetric ML-DAB converters.

6.2.1. Topologies

Fig. 6.1, Fig. 6.2, and Fig. 6.3 present the topologies of the proposed 3L-2L-DAB, 4L-2L-DAB, and 4L-3L-DAB converters, respectively.

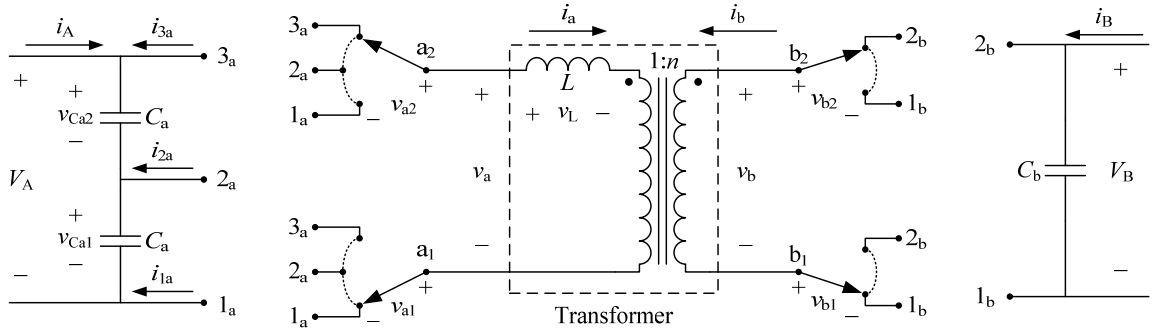


Fig. 6.1. Topology of the proposed 3L-2L-DAB dc-dc converter with phase legs a_1 and a_2 depicted as single-pole triple-throw switches and phase legs b_1 and b_2 depicted as single-pole double-throw switches.

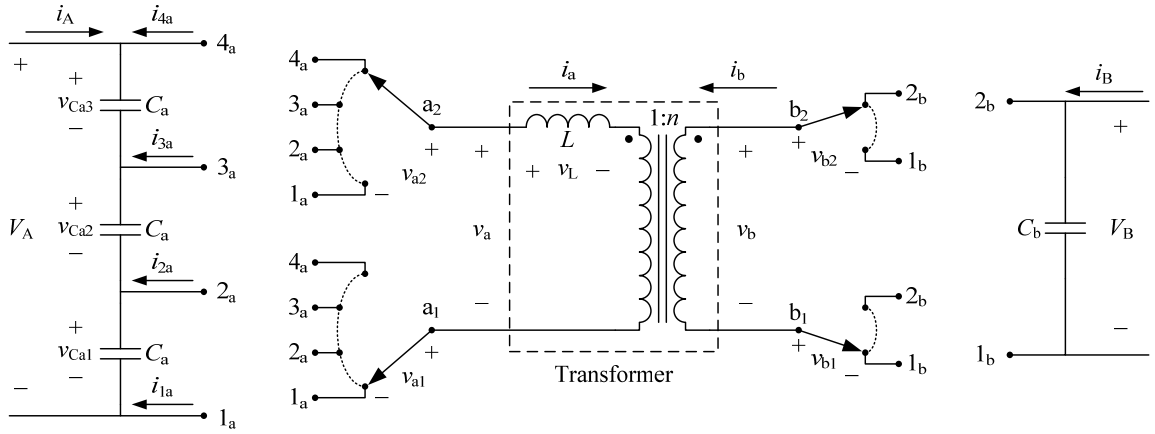


Fig. 6.2. Topology of the proposed 4L-2L-DAB dc-dc converter with phase legs a_1 and a_2 depicted as single-pole quadruple-throw switches and phase legs b_1 and b_2 depicted as single-pole double-throw switches.

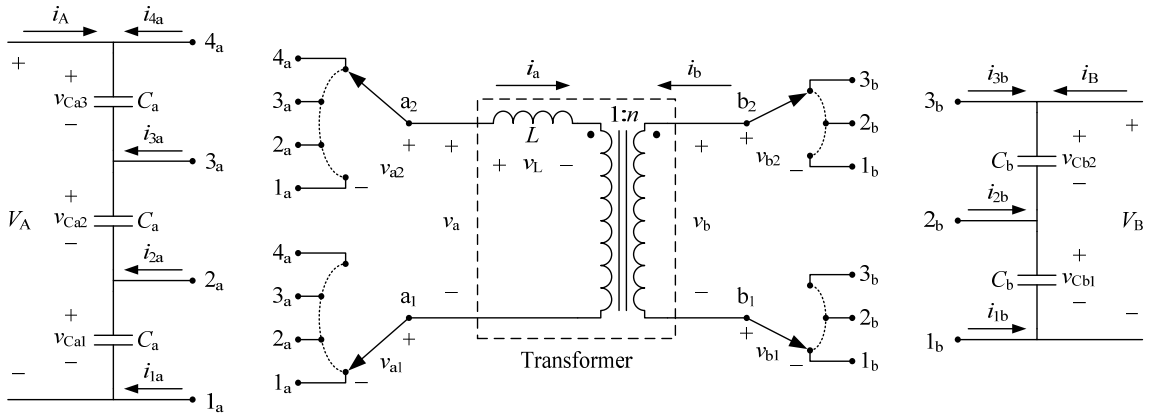


Fig. 6.3. Topology of the proposed 4L-3L-DAB dc-dc converter with phase legs a_1 and a_2 depicted as single-pole quadruple-throw switches and phase legs b_1 and b_2 depicted as single-pole triple-throw switches.

6.2.2. Modulations

The modulation variables and switching sequence that define the transformer voltage waveforms on the N_zL side, with $N_z \in \{3,4\}$, of the proposed asymmetric DAB converters, are the same as in the symmetric case. For example, in the 4L-3L-DAB converter, v_a is defined as in the 4L-DAB modulation (Fig. 3.2), with variables $\{\alpha_{ao1},\alpha_{ao2},\alpha_{ao3},\alpha_{ai1},\alpha_{ai2},\alpha_{ai3}\}$, while v_b is defined as in the 3L-DAB modulation (Fig. 2.4), with variables $\{\alpha_{bo1},\alpha_{bo2},\alpha_{bi1},\alpha_{bi2}\}$. The modulation variables and switching sequence employed on the 2L sides (always side b) of Fig. 6.1 and Fig. 6.2 converters is equal to those proposed in [26], which offers the capability of generating zero-voltage dwell times in v_b. The dwell time where v_b remains at V_B or $-V_B$ is equal to $2\cdot\alpha_b/(360\cdot f_s)$.

6.2.3. Capacitor-voltage-balancing controls

Each N_zL side of the proposed asymmetric ML-DAB converters, with $N_z \in \{3,4\}$, employs the same control as in the symmetric case. For the 4L case, the decoupled full control scheme is employed in the simulations and experimental tests, unless otherwise noted.

6.2.4. Definition of the modulation parameters

The modulation parameters (α_{zk} switching angles) of each N_zL side of the proposed asymmetric DAB converters, with $N_z \in \{3,4\}$, are defined with the practical solutions of the symmetric case. The modulation parameters for each 2L side (always on side b), is defined as the average value of switching angles α_{b1} and α_{b2} defined in the 3L-DAB practical solution. The practical solution parameter values for all the proposed asymmetric DAB converters are $K_{\varphi,th} = 50^o$, $K_{\alpha,th} = 0.2$, and $\varphi_{th,max} = 80^o$.

6.3. Simulation and experimental results

Simulation and experimental tests have been carried out to demonstrate the good performance of the selected asymmetric ML-DAB converters in terms of capacitor-voltage-balancing control and output voltage control. Three MATLAB-Simulink lossless models are used to perform the simulations, one for each converter. It is assumed $n = 1$, $L = 300$ μH, $C_z = 100$ μF for the three-level and four-level dc-links, $C_b = 35$ μF for the two-level dc-link, and $H_{filt}(s) = 2\pi \cdot 1000/(s + 2\pi \cdot 1000)$. The experimental tests are performed with the converter prototypes shown in Appendix A.

In all simulations and experiments, a dc voltage source with a small series resistance (10 mΩ) is connected across the a-side dc-link while a resistance R_B is connected in parallel with the b-side dc-link. The converters are operated at $f_s = 25$ kHz. Switching angles α_{zk} are defined with the practical solutions proposed in Section 6.2.4. The capacitor-voltage-balancing control schemes proposed in Section 6.2.3 are employed, with $G_{zm}(s)$ defined with (2.14) and $k_{P,am} = -k_{P,bm} = 0.3$ $\forall m$ and $T_{I,zm} = 20$ ms $\forall z,m$. Voltage V_B is controlled by the regulator defined in Fig. 2.15, with $K_{ps} = 10000$, $f_{z,ps} = 50$ Hz, $f_{p,ps} = 2500$ Hz, and V_o^* equal to the V_B defined in each working point. Resistance R_B is adjusted so that the phase shift control settles at the φ and V_B values specified in each working point. The switching angle values (α_{zok} and α_{zik}) outputted by the capacitor-voltage-balancing control are processed by the algorithm presented in Appendix B, in order to limit its values to the defined boundaries. The minimum difference between adjacent switching angles is $\Delta\alpha_{z,min} = 6.3^o$ (700 ns at 25 kHz) for the three-level and four-level converter legs (such limit does not apply to the two-level converter legs). All compensator parameters have been tuned through simulation and experiments to obtain an acceptable performance and stable behavior. The steady state and transient behavior is analyzed at six different working points, defined in Table 6.1.

	d	V_A	V_B	φ
WP1	1	100 V	100 V	20º
WP2	1	100 V	100 V	60º
WP3	1.33	150 V	200 V	20º
WP4	1.33	150 V	200 V	60º
WP5	0.67	180 V	120 V	20º
WP6	0.67	180 V	120 V	60º

Table 6.1. Working points defined for the simulation and experimental tests.

6.3.1. Steady-state results

The steady-state results obtained from the simulation and experimental tests performed with the three proposed asymmetric DAB converters are presented below.

6.3.1.1. 3L-2L-DAB

Fig. 6.4 presents the simulation steady-state results obtained at the six defined working points with the 3L-2L-DAB converter, showing the relevant voltage and current waveforms. Fig. 6.5 shows the experimental results for working points WP1 and WP5. It can be observed that simulation and experimental results are in close agreement. Moreover, both results present voltage balance in the dc-link capacitors, since both v_a and v_b present voltage steps with an equal amplitude. The colored dots in the simulation results indicate when a transition is of Type I (red) or Type II (green). With the proposed practical solution and according to the simulation results, when $\varphi \approx 60^o$; i.e., at medium to high transferred power, all the switching transitions are of Type II (soft-switching transitions) and hence low switching losses are achieved. For lower φ values ($\approx 20^o$), some transitions are of Type I (hard-switching transitions), which imply more switching losses. However, since most of these transitions occur at low switching-current values, the overall switching losses are reduced.

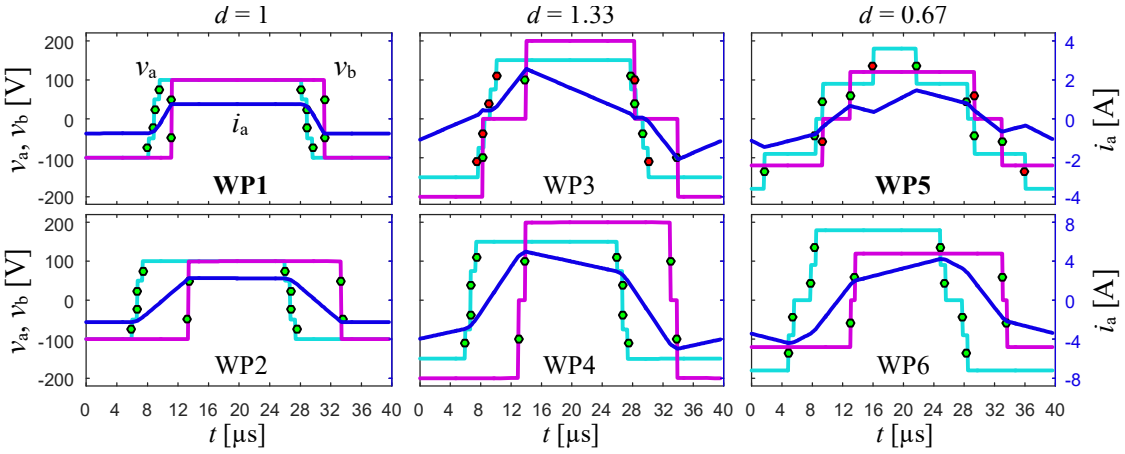


Fig. 6.4. Simulation steady-state results obtained at the specified working points with the 3L-2L-DAB.

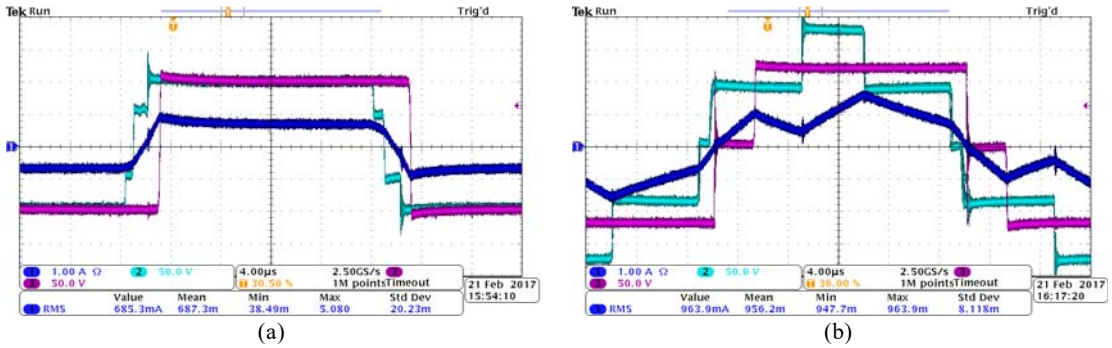


Fig. 6.5. Experimental steady-state results obtained with the 3L-2L-DAB. (a) WP1. (b) WP5.

6.3.1.2. 4L-2L-DAB

Fig. 6.6 presents the simulation steady-state results obtained at the six defined working points with the 4L-2L-DAB converter, while Fig. 6.7 shows the experimental results for working points WP5 and WP6. Again, it can be observed that simulation and experimental results are in close agreement, and both present voltage balance in the dc-link capacitors. It can be observed that the experimental a-side switching angles are not equal to the simulation switching angles. This discrepancy is probably due to the non-idealities of the converter prototype, which worsens the natural unbalance of the capacitor voltages and forces a greater control action of the control scheme. With the proposed practical solution and according to the simulation results, when $\varphi \approx 60^{\circ}$ all the switching transitions are of Type II (soft-switching transitions), leading to reduced switching losses. For lower φ values, some transitions are of Type I (hard-switching transitions), which imply more switching losses, albeit mostly reduced due to the transition low switching-current values. Nevertheless, compared to the 3L-2L-DAB converter, the present converter benefits from the added voltage level on the a-side switching legs, which contributes to lower switching and conduction losses if lower voltage-rated devices are selected.

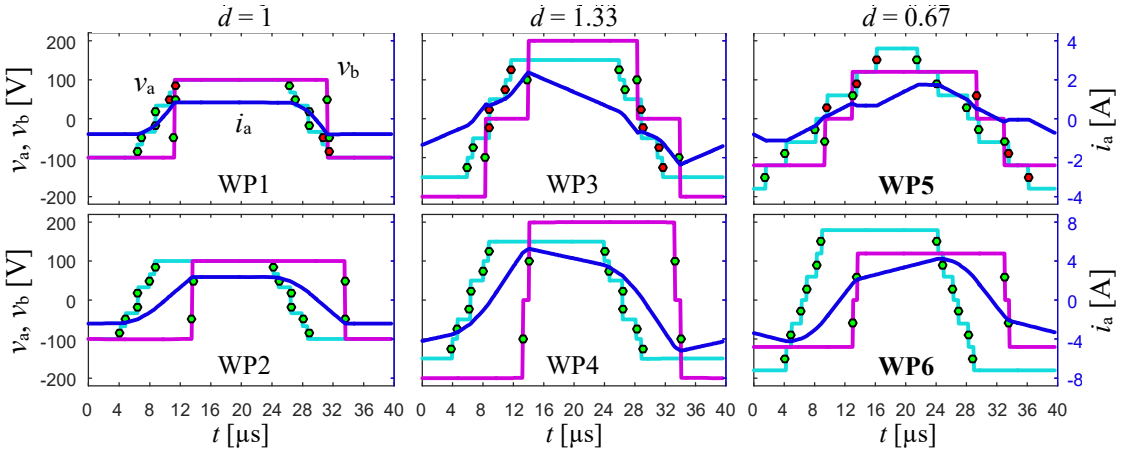


Fig. 6.6. Simulation steady-state results obtained at the specified working points with the 4L-2L-DAB.

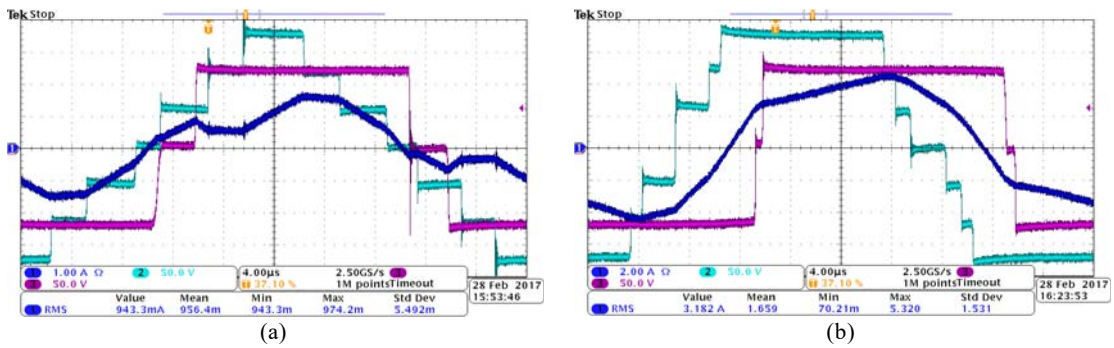


Fig. 6.7. Experimental steady-state results obtained with the 4L-2L-DAB. (a) WP5. (b) WP6.

6.3.1.3. 4L-3L-DAB

Fig. 6.8 presents the simulation steady-state results obtained at the six defined working points with the 4L-3L-DAB converter, while Fig. 6.9 shows the experimental results for working points WP3 and WP6. It can be observed that simulation and experimental results are in close agreement, and both present voltage balance in the dc-link capacitors. It can be noted that there is a discrepancy between the experimental and simulation a-side switching angle values, probably due to the non-idealities of the converter prototype. In addition, with the proposed practical solution and according to the simulation results, soft-switching transitions are achieved at medium to high transferred power values. At low transferred power values, some hard-switching transitions occur, although its current switching values are low. As in the previous case, compared to the 3L-2L-DAB and 4L-2L-DAB converters, the present converter benefits from an added voltage level on one or both sides, which contributes to lower switching and conduction losses if lower voltage-rated devices are selected.

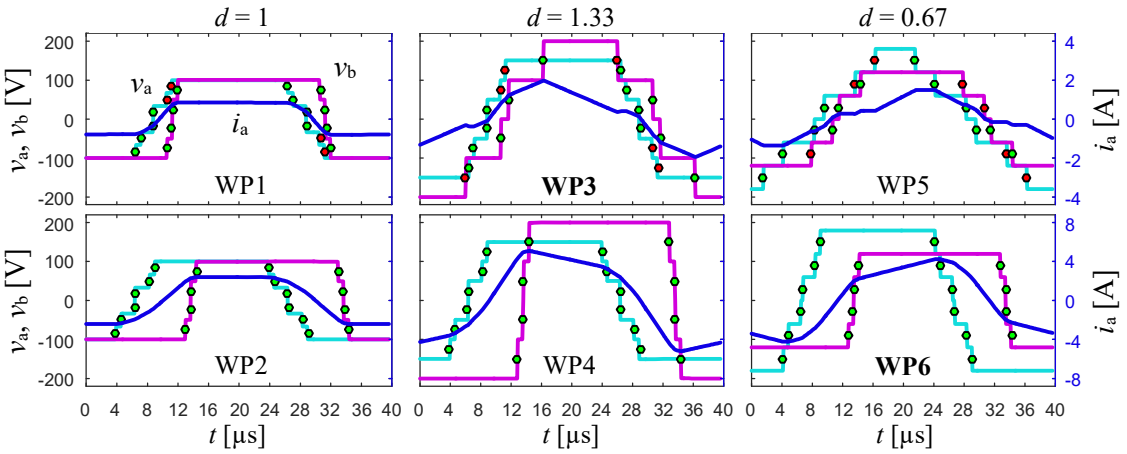
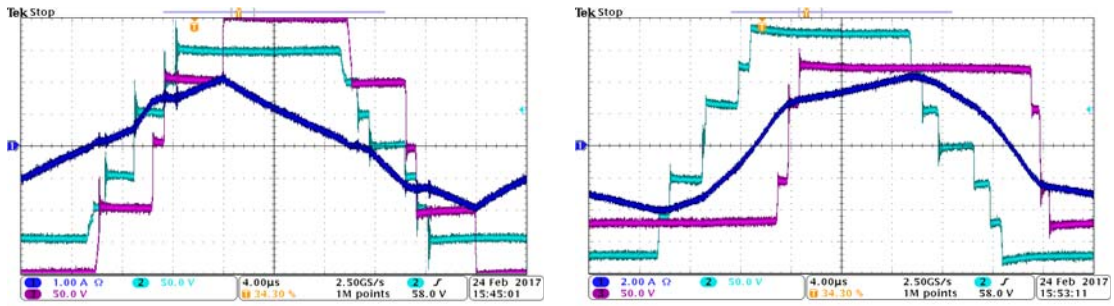


Fig. 6.8. Simulation steady-state results obtained at the specified working points with the 4L-3L-DAB.



(a) (b)

Fig. 6.9. Experimental steady-state results obtained with the 4L-3L-DAB. (a) WP3. (b) WP6.

6.3.2. Transient results

The transient results obtained from the simulation and experimental tests allow analyzing the behavior, performance, and suitability of the proposed capacitor-voltage-balancing control schemes working together with the output voltage control and practical solution for the proposed asymmetric DAB converters. The transient tests consist on forcing a deliberate unbalance of the dc-link capacitor voltages (on side a for the 3L-2L-DAB and 4L-2L-DAB and on both sides for the 4L-3L-DAB), by assigning a pulsed signal with ramped transitions (going from zero to a given value) to y^*_{zm} variables (as in Section 3.6.2 and Section 4.6.2). On all tests, y^*_{zm} ramps have an absolute value of the slopes equal to 3 V/ms.

The transient results, obtained from the simulation and experimental tests performed with the three proposed asymmetric ML-DAB converters are presented below.

6.3.2.1. 3L-2L-DAB

Fig. 6.10 presents the simulation transient results obtained at the six defined working points with the 3L-2L-DAB converter, showing the dc-link capacitor voltages, transformer current, switching angles, and phase shift. Fig. 6.11 shows the experimental transient results for working points WP1 and WP5, only showing both sides capacitor voltages and the transformer current. In the transient tests of working points WP1 to WP4, y^*_{a2} ramped pulse plateau value is 10 V, while on WP5 and WP6 it is 30 V. This sets voltages v_{Cb1} and v_{Cb2} 5 V (15 V for WP5 and WP6) above and below its initial values, respectively.

It can be observed that simulation and experimental results are in close agreement. The capacitor-voltage-balancing control is able to modify the capacitor voltages according to the reference values, even when switching angles α_{ai} and α_{ao} get limited during the transient to 0º, 90º, or to an adjacent switching angle plus/minus margin $\Delta\alpha_{a,min}$. As seen in Fig. 6.10, the modification of the switching angles alters the transferred power and V_B, even though the output voltage control corrects both by modifying the phase shift. Moreover, due to the modification of φ and V_B, switching angles α_{ak} are altered due to the practical solution, which in turn modifies switching angles α_{ai} and α_{ao}. In other words, the capacitor-voltage-balancing control, output voltage control, and practical solution are coupled, and an external alteration of any of the plant variables (capacitor voltages and transformer current, mainly) entails a modification of the modulation variables by the practical solution and both controls. Nevertheless, as demonstrated in the results, this coupling does not make the system unstable if proper compensator parameters are employed. In fact, a large K_{ps} value is required to avoid an oscillation of the output voltage due to the interaction of the output voltage

control and the effect of the parameter values determined by the practical solution. This has been verified through simulation and experimental tests.

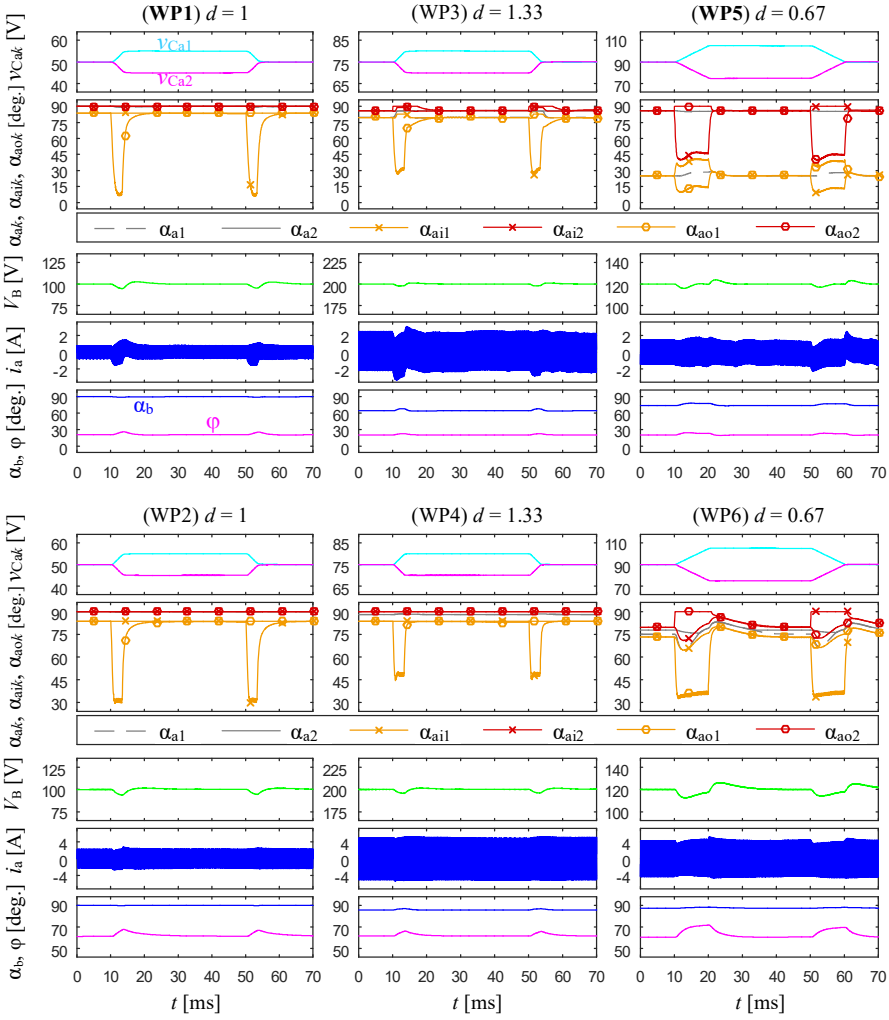


Fig. 6.10. Simulation transient results obtained at the specified working points with the 3L-2L-DAB.

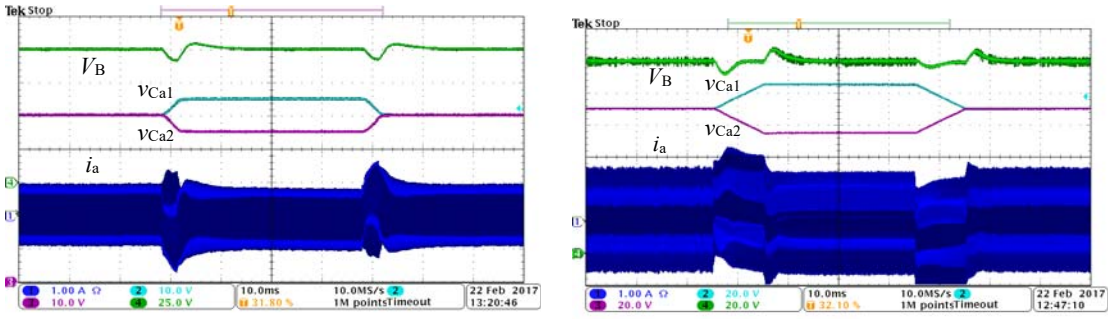


Fig. 6.11. Experimental test transient results obtained with the 3L-2L-DAB. (a) WP1. (b) WP5.

6.3.2.2. 4L-2L-DAB

Fig. 6.12 presents the simulation transient results obtained with the 4L-2L-DAB converter at four of the defined working points and with the non-decoupled and decoupled full control schemes on side a. Fig. 6.13 shows the experimental transient results for working point WP5 and both control schemes. In these tests, y^*_{a2} and y^*_{a3} ramped pulse plateau value is set to 15 V, displacing v_{Ca1} and v_{Ca3} 10 V above and below its initial values, respectively, while ideally maintaining v_{Ca2} constant. To do so, positive charge must be injected into both 2_a and 3_a inner dc-link points, which is accomplished by increasing (decreasing) the distance between the outer (inner) switching angles (see Fig. 3.4).

It can be observed that simulation and experimental results are in close agreement. The capacitor-voltage-balancing control is able to modify the capacitor voltages according to the reference values, even when switching angles α_{aik} and α_{aok} get limited during the transient. As in the previous case, the coupling between the control schemes, practical solution, and the plant does not affect negatively the regulation of the capacitor voltages nor the output voltage. It can be observed that v_{Ca2} is maintained constant when employing the decoupled full control scheme in WP1 and WP2, while a little variation appears during the ramps transient with the non-decoupled control scheme on all the working points. In WP5 and WP6, the decoupled control scheme does not perform satisfactorily and behaves similarly to the non-decoupled control scheme. Most probably, this fact happens due to the loss of the linearity hypothesis (switching angles are limited during the transient), required for the decoupling matrix to be effective.

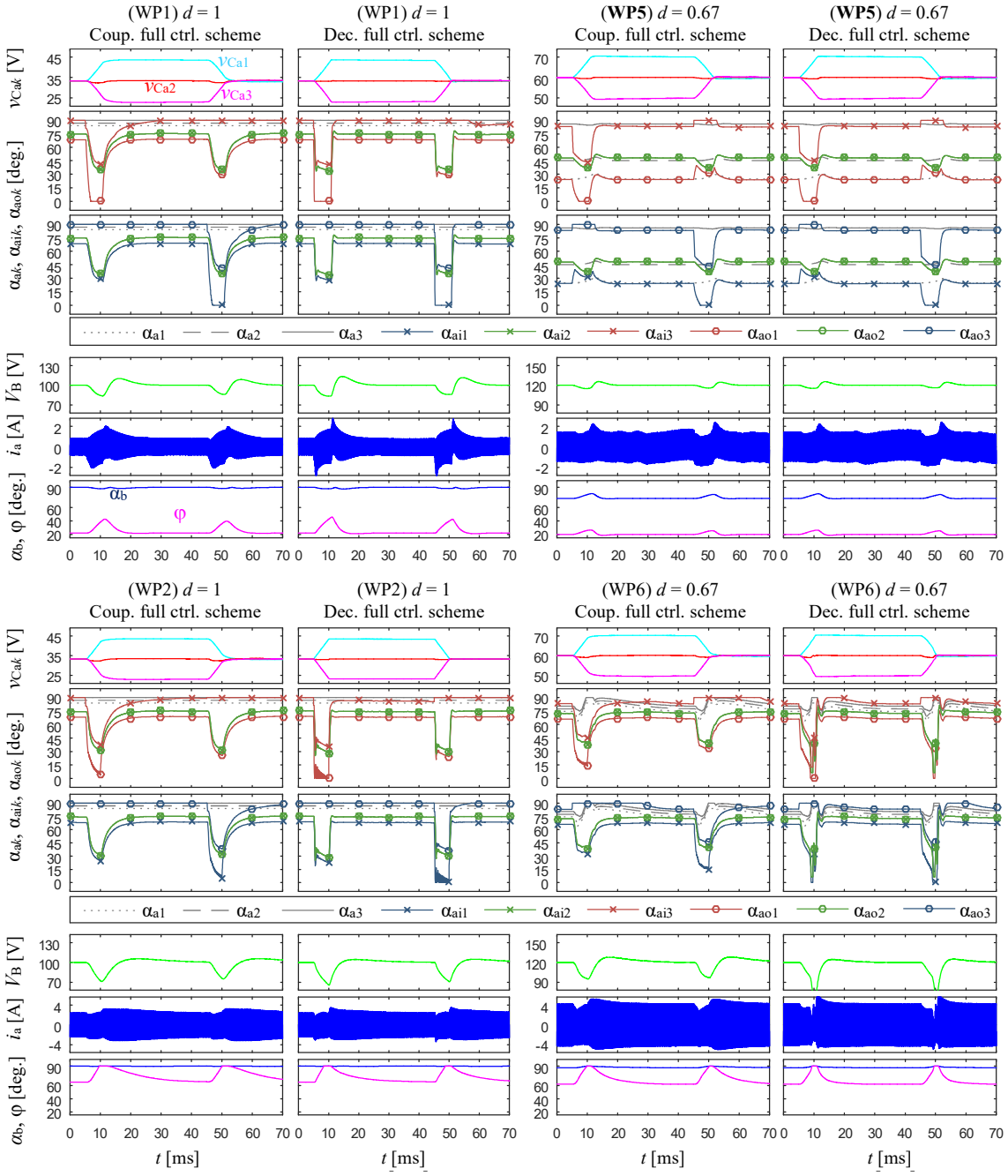
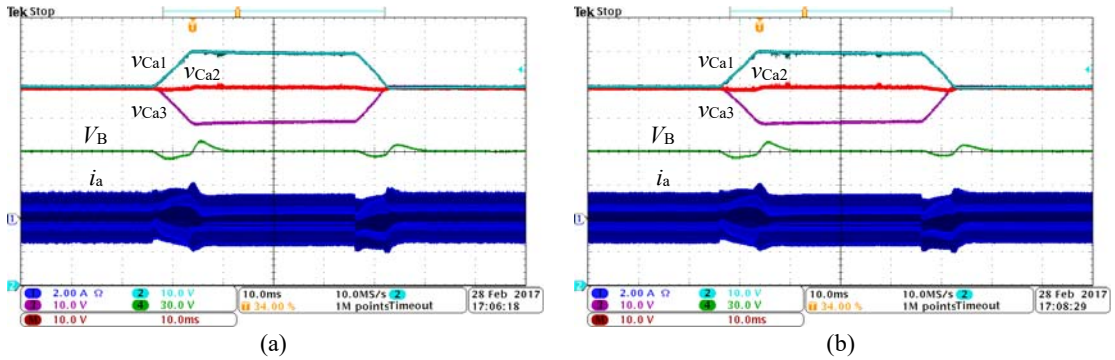


Fig. 6.12. Simulation transient results obtained at working points WP1, WP2, WP5, and WP6 with the 4L-2L-DAB.



(a) (b)

Fig. 6.13. Experimental transient results obtained with the 4L-2L-DAB. (a) WP5 with the non-decoupled full control scheme. (b) WP5 with the decoupled full control scheme.

6.3.2.3. 4L-3L-DAB

Fig. 6.14 presents the simulation transient results obtained at the six working points with the 4L-3L-DAB converter, showing the relevant waveforms. Fig. 6.15 shows the experimental transient results for working points WP3 and WP6. In these tests, the y^*_{a2} and y^*_{a3} ramped pulse plateau value is set to 15 V and the y^*_{b2} ramped pulse plateau value is set to 10 V. This, in fact, sets voltages v_{Ca1} and v_{Ca3} 10 V above and below its initial values, respectively, while v_{Cb1} and v_{Cb2} are set 5 V above and below its initial values, respectively. Ideally, v_{Ca2} is maintained constant. To perform such transients, the control schemes must inject positive charge into 2_a, 3_a, and 2_b inner dc-link points, which is accomplished by increasing (decreasing) the distance between the outer (inner) a-side and between the inner (outer) b-side switching angles (see Fig. 2.6 and Fig. 3.4).

It can be observed that simulation and experimental results are in close agreement. The capacitor-voltage-balancing controls are able to satisfactorily modify the capacitor voltages of both dc-links according to the reference values, even when switching angles get limited during the transient. As in the previous case, the coupling between the control schemes, practical solution, and the plant does not affect negatively the regulation of the capacitor voltages and output voltage. In addition, as in the previous case, the decoupling of the capacitor-voltage-balancing control scheme is successful only in some of the workings points, although, in those cases where it is not successful, the alteration of v_{Ca2} is insignificant.

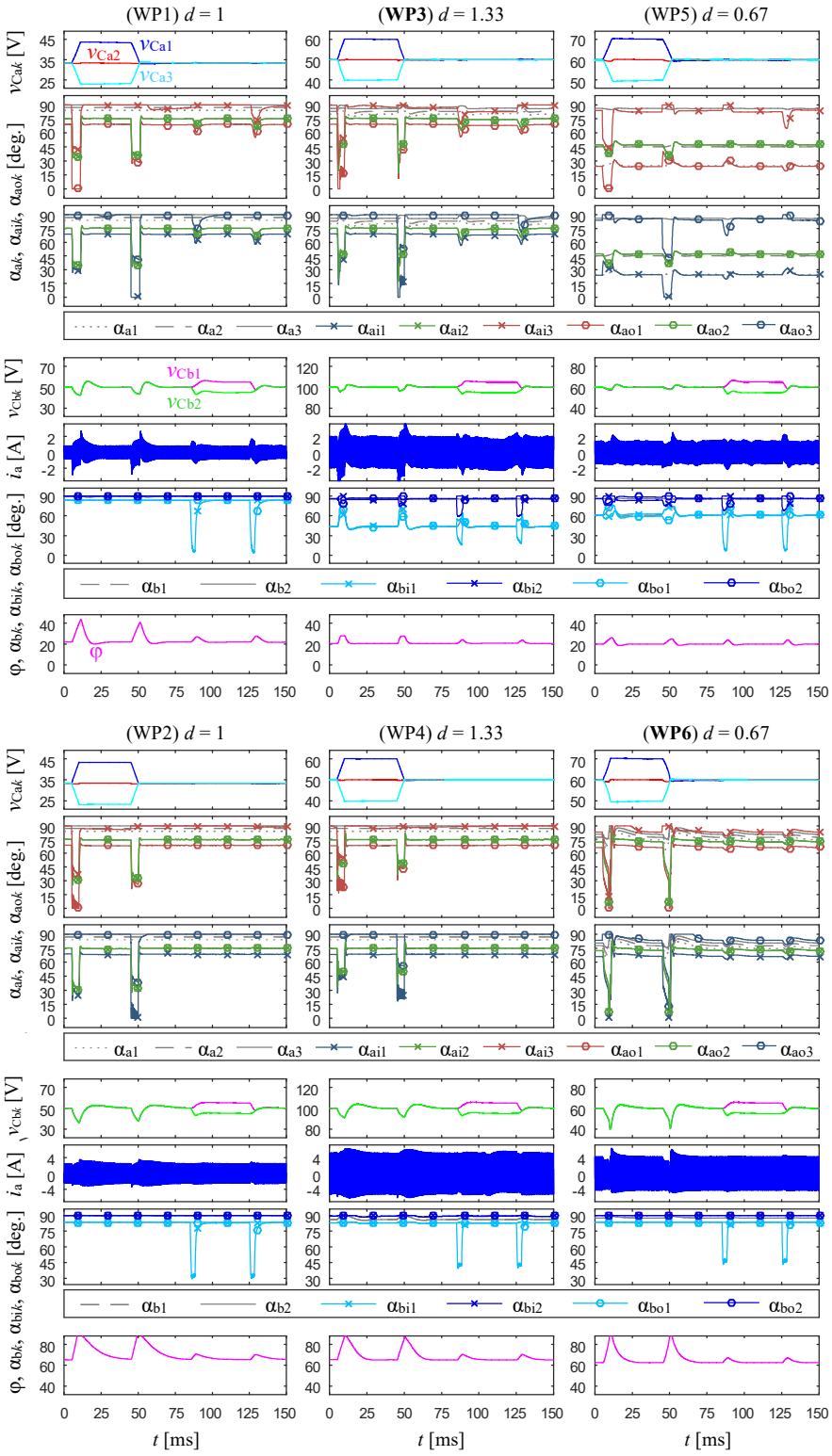
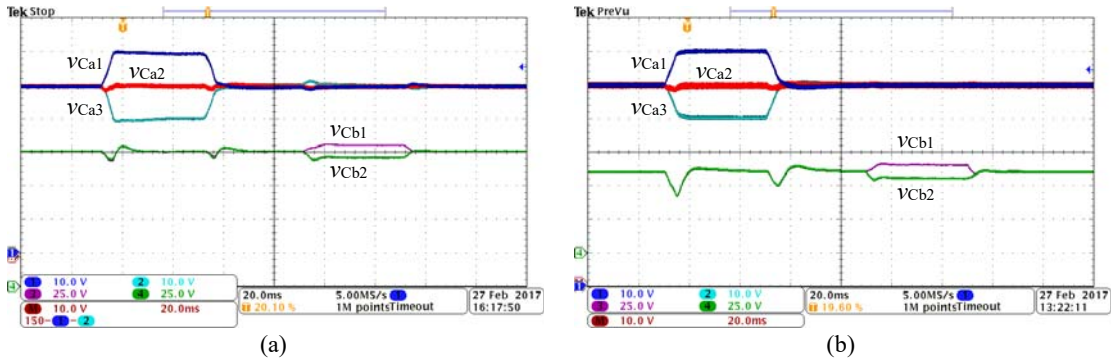


Fig. 6.14. Simulation transient results obtained at the specified working points with the 4L-3L-DAB.



(a) (b)

Fig. 6.15. Experimental transient results obtained with the 4L-3L-DAB. (a) WP3. (b) WP6.

6.4. Conclusion

This chapter has proposed and studied the feasibility of three types of asymmetric ML-DAB converters, each one with a different number of dc-link voltage levels on each side, designated as 3L-2L-DAB, 4L-2L-DAB, and 4L-3L-DAB converters. The converter topologies, modulations, capacitor-voltage-balancing control schemes, and practical solutions to define the modulation parameters are based on the previously studied 3L-DAB and 4L-DAB converters. A set of simulation and experimental tests are performed at six different working points in order to obtain steady-state results and transient results with the three asymmetric ML-DAB converters. In all the tests, the proposed capacitor-voltage-balancing controls, practical solutions, and output voltage control are employed simultaneously.

From the simulation and experimental results, it is concluded that it is feasible to implement a ML-DAB converter with an arbitrary number of dc-link voltage levels on each side; i.e., a general N_aL-N_bL-DAB converter. This can be justified as follows. The main concern regarding the viability of such converter configurations is the necessity to maintain the dc-link capacitor voltages balanced. The regulation of the capacitor voltages is performed with the transformer-current fundamental component, but can be negatively affected by its harmonic components. If the general practical solution is employed, the fundamental component will always be greater than the harmonic components, regardless of the number of dc-link voltage levels on each side. In fact, the harmonic content typically diminishes when the number of levels on any side increase. Hence, the capacitor voltage balancing can be guaranteed for any asymmetric ML-DAB converter configuration.

In addition, the simulation and experimental tests have also shown that the existing coupling between the capacitor-voltage-balancing controls, the output voltage control, the practical solutions defining the modulation parameters, and the plant does not necessarily compromise the correct operation of the overall system. Despite that, a proper study of the interaction between such

subsystems is needed, in order to determine the proper parameter values that ensure the system stability over a full working range.

An asymmetric DAB converter has a great advantage in applications with $V_B/V_A >> 1$ or $V_B/V_A << 1$, since it permits the use of a single highly-optimized switching device for both converter sides, enabling a high power conversion efficiency, a high power density, and a reduced cost.

CHAPTER 7.

CONCLUSION

Abstract — This chapter outlines the thesis contributions and proposes possible future research work.

7.1. Contributions

The main contributions of this thesis can be summarized as follows:

- This thesis studies the use of NPC multilevel legs to substitute the common two-level legs on the FB-DAB converter. Three initial ML-DAB converters are proposed, each one differing on the number of levels of the employed NPC legs. These converters are the 3L-DAB, 4L-DAB and 5L-DAB. The study of each individual case lets us infer and characterize a general *N*L-DAB.
- A main issue of multilevel converter employing NPC legs with capacitor-divided voltage sources is the necessity to maintain the capacitor voltages balanced, in order to guarantee a safe an equal blocking voltage among the legs switches. Many solutions are proposed in the literature for modulations with high switching-to-fundamental frequency ratios. Nonetheless, the principle of operation of the DAB converters implies a switching-to-fundamental frequency ratio equal to one. The limited literature related to ML-DAB converters does not deal with the described issue. Therefore, this thesis has faced the challenge, with satisfactory results, of developing a novel modulation as well as a control scheme that guarantees the capacitor voltage balancing on the converter dc-links of the proposed converters.
- The proposed modulation scheme has the following properties:
    - It guarantees a null dc component on the transformer voltages, even with unbalanced capacitor voltages, hence avoiding the risk of transformer core saturation and a transformer-current dc component, which would increase the converter conduction and switching losses.
    - The transformer-voltages dwell times are defined with a set of switching angles, defining voltage waveforms with odd symmetry. This property is essential to control the charge provided to the inner dc-link points, and hence to maintain the capacitor voltages balanced.
    - The total number of DoF offered by the modulation is $4N - 3$. From this amount, $N + 1$ (for even N) or $N + 2$ (for odd N) DoF are employed to control the power flow between both converter sides and optimize the converter

performance, while $3N - 4$ (for even N) or $3N - 5$ (for odd N) DoF are employed for the capacitor voltage balancing.

- To study the capacitor-voltage-balancing issue, this thesis proposes a simple method consisting on the analysis of the charge provided to the inner dc-link points by the transformer-current fundamental component. To further ease the analysis, the fundamental component is divided into two components: a component in phase and another in quadrature with the transformer-voltage fundamental component.
    - With the proposed modulation, it is possible to provide charge only with the in-phase component, while the charge provided by the in-quadrature component is automatically cancelled within a switching cycle, thanks to the voltage waveform odd symmetry. A more comprehensive study shows that the same behavior is exhibited by the rest of transformer-current harmonics. Nevertheless, most of the charge is provided by the fundamental component.
    - For simplicity, the number of switching angles defining the voltage waveforms can be halved by forcing quarter-wave symmetry on such waveforms. With such condition, it is also easier to determine the switching angle values cancelling the average charge provided to the inner dc-link points by the in-phase fundamental component. For the particular case of the 3L-DAB, it is not necessary since such charge is automatically cancelled when quarter-wave symmetry is met. Moreover, in converters with an odd number of levels, the charge provided by such current to the middle dc-link point is always null when quarter-wave symmetry is met.
    - The transformer current harmonics and converter non-idealities may still cause a capacitor voltage unbalance. In order to correct it, switching angles can be modified (losing quarter-wave symmetry) to provide a controlled non-zero charge to the inner dc-link points with the transformer-current fundamental component.
- Novel control schemes are proposed to regulate the capacitor voltage balancing by modifying the voltage waveform switching angles. A set of variables defining the unbalance of the inner dc-link point voltages are the inputs of the control schemes. Each unbalance variable has an associated control variable modifying the switching angles in order to control the charge provided to the inner dc-link points.
    - A careful analysis shows that two coupling mechanisms exist in the simplest control schemes proposed for each ML-DAB converter (except for the 3L-DAB). These couplings, in principle, cause the modification of the unbalance

variables not associated to a given control variable. Decoupling mechanisms are proposed and simulation and experimental tests demonstrate its good performance in most cases. Nevertheless, such tests also show that the coupling phenomenon does not constitute a significant issue, since the control loop of each unbalance variable is able to correct any deviation caused by the rest of control loop actions.

- A study of the working range of the proposed capacitor-voltage-balancing controls shows that extremely high and low *d* values should be avoided, and a minimum phase-shift value should be guaranteed, in order to have a large enough in-phase component amplitude.
    - To ensure the capacitor voltage balancing on these conditions, an alternative modulation and control scheme is proposed for the 5L-DAB, that allows controlling the capacitor voltages with the charge provided by the in-quadrature component.
- A set of simple and closed-form expressions to define the modulation parameters is proposed and designated as practical solution. Such expressions are derived from the modulation-parameter values minimizing a set of objective functions. These functions are related to the conduction and switching losses of the 3L-DAB and 4L-DAB, each function independent of the converter constructive parameters.
    - The similarity between the 3L-DAB and 4L-DAB optimum results leads to expect similar results for higher number of levels. From this assumption, a general *N*-level practical solution is defined.
    - The objective function values obtained with the practical solutions are close to the minimum values obtained in the optimization and lower than those obtained with the conventional modulation (PSM) employed on the same converter.
    - The efficiency obtained with the 3L-DAB practical solution is compared with the efficiency obtained in the conventional 2L-DAB employing modulations PSM, TRM, and TZM. The proposed practical solution shows better and high efficiency values for the whole power and voltage-gain range.
- Simulation and experimental tests have shown that the capacitor-voltage-balancing controls, the output voltage control, and the practical solutions defining the modulation parameters can function simultaneously without impairing the interaction.
- The feasibility of ML-DAB converters configured with an asymmetric number of levels has been proved. Asymmetric configurations are advantageous in applications where

high or low dc-link voltage gains are required, since it allows using a single highly-optimized switching device in both converter sides, enabling high power conversion efficiencies and power density values, and a reduced cost thanks to economies of scale.

- Since the proposed ML-DAB topologies only increase the number of semiconductors (not the overall size of the passive components storing energy), highly compact implementations can be envisioned, with a better loss spreading and reduced heat sink requirements, and the overall cost could be competitive if popular devices were used with good performance and low cost due to economies of scale. However, the advantages obtained may or may not compensate the drawbacks (increased number of devices, increased control complexity, etc.) depending on the specific application. The optimum number of levels, representing a good trade-off between performance and practicability, will ultimately depend on the particularities of each specific application and the current state of the art in power semiconductor technology.
- The proposed ML-DAB converters could be advantageous in applications such as:
    - Interconnection of high-voltage dc (HVDC) links of the same or different voltage, where galvanic isolation is required.
    - It is possible to realize the interconnection of a HVDC link with an ac grid, by employing a two-stage system (a ML-DAB converter plus a ML dc-ac converter). In such application, galvanic isolation is usually required, and in most cases is implemented with a bulky and expensive grid frequency transformer. With the proposed implementation, the system cost and volume could be greatly reduced.
    - Interconnection of ac grids with a solid-state transformer (SST). The proposed asymmetric ML-DAB converters could be advantageous in SSTs when high voltage gains are required.
    - Interconnection of the traction battery and auxiliary systems battery in electrical vehicles, requiring high voltage gains. The charge balancing among the cells of each battery can be directly implemented with the ML-DAB converters, if individual cells or groups of cells are employed to generate the dc-link voltage levels.
    - Vehicle-to-grid power interfaces with active charge balancing of the battery cells, following the same idea of the previous point.

- These research contributions have already led to the publication of one journal paper [90] and two conference papers [91], [92].

7.2. Future research work

Among the many possible future extensions of the research reported in this thesis, we would like to highlight the following:

- Study the feasibility of multilevel half-bridge configurations on one side or both sides of the ML-DAB converter. Propose novel modulation strategies and control schemes for the capacitor balancing, if it is feasible and necessary.
- Compare the efficiency of the proposed converter for different number of voltage levels with the efficiency values obtained with the 2L-DAB converter employing relevant advanced alternative modulations presented in the literature.
- Study the feasibility of a multilevel three-phase DAB converter, especially regarding the capacitor voltage balancing.
- Identify the modulation parameter value ranges where soft switching occurs in the *N*L-DAB.
- Find the optimum modulation parameter values that minimize the dc-link capacitor rms current in the *N*L-DAB.

APPENDIX A.

EXPERIMENTAL EQUIPMENT

Abstract — This appendix contains a description of the experimental equipment employed.

A.1. Converter prototypes

This chapter presents the different converter prototypes employed to perform the required experimental tests. The control and modulation for each converter are implemented using dSpace processor board DS1006 and two or three (depending on the converter) synchronized dSpace digital waveform output boards DS5101 (each contains an FPGA). All the converter legs are built using the same printed circuit board, which allows building 4L-MAC legs, 3L-MAC legs, and half-bridge (two-level) legs, by only populating the required components and short-circuiting some through-hole connections. Moreover, such converter legs employ the same gate drivers (HCPL-316J), each one powered by a compact and internal gate-driver power-supply circuit, described in [84]. The same transformer is employed in all the converter prototypes, with n = 1, a stray inductance L = 300 μH, and a magnetizing inductance L_m = 12 mH.

A.1.1 3L-DAB prototype

Fig. A.1 presents the 3L-DAB prototype assembled for the experimental test of Chapter 2. It is implemented using four 3L-MAC legs (Chapter 2, Fig. 2.10) with 100 V - 20 A MOSFETs. The implemented switching sequence operation guarantees a blocking voltage of $V_Z/2$ across each switch, if capacitor voltages are balanced.

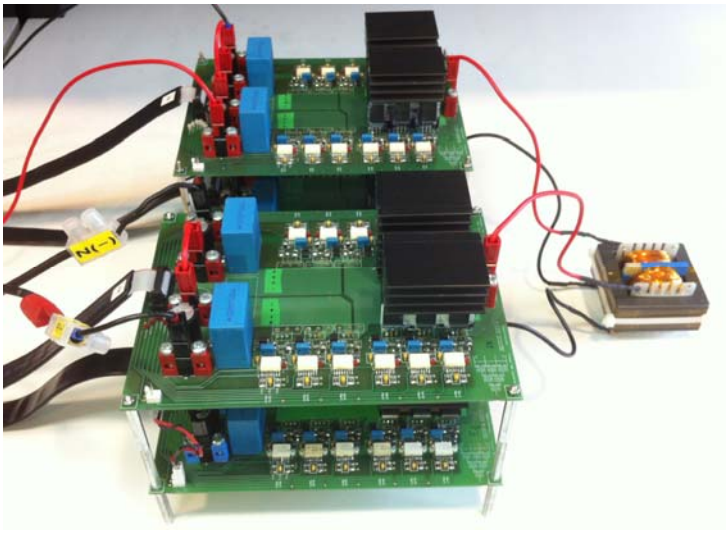


Fig. A.1. 3L-DAB prototype. Components: FDPF3860T MOSFETs and C_z = 103.4 μF.

A.1.2 4L-DAB prototype

Fig. A.2 presents the 4L-DAB prototype assembled for the experimental test of Chapter 3. It is implemented using four 4L-MAC legs (Chapter 3, Fig. 3.10) with 100 V – 20 A MOSFETs. It is operated according to [66], which guarantees a blocking voltage of $V_Z/3$ across each switch, if capacitor voltages are balanced.

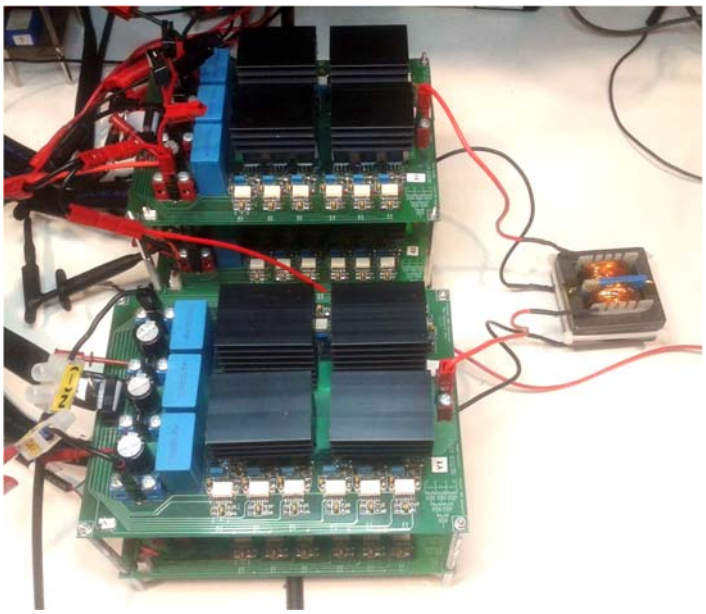


Fig. A.2. Four-level DAB prototype. Components: FDPF3860T MOSFETs, C_z = 103.4 μF.

A.1.3 Asymmetric DAB prototypes

This section presents the prototypes of the three converters assembled to perform the experimental tests in Chapter 6. Its common feature is that the number of voltage levels present in each dc-link is different. The four-level and three-level converter phase legs are operated as in the 4L-DAB and 3L-DAB converter prototypes, respectively. The two-level converter legs are operated as in the conventional FB-DAB.

A.1.3.1 3L-2L-DAB

Fig. A.3 presents the 3L-2L asymmetric DAB prototype, assembled to perform the required experimental tests. Side a is composed of two 3L-MAC legs, which employ 200 V – 18 A MOSFETs, while side b is composed of two half-bridge legs, which employ 500 V – 20 A MOSFETs.

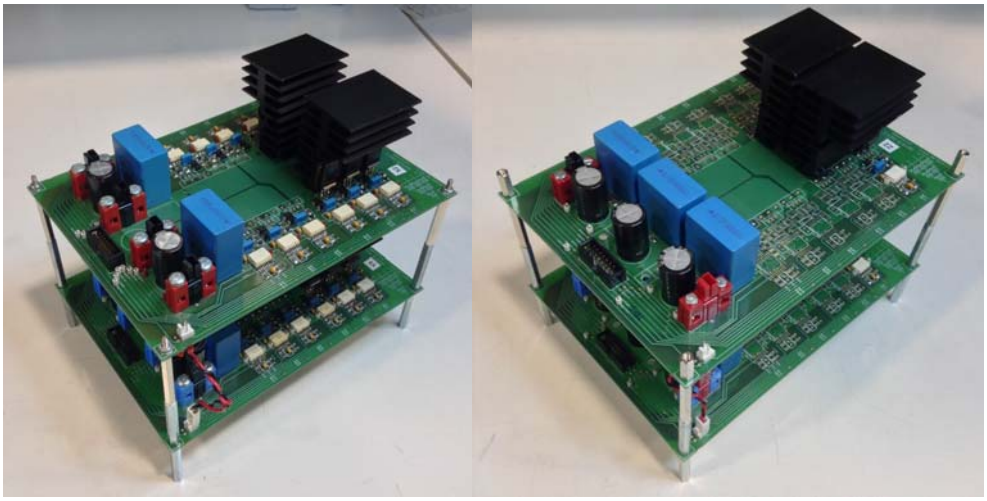


Fig. A.3. 3L-2L-DAB prototype (without the transformer) with three-level legs a_1 and a_2 (left) and two-level phases b_1 and b_2 (right). Components: STP20NF20 MOSFETs (a-side), IRFP460 MOSFETs (b-side), C_a = 103.4 μF, and C_b = 34.5 μF.

A.1.3.2 4L-2L-DAB

Fig. A.4 presents the 4L-2L asymmetric DAB prototype, assembled to perform the required experimental tests. Side a is composed of two 4L-MAC legs, which employ 100 V – 20 A MOSFETs, while side b is composed of two half-bridge legs, which employ 500 V – 20 A MOSFETs.

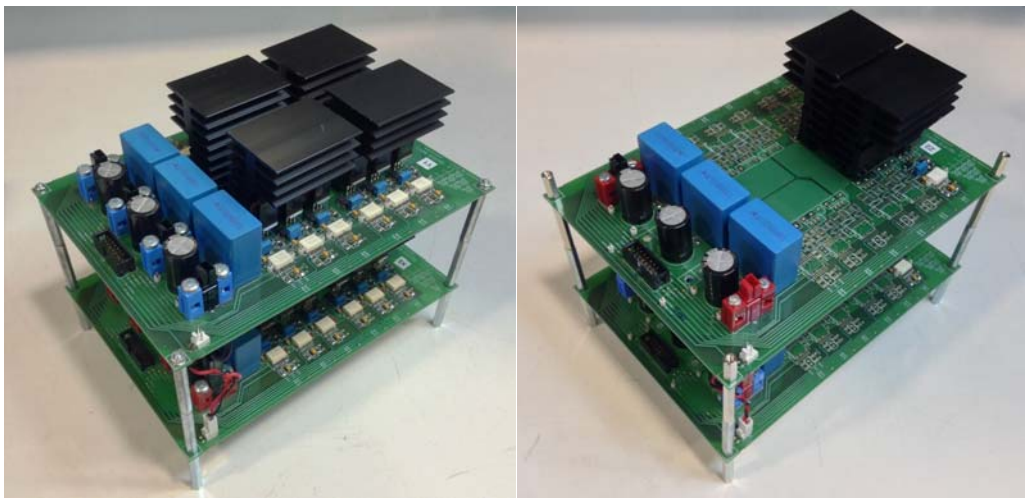


Fig. A.4. 4L-2L-DAB prototype (without the transformer) with four-level legs a_1 and a_2 (left) and two-level phases b_1 and b_2 (right). Components: FDPF3860T MOSFETs (a-side), IRFP460 MOSFETs (b-side), C_a = 103.4 μF, and C_b = 34.5 μF.

A.1.3.3 4L-3L-DAB

Fig. A.5 presents the 4L-3L asymmetric DAB prototype, assembled to perform the required experimental tests. Side a is composed of two 4L-MAC legs, which employ 100 V – 20 A MOSFETs, while side b is composed of two 3L-MAC legs, which employ 200 V – 18 A MOSFETs.

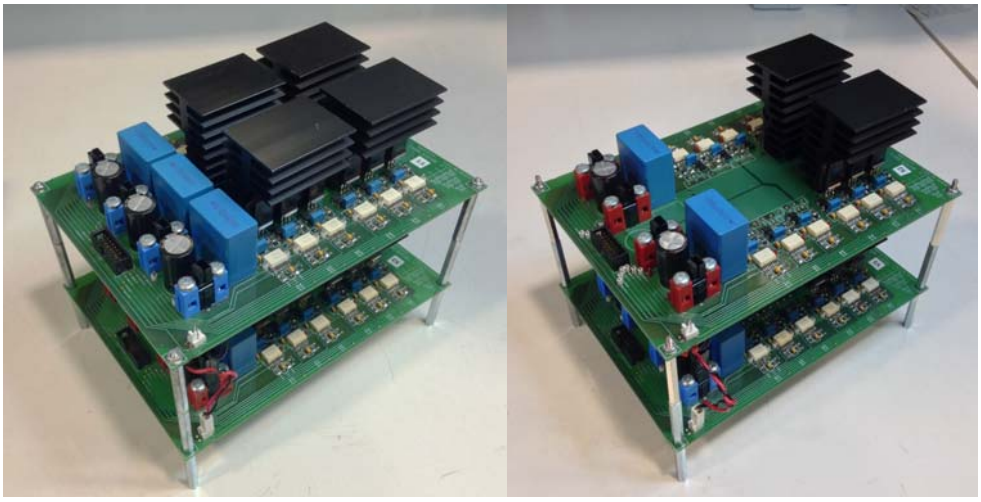


Fig. A.5. 4L-3L-DAB prototype (without the transformer) with four-level legs a_1 and a_2 (left) and three-level phases b_1 and b_2 (right). Components: FDPF3860T MOSFETs (a-side), STP20NF20 MOSFETs (b-side), C_z = 103.4 μF.

A.2. dSpace system

In most performed experiments, the ML-DAB converter modulation strategy and control schemes, and the generation of the switch control signals have been implemented using a dSpace system based on processor board DS1006. Fig. A.6 presents a picture of the dSpace expansion box inside which the different dSpace boards are placed.

Fig. A.6. dSpace system.

The dSpace expansion box contains the following used boards:

- 1 DS1006 processor board.
- 3 DS5101 digital waveform output (DWO) boards.
- 1 DS2004 A/D board.

A.3. Dc power sources

Fig. A.7 presents a picture of the three dc power sources used to supply a dc voltage to the ML-DAB converter sourced dc link, to maintain a minimum dc-voltage value on the load-side dc link, or to maintain fixed dc-link capacitor voltages during early-stage experiments. Power supply 1 corresponds to model 6030A from HP, power supply 2 corresponds to model SPS80-82 from Amrel, and power supply 3 corresponds to model 5001-I from California Instruments. Other power sources with lower power rating have also been used to supply auxiliary circuits like, for example, gate-driver logic circuitry and voltage sensors.

Fig. A.7. Dc power supplies.

Table A.1, Table A.2, and Table A.3 show the main specifications of the three power supplies.

Maximum dc voltage	200 V
Maximum dc current	17 A
Maximum power	1 kW

Table A.1. Dc power supply HP 6030A specifications.

Maximum dc voltage	80 V
Maximum dc current	82 A
Maximum power	6.6 kW

Table A.2. Dc power supply Amrel SPS80-82 specifications.

Maximum dc voltage	300 V
Maximum dc current	16.6 A
Maximum power	5 kW

Table A.3. Dc power supply California Instruments 5001-I specifications.

A.4. Loads

The resistive load connected to the load side of the ML-DAB converter, is formed by the three-phase resistive loads shown in Fig. A.8 plus the electronic load from HP shown in Fig. A.9. Since this is a dc system, the three-phase load is used in an unconventional mode. Different configurations are employed in order to obtain the desired resistance value, e.g., an individual phase, two phases in series, two or three phases in parallel, or one phase in series with two phases in parallel. The electronic load is connected in series with the passive load in order to finely adjust the desired load resistance value.

Fig. A.8. Three-phase resistive load in star configuration with accessible neutral point.

Fig. A.9. Electronic load from HP composed of mainframe model 6050A and three power modules model 60504B with a maximum power, voltage and current of 600 W, 60 V, and 120 A, respectively, per module.

A.5. Scopes

Fig. A.10 and Fig. A.11 show the two scopes used to obtain experimental results. Tektronix MSO 3054 scope was used in the experimental tests with the ML-DAB converters. Tektronix TDS 714L scope was used in conjunction with the double pulse board (Section A.6), to obtain the experimental switching losses values for Chapter 2, Section 2.7.

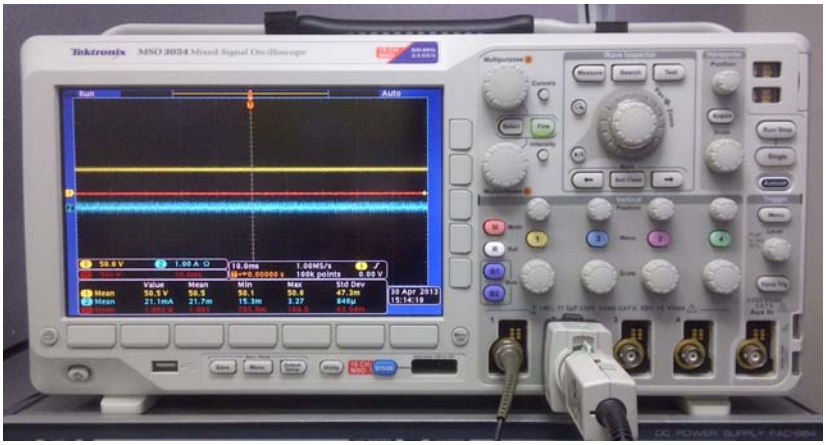


Fig. A.10. Tektronix MSO 3054 scope.

Fig. A.11. Tektronix TDS 714L scope.

A.6. Double-pulse board

The double-pulse board (Fig. A.12) is employed as a test bed to measure the switching losses a particular MOSFET or IGBT. It has been used to obtain the switching losses of MOSFETs FDPF3860T and STF20NF20 in order to compare the efficiency values obtained with the proposed 3L-DAB and the conventional 2L-DAB.

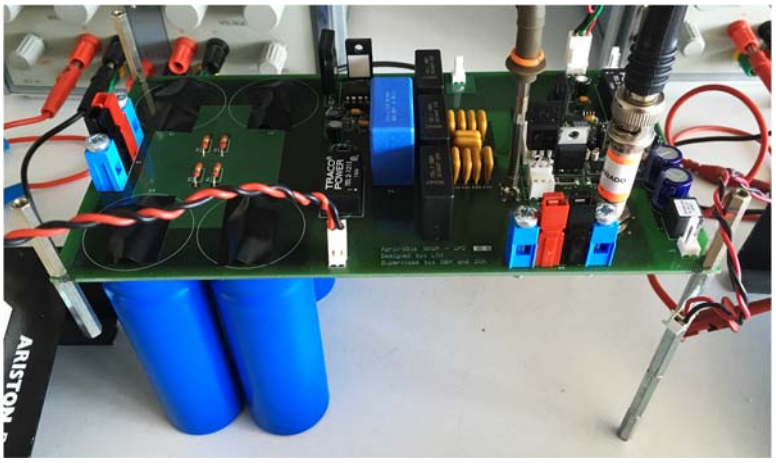


Fig. A.12. Double-pulse board used to measure device switching losses.

APPENDIX B.

LIMITATION OF THE SWITCHING ANGLE VALUES

Abstract — This appendix proposes an algorithm that corrects the switching angles when any value is outside of the predefined boundaries.

The switching angles outputted by the proposed capacitor-voltage-balancing control schemes (α_{zik} and α_{zok}) may not meet the restrictions (5.1) imposed by the modulation. This is because α_{zik} and α_{zok} values result from the product of switching angles α_{zk} (which already meet (5.1) if the practical solution is employed) with control variables u_{zm}, which may take any arbitrary value outputted by the controller.

This appendix proposes an algorithm, which modifies the (inner or outer) z-side switching angles outputted by any of the proposed control schemes in order to meet the restrictions.

In practice, the required blanking time ($t_{b,z}$) between the turn-off of a switch and the turn-on of another in a z-side leg switching transition, forces a minimum margin between adjacent switching angles α_{zxk} and $\alpha_{zx(k+1)}$, where $x \in \{i,o\}$. This margin is defined as

$$\Delta\alpha_{z,\min} = t_{b,z} \cdot f_s \cdot 360°. \tag{B.1}$$

Taking into account practical considerations, restrictions (5.1) are redefined as

$$\begin{gathered} \alpha_{z,\text{bot}} \le \alpha_{zx1} \\ \vdots \\ \alpha_{zxk} + \Delta\alpha_{z,\min}/2 \le \alpha_{zx(k+1)} - \Delta\alpha_{z,\min}/2 \\ \vdots \\ \alpha_{zxM} \le \alpha_{z,\text{top}} \end{gathered} \tag{B.2}$$

where $k \in \{1,2,\ldots,M-1\}$, $\alpha_{z,\text{bot}}$ is the minimum value that α_{zi1} and α_{zo1} can take, and $\alpha_{z,\text{top}}$ is the maximum value that α_{ziM} and α_{zoM} can take. In order to be able to transfer the converter maximum power, $\alpha_{z,\text{top}}$ is generally set to 90º. Limit $\alpha_{z,\text{bot}}$ could be set to -90º. Nevertheless, the implementation of such feature in the experimental platform has proved to be complex. Therefore, $\alpha_{z,\text{bot}} = 0º$ is set for all the experimental tests.

The flow chart of the proposed algorithm is shown in Fig. B.1.

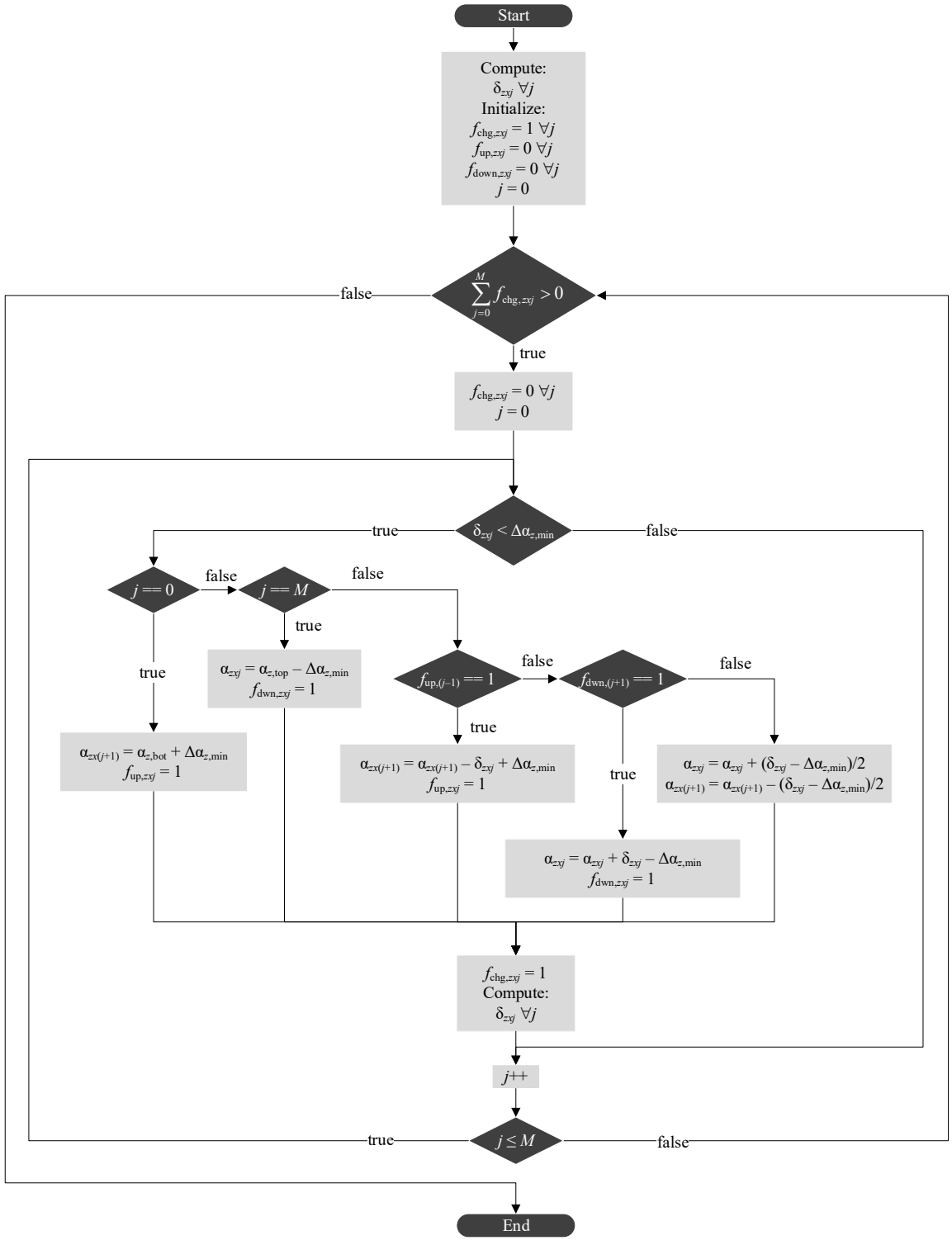


Fig. B.1. Generalized algorithm to limit the inner or outer switching angles outputted by the z-side control scheme of an NL-DAB or an N_aL-N_bL-DAB.

First, the actual differences between the switching angles are computed, as well as the differences between $\alpha_{z,\text{bot}}$ and α_{zx1}, and between α_{zxM} and $\alpha_{z,\text{top}}$. Such differences, shown in Fig. B.2, are stored in vector

$$\begin{aligned}\boldsymbol{\delta}_{zx} &= \left(\delta_{zx0},\delta_{zx1},\ldots,\delta_{zxj},\ldots,\delta_{zxM}\right) \\ &= \left(\alpha_{zx1}-\alpha_{z,\text{bot}},\alpha_{zx2}-\alpha_{zx1},\ldots,\alpha_{zx(j+1)}-\alpha_{zxj},\ldots,\alpha_{z,\text{top}}-\alpha_{zxM}\right).\end{aligned} \tag{B.3}$$

The basic idea of the algorithm is, whenever the difference between two adjacent switching angles, e.g. $\delta_{zxj} = \alpha_{zx(j+1)} - \alpha_{zxj}$, is smaller than $\Delta\alpha_{z,\text{min}}$, switching angles α_{zxj} and $\alpha_{zx(j+1)}$ are recomputed as the average value of both angles plus $\Delta\alpha_{z,\text{min}}/2$ and minus $\Delta\alpha_{z,\text{min}}/2$, respectively. Nevertheless, some special cases exist where the strategy to amend δ_{zxj} is different. For instance, to amend δ_{zx0}, only switching angle α_{zx1} can be modified. After the modification of α_{zx1}, δ_{zx1} might become smaller than $\Delta\alpha_{z,\text{min}}$. In such case, the proper action is modifying only α_{zx2}, since modifying both angles would undo δ_{zx0} correction. These special cases might also occur on further adjacent δ_{zxj}. It can also occur on the other extreme of vector $\boldsymbol{\delta}_{zx}$; i.e., when δ_{zxM} is smaller than $\Delta\alpha_{z,\text{min}}$ and the only way to amend it, is to decrease α_{zxM}. Binary variables $f_{\text{up},zxj}$ and $f_{\text{dwn},zxj}$ are used to indicate whether difference δ_{zxj} has been corrected by moving $\alpha_{zx(j+1)}$ or α_{zxj}, respectively.

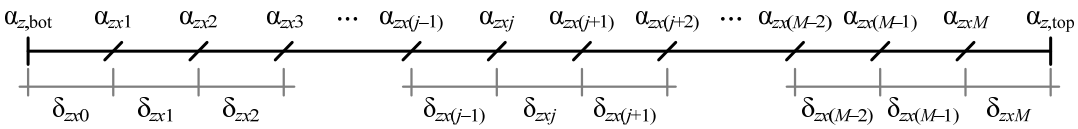


Fig. B.2. General distribution of switching angles, its minimum and maximum limits, and differences between them.

The proposed algorithm works iteratively. In each iteration, the validity of each δ_{zxj} is checked sequentially, beginning at $j = 0$ and ending at $j = M$. Every time a given δ_{zxj} is corrected, its associated binary variable $f_{\text{chg},zxj}$ is set to one. If $f_{\text{up},zx(j-1)} = 1$, then δ_{zxj} is corrected by modifying only $\alpha_{zx(j+1)}$ and $f_{\text{up},zxj}$ is set to one. On the other hand, if $f_{\text{dwn},zx(j+1)} = 1$, δ_{zxj} is corrected by modifying only α_{zxj} and $f_{\text{dwn},zxj}$ is set to one. Hence, any $f_{\text{up},zxj}$ will be equal to one only and only if $f_{\text{up},zx1} = 1$, and any $f_{\text{dwn},j}$ will be equal to one only and only if $f_{\text{dwn},zxM} = 1$.

At the beginning of each iteration, all $f_{\text{chg},zxj}$ are reset. If at the end of an iteration, all $f_{\text{chg},zxj}$ are equal to zero, it means that no switching angles were modified in the last iteration, and hence, the algorithm ends. The computed switching angles are given as an output.

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