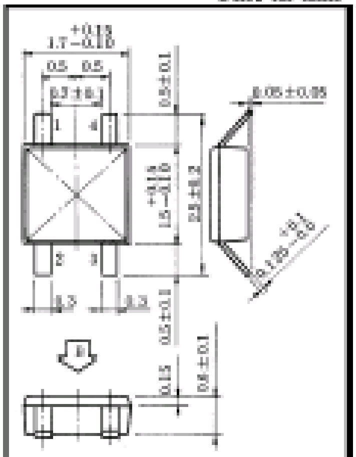
TOSHIBA HALL SENSOR GaAs ION IMPLANTED PLANAR TYPE

THS118

HIGH STABILITY MOTOR CONTROL.
DIGITAL TACHOMETER.
CRANK SHAFT POSITION SENSOR.

- Super Small Package.
- Excellent Temperature Characteristics.
- Wide Operating Temperature Range. (; −55~125°C)
- Excellent Output Voltage Linearity.

Unit in mm



1 (+) – 3 (–) (INPUT)
2 (+) – 4 (–) (OUTPUT)

JEDEC	—
EIAJ	—
TOSHIBA	10-2A1A

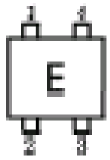
Weight : 0.0047g

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Control Current	DC	I_C	10**	mA
	1s		15**	
Power Dissipation		P_D	100**	mW
Operating Temperature Range		T_{opr}	−55~125	°C
Storage Temperature Range		T_{stg}	−55~150	°C

** Mounted on a printed circuit board.

MARKING



ELECTRICAL CHARACTERISTICS (Ta = 25°C)

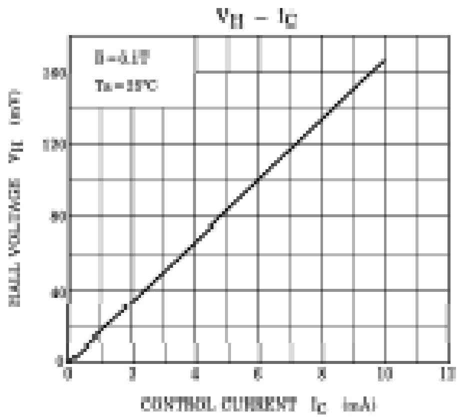
CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Internal Resistance (Input)	R_d	I_C = 5mA	450	—	900	Ω
Residual Voltage Ratio	V_{HO}/V_H	I_C = 5mA, B = 0 / B = 0.1T	—	—	±10	%
Hall Voltage (Note 1)	V_H	I_C = 5mA, B = 0.1T	55	—	140	mV
Temperature Coefficient (Note 2)	V_{HT}	I_C = 5mA, B = 0.1T T1 = 25°C, Ta = 125°C	—	—	−0.06	% / °C
Linearity (Note 3)	ΔK_H	I_C = 5mA, B1 = 0.1T, B2 = 0.5T	—	—	2	%
Specific Sensitivity (Note 4)	K*	I_C = 5mA, B = 0.1T	—	27	—	$\times 10^{-2}$ / T
Internal Resistance (Output)	R_{OUT}	I_C = 5mA	580	—	1350	Ω

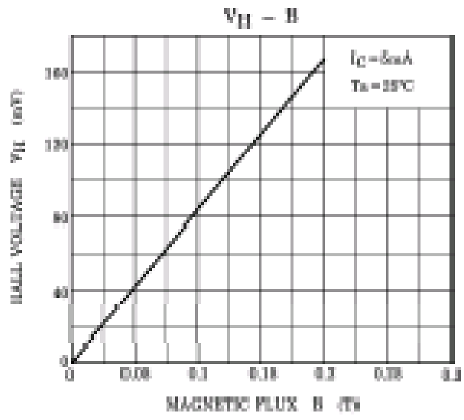
Note 1 : $V_H = V_{HM} - V_{HO}$ (V_{HM} is meter indication)

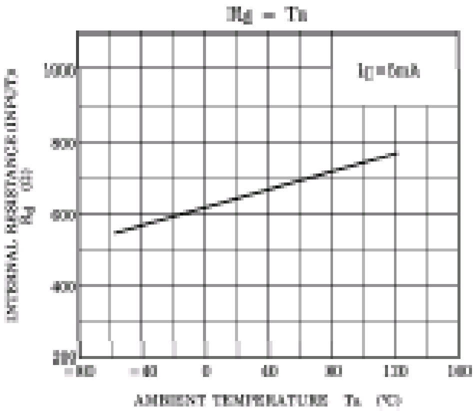
Note 2 : $V_{HT} = \frac{1}{V_{H(T1)}} \cdot \frac{V_{H(T2)} - V_{H(T1)}}{T2 - T1} \times 100\ (\%/°C)$ V_{HO} : Residual Voltage

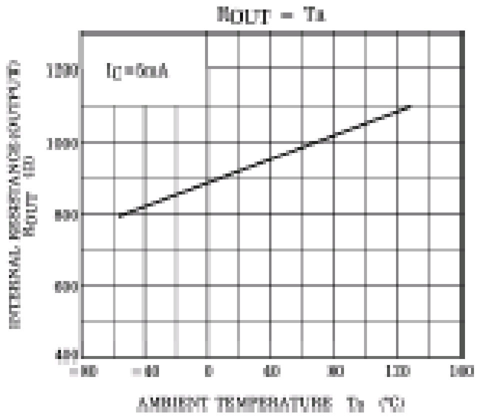
Note 3 : $\Delta K_H = \frac{K_{H(B2)} - K_{H(B1)}}{1/2\{K_{H(B1)} + K_{H(B2)}\}} \times 100 (\%)$, $K_H = \frac{V_H}{I_C \cdot B}$ K_H : Product Sensitivity

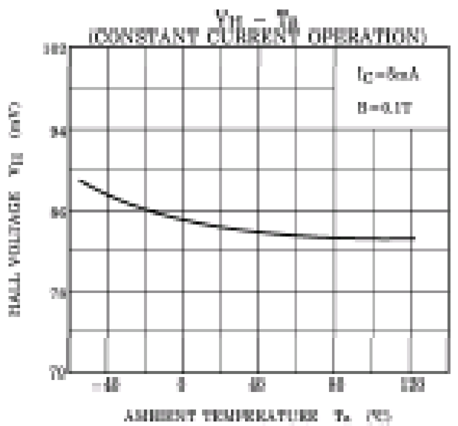
Note 4 : $K^* = V_H / (R_d \times I_C \times B) = K_H / R_d$

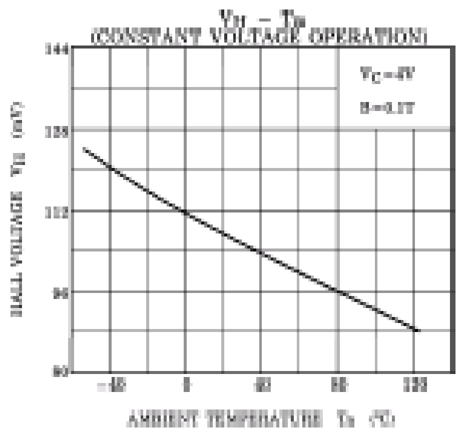

VH – IC
B = 0.1T
Ta = 25°C
HALL VOLTAGE VH (mV)
CONTROL CURRENT IC (mA)


VH – B
IC = 5mA
Ta = 25°C
HALL VOLTAGE VH (mV)
MAGNETIC FLUX B (T)


Rd – Ta
IC = 5mA
AMBIENT TEMPERATURE Ta (°C)


ROUT – Ta
IC = 5mA
AMBIENT TEMPERATURE Ta (°C)


VH – Ta
(CONSTANT CURRENT OPERATION)
IC = 5mA
B = 0.1T
HALL VOLTAGE VH (mV)
AMBIENT TEMPERATURE Ta (°C)


VH – Ta
(CONSTANT VOLTAGE OPERATION)
B = 0.1T
HALL VOLTAGE VH (mV)
AMBIENT TEMPERATURE Ta (°C)

TIL111, TIL114, TIL116, TIL117
OPTOCOUPLERS

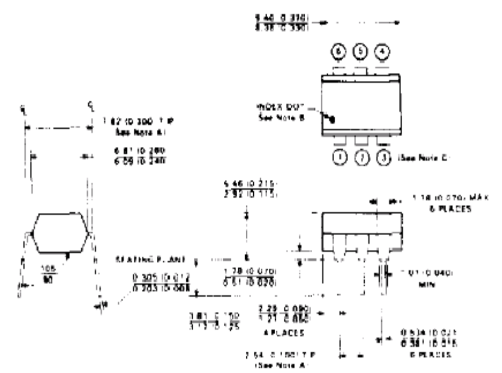
SOOS040 D1607, NOVEMBER 1973–REVISED FEBRUARY 1983

COMPATIBLE WITH STANDARD TTL INTEGRATED CIRCUITS

- **Gallium Arsenide Diode Infrared Source Optically Coupled to a Silicon N-P-N Phototransistor**
- **High Direct-Current Transfer Ratio**
- **High-Voltage Electrical Isolation . . . 1.5-kV or 2.5-kV Rating**
- **Plastic Dual-In-Line Package**
- **High-Speed Switching: t_r = 5 μs, t_f = 5 μs Typical**

mechanical data

The package consists of a gallium arsenide infrared-emitting diode and an n-p-n silicon phototransistor mounted on a 6-lead frame encapsulated within an electrically nonconductive plastic compound. The case will withstand soldering temperature with no deformation and device performance characteristics remain stable when operated in high-humidity conditions. Unit weight is approximately 0.52 grams.



NOTES:

a. Leads are within 0.13 mm (0.005 inch) radius of true position (T.P.) with maximum material condition and unit installed.

b. Pin 1 identified by index dot.

c. Terminal connections:

1. Anode } Infrared-emitting diode
2. Cathode
3. No internal connection
4. Emitter } Phototransistor
5. Collector
6. Base

FALLS WITHIN JEDEC MO-001AM DIMENSIONS

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Input-to-Output Voltage: TIL111	±1.5 kV
TIL114, TIL116, TIL117	±2.5 kV
Collector-Base Voltage	70 V
Collector-Emitter Voltage (See Note 1)	30 V
Emitter-Collector Voltage	7 V
Emitter-Base Voltage	7 V
Input-Diode Reverse Voltage	3 V
Input Diode Continuous Forward Current at (or below) 25°C Free-Air Temperature (See Note 2)	100 mA
Continuous Power Dissipation at (or below) 25°C Free-Air Temperature:	
Infrared-Emitting Diode (See Note 3)	150 mW
Phototransistor (See Note 4)	150 mW
Total, Infrared-Emitting Diode plus Phototransistor (See Note 5)	250 mW
Storage Temperature Range	−55°C to 150°C
Lead Temperature 1,6 mm (1/16 Inch) from Case for 10 Seconds	260°C

NOTES: 1. This value applies when the base emitter diode is open circuited.
2. Derate linearly to 100°C free-air temperature at the rate of 1.33 mA/°C.
3. Derate linearly to 100°C free-air temperature at the rate of 2 mW/°C.
4. Derate linearly to 100°C free-air temperature at the rate of 2 mW/°C.
5. Derate linearly to 100°C free-air temperature at the rate of 3.33 mW/°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TIL111, TIL114, TIL116, TIL117 OPTOCOUPLERS

electrical characteristics at 25°C free-air temperature

PARAMETER			TEST CONDITIONS	TIL111 TIL114 MIN	TIL111 TIL114 TYP	TIL111 TIL114 MAX	TIL116 MIN	TIL116 TYP	TIL116 MAX	TIL117 MIN	TIL117 TYP	TIL117 MAX	UNIT
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage		$I_C = 10\ \mu A$, $I_E = 0$, $I_F = 0$	70			70			70			V
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage		$I_C = 1\ mA$, $I_B = 0$, $I_F = 0$	30			30			30			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage		$I_E = 10\ \mu A$, $I_C = 0$, $I_F = 0$	7			7			7			V
I_R	Input Diode Static Reverse Current		$V_R = 3\ V$			10			10			10	µA
$I_{C(on)}$	On-State Collector Current	Phototransistor Operation	$V_{CE} = 0.4\ V$, $I_F = 16\ mA$, $I_B = 0$	2	7								mA
			$V_{CE} = 10\ V$, $I_F = 10\ mA$, $I_B = 0$				2	5		5	9		mA
		Photodiode Operation	$V_{CB} = 0.4\ V$, $I_F = 16\ mA$, $I_E = 0$	7	20		7	20		7	20		µA
$I_{C(off)}$	Off-State Collector Current	Phototransistor Operation	$V_{CE} = 10\ V$, $I_F = 0$, $I_B = 0$		1	50		1	50		1	50	nA
		Photodiode Operation	$V_{CB} = 10\ V$, $I_F = 0$, $I_E = 0$		0.1	20		0.1	20		0.1	20	nA
h_{FE}	Transistor Static Forward Current Transfer Ratio		$V_{CE} = 5\ V$, $I_C = 10\ mA$, $I_F = 0$	100	300					200	550		
			$V_{CE} = 5\ V$, $I_C = 100\ \mu A$, $I_F = 0$				100	300					
V_F	Input Diode Static Forward Voltage		$I_F = 16\ mA$		1.2	1.4					1.2	1.4	V
			$I_F = 60\ mA$					1.25	1.5				V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage		$I_C = 2\ mA$, $I_F = 16\ mA$, $I_B = 0$		0.25	0.4							V
			$I_C = 2.2\ mA$, $I_F = 15\ mA$, $I_B = 0$					0.25	0.4				V
			$I_C = 0.5\ mA$, $I_F = 10\ mA$, $I_B = 0$								0.25	0.4	V
r_{IO}	Input-to-Output Internal Resistance		$V_{in-out} = \pm 1.5\ kV$ for TIL111, $\pm 2.5\ kV$ for all others, See Note 6	10^{11}			10^{11}			10^{11}			Ω
C_{io}	Input-to-Output Capacitance		$V_{in-out} = 0$, $f = 1\ MHz$, See Note 6		1	1.3		1	1.3		1	1.3	pF

NOTE 6 These parameters are measured between both input diode leads shorted together and all the phototransistor leads shorted together.

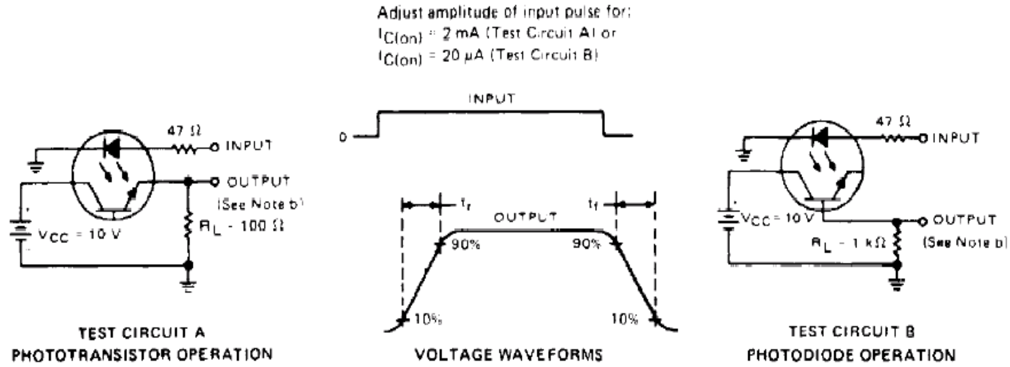
switching characteristics at 25°C free-air temperature

PARAMETER			TEST CONDITIONS	TIL111 TIL114 MIN	TIL111 TIL114 TYP	TIL111 TIL114 MAX	TIL116 MIN	TIL116 TYP	TIL116 MAX	TIL117 MIN	TIL117 TYP	TIL117 MAX	UNIT
t_r	Rise Time	Phototransistor Operation	$V_{CC} = 10\ V$, $I_{C(on)} = 2\ mA$, $R_L = 100\ \Omega$, See Test Circuit A of Figure 1		5	10		5	10		5	10	µs
t_f	Fall Time				5	10		5	10		5	10	µs
t_r	Rise Time	Photodiode Operation	$V_{CC} = 10\ V$, $I_{C(on)} = 20\ \mu A$, $R_L = 1\ k\Omega$, See Test Circuit B of Figure 1		1			1			1		µs
t_f	Fall Time				1			1			1		µs

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION



NOTES a. The input waveform is supplied by a generator with the following characteristics: Z_{out} = 50 Ω, t_r ≤ 15 ns, duty cycle ≈ 1%, t_w = 100 µs

b. The output waveform is monitored on an oscilloscope with the following characteristics: t_r ≤ 12 ns, R_{in} ≥ 1 MΩ, C_{in} ≤ 20 pF.

FIGURE 1—SWITCHING TIMES

TYPICAL CHARACTERISTICS

TIL111, TIL114

COLLECTOR CURRENT
vs
INPUT-DIODE FORWARD CURRENT

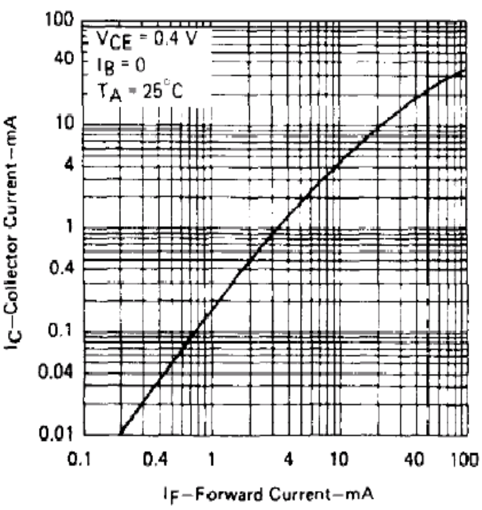


FIGURE 2

TIL116, TIL117

COLLECTOR CURRENT
vs
INPUT-DIODE FORWARD CURRENT

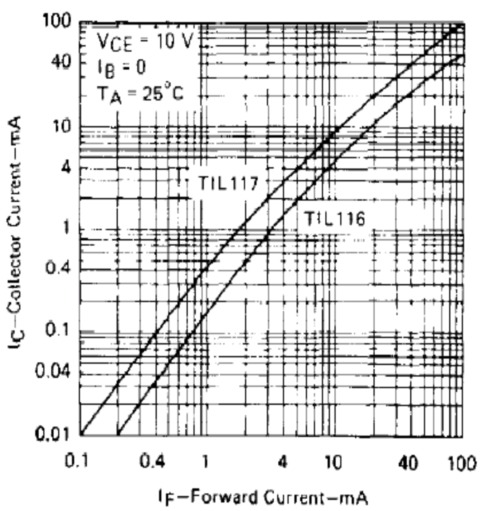


FIGURE 3

TEXAS INSTRUMENTS
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TIL111, TIL114, TIL116, TIL117
OPTOCOUPLERS

TYPICAL CHARACTERISTICS

TIL111, TIL114

COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

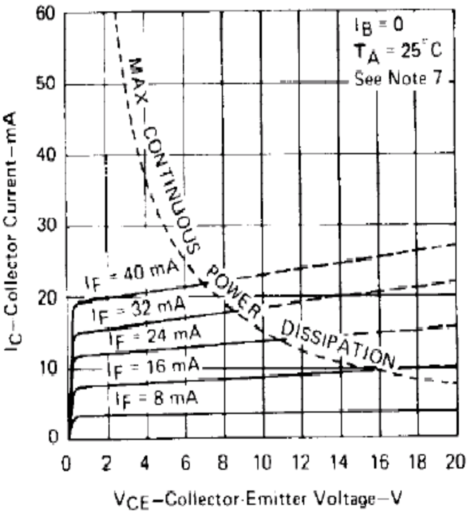


FIGURE 4

TIL116

COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

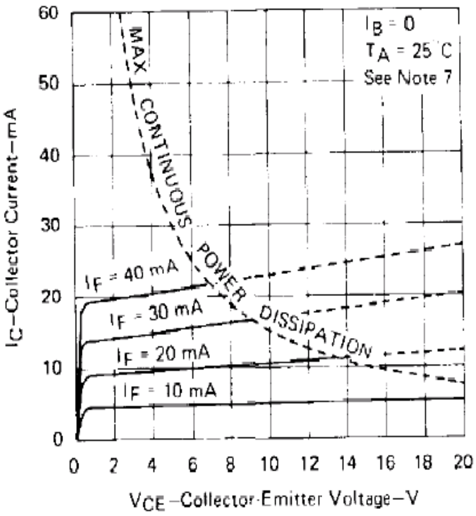


FIGURE 5

TIL117

COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

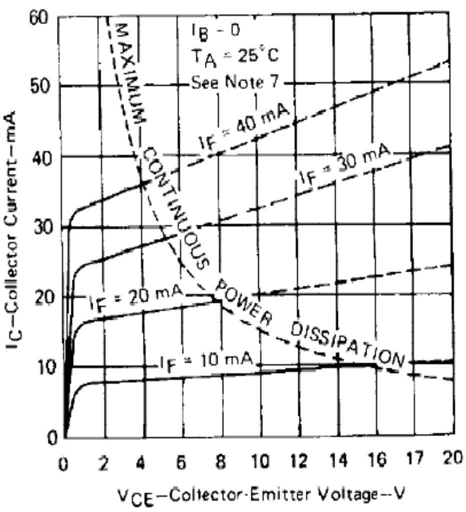


FIGURE 6

RELATIVE ON-STATE COLLECTOR CURRENT
vs
FREE-AIR TEMPERATURE

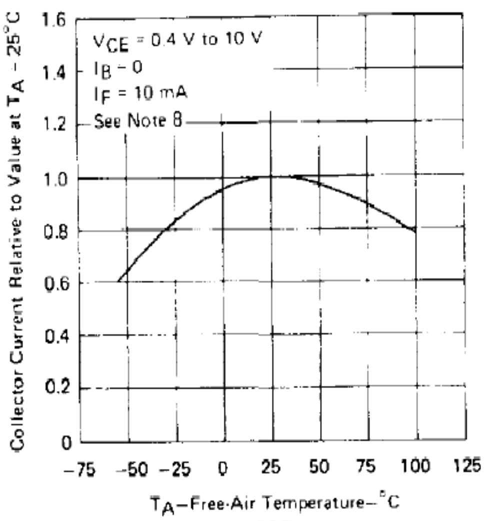


FIGURE 7

NOTES 7. Pulse operation of input diode is required for operation beyond limits shown by dotted lines.
8. These parameters were measured using pulse techniques. t_w = 1 ms, duty cycle ≤ 2%

TYPICAL CHARACTERISTICS

OFF-STATE COLLECTOR CURRENT
vs
FREE-AIR TEMPERATURE

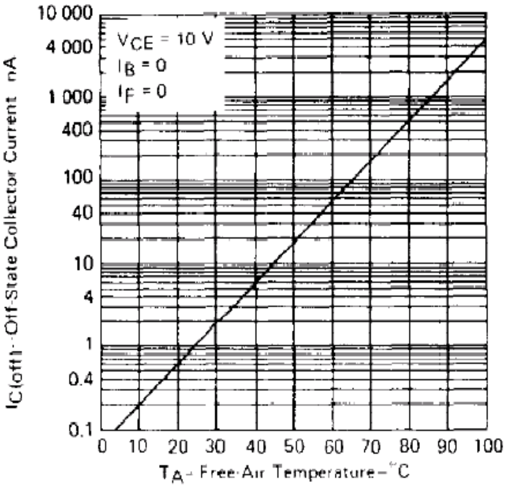


FIGURE 8

NORMALIZED TRANSISTOR STATIC FORWARD
CURRENT TRANSFER RATIO
vs
ON-STATE COLLECTOR CURRENT

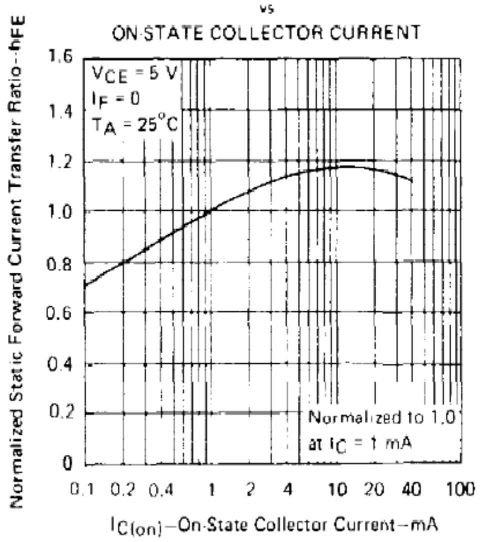


FIGURE 9

INPUT DIODE FORWARD
CONDUCTION CHARACTERISTICS

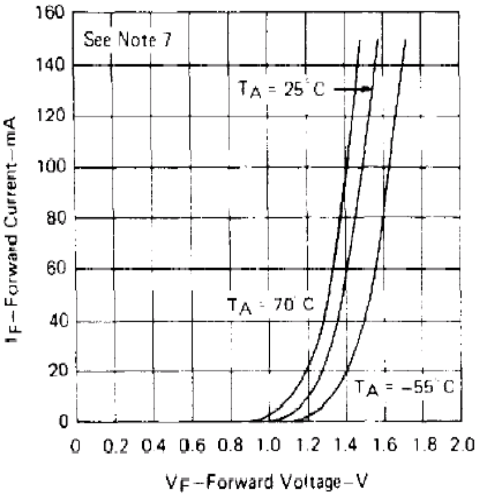


FIGURE 10

COLLECTOR CURRENT
vs
MODULATION FREQUENCY

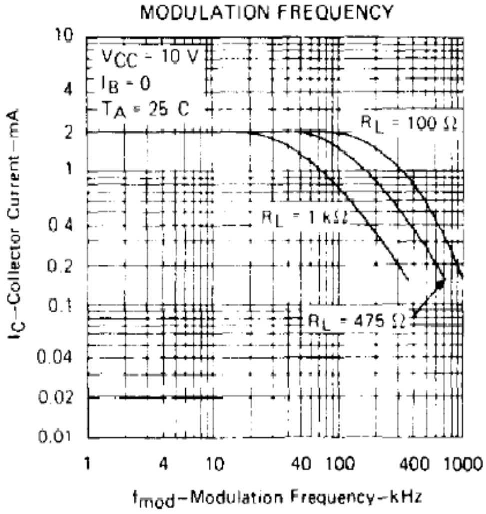


FIGURE 11

NOTE 7: These parameters were measured using pulse techniques. t_w = 1 ms, duty cycle ≤ 2%

SGS-THOMSON MICROELECTRONICS

TIP120/121/122
TIP125/126/127

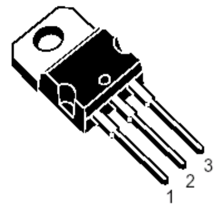
COMPLEMENTARY SILICON POWER DARLINGTON TRANSISTORS

- SGS-THOMSON PREFERRED SALESTYPES

DESCRIPTION

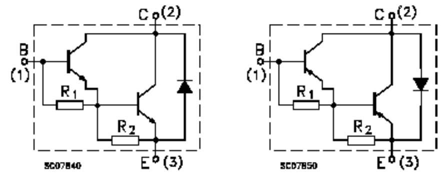
The TIP120, TIP121 and TIP122 are silicon epitaxial-base NPN power transistors in monolithic Darlington configuration Jedec TO-220 plastic package, intented for use in power linear and switching applications.

The complementary PNP types are TIP125, TIP126 and TIP127.



TO-220

INTERNAL SCHEMATIC DIAGRAM



R_1 Typ. = 5 KΩ R_2 Typ. = 150 Ω

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value			Unit
		NPN	TIP120	TIP121	TIP122	
		PNP	TIP125	TIP126	TIP127	
V_{CBO}	Collector-Base Voltage (I_E = 0)		60	80	100	V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)		60	80	100	V
V_{EBO}	Emitter-Base Voltage (I_C = 0)		5			V
I_C	Collector Current		5			A
I_{CM}	Collector Peak Current		8			A
I_B	Base Current		0.1			A
P_{tot}	Total Dissipation at $T_{case} \leq 25$ °C $T_{amb} \leq 25$ °C		65 2			W W
T_{stg}	Storage Temperature		-65 to 150			°C
T_j	Max. Operating Junction Temperature		150			°C

* For PNP types voltage and current values are negative.

THERMAL DATA

$R_{thj-case}$	Thermal Resistance Junction-case	Max	1.92	°C/W
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max	62.5	°C/W

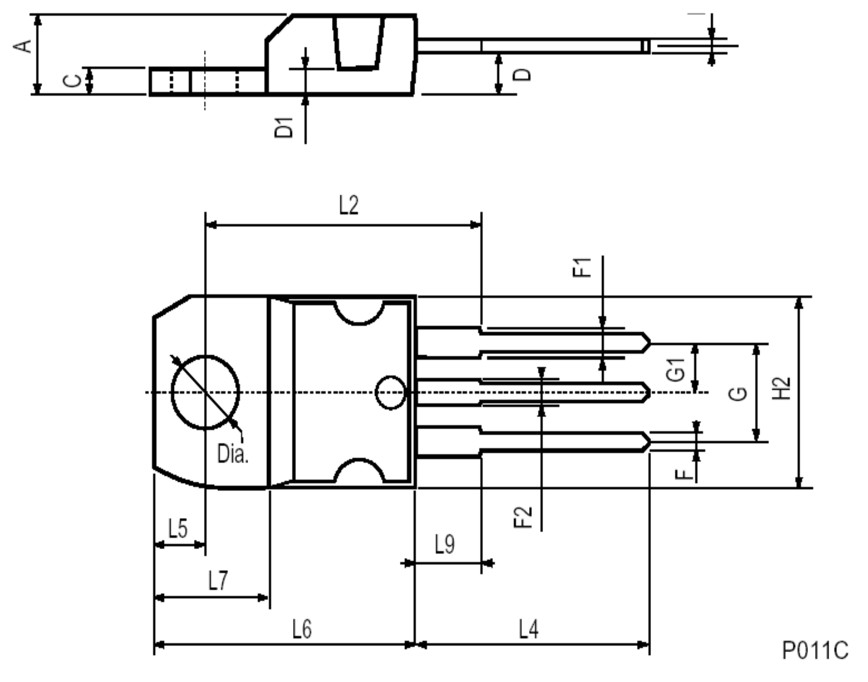
ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
I_{CEO}	Collector Cut-off Current (I_B = 0)	for **TIP120/125** for **TIP121/126** for **TIP122/127**	**V**$_{CE}$ = 30 V V_{CE} = 40 V V_{CE} = 50 V			0.5 0.5 0.5	mA mA mA
I_{CBO}	Collector Cut-off Current (I_B = 0)	for **TIP120/125** for **TIP121/126** for **TIP122/127**	**V**$_{CE}$ = 60 V V_{CE} = 80 V V_{CE} = 100 V			0.2 0.2 0.2	mA mA mA
I_{EBO}	Emitter Cut-off Current (I_C = 0)	V_{EB} = 5 V				2	mA
$V_{CEO(sus)}$*	Collector-Emitter Sustaining Voltage (I_B = 0)	I_C = 30 mA for **TIP120/125** for **TIP121/126** for **TIP122/127**		 60 80 100			 V V V
$V_{CE(sat)}$*	Collector-Emitter Saturation Voltage	I_C = 3 A I_C = 5 A	I_B = 12 mA I_B = 20 mA			2 4	V V
$V_{BE(on)}$*	Base-Emitter Voltage	I_C = 3 A	V_{CE} = 3 V			2.5	V
h_{FE}*	DC Current Gain	I_C = 0.5 A I_C = 3 A	V_{CE} = 3 V V_{CE} = 3 V	1000 1000			

* For PNP types voltage and current values are negative.

TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



TL071, TL071A, TL071B, TL072 TL072A, TL072B, TL074, TL074A, TL074B LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS

SLOS080D – SEPTEMBER 1978 – REVISED AUGUST 1996

- Low Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- Low Total Harmonic Distortion 0.003% Typ
- Low Noise V_n = 18 nV/√Hz Typ at f = 1 kHz
- High Input Impedance . . . JFET Input Stage
- Internal Frequency Compensation
- Latch-Up-Free Operation
- High Slew Rate . . . 13 V/μs Typ
- Common-Mode Input Voltage Range Includes V_{CC+}

description

The JFET-input operational amplifiers in the TL07_ series are designed as low-noise versions of the TL08_ series amplifiers with low input bias and offset currents and fast slew rate. The low harmonic distortion and low noise make the TL07_ series ideally suited for high-fidelity and audio preamplifier applications. Each amplifier features JFET inputs (for high input impedance) coupled with bipolar output stages integrated on a single monolithic chip.

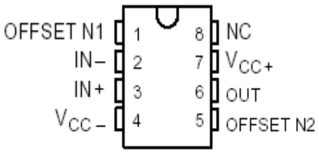
The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

AVAILABLE OPTIONS

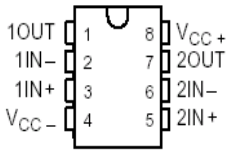
T_A	V_{IO}max AT 25°C	PACKAGE							
		SMALL OUTLINE (D)†	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	PLASTIC DIP (N)	PLASTIC DIP (P)	TSSOP PACKAGE (PW)	FLAT PACKAGE (W)
0°C to 70°C	10 mV 6 mV 3 mV	TL071CD TL071ACD TL071BCD	—	—	—	—	TL071CP TL071ACP TL071BCP	TL071CPWLE — —	—
	10 mV 6 mV 3 mV	TL072CD TL072ACD TL072BCD	—	—	—	—	TL072CP TL072ACP TL072BCP	TL072CPWLE — —	—
	10 mV 6 mV 3 mV	TL074CD TL074ACD TL074BCD	—	—	—	TL074CN TL074ACN TL074BCN	—	TL074CPWLE — —	—
–40°C to 85°C	6 mV	TL071ID TL072ID TL074ID	—	—	—	— — TL074IN	TL071IP TL072IP —	—	—
–55°C to 125°C	6 mV 6 mV 9 mV	—	TL071MFK TL072MFK TL074MFK	— — TL074MJ	TL071MJG TL072MJG —	— — TL074MN	— TL072MP —	—	— — TL074MW

† The D package is available taped and reeled. Add the suffix R to the device type (e.g., TL071CDR). The PW package is only available left-ended taped and reeled (e.g., TL072CPWLE).

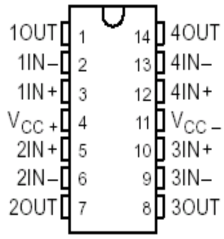
TL071, TL071A, TL071B
D, JG, P, OR PW PACKAGE
(TOP VIEW)



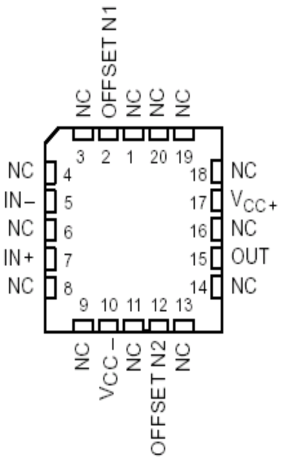
TL072, TL072A, TL072B
D, JG, P, OR PW PACKAGE
(TOP VIEW)



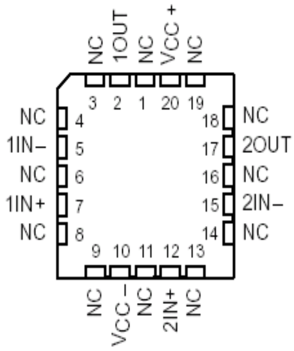
TL074, TL074A, TL074B
D, J, N, OR PW PACKAGE
TL074 . . . W PACKAGE
(TOP VIEW)



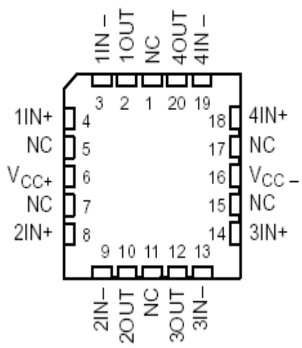
TL071
FK PACKAGE
(TOP VIEW)



TL072
FK PACKAGE
(TOP VIEW)



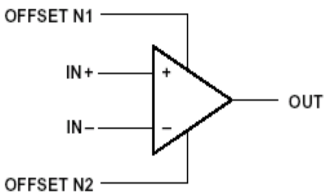
TL074
FK PACKAGE
(TOP VIEW)



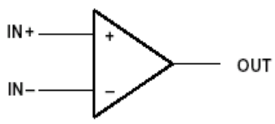
NC – No internal connection

symbols

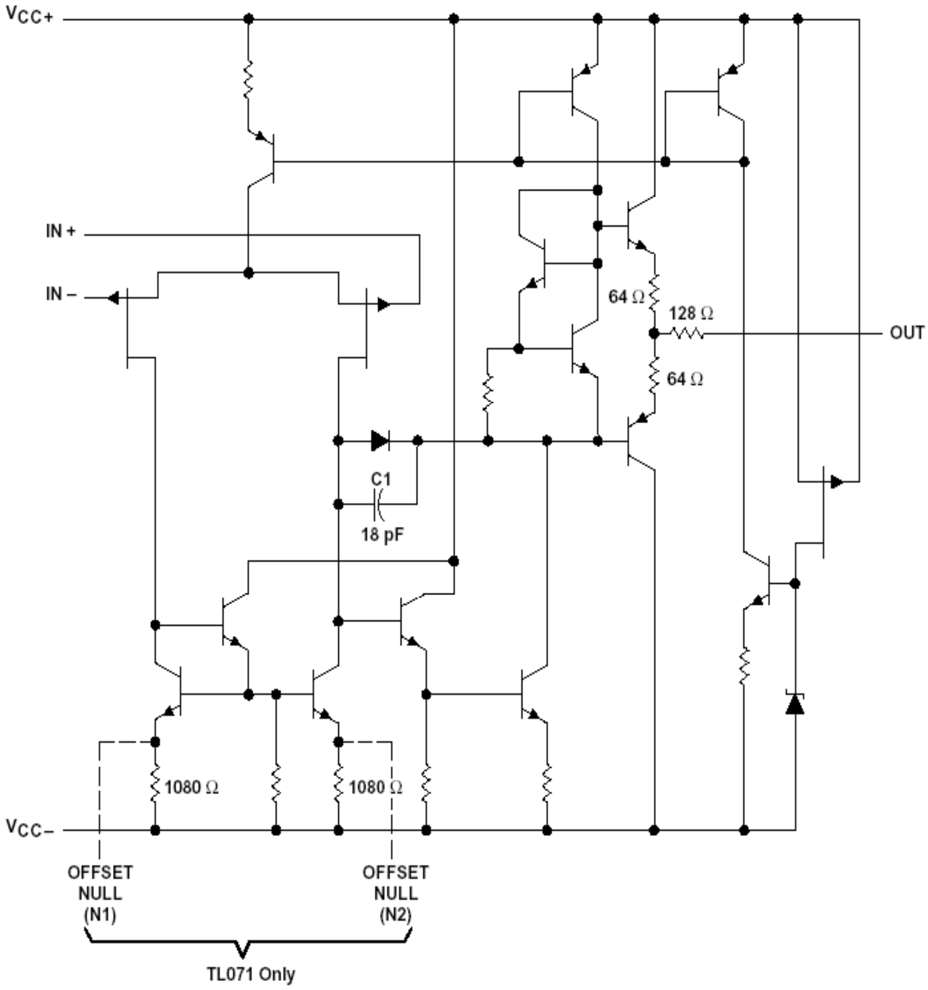
TL071



TL072 (each amplifier)
TL074 (each amplifier)



schematic (each amplifier)



All component values shown are nominal.

COMPONENT COUNT†			
COMPONENT TYPE	TL071	TL072	TL074
Resistors	11	22	44
Transistors	14	28	56
JFET	2	4	6
Diodes	1	2	4
Capacitors	1	2	4
epi-FET	1	2	4

† Includes bias and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) .... 18 V
Supply voltage, V_{CC-} (see Note 1) .... –18 V
Differential input voltage, V_{ID} (see Note 2) .... ±30 V
Input voltage, V_I (see Notes 1 and 3) .... ±15 V
Duration of output short circuit (see Note 4) .... unlimited
Continuous total power dissipation .... See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix .... 0°C to 70°C
I suffix .... –40°C to 85°C
M suffix .... –55°C to 125°C
Storage temperature range .... –65°C to 150°C
Case temperature for 60 seconds: FK package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: J, JG, or W package .... 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, P, or PW package .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN–.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D (8 pin)	680 mW	5.8 mW/°C	33°C	465 mW	378 mW	N/A
D (14 pin)	680 mW	7.6 mW/°C	60°C	604 mW	490 mW	N/A
FK	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	273 mW
J	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	273 mW
JG	680 mW	8.4 mW/°C	69°C	672 mW	546 mW	210 mW
N	680 mW	9.2 mW/°C	76°C	680 mW	597 mW	N/A
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	N/A
PW (8 pin)	525 mW	4.2 mW/°C	70°C	525 mW	N/A	N/A
PW (14 pin)	700 mW	5.6 mW/°C	70°C	700 mW	N/A	N/A
W	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	200 mW

electrical characteristics, $V_{CC\pm} = \pm15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		T_A‡	TL071M TL072M			TL074M			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$,	$R_S = 50\ \Omega$	25°C		3	6		3	9	mV
				Full range			9			15	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$,	$R_S = 50\ \Omega$	Full range		18			18		μV/°C
I_{IO}	Input offset current	$V_O = 0$		25°C		5	100		5	100	pA
				Full range			20			20	nA
I_{IB}	Input bias current‡	$V_O = 0$		25°C		65	200		65	200	pA
							50			50	nA
V_{ICR}	Common-mode input voltage range			25°C	±11	–12 to 15		±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ k\Omega$		25°C	±12	±13.5		±12	±13.5		V
		$R_L \geq 10\ k\Omega$		Full range	±12			±12			
		$R_L \geq 2\ k\Omega$			±10			±10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm10$ V,	$R_L \geq 2\ k\Omega$	25°C	35	200		35	200		V/mV
					15			15			
B_1	Unity-gain bandwidth	$T_A = 25°C$				3			3		MHz
r_i	Input resistance	$T_A = 25°C$				10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, $V_O = 0$,	$R_S = 50\ \Omega$	25°C	80	86		80	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm9$ V to ±15 V, $V_O = 0$,	$R_S = 50\ \Omega$	25°C	80	86		80	86		dB
I_{CC}	Supply current (each amplifier)	$V_O = 0$,	No load	25°C		1.4	2.5		1.4	2.5	mA
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

† Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 4. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.
‡ All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range is $T_A = -55°C$ to 125°C.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		TL07xM MIN	TL07xM TYP	TL07xM MAX	ALL OTHERS MIN	ALL OTHERS TYP	ALL OTHERS MAX	UNIT
SR	Slew rate at unity gain	V_I = 10 V, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1	5	13		8	13		V/μs
t_r	Rise time overshoot factor	V_I = 20 mV, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1		0.1			0.1		μs
					20%			20%		
V_n	Equivalent input noise voltage	R_S = 20 Ω	f = 1 kHz		18			18		nV/√Hz
			f = 10 Hz to 10 kHz		4			4		μV
I_n	Equivalent input noise current	R_S = 20 Ω,	f = 1 kHz		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	V_{Irms} = 6 V, $R_L \geq$ 2 kΩ, f = 1 kHz	A_{VD} = 1, $R_S \leq$ 1 kΩ,		0.003%			0.003%		

PARAMETER MEASUREMENT INFORMATION

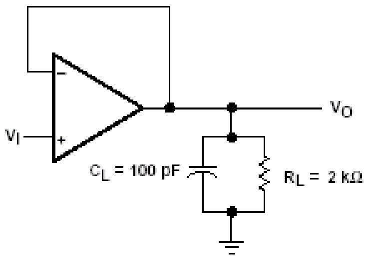


Figure 1. Unity-Gain Amplifier

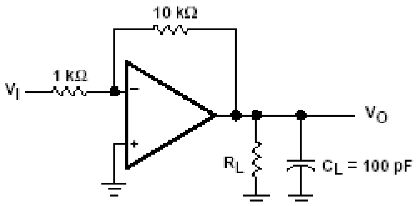


Figure 2. Gain-of-10 Inverting Amplifier

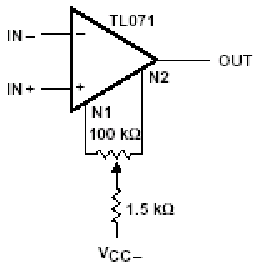


Figure 3. Input Offset Voltage Null Circuit

TYPICAL CHARACTERISTICS†

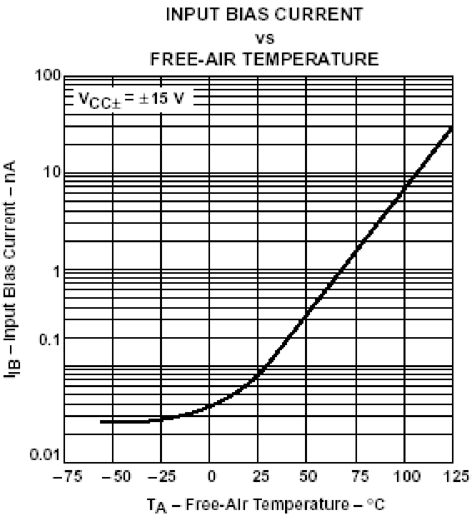


Figure 4

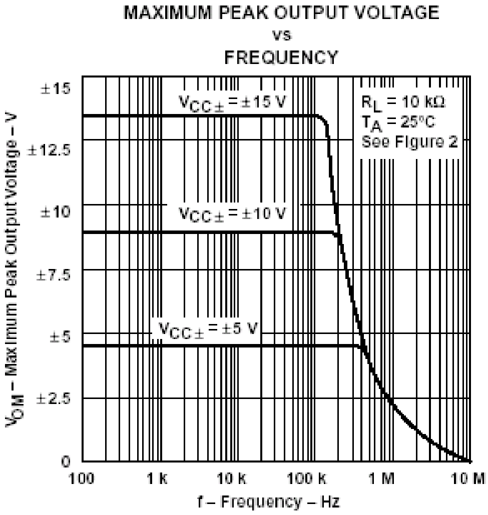


Figure 5

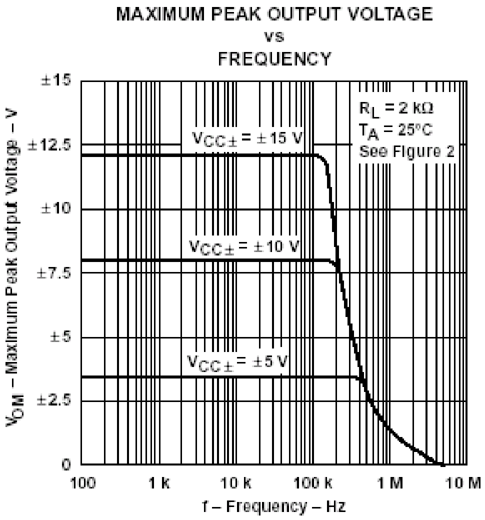


Figure 6

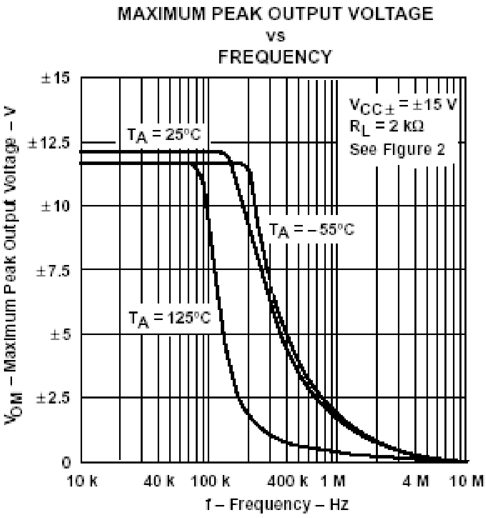


Figure 7

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

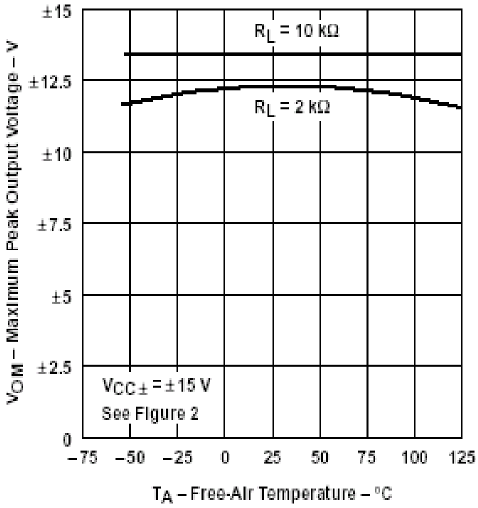


Figure 8

MAXIMUM PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

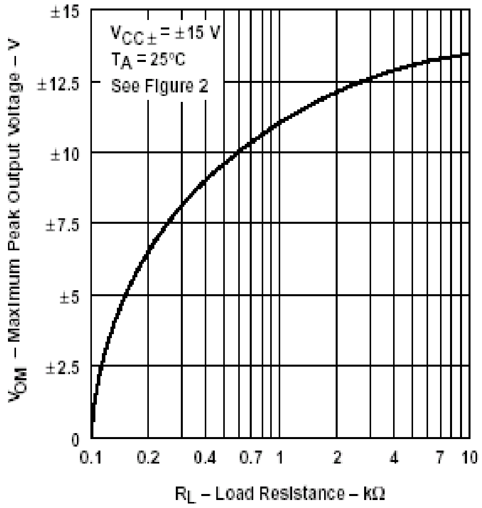


Figure 9

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

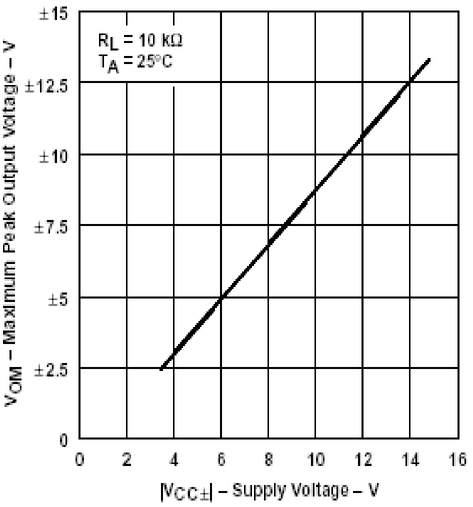


Figure 10

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

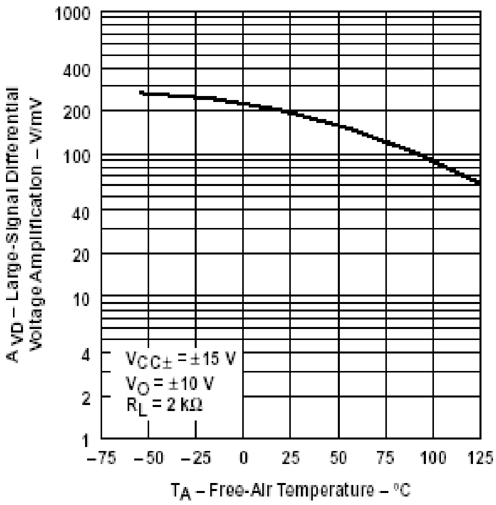


Figure 11

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
AND PHASE SHIFT
vs
FREQUENCY

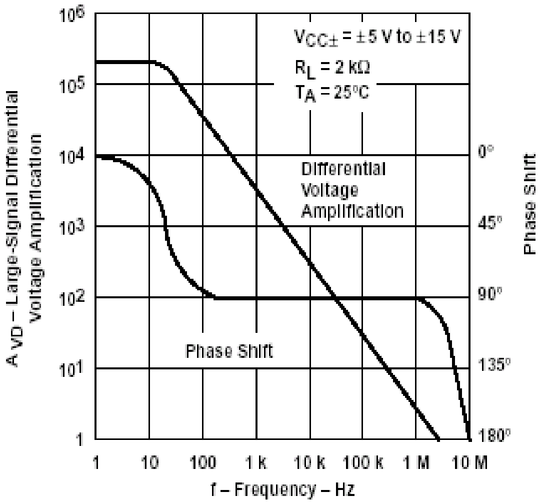


Figure 12

NORMALIZED UNITY-GAIN BANDWIDTH
AND PHASE SHIFT
vs
FREE-AIR TEMPERATURE

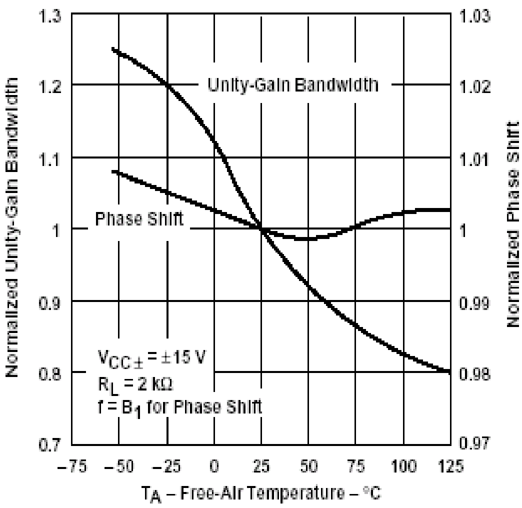


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

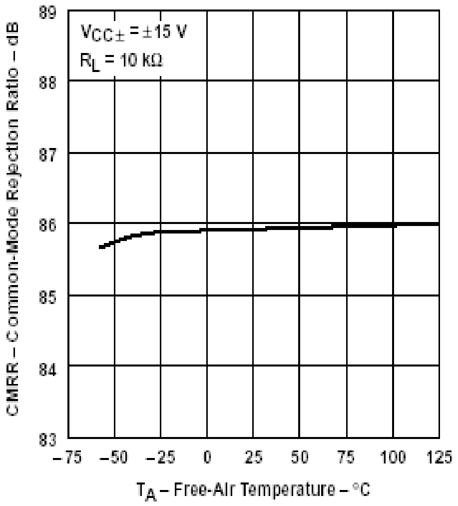


Figure 14

SUPPLY CURRENT PER AMPLIFIER
vs
SUPPLY VOLTAGE

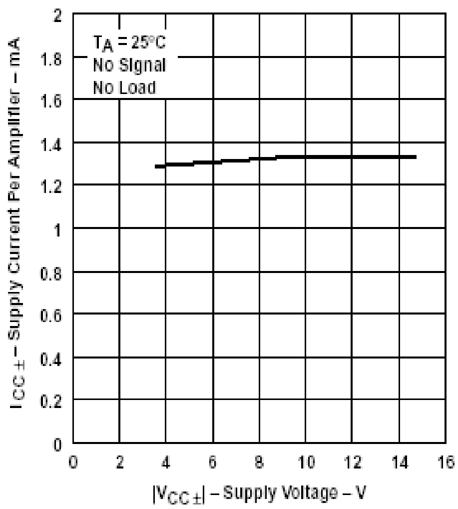


Figure 15

SUPPLY CURRENT PER AMPLIFIER
vs
FREE-AIR TEMPERATURE

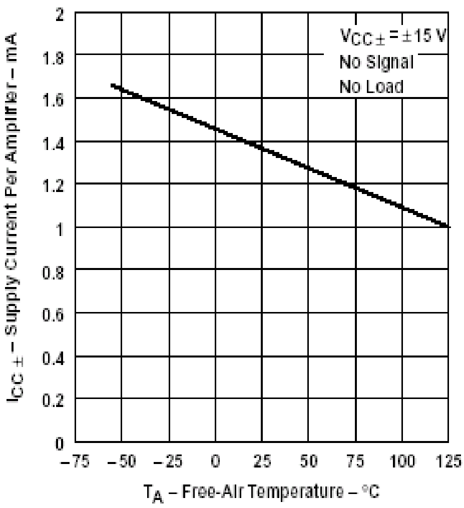


Figure 16

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

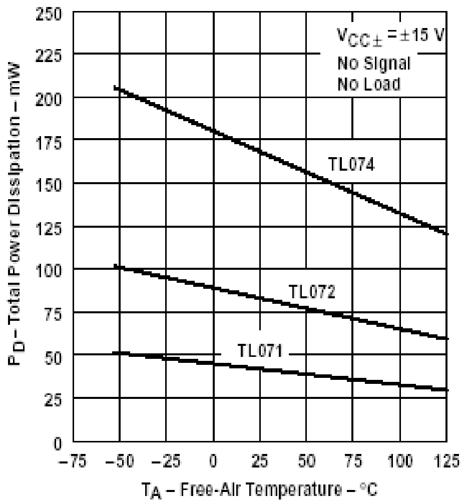


Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

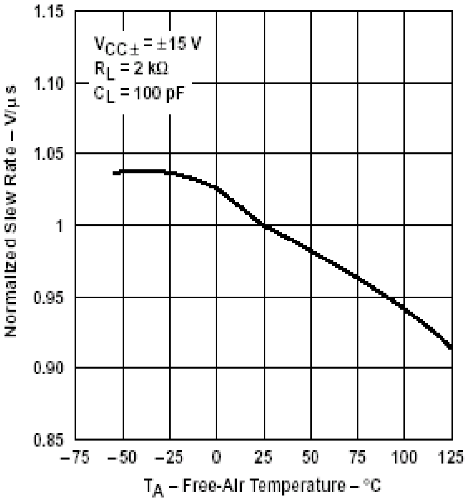


Figure 18

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

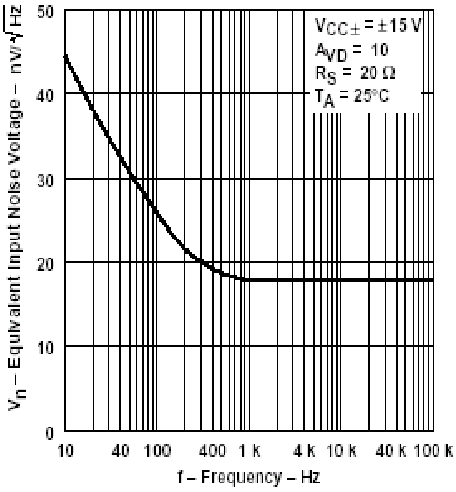


Figure 19

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

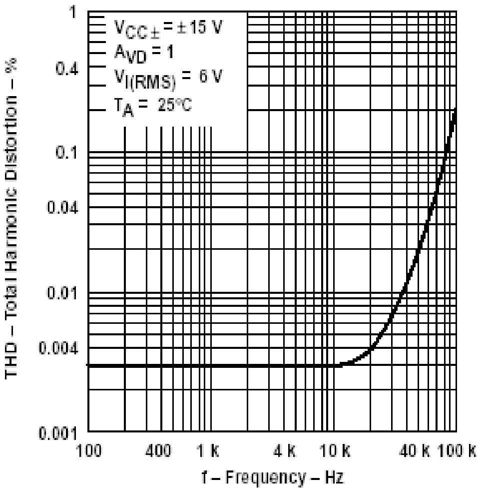


Figure 20

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

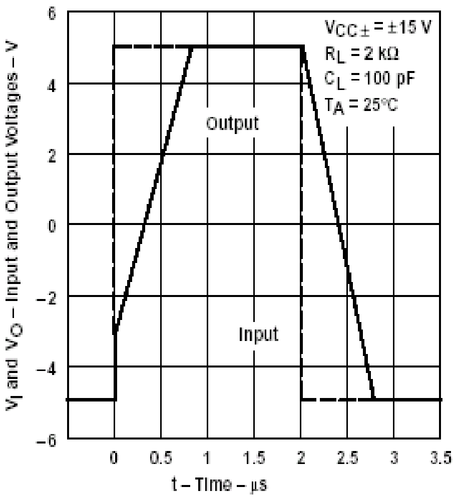


Figure 21

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
ELAPSED TIME

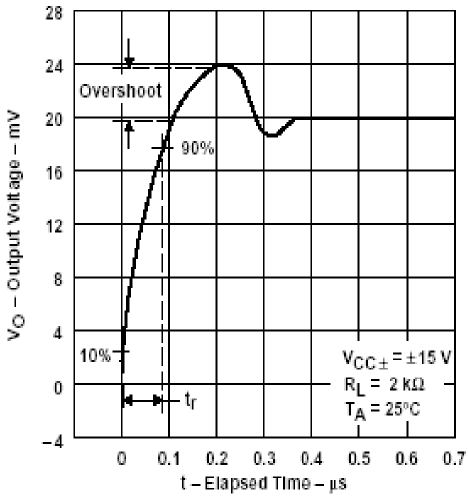


Figure 22

APPLICATION INFORMATION

Table of Application Diagrams

APPLICATION DIAGRAM	PART NUMBER	FIGURE
0.5-Hz square-wave oscillator	TL071	23
High-Q notch filter	TL071	24
Audio-distribution amplifier	TL074	25
100-kHz quadrature oscillator	TL072	26
AC amplifier	TL071	27

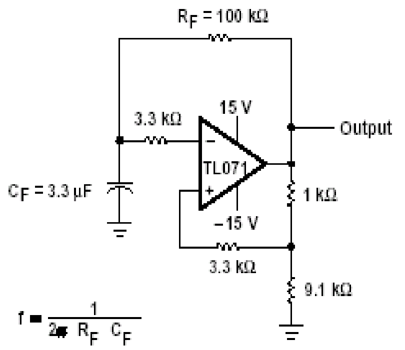


Figure 23. 0.5-Hz Square-Wave Oscillator

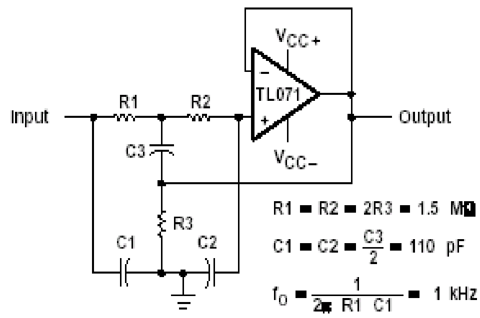


Figure 24. High-Q Notch Filter

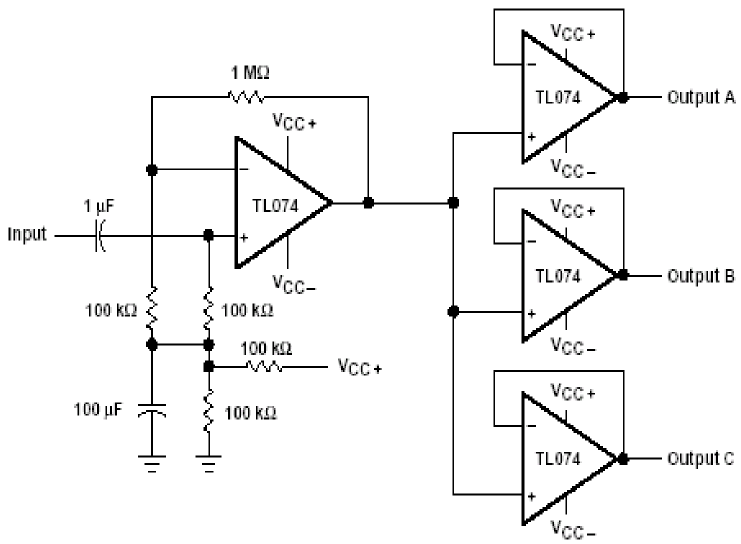
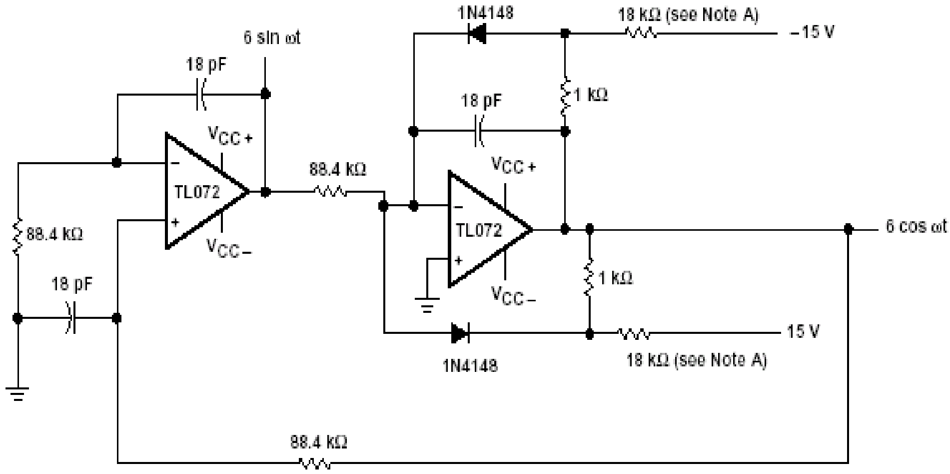


Figure 25. Audio-Distribution Amplifier

APPLICATION INFORMATION



NOTE A: These resistor values may be adjusted for a symmetrical output.

Figure 26. 100-kHz Quadrature Oscillator

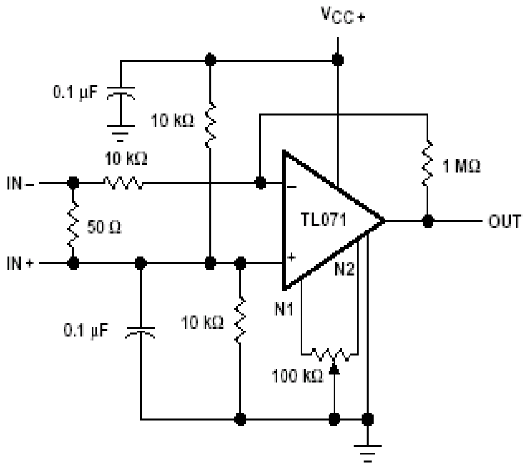


Figure 27. AC Amplifier

electrical characteristics, $V_{CC\pm} = \pm15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A‡	TL071C TL072C TL074C			TL071AC TL072AC TL074AC			TL071BC TL072BC TL074BC			TL071I TL072I TL074I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	25°C		3	10		3	6		2	3		3	6	mV
			Full range			13			7.5			5			8	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	Full range		18			18			18			18		µV/°C
I_{IO}	Input offset current	$V_O = 0$	25°C		5	100		5	100		5	100		5	100	pA
			Full range			10			2			2			2	nA
I_{IB}	Input bias current§	$V_O = 0$	25°C		65	200		65	200		65	200		65	200	pA
			Full range			7			7			7			20	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ k\Omega$	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
		$R_L \geq 10\ k\Omega$	Full range	±12			±12			±12			±12			
		$R_L \geq 2\ k\Omega$		±10			±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm10$ V, $R_L \geq 2\ k\Omega$	25°C	25	200		50	200		50	200		50	200		V/mV
			Full range	15			25			25			25			
B_1	Unity-gain bandwidth		25°C		3			3			3			3		MHz
r_i	Input resistance		25°C		10^{12}			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, $V_O = 0$, $R_S = 50\ \Omega$	25°C	70	100		75	100		75	100		75	100		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm9$ V to ±15 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	70	100		80	100		80	100		80	100		dB
I_{CC}	Supply current (each amplifier)	$V_O = 0$, No load	25°C		1.4	2.5		1.4	2.5		1.4	2.5		1.4	2.5	mA
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$	25°C		120			120			120			120		dB

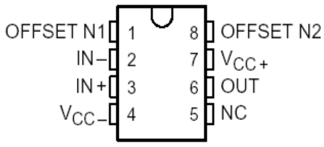
† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified.
‡ Full range is T_A = 0°C to 70°C for TL07_C,TL07_AC, TL07_BC and is T_A = −40°C to 85°C for TL07_I.
§ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 4. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

OP07C, OP07D, OP07Y
PRECISION OPERATIONAL AMPLIFIERS

SLOS099B – OCTOBER 1983 – REVISED AUGUST 1996

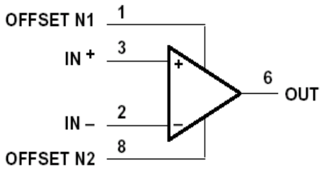
- **Low Noise**
- **No External Components Required**
- **Replaces Chopper Amplifiers at a Lower Cost**
- **Single-Chip Monolithic Fabrication**
- **Wide Input Voltage Range**
  0 to ±14 V Typ
- **Wide Supply Voltage Range**
  ±3 V to ±18 V
- **Essentially Equivalent to Fairchild µA714 Operational Amplifiers**
- **Direct Replacement for PMI OP07C and OP07D**

D OR P PACKAGE
(TOP VIEW)



NC – No internal connection

symbol



description

These devices represent a breakthrough in operational amplifier performance. Low offset and long-term stability are achieved by means of a low-noise, chopperless, bipolar-input-transistor amplifier circuit. For most applications, external components are not required for offset nulling and frequency compensation. The true differential input, with a wide input voltage range and outstanding common-mode rejection, provides maximum flexibility and performance in high-noise environments and in noninverting applications. Low bias currents and extremely high input impedances are maintained over the entire temperature range. The OP07 is unsurpassed for low-noise, high-accuracy amplification of very low-level signals.

These devices are characterized for operation from 0°C to 70°C.

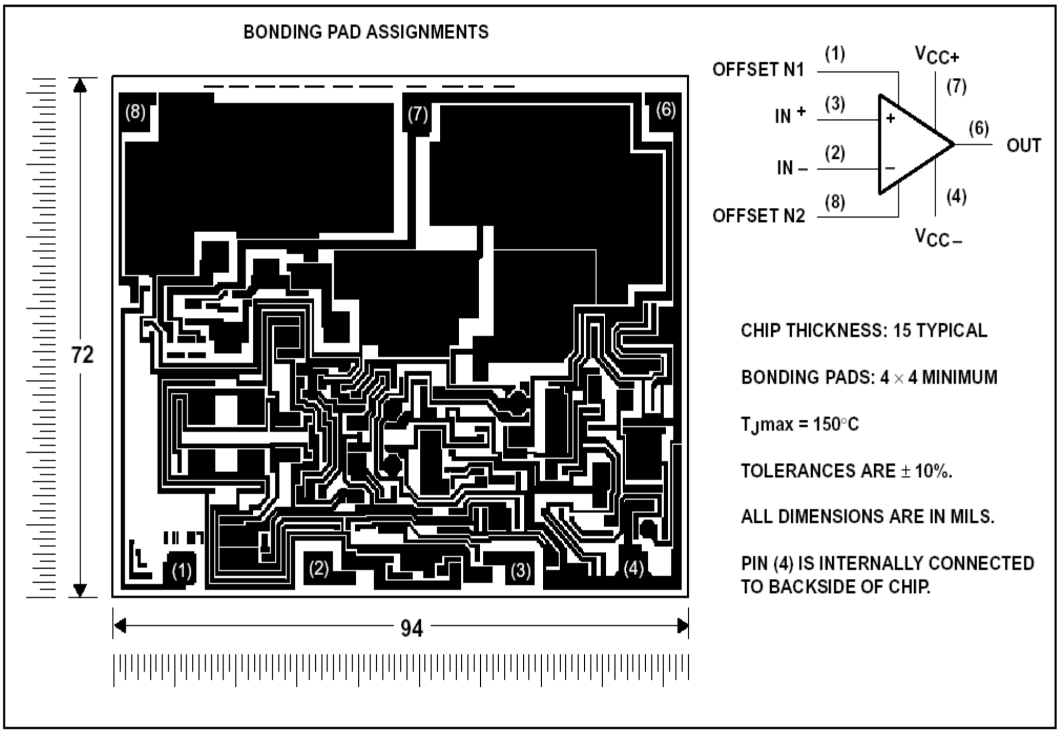
AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES		CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	
0°C to 70°C	150 µV	OP07CD OP07DD	OP07CP OP07DP	OP07Y

The D package is available taped and reeled. Add the suffix R to the device type (e.g., OP07CDR). The chip form is tested at T_A = 25°C.

OP07Y chip information

These chips, properly assembled, display characteristics similar to the OP07. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



OP07C, OP07D, OP07Y
PRECISION OPERATIONAL AMPLIFIERS

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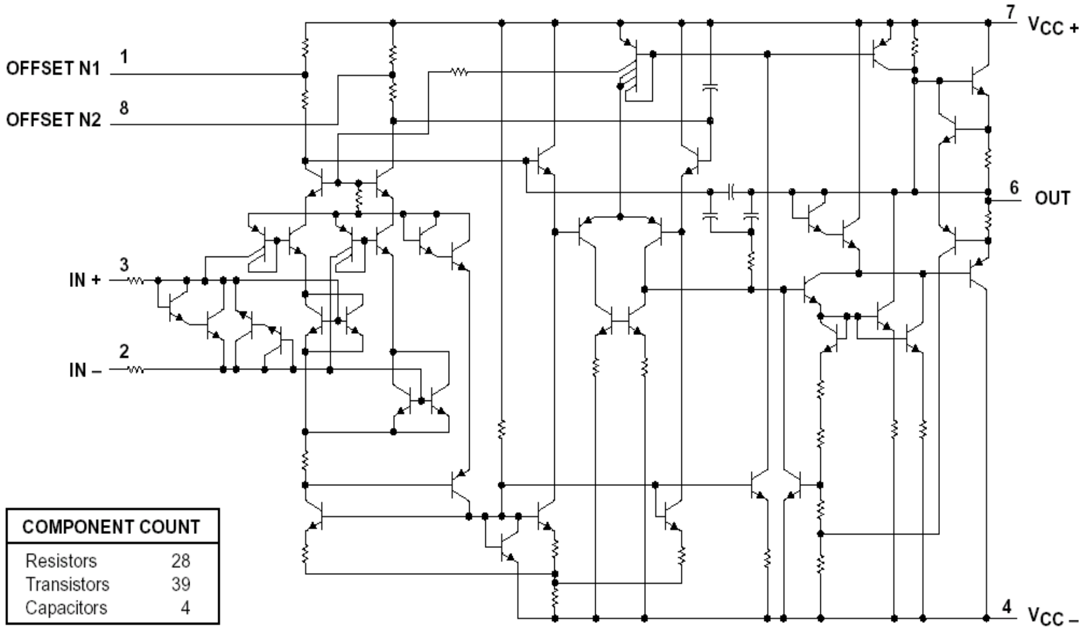
schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . 22 V
Supply voltage, V_{CC-} . . . . –22 V
Differential input voltage (see Note 2) . . . . ±30 V
Input voltage, V_I (either input, see Note 3) . . . . ±22 V
Duration of output short circuit (see Note 4) . . . . unlimited
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5) . . . . 500 mW
Operating free-air temperature range, T_A . . . . 0°C to 70°C
Storage temperature range . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN–.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or either power supply.
5. For operation above 64°C free-air temperature, derate the D package to 464 mW at 70°C at the rate of 5.8 mW/°C.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, $V_{CC\pm}$		±3	±18	V
Common-mode input voltage, V_{IC}	$V_{CC\pm}$ = ±15 V	–13	13	V
Operating free-air temperature, T_A		0	70	°C

electrical characteristics at specified free-air temperature, $V_{CC}\pm = \pm15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A	OP07C			OP07D			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	25°C		60	150		60	150	µV
			0°C to 70°C		85	250		85	250	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	0°C to 70°C		0.5	1.8		0.7	2.5	µV/°C
	Long-term drift of input offset voltage	See Note 6			0.4			0.5		µV/mo
	Offset adjustment range	$R_S = 20$ kΩ, See Figure 1	25°C		±4			±4		mV
I_{IO}	Input offset current		25°C		0.8	6		0.8	6	nA
			0°C to 70°C		1.6	8		1.6	8	
α_{IIO}	Temperature coefficient of input offset current		0°C to 70°C		12	50		12	50	pA/°C
I_{IB}	Input bias current		25°C		±1.8	±7		±2	±12	nA
			0°C to 70°C		±2.2	±9		±3	±14	
α_{IIB}	Temperature coefficient of input bias current		0°C to 70°C		18	50		18	50	pA/°C
V_{ICR}	Common-mode input voltge range		25°C	±13	±14		±13	±14		V
			0°C to 70°C	±13	±13.5		±13	±13.5		
V_{OM}	Peak output voltage	$R_L \geq 10$ kΩ	25°C	±12	±13		±12	±13		V
		$R_L \geq 2$ kΩ	25°C	±11.5	±12.8		±11.5	±12.8		
		$R_L \geq 1$ kΩ	25°C		±12			±12		
		$R_L \geq 2$ kΩ	0°C to 70°C	±11	±12.6		±11	±12.6		
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm} = \pm3$ V, $V_O = \pm0.5$ V, $R_L \geq 500$ kΩ	25°C	100	400			400		V/mV
		$V_O = \pm10$ V, $R_L = 2$ kΩ	25°C	120	400		120	400		
			0°C to 70°C	100	400		100	400		
B_1	Unity-gain bandwidth		25°C	0.4	0.6		0.4	0.6		MHz
r_i	Input resistance		25°C	8	33		7	31		MΩ
CMRR	Common-mode rejection ratio	$V_{IC} = \pm13$ V, $R_S = 50\ \Omega$	25°C	100	120		94	110		dB
			0°C to 70°C	97	120		94	106		
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC\pm} = \pm3$ V to ±18 V, $R_S = 50\ \Omega$	25°C		7	32		7	32	µV/V
			0°C to 70°C		10	51		10	51	
P_D	Power dissipation	$V_O = 0$, No load	25°C		80	150		80	150	mW
		$V_{CC\pm} = \pm3$ V, $V_O = 0$, No load	25°C		4	8		4	8	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise noted.

NOTE 6: Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a warranty. It is an engineering estimate of the averaged trend line of drift versus time over extended periods after the first thirty days of operation.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS†	OP07C MIN	OP07C TYP	OP07C MAX	OP07D MIN	OP07D TYP	OP07D MAX	UNIT
V_n	Equivalent input noise voltage	f = 10 Hz		10.5			10.5		nV/√Hz
		f = 100 Hz		10.2			10.3		
		f = 1 kHz		9.8			9.8		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		0.38			0.38		µV
I_n	Equivalent input noise current	f = 10 Hz		0.35			0.35		pA/√Hz
		f = 100 Hz		0.15			0.15		
		f = 1 kHz		0.13			0.13		
$I_{N(PP)}$	Peak-to-peak equivalent input noise current	f = 0.1 Hz to 10 Hz		15			15		pA
SR	Slew rate	$R_L \geq 2$ kΩ		0.3			0.3		V/µs

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise noted.

electrical characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	OP07Y MIN	OP07Y TYP	OP07Y MAX	UNIT
V_{IO}	Input offset voltage	$R_S = 50$ Ω		60	150	µV
	Long-term drift of input offset voltage	See Note 6		0.5		µV/mo
	Offset adjustment range	$R_S = 20$ kΩ, See Figure 1		±4		mV
I_{IO}	Input offset current			0.8	6	nA
I_{IB}	Input bias current			±2	±12	nA
V_{ICR}	Common-mode input voltage range		±13	±14		V
V_{OM}	Peak output voltage	$R_L \leq 10$ kΩ	±12	±13		V
		$R_L \leq 2$ kΩ	±11.5	±12.8		
		$R_L \leq 1$ kΩ		±12		
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm} = \pm 3$ V, $V_O = \pm 0.5$ V, $R_L \leq 500$ kΩ		400		
		$V_O = \pm 10$ V, $R_L = 2$ kΩ	120	400		
B_1	Unity-gain bandwidth		0.4	0.6		MHz
r_i	Input resistance		7	31		MΩ
CMRR	Common-mode input resistance	$V_{IC} = \pm 13$ V, $R_S = 50$ Ω	94	110		dB
k_{SVS}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 3$ V to ± 18 V, $R_S = 50$ Ω		7	32	µV/V
P_D	Power dissipation	$V_O = 0$, No load		80	150	MΩ
		$V_{CC\pm} = \pm 3$ V, $V_O = 0$, No load		4	8	

NOTE 6: Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a warranty. It is an engineering estimate of the averaged trend line of drift versus time over extended periods after the first thirty days of operation.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS†	OP07Y MIN	OP07Y TYP	OP07Y MAX	UNIT
V_n	Equivalent input noise voltage	f = 10 Hz		10.5		nV/√Hz
		f = 1 kHz		10.3		
		f = 0.1 Hz to 10 Hz		9.8		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		0.38		μV
I_n	Equivalent input noise current	f = 10 Hz		0.35		pA/√Hz
		f = 100 Hz		0.15		
		f = 1 kHz		0.13		
$I_{N(PP)}$	Peak-to-peak equivalent input noise current	f = 0.1 Hz to 10 Hz		15		pA
SR	Slew rate	R_L = 2 kΩ		0.3		V/μs

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise noted.

APPLICATION INFORMATION

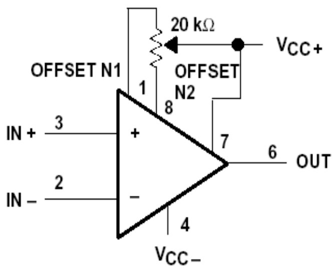


Figure 1. Input Offset Voltage Null Circuit

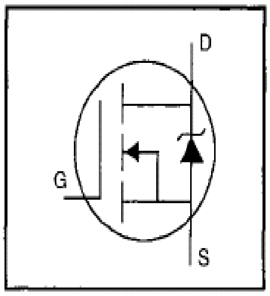
International IOR Rectifier

PD-9.544A

IRFP054

HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Isolated Central Mounting Hole
- 175°C Operating Temperature
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements



V_{DSS} = 60V

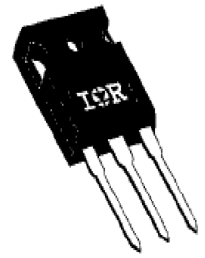
$R_{DS(on)}$ = 0.014Ω

I_D = 70*A

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-247 package is preferred for commercial–industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole. It also provides greater creepage distance between pins to meet the requirements of most safety specifications.



TO-247AC

DATA SHEETS

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10 V	70*	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10 V	64	
I_{DM}	Pulsed Drain Current ①	360	
P_D @ T_C = 25°C	Power Dissipation	230	W
	Linear Derating Factor	1.5	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	640	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)	

Thermal Resistance

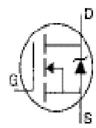
	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	0.65	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	40	

IRFP054

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	—	—	V	V_{GS}=0V, I_D= 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.056	—	V/°C	Reference to 25°C, I_D= 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.014	Ω	V_{GS}=10V, I_D=54A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS}=V_{GS}, I_D= 250μA
g_{fs}	Forward Transconductance	25	—	—	S	V_{DS}=25V, I_D=54A ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V_{DS}=60V, V_{GS}=0V
		—	—	250		V_{DS}=48V, V_{GS}=0V, T_J=150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS}=20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS}=-20V
Q_g	Total Gate Charge	—	—	160	nC	I_D=64A
Q_{gs}	Gate-to-Source Charge	—	—	48		V_{DS}=48V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	54		V_{GS}=10V See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	20	—	ns	V_{DD}=30V
t_r	Rise Time	—	160	—		I_D=64A
$t_{d(off)}$	Turn-Off Delay Time	—	83	—		R_G=6.2Ω
t_f	Fall Time	—	150	—		R_D=0.45Ω See Figure 10 ④
L_D	Internal Drain Inductance	—	5.0	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	—	13	—		
C_{iss}	Input Capacitance	—	4500	—	pF	V_{GS}=0V
C_{oss}	Output Capacitance	—	2000	—		V_{DS}= 25V
C_{rss}	Reverse Transfer Capacitance	—	300	—		f=1.0MHz See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	70*	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	360		
V_{SD}	Diode Forward Voltage	—	—	2.5	V	T_J=25°C, I_S=90A, V_{GS}=0V ④
t_{rr}	Reverse Recovery Time	—	270	540	ns	T_J=25°C, I_F=64A
Q_{rr}	Reverse Recovery Charge	—	1.1	2.2	μC	di/dt=100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is neglegible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

② V_{DD}=25V, starting T_J=25°C, L=92μH R_G=25Ω, I_{AS}=90A (See Figure 12)

③ I_{SD}≤90A, di/dt≤200A/μs, V_{DD}≤$V_{(BR)DSS}$, T_J≤175°C

④ Pulse width ≤ 300 μs; duty cycle ≤2%.

* Current limited by the package, (Die Current =90A)

IOR **IRFP054**

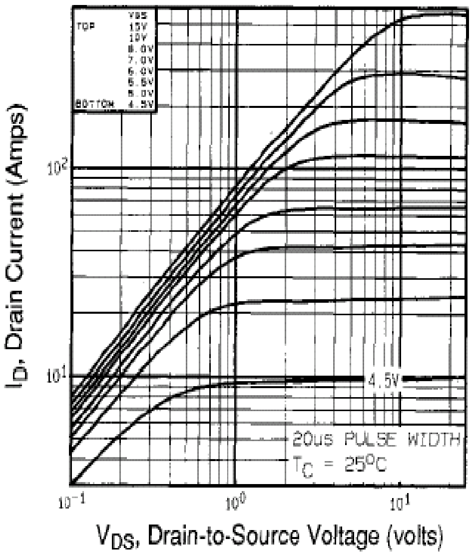


Fig 1. Typical Output Characteristics, T_C=25°C

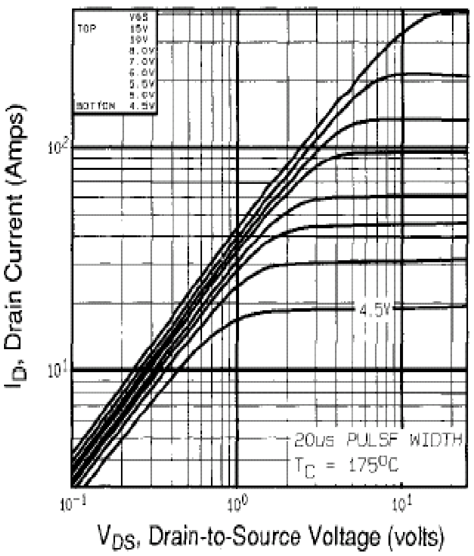


Fig 2. Typical Output Characteristics, T_C=175°C

DATA SHEETS

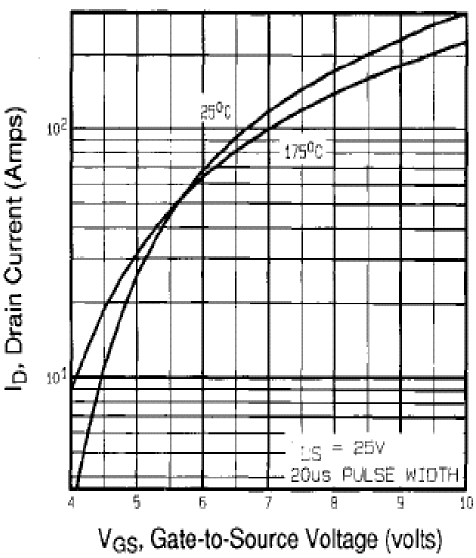


Fig 3. Typical Transfer Characteristics

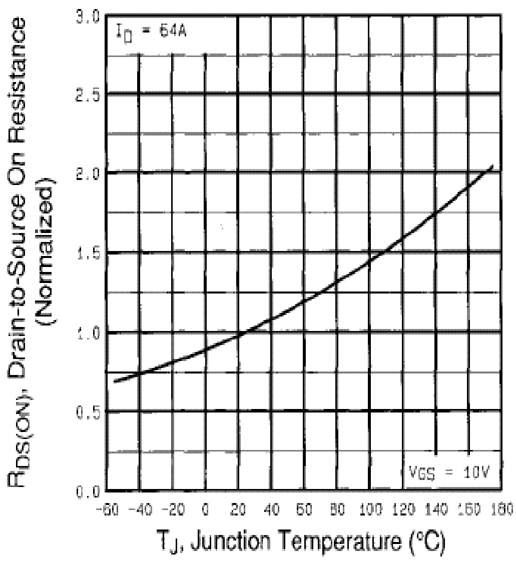


Fig 4. Normalized On-Resistance Vs. Temperature

IRFP054

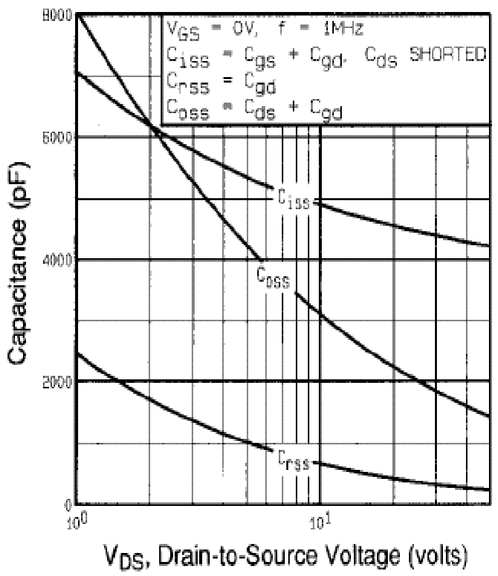


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

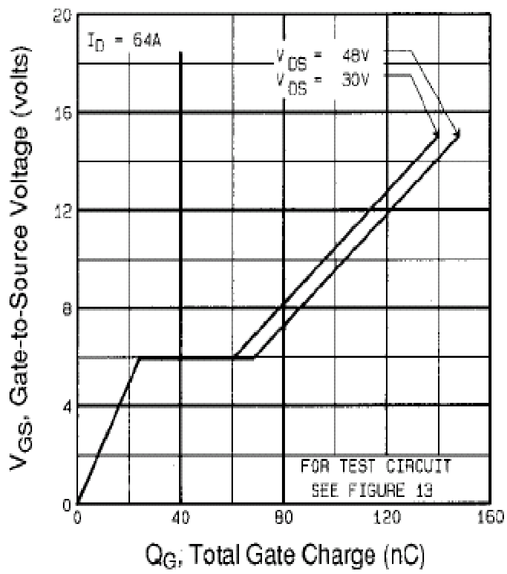


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

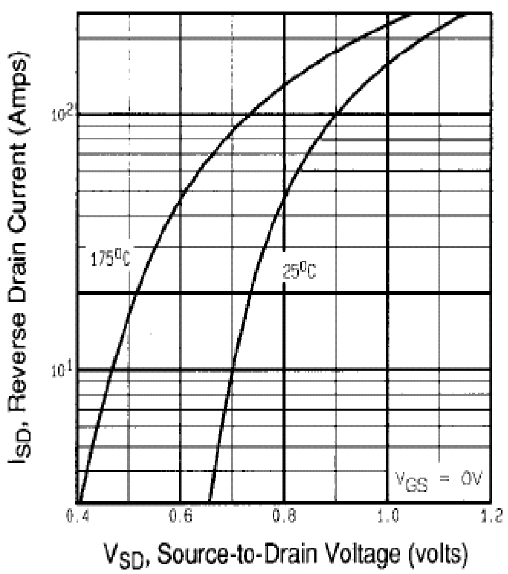


Fig 7. Typical Source-Drain Diode Forward Voltage

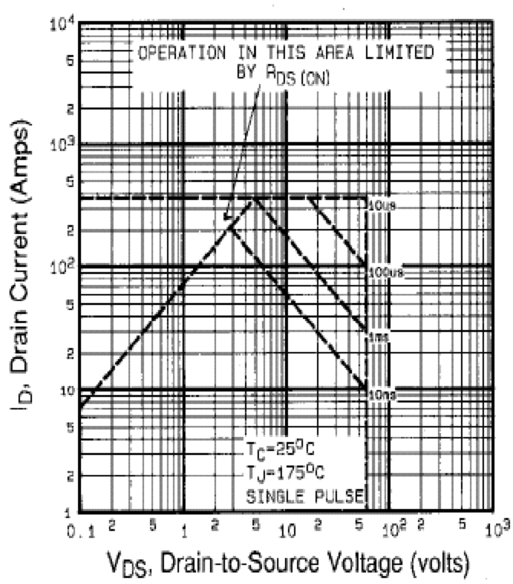


Fig 8. Maximum Safe Operating Area

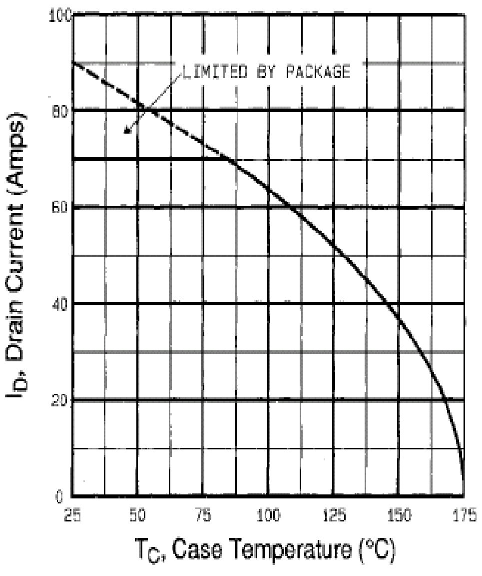


Fig 9. Maximum Drain Current Vs. Case Temperature

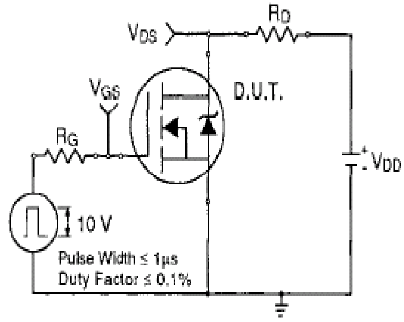


Fig 10a. Switching Time Test Circuit

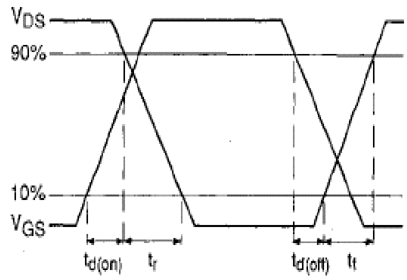


Fig 10b. Switching Time Waveforms

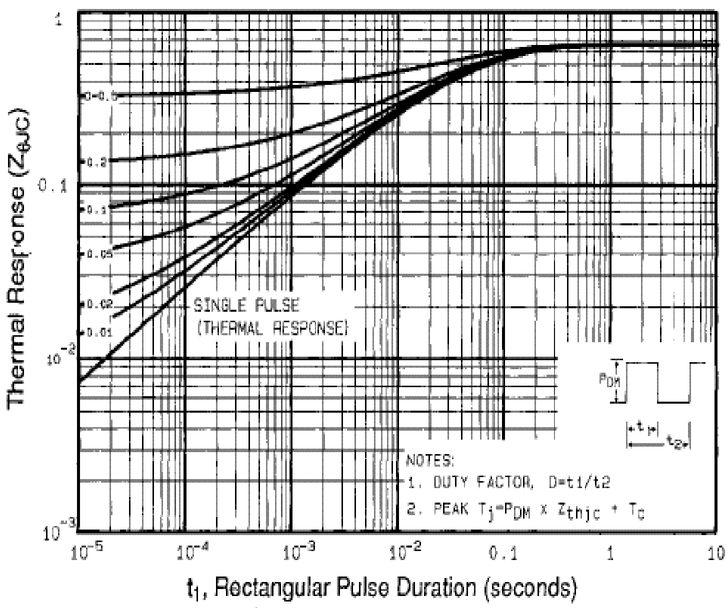


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

IRFP054

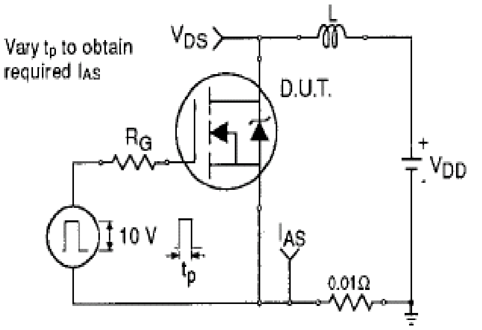


Fig 12a. Unclamped Inductive Test Circuit

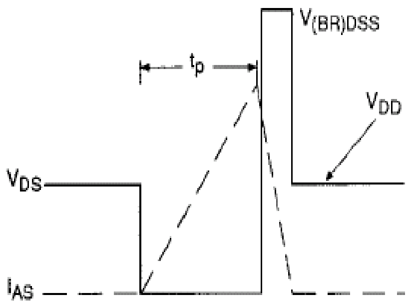


Fig 12b. Unclamped Inductive Waveforms

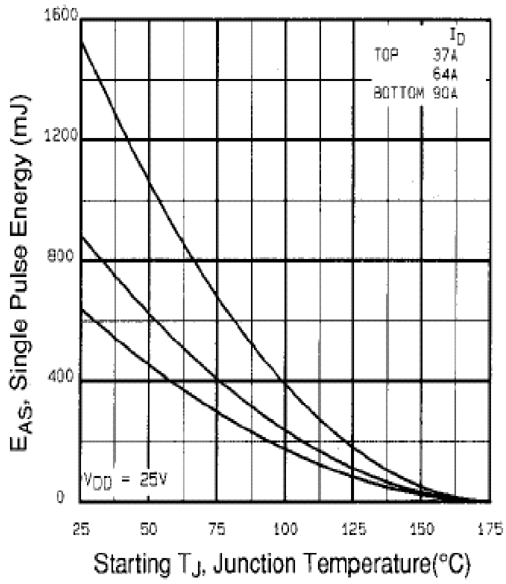


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

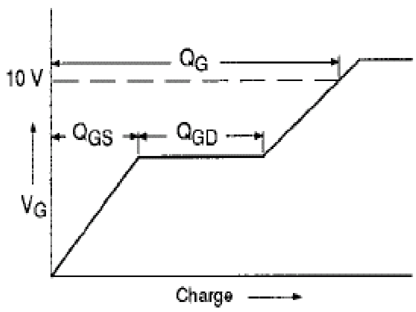


Fig 13a. Basic Gate Charge Waveform

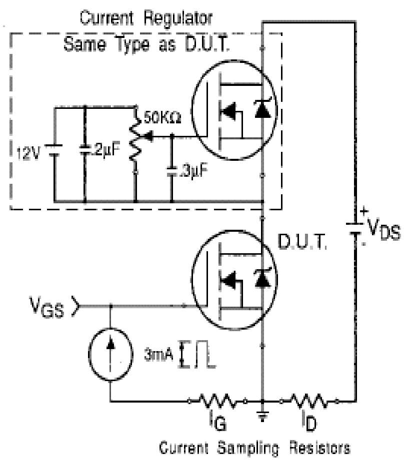


Fig 13b. Gate Charge Test Circuit

Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit – See page 1505

Appendix B: Package Outline Mechanical Drawing – See page 1511

Appendix C: Part Marking Information – See page 1517

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