CHAPTER III

MICROELECTRONIC DESIGN

In the previous chapter, we have presented a network of oscillators that can successfully segment images. Although the model can be easily simulated on a digital computer, its oscillatory nature makes it no practical for real applications. The number of differential equations to be solved is proportional to the number of pixels in the image and this number increases very fast when resolution increases. To give an example, suppose a 32x32 image, thus the total number of basic oscillators is 1024. Considering that two integrators per cell plus synapses should be solved through some periods to obtain the required solution (let's say 3 periods with 1000 time steps per period) 1024x2x3x1000≈6Mops per image are needed. If 25 images per second should be solved, the computational load for a simple 32x32 image is 150Mops/sec. Thus, computational load for a standard VGA image is on the order of tens of giga-ops per second. In addition to this, synapses and the global inhibitor have not been considered, so more computational power shall be needed for a final real-time system. Of course, this is a rough approximation; some algorithms can be developed to reduce this number (simplifying the algorithm or improving the integration method), however, the number of operations is still too large to be implemented on real-time applications especially if low-power consumption and small area are needed as in portable systems.

On the other hand, if we could generate the required oscillations on a physical system instead of simulating them, no differential equations should be solved and consumption will be reduced to that needed to maintain these oscillations. Then, the main issue will be whether oscillations are fast enough and the speed of the system should not be measured in operations per second but in oscillations per second. However, some problems that must be solved arise with that approach. First, as the system is parallel, it will need as many physical oscillators as pixels are in the input image, thus a large-scale integration technology shall be used. Second, the system should output the processed information as fast as it produces this information. Communication is a key issue in parallel approaches. Nevertheless, segmentation is only a step in the visual information process. Therefore, if the next processing step is embedded in the system, it should not output so much information. A system that counts the number of objects in an image can be a good example because information to output is just a number and not the exact information of each object.

Some implementations of neural oscillators have been proposed in the literature. Most of them have been designed to model natural neurons as close as possible [Keener,83] [Linares et al.,89] [Toumazou et al.,98], however large silicon areas are needed to implemented them. Others are small but they are not appropriate for computation purposes of this work because they cannot be easily coupled to other cells [Patel and DeWeerth,97] [Mead,89]. The objective of this thesis is to design an oscillator with low power consumption and small enough to build massive parallel networks for practical applications.

One of the most important problems when implementing a neural network on hardware architectures is the large number of connections that usually exist between cells. Thus, a fundamental characteristic for a microelectronic implementation of a neural net is that this number must be reduced as much as possible, especially distant connections. This is a characteristic of the oscillatory network presented in the previous chapter. Except the global inhibitor, which is connected to each cell, all other cells are only locally coupled, thus the number of connections is proportional to the number of cells and a parallel microelectronic implementation is feasible.

In this chapter, we present a microelectronic implementation of the segmentation network analyzed in the previous chapter. We have used a standard CMOS analog technology. The main advantage of this choice is that the final chip does not require expensive manufacturing processes but a common one as other standard processors.

In addition to this, CMOS phototransducers can be easily embedded on a segmentation network implemented using the same technology. Advances on this technology promises that in a near future, CMOS cameras will be as effective as present CCD devices, which require a more expensive manufacturing process. In addition, CMOS power consumption is lower than required by bipolar technology, therefore, power consumption of the system is kept low.

The minimum feature size of the process (0.8μm) used in this design was a standard size when the circuit was designed. However, present smaller technologies allow us to reduce cell size.

The circuit described in this work is a test chip to validate the feasibility of the implementation and allow maximum flexibility for testing operation under a large number of conditions and enabling a convenient input-output. For this reason we have implemented a serial input/output interface in the chip and a memory cell for each oscillator. Nevertheless, for real applications, information should be entered via a parallel interface as an embedded matrix of photo-detectors, which will also replace the memory cell. In addition, following processing steps shall be embedded in the system.

In this chapter, first, we adapt the model presented in chapter II to a microelectronic scheme. Then, we describe the global architecture of the system. After this, we show in detail each different element that builds the whole circuit, from the signal-processing core to the output circuitry. We also study the dependency of frequency and duty cycle of oscillators as a function of different bias values. Finally, we show some microphotographs of the chip that has been implemented and a discussion concludes the chapter.

III.1 MICROELECTRONIC MODEL

In chapter II we have analyzed an oscillator model based on two integrators with different time constants, a fast one for the hysteresis comparator and a slow one for the strictly speaking integrator. Implementating integrators is easy in CMOS technology because only a current source as a transistor and a capacitor are needed. Thus, taking the most of this property, a block diagram of current sources and capacitors equivalent to the output delay oscillator of the previous chapter is shown in Figure III.1.
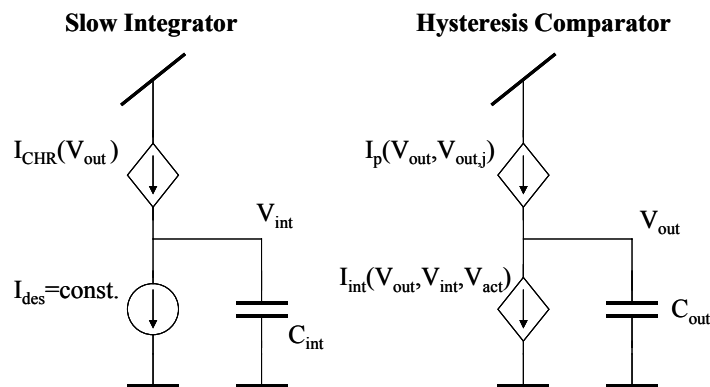
Figure III.1: Oscillator modeled as dependent current sources.

I_{CHR} current is switched on and off depending on the oscillator state and it is responsible of charging the integrator capacitor. On the other hand, I_{des} is a constant discharge current of the integrator. As this current is usually low during normal operation of the network to improve its functionallity, there is no need to switch it off during charge cycle. This current being continuous, simplifies the design, reduces area and since integrator charge is performed by I_{chr} current, which is usually greater than I_{des}, power consumption increase due to this current is not significant.

I_p is the threshold current of the comparator. This threshold depends on oscillator state (hysteresis) and it also depends on the state of other coupled oscillators (excitatory synapses). This current is compared to I_{int} in the output node that is controlled by integrator node voltage (V_{int}). This current also depends on the state of all network cells (inhibitory synapse).

$$I_{CHR}(V_{out}) = \begin{cases} 0 & V_{out} < V_{ref} \\ I_{chr} & V_{ref} \le V_{out} \end{cases}$$

$$I_{int}(V_{out}, V_{int}, V_{act}) = \begin{cases} \left(k(V_{int} - V_{th})^2 + I_I(V_{act})\right)\dfrac{V_{out}}{V_C} & V_{out} < V_C \\ k(V_{int} - V_{th})^2 + I_I(V_{act}) & V_C \le V_{out} \end{cases}$$

$$I_p(V_{out}, V_{out,j}) = \begin{cases} I_{pos} + I_E(V_{out,j}) & V_{out} < V_{ref} \\ I_{pos} + I_{wid} + I_E(V_{out,j}) & V_{ref} \le V_{out} < V_{DD} - V_C \\ \left(I_{pos} + I_{wid} + I_E(V_{out,j})\right)\dfrac{V_{DD} - V_{out}}{V_C} & V_{DD} - V_C \le V_{out} \end{cases}$$

Eq.III.1

Notice that functions I_{int} and I_p are rough piece-wise linear approximations of MOS transistor drain currents in different regions of operation (see Figures II.17 and II.18). In addition to this, current I_{int} is the drain current of a NMOS transistor whose gate to source voltage is V_{int}.
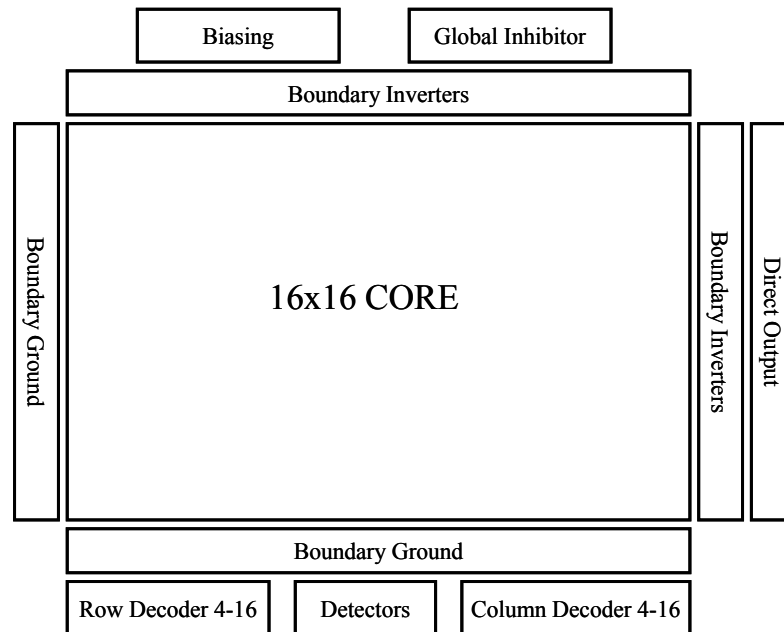
Functions I_E and I_I are synapse current sources. I_E is the sum of all excitatory synapse currents that equals to 0 when each neighbor cell is silent and I_{exc} when all neighbor cells are active. I_I represents the inhibitory synapse that equals to 0 for each oscillator when all cells in the network are silent and I_{inh} when any cell is active. These dependencies are represented by $V_{out,j}$ for neighbor cells and V_{act} for any active cell in the net.

Notice that electronic parameters are related to dimensionless parameters in chapter II and functions are similar except that reference values may change to be adapted to electronic values as shown:

$$
\begin{array}{llll}
V_{out} \equiv x ; & I_{des}/C_{int} \equiv q ; & I_{pos} \equiv \gamma ; & I_{inh} \equiv i ; \quad V_C \equiv C ; \\
V_{int} - V_{th} \equiv y ; & I_{chr}/C_{int} \equiv p+q ; & I_{wid} \equiv \theta ; & V_{DD} \equiv 1 \quad V_{ref} \equiv R ; \\
I_{int} \equiv z ; & I_p \equiv w ; & I_{exc} \equiv s ; & C_{out} \equiv \varepsilon
\end{array}
$$

Eq.III.2

III.2 SYSTEM ARCHITECTURE

Figure III.2 shows the block diagram of the chip. It consists of a 16x16 array of coupled oscillators that constitutes the core of the device. Each oscillator is mapped to an input image and this information establishes excitatory synapses implemented by current sources and digital gates. In addition, a global inhibitor is connected to each core oscillator. These analog elements are biased by an embedded biasing circuit.

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┌─────────────────┐   ┌─────────────────┐
│     Biasing     │   │ Global Inhibitor │
└─────────────────┘   └─────────────────┘
┌───────────────────────────────────────────┐
│            Boundary Inverters               │
└───────────────────────────────────────────┘
┌───┐ ┌─────────────────────────────┐ ┌───┐ ┌───┐
│   │ │                             │ │   │ │   │
│ B │ │                             │ │ B │ │ D │
│ o │ │                             │ │ o │ │ i │
│ u │ │        16x16 CORE           │ │ u │ │ r │
│ n │ │                             │ │ n │ │ e │
│ d │ │                             │ │ d │ │ c │
│ a │ │                             │ │ a │ │ t │
│ r │ │                             │ │ r │ │   │
│ y │ │                             │ │ y │ │ O │
│   │ │                             │ │   │ │ u │
│ G │ │                             │ │ I │ │ t │
│ r │ │                             │ │ n │ │ p │
│ o │ │                             │ │ v │ │ u │
│ u │ │                             │ │ . │ │ t │
│ n │ │                             │ │   │ │   │
│ d │ │                             │ │   │ │   │
└───┘ └─────────────────────────────┘ └───┘ └───┘
      ┌─────────────────────────────────┐
      │         Boundary Ground          │
      └─────────────────────────────────┘
┌─────────────────┐ ┌──────────┐ ┌──────────────────┐
│ Row Decoder 4-16 │ │ Detectors │ │ Column Decoder 4-16 │
└─────────────────┘ └──────────┘ └──────────────────┘
```

Figure III.2: System architecture. The 16x16 oscillator core is surrounded by the global inhibitor, digital control, analog biasing, direct outputs of some oscillators and boundary circuits to cancel boundary synapses.

To input the information to be processed to the chip, a 256-bit shift register is used. Its D flip-flops are distributed throughout the core so there is one single-bit memory element for each cell. Moreover, some digital control has been added to output processed information. A 4-bit row decoder selects the row to output through a 16-bit bus. This information is buffered by the detection circuit that can also drive it to a 1-bit serial output controlled by the 4-bit column detector. The reason of this output is to allow the connection of the circuit to a serial input device as a VGA monitor.

It has also been added some buffers to output directly the state of some oscillators for testing purposes.

III.3 THE CORE

The network core consists of a rectangular array of oscillators with their synapses and a 1-bit memory element for each cell plus a global inhibitor cell common to the entire network. For this design we have chosen a simple level of connectivity, thus each cell is excitatory coupled to its nearest 4 neighbors, i.e. top, bottom, right and left. (Figure III.3). The input image is mapped to oscillator core; thus, each oscillator is mapped to one input pixel.
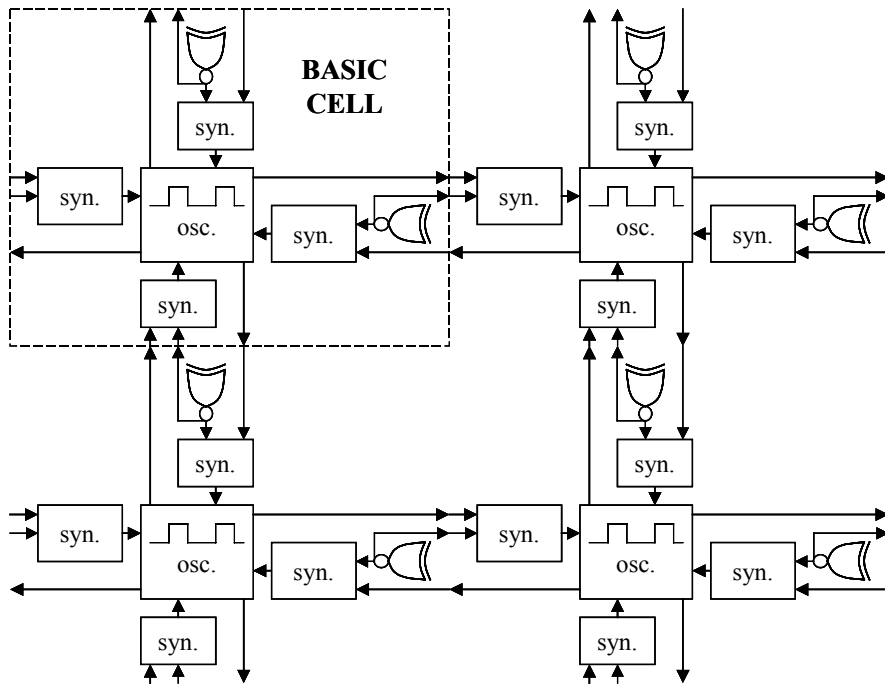
Figure III.3: Diagram of four core elements. Each cell has 1 oscillator, 4 synapse circuits and two XNOR gates that are shared between adjacent cells. Memory elements and their connections to digital gates are not shown for clarity.

The basic element of the network is the oscillator and its evolution will be the responsible of segmenting the image. Each oscillator, also, is connected to four synapses that excite its oscillation when neighbor cells that share the same input value are active. This value is stored in a 1-bit memory element for each cell. Synapses consist of a current source that can shift thresholds of the comparator and a XNOR gate that compares values of its own cell and neighbor cells to check if they share the same value. If values are equal, the XNOR gate, which outputs 1, activates the synapse current source. This current source, then, will be able to drive a current to the oscillator when the neighbor cell is active. However, if cell values are different, the XNOR gate will switch off the synapse and it will not be able to drive any current even when the neighbor cell is active. Note that despite being 4 synapses per cell, only two XNOR gates are needed because adjacent cells share them.

To keep modularity and simplify the design, basic cells must be identical through the entire network in spite of different connectivity in edge and corner cells that are connected to 3 or 2 neighbors respectively instead of 4. To solve that problem, boundaries 'simulate' cells in order that synapses in the boundary are null. This is achieved by inverters that complement the digital content of memory elements in the boundary cell or by direct connection to ground when there is no digital gate (Figure III.4). Thus, XNOR gates switch off synapse circuits assigned to boundaries ($A\ XNOR\ \overline{A} = 0$).
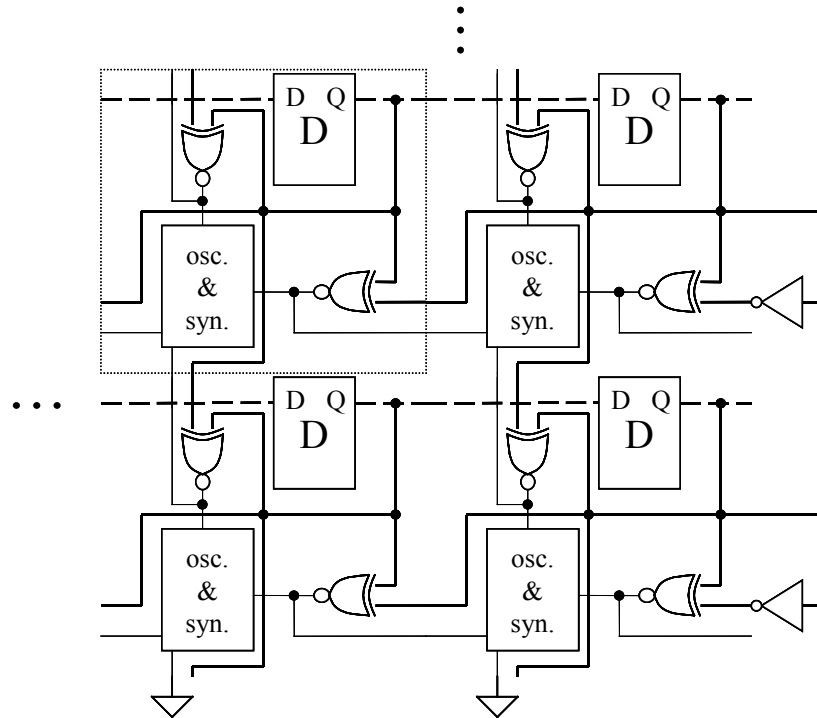
Figure III.4: Digital architecture of the network. Only four cells of the bottom-right corner are presented. Note inverters in the right boundary that force a 0 output of the XNOR gates and the direct connections to ground on the bottom boundary to switch off synapses.

III.3.1 NEURAL OSCILLATOR

The key element of the network is the basic oscillator that makes up the core. This circuit has to be replicated as many times as pixels are in the original image and occupies most of the area and consumes most of the power. For these reasons, the achievement of a small area and low power design is essential while keeping necessary oscillator characteristics, mismatch as low as possible and fast response to other oscillator excitations. In addition, this cell should simplify as much as possible the operation of other elements as synapses and memories.

An important issue to consider in this design is that currents to be compared in the comparator block are low and they must change an output voltage from GND to V_{DD}. Therefore, a first choice was a fast comparator to overcome this drawback. Träff's current comparator [Träff,92] or a fastest version by Tang and Toumazou [Tang and Toumazou,94] were good candidates for it. However, after an analysis and several circuit modifications, we realized that their power consumption was too large for a design whose aim was to reduce this parameter. The reason for its high power consumption is the class B or AB input stage whose transistors operate in saturation zone not only during switching periods but during all the time. This consumption cannot be reduced because the speed of the comparator directly depends on how much current these transistors steer, thus, a possible solution as could be the addition of

starving transistors to reduce currents did not solve the problem. The reduced power consumption is at the cost of a worse speed response and an added complexity (more transistors and bias lines are needed).

Hence, we opted for another comparator design that needed less power than fast comparators mentioned above and more simpler and smaller than starving ones also referenced. The solution was Wang and Guggengühl's hysteresis current comparator [Wang and Guggenbühl,89]. Advantages of this comparator are the possibility of easily controlling comparator thresholds, current consumption is significantly reduced compared to fastest comparators described in the previous paragraph and its area overhead is reasonable. However, its main drawback is its speed for low input currents, which are common in our design.

III.3.1.1 Schematics

The neural oscillator (Figure III.5) is based in Linares et al. current-mode oscillator [Linares et al.,91] and it is composed of a version of Wang and Guggengühl's hysteresis current comparator presented above and an integrator. The main advantage of this circuit is that hysteresis cycle can be easily shifted to both sides because of its current mode input. It only has to be driven some positive or negative current to the output node to shift the cycle to higher or lower thresholds. In addition, as the output is coded in a voltage, it can be easily distributed to neighbor cells. The main drawback of this design is that output capacitance can also alter oscillator orbit. However, as this parasitic capacitance can be controlled in the design step, we have chosen not to buffer the output using any inverter to reduce power consumption peaks during transitions.
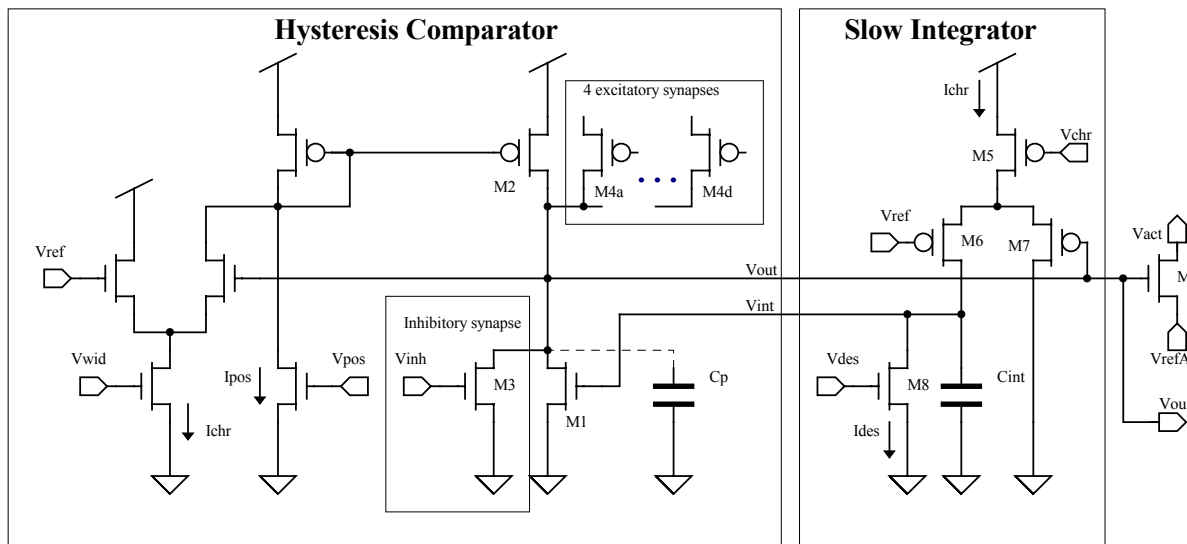
Figure III.5: Basic oscillator schematics.

The output voltage (V_{out}) is the result of integrating the sum of currents driven by transistors M1, M2, M3 and excitatory synapses (M4a…M4d) on the parasitic capacitance (C_p) of the output node. Transistor M1 drives a current that depends on the integrator state (V_{int}) as the I-V characteristic of the MOS transistor. This value is the input current of the comparator. Transistor M2 drives a current that depends on the output voltage and is the responsible of the hysteresis characteristic of the comparator.

When V_{out} is higher than V_{ref}, current I_{wid} is mirrored to M2 and this transistor drives $I_{pos}+I_{wid}$. However, when the output voltage is lower than V_{ref}, M2 only drives I_{pos}. Thus, V_{pos} and V_{wid} control position and width of the hysteresis cycle respectively when synapses are switched off.

Transistor M3 drives the inhibitory current that decreases comparison thresholds and its activity depends on the state of the global inhibitor. Transistors M4a..M4d are the output stages of the excitatory synapses. These transistors shift the hysteresis cycle to higher currents when their associated neighbor cells are active.

The slow integrator consists of a controlled current source (M5, M6 and M7) and a fixed one (M8). The former charges capacitor C_{int} when output voltage is higher than a voltage reference (V_{ref}) and the latter discharges the same capacitor with a constant current given by V_{des}. As current driven by M8 is lower than current driven by M6 when the later is on, the overall result of this circuit is that the capacitor is charged when output voltage is higher than V_{ref} and discharged when this voltage is lower than V_{ref}.

III.3.1.2 Simulations

To study dependencies of this oscillator with its parameters, we have simulated the cell under various conditions. At this step, we have considered that there is no synapse activity, thus the main parameters of the oscillator circuit are bias currents (I_{wid}, I_{pos}, I_{chr}, I_{des}), the reference voltage (V_{ref}) and capacitances C_{int} and C_{out}. Biasing parameters for simulations in this section are shown in Table III.1. Capacitances are equal for all simulations and power-supply voltage is 3.3V as usual in the target technology. Parasitic capacitance in the output node ($C_{int}=15fF$) has been chosen to be as close as possible as estimated after the layout design stage.

I_{wid}	I_{pos}	I_{chr}	I_{des}	V_{ref}	C_{int}	C_{out}	V_{DD}
1µA	300nA	1µA	120nA	1V	1pF	15fF	3.33V

**Table III.1:** Bias parameters used in this section.

In Figure III.6, we present the temporal evolution of output and integrator voltage of the oscillator in the steady state after a brief transient response, which is not depicted. We also show oscillator orbit under the same conditions and voltage thresholds corresponding to I_{pos} and $I_{pos}+I_{wid}$ in Figure III.7.
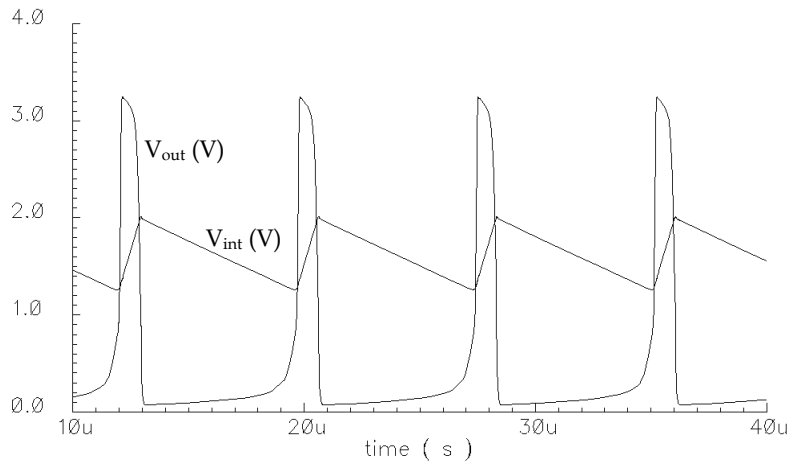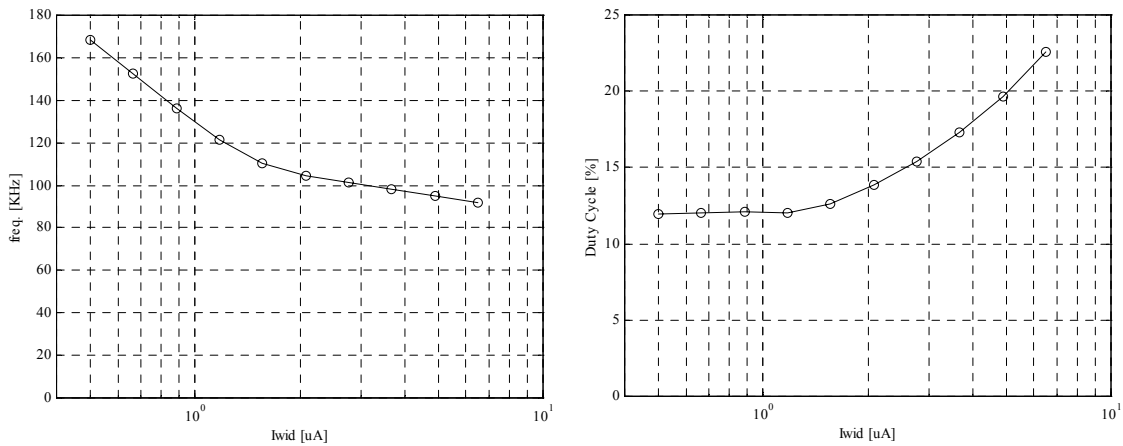
Figure III.6: Temporal evolution of V_{out} and V_{int} voltages of the basic oscillator
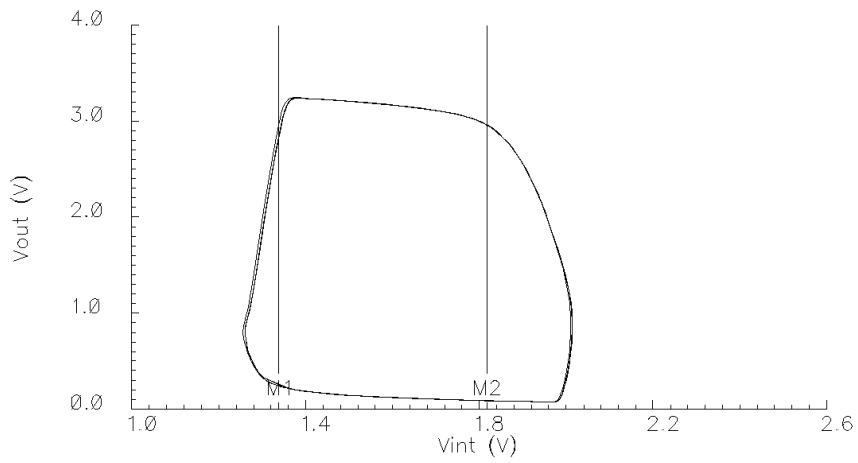
Figure III.7: Oscillator orbit and static voltage thresholds: $V(I_{pos})$ as M1 and $V(I_{pos}+I_{wid})$ as (M2)
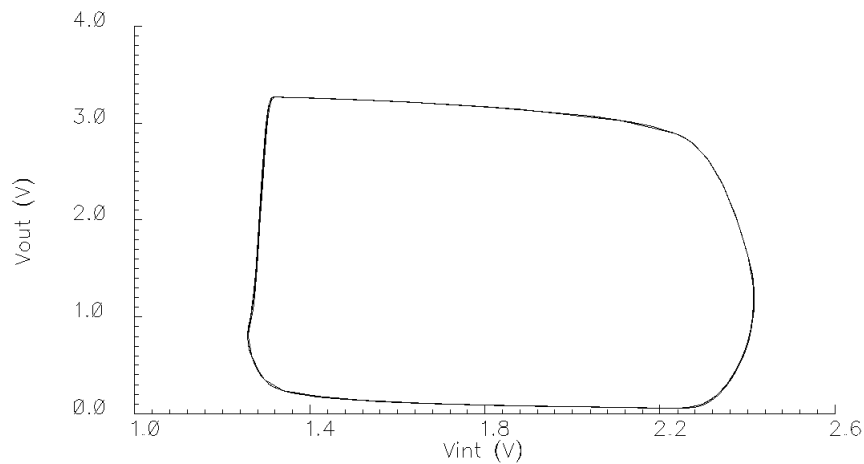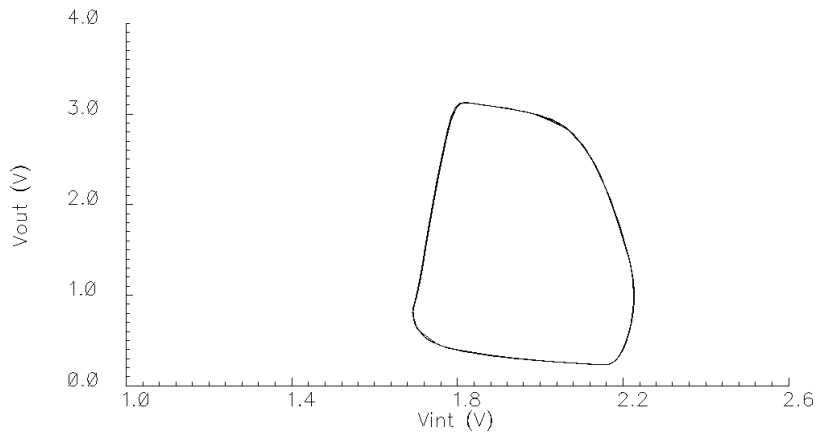
**Figure III.8:** Oscillator orbit when I_{wid} is increased (I_{wid}=2.5μA)

Figure III.9: Oscillator frequency and duty cycle as a function of I_{wid}

Next, we show variations of parameters of the oscillator as a function of biasing current I_{wid}. For simplicity, temporal waveforms of oscillators are not presented in this section because they do not show relevant information. Figure III.8 shows the oscillation orbit of a cell with higher I_{wid}. Notice that when orbit increases its width, oscillation period also increases. In Figure III.9 we show frequency and duty cycle as functions of I_{wid}. Frequency decreases as hysteresis width bias current increases because oscillation trajectory is longer. However, as integrator voltage swing is proportional to the square of currents that are compared and its charging and discharging time is proportional to this voltage swing, frequency decrease is slower at higher currents as depicted. Duty cycle, on the other hand, is kept approximately constant at low currents but it increases as currents become higher.

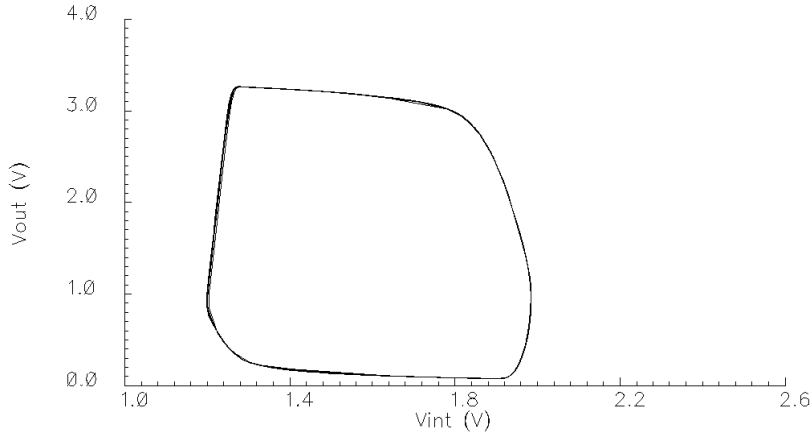**Figure III.10:** Oscillator orbit when I_{pos} is increased (I_{pos}=1µA)
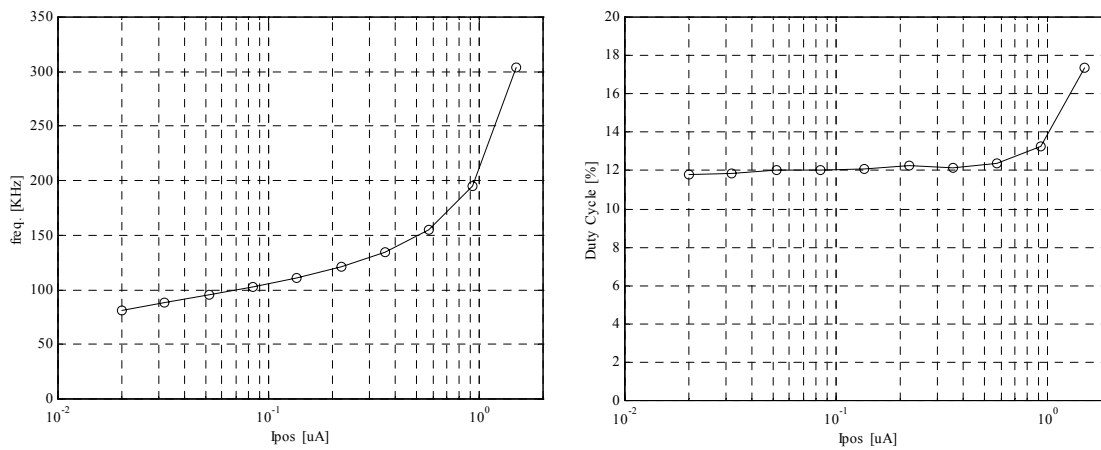
Figure III.11: Oscillator frequency and duty cycle as a function of I_{pos}

In orbit shown in Figure III.10 we have shifted both hysteresis thresholds to higher currents by increasing I_{pos}. This orbit has diminished due to the quadratic relation between V_{int} and the input current of the comparator in Figure III.5, thus, oscillation frequency has increased. Frequency and duty cycle as a function of I_{pos} current is shown in Figure III.11. This plot shows that frequency increases as I_{pos} current increases while duty cycle does almost not change except at higher currents.
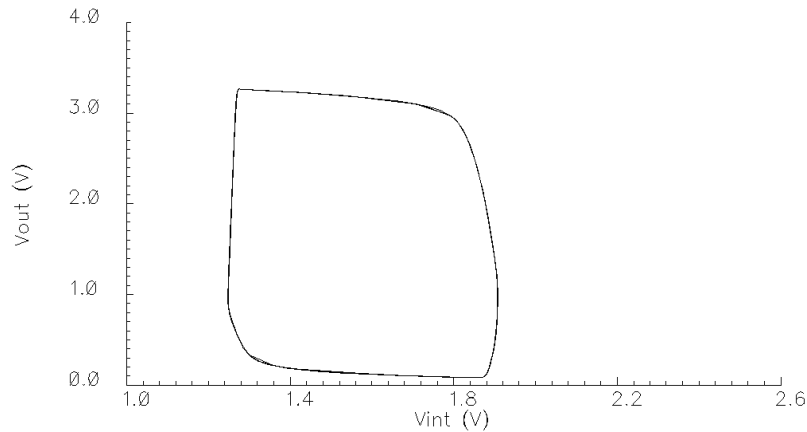
**Figure III.12:** Oscillator orbit when I_{chr} decreases (I_{chr}=333nA)
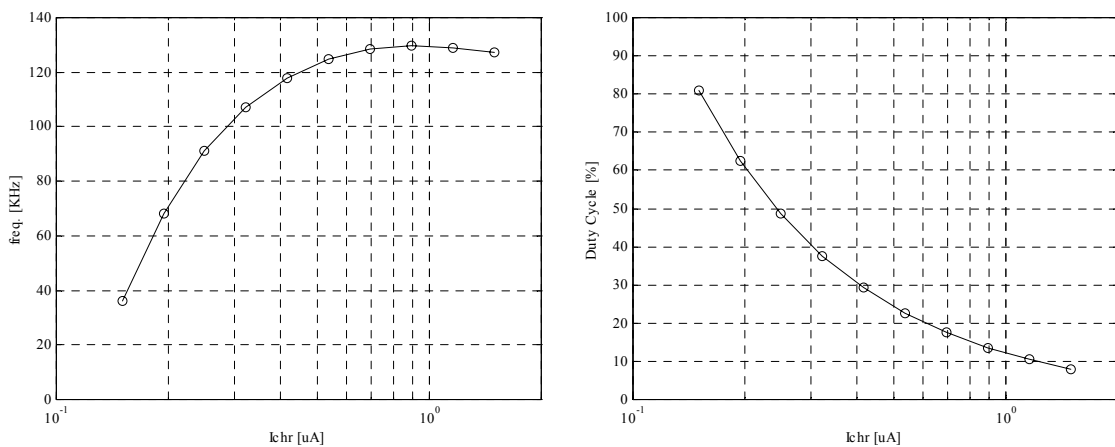
Figure III. 13: Oscillator frequency and duty cycle as a function of I_{chr}

In Figure III.12, we show the orbit of an oscillator with a smaller charging current (I_{chr}). As this current is lower than compared to Figure III.7, changes in the integrator node (V_{int}) are slower and the orbit is closer to the ideal orbit with no output delay. We also show frequency and duty cycle as a function of this current in Figure III. 13. Frequency increases and duty cycle decreases as charging current increases due to the reduction of the charging time of the integrator capacitor. However, the effects of I_{chr} on frequency are weaker as this current increases because active cycle is shorter and frequency depends more on I_{des}. Both biasing parameters are very important for computing purposes due to the high dependency of duty cycle on them. The smaller the duty cycle is the more objects that can be segregated in a scene.

Figure III.14: Oscillator orbit when I_{des} increases (I_{des}=333nA)
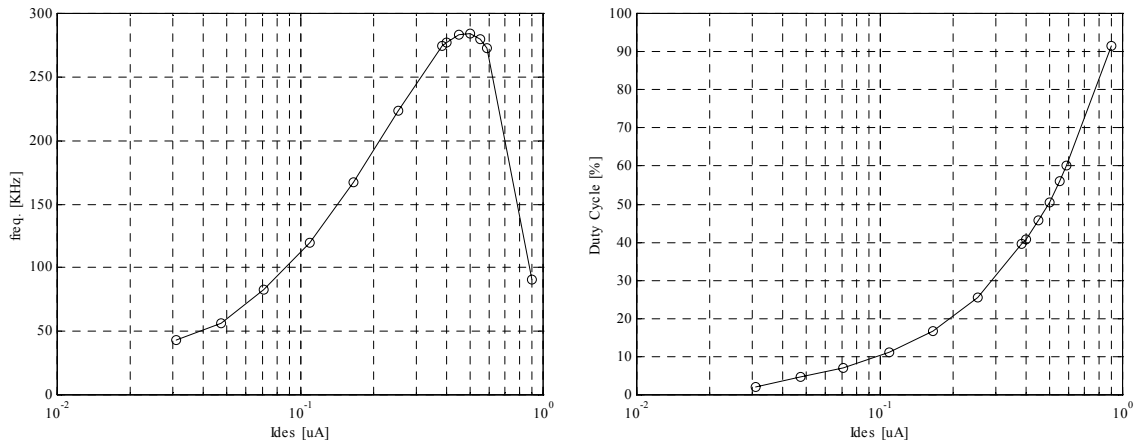
**Figure III.15:** Oscillator frequency and duty cycle as a function of I_{chr}

Next, we show the influence of I_{des} to frequency and duty cycle. In Figure III.14, the orbit is plotted as a function of I_{des}. When this current is increased, as depicted in Figure III.15, duty cycle and frequency increase due to faster integrator discharge. However, as total integrator charge current is the difference of I_{chr} and I_{des}, frequency decreases when total charge current (I_{chr}-I_{des}) equals the discharge one (I_{chr}-I_{des}=I_{des}⇒I_{des}=I_{chr}/2=500nA in the example). This is because frequency is inversely proportional to the sum of charging and discharging time and this value has a minimum at this point.

Finally, although not shown, we have simulated the effect of varying V_{ref}. Simulations have shown that variations of this parameter does not affect frequency and duty cycle, as expected, provided comparator transistors remain in saturation zone.

III.3.2 EXCITATORY SYNAPSES

Excitatory synapses are presented in Figure III.16. The objective of this module is to drive a current to the output node when an excitatory cell is in its active state. Excitatory cell in this context means that the cell is physically adjacent to the basic cell and they both have the same feature (i.e. both cells store black pixels or both cells store white pixels). In addition to this, the result of the sum of excitatory currents fed to a

single cell should be normalized to maintain the same orbit (thus the same frequency) for all oscillators. For this reason, the total current is first divided between all excitatory cells, thus, each cell can drive a current I_{exc}/n where n is the number of excitatory cells (neighbor cells with the same feature).
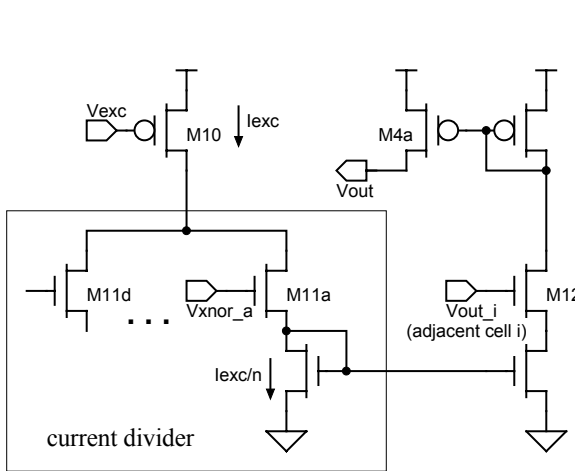
Figure III.16: Excitatory synapse schematic
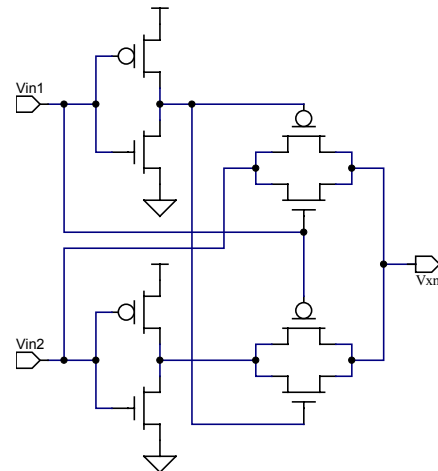
Figure III.17: XNOR gate

As the design presented in this chapter considers a neighborhood of 4 cells, the circuit has 4 different branches (branch *a* to branch *d*) to divide the excitatory current that is driven to the comparator.

To detect similarity of cells, a XNOR operation is performed by circuit shown in Figure III.17. Digital outputs of four XNOR operations for each cell control pass transistors M11a..M11d in Figure III.16. Excitatory current is mirrored to M12a..M12d. These transistors are switched on and off depending on the state of the neighbor cell output. Thus, when the neighbor cell has the same feature (M11 on) and is active (M12 on), current is driven to M4a (represented as M4a..M4d in Figure III.5 referring to all four synapses per cell) and comparison thresholds of oscillator are increased. On the other hand, if one or both of conditions are not accomplished, no current is driven to the comparator and thresholds are not shifted.

Note that delays generated in excitatory synapses can be neglected. Sources of delays in this stage are rising time of the excitatory adjacent cell connected to gate of M12, output of synapse (transistor M4) that is connected to the output of the cell and gates of PMOS current mirrors that are switched on and off in each cycle. As the first and second of these delays are related to an output node, they are computed when the output capacitor is considered in the output delay model. The latter source, can be estimated by Eq.III.3:

$$\Delta t = \Delta V \frac{C}{I}$$

Eq.III.3

where Δt is the time to switch excitatory current from zero to its final value, ΔV is the voltage shift of transistor gates ($\approx$0.2 Volts), I the value of biasing current and C the parasitic capacitance of the node. This parasitic capacitance is mainly due to transistor

gates and its value for two 2x2μm² transistors in AMS 0.8 technology is calculated for this design in Eq.III.4:

$$C_{gates} = 2 \cdot \frac{w \cdot l \cdot \varepsilon_{ox}}{t_{ox}} \cong 18 fF \qquad \text{Eq.III.4}$$

where t_{ox} is the gate oxide thickness (15nm), ε_{ox} is the gate oxide permittivity ($3.45 \cdot 10^{-11} F/m$) and w and l are transistor dimensions (2x2μm²).

Result for Eq.III.3 is Δt[ns]≈3.6/I[μA], which is much smaller than delay produced by the output capacitance of cells. Simulations (Figure III.18) for different biasing conditions demonstrate that they are small enough to be neglected or modeled as a different reference voltage (V_ref) when pulses are as slow as presented in previous simulations.
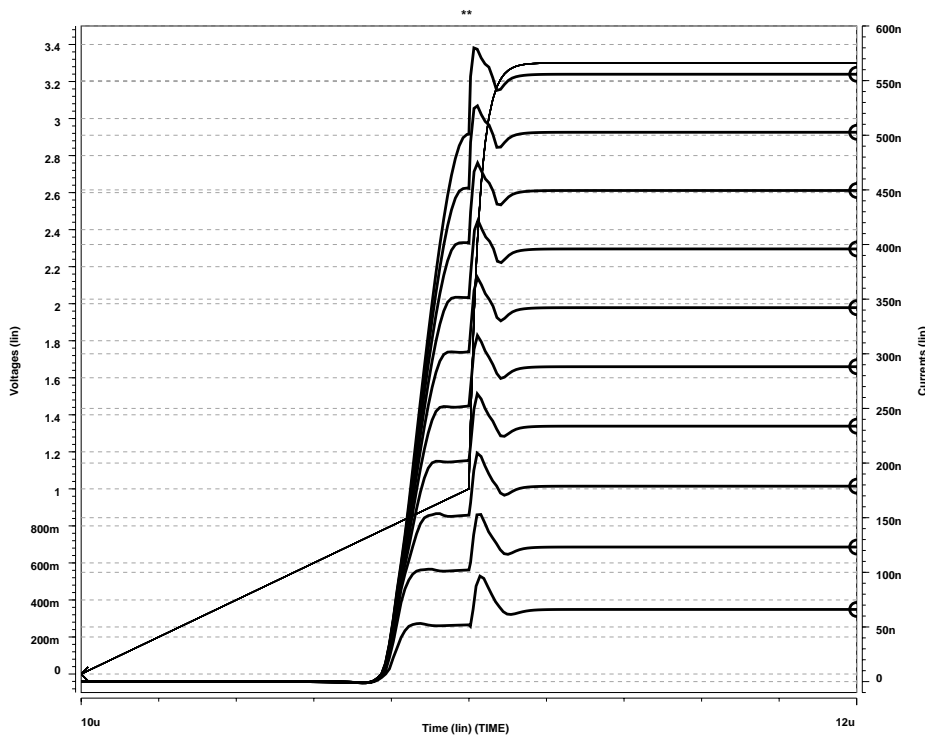
Figure III.18: Excitatory synapse current activity (thick lines) for different biasing values when a neighbor cell output voltage (thin line) switches to active. Note that excitatory synapse becomes active during the switching time of the output voltage; thus, the former delay can be modeled as a slight modification of the reference voltage.
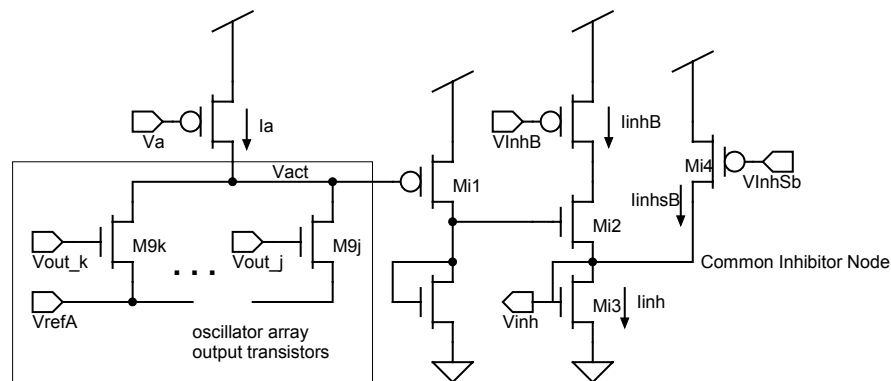
III.4 GLOBAL INHIBITOR

Inhibition is performed by M3 transistor current (Figure III.5). This transistor is controlled by voltage V_{inh} that is generated by circuit of Figure III.19. A switching transistor (M9 in Figure III.5) is connected to the output of each basic cell. Any M9 transistor of the network can pull down a common node voltage V_{act} to V_{refA} when its cell is active, thus, oscillator activity is easily detected in this common node.

When the common node V_{act} voltage is pulled down to V_{refA}, it turns on switches Mi1 and Mi2. Thus, current I_{inhB} is driven to transistor Mi3 and this current is mirrored to transistors M3 (Figure III.5) of each basic cell, inhibiting the activity of all oscillators. To speed up transistor MI3 switch, whose gate is connected to a very large parasitic capacitance because this line is distributed to the whole network, a small biasing current I_{inhSb} is generated by Mi4. This current maintains transistor Mi3 in its active state even when there is no inhibition. Note that this small biasing current does not have any effect on oscillators because it can be easily compensated by higher I_{pos} biasing. In addition to this, I_{inhSb} can be also used to control the switching time of the global inhibitor and improve the performance of the overall system.

Note that a different node (V_{refA}) has been used as a reference for the inhibitor. The reason for this is to keep the other reference node (V_{ref}) as stable as possible and not affected by currents flowing through node V_{refA}.

Figure III.19: Global inhibitor cell

Temporal response of circuit in Figure III.19 mainly depends on biasing current (I_a), the aspect ratio of transistors M9 and the parasitic capacitance in node V_{act}, which is quite big because all cells in the network are connected to it. Minimum size transistors are used to reduce cell area ($2 \times 0.8 \mu m^2$ in our technology) and parasitic capacitance depends on layout design and network size, which is 5pF in our design. Thus, parameter I_a is the best suited to easily modify the delay of this node.

When there is no activity in the network, no pull-down transistor is turned on and voltage V_{act} is close to V_{DD}. The falling time can be approximated by Eq.III.3 where $\Delta V = V_{dd} - V_{refA}$ (2.3V in our tests) and C=5pF in our tests ($\approx$20fF/cell*256cells).

Therefore:

$$\Delta t[\mu s] \approx 11.5/I_a[\mu A] \qquad\qquad \text{Eq.III.5}$$

To estimate the rising time of V_{act} is not as easy as the falling time, in spite of being of more interest because it is the responsible of distinguishing objects in the network. The drain resistance of a diode-connected transistor (M9) with a certain bulk to source voltage varies with drain and gate voltages (Eq.III.6) [Weste and Eshraghian,93]. These voltages vary during the switching cycle and delay depends on the number of transistors that are switched on. Moreover, transistors do not have to switch simultaneously, which makes estimation more complex.

Estimation for the drain to source resistance is [Weste and Eshraghian,93]:

$$\begin{cases} R_{DS} = \dfrac{V_{DS}}{\beta(V_{GS}-V_T)^2} & \textit{saturation region} \\[2em] R_{DS} = \dfrac{1}{\beta\left(V_{GS}-V_T-\dfrac{V_{DS}}{2}\right)} & \textit{linear region} \qquad \text{Eq.III.6} \\[2em] V_T = V_{T0} + \gamma\left(\sqrt{2|\phi_F|+V_S}-\sqrt{2|\phi_F|}\right) \end{cases}$$

where β is the transconductance parameter, V_{GS} the gate-source voltage, V_{DS} the drain-source voltage, V_{T0} the zero bias threshold voltage, γ is the bulk threshold parameter and $2|\phi_F|$ the surface potential.

When the output of a given oscillator cell k is above a threshold voltage ($V_{refA}+V_T$), the switching transistor M9k turns on and sinks I_a current to the reference node through its drain to source resistance (Eq.III.6). Notice that when the activity detector receives cell activity, it will not reach V_{refA} but a value above it due to MOS switch channel resistance. This resistance depends on MOS transistor threshold voltage, which also depends on the body effect.

The switching process is as follows. First, the switching transistor is at its saturation region ($V_{DS}>V_{GS}-V_T$) but it operates in its linear zone when the output voltage decreases to $V_{act}=V_{DD}-V_T-V_{ref\_a}$. For a rough estimation of switching delay of the activity detector, we consider that this value is constant and it is approximated by its mean value, although being an optimistic approximation [Laker and Sansen,94]. For a minimum transistor of the technology we have used, a voltage reference of 0.5V and a 3.3V power supply, this resistance is $\approx 3k\Omega$. If voltage should change from V_{DD} to V_{refA} and the output pulse is a perfect square wave, the time constant for a parasitic capacitance of 5pF is 15ns and the node final value $V_{act}(t\rightarrow\infty)\rightarrow V_{refA}+(3k\Omega)\cdot I_a$, which is on the order of some tens of millivolts over V_{refA} for currents of some microampere. Thus, the resistance component can be neglected as well as being even smaller when more than one switching transistor is on.

For a better approach, we have simulated the discharging time of node V_{act} under the assumed conditions in Figure III.20. It plots the temporal behavior of this node in Figure III.19 plus a parasitic capacitor of 5pF for different I_a biasing currents (from 1μA to 100μA).
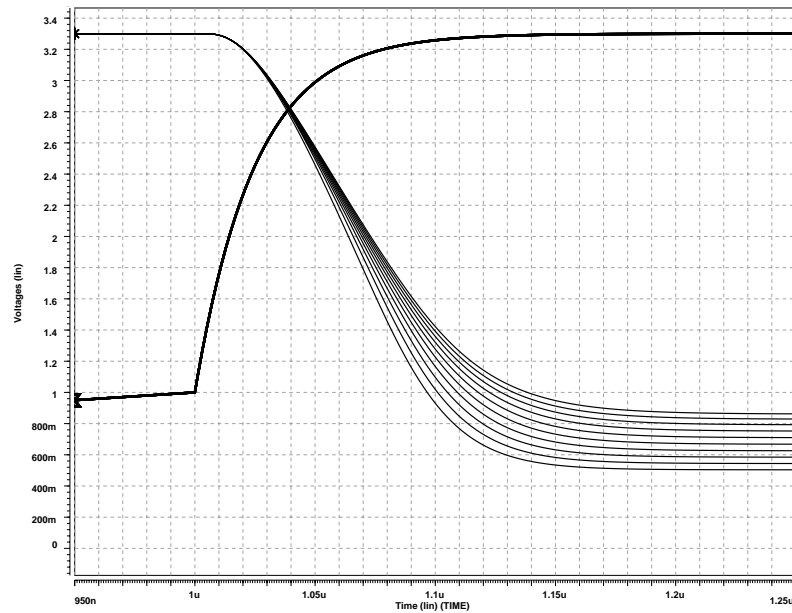
Figure III.20: Discharging time delay of V_{act} node (thin lines) for different pull-up I_a current biasing (from 1µA to 100µA**)** and an oscillator like input (thick line)

Note that the switching starts after the input voltage has reached a threshold ($V_{ref\_a}+V_T$), which depends on the pull-down transistor (Eq.III.6). This reference voltage must be adjusted to be bigger than the reference voltage that shifts hysteresis comparators of oscillators because if inhibition starts before the hysteresis shift, it could stop oscillations. Simulations show that the shift of this voltage is quite fast (it is on the order of some tenths of nanoseconds) and the voltage difference due to drain to source resistance is not important. Therefore, parameter I_a must be chosen for an appropriate time delay in Eq.III.5 and moderate power consumption.

III.5 ACTIVITY DETECTORS

To detect the state of oscillators and output this information to external circuits, some elements have been added. It is important to note that the output process may take an important fraction of oscillation cycle, thus, the network state at a certain time should be memorized and then, the circuit should output this information independently of the evolution of oscillators. This operation is achieved by first activating a *'load'* signal. Afterwards, each cell memorizes its state in a dynamic memory cell and then, the circuit outputs the stored information by rows through a 16-bit output bus.

In Figure III.21 we show the activity detection circuit for one column of the network. The block on the left is cloned in each oscillatory cell. This block consists of 3 NMOS transistors. Md1 switches on when the global signal *'load'* activates. Then, oscillator output is loaded into the gate of Md2. If this oscillator were in its active state,

this transistor gate is charged and this charge is maintained, at least a few milliseconds, this state when the *'load'* signal changes to ground independently of posterior oscillator evolution. When the corresponding row is selected, transistor Md3 switches on and transistor Md2 pulls down the voltage of the column common line. This column line is connected to a pull-up transistor Mdb. Thus, the column voltage is low when the cell selected was in its active state when the *'load'* signal was generated. Otherwise, the column voltage remains high. Then, the output inverter detects the column voltage and buffers it to the column output, which is 0 when the cell was silent and V_{DD} when it was active.
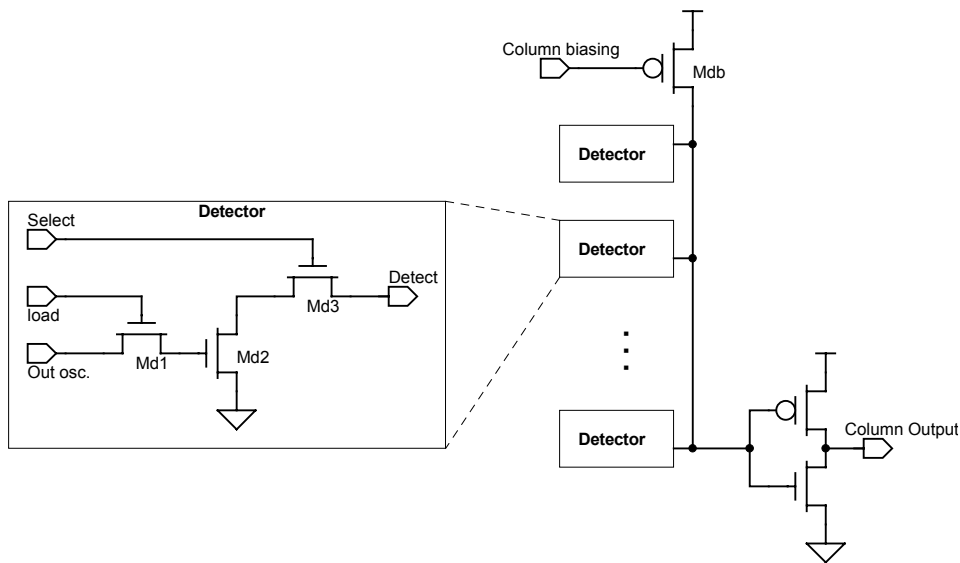
Figure III.21. Activity detection circuit for 1 column. The block depicted on the right is cloned in each cell.

The circuit presented above does not strictly belong to the segmentation scheme presented in this chapter. It is an engineering solution to sample and output results of the network. The final design will depend on the application of the circuit and the stage where it is connected.

Although it is important to know how long digital information stored in transistor Md2 is valid, no simulations are presented in this chapter because simulation models are not accurate enough to obtain this value. However, a rough approximation can be made. If leakage current of transistor Md1 is on the order of 1fA (drain perimeter is 8μm and leakage current 0.12fA/μm), gate capacitance of transistor Md2 is 3.6fF (2x0.8μm^2) and we can accept a fluctuation of gate voltage of 1V, information is valid during some seconds. This information must be kept until the reading process is completed, which will take much less than one second.

In addition to this, the reading process must be also fast because the *'load'* signal only stores the network state at a certain time step and it is necessary to know the state of the network at different time steps to detect different objects. The faster the reading process is, the better the temporal resolution of the output is. If the system cannot

output the information fast enough, some kind of trigger synchronization should be added to read information during different oscillation cycles.

For this reason it is important to know the time it takes the circuit to read a bit of data. This delay is related to the biasing current of each column driven by Mdb and drain resistances of Md3 and Md2. This value can be estimated with Eq.III.6, but it will not be a good approximation as discussed above in estimation of delay of V_{act}. Moreover, this estimation will be even worse because there are two transistors and two output nodes instead of one. For this reason we only show some simulations with different column biasing currents (from 3μA to 30μA), a pull-down minimum transistor (2x0.8μm^2) and a parasitic capacitance of 300fF in Figure III.22.
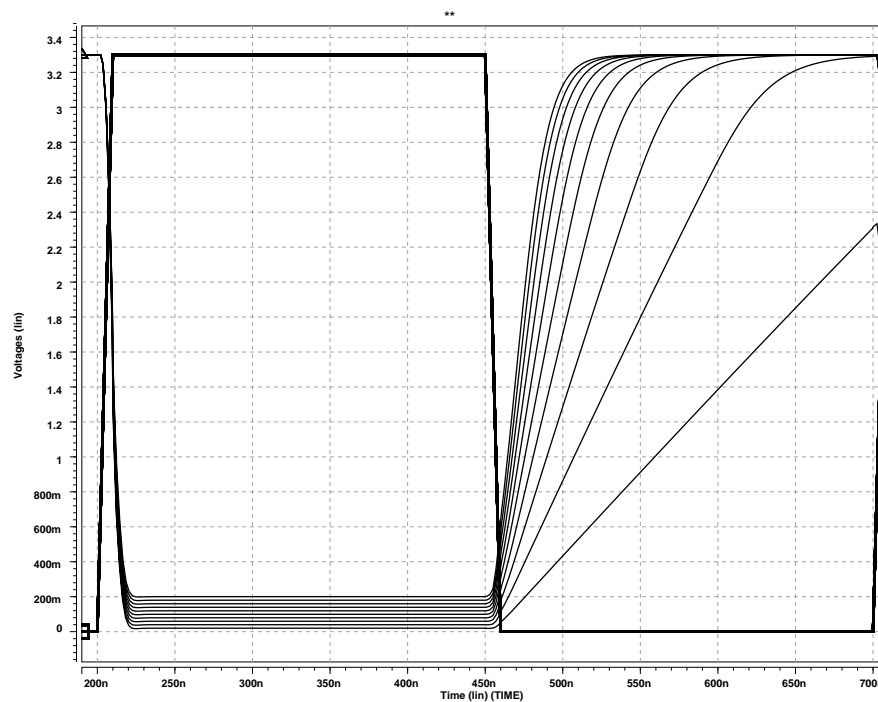
Figure III.22: Activity detector response (thin line) to selection pulse (thick line) with different pull-up biasing currents (from 10μA to 100μA)

As seen in Figure III.22, in addition to the trade-off between speed and power consumption, transistor area must be considered. Drain resistances of pull-down transistors are responsible for the output not reaching the ground voltage, thus, for larger biasing pull-up currents, pull-down transistors should be bigger to keep the low-state voltage low enough if no complicated or power consuming sense amplifiers are to be used.

III.6 CONTROL CIRCUITS

In addition to network circuits, some other biasing analog circuitry and digital circuitry has been added to control input-output operations.

III.6.1 ANALOG BIASING

To generate biasing currents for analog circuits, simple current mirrors that copy an input current to all cells are used. As exact value of these currents is not crucial if it is the same for all cells, high precision is not important at this stage. For this reason we have used simple current mirrors and not more complex ones as cascodes. In addition to this, the input value is a current and not a gate voltage to avoid temporal fluctuations of the voltage that would affect currents quadratically. In addition, this structure protects transistor gates, which are more sensitive to outer electrostatic discharges than transistor drains.

This configuration, although not being practical for a final design because it needs external current or voltage generators, it allows us to change biasing values for testing purposes easily.

III.6.2 DIGITAL CONTROL

To select the row to output in the 16-output mode or the row and column for the serial output, two 4x16 standard digital decoders have been implemented.

Moreover, there are also direct outputs from some border cells to quickly and easily check network oscillations without the need of using activity detectors described above and decoders. They are just buffer inverters whose inputs are connected to outputs of some border oscillators.

III.7 IMPLEMENTATION

To implement this network we used standard double-poly CMOS AMS 0.8μm technology. This technology allowed us to build oscillators with precise and compact integration capacitances. Although capacitor precision is not important if all capacitors are as similar as possible, double-poly technology allowed us to isolate integrators from substrate interferences. This is an important feature if integrator node controls oscillations with a reduced voltage swing and it is more sensible to interferences. These interferences would be more important in poly to substrate capacitors and maybe they could have produced critical undesired effects.

The circuit has been packaged in a CLCC package with 84 external connections and the final design silicon area of the complete circuit, including I/O Pad's, is 6.7mm². In Figure III.23 we show a microphotograph of the circuit. In addition to this, in Figure III.24 we show the detail of a single cell we have designed that can be easily replicated to build MxN networks. Its area is 129x90μm² including biasing wiring and 85x79μm² without biasing wiring.
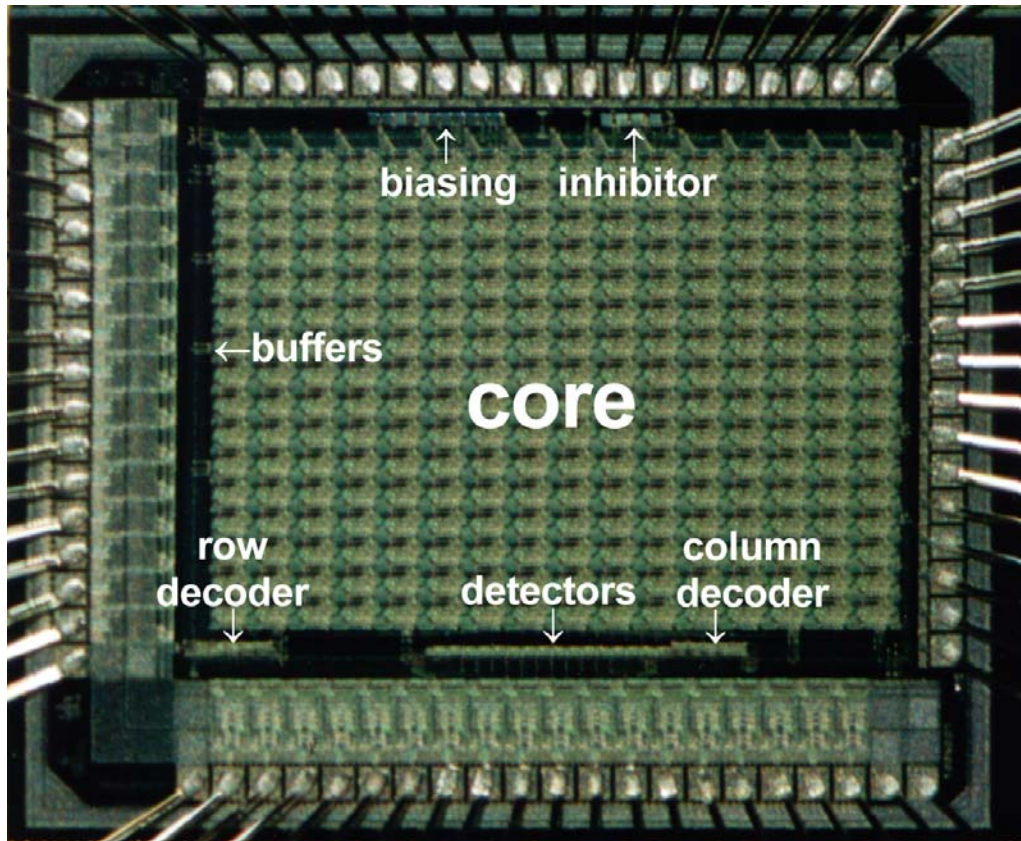
Figure III.23: Microphotograph of the complete circuit. We indicate different components of the design.
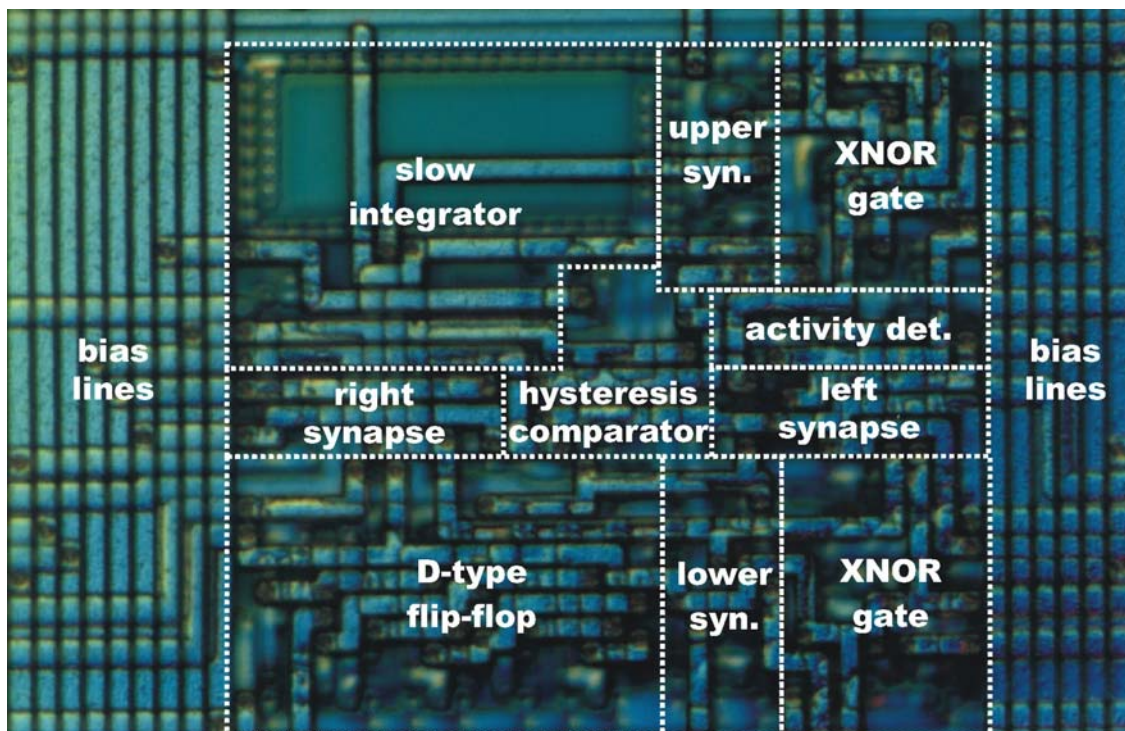

Figure III.24: Microphotograph of a single cell with its different parts. Biasing connections can be easily distinguished on each side of the photograph and the integrator capacitor on the upper left corner.

III.8 CONCLUSIONS

In this chapter, we have presented a microelectronic design for the network of oscillators and we have simulated its behavior under different biasing conditions. Simulations show that this implementation of the circuit accomplishes the basic conditions for segmentation purposes while maintaining a small and compact design.

It should be mentioned that although using a double-poly analog technology, possibilities to build this network using a cheaper digital technology should be studied. This technology, in addition of being cheaper, would allow more connectivity because of the higher number of metal layers, higher integration and the possibility of embedding it with other digital circuits.

We should note that the design presented has been designed for testing purposes, thus it has been optimized for it. A final design should have different input stages (photoreceptor devices instead of D-type flip-flops) and output circuitry can be reduced to application purposes because it could not be necessary so much information as extracted in our design.