Chapter 2.

MULTILEVEL TOPOLOGIES. PROTOTYPE DESCRIPTION AND MODELING

2.1. Multilevel Topologies

There is a growing interest in multilevel topologies since they can extend the application of power electronics systems to higher voltages and power ratios. Multilevel converters are the most attractive technology for the medium- to high-voltage range (2-13 kV), which includes motor drives, power distribution, power quality and power conditioning applications.

Multilevel converters can synthesize waveforms by using more than two voltage levels; hence, the quality of the spectra is significantly improved compared with the classic two-level topology.

The main drawbacks of the multilevel converters are that:

- these topologies require a high number of switches,

- their control is difficult because of such amount of devices, and

- several DC voltage sources are required, which are usually provided by capacitors. Balancing the voltages of these capacitors according to an operating point is a difficult challenge.

Despite these drawbacks, multilevel converters have turned out to be a very good alternative for high-power applications, since the cost of the control for these cases is a small portion of the whole cost of the system. Furthermore, as prices of

power semiconductors and DSPs continue to decrease, the use of multilevel topologies is expected to extend to low-power applications (those of less than 10 kW) as well. Fast power devices (CMOS transistors), which can operate at very high switching frequencies, can be used for low voltages. Therefore, the values of the reactive components will undergo significant reduction. Furthermore, new power devices are expected to appear in the next some years, and these may also extend the application of multilevel topologies.

So far, the most actively developed multilevel topologies are:

- the diode-clamped converter,

- the floating-capacitor converter, and

- the cascaded H-bridge converter.

Other names are used to define these topologies. For example, when referring to the three-level diode-clamped converter, it is also called the NPC converter. This name cannot be extended to topologies with a higher number of levels because of the multi-clamped points available.

On the other hand, the name “converter” is preferred instead of “inverter” in this dissertation, because of the more general sense of this word. These systems can operate as inverters or as rectifiers, depending on whether the energy flux flows from the DC to the AC side, or from the AC to the DC side, respectively.

2.1.1. Diode-Clamped Converter

Since its introduction in 1981 by Nabae et al. [A1], the three-level diode-clamped converter (or NPC converter) has been the most practical and widely studied multilevel topology (Fig. 2.1).

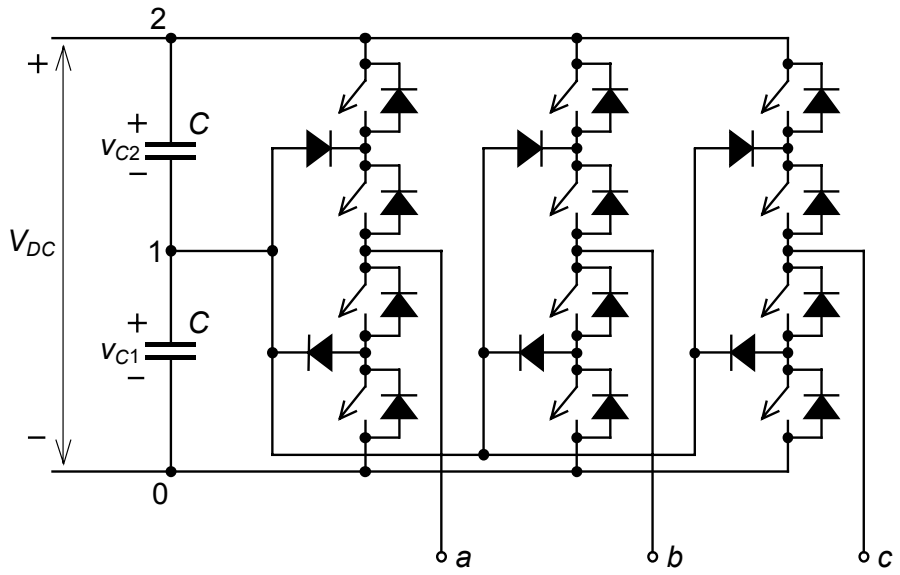


Fig. 2.1. *Three-level diode-clamped converter.*

This topology has been extended to higher numbers of levels. Fig. 2.2 shows the four-level version of this converter.

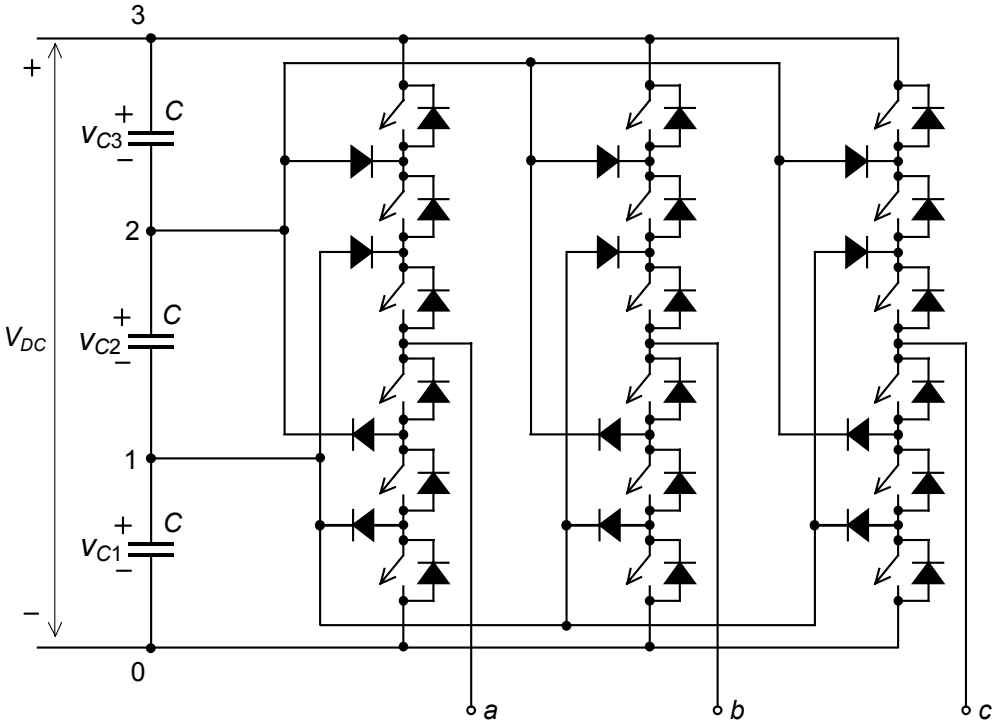


Fig. 2.2. *Four-level diode-clamped converter.*

For the general case of an n-level topology, *n*-1 consecutive switches of each leg must be in the on-state. As a result, a defined voltage level of the series capacitors is connected to the output. Three single-pole n-throw switches, as shown in Fig. 2.3, can perform as a functional diagram of this converter.

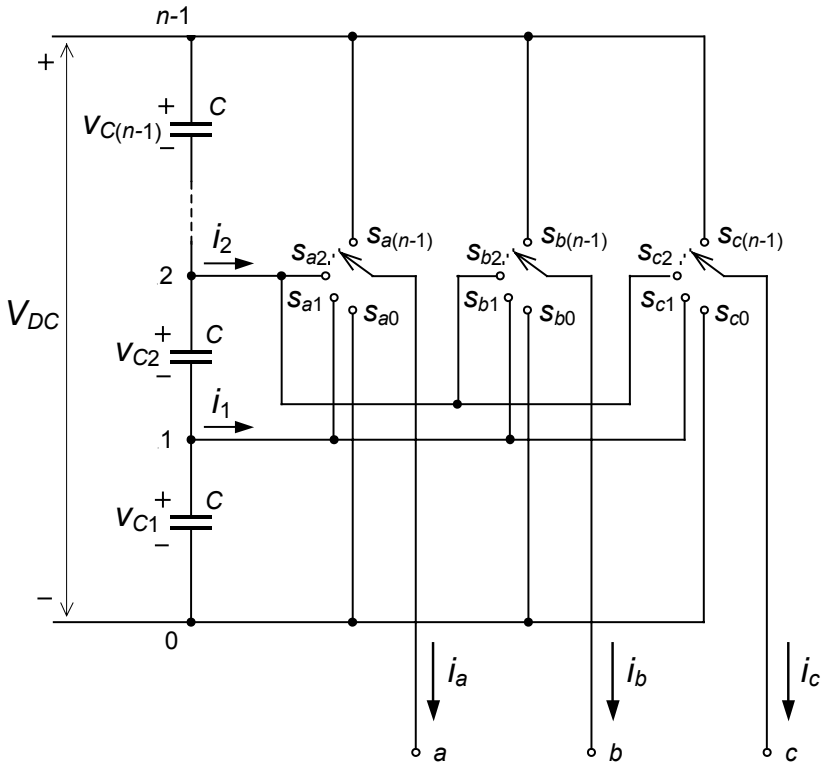


Fig. 2.3. *Functional diagram of the n-level diode-clamped converter.*

Expression (2.1) summarizes all of the possible combinations. The variables s_{ij} are the control functions of the single-pole n-throw switches. These variables define the position of the switches, so that they have the unity value when the *i* output is connected to the *j* point; otherwise they are zero ($s_{ij} = \{0, 1\}$).

$$\sum_{j=0}^{n-1} s_{ij} = 1 \quad \text{with } i=\{a,b,c\} \tag{2.1}$$

Referring all of the voltages to the lower DC-link voltage level (“0” reference), each output voltage consists of contributions by a determinate number of consecutive capacitors:

$$v_{i0} = \sum_{j=1}^{n-1} \left(s_{ij} \sum_{p=1}^{j} v_{Cp} \right) \quad \text{with } i=\{a,b,c\}. \tag{2.2}$$

When balanced distribution of the DC-link voltage among the capacitors is assumed:

$$v_{i0} = \frac{V_{DC}}{n-1} \sum_{j=1}^{n-1} j\, s_{ij} \quad \text{with } i=\{a,b,c\}. \tag{2.3}$$

Under balanced conditions, the maximum forward voltage applied to the switches of the bridge is the voltage of one single capacitor.

Fig. 2.4 shows a voltage waveform obtained from an n-level converter in the case of balanced voltages in the capacitors.

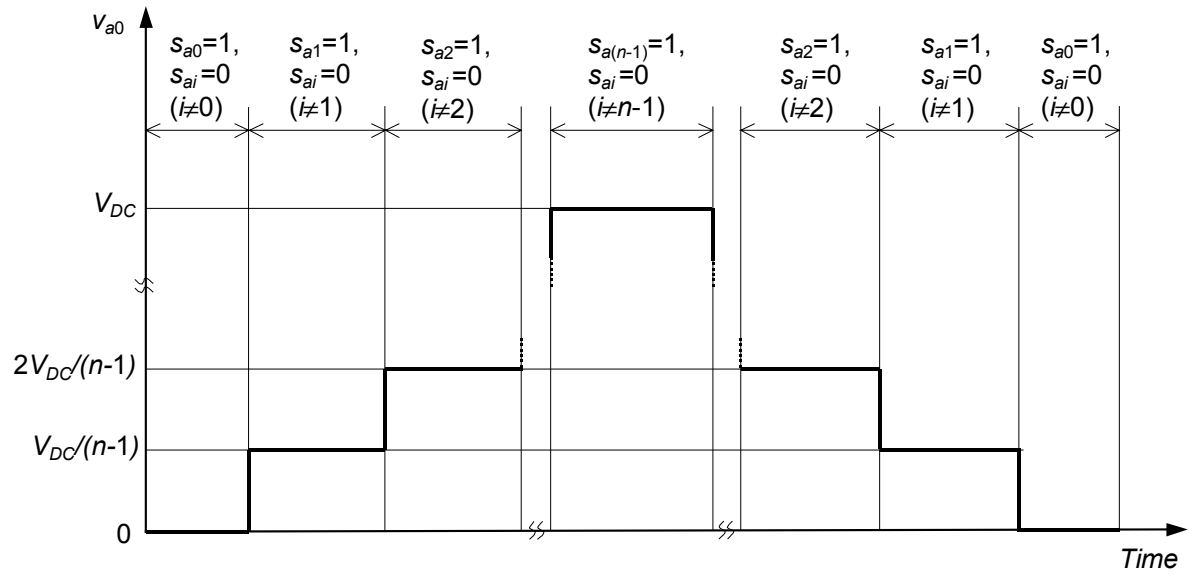


Fig. 2.4. *Example of voltage waveform generated by an n-level converter.*

The advantages of the diode-clamped converter compared with other multilevel topologies are that:

- They use a low number of capacitors. Although these topologies require some additional clamping diodes, their low number of reactive components is usually preferred from the standpoint of cost.

- They can be connected to a single DC-link voltage. The floating-capacitor topology also shares this advantage, but the cascade converter does not, since this converter requires multiple isolated DC power supplies.

Nevertheless, some practical experience with this topology reveals technical difficulties that complicate its application, as follows:

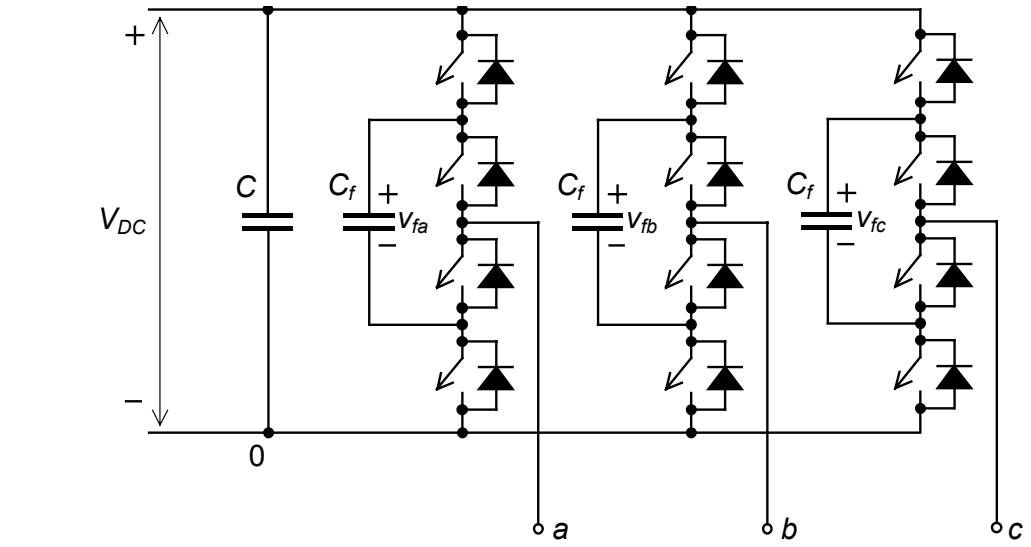
- For topologies with more than three levels, the clamping diodes are subject to high voltage stress equal to $V_{DC}(n-2)/(n-1)$. As a result, series connection of the diodes is required. This issue complicates the design and raises reliability and cost concerns.

- The objective of maintaining the charge balance of the capacitors in topologies with a high number of levels (more than three) has been demonstrated to be impossible for some operating conditions [A37]. These balancing problems appear when dealing with deep modulation indices and active currents. Therefore, high AC output voltages cannot be achieved, which inhibits the most important attribute of multilevel converters. Significant balancing improvements are obtained when two or more converters are connected to the same DC link. These converters are also used for static VAR compensation circuits in which no active power is transmitted and the balancing problem can be handled.

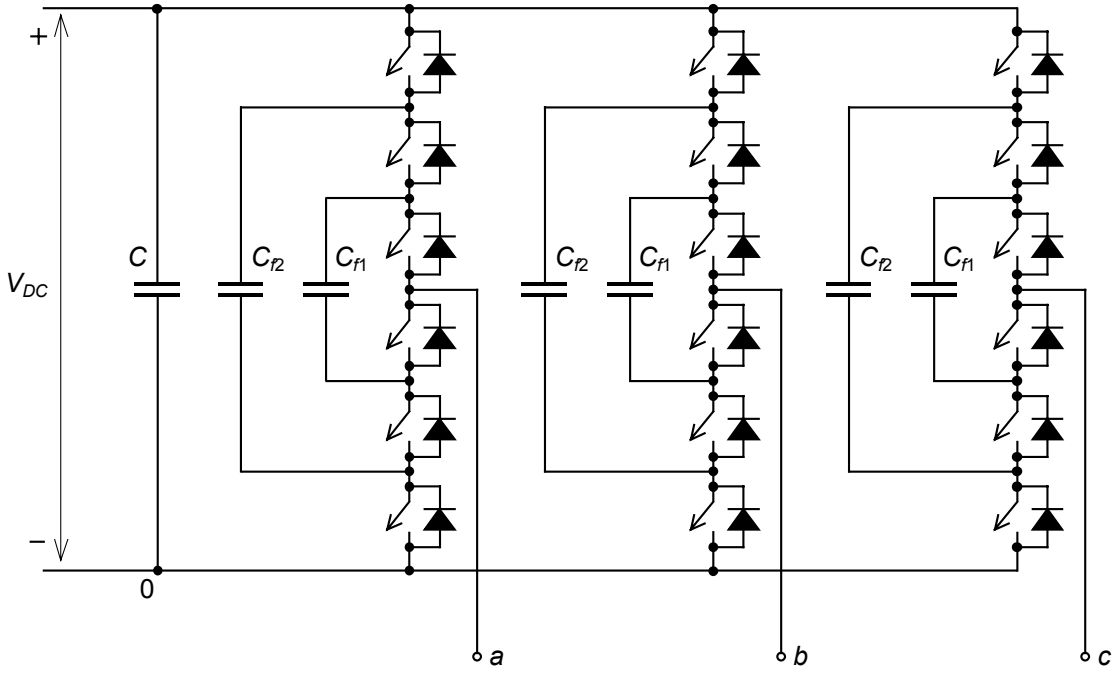
- Although proper control of the three-level topology overcomes the voltage balance concern, a low-frequency ripple in the NP potential appears when dealing with large modulation indices and low PFs. The maximum voltage applied to the devices is higher due to this oscillation, and additionally, it produces low-frequency distortion in the AC output voltages. Some solutions for this problem are proposed in this dissertation.

2.1.2. Floating-Capacitor Converter

Meynard et al. [A2, A3] introduced the floating-capacitor converter. In this topology the voltage clamping is achieved by means of capacitors that “float” with respect to the earth potential. In Fig. 2.5, the three-level and four-level versions of this converter are shown.



(a)



(b)

Fig. 2.5. *(a) Three-level and (b) four-level floating-capacitor converters.*

Each leg of these topologies can be seen as an imbricate cell where the output voltage is synthesized by connecting a defined number of capacitors in series.

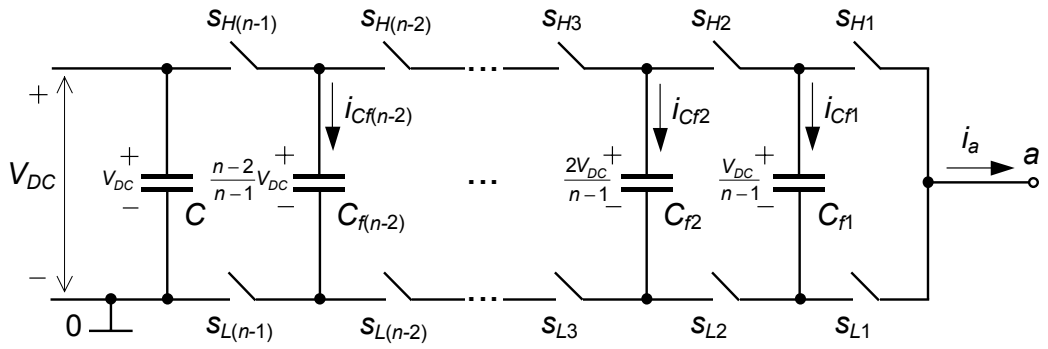


Fig. 2.6. *Imbricate cell, base of the floating-capacitor converter.*

One out of each pair of switches s_{Hi} and s_{Li} must be in the on-state for a proper connection to exist between the DC-link potential and the output through some capacitors. Additionally, both switches cannot be on at the same time or else short circuits will occur in the capacitors. Table 2.1 shows all the possible states of the switches in three-level and four-level converters (only the upper switches' states are given).

Table 2.1. *Possible states of the switches in (a) the three-level, and (b) the four-level floating-capacitor converters.*

s_{H2}	s_{H1}	v_{a0}	i_{Cf1}
off	*off*	0	0
off	*on*	$V_{DC}/2$	$-i_a$
on	*off*	$V_{DC}/2$	i_a
on	*on*	V_{DC}	0

(a)

s_{H3}	s_{H2}	s_{H1}	v_{a0}	i_{Cf2}	i_{Cf1}
off	*off*	*off*	0	0	0
off	*off*	*on*	$V_{DC}/3$	0	$-i_a$
off	*on*	*off*	$V_{DC}/3$	$-i_a$	i_a
on	*off*	*off*	$V_{DC}/3$	i_a	0
off	*on*	*on*	$2V_{DC}/3$	$-i_a$	0
on	*off*	*on*	$2V_{DC}/3$	i_a	$-i_a$
on	*on*	*off*	$2V_{DC}/3$	0	i_a
on	*on*	*on*	V_{DC}	0	0

(b)

Different combinations of states of the switches define the same output voltage. This redundancy is enough to guarantee balanced voltages in the floating capacitors for any operation conditions using proper modulation. For example, for the case of the three-level converter, there are only two states that affect the voltage of the floating capacitor, and both provide the same output voltage ($V_{DC}/2$). However, the current through the capacitor flows in the opposite direction. Hence, by choosing the

suitable state according to the direction of the output current, this voltage can always be controlled.

For the three-level converter, all of the eligible states between consecutive output voltage steps are adjacent. This statement is not valid for converters with higher numbers of levels that produce significantly increased switching frequencies. Fig. 2.7 shows the transitions between two consecutive voltage levels in the four-level converter. Some of these transitions (dashed lines) force all of the switches of the leg to switch. Nevertheless, these critical transitions must be used to achieve full control of the voltages of the floating capacitors.

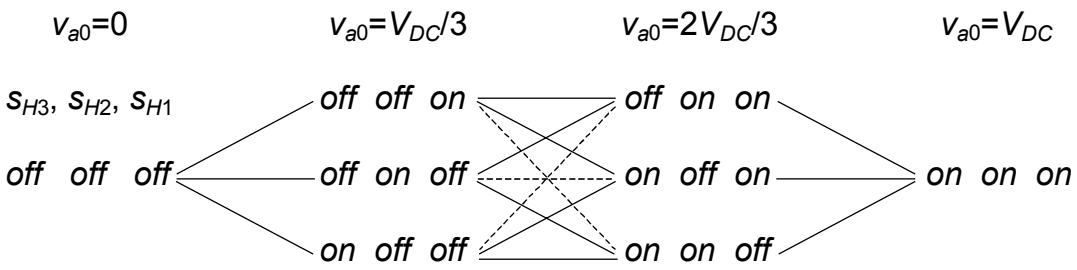


Fig. 2.7. *Transitions between consecutive voltage levels.*

Some important conclusions related to the voltage balancing issue in the floating-capacitor converters are as follows:

- Each leg can be analyzed independently from the others. This is an important difference with the diode-clamped converter, in which the entire three-phase system must be considered for the balancing issue.

- These converters can control the voltages of the floating capacitors thanks to their redundancy of states. However, in converters with more than three levels, some transitions between two consecutive voltage levels produce high switching frequencies. If these transitions are avoided, the amplitude of the voltage ripple in the capacitors will increase, and it might not be controllable.

On the other hand, regarding Fig. 2.5(b), the floating capacitor C_{f2} has double voltage applied as compared with capacitor C_{f1}. Additionally, as the current level through all the floating capacitors is the same, they should have the same capacitance to produce similar amplitudes of their voltage ripple. Therefore, assuming series and parallel connections based on the same elementary component, capacitor C_{f2} requires four times the number of components required by C_{f1}.

In conclusion, one of the major drawbacks of this topology is its high number of capacitors, not only those in the topology itself, but also those required for the series and parallel connections.

2.1.3. Cascaded H-bridge Converter

One of the earliest applications for the series connection of single-phase full-bridge inverter topology was its use for plasma stabilization in 1988 [A4]. Later, this approach was extended to include three-phase systems.

The basic three-phase structure used in the cascade converter is shown in Fig. 2.8.

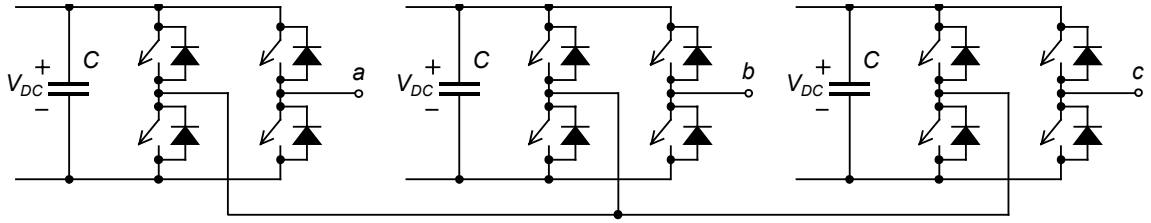


Fig. 2.8. *Three-level converter.*

A chain of H-bridge topologies can perform as a converter with higher numbers of levels (Fig. 2.9).

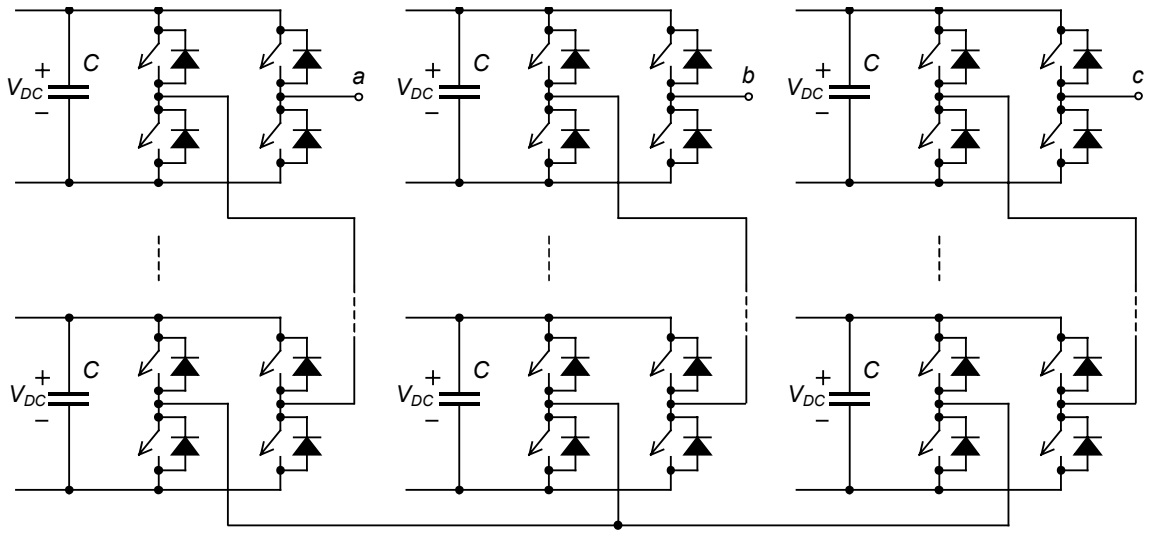


Fig. 2.9. *Multilevel cascade converter.*

To achieve an even number of levels, a half-bridge topology must be added to the chain of H-bridge converters. Fig. 2.10 shows the structure of a four-level converter.

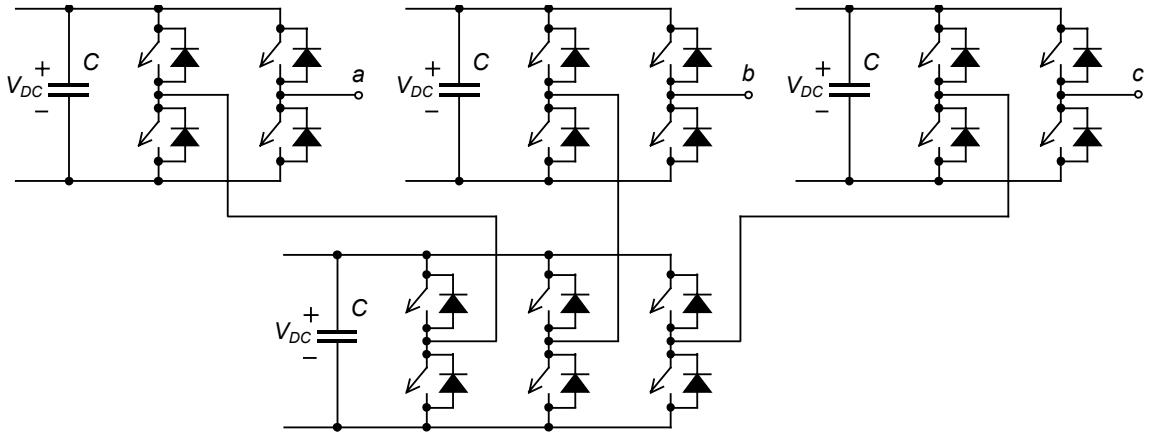


Fig. 2.10. *Four-level cascade converter.*

The modularity of this topology is an important feature. However, the fact that the DC-link voltages must be isolated is the major drawback for application of these structures. Several independent DC power supplies are required, which can be provided either by a transformer with multiple isolated secondaries or by several transformers. For electrical vehicles, batteries or fuel cells can also be used.

In order to balance the power provided by the DC voltage sources, each cell can be used in a cyclic way throughout each semi-cycle of a line period [A51]. Another benefit of this circulating method is that it achieves the same switching frequencies for all of the devices.

For a given topology, a higher number of levels can be obtained if each cascade level is fed by a different DC voltage value. Different devices would make up each cell, so that the fastest ones, which may synthesize the cell fed by the lower voltage, will define the output voltage switching frequency [A52].

2.1.4. General Data for Basic Multilevel Topologies

Table 2.2 summarizes the general characteristics of basic multilevel topologies.

Table 2.2. *Main characteristics of multilevel topologies.*

Topology		a	b	c	d	e	f	g	h	i	j
Diode-Clamped Converter	n-Level	$6(n-1)$	$6(n-2)$	$3(n-1)(n-2)$	$n-1$	$n-1$	$V_{DC}/(n-1)$	$2n-1$	$4n-3$	n^3	$n^3-(n-1)^3$
	3-Level	12	6	6	2	2	$V_{DC}/2$	5	9	27	19
	4-Level	18	12	18	3	3	$V_{DC}/3$	7	13	64	37
	5-Level	24	18	36	4	4	$V_{DC}/4$	9	17	125	61
Floating-Capacitor Converter	n-Level	$6(n-1)$	0	0	$3n-5$	$(n-1)^2+3\sum_{i=1}^{n-2} i^2$	$V_{DC}/(n-1)$	$2n-1$	$4n-3$	$2^{3(n-1)}$	$n^3-(n-1)^3$
	3-Level	12	0	0	4	7	$V_{DC}/2$	5	9	64	19
	4-Level	18	0	0	7	24	$V_{DC}/3$	7	13	512	37
	5-Level	24	0	0	10	58	$V_{DC}/4$	9	17	4096	61
Cascade Converter	n-Level	$6(n-1)$	0	0	(Even) $3n/2-1.5$ (Odd) $3n/2-2$	(Even) $3n/2-1.5$ (Odd) $3n/2-2$	$V_{DC\,equiv}/(n-1)$	$2n-1$	$4n-3$	$2^{3(n-1)}$	$n^3-(n-1)^3$
	3-Level	12	0	0	3	3	$V_{DC\,equiv}/2$	5	9	64	19
	4-Level	18	0	0	4	4	$V_{DC\,equiv}/3$	7	13	512	37
	5-Level	24	0	0	6	6	$V_{DC\,equiv}/4$	9	17	4096	61

a: switches (with free-wheeling diodes)
b: independent diodes (with different reverse voltages possible)
c: real number of independent diodes (series connection for same reverse voltage distribution)
d: capacitors (with different voltages possible)
e: real number of capacitors (series and parallel connections for the same voltage distribution and capacitance)
f: maximum voltage applied
g: line-to-line output voltage levels
h: phase voltage levels for star load connection
i: states of the converter (total vectors of the SV diagram, including multiple ones)
j: states of the converter with different line-to-line voltages (different vectors of the SV diagram)

2.2. Prototype Description

2.2.1. SMES System

The experimental results presented in this dissertation have been obtained using the DC-AC converter of an SMES system [A10]. Fig. 2.11 shows this prototype, which was built in the CPES laboratory, in Virginia Tech, VA, USA.

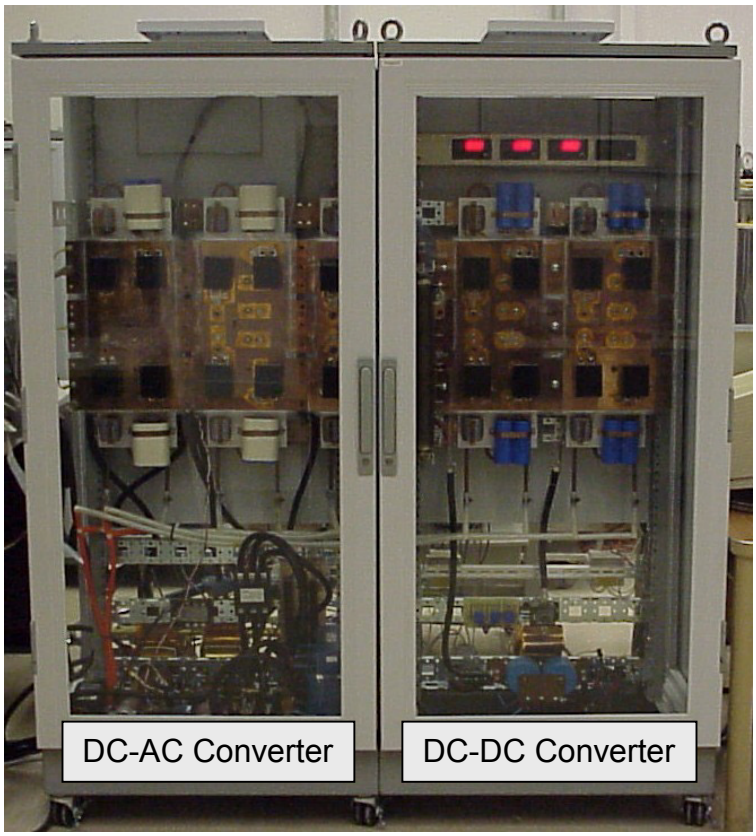


Fig. 2.11. *SMES prototype.*

SMES systems have the objective of storing energy in the magnetic field of a superconducting coil, so that this energy can be used later [B4]. High DC current continues to flow through the inductor producing minimal losses due to its extremely low resistance.

Most of the interest in this type of systems is for use in utility applications, in which it performs a buffer between power generation and load consumption. Other utility applications are active filtering and in uninterruptible power systems (UPSs).

SMES systems can perform numerous operation cycles with high control of the energy flux between the utility and the coil. Additionally, these processes can be very

fast, so that a great amount of energy flows from the coil to the grid in few seconds or a fraction of second, allowing pulse power loads to be supplied.

Since SMES systems deal with high power levels, multilevel converters are useful to act as the proper interface between the superconducting coil (DC current) and the utility (AC current). Fig. 2.12 shows the general diagram of the SMES system designed in the CPES laboratory. Both converters, the DC-DC converter and the DC-AC converter, are based on three-level topologies.

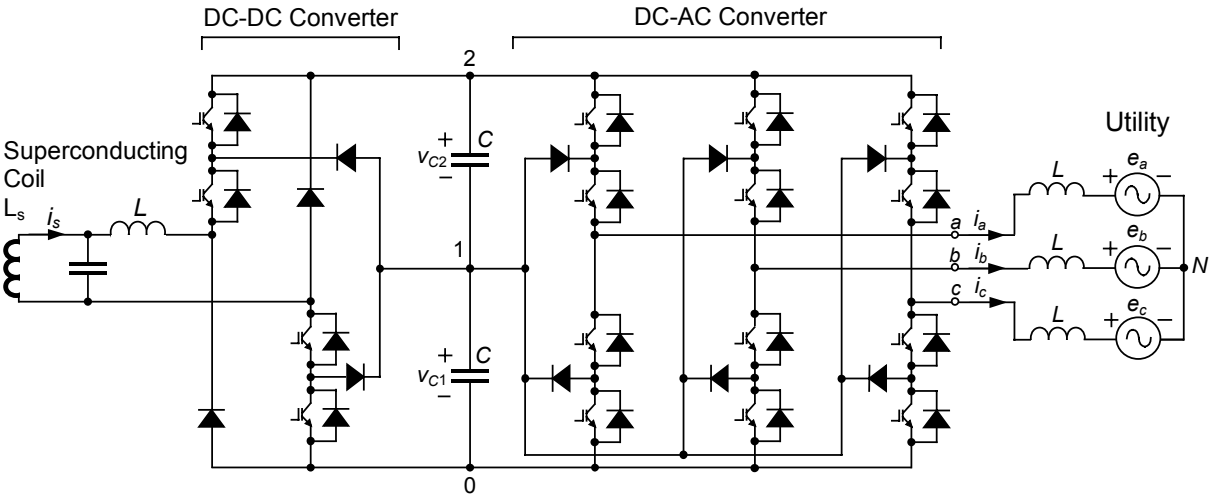


Fig. 2.12. *General diagram of the SMES system.*

All phase legs in Fig. 2.12 are built using the concept of power electronics building blocks (PEBBs) based on IGBTs. Some of the advanced features of this include the zero-current-transition (ZCT) soft-switching technique, which allows the system to be rated at 250 kVA while switching at 20 kHz. The maximum DC-link voltage is 1800 V and the maximum DC-link current is 150 A.

2.2.2. Digital Control Hardware

The complexity of control in multilevel converters, results in the almost exclusive application of digital control hardware for these systems. In addition, the versatility of modern microprocessors allows implementation of any type of control and modulation algorithms.

The main aspects of the digital control of the SMES system are presented in the following. An extended description can be found in [B1].

2.2.2.1. Description of the Controller Architecture

Fig. 2.13 shows the block diagram of the DSP-based controller of the three-level DC-AC converter. It is divided into the three following functional subsystems, implemented on separate printed circuit boards:

- DSP subsystem
- Digital interface subsystem with flex erasable and programmable logic devices (EPLDs)
- Analog interface subsystem with A/D and D/A converters

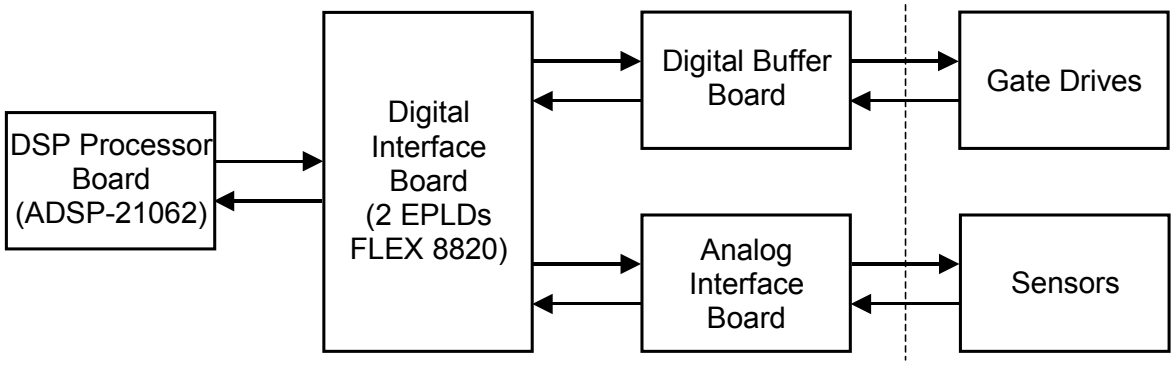


Fig. 2.13. *Architecture of the SMES digital controller.*

DSP Board

The ADSP-21062 EZ-LAB from Analog Devices used in this architecture is a complete development system based on the ADSP 21062 (SHARC) processor. This is a 32-bit floating-point processor with a throughput of 40 MFLOPS. It has a 1M bit of on-chip program memory and a 1M bit of on-chip data memory. This board allows the use of the AZ in-circuit emulator and facilitates communication with additional modules through the SHARCPAC expansion connectors, which are used to interface with the digital interface board.

Digital Interface Board

The digital interface board consists of two back-to-back connected EPLD FLEX 8820s from ALTERA. Each chip has 8,000 usable gates, 820 flip-flops and 152 pins that can be user-defined as input, output or input/output. These EPLDs share the address/data and control lines with the processor. They can be electrically

programmed to implement any logic functions by a serial cable from a personal computer or using the programmable read only memories (PROMs). This board performs the majority of the PWM generation and system protection tasks such as shutdown at repeated fault signal from gate drives, watchdog timer function and shoot-through protection.

Analog Interface Board

The processor acquires the analog feedback signals from the plant through A/D converters. Sixteen analog input channels are level-shifted, inverted and filtered, and then fed into two analog multiplexers (both 2 x 4-to-1). The outputs of the multiplexers are routed to four 10-bit 20 MSPS A/D converters (AD876), which are all connected to the digital interface board via common data lines. The main consideration in this architecture is the high sample speed, which cannot be achieved using a single converter with multiplexed input. The analog interface board also has eight analog outputs, which are mostly used for debugging and transfer function measurement. The analog output signals of the D/A converters (Quad 12-bit DAC8412 from Analog Devices) are buffered using voltage followers; two of these converters drive the current transmitters that can be used to feed long cables.

2.2.2.2. Functions of the EPLD

The main function of the EPLD is to generate the PWM signals that are fed into the converter gate drives, based on the data received from the DSP. A functional diagram of the EPLD logic responsible for generating the PWM signals is shown in Fig. 2.14.

The DSP receives periodic interrupt requests (IRQs) from the EPLD at modulation period (T_m), which is the same as the control-sampling period. After receiving an IRQ, the processor reads the feedback variables from the A/D converters and calculates the switching states and their duty cycles. They are loaded into the double-buffered register bank in the EPLD to be used in the subsequent modulation cycle. The processor then enters the idle state until receiving a new IRQ.

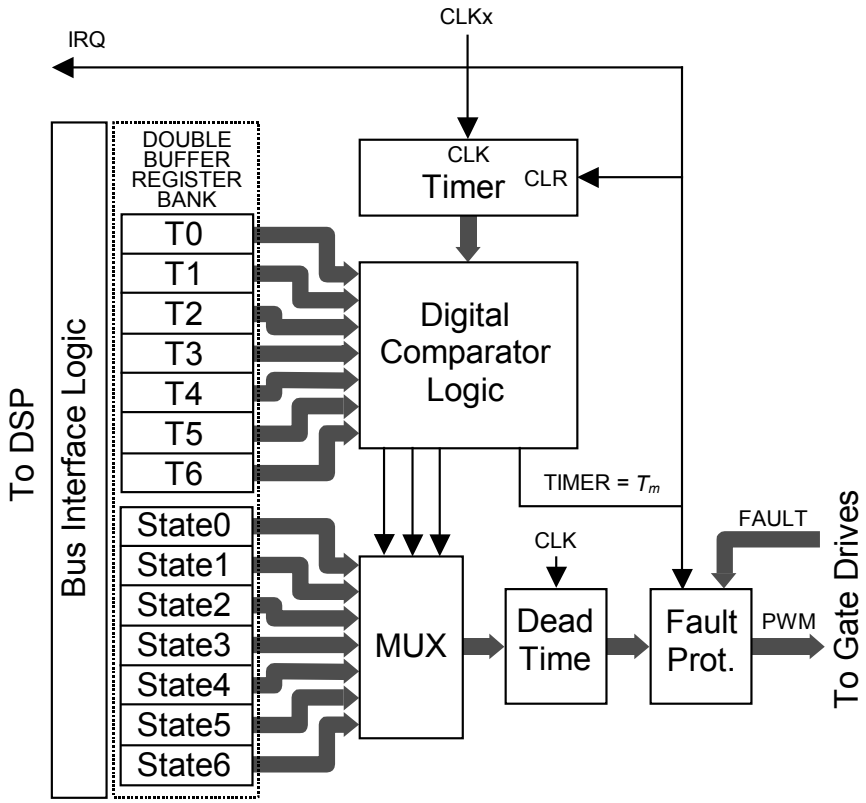


Fig. 2.14. *PWM signal-generation logic within the EPLD.*

The double-buffered register bank consists of timer registers and state registers, the amount of which varies for different applications. Each register is double-buffered, so that the PWM data used in the current modulation period is not affected when the asynchronous DSP writes into the first buffer. The fresh data is loaded into the second buffer by an IRQ signal at the beginning of each modulation period.

The state registers contain those switching-state codes which are used for PWM in the current modulation cycle, ordered in the sequence in which they will be applied. The time registers contain the duty-cycle information, i.e., the times from the beginning of the modulation cycle (measured in the units of EPLD CLK period) to the time when the corresponding switching state ends.

Generation of PWM Signals

The timer in Fig. 2.14 is a free-running counter with the same length as the time registers in the register bank. It can be fed by any of the three clock signals available on the digital interface board. The counter is cleared by the IRQ signal at the beginning of each modulation cycle. The digital comparator logic and MUX in Fig. 2.14 sequentially outputs the switching states using the current data in the double-

buffered register bank. After the timer reaches T_m, the digital comparator logic generates the IRQ signal, which starts a new modulation cycle by interrupting the processor, loading the new data into the double-buffered register bank, and cleaning the timer counter.

Dead-time protection is provided to avoid any shoot-through of the inverter legs. This is done by delaying the rising edges of all the signals by a particular number of clock cycles.

Fault Protection

In the event of a fault, the PWM signals are shut down to save the power stage. Two kinds of fault protection have been provided: internal and external. If for some reason the PWM signals received from the dead-time block are such that they turn on the top and bottom switches of a given phase leg, then a fault signal is generated inside the EPLD (internal fault) and the PWM pulses are shut down. The internal fault can also be generated by the watchdog timer. These conditions should not occur under normal operating conditions. They are a protection against software failure.

External fault protection is activated when a gate driver senses an over-current through the power device and sends a fault signal to the digital buffer board. This fault signal is passed to the EPLD where it enables an IRQ counter. If the fault persists for a particular number of modulation cycles (this number can be programmed into the IRQ counter), the PWM signals are shut down. In this way, the entire converter is not shut down if the over-current condition happens in only a couple of modulation cycles, which is acceptable because the gate drives automatically turn off the switch whenever over-current is detected.

Other EPLD Functions

The analog interface board has four A/D converters and two D/A converters that all communicate through the same 12-bit data bus. In addition, the processor and A/D converters have different frequency clocks that are not synchronized. Therefore, to insure proper operation of the board, the timing control signals are crucial. The logic that receives signals from the analog interface board and takes care of synchronization is implemented inside the EPLD. In addition, the system watchdog timer and the address decoding of the input and output port are also implemented in the EPLD.

2.3. Models of the Diode-Clamped Converter

Some models of the diode-clamped converter are presented in this section. General models are given for multilevel topologies (n-level), and they are also particularized for the three-level case.

Different kinds of models are required:

- “Large-signal” models. These mathematical models are used to obtain simulated results for the converter. They are formulated in terms of control functions of the switches. Nevertheless, if the switching functions are substituted by their duty cycles, the waveforms obtained are free of certain components related to switching frequency. These models may be interesting in terms of ability to analyze transitory averaged evolutions of voltages and currents, as well as to perform low-frequency analysis.

- “Small-signal” model. This model is required to design and study control loop strategies. As the control stage must achieve the operation point of the system while disregarding high-frequency components of the variables (switching frequency), this model is formulated in terms of local averaged variables. State-space formulation is used for the model.

2.3.1. Multilevel Models

Fig. 2.15 shows the diagram of the multilevel system to be modeled. Conventional signs of voltages and currents are also indicated.

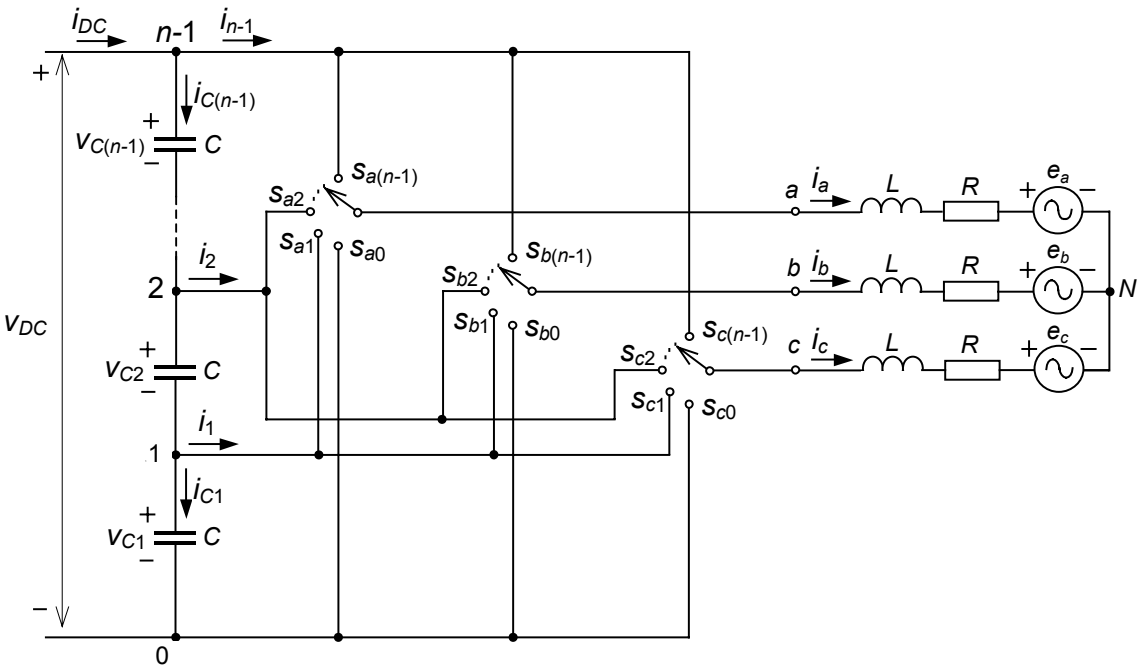


Fig. 2.15. *General multilevel system to be modeled.*

2.3.1.1. Phase Model

The output voltages in Fig. 2.15 referring to the lower DC-link potential ("0") can be expressed as:

$$v_{a0} = L\frac{di_a}{dt} + R\,i_a + e_a + v_{N0}\,, \tag{2.4a}$$

$$v_{b0} = L\frac{di_b}{dt} + R\,i_b + e_b + v_{N0} \quad \text{and} \tag{2.4b}$$

$$v_{c0} = L\frac{di_c}{dt} + R\,i_c + e_c + v_{N0}\,. \tag{2.4c}$$

The AC NP potential ("*N*") can be found by summing all the terms in (2.4), and in regards to the fact that $i_a + i_b + i_c = 0$, then:

$$v_{N0} = \frac{v_{a0} + v_{b0} + v_{c0} - (e_a + e_b + e_c)}{3}\,. \tag{2.5}$$

A first-order matrix equation describes the AC side of the system, such that

$$\frac{d}{dt}\mathbf{i}_{ph} = -\frac{R}{L}\mathbf{i}_{ph} - \frac{1}{L}\,\mathbf{e}_{ph} + \frac{1}{L}\mathbf{v}_{ph0} - \frac{1}{L}\mathbf{U}_3 v_{N0}\,, \tag{2.6}$$

where the subscript *ph* indicates the following phase components:

$$\mathbf{i}_{ph} = \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}, \quad \mathbf{e}_{ph} = \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix}, \quad \text{and} \quad \mathbf{v}_{ph0} = \begin{bmatrix} v_{a0} \\ v_{b0} \\ v_{c0} \end{bmatrix}.$$

The term $\mathbf{U}_3$ in (2.6) is a conventional notation[①] that stands for $\begin{bmatrix}1 & 1 & 1\end{bmatrix}^{\mathrm{T}}$.

On the other hand, the following equation indicates the currents through the capacitors in the DC side of the converter:

$$i_{Cj} = C\frac{dv_{Cj}}{dt} = i_{DC} - \sum_{k=j}^{n-1} i_k \,, \quad \text{where } j = \{1, 2, \ldots, n\text{-}1\}, \tag{2.7}$$

or

$$\frac{d}{dt}\mathbf{v}_C = \frac{1}{C}\mathbf{U}_{n-1}\, i_{DC} - \frac{1}{C}\mathbf{K}_{NC}\,\mathbf{i}_{NC}\,, \tag{2.8}$$

where

$$\mathbf{v}_C = \begin{bmatrix} v_{C(n-1)} \\ v_{C(n-2)} \\ \vdots \\ v_{C2} \\ v_{C1} \end{bmatrix}, \quad \mathbf{i}_{NC} = \begin{bmatrix} i_{n-1} \\ i_{n-2} \\ \vdots \\ i_2 \\ i_1 \end{bmatrix} \quad \text{and} \quad \mathbf{K}_{NC} = \begin{bmatrix} 1 & 0 & \cdots & 0 & 0 \\ 1 & 1 & \cdots & 0 & 0 \\ \vdots & \vdots & \cdots & \vdots & \vdots \\ 1 & 1 & \cdots & 1 & 0 \\ 1 & 1 & \cdots & 1 & 1 \end{bmatrix}.$$

Equations (2.6) and (2.8) describe the entire system except for the switching stage. The control functions of each single-pole n-throw switch can interrelate voltages and currents between the AC side and the DC side of the converter, such that

$$\mathbf{v}_{ph0} = \mathbf{s}_{ph}\,\mathbf{v}_C; \quad \mathbf{K}_{NC}\,\mathbf{i}_{NC} = \mathbf{s}_{ph}^{\mathrm{T}}\,\mathbf{i}_{ph}\,, \tag{2.9}$$

where the switching matrix is:

$$\mathbf{s}_{ph} = \begin{bmatrix} s_{a(n-1)} & s_{a(n-1)} + s_{a(n-2)} & \cdots & \sum_{i=2}^{n-1} s_{ai} & \sum_{i=1}^{n-1} s_{ai} \\ s_{b(n-1)} & s_{b(n-1)} + s_{b(n-2)} & \cdots & \sum_{i=2}^{n-1} s_{bi} & \sum_{i=1}^{n-1} s_{bi} \\ s_{c(n-1)} & s_{c(n-1)} + s_{c(n-2)} & \cdots & \sum_{i=2}^{n-1} s_{ci} & \sum_{i=1}^{n-1} s_{ci} \end{bmatrix}.$$

[①] The notation $\mathbf{U}_x$ will henceforth characterize [1 1 1 ... 1]$^{\mathrm{T}}$, in which the subscript x is the number of rows of this column vector.

By substituting (2.9) into (2.6) and (2.8), a set of dynamic equations describing the switched model of the multilevel system is developed. This model is general, complete and makes no assumptions other than the use of ideal switches:

$$\frac{d}{dt}\mathbf{i}_{ph} = -\frac{R}{L}\mathbf{i}_{ph} - \frac{1}{L}\mathbf{e}_{ph} + \frac{1}{L}\mathbf{s}_{ph}\,\mathbf{v}_C - \frac{1}{L}v_{N0} \quad \text{and} \tag{2.10a}$$

$$\frac{d}{dt}\mathbf{v}_C = \frac{1}{C}\mathbf{U}_{n-1}\,i_{DC} - \frac{1}{C}\mathbf{s}_{ph}^{\mathsf{T}}\,\mathbf{i}_{ph}\,. \tag{2.10b}$$

Although this mathematical model can be used for simulations, the term v_{N0} must be calculated during the simulation, which involves solving for voltages v_{a0}, v_{b0} and v_{c0}. However, if the system equation is translated into dq rotating-coordinate frames, this term no longer affects any current because it is only involved in the homopolar current equation, which is always zero. As the voltage-balancing process of the capacitors will be performed by the modulation itself, the voltage v_{N0} does not provide any useful information for control. This term can also be avoided if the converter is modeled from the standpoint of line-to-line components.

2.3.1.2. Line-to-Line Model

To deal with line-to-line components, the terms of the consecutive equations in (2.4) are subtracted from each other, so that:

$$v_{ab} = L\frac{di_{ab}}{dt} + R\,i_{ab} + e_{ab}\,, \tag{2.11a}$$

$$v_{bc} = L\frac{di_{bc}}{dt} + R\,i_{bc} + e_{bc} \quad \text{and} \tag{2.11b}$$

$$v_{ca} = L\frac{di_{ca}}{dt} + R\,i_{ca} + e_{ca}\,, \tag{2.11c}$$

where $v_{ab} = v_{a0} - v_{b0}$, $i_{ab} = i_a - i_b$, $e_{ab} = e_a - e_b$, etc.

Note that the AC NP voltage term has disappeared from these expressions.

By proceeding in a way similar to that for the phase model, the final equations of the line-to-line model are:

$$\frac{d}{dt}\mathbf{i}_{LL} = -\frac{R}{L}\mathbf{i}_{LL} - \frac{1}{L}\mathbf{e}_{LL} + \frac{1}{L}\mathbf{s}_{LL}\,\mathbf{v}_C \quad \text{and} \tag{2.12a}$$

$$\frac{d}{dt}\mathbf{v}_C = \frac{1}{C}\mathbf{U}_{n-1}\, i_{DC} - \frac{1}{3C}\mathbf{s}_{LL}^{\mathrm{T}}\,\mathbf{i}_{LL}\,, \tag{2.12b}$$

where

$$\mathbf{i}_{LL} = \begin{bmatrix} i_{ab} \\ i_{bc} \\ i_{ca} \end{bmatrix} \quad \text{and} \quad \mathbf{e}_{LL} = \begin{bmatrix} e_{ab} \\ e_{bc} \\ c_{ca} \end{bmatrix},$$

and where the switching matrix is:

$$\mathbf{s}_{LL} = \begin{bmatrix} s_{ab(n-1)} & s_{ab(n-1)} + s_{ab(n-2)} & \cdots & \sum_{i=2}^{n-1} s_{abi} & \sum_{i=1}^{n-1} s_{abi} \\ s_{bc(n-1)} & s_{bc(n-1)} + s_{bc(n-2)} & \cdots & \sum_{i=2}^{n-1} s_{bci} & \sum_{i=1}^{n-1} s_{bci} \\ s_{ca(n-1)} & s_{ca(n-1)} + s_{ca(n-2)} & \cdots & \sum_{i=2}^{n-1} s_{cai} & \sum_{i=1}^{n-1} s_{cai} \end{bmatrix},$$

with $s_{ijk} = s_{ik} - s_{jk}$; $i, j = \{a, b, c\}$; and $k = \{1, 2, \ldots, n\text{-}1\}$.

The number three in (2.12(b)) appears because

$$i_p = \frac{1}{3}\left(s_{abp} i_{ab} + s_{bcp} i_{bc} + s_{cap} i_{ca}\right), \quad \text{with} \quad p = \{1, 2, ..., n-1\}, \tag{2.13}$$

which can be demonstrated from

$$i_p = s_{ap} i_a + s_{bp} i_b + s_{cp} i_c \quad \text{and} \quad i_a + i_b + i_c = 0\,. \tag{2.14}$$

2.3.2. Three-Level Models

Fig. 2.16 shows the diagram of the three-level system that has been modeled. Conventional signs of voltages and currents are also indicated.

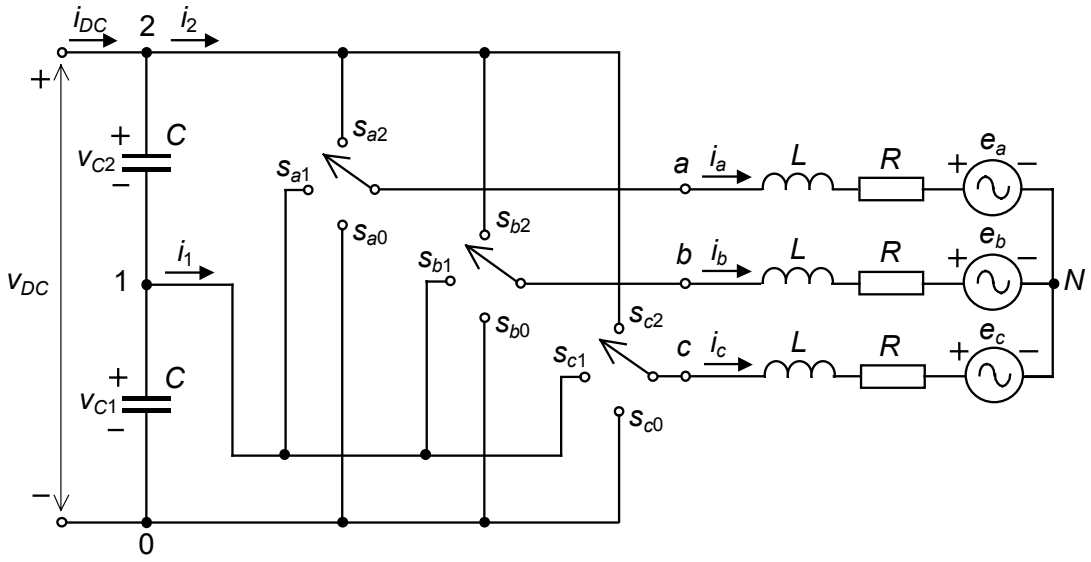


Fig. 2.16. *Conventional signs of the variables of the three-level converter.*

2.3.2.1. Phase Model

The general equations (2.10(a) and (b)) of the phase model are now applied to *n*=3 (three-level converter), such that

$$\frac{d}{dt}\mathbf{i}_{ph} = -\frac{R}{L}\mathbf{i}_{ph} - \frac{1}{L}\mathbf{e}_{ph} + \frac{1}{L}\mathbf{s}_{ph3L}\,\mathbf{v}_{C3L} - \frac{1}{L}\mathbf{U}_3 v_{N0} \quad \text{and} \tag{2.15a}$$

$$\frac{d}{dt}\mathbf{v}_{C3L} = \frac{1}{C}\mathbf{U}_2\, i_{DC} - \frac{1}{C}\mathbf{s}_{ph3L}^{\mathsf{T}}\,\mathbf{i}_{ph}\,, \tag{2.15b}$$

where, for this particular case:

$$\mathbf{v}_{C3L} = \begin{bmatrix} v_{C2} \\ v_{C1} \end{bmatrix} \quad \text{and} \quad \mathbf{s}_{ph3L} = \begin{bmatrix} s_{a2} & s_{a2}+s_{a1} \\ s_{b2} & s_{b2}+s_{b1} \\ s_{c2} & s_{c2}+s_{c1} \end{bmatrix}.$$

Since each single-pole three-throw switch only can take one position at any time, the switching matrix can be expressed as:

$$\mathbf{s}_{ph3L} = \begin{bmatrix} s_{a2} & 1-s_{a0} \\ s_{b2} & 1-s_{b0} \\ s_{c2} & 1-s_{c0} \end{bmatrix}. \tag{2.16}$$

By substituting this switching matrix into (2.15):

$$\mathbf{s}_{ph3L}\,\mathbf{v}_{C3L} = \begin{bmatrix} s_{a2} & -s_{a0} \\ s_{b2} & -s_{b0} \\ s_{c2} & -s_{c0} \end{bmatrix} \begin{bmatrix} v_{C2} \\ v_{C1} \end{bmatrix} + \mathbf{U}_2 v_{C1}; \quad \mathbf{s}_{ph3L}^{\mathrm{T}}\,\mathbf{i}_{ph} = \begin{bmatrix} s_{a2} & s_{b2} & s_{c2} \\ -s_{a0} & -s_{b0} & -s_{c0} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}. \quad (2.17)$$

Therefore, the equations of the three-level converter are:

$$\frac{d}{dt}\mathbf{i}_{ph} = -\frac{R}{L}\mathbf{i}_{ph} - \frac{1}{L}\mathbf{e}_{ph} + \frac{1}{L}\mathbf{s}_{ph3}\,\mathbf{v}_{C3L} - \frac{1}{L}\mathbf{U}_3\left(v_{N0} - v_{C1}\right) \quad \text{and} \quad (2.18a)$$

$$\frac{d}{dt}\mathbf{v}_{C3L} = \frac{1}{C}\mathbf{U}_2 i_{DC} - \frac{1}{C}\mathbf{s}_{ph3}^{\mathrm{T}}\,\mathbf{i}_{ph}, \quad (2.18b)$$

where the new switching matrix is:

$$\mathbf{s}_{ph3L} = \begin{bmatrix} s_{a2} & -s_{a0} \\ s_{b2} & -s_{b0} \\ s_{c2} & -s_{c0} \end{bmatrix}.$$

Referring the AC NP potential ("*N*") with the NP of the DC-link ("1"), (2.18(a)) becomes:

$$\frac{d}{dt}\mathbf{i}_{ph} = -\frac{R}{L}\mathbf{i}_{ph} - \frac{1}{L}\mathbf{e}_{ph} + \frac{1}{L}\mathbf{s}_{ph3L}\,\mathbf{v}_{C3L} - \frac{1}{L}\mathbf{U}_3 v_{N1}. \quad (2.19)$$

2.3.2.2. Line-to-Line Model

The general equations of the line-to-line model are applied now to the three-level converter:

$$\frac{d}{dt}\mathbf{i}_{LL} = -\frac{R}{L}\mathbf{i}_{LL} - \frac{1}{L}\mathbf{e}_{LL} + \frac{1}{L}\mathbf{s}_{LL3L}\,\mathbf{v}_{C3L} \quad \text{and} \quad (2.20a)$$

$$\frac{d}{dt}\mathbf{v}_{C3L} = \frac{1}{C}\mathbf{U}_2 i_{DC} - \frac{1}{3C}\mathbf{s}_{LL3}^{\mathrm{T}}\,\mathbf{i}_{LL}, \quad (2.20b)$$

where, for this particular case:

$$\mathbf{v}_{C3L} = \begin{bmatrix} v_{C2} \\ v_{C1} \end{bmatrix} \quad \text{and} \quad \mathbf{s}_{LL3L} = \begin{bmatrix} s_{ab2} & s_{ab2} + s_{ab1} \\ s_{bc2} & s_{bc2} + s_{bc1} \\ s_{ca2} & s_{ca2} + s_{ca1} \end{bmatrix}.$$

If the switching matrix is preferred to contain switching functions of the higher and lower connection poles ("2" and "0" subscripts), it can be expressed as:

$$\mathbf{s}_{LL3L} = \begin{bmatrix} s_{ab2} & -s_{ab0} \\ s_{bc2} & -s_{bc0} \\ s_{ca2} & -s_{ca0} \end{bmatrix}. \quad (2.21)$$

2.3.3. Model for the Control

The small-signal model of the three-level converter is developed in this section so that proper control loops can be designed. This model is based on the phase model, but it could be based on the line-to-line model without significant differences.

2.3.3.1. State-Space Model

From (2.6):

$$\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & 0 & 0 \\ 0 & -\frac{R}{L} & 0 \\ 0 & 0 & -\frac{R}{L} \end{bmatrix}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} -\frac{1}{L} & 0 & 0 \\ 0 & -\frac{1}{L} & 0 \\ 0 & 0 & -\frac{1}{L} \end{bmatrix}\begin{bmatrix} e_a - v_{a0} \\ e_b - v_{b0} \\ e_c - v_{c0} \end{bmatrix} + \begin{bmatrix} -\frac{1}{L} \\ -\frac{1}{L} \\ -\frac{1}{L} \end{bmatrix} v_{N0}. \quad (2.22)$$

Transforming (2.22) into rotating frames according to the dq transformation (Appendix A):

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ i_o \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & \omega & 0 \\ -\omega & -\frac{R}{L} & 0 \\ 0 & 0 & -\frac{R}{L} \end{bmatrix}\begin{bmatrix} i_d \\ i_q \\ i_o \end{bmatrix} + \begin{bmatrix} -\frac{1}{L} & 0 & 0 \\ 0 & -\frac{1}{L} & 0 \\ 0 & 0 & -\frac{1}{L} \end{bmatrix}\begin{bmatrix} e_d - v_d \\ e_q - v_q \\ e_o - v_o \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ -\frac{\sqrt{3}}{L} \end{bmatrix} v_{N0}, \quad (2.23)$$

where ω is the line angular frequency, and the transformed variables are:

$$\begin{bmatrix} i_d \\ i_q \\ i_o \end{bmatrix} = \mathbf{T}_{dq}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}, \quad \begin{bmatrix} e_d \\ e_q \\ e_o \end{bmatrix} = \mathbf{T}_{dq}\begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} \text{ and } \begin{bmatrix} v_d \\ v_q \\ v_o \end{bmatrix} = \mathbf{T}_{dq}\begin{bmatrix} v_{a0} \\ v_{b0} \\ v_{c0} \end{bmatrix}. \quad (2.24)$$

As the sum of the three line currents is zero, there is no homopolar component (i_o=0). Therefore, the AC NP voltage (v_{N0}) does not affect any transformed current. This voltage can be deduced from (2.23) as:

$$v_{N0} = \frac{e_o - v_o}{\sqrt{3}}. \tag{2.25}$$

The AC NP voltage only depends on homopolar voltage components. Additionally, when the electrical grid is balanced, the averaged value of e_o is zero; hence, v_{N0} depends only on the homopolar component of the AC voltages of the converter.

Defining the original position of the dq axis to be e_q=0, the other component is e_d=E_L, which is the value of the line-to-line RMS voltage. Therefore, (2.23) can be expressed as:

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & \omega \\ -\omega & -\frac{R}{L} \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix}\begin{bmatrix} v_d \\ v_q \end{bmatrix} + \begin{bmatrix} -\frac{1}{L} \\ 0 \end{bmatrix} E_L, \tag{2.26}$$

where the homopolar component has been omitted.

On the other hand, from (2.8), the DC side of the system can be expressed as:

$$\frac{d}{dt}\begin{bmatrix} v_{C2} \\ v_{C1} \end{bmatrix} = \frac{1}{C} i_{DC} - \frac{1}{C}\begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix}\begin{bmatrix} i_2 \\ i_1 \end{bmatrix}. \tag{2.27}$$

In order to avoid switching functions, the equation of the DC side (2.27) can be related to the AC side (2.26) by the power-balance relationship. Taking into account that the dq transformation is power conservative (Appendix A):

$$p = v_a\, i_a + v_b\, i_b + v_c\, i_c = v_d\, i_d + v_q\, i_q, \tag{2.28}$$

and assuming efficiency of 100%, the instantaneous power at the DC side is:

$$p = (v_{C1} + v_{C2})\, i_2 + v_{C1}\, i_1. \tag{2.29}$$

Making both power values equal, current i_2 is:

$$i_2 = \frac{v_d i_d + v_q i_q - v_{C1} i_1}{v_{C1} + v_{C2}}, \tag{2.30}$$

and substituting this current into (2.27):

$$\frac{dv_{C2}}{dt} = \frac{i_{DC}}{C} - \frac{v_d\, i_d + v_q\, i_q - v_{C1}\, i_1}{C(v_{C1} + v_{C2})} \quad \text{and} \tag{2.31a}$$

$$\frac{dv_{C1}}{dt} = \frac{i_{DC}}{C} - \frac{v_d\, i_d + v_q\, i_q + v_{C2}\, i_1}{C(v_{C1} + v_{C2})}. \tag{2.31b}$$

The large-signal model of the system is defined by (2.26) and (2.31).

Since the modulation algorithm will balance the NP voltage, the control stage must only regulate the total DC-link voltage and the AC currents. Therefore, the model can be simplified assuming balanced voltages in the capacitors (v_{C1}=v_{C2}=v_{DC}/2)[②]. Summing term by term in (2.31):

$$\frac{dv_{DC}}{dt} = 2\frac{i_{DC}}{C} - 2\frac{v_d\, i_d + v_q\, i_q}{C v_{DC}}. \tag{2.32}$$

This equation is nonlinear; therefore, it should be linearized to obtain a useful model for the control. Averaged variables are assumed, according to the local averaging operator:

$$\overline{x}_{(t)} = \frac{1}{T_m}\int_{t-T_m}^{t} x_{(\tau)}\, d\tau. \tag{2.33}$$

As a result of applying this linear operator to the model of the system, all components of the variables related to switching frequency disappear. The variables of the model are assumed henceforth to be averaged variables. For the purpose of simplicity, no difference in notation has been included.

The variables assumed to be controlled are the reactive current component and the DC-link voltage:

$$i_q = I_q^* \quad \text{and} \quad v_{DC} = V_{DC}^*, \tag{2.34}$$

where I_q^* and V_{DC}^* denote the reference values.

The transformed AC voltages of the converter (v_d, v_q) are the control variables. Thus, the system is simplified to a two-input-two-output three-order system.

In steady-state conditions, the subscript "*ss*" is added to the variables to identify the operating point:

$$e_{dss} = E_L, \quad e_{qss} = 0, \quad i_{qss} = I_q^* \quad \text{and} \quad v_{DCss} = V_{DC}^*. \tag{2.35}$$

[②] The total DC-link voltage is usually indicated in upper case (V_{DC}) because it is assumed constant or referred to its rated value. However, in modeling and controlling sections, it is indicated in lower case (v_{DC}) due to its variable condition.

The remaining steady-state variables are found by imposing zero into the dynamic of the system; in other words, they are obtained by making the derivatives of the variables equal zero, as follows:

$$\frac{di_{dss}}{dt} = -\frac{R}{L} i_{dss} + \omega I_q^* + \frac{1}{L} v_{dss} - \frac{1}{L} E_L = 0, \tag{2.36a}$$

$$\frac{di_{qss}}{dt} = -\omega i_{dss} - \frac{R}{L} I_q^* + \frac{1}{L} v_{qss} = 0 \quad \text{and} \tag{2.36b}$$

$$\frac{dv_{DCss}}{dt} = 2\frac{i_{DCss}}{C} - 2\frac{v_{dss} i_{dss} + v_{qss} I_q^*}{C V_{DC}^*} = 0. \tag{2.36c}$$

Solving for the steady-state values:

$$i_{dss} = \sqrt{\left(\frac{E_L}{2R}\right)^2 + \frac{V_{DC}^*}{R} i_{DCss} - I_q^{*2}} - \frac{E_L}{2R}, \tag{2.37a}$$

$$v_{dss} = E_L + R\, i_{dss} - \omega L I_q^* \quad \text{and} \tag{2.37b}$$

$$v_{qss} = \omega\, L\, i_{dss} + R I_q^*. \tag{2.37c}$$

The model is linearized by applying Taylor's Series around the operating point and by disregarding high-order terms. This is acceptable if variations around the operating point are assumed to be small; therefore, the state-space equation of the small-signal model is obtained.

In a general sense, any function $y = f(x_1, x_2, ..., x_n)$, which has the value $y_{ss} = f(x_{1ss}, x_{2ss}, ..., x_{nss})$ at the operating point, can be developed using Taylor's Series around this point and by approximating to the first-order terms:

$$y \approx y_{ss} + \left.\frac{\partial f}{\partial x_1}\right|_{ss} (x_1 - x_{1ss}) + \left.\frac{\partial f}{\partial x_2}\right|_{ss} (x_2 - x_{2ss}) + ... + \left.\frac{\partial f}{\partial x_n}\right|_{ss} (x_n - x_{nss}) \quad \text{and} \tag{2.38a}$$

$$y - y_{ss} \approx \left.\frac{\partial f}{\partial x_1}\right|_{ss} (x_1 - x_{1ss}) + \left.\frac{\partial f}{\partial x_2}\right|_{ss} (x_2 - x_{2ss}) + ... + \left.\frac{\partial f}{\partial x_n}\right|_{ss} (x_n - x_{nss}). \tag{2.38b}$$

or

$$\tilde{y} \approx \left.\frac{\partial f}{\partial x_1}\right|_{ss} \tilde{x}_1 + \left.\frac{\partial f}{\partial x_2}\right|_{ss} \tilde{x}_2 + ... + \left.\frac{\partial f}{\partial x_n}\right|_{ss} \tilde{x}_n. \tag{2.39}$$

The variations around the operating point are indicated as: $\tilde{y} = y - y_{ss}$, $\tilde{x}_1 = x_1 - x_{1ss}$, $\tilde{x}_2 = x_2 - x_{2ss}$ and $\tilde{x}_n = x_n - x_{nss}$.

Finally, applying this linearizing method to (2.26) and (2.32):

$$\frac{d}{dt}\begin{bmatrix}\tilde{i}_d\\ \tilde{i}_q\\ \tilde{v}_{DC}\end{bmatrix}=\begin{bmatrix}-\frac{R}{L} & \omega & 0\\ -\omega & -\frac{R}{L} & 0\\ -\frac{2v_{dss}}{CV_{DC}^*} & -\frac{2v_{qss}}{CV_{DC}^*} & \frac{2(v_{dss}i_{dss}+v_{qss}I_q^*)}{CV_{DC}^{*\,2}}\end{bmatrix}\begin{bmatrix}\tilde{i}_d\\ \tilde{i}_q\\ \tilde{v}_{DC}\end{bmatrix}+\begin{bmatrix}\frac{1}{L} & 0\\ 0 & \frac{1}{L}\\ -\frac{2i_{dss}}{CV_{DC}^*} & -\frac{2I_q^*}{CV_{DC}^*}\end{bmatrix}\begin{bmatrix}\tilde{v}_d\\ \tilde{v}_q\end{bmatrix}+\begin{bmatrix}-\frac{1}{L} & 0\\ 0 & 0\\ 0 & \frac{2}{C}\end{bmatrix}\begin{bmatrix}\tilde{E}_L\\ \tilde{i}_{DC}\end{bmatrix}. \tag{2.40}$$

The control strategy proposed in Chapter 7 is based on this mathematical model[③].

2.3.3.2. Equivalent Circuit

The equations of the state-space representation (2.40) can be given as:

$$\tilde{v}_d - \tilde{E}_L = L\frac{d\tilde{i}_d}{dt} + R\tilde{i}_d - \omega L\tilde{i}_q, \tag{2.41a}$$

$$\tilde{v}_q = L\frac{d\tilde{i}_q}{dt} + R\tilde{i}_q + \omega L\tilde{i}_d \quad \text{and} \tag{2.41b}$$

$$\tilde{i}_{DC} = \frac{C}{2}\frac{d\tilde{v}_{DC}}{dt} + \frac{v_{dss}}{V_{DC}^*}\tilde{i}_d + \frac{v_{qss}}{V_{DC}^*}\tilde{i}_q + \frac{i_{dss}}{V_{DC}^*}\tilde{v}_d + \frac{I_q^*}{V_{DC}^*}\tilde{v}_q - \frac{v_{dss}i_{dss}+v_{qss}I_q^*}{V_{DC}^{*\,2}}\tilde{v}_{DC}. \tag{2.41c}$$

From these equations, the following equivalent circuit is obtained:

[③] This state-space model assumes that the control variables of the converter are v_d and v_q instead of the duty cycles of switches. The controller based on this model will provide these control references to the modulator, which is responsible for generating the voltages in the converter. Although this method avoids using duty cycles in the model, accurate measure of the DC-link voltage will be required not only for the controller, but also for the modulator.

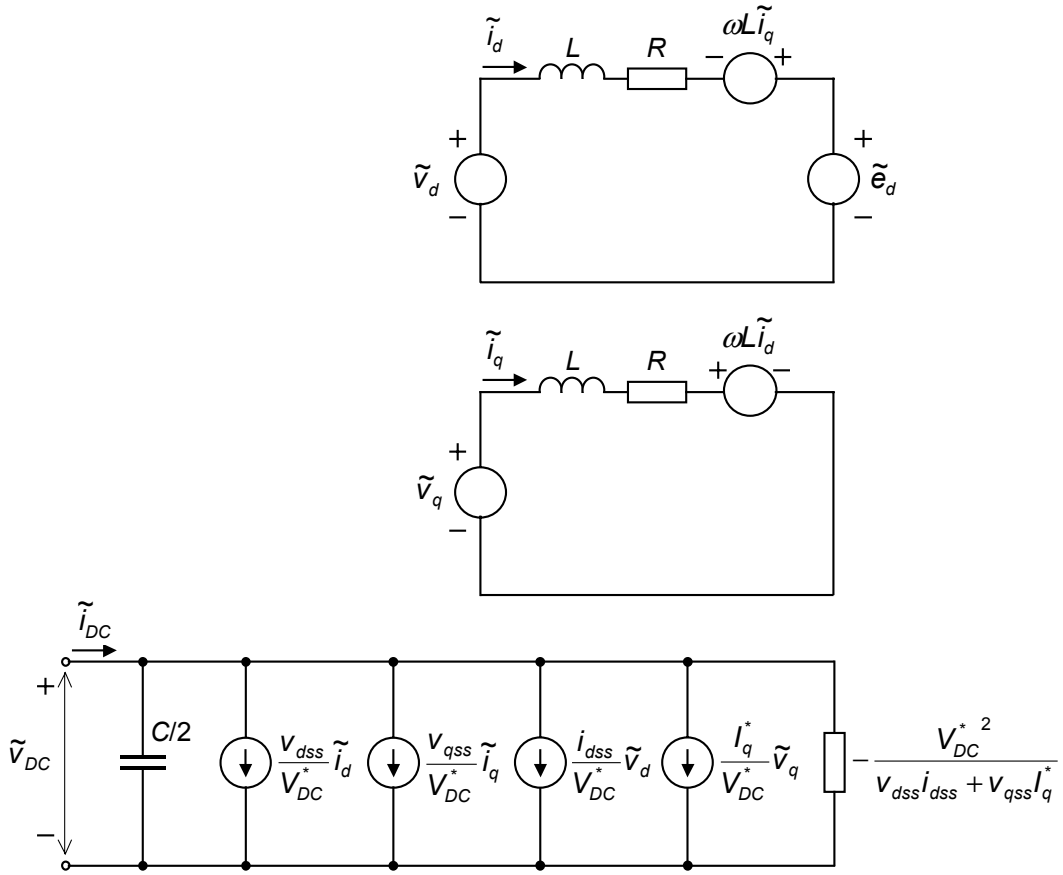


Fig. 2.17. *Equivalent small-signal circuit.*

For the case of unity PF, the reference value of the reactive current component is zero ($I_q^* = 0$). Therefore, the equivalent circuit in Fig. 2.17 is simplified, as are its corresponding expressions.

If a PF other than zero is required, the reference value of the reactive current will be given as:

$$I_q^* = \pm i_{dss}\sqrt{\frac{1}{PF} - 1}\ , \tag{2.42}$$

in which the PF is cos φ when dealing with sinusoidal waveforms, and φ is the current phase angle in relation to the voltage phase angle. The sign in (2.42) will be positive for inductive PFs and negative for capacitive PFs.