# *Síntesis de Estructuras Multiplicadoras de Tensión Basadas en Células Convertidoras Continua-Continua de Tipo Conmutado*

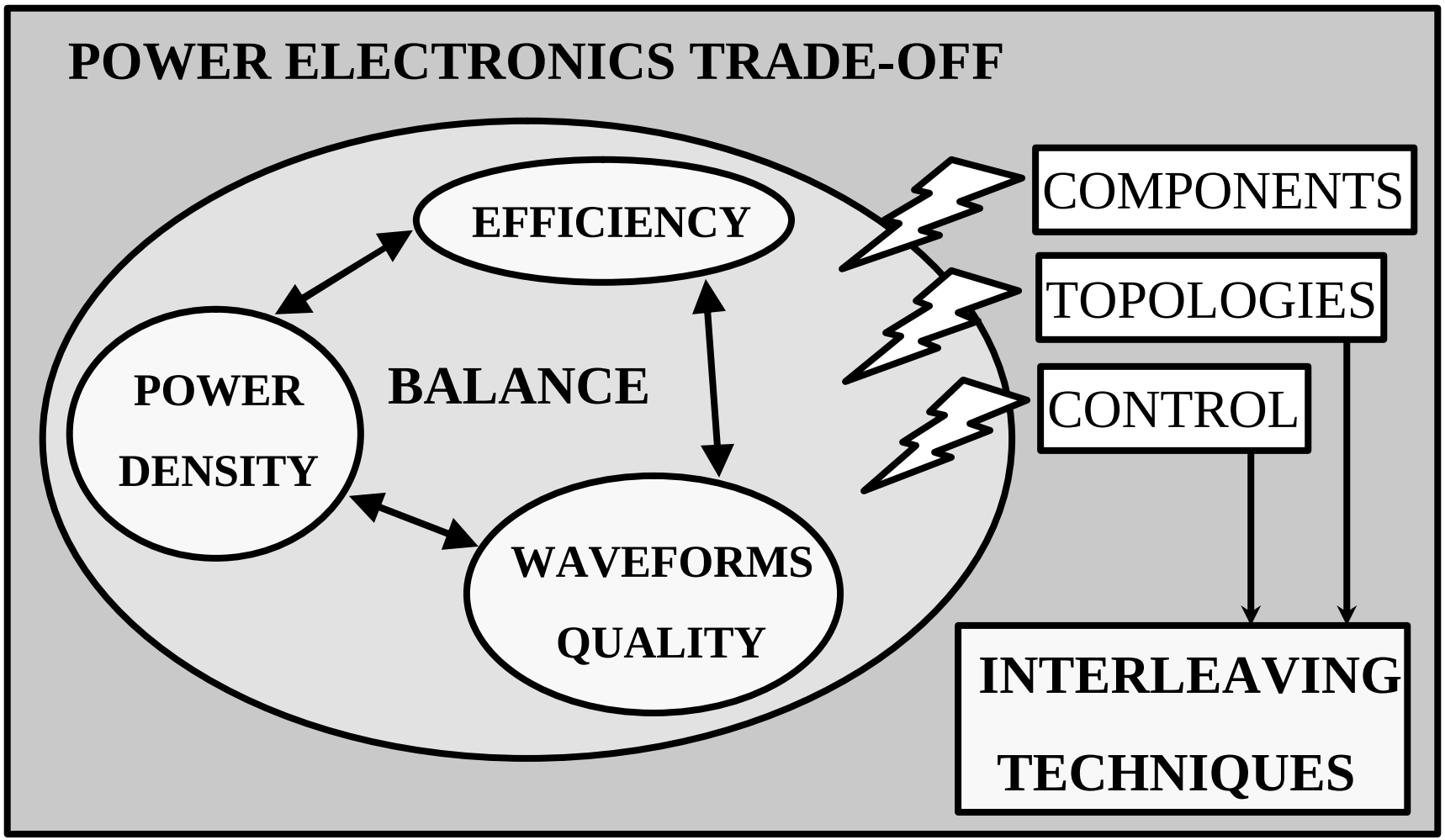
Author: Roberto Giral Castillón

Thesis Supervisor: Luis Martínez-Salamero

# OUTLINE

- Introduction and Previous Works
- The Doubler Circuit
- The Triplier Circuit
- Multiplier Circuits
- The Modified Doubler
- The Quadruplier Circuit (SCIDB)
- Conclusions and Future Research

# IMPROVEMENTS IN POWER CONVERSION



# INTERLEAVING - Previous Works

**B.A.MIWA,** ***"Interleaved Conversion Techniques for High Density Power Supplies"***

- N IDENTICAL CELLS IN PARALLEL (BOOST)
- PWM CONTROL with EQUAL DUTY CYCLE
- PHASE SHIFTING OF CONTROL SIGNALS ($2\pi/N$)
- Intuitive Example:

  Multicylinder Internal Combustion Engine
- Application: Power Factor Correction

# INTERLEAVING BENEFITS

- ✦ Reduction of Input Current and Output Voltage Ripples (High Effective Switching Frequency)
- ✦ Real Switching Frequency Low (Small Losses)
- ✦ Input Current Sharing (Boost cells in parallel)
  - 👎 👍 Size (Distributed Inductors and Switches)
  - 👍 Thermal Management - (Thermal Sinks)
  - 👍 Less Restrictive Specifications (I, V)

# MAIN GOAL

**OBTAINING VOLTAGE MULTIPLIER CIRCUITS**

- ☺ **LOW - RIPPLES**
- ☺ **GOOD DYNAMIC RESPONSE**

**HOW?**

- INTERLEAVING OF IDENTICAL BOOST CELLS
- COMPLEMENTARY ACTIVATION OF SWITCHES
- CURRENT MODE CONTROL (LARGE SIGNAL)
  - ✦ SLIDING-MODE, NON-LINEAR

# The Doubler Circuit

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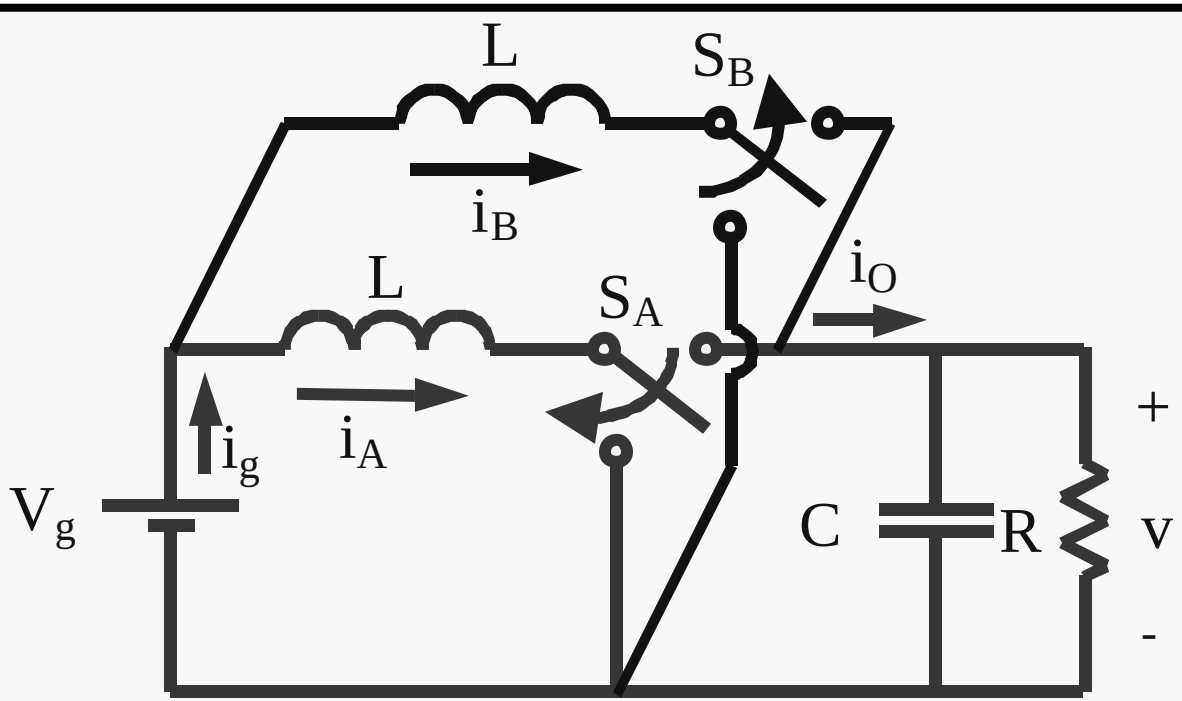
# Interleaving Dual Boost Boost Cell




- 2 Identical Boost Cells in Parallel (Continuous Conduction Mode)
- Complementary Activation of Switches

# STATE SPACE AVERAGING METHOD

- CONSTANT DUTY CYCLE (D), (D'=1-D)
- EQUAL OHMIC LOSSES (r) FOR BOTH BOOST CELLS
- STEADY-STATE OPERATING POINT

$$\begin{bmatrix} I_A \\ I_B \\ V \end{bmatrix} = \frac{V_g}{\left(D^2 + D'^2\right)} \begin{bmatrix} \frac{D}{r}(2D-1) \\ -\frac{D'}{r}(2D-1) \\ 1 \end{bmatrix}$$

IF SMALL LOSSES AND $D \neq D'$

HIGH CIRCULATING CURRENTS

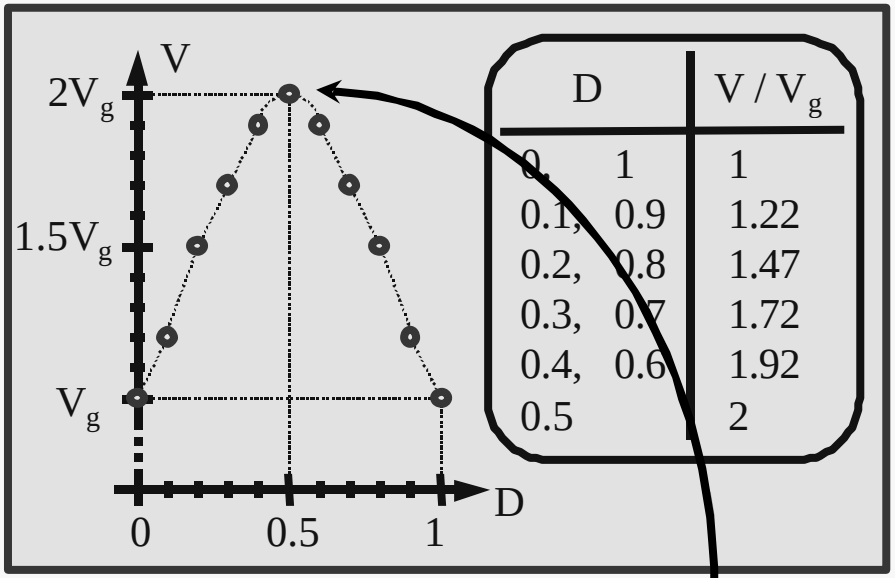
Voltage sources in parallel

D must be near 50%

# Output Voltage

Steady-State

$$V = \frac{V_g}{D^2 + D'^2} = \frac{V_g}{2D^2 - 2D + 1}$$




| D | V / $V_g$ |
|---|---|
| 0, 1 | 1 |
| 0.1, 0.9 | 1.22 |
| 0.2, 0.8 | 1.47 |
| 0.3, 0.7 | 1.72 |
| 0.4, 0.6 | 1.92 |
| 0.5 | 2 |

Voltage to duty-cycle transfer function

$$\left.\frac{\hat{V}(s)}{\hat{D}(s)}\right|_{D=D'} = 0$$

CONTROLLABILITY PROBLEM WHEN D = 50%

**VOLTAGE DOUBLER !**

**D = 50%**

# Other Transfer Functions around D=50%

Input Current

$$\frac{\hat{I}_g(s)}{\hat{D}(s)} = 0$$

Inductor Currents

$$\frac{\hat{I}_A(s)}{\hat{D}(s)} = \frac{V_g R}{L\left[r + \frac{R}{2}\right]\left(s + \frac{r}{L}\right)}$$

$$\frac{\hat{I}_B(s)}{\hat{D}(s)} = \frac{-V_g R}{L\left[r + \frac{R}{2}\right]\left(s + \frac{r}{L}\right)}$$

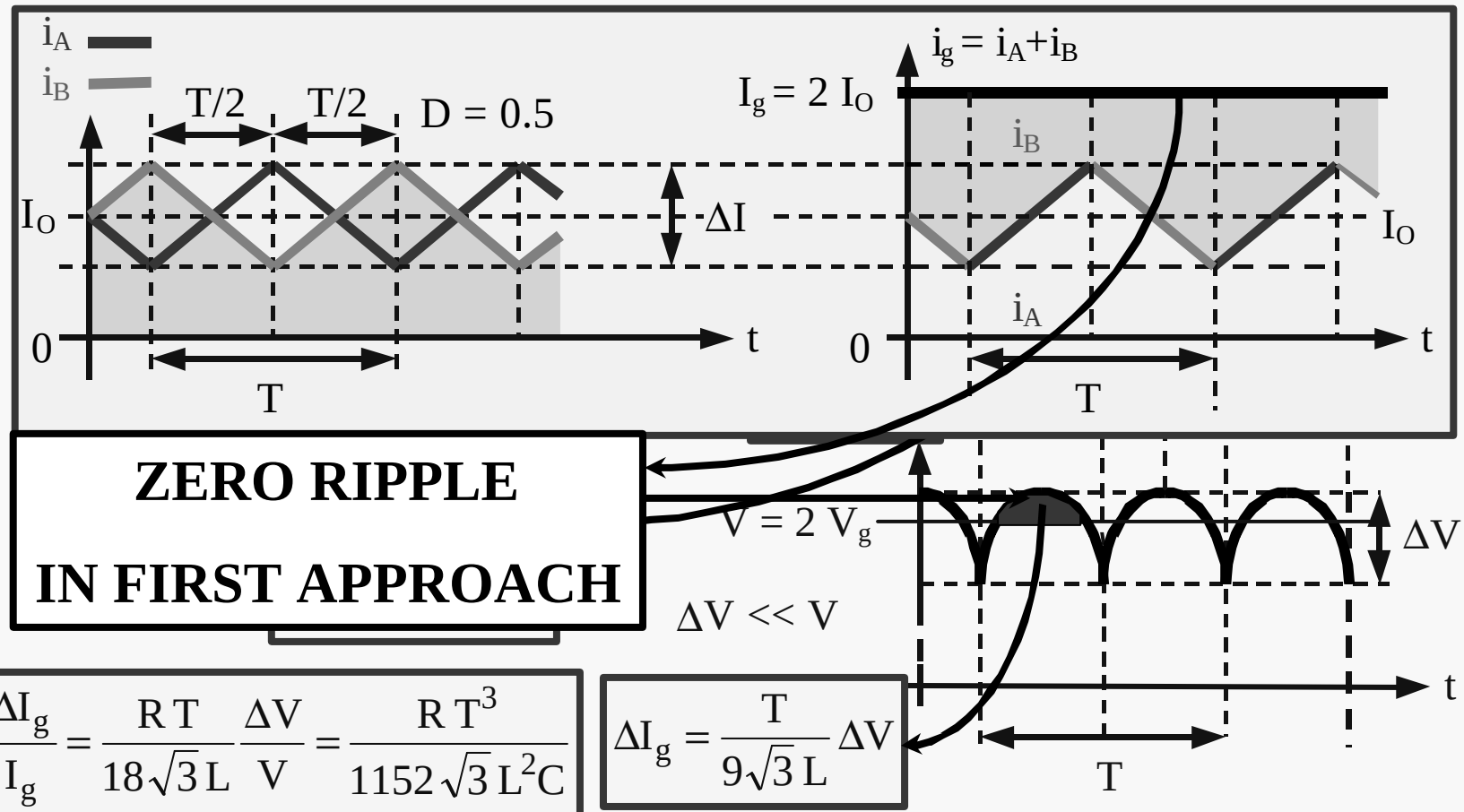
Possibility of small-signal control strategy

Input & Load perturbations (no losses )

$$\frac{\hat{V}(s)}{\hat{I}_L(s)} = \frac{-\frac{s}{C}}{s^2 + \frac{s}{RC} + \frac{1}{2LC}}$$

$$\frac{\hat{I}_g(s)}{\hat{I}_L(s)} = \frac{\frac{1}{LC}}{s^2 + \frac{s}{RC} + \frac{1}{2LC}}$$

# INPUT CURRENT RIPPLE (D=50%)




**ZERO RIPPLE**

**IN FIRST APPROACH**

$$\frac{\Delta I_g}{I_g} = \frac{R\,T}{18\sqrt{3}\,L}\frac{\Delta V}{V} = \frac{R\,T^3}{1152\sqrt{3}\,L^2 C}$$

$$\Delta I_g = \frac{T}{9\sqrt{3}\,L}\Delta V$$

# Ripple Comparisons (Doubler-Boost)

- Same Input Voltage, Load, Capacitor, Period and D = 50%.
  $V_g = 10\ V,\ R = 100\ \Omega,\ C = 1\ \mu F,\ T = 20\ \mu s$ and $D = 50\%$.
- EQUAL: ENERGY STORAGE ($L_D = 2\ L_S$) or INDUCTORS ($L_D \Delta I_D = L_S \Delta I_S$)

$$\frac{\Delta V_D}{\Delta V_S} \le \frac{T R}{32 L_D} \qquad \frac{\Delta I_{g_D}}{\Delta I_{g_S}} \le \frac{2}{9\sqrt{3}} \left(\frac{L_D}{2RC}\right)\left(\frac{\Delta V_D}{\Delta V_S}\right)$$

| **Doubler** | **V** | D**V** | D**V/V** | $\mathbf{I_g}$ | D$\mathbf{I_g}$ | D$\mathbf{I_g/I_g}$ |
|---|---|---|---|---|---|---|
| $L_D$ = 2 mH | 20.00 V | 125.00 mV | 0.63% | 0.40 A | 0.16 mA | 0.04% |
| $L_D$ = 1 mH | 20.00 V | 62.50 mV | 0.31% | 0.40 A | 0.04 mA | 0.01% |
| **Boost** | **V** | $(\mathbf{\Delta V})_{min}$ | $(\mathbf{\Delta V/V})_{min}$ | $\mathbf{I_g}$ | D$\mathbf{I_g}$ | D$\mathbf{I_g/I_g}$ |
| $L_S$ = 1 mH | 20.00 V | 2.00 V | 10.00% | 0.40 A | 0.10 A | 25.00% |

# CLOSED-LOOP CURRENT-MODE CONTROL

Why Closed Loop ? → Compensates Parameter (L, r) Mismatching

Why CMC ? → Current Sources in Parallel

- OUR CHOICE:
  - LARGE-SIGNAL TECHNIQUES
  - IN DOUBLER: SLIDING MODE CONTROL

    SWITCHING SURFACE: $S(x) = i_A - i_B = 0$
    - In equilibrium $i_A = i_B$

# SLIDING-MODE CONTROL

Ideal Sliding Dynamics (neglecting losses)

$$\begin{cases} \dfrac{di_g}{dt} = \dfrac{-v + 2V_g}{L} \\ \dfrac{dv}{dt} = \dfrac{i_g}{2C} - \dfrac{v}{RC} \end{cases}$$

LINEAR!

STABLE!

Equilibrium Point

$$\begin{cases} i_g^* = \dfrac{4V_g}{R} \\ v^* = 2V_g \end{cases} \rightarrow$$

Voltage Doubler!

$$x^* = \left(i_A^*, i_B^*, v^*\right) = \left(\frac{2V_g}{R}, \frac{2V_g}{R}, 2V_g\right)$$

STABILITY: Characteristic Polynomial

$$s^2 + \frac{s}{RC} + \frac{1}{2LC}$$

- Same poles than in open loop when (D=50%)

# Experimental Comparisons (Doubler-Boost)

- $V_g$ = 10 V, L = 1 mH, R = 50 Ω, C = 6.8 μF, T = 20 μs, current sensing resistors r = 500 mΩ and D = 50%.

| **Doubler** | **V** | D**V** | D**V/V** | $\mathbf{I_g}$ | D$\mathbf{I_g}$ | D$\mathbf{I_g/I_g}$ |
|---|---|---|---|---|---|---|
| Theory | 20.00 V | 18.38 mV | 0.09% | 0.80 A | 23.58 μA | 0.003% |
| Experimental | 18.11 V | 45.00 mV | 0.25% | 0.71 A | 15.00 mA | 2.11% |
| **Boost** | **V** | D**V** | D**V/V** | $\mathbf{I_g}$ | D$\mathbf{I_g}$ | D$\mathbf{I_g/I_g}$ |
| Theory | 20.00 V | 0.59 V | 2.95% | 0.80 A | 0.10 A | 12.50% |
| Experimental | 17.50 V | 0.57 V | 3.26% | 0.67 A | 0.09 A | 13.43% |

# Ripple Details of Doubler

$V_g = 12$ V

L = 1 mH

R = 50 Ω

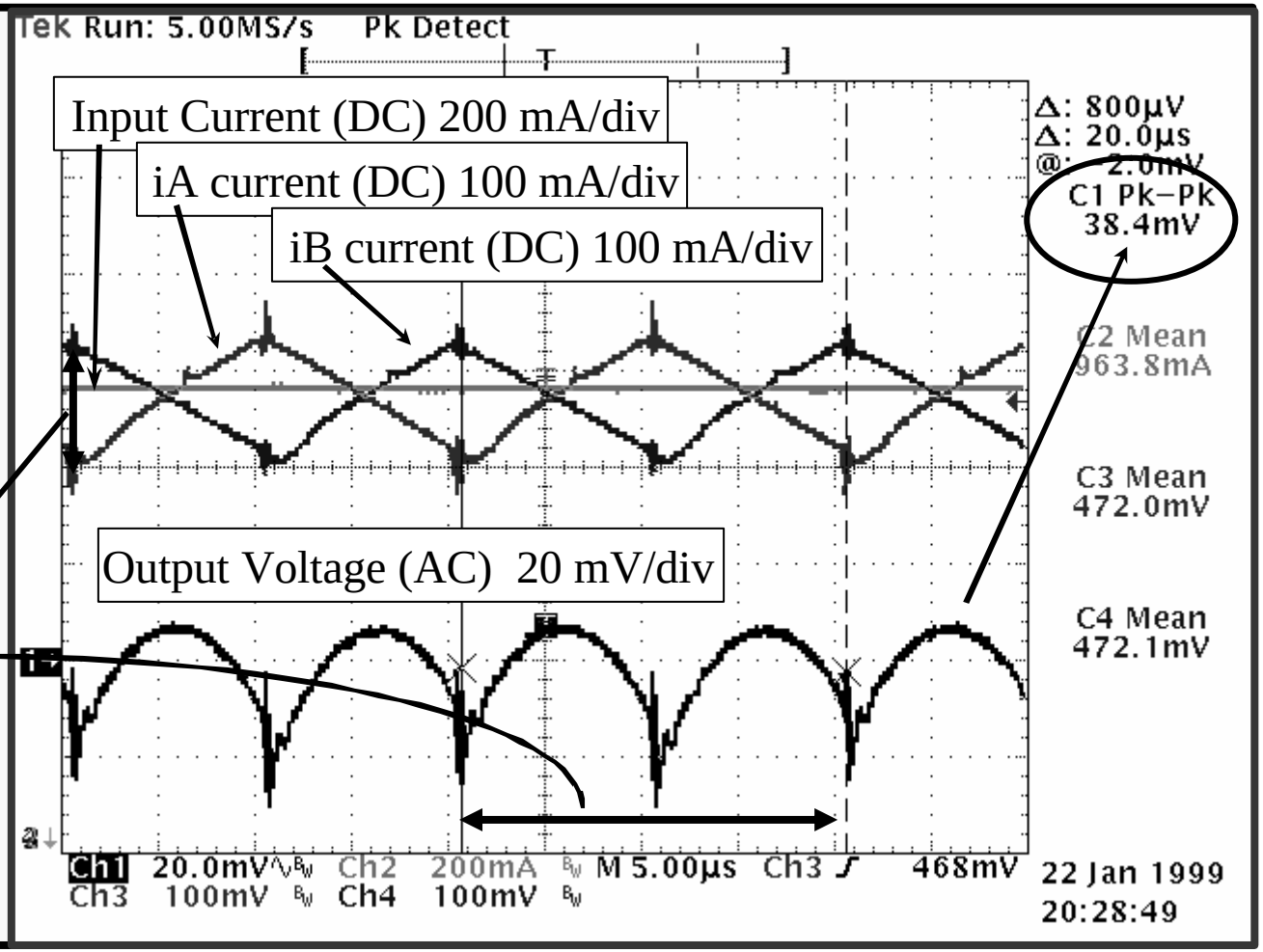
C = 6.8 μF

Δi = 120 mA

T = 20 μs

**r = 33 m**W

D = 50%



# OTHER EXPERIMENTS

- LOAD REGULATION (50 Ω-100 Ω) As expected
- LINE REGULATION (x2) As expected
- EFFICIENCY ($V_g$ from 9 V to 16 V)
  - 88% - 91% for a 50 Ω Resitive Load (6 - 22 W)
  - 82% - 89% for a 100 Ω Resistive Load (3 - 11 W)
- Output Voltage Ripple ($V_g$ from 9 V to 16 V)
  - 40 - 80 mV (50 Ω Load)
  - 60 - 350 mV (100 Ω Load)

# Doubler Summary

- The Interleaved Dual Boost is Presented:

  Requires D=50% to Avoid High Circulating Currents

- Low-Ripple Voltage Doubler Behaviour
- Closed-loop CMC (Self-Oscillating Sliding)
  - 👍 Linear & Stable Large-Signal Dynamics
  - 👍 Compensates for Parameter Mismatching
  - No Output Voltage Regulation
  - Variable Switching Frequency (depends on $V_g$)

# The Triplier Circuit

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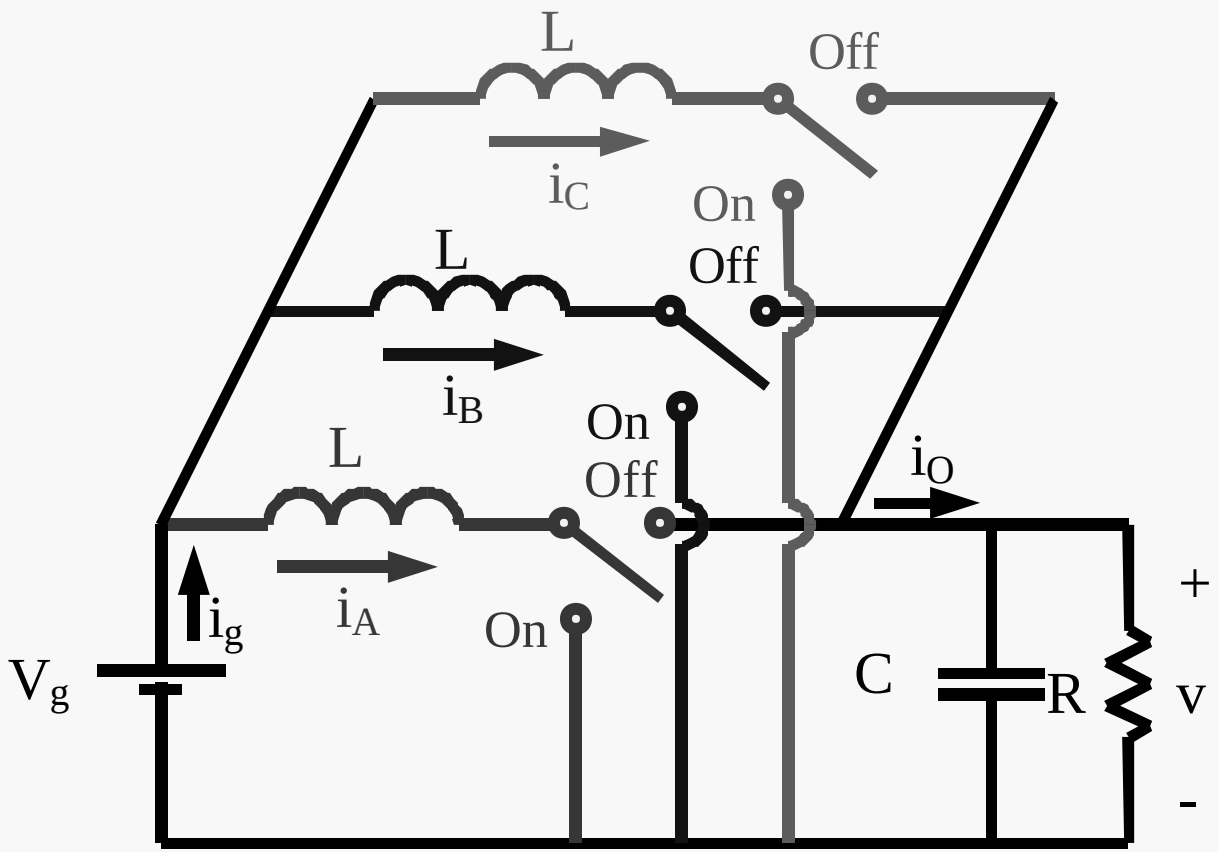
# Triplier Circuit

- Other Input-Output Voltage Ratios
- Keeping Low-Ripple by Means of Interleaving
  - Connecting More Converters in Parallel (N)
  - Maintaining Complementary Activation of Switches
  - (N-1) Optimal Duty Cycles with Harmonic Cancellation.

TRIPLIER !

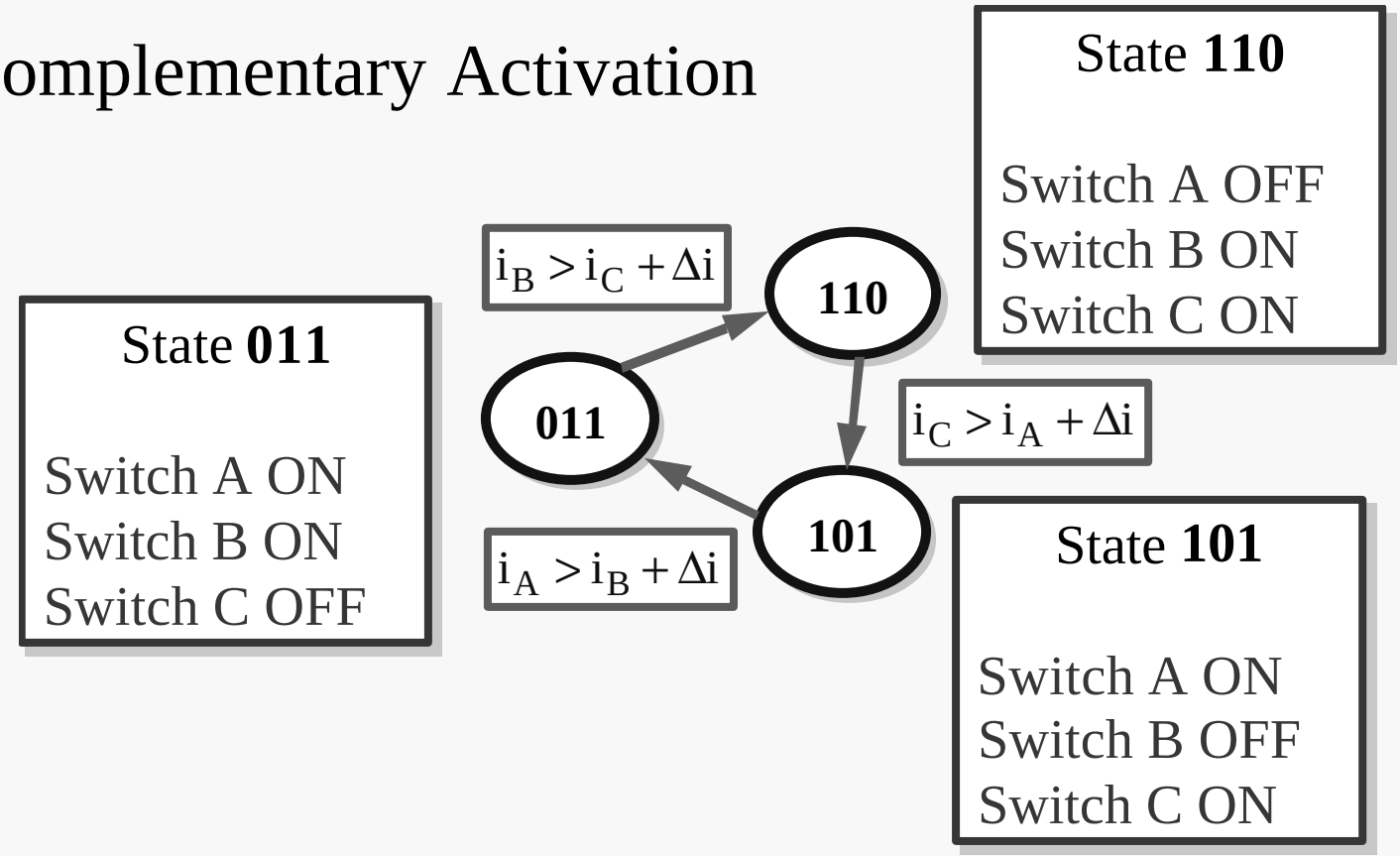
- (N=3) $D = 1/3$ & $D = 2/3$
- Output Voltages: $V = 3\,V_g/2$ & $\mathbf{V = 3\,V_g}$

# Power Stage

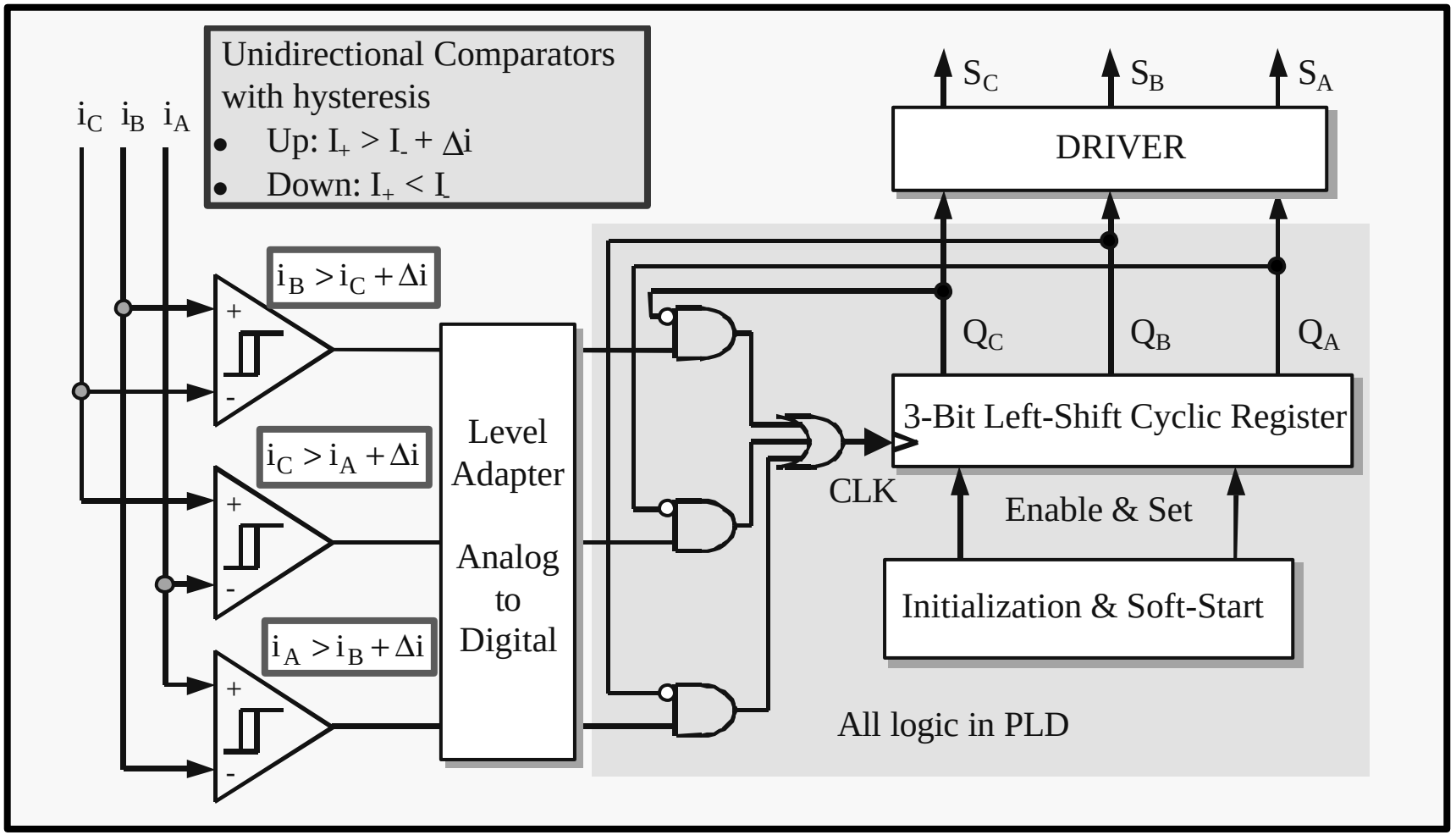


# Switching Strategy

Complementary Activation



# Implementation of the Switching Strategy



# Ripples & Comparison with Boost

| T | V | D**V** | D**V**/**V** | $I_g$ | D$I_g$ | D$I_g$/$I_g$ |
|---|---|---|---|---|---|---|
| 20.00 μs | 30.00 V | 112.92 mV | 0.38% | 1.80 A | 80.5 μA | 0.005% |
| 16.67 μs | 30.00 V | 78.41 mV | 0.26% | 1.80 A | 46.6 μA | 0.003% |
| 6.15 μs | 30.00 V | 10.68 mV | 0.04% | 1.80 A | 2.34 μA | 0.000% |

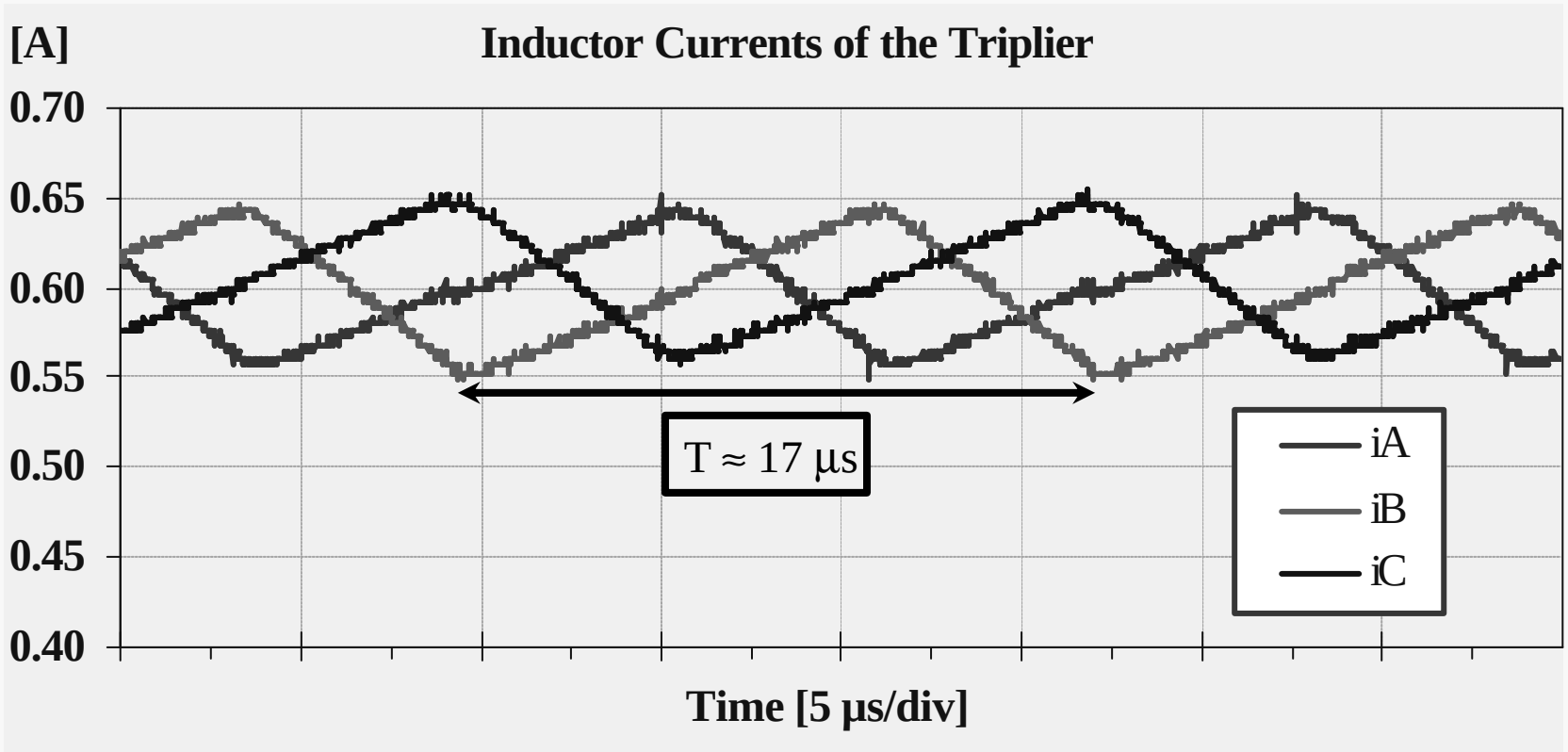
- Equal inductive storage ($L_S$ = L/3) and D = 2/3.
- $V_g$ = 10 V, L = 1.2 mH, C = 820 nF, R = 50 Ω

Boost

| T | V | (D**V**)$_{min}$ | (D**V**/**V**)$_{min}$ | $I_g$ | D$I_g$ | D$I_g$/$I_g$ |
|---|---|---|---|---|---|---|
| 20.00 μs | 30.00 V | 9.76 V | 32.53% | 1.80 A | 0.33 A | 18.52% |
| 16.67 μs | 30.00 V | 8.13 V | 27.10% | 1.80 A | 0.28 A | 15.43% |
| 6.15 μs | 30.00 V | 3.00 V | 10.00% | 1.80 A | 0.10 A | 5.69% |

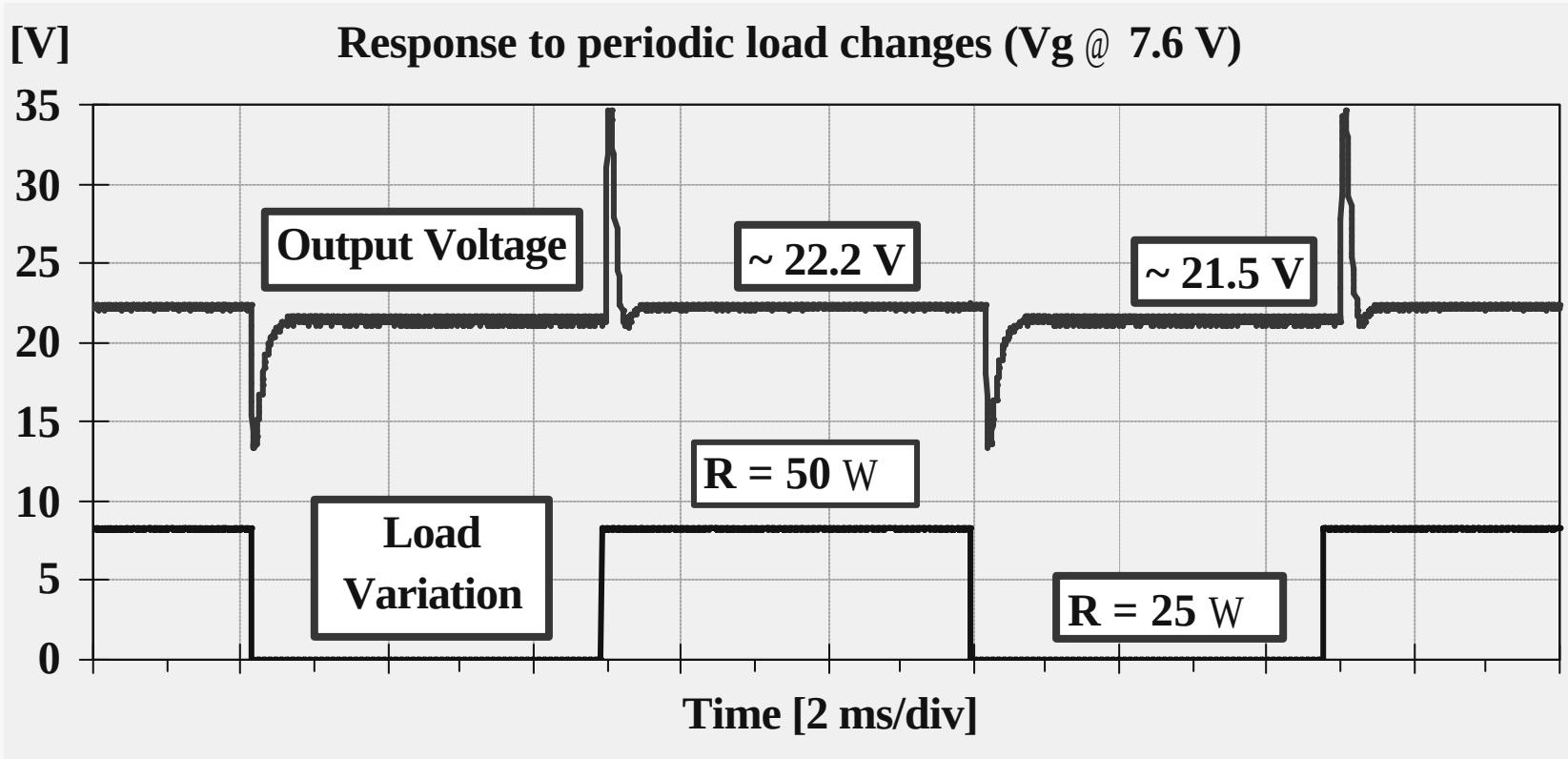
# Currents of Inductors (Experimental)

**Corresponding Output Voltage of 29.3 V with Maximum Ripple Peaks of 200 mV**



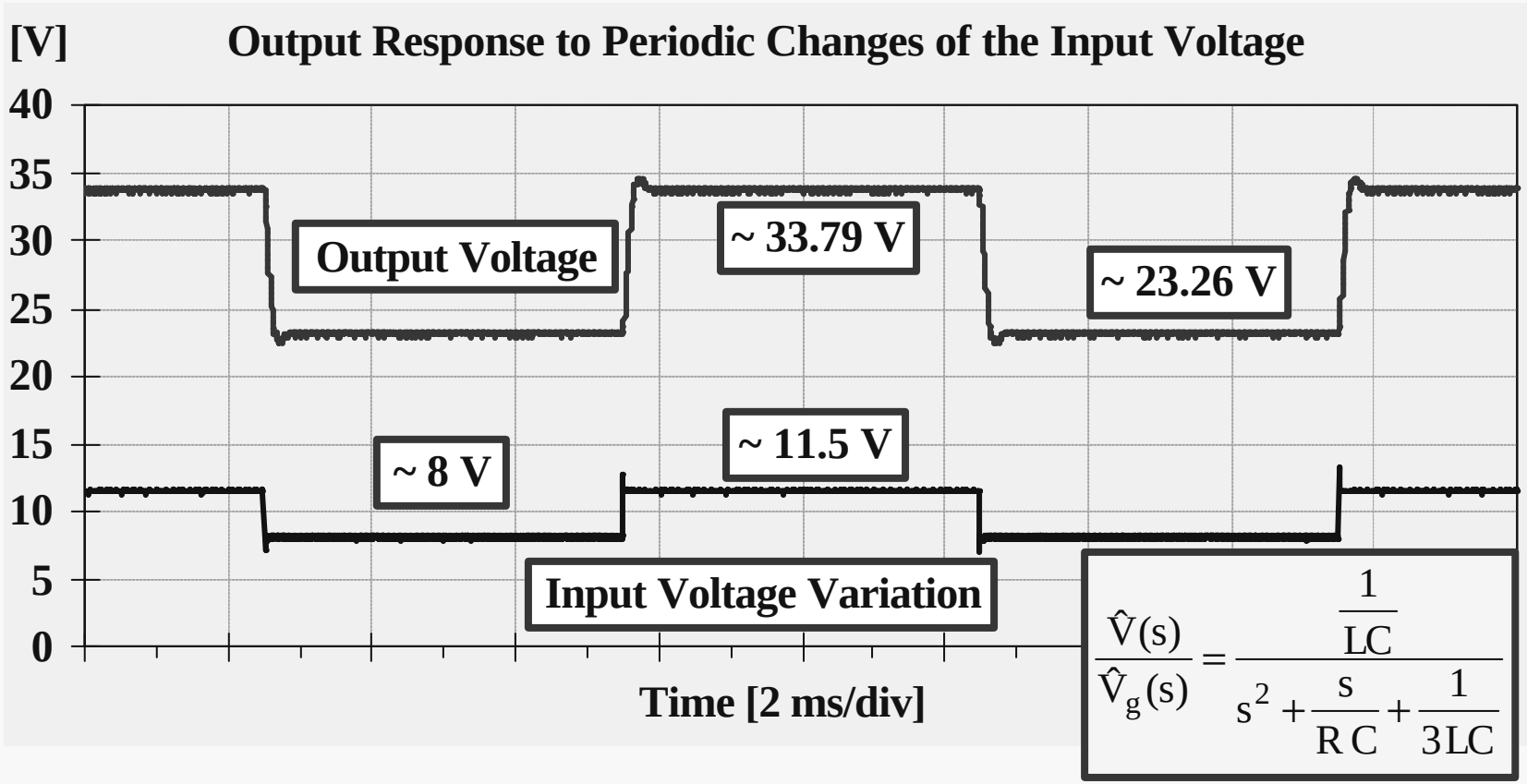

- $V_g$ = 10 V, L = 1.2 mH, **C = 820 nF**, R = 50 Ω, r = 33 mΩ, Δi = 50 mA

# Load Regulation (Experimental)




- $V_g$ = 10 V, L = 1.2 mH, C = 820 nF, r = 33 mΩ, Δi = 50 mA

# Input Voltage Variations (Experimental)




- L = 1.2 mH, C = 820 nF, R = 50 Ω, r = 33 mΩ, Δi = 50 mA

# Triplier Summary

- Increasing the Number of Interleaved Cells (N) Provides (N-1) Optimal Duty Cycles
- Derived from the Doubler Case, a Closed-Loop CMC Self-Oscillating Strategy is Applied when N=3
- In General, the Results are Similar to Those Obtained in the Doubler Case
- Low-Ripple Voltage Triplier Behaviour
  - 👍 Higher Effective Switching Frequency
  - 👎 Increased Complexity and More Parts

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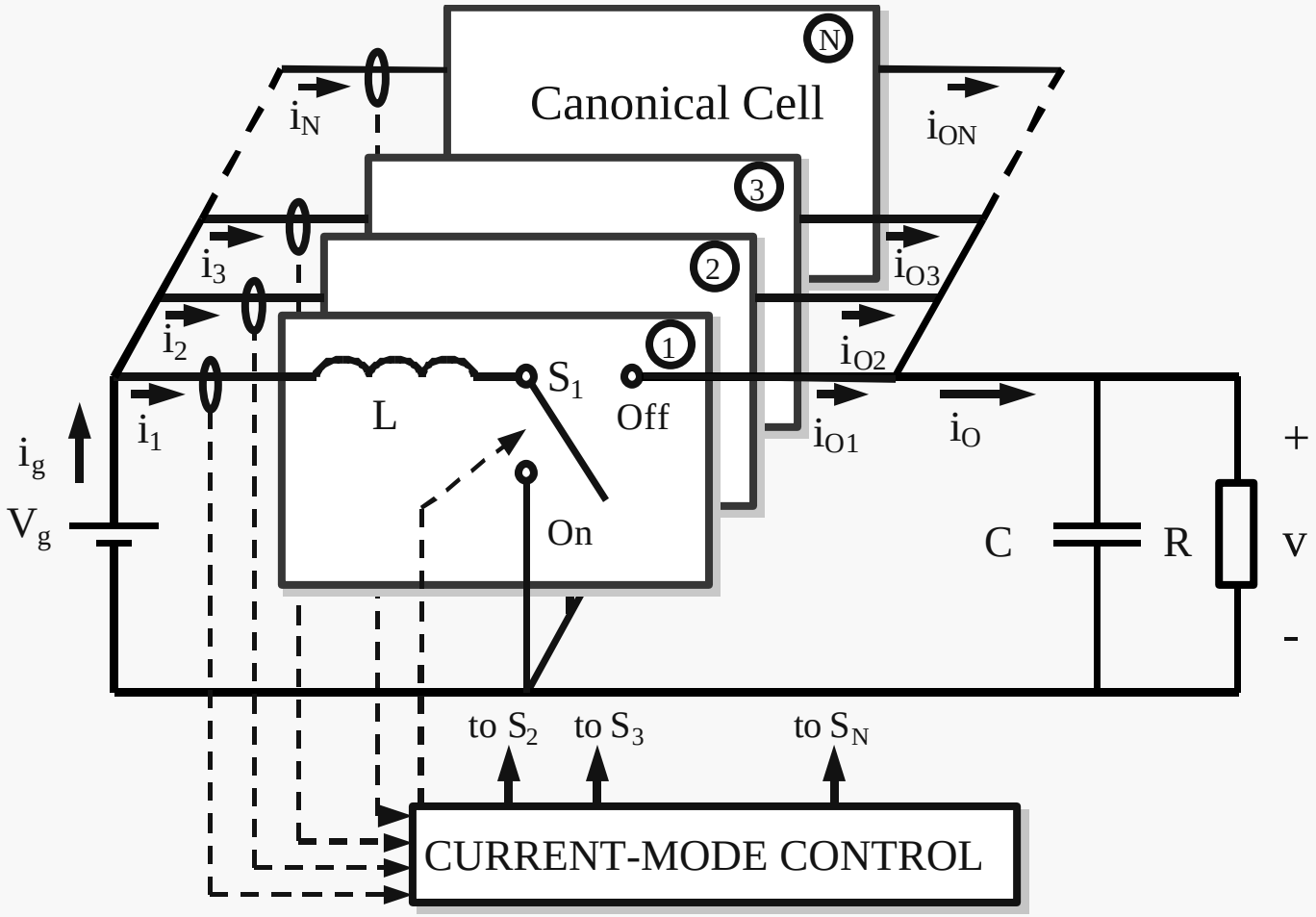
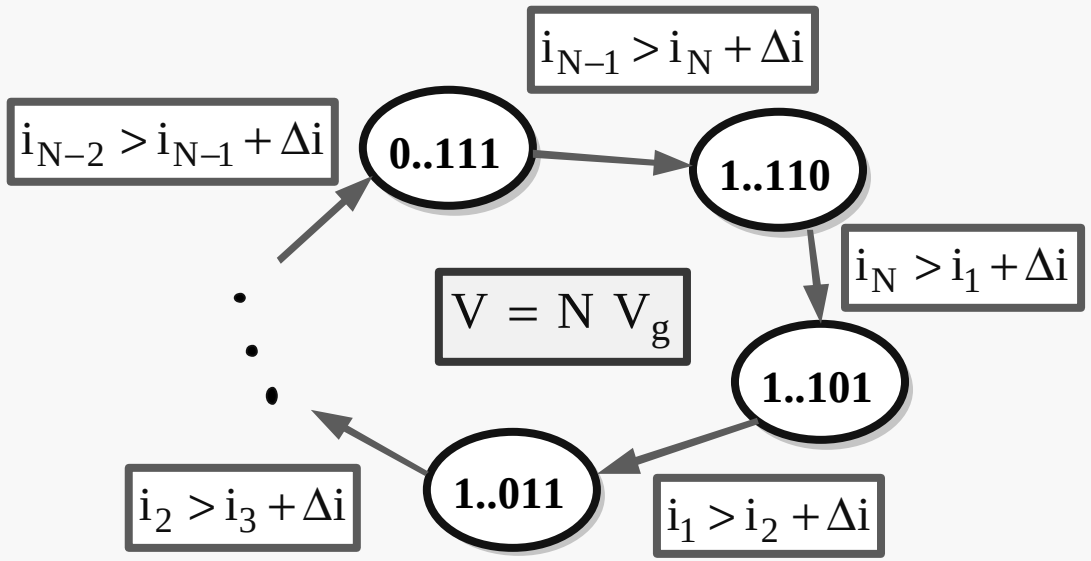
# Increasing the Number of Converters



# Control Strategy for Voltage Multiplication




| State 0..111 | State 1..110 |
|---|---|
| Switch 1 ON<br>Switch 2 ON<br>Switch 3 ON<br>…<br>Switch N OFF | Switch 1 OFF<br>Switch 2 ON<br>Switch 3 ON<br>…<br>Switch N ON |
| **State 1..101** | **State 1..011** |
| Switch 1 ON<br>Switch 2 OFF<br>Switch 3 ON<br>…<br>Switch N ON | Switch 1 ON<br>Switch 2 ON<br>Switch 3 OFF<br>…<br>Switch N ON |

Input-Output Transfer Function

$$\frac{\hat{V}(s)}{\hat{V}_g(s)} = \frac{\frac{1}{LC}}{s^2 + \frac{s}{RC} + \frac{1}{NLC}}$$

# Ripples

| $\Delta Ig$ | $\Delta I/Ig$ | $\Delta V$ | $\Delta V/V$ |
|---|---|---|---|
| $\frac{V_g(N-1)}{36\sqrt{3}L^2C}\cdot\left(\frac{T}{N}\right)^3$ | $\frac{R(N-1)}{36\sqrt{3}L^2C}\cdot\frac{T^3}{N^5}$ | $\frac{V_g(N-1)}{8LC}\cdot\left(\frac{T}{N}\right)^2$ | $\frac{(N-1)}{8LC}\cdot\frac{T^2}{N^3}$ |

Comparison with Boost

$$\frac{\Delta I_g}{\Delta I_{gS}} \le \frac{T^2}{36\sqrt{3}LCN^3}$$

$$\frac{\Delta V}{\Delta V_S} \le \frac{TR}{8LN^2}$$

| **Octuplier N=8** | **V** | D**V** | D**V/V** | $\mathbf{I_g}$ | D$\mathbf{I_g}$ | D$\mathbf{I_g/I_g}$ |
|---|---|---|---|---|---|---|
| L = 2 mH | 80.00 V | 34.18 mV | 0.04% | 6.40 A | 5.48 μA | 0.00% |
| **Boost** | **V** | $(\Delta\mathbf{V})_{\mathbf{min}}$ | $(\Delta\mathbf{V/V})_{\mathbf{min}}$ | $\mathbf{I_g}$ | D$\mathbf{I_g}$ | D$\mathbf{I_g/I_g}$ |
| $L_S$ = 250 μH | 80.00 V | 17.50 V | 21.86% | 6.40 A | 0.70 A | 10.94% |

$V_g$ = 10 V, R = 100 Ω, C = 800 nF, T = 20 μs (Hysteresis width Δi = 12.5 mA).

# Summary

- LIMITS to N
  - Desired Output Voltage is $N V_g$?
  - Switching Frequency - Hysteresis Width → $T = \frac{N L \Delta i}{V_g}$
  - Maximum Duty Cycle ( D = (N-1)/N  if  Dmax = 90% : N = 10 )
- Other Optimal Duty Cycles Among (N-1) are Possible
  - How? :  More Switches OFF at the Same Time.
  - More Complexity
  - Option: Very Large Number + Integration
  - More Features (i.e., Fault Tolerance)
  - Discontinuous Conduction Mode

# The Modified Doubler

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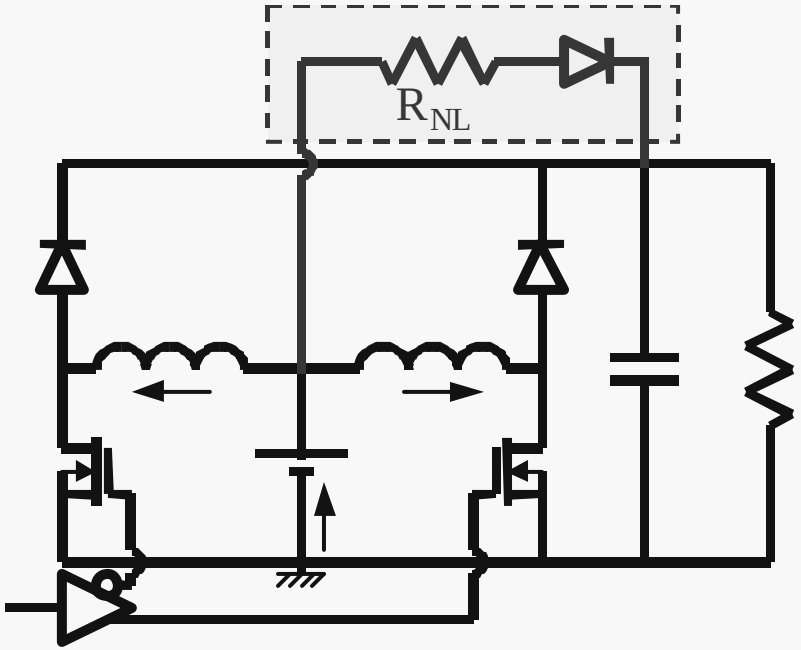
# Several Possibilities Studied in the Doubler

- Boost Cells are Different (Example: Inductance Values)
  - Ripple Increasing but Compensated by Closed-Loop
- Magnetic Coupling Between Inductors
  - Additional Freedom Degree $\longrightarrow$ $s^2 + \frac{s}{RC} + \frac{1}{2L(1+k)C}$
- Unidirectional Switches
  - Discontinuous Conduction Mode Possibility
- More General Sliding Surface $S(x) = i_A - \alpha\, i_B = 0 \quad (\alpha > 0)$
  - Equilibrium Point Insensitive to Current Sensing Errors

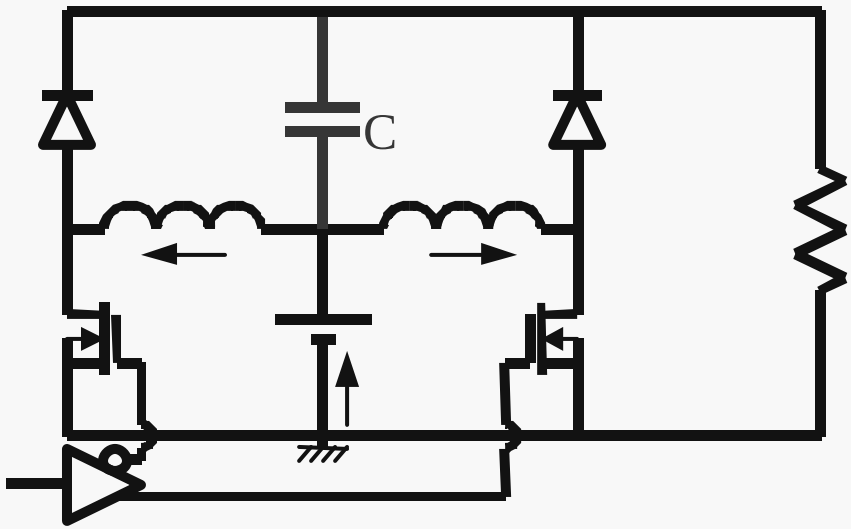
# Topology Modifications

- Non-Linear Network
  - Overshoot Reduction in Start-Up



# Topology Modifications II

- Floating Output Capacitor
  - Reduces the Voltage in the Capacitor
  - More Input Current Ripple
  - Origin of SCIDB



# The Quadruplier Circuit (SCIDB)

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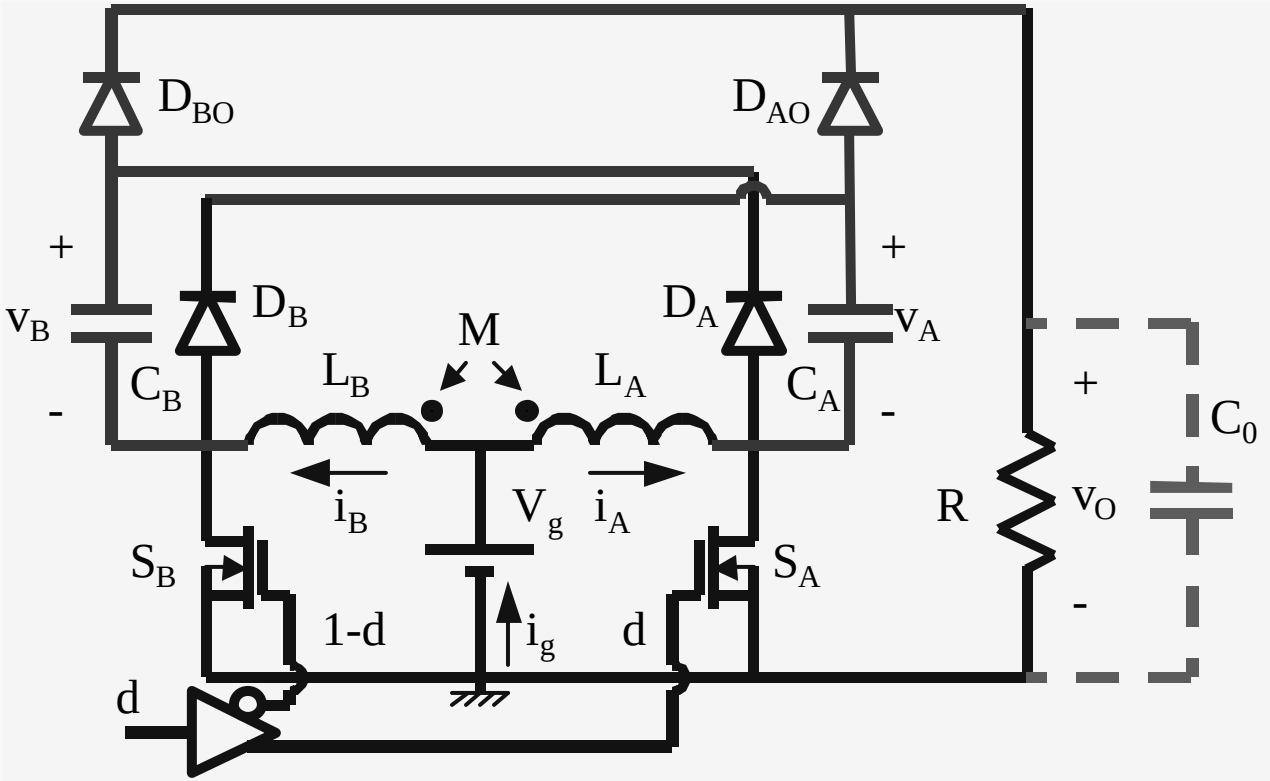
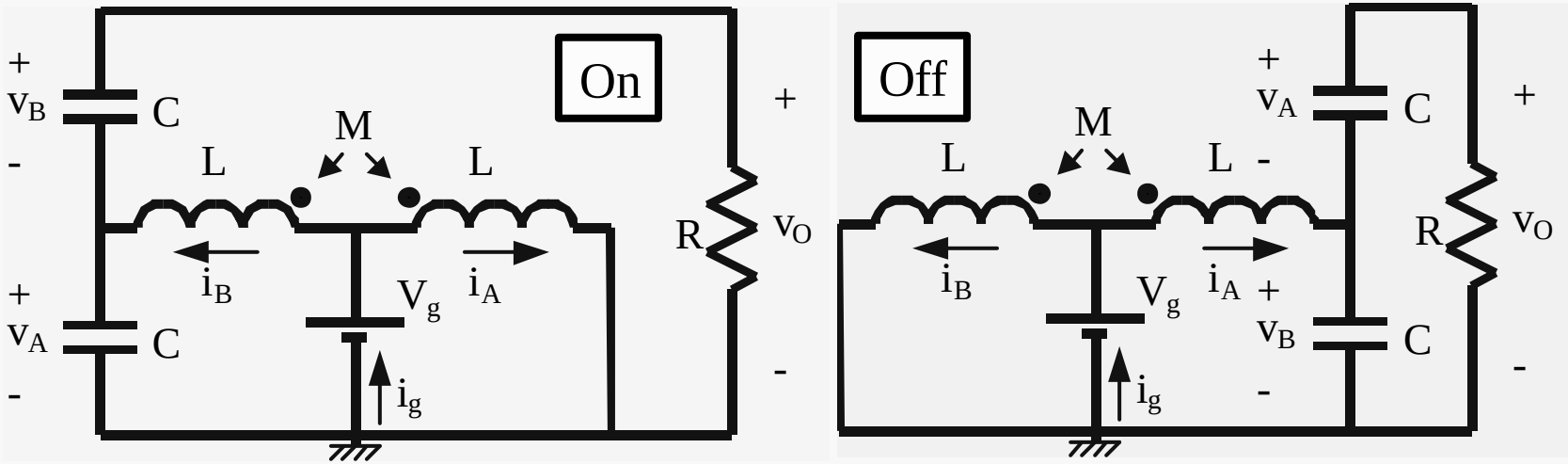
# SCIDB Circuit

- Switched Capacitor Interleaved Dual Boost



# State-Space Averaging Method




- Equilibrium Point (Open-Loop)

$$\begin{cases} I_A = \dfrac{V_g}{R\,D\,(1-D)^2} \\ I_B = \dfrac{V_g}{R\,D^2(1-D)} \end{cases}$$

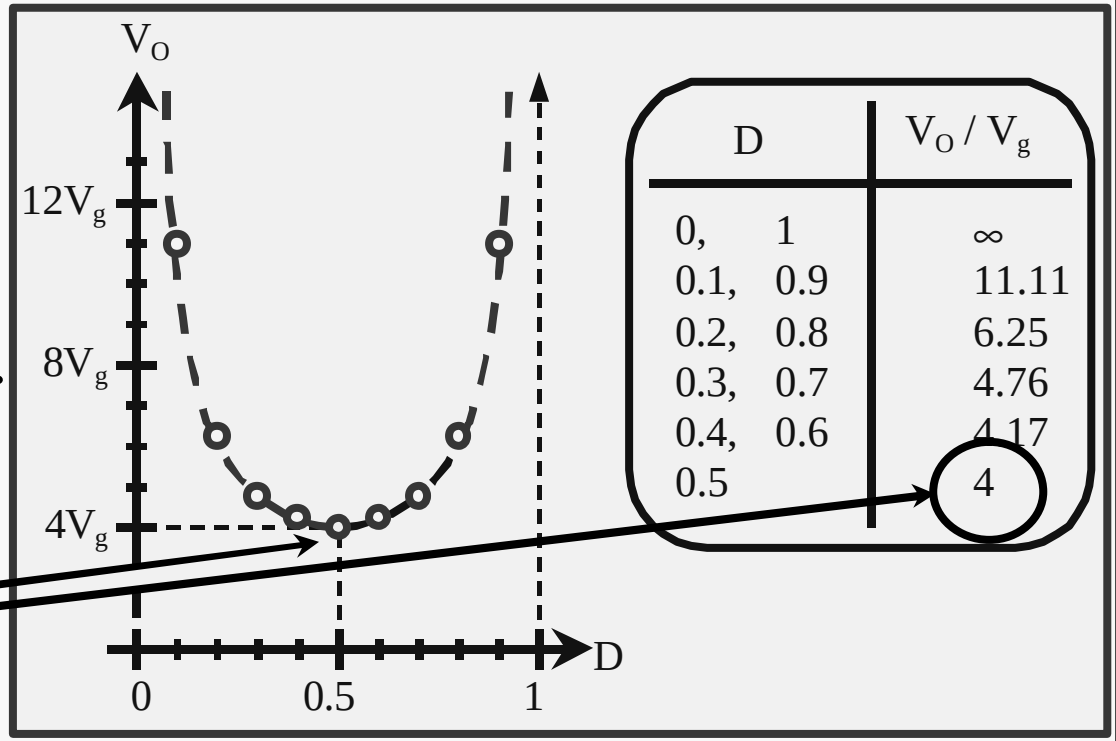
$$\begin{cases} V_A = \dfrac{V_g}{D} \\ V_B = \dfrac{V_g}{1-D} \end{cases}$$

$$\begin{cases} I_g = I_A + I_B = \dfrac{V_g}{RD^2(1-D)^2} \\ V_O = V_A + V_B = \dfrac{V_g}{D(1-D)} \end{cases}$$

# Output Voltage

Steady-State

$$V_O = \frac{V_g}{D\,D'} = \frac{V_g}{D - D^2}$$




| D | $V_O / V_g$ |
|---|---|
| 0, 1 | ∞ |
| 0.1, 0.9 | 11.11 |
| 0.2, 0.8 | 6.25 |
| 0.3, 0.7 | 4.76 |
| 0.4, 0.6 | 4.17 |
| 0.5 | 4 |

**VOLTAGE QUADRUPLIER !**

**D = 50%**

- No Circulating Currents
- Wide Margin of Possible Duty Cycles

# SMALL-SIGNAL ANALYSIS

- Fourth Order Transfer Function
- Same Controllability Problem of the Doubler Circuit Around D=50% for $V_O$ or $I_g$
- Existence of Right-Half Plane Zeros

CMC CLOSED-LOOP

- Same Sliding-Mode Strategy used in the Doubler

$$S(x) = i_A - \alpha\, i_B = 0 \qquad (\alpha > 0)$$

# SLIDING-MODE CONTROL

- Non-Linear Ideal Sliding Dynamics
- Equilibrium Point ⟶

$$i_A^* = \frac{(1+\alpha)^3}{\alpha} \cdot \frac{V_g}{R} \qquad v_A^* = \frac{(1+\alpha)}{\alpha} V_g$$

$$i_B^* = \frac{(1+\alpha)^3}{\alpha^2} \cdot \frac{V_g}{R} \qquad v_B^* = (1+\alpha) V_g$$

$$i_g^* = \frac{(1+\alpha)^4}{R\,\alpha^2} V_g \qquad v_O^* = \frac{(1+\alpha)^2}{\alpha} V_g$$

Relation between $\alpha$ and D

$$D = \frac{\alpha}{1+\alpha} \qquad \alpha = \frac{D}{1-D} = \frac{D}{D'}$$

$\alpha = 1$ implies D = 50%

Voltage Quadruplier !

# ASYMPTOTIC STABILITY

- Local Stability Condition

  $(-1 < k < 1) \quad (\alpha > 0)$

$$k > \frac{-2\alpha}{1+\alpha^2}$$

**Always Satisfied if k = 0**

- Characteristic Polynomial in the Quadruplier Case ($\alpha = 1$)

$$\left(s+\frac{2}{RC}\right)\left(s^2+\frac{2}{RC}s+\frac{1}{4L(1+k)C}\right)$$

STABLE!

- 2nd Lyapunov Method aplied to the Quadruplier

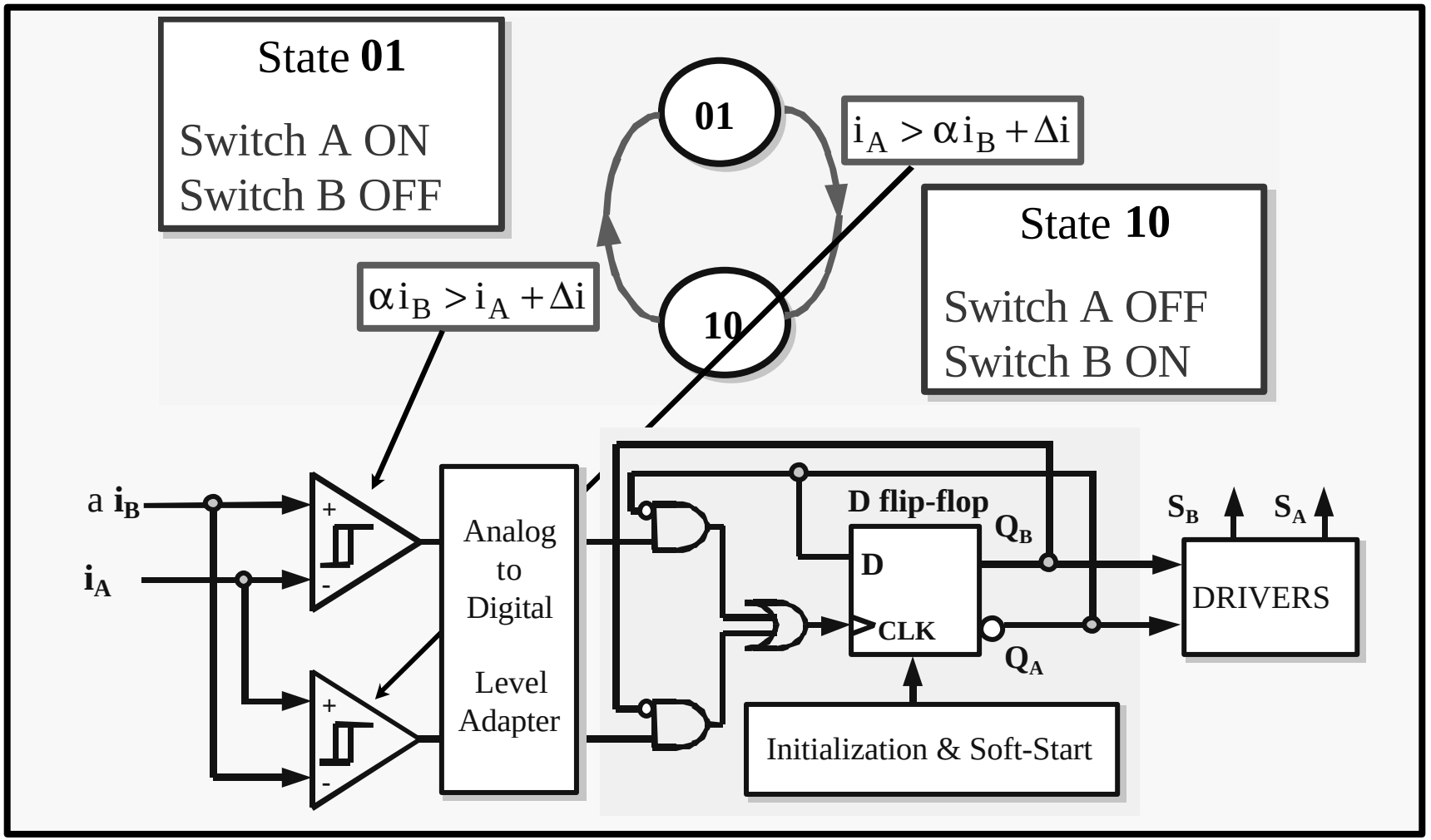
$$V(x) = R\left[\frac{(1+k)L}{2}\hat{i}_g^2 + C\left(\hat{v}_A^2+\hat{v}_B^2\right)\right]$$

$$\frac{dV}{dt} = -2\left(\hat{v}_A^2+\hat{v}_B^2+\frac{2}{v_A+v_B}\left(v_B\hat{v}_A^2+v_A\hat{v}_B^2\right)\right)$$

Positive Energy Function with Negative Derivative

**Stable in the Large !**

# Switching Strategy



# Waveforms of Quadruplier

$V_g$ = 12 V

L = 1 mH

R = 100 Ω

C = 1.7 μF

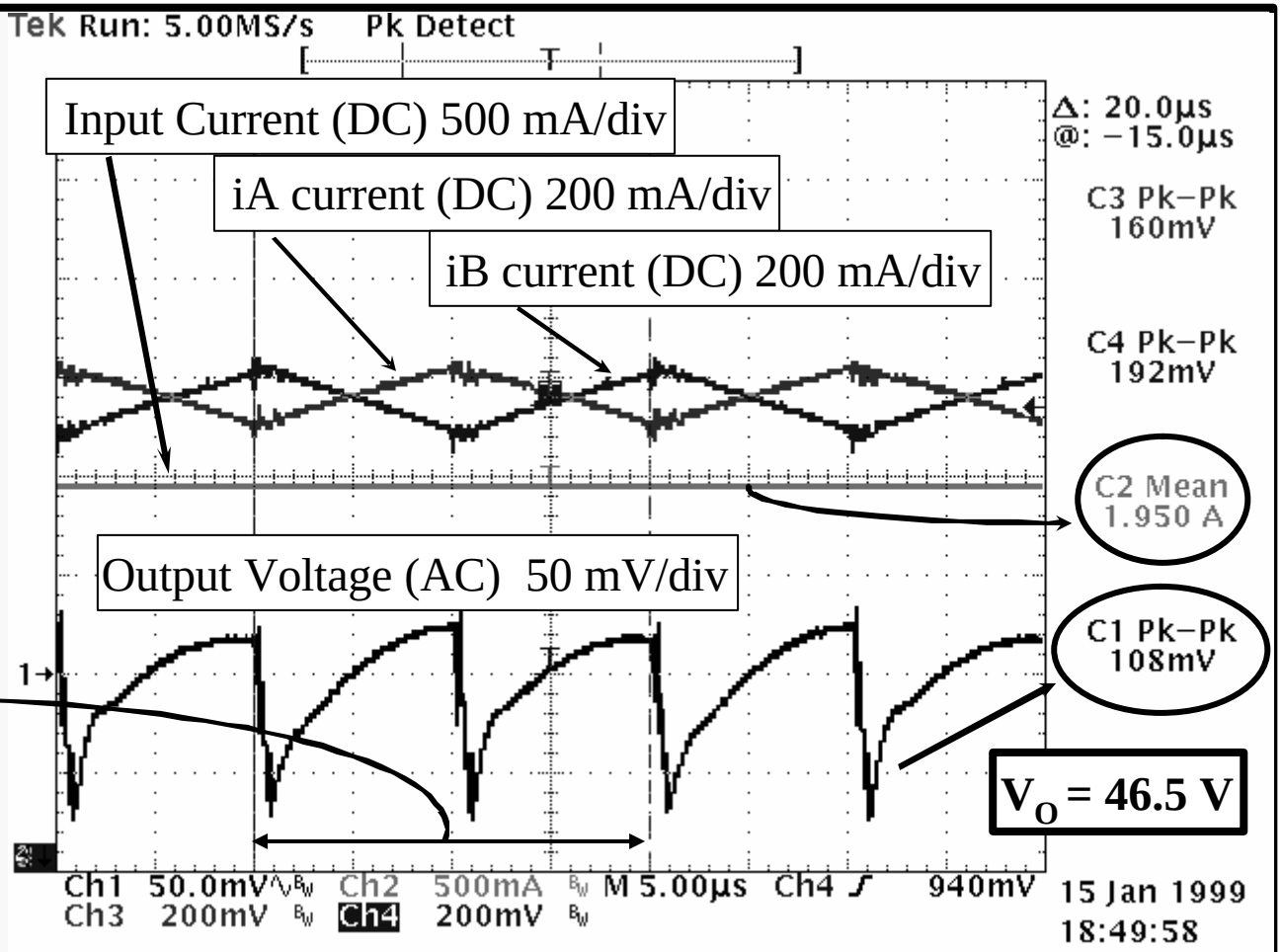
**Co = 3 mF**

Δi = 120 mA

T = 20 μs

r = 33 mΩ

α = 1




**$V_O$ = 46.5 V**

# Load Regulation (Experimental)

L = 1 mH

C = 1.7 μF

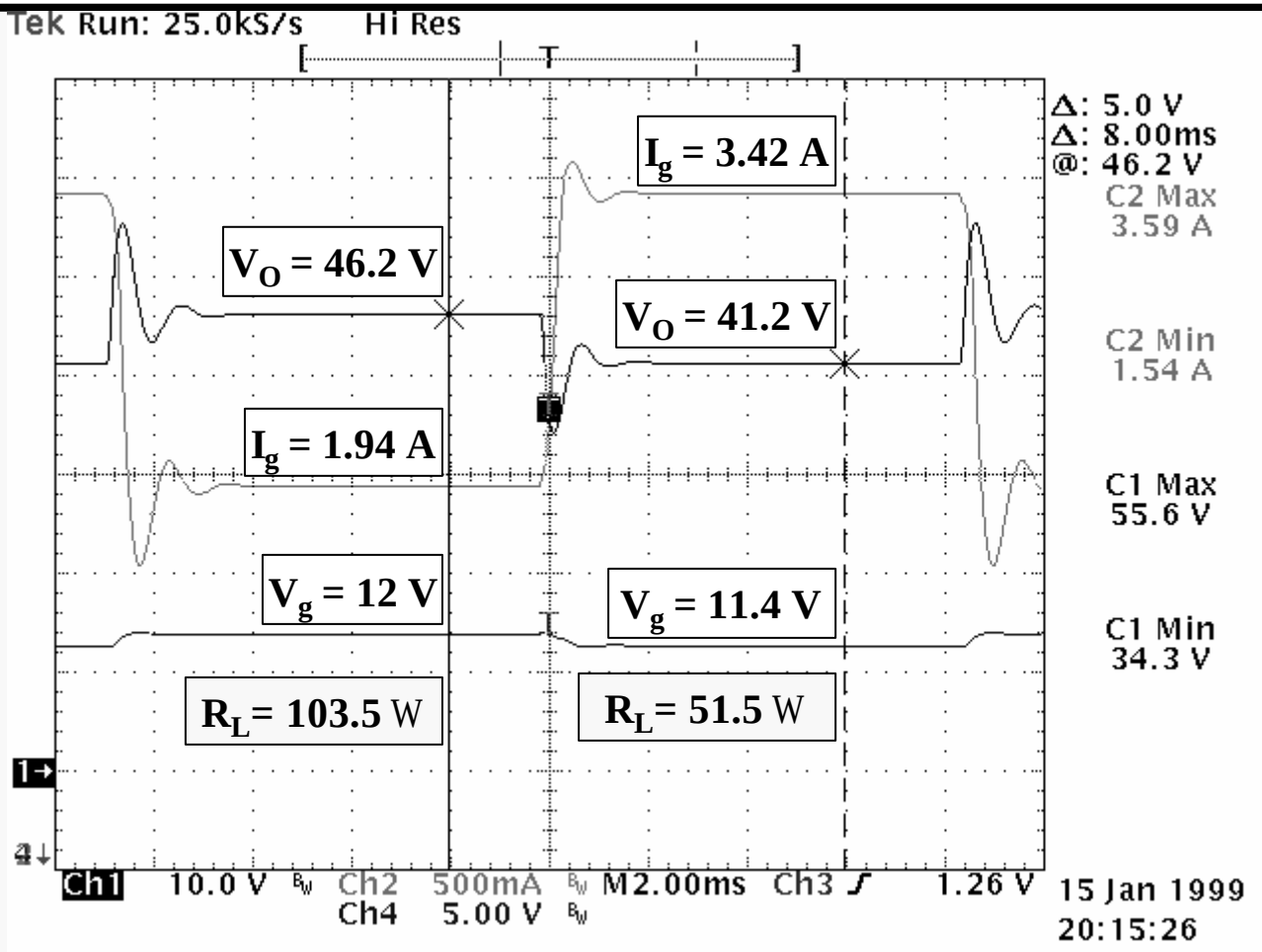
**Co = 3 mF**

Δi = 120 mA

T = 20 μs

r = 33 mΩ

α = 1



# Output Voltage Ripples (Experimental)

L = 1 mH

C = 1.7 μF

**Co = 3 mF**

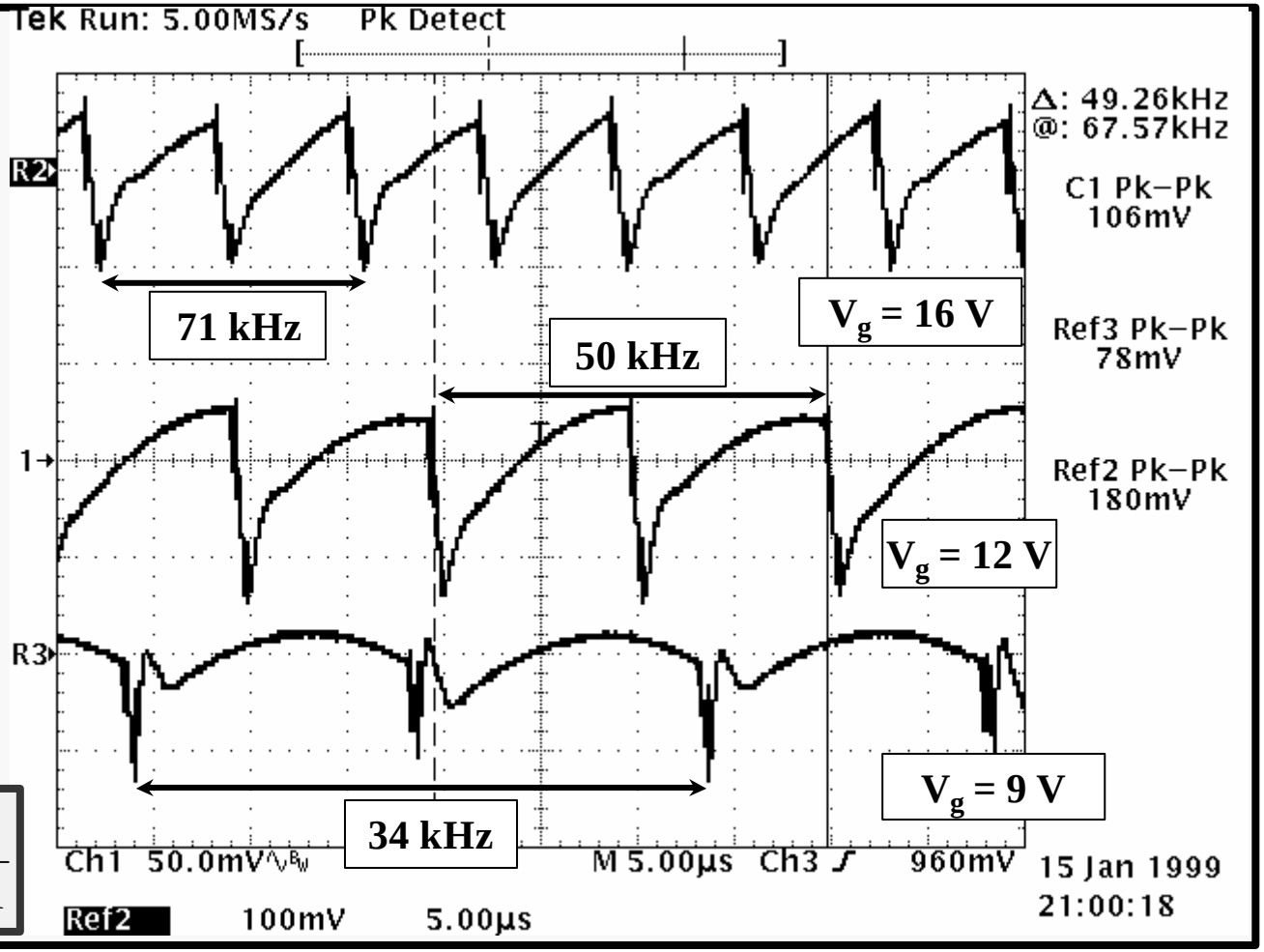
R = 100 Ω

Δi = 120 mA

r = 33 mΩ

α = 1

$$f_S = \frac{V_g}{2 L \Delta i}$$



# Waveforms of SCIDB for a = 2

$V_g$ = 12 V

L = 1 mH

R = 100 Ω

C = 1.7 μF

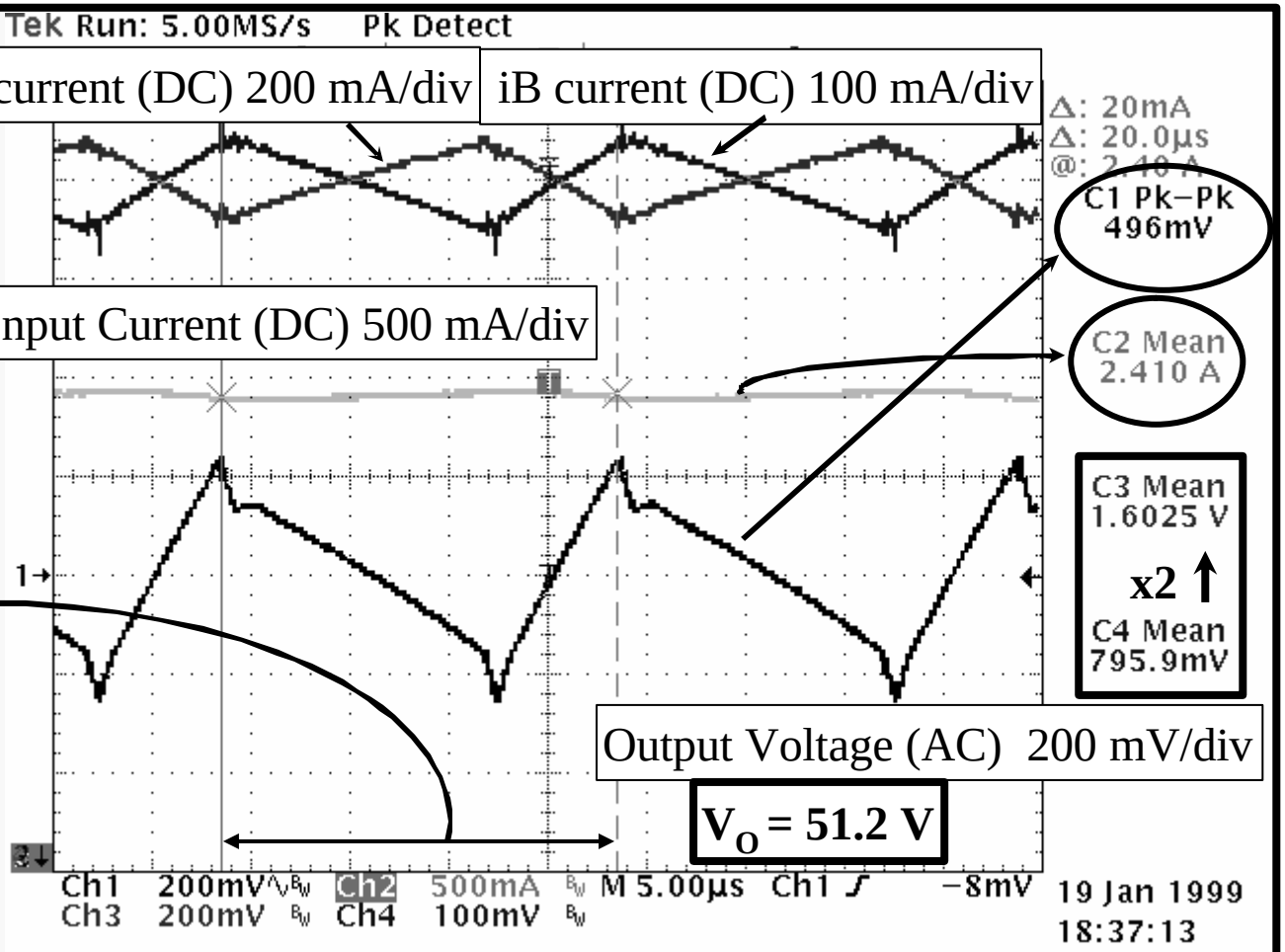
Co = 3 μF

**Di = 160 mA**

T = 20 μs

r = 33 mΩ

**D = 66.67%**



# Steady-State Experiments Summary

- Different $\alpha$ Values. $\alpha$ = 1, 1.5, 2, and 2.5
- Nominal Load Values of 50, 100 and 200 Ω
- Input Voltage Range : 9-16 V (in steps of 1 V)
  - Frequency Adjusted to 50 kHz for $\alpha$ = 1, 12 V, 100 Ω
- Input to Output Voltage Ratios of 4, 4.17, 4.5, 4.9
  - Maximum Errors of -5.5 V and + 3.2 V
  - Output Ripples from 80 to 770 mV
- Input Power Range: 6.5 W - 73.5 W
  - Efficiency Range: 82 - 89 %

**Not all combination**

**have been tested.**

**Max. 3 A per leg !**

# SCIDB SUMMARY

- New Step-Up Structure. $V_O \geq 4\, V_g$.
- Closed-Loop Sliding Mode Control Tested ($\alpha \geq 1$)
- Asymptotic Stability has been Analyzed
  - Local in the General Case (Small-Signal Perturbations)
  - Large-Signal for Quadruplier (Lyapunov 2nd Method)
- Experimental Performance: Efficiency 82-89 %
  - Output Voltage Ripple Increases with $\alpha$ (80-800 mV)
  - Very Small Input Current Ripple (worst case < 50 mA, 2 %)

# Conclusions and Future Research

- Introduction and Previous Works
- The Doubler Circuit
- The Triplier Circuit
- Multiplier Circuits
- The Modified Doubler
- The Quadruplier Circuit (SCIDB)
- Conclusions and Future Research

# CONCLUSIONS (I)

**Low-Ripple Voltage Multiplier Circuits with Good Dynamic Response Have Been Obtained.**

- **Complementary Activation of Switches**
- **Self-Oscillating Current-Mode Control Closed-Loop**
  - **Avoids High Circulating Currents**
- **Linear & Stable Sliding Dynamics N=2 (IDB-Doubler)**
- **Magnetic Coupling Adds a Design Freedom Degree**
- **Drawback: Unregulated Output Voltage**

# CONCLUSIONS (II)

## Increasing the Number of Converters

- **Generalization of CMC Strategy and Complementary Activation of Switches (N = 3: Triplier)**
- **Higher Number of Cells in Parallel**
  - **Main Limit of N is Given by the Duty Cycle**
  - **Frequency-Hysteresis Consideration**
  - **Other (N-1) Optimal Operating Points + Integration Possibility in Future Studies**

# CONCLUSIONS (and III)

**SCIDB: Switched Capacitor Interleaved Dual Boost derived from IDB + Classical Multiplier.**

- **Output Voltage $\geq$ 4 times the Input Voltage**
- **Sliding with $a=1$ : Low-Ripple Voltage Quadruplier with Stable in the Large and Quasi-Linear Dynamics**
  - **Experimental Need of Output Filtering**
  - **Wide Range of Possible Operating Points (Regulation?)**
  - **Experimental Results are in Good Agreement with Theory**

# Future Research (I)

- **Cascade Connection with Other Circuits**
  - **More Filtering and/or Voltage Regulation (TI-Buck)**
- **Expand the Circuit Structure:**
  - **Horizontally: More Cells in Parallel. Splits Input Power**
  - **Vertically: More Diodes & Capacitors. Increase of $V_O$**
- **Adapting the Circuit for Soft-Switching**
- **Consider other Types of Canonical Cells**

# Future Research (and II)

- **Study of Converters in DCM**
- **Conventional Interleaving without Complementary Activation of Switches but with Current-Mode Control**
- **Application of PWM Classical Techniques**
  - **Output Voltage Regulation of SCIDB using PI is in Progress**
- **Combination of Fast Current Inner-Loop and Voltage PI External Loop.**
  - **Sliding $S(x) = i_A - i_B - F(\text{voltage error}) = 0$**
  - **Equivalent approach in PWM**

Síntesis de Estructuras

Multiplicadoras de Tensión

Basadas en Células Convertidoras

Continua-Continua de Tipo Conmutado

***Thank you for your attention !***