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ENHANCEMENT OF DEFECT DIAGNOSIS BASED ON THE ANALYSIS OF CMOS DUT BEHAVIOUR

Tesi doctoral presentada per a l’obtenció del títol de doctor

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ABBREVIATIONS AND ACRONYMS

α	*Open location*
α'	*Carrier velocity saturation index*
β_1	*Regression line slope*
β_0	*Intercept point*
δ	*Delay*
ε	*Random error component*
ε_{ox}	*Oxide permittivity*
φ_{ox}	*Tunnelling barrier height*
$\eta(N_1,\ldots,N_l)$	*Pull-up ratio*
μ	*Mobility of carriers*
μ_n	*Mobility of carriers in an nMOS transistor*
μ_p	*Mobility of carriers in a pMOS transistor*
ATE	*Automatic Test Equipment*
C_{down}	*Parasitic capacitance between the floating net and a structure set to ground*
$C_{eq\text{-}d}$	*Equivalent downstream node capacitance*
C_{gb}	*Gate-to-bulk transistor parasitic capacitance*
C_{gd}	*Gate-to-drain transistor parasitic capacitance*
C_{gs}	*Gate-to-source transistor parasitic capacitance*
C_N	*Cross-coupled neighbouring capacitance*
$C_{SUBSTRATE}$	*Parasitic capacitance to substrate*
C_{up}	*Parasitic capacitance between the floating net and a structure set to power*
C_{WELL}	*Parasitic capacitance to well*
CMOS	*Complementary Metal-Oxide-Semiconductor*
d	*Distance*
DC	*Direct current*
DIBL	*Drain Induced Barrier Lowering*
DUD	*Device Under Diagnosis*
DUT	*Device Under Test*
E_{ox}	*Electric filed across the oxide*

ECB	*Electron Conduction-Band tunnelling*
EO	*Erroneous Observation*
EVB	*Electron Valence-Band tunnelling*
FF	*Flip-flop*
FIB	*Focus Ion Beam*
FN	*Floating Node*
FOS	*Full Open Segment*
FS	*Fail Scenario*
ft	*Falling transition*
GOS	*Gate Oxide Short*
h	*Planck constant*
$\hbar$	*Reduced Planck constant*
H	*Height*
HV	*High Voltage*
HVB	*Hole Valence-Band tunnelling*
I_b	*Bridge current*
I_d	*Downstream current*
I_{D0}	*Drain current at* $V_{GS} = V_{DS} = V_{DD}$
I_g	*Gate current*
I_{gb}	*Gate-to-substrate leakage current*
I_{gc}	*Gate-to-inverted channel leakage current*
I_{gcd}	*Gate-to-inverted channel leakage current collected by the drain*
I_{gcs}	*Gate-to-inverted channel leakage current collected by the source*
I_{gdo}	*Gate-to-drain leakage current through the overlap region*
I_{gso}	*Gate-to-source leakage current through the overlap region*
I_{IN}	*Addition of all the currents components flowing into and out of the floating node*
I_{OFF}	*Transistor off-state current*
I_{ON}	*Transistor on-state current*
I_t	*Total current cause by a bridging fault*
I_{DDQ}	*Quiescent power supply current*
IC	*Integrated Circuit*
$I(N_i)$	*0-1 value function depending on the logic value of* N_i
$I'(N_i)$	*Function for the effective crosstalk capacitances between nets*

ITRS	*International Technology Roadmap for Semiconductors*
J_{go}	*Gate tunnelling current density*
k	*Process parameter for MOS transistors*
k'	*Parameter that accounts for the influence of V_{DS} in the partition of the gate-to-inverted channel leakage current*
L	*Length*
L_c	*Critical length*
L_{CNi}	*Coupling length between the defective line and neighbouring line N_i*
L_{Fline}	*Floating line length*
M	*Matching*
m*	*Effective carrier mass*
m_o	*Free electron mass*
nMOS	*n-channel MOS transistor*
NW	*Network*
P	*Prediction*
pMOS	*p-channel MOS transistor*
ppm	*Parts per million*
PTM	*Predictive Technology Model*
q	*Charge of a free electron*
R^2	*Coefficient of determination*
R_b	*Bridge resistance*
R_c	*Critical resistance*
R_o	*Open resistance*
R_{on}	*On-resistance*
RN	*Resistive node*
ROBDD	*Reduce Ordered Binary Decision Diagrams*
rt	*Rising transition*
RTC	*Resistance Temperature Coefficient*
SA	*Stuck-at*
SA0	*Stuck-at 0*
SA1	*Stuck-at 1*
Seg_i	*Segment i*
Si	*Silicon*
SiO_2	*Oxide silicon*

SIO	*Silicon On Insulator*
SLAT	*Single Location At a Time*
SOC	*System On Chip*
SPICE	*Simulation Program with Integrated Circuit Emphasis*
SS_R	*Model sum of squares*
SS_{Res}	*Error sum of squares*
SS_T	*Total sum of squares*
STAT	*Single Test At a Time*
T	*Temperature*
T_{ox}	*Oxide thickness*
TH	*Thickness*
TP	*Test pattern*
V_{D0}	*Drain saturation voltage at* $V_{GS}=V_{DD}$
V_{DD}	*Power supply voltage*
V_{DS}	*Drain-to-source voltage*
V_{FLine}	*Floating line voltage*
V_g	*Gate voltage*
V_{GND}	*Ground voltage*
V_{GS}	*Gate-to-source voltage*
V_{IHmin}	*Minimum voltage applied to the input interpreted as logic high*
V_{ILmax}	*Maximum voltage applied to the input interpreted as logic low*
V_{LTH}	*Logic threshold*
V_{OHmin}	*Minimum voltage applied to the output interpreted as logic high*
V_{OLmax}	*Maximum voltage applied to the output interpreted as logic low*
V_{OX}	*Voltage across the oxide*
V_{Qo}	*Voltage due to the trapped charge*
V_{TH}	*Threshold voltage*
$V_{TH(nMOS)}$	*Threshold voltage of an nMOS transistor*
$V_{TH(pMOS)}$	*Threshold voltage of a pMOS transistor*
VLV	*Very Low Voltage*
W	*Width*
W_n	*Transistor width (nMOS)*
W_p	*Transistor width (pMOS)*

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CHAPTER 1.

INTRODUCTION

Nowadays, a single CMOS (Complementary Metal Oxide Semiconductor) Integrated Circuit (IC) may contain more than one billion transistors as well as billions of metal vias. Furthermore, transistor dimensions shrink with every new technology so that the ICs manufacturing process becomes more challenging. Due to the complexity of the process, it is not possible to assure that every part of the fabricated ICs will meet the expected specifications. Many failure mechanisms arise during the fabrication process, generating thus defects. Therefore, ICs are tested before being shipped to the customer. However, testing for every possible defect is not feasible due to the huge amount of time and resources required for that purpose. Instead, test generation relies on fault models, which try to represent physical defects by the behaviour they produce.

Once detected a faulty IC, it is important to know the location and the class of failure. This is the goal of fault diagnosis. The diagnosis procedure usually relies also on

fault models and a comparison algorithm. Fault diagnosis is a key factor in both failure analysis and yield improvement. On the one hand, failure analysis is the process using (electrical) and physical methods to determine the location and the class of failure. On the other hand, yield analysis tries to find systematic repeating defects. If these defects are located and characterized, they can be subsequently eliminated by taking proper corrective actions, improving the quality of the fabrication process.

1.1 MOTIVATION

Due to market pressure, there is an increasing need of reducing the time-to-market of a product. Hence, the industry is demanding the obtaining of low parts-per-million (ppm) in shorter periods. Furthermore, the development of smaller nanometer technologies arises new complex failure mechanisms, which will not be diagnosed by present diagnosis methodologies. Physical failure analysis, although indispensable, cannot afford these new challenges, since it requires extremely high cost equipment. For that reason, a detailed understanding and knowledge of defect behaviours is a key factor for the development of improved diagnosed methodologies, which should facilitate and shorten the time required for defect location.

1.2 OBJECTIVES

The goals of the present thesis are the following ones:

- Identification and analysis of existing and new failure mechanisms so that the excitation and observability conditions of defects present in CMOS devices can be predicted.
- Development of new diagnosis methodologies based on low cost techniques which improve the accuracy of the results reported by the diagnosis tool from *NXP Semiconductors*.

For these purposes, extensive analytical and simulation work has been done. Furthermore, experimentations with defective devices from different technologies (0.35 μm from *AMS* and 0.18 μm and 90 nm technologies from *NXP Semiconductors*) have been carried out to demonstrate the feasibility and usefulness of the diagnosis methodologies developed in the present work.

1.3 OVERVIEW

This thesis is composed of five more chapters, which are described next:

- In Chapter 2, the state of the art of fault models and diagnosis methodologies for the location of defects in CMOS technologies is reviewed.
- Chapter 3 focuses on bridging faults. The characterization of this class of faults is presented in the first part of the chapter. Next, a new diagnosis methodology for bridging faults based on current information is introduced. Its application is experimentally demonstrated. Finally, the effectiveness of shmoo plots for diagnosis purposes in the presence of bridging faults is analyzed in the last part of the chapter.
- The work based on interconnect open faults is developed in Chapter 4. The chapter begins with the characterization of interconnect open defects by means of analytical work and an experimental chip designed and fabricated in a 0.35 µm technology. Based on these results, a diagnosis methodology is proposed for a more accurate localization of interconnect full open defects along the defective nets. Finally, the impact of tunnelling leakage currents on the behaviour of interconnect full open defects concludes this chapter.
- Chapter 5 summarizes the experimental results of the methodologies presented in Chapter 3 and 4 applied to faulty industrial devices belonging to 0.18 µm and 90 nm technologies of *NXP Semiconductors*.
- Finally, Chapter 6 presents the conclusion of the thesis and the possible future research directions derived from the development of the work.

CHAPTER 2.

STATE OF THE ART

Most of diagnosis methodologies are composed of two main elements, namely: a fault model and a comparison algorithm. Hence, in the first part of the chapter, a review of fault models is presented. The second part describes the evolution of the matching algorithms for diagnosis purposes. Furthermore, some diagnosis methodologies, which are not made up of a fault model and a comparison algorithm, are also commented at the end of the chapter.

2.1 FAULT MODELS

Fault models are simplifications that try to represent physical defects by the behaviour they produce. Fault models are a key factor in ICs testing and fault diagnosis. Although fault models have been improved during the last years, extensive work is still required for the development of new fault models which overcome the paradigms arisen

with nanometer technologies. A review of the main fault models are described in the next subsections.

2.1.1 STUCK-AT FAULTS

The stuck-at (SA) fault model is the first and the most widely studied and used fault model [1]-[2]. It had great success in bipolar circuits. For that reason, it gained acceptance also in CMOS technologies. The SA fault model assumes that a line or a node in the circuit is always set to a fixed logic value, either logic 1 or logic 0. Therefore, the faulty line or node is said to be stuck-at 1 (SA1) or stuck-at 0 (SA0). The physical defect related with this model is a short between the faulty line and a power supply (V_{DD}) or ground (V_{GND}) rail, as illustrated in Figure 2.1.

Although the use of the SA fault model has gathered good results, it does not properly represent the behaviour of physical defects. Real defects are much more complicated. For the majority of them, more sophisticated fault models are required. Anyway, although inaccurate for CMOS technologies, the SA fault model has different advantages: it has easy computational efficiency, it can represent different physical defects and can be used to model other type of faults.

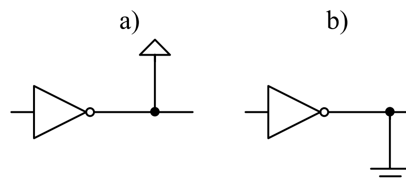

Figure 2.1. SA fault at the output of an inverter a) SA1 b) SA0.

2.1.2 BRIDGING FAULTS

A bridging fault assumes the electrical connection between two signal nets, which should not be connected by design [2]. Bridges are divided into two groups: external and internal bridges. On the one hand, external bridges are bridging faults between any logic gate inputs, outputs, V_{DD} or V_{GND}. On the other hand, internal bridges involve two nets within a logic gate or module, or an internal net and an input, output, V_{DD} or V_{GND} of the same gate. Figure 2.2 shows an example of an external bridge between the output of an inverter and V_{DD}. Assuming an ideal short (negligible bridge resistance R_b), when V_{IN} is set to a low logic value, the pMOS transistor is on and the nMOS transistor is off. Both, the pMOS transistor and the bridge pull the output of the inverter to logic 1. When V_{IN} is set to a high logic state, the nMOS transistor is on and the pMOS transistor

is off. Nevertheless, the bridging fault still pulls up the output of the inverter to logic 1. As the nMOS transistor is on, there is a conducting path created from V_{DD} to V_{GND}. In a similar way, Figure 2.3 illustrates an internal bridge in a 2-input NAND gate.

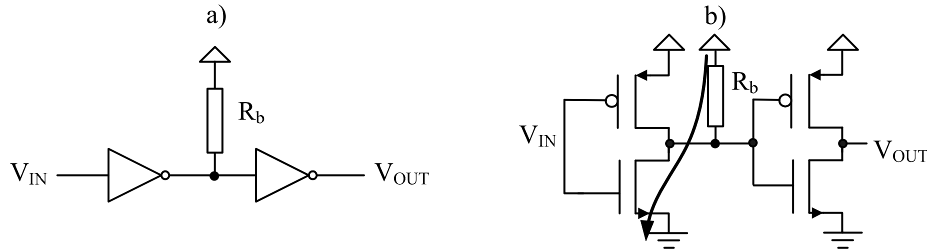

Figure 2.2. External bridge at the output of an inverter a) Gate level b) Transistor level.

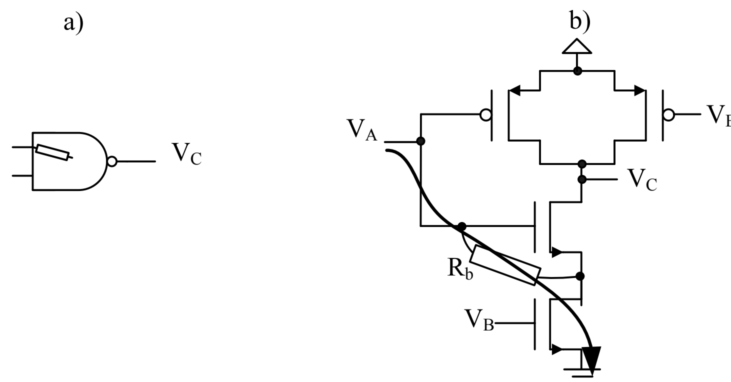

Figure 2.3. Internal bridge in a NAND gate a) Gate level b) Transistor level.

2.1.2.1 BYZANTINE GENERAL'S PROBLEM IN BRIDGING FAULTS

Different factors affect the behaviour of bridging faults, namely: the nMOS and pMOS network strengths driving the bridged nodes, the bridge resistance (R_b) and the input logic thresholds (V_{IHmin} and V_{ILmax}) of the gates driven by the bridged nets. The latter is important since for the same voltage value on the defective net, the gates driven by the bridged nets (downstream gates) can interpret it differently if they do not have the same logic threshold voltages. It is the so-called Byzantine General's problem [3]. An example is illustrated in Figure 2.4, where the outputs of two 2-input NAND gates (*NAND1* and *NAND2*) are connected by means of a bridge. If the excitation of the bridge causes V_A to be set to an intermediate value, the downstream gates (*INV* and *NAND3*) may interpret V_A in different ways. For instance, assuming the logic thresholds follows that $V_{IH\min(INV)} < V_A < V_{IL\max(NAND3)}$, then V_A is interpreted as logic 1 by *INV* and as logic 0 by *NAND3*.

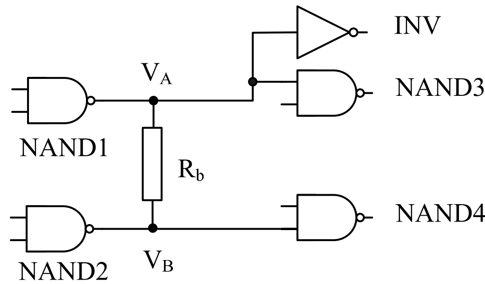

Figure 2.4. Byzantine General's problem due to a bridging fault.

2.1.2.2 BRIDGING FAULT MODEL EVOLUTION

The first bridging fault models were introduced by Mei in [2]. These bridging fault models are known as the wired-AND and the wired-OR bridging fault models. In a bridging fault, each signal net tries to drive the bridged nets to a value equal to the logic value in the fault-free circuit. The wired-AND and the wired-OR fault models assume that the values on the bridged nets are both the same (zero bridge resistance) and are the result of an AND or an OR operation between the logic values of the nets, respectively. Figure 2.5 shows an example of a bridge between the outputs of two NAND gates and their equivalent wired-AND and wired-OR fault models. On the one hand, the wired-AND fault model assumes that the nMOS transistor networks logically win and drive the bridged nets when they are excited. On the other hand, the wired-OR fault model considers that the pMOS transistor networks logically win when they are excited. These fault models, although widely used in the past, do not reflect the behaviour of bridging faults in CMOS technologies. The voltage on the bridged nets is not always logic 0 or logic 1, as the wired-AND and the wired-OR fault models assume. These fault models are more suitable for technologies where one of the logic levels is clearly stronger than the other one. However, the wired-AND and wired-OR fault models are the easiest for simulation, pattern generation and diagnosis purposes.

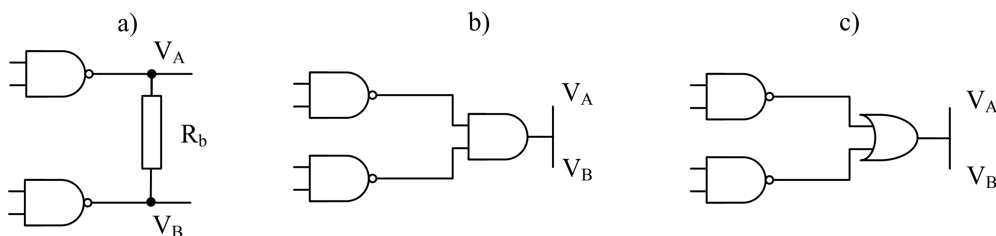

Figure 2.5. Two NAND gates a) Bridging fault b) Wired-AND c) Wired-OR.

A more complex fault model than the wired-AND and the wired-OR fault models was subsequently presented by Acken and Millman, the voting model [4]. When the bridged nets are set to opposite logic values, the voting model considers the resultant

circuit as a resistive divider between V_{DD} and V_{GND}. In CMOS circuits, the electrical resistance to V_{DD} comes from a combination of conducting pMOS transistors, whereas the resistance to V_{GND} comes from a combination of conducting nMOS transistors. The voting model also assumes that the bridge resistance is negligible. The evaluation of the two networks strengths determine whether the net is considered as logic 1 or logic 0. Nevertheless, this fault model does not determine the actual values on the bridged nets. Considering the transistor description of the bridge between the outputs of two 2-input NAND gates illustrated in Figure 2.6, the voting model differentiates between the strengths of the pMOS networks depending on the number of conducting pMOS transistors to determine the logic interpretation of the bridged nets. The voting model evaluates the relative strengths of the different networks by means of SPICE simulations, which are stored in tables. During fault simulation, this information is accessible and no SPICE simulations are required. In a first approach, the model assumes that all the downstream gates have the same threshold. However, the same authors refined this fact in [5]. The limitation of this fault model is that if any new logic element has a threshold voltage outside the range used to generate the tables, new simulations are required. Furthermore, results when the strengths of the pMOS and nMOS networks are similar are not accurate. To overcome the limitations of the voting model, an improved fault model was proposed by Maxwell and Aitken, the biased voting model [6]. In this case, the threshold voltage is not considered fixed. The biased voting model is able to calculate the voltage values of the bridged nets by means of an iterative procedure.

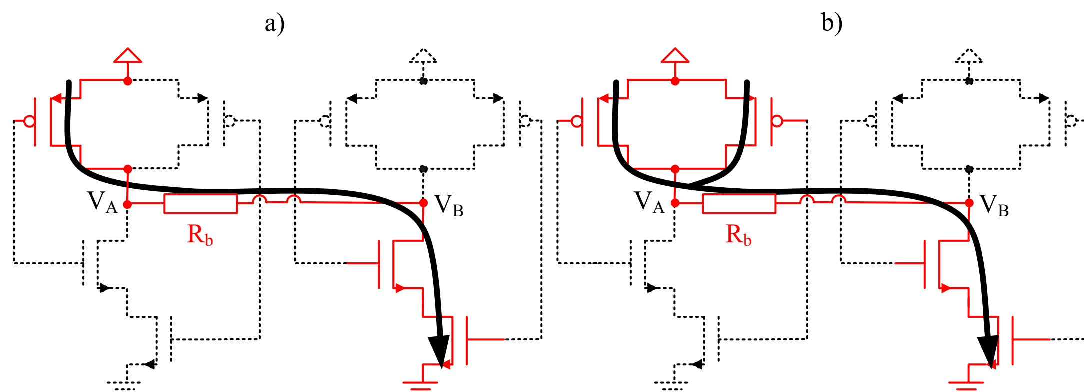

Figure 2.6. Transistor description of a bridging fault between two NAND gates a) One pMOS transistor on b) Both pMOS transistors on.

Other works tried to develop more accurate fault models. Rearick and Patel presented in [7] a fault model where the use of SPICE-derived data for every input of the bridged gates is taken into account. A different approach was presented by Di and Jess [8], who proposed a method based on Faulty Boolean Expressions in order to calculate the voltage of the bridged nodes. For that purpose, a simplified transistor model is used.

So far, none of the models has taken the value of the bridge resistance into consideration. All of them assumed it negligible. Although most of bridging defects have low resistance values, based on some measurements carried out on process-related defect monitoring wafers, Rodriguez-Montañés et al. reported in [9] that there are a non-negligible percentage of bridges with significant resistance (in the range of 500Ω to 20kΩ). Some recent models took then the bridge resistance into account, e.g., the one presented by Renovell et al. [10]. This fault model determines the voltage of the bridged nets based on equations describing the operation of MOS transistors. Due to different approximations, the model is not very accurate when the values are not close to $V_{DD}/2$. In the presence of a zero bridge resistance, both nets have the same voltage value and the circuit exhibits faulty logic behaviour. However, as the bridge resistance increases, the voltage of the bridged nets gets closer to the defect free value so that for high resistance values, the circuit operates properly. In this way, there is a critical resistance value (R_C) above which the circuit does not show faulty logic behaviour [11]. This behaviour is illustrated in Figure 2.7. Suppose that the bridge in Figure 2.7a is excited in such a way that V_A is set to logic 1 in the defect free case, whereas V_B is set to logic 0. The plot in Figure 2.7b represents the voltage of the bridged nets as a function of the bridge resistance. For a zero bridge resistance, both V_A and V_B have the same value. However, as R_b increases, V_A increases and V_B decreases, to the point that R_b is so high that V_A is properly interpreted by *NAND3* ($R_{C(NAND3)}$), and for a higher resistance V_B is also properly interpreted by *NAND4* ($R_{C(NAND4)}$). Therefore, when $R_b < R_{C(NAND3)}$, logic errors are propagated through both *NAND3* and *NAND4*. When $R_{C(NAND3)} < R_b < R_{C(NAND4)}$, logic errors are propagated through *NAND4*. Finally, when $R_b > R_{C(NAND4)}$, the circuit does not show faulty logic behaviour.

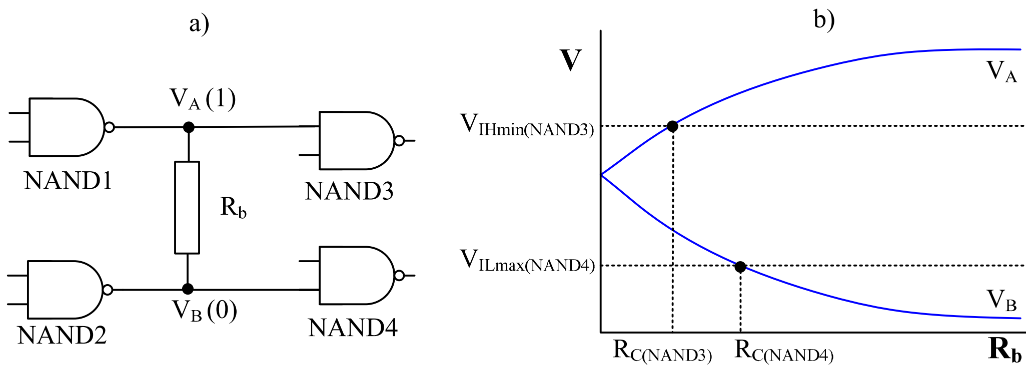

Figure 2.7. Resistive bridge between two NAND gates a) Gate level b) V-R_b characteristic.

A detailed analysis of the behaviour of bridging defects was presented by Sar-Dessai and Walker in [12]. This work analysed five different bridging fault configurations, namely: a bridging fault between two primary inputs, between a primary input and a gate output, between two gate outputs, between two gates outputs driving the same gate and between two primary outputs. Based on the model for these five configurations, look-up tables can be constructed, where the information about the voltage on the bridged nets is stored for every vector. The detectable resistance interval [11] and the propagating path are also taken into account. Furthermore, it is also determined whether the bridging fault is detectable at the driven gate outputs based on their logic thresholds. In a more recent work carried out by Polian et al. [13], the critical resistance was calculated based on more accurate transistor models: the Fitted Model, which uses equations with free variables that are fitted in order to match actual SPICE data, and the Predictive Model, which is fully analytical and employs BSIM4 equations.

The characterization of bridging faults can be also based on electrical current information instead of looking the logic behaviour [14]. The easiest model is the so-called simple I_{DDQ} bridging fault model. It assumes that when the bridged nodes are set to the same logic value related to the defect free case, no extra current is added. However, when they have different logic values, a current path is created between power and ground and extra current is generated. An example is illustrated in Figure 2.8a. The inverter contains a bridge between the source and the gate of the pMOS transistor. When the inverter input (V_A) is in a high logic state, the nMOS transistor is on. The current consumption is only due to leakage current, as described in Figure 2.8b. However, if V_A transitions from logic 1 to logic 0, the nMOS transistor turns off and the pMOS transistor turns on. In the fault free case, once all the signals have settled-down,

the current consumption is again the leakage current. Nevertheless, due to presence of the bridge, during the low logic state of V_A, there is current flowing from the source to the gate of the pMOS transistor, increasing the quiescent current value.

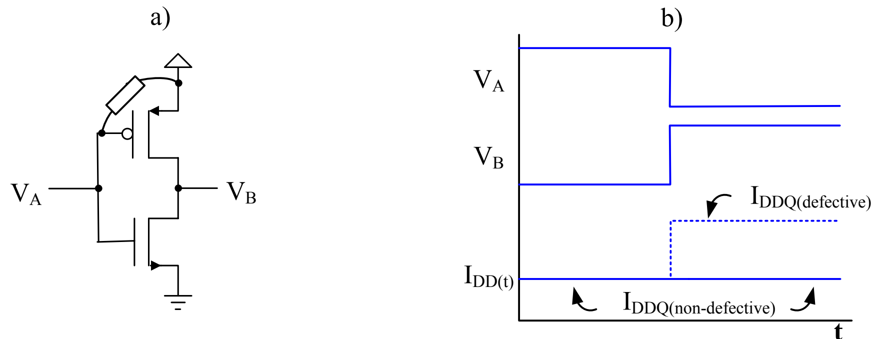

Figure 2.8. Bridge affecting the pMOS transistor of an inverter a) Gate level b) $I_{DD(t)}$.

The current behaviour of bridging faults can be more accurately described if the concept of the voting model is adapted to the current behaviour. Every network excitation is expected to add different currents values, as illustrated in Figure 2.9. The extra current depends on the number of pMOS transistors of the NAND gate in the on state when the bridge is excited.

The extensive work carried out to characterize bridging faults has improved their models since their appearance. However, more research is still needed, since some cases have not been yet fully solved. Transistor parameters and bridge resistances are susceptible to process variation, which are difficult to predict and influence the behaviour of this class of faults. Feedback bridging faults are still difficult to detect. Furthermore, bridging faults involving more than two nets are not considered by present fault models.

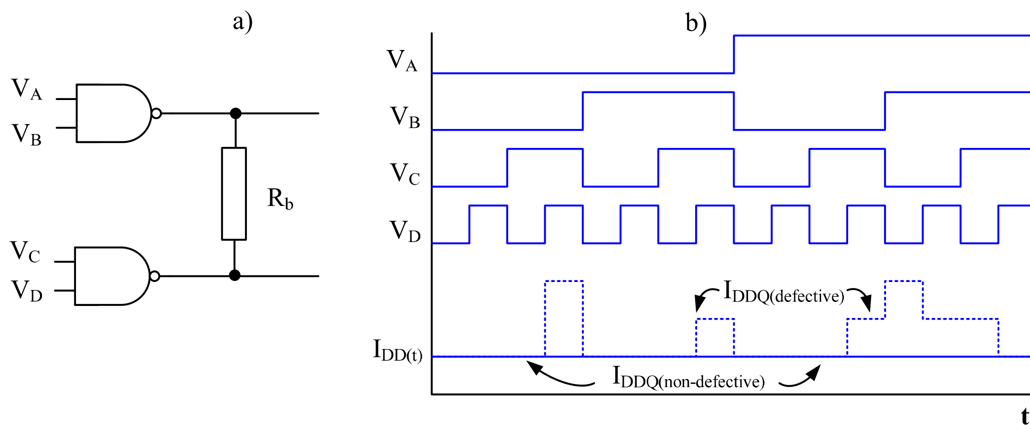

Figure 2.9. Bridge affecting the outputs of two NAND gates a) Gate level b) $I_{DD(t)}$.

2.1.2.3 FEEDBACK BRIDGING FAULTS

A feedback bridging fault is a bridging fault such that both involved nets lie on the same path in the circuit [2]. The voltage value of one bridged net may depend on the value of the other bridged net. The bridged net with lower topological ordering is usually called the back net, while the other one is called the front net. The analysis of feedback bridging faults is complex. They can induce sequential behaviour in combinational circuits, depending whether the path is sensitized or not and depending also on the topological situation of the bridge. Thus, three different cases may appear [15]-[18]:

1. The logic path is not sensitized.
2. The logic path is sensitized and the feedback loop has an even number of inversions.
3. The logic path is sensitized and the feedback loop has an odd number of inversions.

When the logic path is not sensitized, it is equivalent to a non-feedback bridging fault. The logic value of the back net is independent of the logic value of the front net. Considering the examples shown in Figure 2.10, this is accomplished as long as V_C is set to logic 0.

If the logic path is sensitized and the feedback loop has an even number of inversions, both nets have the same logic value. An example is illustrated in Figure 2.10a provided that V_C is set to logic 1. This case is redundant as long as the back net is stronger than the front net, otherwise a circuit with asynchronous memory behaviour appears. It can be then described as a latched state. The voltage on the bridged nets depends on the transistor strengths and the bridge resistance. The detectability of such fault cases relies on the sequence of test patterns applied.

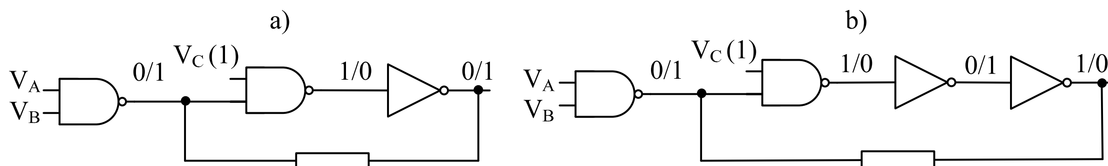

Figure 2.10. Feedback bridge a) Even number of inversions b) Odd number of inversions.

Finally, if the logic path is sensitized with an odd number of inversions, the logic values of the bridged nets are opposite on a fault-free circuit (see Figure 2.10b). Two different behaviours may appear depending on the gate strengths. If the back gate is stronger than the front gate, it behaves as a non-feedback bridging fault. However, if the front gate is stronger, the defect may cause oscillation in the circuit. The oscillation

period is related to the delay of the logic connecting the bridged nodes and it is usually lower than the clock period.

The impact of the bridge resistance in feedback bridges is not a trivial issue, since it turns out to be computationally complex [19]. However, bridge resistances with high values usually result in fewer situations of active feedback because the dominance conditions of the front net are less likely to be accomplished.

2.1.2.4 GATE OXIDE SHORTS (GOS)

Gate Oxide Shorts (GOS) may be considered as a particular class of bridging faults. GOS are intra-transistor bridges caused by hard transistor oxide breakdowns from particles or oxide imperfections [20]. In a defect-free transistor, the polysilicon gate is electrically isolated from the rest of terminals by means of a thin layer of silicon dioxide (SiO_2). A GOS is a rupture in this silicon dioxide, connecting the gate terminal with one of the silicon structures beneath the oxide. The electrical properties of a GOS depend on their location, since there are three different regions to which the gate can be connected. In this way, a GOS may connect the polysilicon gate terminal with the drain, source or bulk of the device. Furthermore, the doping type of the connected silicon structures affects the electrical properties of the GOS. When the polysilicon gate and the diffusion are of the same doping type, the electrical characteristic of the junction is ohmic. However, when they are of different doping type, the electrical model is a pn junction diode between both terminals.

The GOS fault model depends on the semiconductor structures taking part in the fault. From here on assume that the polysilicon gate doping is n-type, which has been the more common doping type for long-channel technologies. Anyway, the GOS behaviour with p-doped polysilicon gate can be deduced from the complementary behaviour assuming n-doped polysilicon gates. Therefore, the behaviour of a GOS between the p-doped polysilicon gate and the bulk of a pMOS transistor can be derived from the behaviour of a GOS between the n-doped polysilicon gate and the bulk of an nMOS transistor, as observed in Figure 2.11 [20]-[21].

An n-doped polysilicon gate to drain/source GOS in nMOS transistors generates an ohmic connection. The behaviour is similar to an external bridge between both terminals.

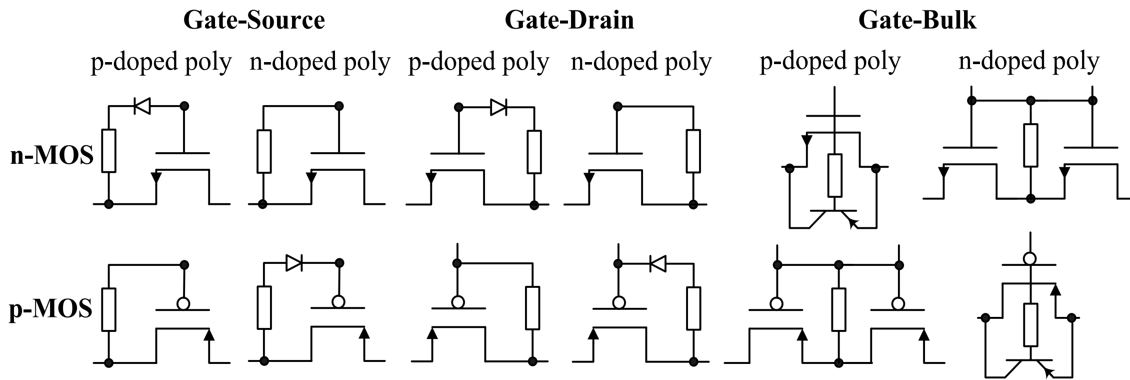

Figure 2.11. Electrical models for Gate Oxide Shorts [20]-[21].

A gate to bulk GOS present in nMOS transistors results in a diode with the anode at the bulk and the cathode at the gate. Under normal operation, the diode is expected to be reversed biased, adding negligible current. However, a parasitic nMOS transistor forms. The transistor with the GOS behaves in a similar way as two minor transistors connected in series with a resistance between the gates and the common terminal of both transistors. Figure 2.11 shows the equivalent electrical model for this case.

A GOS defect between the gate and the source/drain of a pMOS transistor forms a parasitic diode between both terminals, being the gate the cathode and the source/drain the anode of the diode. On the one hand, a GOS to the source of the pMOS transistor clamps the gate voltage to a diode drop below V_{DD} when the preceding stage is trying to set the gate to a low logic value. Otherwise, the diode is reverse biased, adding negligible current. On the other hand, the behaviour of a GOS to the drain of the transistor is more complicated. The diode acts as a feedback element from the drain to the gate of the transistor.

In case of a GOS between the gate and the bulk of a pMOS transistor, a resistive ohmic contact forms. However, once the transistor is switched on, the parasitic GOS resistance allows base terminal current injection in the parasitic bipolar transistor. In this case, the gate current acts as the base current for the parasitic bipolar transistor.

As GOS behaviour depends on its location, fault models considering its exact location have been developed. Sytrzycki [22] presented an approach which relies on designing the transistor physics-based model by means of lumped-elements. In this way, a non-defective channel is represented by a bi-dimensional array of MOS transistors. One can arbitrary choose the number and size of elements. The higher the number of elements, the most accurate the model. However, more computational effort is required.

This model allows placing a GOS model from Figure 2.11 close to the specific region of interest within the channel as well as to control the dimensions of the defective part of the channel. Thereby, it is possible to model different GOS mechanisms that may arise in any part of the channel. Finally, in a more recent work, Renovell et al. [23] analyzed the behaviour of GOS defects and the effectiveness of the model based on lumped elements.

2.1.2.5 BRIDGING FAULTS OBSERVABILITY

For testing and diagnosis purposes, measurements should be optimized based on the class of defect we are looking for. In this way, the conditions under which measurements are obtained and the post-processing of experimental data are important to make defects more observable. In case of bridges, different techniques have been developed to improve their observability. One of the most common techniques is lowering the power supply voltage below the normal operation value. In fact, this technique has been demonstrated to detect defects which are not detected by means of other test techniques [24]-[25]. Different works reported the effectiveness of lowering the power supply in logic tests when detecting bridges. Hao and McCluskey stated in [26] that Very Low Voltage (VLV) logic testing is suitable in order to detect resistive bridges. Other works also reported that lowering V_{DD} is appropriate to detect bridges [27], since the critical resistance (the highest bridge resistance which can be detected by means of logic tests) increases as V_{DD} decreases [28]. Chao-Wen et al. proposed in [29] a different concept when lowering the power supply value. It is the concept of $V_{DDMIN.}$ This technique consists of, at a given clock frequency, decreasing the V_{DD} value until obtaining the minimum V_{DD} at which the device still functions. This work showed that some defective devices had a higher V_{DDMIN} than the fault free ones. In general, lowering the power supply value is easy to implement, since it does not require any extra equipment or performance. However, it decreases circuit speed. Thus, there is an increase in test time because the clock frequency is lower than at nominal conditions.

Bridges may cause intermediate voltages. These behaviours cannot be observed by means of voltage-based techniques, since these intermediate voltages are lately restored by successive gates. However, current-based techniques are demonstrated to be effective in such cases. The first and most popular current based technique is the quiescent power supply current (I_{DDQ}) testing. In the steady state, when all switching

transients are settled-down, CMOS circuits have ideally no current consumption, since leakage current is negligible. The presence of some class of defects may form a conduction path from power supply to ground, generating an elevated current, orders of magnitude higher than the defect-free leakage value. The idea is monitoring the power supply current (I_{DDQ}) once all the transient currents in the circuit have settled-down. The measured current is then compared to a threshold value. If the current value is higher than the threshold limit, the device is considered faulty. I_{DDQ} testing was proposed by Levi in [14], subsequently formulated by Malaiya and Su in [30] and by Acken in [31] for the detection of bridging faults. The effectiveness of I_{DDQ} testing was reported in different works [32]-[34] to detect different bridging defect classes, such as interconnect bridges, gate oxide shorts and inter-gate shorts.

I_{DDQ} testing provides high observability. It requires only fault sensitization, since the fault-effect is always observable through the power supply current. Hence, the fault propagation effort during test generation is not needed unlike logic based techniques. However, with the shrinking of minimum feature size for every new technology, there is great concern related to the usefulness of I_{DDQ}. The theoretical basis of I_{DDQ} is based on the estimation of the leakage current in a defect-free circuit and then setting a threshold limit above which a circuit is considered defective. Due to statistical variations, the distribution of the device current consumption is Gaussian. Thus, the threshold limit is set much higher than the mean. Assuming also a Gaussian distribution for the defective devices, if both distributions are far enough, an easy distinction is made between defect-free and defective devices. However, the leakage current increases in an exponential way for every new technology, as described in Figure 2.12 [35]. Therefore, it has become comparable or higher than the defect current. The current mean value of the distribution of the fault-free devices increases and gets closer to the mean of the defective devices, overlapping both distributions. Thereby, it becomes more difficult to determine whether a variation in the I_{DDQ} value is due to the leakage current or due to a defect. Furthermore, I_{DDQ} testing has also the drawback of speed when measuring quiescent current, which is lower related to other test techniques. Anyway, this is partially solved because the required number of vectors is lower than the ones required in voltage based techniques.

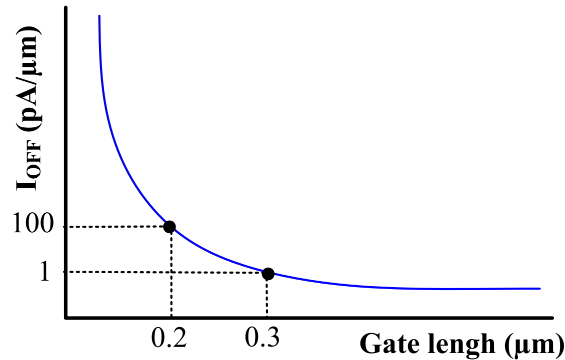

Figure 2.12. Evolution of leakage current [35].

Some solutions have been proposed in order to overcome the leakage problem [36]-[39], namely: lowering test temperature, controlling the back vias voltages, partitioning the device using multiple power sources, multiple transistors thresholds or Silicon On Insulator (SOI) technologies for a sharper sub-threshold swing.

Some techniques based on the post-processing of I_{DDQ} data have also been developed to extend the effectiveness of I_{DDQ}. One of these techniques is delta I_{DDQ} [40]-[42]. This method is conceptually the same as I_{DDQ}. However, instead of observing the absolute value of the power supply current, delta I_{DDQ} considers the difference of the power supply current among successive test vectors. This difference is treated probabilistically to determine if the circuit is defective or not.

Another technique is current signatures, which was proposed by Gattiker and Maly [43]. The measured I_{DDQ} value is not compared to a single limit value, but it is measured the current for the whole test set [43]-[44]. A current signature is generated by ordering all the obtained measures from the smallest to the highest value. This technique looks for jumps in the current signature, which indicates some kind of defect in the device. In case of bridges, the number of jumps may give information about the number of network excitations that have been activated. In Figure 2.13 it is shown the I_{DDQ} values for a real 0.18 µm defective device. On the one hand, Figure 2.13a shows the I_{DDQ} values in the same order as in the test procedure. On the other hand, the values are ordered in Figure 2.13b. Notice that different jumps are observed for the current signature of the defective device. Current signatures avoid the problem of I_{DDQ} and delta I_{DDQ} testing when deciding the current threshold limit.

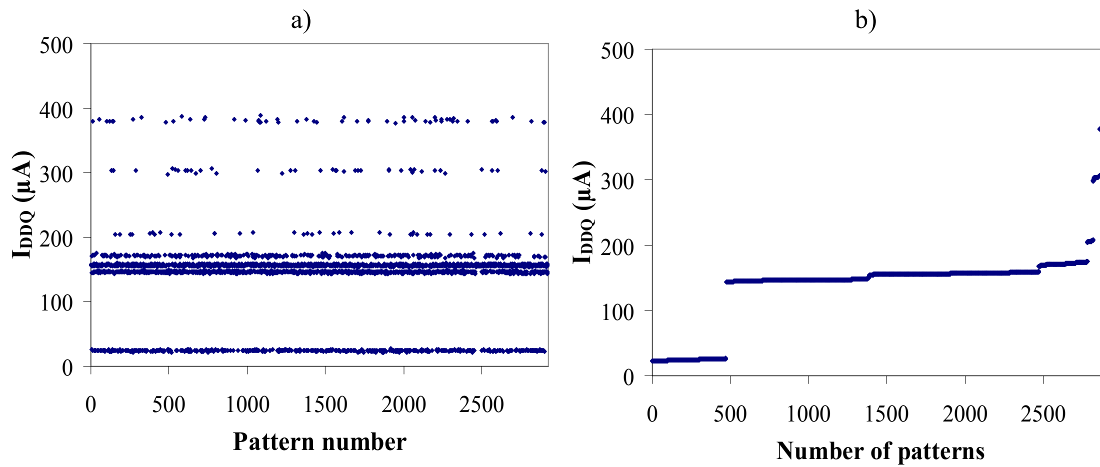

Figure 2.13. I_{DDQ} test for a real 0.18 µm defective device a) Non-ordered b) Current signature.

The current ratios technique [45] is based on the same idea as current signatures, but adding tolerating parameter variations. The basis is that the slopes of the rank-ordered current signatures for dies having differences in the absolute I_{DDQ} values are quite similar. Therefore, it is possible to set a test limit based on the ratio of the maximum to minimum I_{DDQ} value. This value is more or less constant and independent of the mean of the I_{DDQ} measurements for each die. This ratio is determined by means of an iterative process. Once obtained the ratio, the vector which typically gives the minimum current is identified. The current for that vector is measured. Subsequently, the maximum current is computed due to the ratio previously obtained. Outliers are then identified.

Temperature may also give additional information to detect bridges which are not observable at nominal conditions. Resistive bridges are temperature sensitive because their electrical resistance varies with temperature [46]. Bridge materials having a positive resistance temperature coefficient (RTC) such as metals and polysilicon increase their resistance at high temperatures. Thereby, at low temperatures the bridge resistance induces higher I_{DDQ} values. Furthermore, the probability of inducing faulty logic behaviour is also higher. Some works provided experimental results where testing at two different temperatures was useful to detect device outliers [47]-[48]. However, there are some drawbacks when introducing temperature in the production environment. It is time consuming and expensive, especially for cold temperatures, which requires specialised equipment.

2.1.3 OPEN FAULTS

An open is missing material causing an electrical discontinuity in metal, polysilicon or diffusion regions. The properties of the open depend mainly on [49], namely: defect location, local electrical structure and defect nature, as summarized in the next subsections.

2.1.3.1 DEFECT LOCATION

Based on the location of the open, it can be categorized into four different groups [50]-[51], as illustrated in the examples in Figure 2.14:

1. Interconnect open: It is localized in the interconnect wiring, resulting in gate inputs being partially or totally disconnected from their drivers.
2. Network open: It is inside a cell, affecting the connection between the drain and the source of transistors.
3. Open inside a cell: It affects the connection between the bulk of an nMOS transistor and V_{GND} or the bulk of a pMOS transistor and V_{DD}.
4. Open disconnecting a single transistor gate and its driver.

In nowadays technologies with more than six metal layers, the interconnect wiring is the most likely place for an open, as derived from the critical area analysis [52]. Vias are also susceptible to breaks [53], since the number of vias exceeds the number of transistors in most designs.

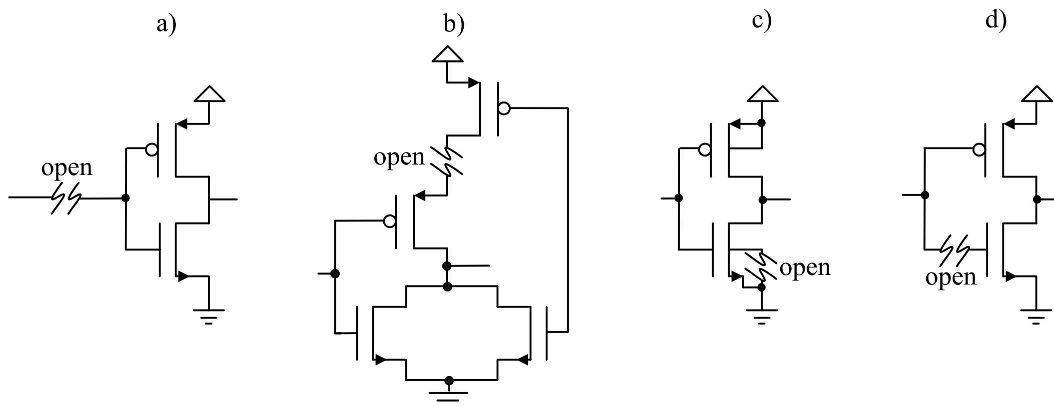

Figure 2.14. Open categories a) Interconnect b) Network c) Inside a cell b) Disconnecting a single transistor.

2.1.3.2 LOCAL ELECTRICAL STRUCTURE

An open can be classified into two different groups based on its electrical nature: full open and resistive open. When the lack of material causes a discontinuity eliminating the electrical connection between the two end points of the fault, it is said to

be a strong or full open. On the other hand, if the discontinuity does not cause a complete disconnection, the open is said to be resistive or weak open. Although the majority of opens present in metal lines belongs to the class of strong opens, a non negligible amount of them lies in the low resistive range, as reported by Rodríguez-Montañés et al. in [54].

The electrical behaviour of opens in interconnect lines differs depending on its strong or weak (resistive) nature. In a full open, a floating net is generated and its behaviour depends on local electrical structures [51], [55]-[59], namely, (a) the capacitances between the floating net and its neighbouring lines, substrate and well, (b) the transistors capacitances to the floating net and (c) the trapped charge on the floating structure. As technology dimensions decrease, the width (W) of the interconnect lines shrinks also. Considering the inverse increase of the resistance with the transversal section of the wire, the area (WxH) is kept within reasonable high values. As a result, the height increases for every new technology. Subsequently, the aspect ratio (the relationship W/H) has been decreasing over the last years and has crossed below unity for high metal levels. This fact has caused an increment in the influence of coupling capacitances between lines in a circuit and it is expected to increase in the future.

In order to characterize the behaviour of a floating line, suppose the example illustrated in Figure 2.15 (n-well technology). A metal track contains a break generating a floating line. Furthermore, three neighbouring metal tracks are routed close to the defective one. Notice that neighbours may be in the same or at different metal layers. The parasitic coupling capacitances affecting the floating line are shown in Figure 2.15, namely: the parasitic capacitances to the ground ($C_{SUBSTRATE}$) and the power plane (C_{WELL}) and the coupling capacitances to the three neighbouring lines (C_{N1}, C_{N2} and C_{N3}). The value of the capacitances depends on the dielectric filling the space, the distance between lines and the physical dimensions of the lines.

Another set of capacitances influencing the interconnect line is made up of the transistor capacitances connected to the floating wire. These capacitances are driven by the open line and consist of gate_drain (C_{gd}), gate_source (C_{gs}) and gate_bulk (C_{gb}) capacitances. These transistor capacitances are shown in Figure 2.16a for the particular case of an inverter as the next driven stage. Notice that the bulk terminals of pMOS and

nMOS transistors are connected to V_{DD} and V_{GND}, respectively. The values of these transistor parasitic capacitances vary with the conduction state of the transistors.

A third important factor in the final behaviour of the open line is the trapped charge in the floating structure. The trapped charge is an unknown parameter and is difficult to predict. Previous published works [57], [60]-[61] evaluated this influence. Johnson [60] presented measurements of the trapped charge performed on test structures consisting of floating-gate transistors with different polysilicon length extensions. These measurements showed always a positive charge on the floating polysilicon, generating voltages ranged from 0.1 to 2.3 V. However, Konuk and Ferguson [61] presented measurements in a 0.18 μm n-well technology with positive as well as negative trapped charge values, down to -4 V.

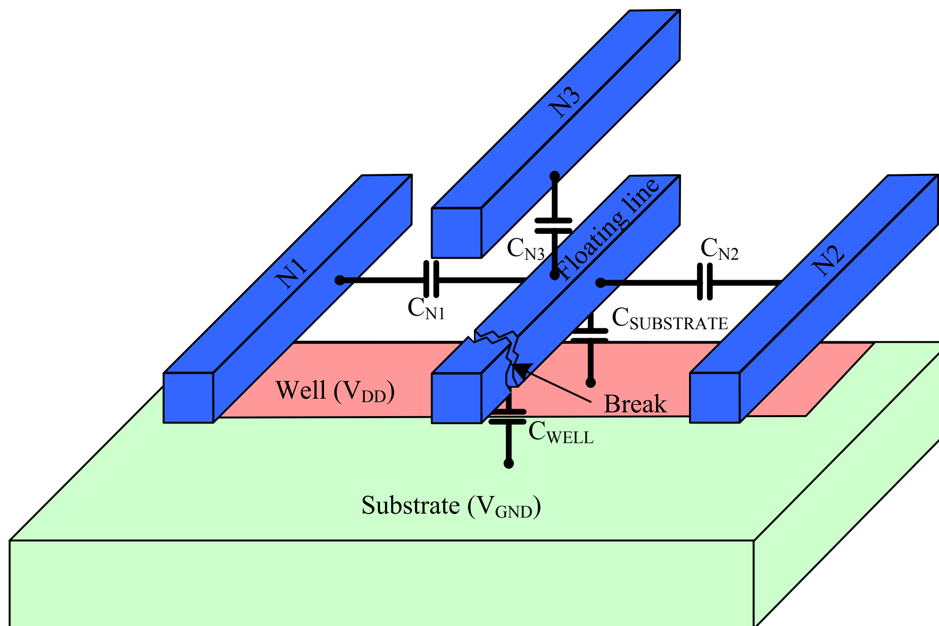

Figure 2.15. Parasitic coupling capacitances to the floating line.

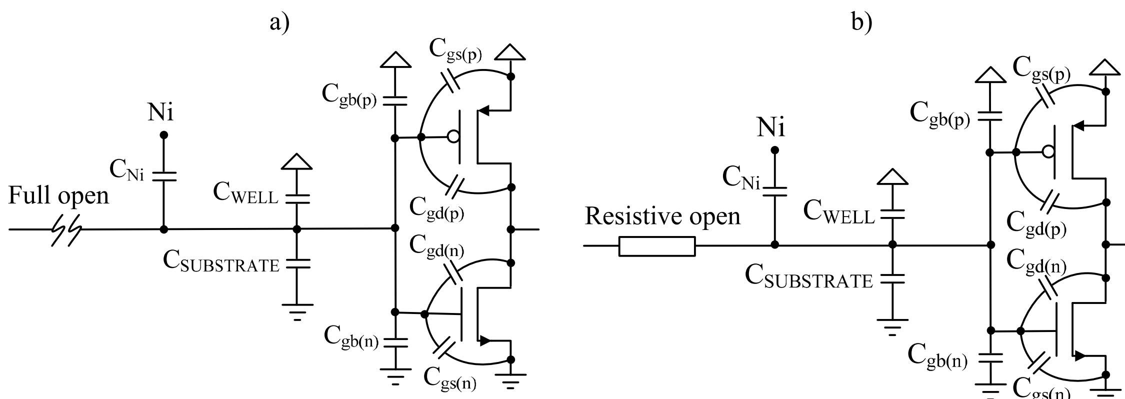

Figure 2.16. Parasitic capacitances to the defective line a) Full open b) Resistive open.

For a given topology of the circuit, the ratio between the capacitances to the l neighbouring structures together with the capacitances of the next driven gates and the initial trapped charge determines the static voltage value of the floating line (V_{Fline}), as described in (2.1), assuming an n-well technology and an inverter as the load driven by the floating line.

$$V_{Fline}=\frac{\left(\sum_{i=1}^{i=l}C_{Ni}\cdot I(N_i)+C_{WELL}+C_{gb(p)}+C_{gs(p)}+C_{gd(p)}(V_{Fline})+C_{gd(n)}(V_{Fline})\right)}{\sum_{i=1}^{i=l}C_{Ni}+C_{SUBSTRATE}+C_{WELL}+C_{gb(p)}+C_{gs(p)}+C_{gd(p)}(V_{Fline})+C_{gb(n)}+C_{gs(n)}+C_{gd(n)}(V_{Fline})}V_{DD}+V_{Qo} \qquad (2.1)$$

where C_{Ni} is the coupling capacitance between the floating line and neighbour N_i, $C_{SUBSTRATE}$ and C_{WELL} are the coupling capacitances between the floating line and the ground and power planes respectively, C_{gb}, C_{gs}, $C_{gd}(V_{Fline})$ are the transistor capacitances of the inverter driven by the floating line, V_{Qo} is the voltage due to the trapped charge and $I(N_i)$ is an indicator function, described in (2.2), a 0-1 value function which depends on the logic value of neighbour N_i for every test pattern. Notice how the gate-to-drain parasitic capacitances $C_{gd}(V_{Fline})$ depend on the voltage of the floating net. Anyway, for long lines where the neighbouring capacitances (C_{Ni}) are high, transistor capacitances (including $C_{gd}(V_{Fline})$) can be neglected.

$$I(N_i)\begin{cases}0 \text{ when } \mathrm{V_{Ni}}=0\\ 1 \text{ when } \mathrm{V_{Ni}}=V_{DD}\end{cases} \qquad (2.2)$$

In case of resistive opens, they are modelled in the same way as full opens, but replacing the complete disconnection by a resistive connection between the two end points of the fault, as shown in Figure 2.16b.

2.1.3.3 FULL OPEN NATURE

Full opens have different behaviours depending whether it is a large or a small open. A large open decouples completely the two end points of the defect. However, if the open is not large, the distance between the two disconnected points is so small that the oxide in between is very thin. In this case, electrons and holes are able to tunnel through [62], generating a current through the disconnected points. There are three different mechanisms generating tunnelling currents in CMOS technologies, which are described next:

1. Trap assisted tunnelling: It is a tunnelling current created by the traps generated by the impurities in the oxide. This effect happens at low electric fields. The magnitude of this tunnelling current depends on the quality of the oxide.
2. Fowler-Nordheim tunnelling: When the electric field across the oxide is strong enough, it causes band bending which makes the barrier thinner. Therefore, this tunnelling current increases as the electric field gets stronger.
3. Direct tunnelling: This mechanism occurs for very thin oxides and for low electric fields. It is modelled as the Fowler-Nordheim tunnelling current multiplied by a correction factor.

Small opens generating tunnelling currents are not as frequent as large opens. Furthermore, the current passing across the defect is lower than in the fault-free case. In this way, small opens are detected when an increase at the rise and at the fall time of the line is observed.

2.1.3.4 BYZANTINE GENERAL'S PROBLEM IN OPEN FAULTS

In a similar way as for bridging faults, open faults may cause the Byzantine General's problem. If the floating net voltage (V_{Fline}) is higher than the input logic threshold of the next gate, it is interpreted as logic 1, otherwise it is interpreted as logic 0. In case of a floating net with fan-out, the logic interpretation by the driven instances may be different depending on their logic thresholds. Consider the example in Figure 2.17. If $V_{ILmax(INV)} > V_{Fline} > V_{IHmin(NAND2)}$, then V_{Fline} is interpreted as logic 0 by *INV* and as logic 1 by *NAND2*. However, if $V_{IHmin(INV)} < V_{Fline} < V_{ILmax(NAND2)}$, V_{Fline} is interpreted as logic 1 by INV and as logic 0 by *NAND2*.

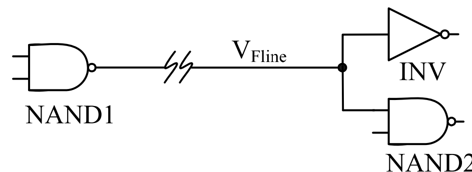

Figure 2.17. Byzantine General's problem due to a full open fault.

2.1.3.5 OPEN FAULT MODEL EVOLUTION

The most known open fault model is the stuck-open fault model. It was proposed by Wadsack in [63]. In this model, the transistor gate is fixed due to the open and cannot pull the gate output to its defect-free voltage. The fault model assumes a loss of charge in one transistor gate terminal in such a way that the output node is set to a high impedance state for at least one logic state. Therefore, a sequential behaviour can be

induced at the output, depending on the previous pattern applied. In Figure 2.18 it is depicted a 2-input NAND gate with a stuck-open in one of the pMOS transistors. For the state (V_A V_B) = (1 0) the output (V_Z) is in a high impedance state. Thus, if the previous pattern was (V_A V_B) = (1 1), the output would be interpreted as logic 0, otherwise as logic 1.

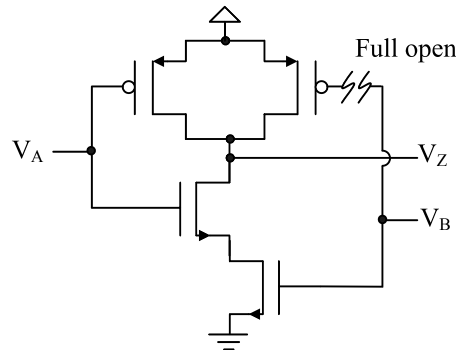

Figure 2.18. NAND gate with a stuck-open fault.

The transient response as well as the current behaviour of stuck-open faults were evaluated by Soden et al. in [64]. In a subsequent work, Maly et al. [56] reported that stuck-open faults only cover a small fraction of faults caused by actual opens. This work considered the location of the open in any of the transistor terminals, as illustrated in Figure 2.19 for an nMOS transistor. These models analyse the behaviour of a transistor in the presence of open faults. However, a single stuck-open transistor does not consider all possible opens. Furthermore, these models are not robust because they ignore both hazards and charge-sharing effects. To overcome these limitations, Di and Jess proposed a new fault model [65], where the hazard and the charge-sharing effects were considered at logic level. The detectability conditions were then represented by Reduce Ordered Binary Decision Diagrams (ROBDD) data structures utilised during fault simulation. In a subsequent work [66], Favalli et al. presented the node break fault model [66]. Broken connections without having knowledge about circuit layout were taken into account. The conditions of a node break fault were derived from electrical considerations. The minimum number of patterns needed to test the fault was determined based on graph theory. Testing a node-break fault is an implicit test for stuck-open faults of every transistor whose drain or source is connected to that node.

So far, all the fault models assume that the open causes a complete electrical disconnection. However, as a non-negligible amount of opens present in CMOS circuits belongs to the class of weak or resistive opens [54], recent works are also addressed to

resistive opens [67]. The electrical behaviour of resistive opens relies on the value of the unknown resistance value.

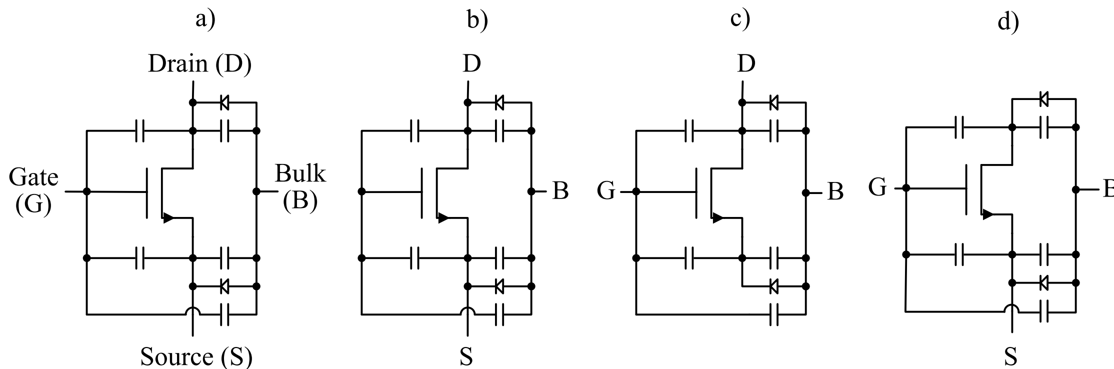

Figure 2.19. nMOS transistor model a) Defect free b) Open gate c) Open source d) Open drain.

Predicting the behaviour of open defects is challenging and difficult. What is more, interconnect opens may cause oscillation or sequential behaviour due to feedback capacitive couplings [68]. The capacitive feedback is due to either wire-to-wire capacitance or to Miller feedback capacitances from within a single logic gate. The range of initial voltages on the floating net causing oscillation or additional states is around $V_{DD}/2$. This is the most probable value to be charged due to the probable distribution of voltages and due to Miller capacitances during circuit power up. The most popular open fault model, the stuck-open fault model, does not represent most of actual open defects. The rest of fault models only targets certain classes of open defects or require specific test methods. Subsequently, although extensive work has been carried out to improve open fault models, more research is still required to develop new models that can cover part or all the real effects of such class of defects.

2.1.3.6 OPEN FAULTS OBSERVABILITY

Similar to bridges, different methods have been demonstrated to improve the observability of open defects. N-detect or multiple detect testing employs the SA fault model in order to generate patterns by targeting faults more than once to increase the probability of catching non-modelled faults [25], [69]-[70]. Every fault is targeted N times, i.e., a 2-detect test targets every SA fault twice, a 3-detect test targets the faults three times, etc. N-detect testing is not selective in targeting defect mechanisms or likelihood of defect occurrence. However, when targeting the same fault different times, it is likely to vary the neighbourhood state that surrounds the targeted fault. Hence, it is useful when targeting interconnect open defects, since the neighbouring lines cross-

coupled to the floating line are excited in different ways, modifying the state of the defective line.

Similar to lowering the power supply voltage, High Voltage (HV) testing is also used to improve the observability of defects. However, it does not have the success of VLV testing. Anyway, some works reported the usefulness of this technique when targeting resistive opens [71]-[73]. The delay added by the resistive open increases with the power supply value. Furthermore, high voltages are also used as voltage stress testing for reliability screening. Stressing the device with high voltages may improve the detection of such defect classes [74]-[76]. This technique is especially useful to detect oxide thinnings and via defects, which shorten the lifetime of devices. The goal of stressing devices is making evident these flaws, causing via defects to become opens and causing oxide thinnings to become oxide breaks. However, two parameters must be controlled thoroughly, the power supply voltage and the stressing time. If any of these two parameters exceeds the allowed limit, defect-free devices can be damaged. Following with the idea of modifying the power supply value, in the work by Haihua and Singh [77], it is exploited the idea of sweeping the power supply value. The authors proposed measuring the delay of defective circuits at different power supply voltages. They simulated the delay added by transistor related defects and resistive interconnect defects at different supply values. The results showed that the delay added by transistor related defects increased non-linearly when decreasing the power supply value. However, modifying the power supply value had a weak impact on the delay added by resistive interconnect defects. Thereby, the authors reported that it is possible to differentiate resistive interconnect defects from transistors related defects measuring the delay at multiple power supply values.

Although useful, I_{DDQ} testing is less effective for open defects than for bridging defects. The detection of opens by means of I_{DDQ} is highly subjective to the cell design style and the topology of the circuit [78]. Nigh and Gattiker reported in [44] that I_{DDQ} vs. time can give information about open defects. Some defective devices showed time-dependent I_{DDQ} behaviour with evolution in the order of seconds. The authors reported that a possible explanation of this phenomenon could be a floating gate caused by an open defect. Figure 2.20 shows a *NOR* gate with one of the gates of an nMOS transistor floating. When V_A is set to logic 1 and V_B to logic 0, V_C is in a high-impedance state. In

such a case, the steady state voltage of the net is primarily determined by the balance between the different leakage current components flowing into and out of the node (subthreshold, gate and reverse bias pn junction leakage currents). These currents are very small. Therefore, it may take seconds in order to reach the final state. During the evolution of V_C, as long as it has a voltage between $V_{TH(nMOS)}$ and V_{DD}-$V_{TH(pMOS)}$ and V_D is set to logic 0, there is current flowing through the downstream NOR gate. The current consumed by the NOR gate is different as the voltage on V_A evolves (see Figure 2.20b), which could explain the behaviour of defective devices with time-dependent I_{DDQ} as the ones reported in [42].

Temperature may also affect the behaviour of open faults. As the open resistance varies with temperature, the delay induced by the open changes also with temperature. Therefore, they can then be detected at a temperature different from the nominal one [71], [73]. Kruseman and Heiligers [47] reported that cold testing improve the detectability of open defects. Furthermore, in the work of Needham et al. [79] it was reported that a resistive open between an interconnect and a via caused a functional failure at -20ºC.

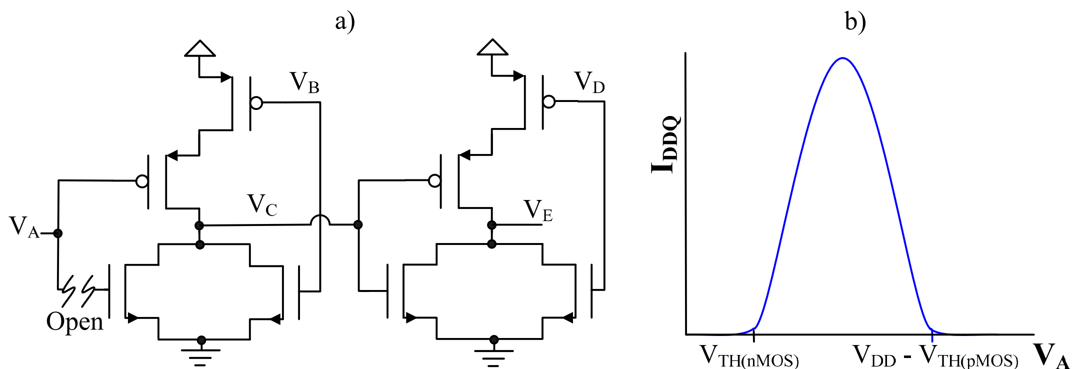

Figure 2.20. NOR gate with an open fault a) Transistor description b) I_{DDQ} vs. V_A.

2.1.4 DELAY FAULTS

An important part of real defects causes logic malfunctions at the working frequency, but functions properly at lower frequencies. These timing related failures are modelled as delay faults. There are three classical delay fault models, namely: the transition delay fault, the gate delay fault and the path delay fault model. However, two fault models have been developed more recently, which are partially based on the classical ones. They are the line delay fault and the segment delay fault model.

2.1.4.1 TRANSITION DELAY FAULT MODEL

The transition delay fault model is considered as a logical model for a defect which causes delay between the transition at the inputs and at the outputs of a gate [80]-[81]. There are two different transition faults: the slow-to-rise and the slow-to-fall transition. The slow-to-rise (slow-to-fall) behaves for a certain period of time like a SA0 (SA1). Two vectors are needed in order to carry out a test. Its main drawback is that it only detects large delay variations. As defects can cause a wide range of delays, some of them small, many faults are not detected. Therefore, the transition delay fault model is suitable as long as it can be assumed that delays are large enough to cause a faulty behaviour independently of the path through which they are propagated.

2.1.4.2 GATE DELAY FAULT MODEL

The gate delay fault model [82]-[84] assumes that the delays through the gates are known. The characteristics of likely delay faults are also known. The fault is considered as an added delay in the propagation of the transitions from the input to the output of the gate. Hence, variations resulting from the fabrication process are assumed to affect each gate individually. Its main advantage is the limited number of modelled faults in order to test the whole circuit. As inputs and outputs of every gate may have two possible faults (slow-to-rise and slow-to-fall), the number of faults is linearly dependent with the number of gates of the circuit. The main drawback is that it is necessary the model for the delays, which is not always available.

2.1.4.3 PATH DELAY FAULT MODEL

In the path delay fault model [85]-[88], faults are modelled as the sum of small delays on each connection along the signal path. Any path with a total delay exceeding the clock interval is said to have a path delay fault. This model covers every fault with a sensitisable path. Furthermore, every path corresponds to two logical paths, one to test the rising fault and the other to test the falling fault. A pair of vectors is required to test the fault. The first vector is applied to set the path to a known state and the second one to generate the desired transition. The main drawback of this model is the number of paths in a logic circuit, which can be huge. In the worst case, it is exponentially dependent with the number of lines. Thus, it is impossible to test the whole circuit exhaustively. A feasible method to overcome this problem is selecting a set of paths which covers each signal in the circuit based on some criteria. When making the path selection, it must be considered that some paths are not testable. Thereby, it must be

guaranteed that the chosen paths are testable. The proper path selection is the one which selects the smallest test set with the maximum coverage.

2.1.4.4 LINE DELAY FAULT MODEL

The line delay fault model [89] is a combination between the transition and the path delay fault model. A rising (falling) line delay fault tests the longest sensitisable path passing through a target line producing a rising (falling) transition on it. In this way, lines are covered with two possible transitions. The number of faults is directly dependent on the number of lines. It is the similar issue as in the path delay fault model, as the number of lines in a circuit can be huge. Thus, a properly line selection is required.

2.1.4.5 SEGMENT DELAY FAULT MODEL

The segment delay fault model [90] considers slow-to-rise and slow-to-fall faults on segments. The length of these segments can be as small as one (transition delay fault model), or as large as the maximum depth of the circuit (path delay fault model). The idea is to combine the advantages of single models while avoiding their limitations. It is more realistic to think that the delay over a segment can affect any path passing through it more than the delay over a line. Furthermore, the segment delay fault model prevents the increase in the number of faults to be considered.

2.1.4.6 DELAY FAULTS OBSERVABILITY

Modifying the power supply value is useful to detect delay faults. In fact, the impact of some delay faults increases at low power supply values, so that delay faults not observable at nominal conditions become observable at lower supply voltages [91]-[92]. The effectiveness of VLV testing increases at increasingly lower power supply voltages. However, reducing the supply voltage has the disadvantages of decreasing the noise margin and the operating speed of the circuit.

Another technique which improves the observability of delay faults consists in capturing the circuit outputs at multiple clock periods shorter than the nominal one [93]-[95]. In some cases, this methodology is composed of two stages. In the work by Liou et al. [94], after the multiple clock test, a different pattern set is added to the original pattern set used for quality enhancement. On the other hand, in the work presented by Haihua and Singh [95], the results of the multiple clock test are compared to those for neighbouring dies to minimize the effect of parameter variations.

Analyzing the power supply transients in both time and frequency domain has also been considered. It is the so-called transient signal analysis (TSA) [96]. In the presence of delay faults, the parasitic components of the device are modified so that a different transient behaviour is obtained ant therefore, delay faults can be observed.

Finally, with the continuous shrinking of dimensions in nanometer technologies, parameter variations become more important, influencing the delay of signal paths from die to die and within dies. This fact makes more difficult the distinction between fault-free devices and the ones containing delay faults. To avoid this problem, some approaches have incorporated statistical methods in delay testing [97]-[98].

2.2 DIAGNOSIS METHODOLOGIES

Diagnosis is the process which locates the failure site of a faulty device. Subsequently, a failure analysis can be performed, if desired, to examine the defect physically. Precise diagnosis is important. It helps manufacturers solving process problems, improving yield and saving time on physical failure analysis, which is time consuming and require significant investment in equipments, tools and qualified personnel.

Diagnosis techniques combine simulation results with the data obtained from the ATE (Automatic Test Equipment). Most of the techniques involves two main elements: a fault model and a comparison algorithm. Thus, using accurate fault models is a key factor. If models are not accurate, the result may be an imprecise or even an incorrect location of the failure site.

Fault diagnosis techniques can be broadly classified into two groups: cause-effect and effect-cause techniques [99]. Cause-effect diagnosis techniques are based on fault simulations to determine the possible response of a circuit in the presence of faults. This information is then compared with the response obtained from the tester in order to obtain the fault location. Some cause-effect techniques use a pre-computed fault dictionary, which is a database containing the faulty responses of each fault. The algorithm then determines which fault from the dictionary best matches the faulty behaviour observed on the tester. Techniques using a fault dictionary are also known as static diagnosis techniques. However, with the increasing complexity and number of transistors in today's ICs, sometimes it is not feasible to build a dictionary for every

possible fault, since the size of the dictionary would be prohibitive. Thereby, a lot effort is focused in reducing and compressing the size of fault dictionaries [100]-[102]. The other possibility is using dynamic diagnosis. Dynamic diagnosis techniques analyse the response of the faulty circuit. The list of fault candidates is then reduced based on the response of the circuit and only the most probable faults are considered.

The effect-cause approach backtracks logic errors from the primary outputs to the location of the fault deducing the internal values of the circuit. In principle, most of these diagnosis techniques do not require neither fault dictionary nor fault enumeration.

2.2.1 SA FAULT DIAGNOSIS

Primary diagnosis techniques were based on the SA fault model. The SA fault model has demonstrated to be effective to detect other class of faults. However, most of real defects do not behave as SA faults. Therefore, diagnosis methods based on the SA fault model had limited success. Anyway, extensive work has been developed to diagnose such faults. In an early work, the fault dictionary was used where the faulty responses of each modelled fault were stored [103]. The fault dictionary is built for a specific set of faults. Therefore, a faulty response obtained on the tester, which is not equivalent to any of the simulated faults from the dictionary, cannot be located in the dictionary. Thereby, the location of the fault is carried out based on a closest-match analysis. In this way, different matching algorithms with increasing complexity were subsequently developed to improve diagnosis results [104]-[107]. However, fault dictionaries for SA faults are prohibitive due to computational effort both in time and storage space. For this reason, some works utilise a two-step procedure [108]-[109]. The first step consists in a dictionary reduction to save time and memory space, assuming some loss in precision and accuracy. The second step is the matching algorithm.

In general, the use of SA fault signatures usually results in large diagnosis sizes and a ranking algorithm is required to reduce the size of the results. Since the ranking of faults depends heavily on the number of failing primary outputs, it performs poorly when the number of primary outputs is small. For these reasons, more attention was subsequently paid on the diagnosis of other types of faults.

The effect-cause approach has also been applied based on the SA fault model. These techniques process the response obtained from the tester to determine the internal values of the device under diagnosis (DUD) [110]-[111]. Internal values are computed

by a deduction algorithm, which tries to justify all the values obtained at the primary outputs.

2.2.2 BRIDGING FAULT DIAGNOSIS

Diagnosis of bridging faults using information from single SA faults was common in the past, since processing SA faults is computationally simpler than processing bridging faults, both in terms of fault list size and fault simulation complexity. Different logic diagnosis methodologies have been developed using fault dictionaries and fault simulation. In the fault dictionary [112]-[117], the faulty response of each considered bridging fault is stored for every test pattern. The diagnosis process is carried out comparing the output response of the failing device to the information contained in the fault dictionary of bridges. In the works by Chakravarty and Gong [113], [117] the initialization graphs are used for generating the initial set of bridging fault candidates. Subsequently, a set of pruning rules are considered to reduce the candidates set. The first work [113] is based on the wired-AND and the wired-OR bridging fault model, whereas the second work [117] is based on the voting model. Other works [112], [114]-[116] took benefit from composite signatures. A composite signature [112] is the bridge fault signature resulting from the union of the four stuck-at fault signatures associated with the bridged nodes. The main improvement in the work by Chess et al. [114] related to previous work in [112] is the restriction of the number of faults under consideration, which increases the efficiency of the methodology. This is achieved by eliminating from the composite signature entries that cannot be used to detect the bridging fault and also defining the set of vectors which should detect a particular bridge. In [116], quality measurements were defined to create a ranking criterion for bridging faults. These quality measurements were subsequently used for other works and even applied to other fault models. The criterion is based on the comparison between the results obtained on the tester and the prediction of the bridging fault model so that the part of the tester results, which is also included in the fault model prediction, is called *Intersection* (see Figure 2.21). Failing vectors predicted by the fault model, which have not failed on the tester, are called *Mispredictions* and vectors which have failed on the tester, but are not predicted by the fault model, are called *Nonpredictions*. The ranking criterion is based on the *Intersection* value. The higher, the better.

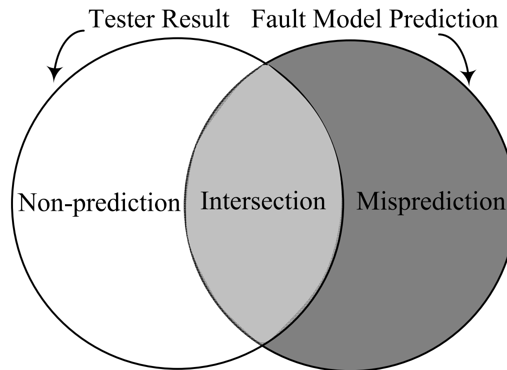

Figure 2.21. Matching algorithm [116].

Fault dictionaries are feasible when the diagnosis is performed repeatedly for a given design. However, their main drawback is the storage space. A circuit with *n* number of nets has $\binom{n}{2}$ possible bridging faults. Thus, considering every possible bridging fault is infeasible. Physical layout information is usually considered to eliminate bridges between nets that are extremely unlikely to be bridged together due to their physical location [115]-[116]. If the two nets are not closer than some minimum distance or if there is another net separating them that would also be involved in the bridge, the corresponding bridging fault is discarded. However, there are also some techniques to reduce the number of candidates without using layout information, as the two techniques reported by Lavo et al. in [118]. The first technique uses the SA fault diagnosis to identify one of the bridged nets. If this is accomplished, assuming a circuit with *n* nets, knowing the *d* net candidates to be one of the nets involved in the bridge, the number of bridged pairs is then reduced to $n \cdot d$. The second technique identifies the candidates that can have an intersection with the behaviour observed on the tester. Candidates with no intersection are then discarded.

In a more recent work, Zou et al. [119] proposed a diagnosis methodology based on dictionaries which take the bridge resistance into account. The methodology is divided into two steps. The first step consists in a logic diagnosis to find the potential candidates that can explain the faulty behaviour. In the second step, layout information as well as the resistive bridging fault model using the concept of critical resistance [11] are used to prune the candidates list. The intersection between resistive intervals is utilized to discard bridging candidates. As an example, consider the bridged outputs (net *A* and *B*) of two gates (*G1* and *G2*), as depicted in Figure 2.22. They drive in turn gates *G3* and *G4*, respectively. Assume that test patterns TP_1 and TP_2 cause *G3* and *G4* to fail,

respectively, whereas TP_3 passes although it also activates the bridge. Gate *G3* should have failed in this case. In the fault free case, consider that TP_1 and TP_3 set net *A* and net *B* to logic 1 and 0 respectively. On the contrary, TP_2 sets them to logic 0 and logic 1, respectively. As test patterns TP_1 and TP_2 fail, the bridge resistance should be lower than the minimum of the two critical resistances $R_c(TP_1,G3)$ and $R_c(TP_2,G4)$. Nevertheless, for passing pattern TP_3, the bridge resistance should be higher than the critical resistance $R_c(TP_3,G3)$. Thus, it must be accomplished that the bridge resistance is $R_c(TP_3,G3) < R_b < min(R_c(TP_1,G3),R_c(TP_2,G4))$. On the other hand, in case that $R_c(TP_3,G3) > min(R_c(TP_1,G3), R_c(TP_2,G4)$, there is no bridge resistance explaining the faulty behaviour, and therefore, this candidate can be removed from the list.

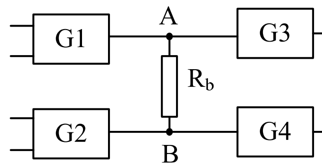

Figure 2.22. Resistive bridging fault diagnosis.

Instead of using the pre-computed information stored in a table used by fault dictionaries, the fault simulation procedures [120]-[121] consist in comparing the actual output response of the failing device to the expected response for each possible bridge. A list of fault candidates is then generated. Faults whose effects most closely match the response of the failing device are identified as candidates. The advantage of this approach compared to fault dictionaries is that fault simulation is faster. In the work developed by Wu and Rudnick [121], information from single SA faults is used. Single SA fault simulations are performed during fault diagnosis for a more accurate result.

All the presented methods are implemented at inter-gate level. However, bridging faults at intra-gate level are also possible. A recent work by Fan et al. [122] addresses the logic diagnosis of intra-gate bridging faults by means of a transformation method.

I_{DDQ} has demonstrated to be also effective for the diagnosis of bridging faults. At the beginning, it was believed that I_{DDQ} could not provide enough information for diagnosis purposes [5]. Subsequently, different works demonstrated the effectiveness of I_{DDQ} for bridging fault localisation. The main advantage of current methodologies is that fault signatures are easy to generate. The first works [123]-[126] were based on the simple I_{DDQ} bridging fault model, which assumes that abnormal high current is generated when the bridged nets are set to different logic values. Aitken [123]

demonstrated that combining logic and current information diagnosis resolution was improved. Subsequently, the same author presented diagnosis results without using logic information [124]. Chakravarty and Suresh proposed in [125] an I_{DDQ} based diagnosis algorithm which considers also whether one of the nodes involved in the bridge is internal. Subsequently, Nigh et al. [126] relied on a set of realistic bridges based on layout information with good results. As the number of possible bridges to be considered is huge, most of the works relied on a set of limited realistic bridges obtained by extraction tools. Nevertheless, although this idea has been demonstrated to be effective, most of the extractors only identify possible bridges between nets in the same metal layer. However, reality has shown that bridges between nets in different metal layers are also possible [124]. To avoid this loss of accuracy, Heaberlin proposed in a recent work [127] a heuristic method for high-speed diagnosis feasible for large industrial designs, which considers *a priori* all possible bridges in the circuit [127].

The application of the simple I_{DDQ} bridging fault model has mainly two drawbacks. The first one is that a bridge may have many equivalent faults which cannot be distinguished. The second drawback is the increase of leakage current for future technologies. Some works have been proposed to overcome the limitations caused by the leakage current. Gattiker and Maly presented in [43] and [128] the amount of diagnostic information present in current signatures and how the number of current levels may distinguish bridging faults, which are equivalent under the assumption of the simple I_{DDQ} bridging fault model. Furthermore, Thibeault proposed in [129] and [130] a method based on differential or delta I_{DDQ} probabilistic signatures for bridging faults. The method is performed into two steps. The first one is a pre-processing step, where the most probable faults are listed. This is the starting point of the second step, where the fault location is carried out by finding the location that causes the expected current values match experimental measures. In subsequent works [131]-[132], Hariri and Thibeault proposed a diagnostic method combining three data sources, namely: I_{DDQ} measures to identify the most probable bridging faults, parasitic capacitances extracted from layout to create a list of realistic bridges and finally, logical errors produced by logic fault simulation to perform fault isolation. The I_{DDQ} stage procedure is based on delta I_{DDQ} probabilistic signatures previously proposed in [129] and [130].

2.2.3 OPEN FAULT DIAGNOSIS

Research on diagnosing open faults is not as extensive as on bridging faults. In fact, the most important part of this effort has been focused on diagnosing interconnect open faults. One of the first works in this field was presented by Venkataraman and Drummonds [133]. This work uses logic diagnosis based on the net diagnostic model. The approach is similar to the composite signature applied to bridging faults. Consider the net in Figure 2.23, which is composed of the stem *A* and the branches *B* and *C*. The logic errors caused by a 0/1 error at locations *A*, *B* and *C* are saved in the erroneous observation (EO) sets EO_1, EO_3 and EO_5, respectively, as described in Table 2.I. Similarly, the errors caused by a 1/0 error are saved in the sets EO_2, EO_4 and EO_6, respectively. The diagnostic signature EO for the stem A is then computed as the union of the sets EO_1, EO_2, EO_3, EO_4, EO_5 and EO_6. In the presence of an open on net *ABC*, only a subset of the set EO will be faulty. A path-tracing procedure is then used in order to identify the logic nets potentially associated with an interconnect open defect. The metrics for the candidates ranking is the same used in [116].

Liu et al. [134] presented a model-free diagnosis algorithm for multiple interconnect open faults. In the presence of an open fault, each fan-out branch of the stem is considered to behave at random independent of the value on the stem. Therefore, every branch may take an arbitrary logic 1 or 0 for each pattern. An iterative algorithm using X values identifies possible faulty locations. Subsequently, simulations are carried out to reduce the set of candidates.

Unlike these previous works, some recent works considered physical information. Huang [135] proposed a diagnosis procedure based on the segment fault model. A segment is a part of a net based on routing information. Knowing the layout, the target net can be divided into several segments, as shown in Figure 2.24. Symbolic simulation is then performed to find open segments on the target line. The main drawback of this methodology is that there are cases where segments are still long and the open fault cannot be precisely located along the segment.

Sato et al. [136] introduced a technique to find open vias by using physical information. The capacitances between the floating net and its neighbouring lines are taken into account to predict the changes in the floating node voltage for every pattern, as described in (2.3):

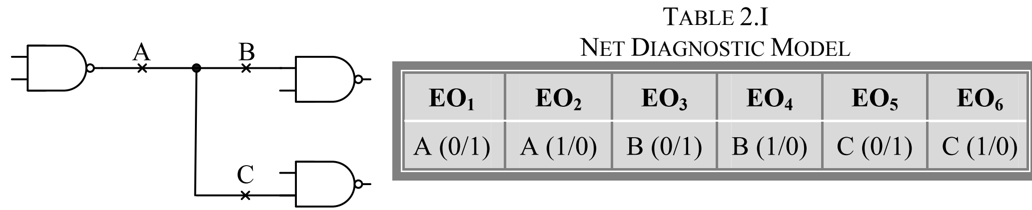

TABLE 2.I
NET DIAGNOSTIC MODEL

EO_1	EO_2	EO_3	EO_4	EO_5	EO_6
A (0/1)	A (1/0)	B (0/1)	B (1/0)	C (0/1)	C (1/0)

Figure 2.23. Net diagnostic model.

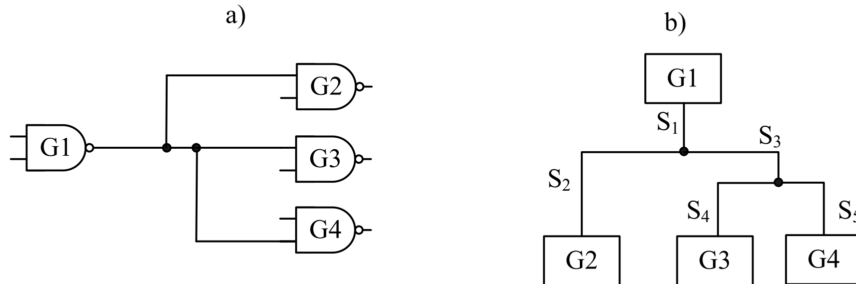

Figure 2.24. Segment fault model a) Gate level b) Layout (S_i segment).

$$E(p) = \frac{C_1(p)}{C_0(p) + C_1(p)} \tag{2.3}$$

where $C_1(p)$ is the sum of the capacitances between the floating net and its coupled neighbours which are set to logic 1 for a specific test pattern (p) and $C_0(p)$ the sum of the capacitances between the floating net and its coupled neighbours which are set to logic 0 for the same p pattern. The patterns detecting the fault are then divided into two sets: Ω_0 and Ω_1. Ω_0 (Ω_1) is composed of patterns which set the floating net voltage to a value lower (higher) than the threshold voltage of the driven gate. Therefore, in the presence of an open defect, it should be satisfied the expression in (2.4) for any of the open vias located along the net.

$$E(\Omega_0) < E(\Omega_1) \tag{2.4}$$

The main drawback of this methodology is that capacitances between internal nodes and gate input threshold voltages are not considered. Thereby, in situations where the floating net has fan-out and the threshold voltages of the inputs of the driven gates are different may cause expression (2.4) not to be satisfied. Furthermore, this work is limited only to open vias and discards finding opens caused by broken metal tracks.

Zou et al. [137] presented a diagnosis technique based on the segment fault model proposed in [135]. SPICE simulations are used to get the input threshold voltages of the driven gates. With this information and the principle of charge conservation a prediction of the initial trapped charged is obtained, which is used to reduce the number of possible

open vias within the segment explaining the faulty behaviour. Opens caused by broken metals tracks are neither considered.

Some research has also been carried out to diagnose stuck-open faults. In the work by Li [138], a table was built up for every type of gate. The same author considered the possible sequence behaviour of open defects in the diagnosis procedure [139]. Fan et al. [140]-[141] developed a transformation method which allows a stuck-at fault diagnosis tool to be applied directly on the diagnosis of inter gate stuck-open faults. Finally, it must be noticed the work by Li and McCluskey [142], where it was presented a methodology for the diagnosis of a specific open fault type presented previously in 2.1.3.3, the tunnelling open.

2.2.4 DELAY FAULT DIAGNOSIS

With timing-related defects affecting today's circuits, delay faults are also focusing part of diagnosis effort. The methodologies developed for the diagnosis of delay faults are based on different fault models, which were presented in Section 2.1.4. One of the first works in this field was presented by Cox and Rajski [143]. It was based on the transition fault model. Some other recent works were also based on the same fault model. Pomeranz and Reddy [144] used the assumption of pattern dependence in order to improve diagnosis resolution. In the work by James and McCluskey [145], the methodology was developed for the diagnosis of resistive opens and stuck-opens, where the sequence dependence of open faults was taken into account.

The transition fault model is not the only one used for diagnosis purposes. Flottes et al. [146] and Girard et al. [147] presented works to diagnose delay faults based on the gate delay fault model. In [146], a two-valued logic simulation was used. However, an improved method using a six-valued symbolic simulation was considered in [147].

Recently, the path delay fault model has been the most common delay fault model used for diagnosis purposes. Pant et al. [148] applied the effect-cause analysis to diagnose path delay faults. A different approach was considered in the works by Ghosh-Dastidar and Touba [149] and Tekumalla [150], where an explicit test for each suspect delay fault was generated. Finally, Sivaraman and Strojwas [151] identified the likely sub-paths that may cause delay faults considering process parameter variations.

2.2.5 OTHER METHODOLOGIES

There are some other interesting methodologies which cannot be classified in the previous sections. For example, the work developed by Ventakaraman and Drummonds [152]. They proposed a diagnosis method able to locate four different types of faults: SA, bridge, node and net fault. The SA fault covers shorts to power and ground. The bridge model covers shorts between lines. The node model covers opens and cell faults. Finally, the net model covers opens on large interconnect lines with fan-out. These four models are built based on composite signatures. The three metrics used to rank the fault candidates are the same as the ones proposed in [116].

Some others works are not based on the classical fault models presented so far. Boppana and Fujita [153] developed a methodology based on capturing the unmodeled faulty behaviours. This method is able to model all possible behaviours created from a specific set of nodes. The simulation results are then compared with the tester results and a matching algorithm ranks the candidate faults. The main drawback of this proposal is that it becomes unfeasible for large circuits. Bartenstein et al. [154] proposed a diagnosis method based on logical defects. A logical defect is the minimum set of nets that can be affected by the physical defect. Therefore, this method is focusing on the location of the defect without considering any specific fault model. For that purpose, only a specific class of failing patterns are analyzed, the so-called SLAT (Single Location At a Time) patterns. A pattern has the SLAT property if all the observed fails of the pattern can be explained exactly by at least one single net fault. Desineni and Blanton [155] developed a methodology which also takes benefit from the SLAT patterns. The methodology attempts to derive defect behaviours from tester data. A path trace procedure is carried out to identify the faulty lines. The method extracts then the set of logical conditions for the physical neighbours responsible for the excitation of the fault. Subsequently, simulations are carried out to validate the faulty behaviour even for the passing patterns. Nevertheless, the method must make some assumptions in order to keep the problem tractable. In the work by Wang et al. [156], it is proposed a multiple-fault-diagnosis methodology based on the partition of the failing outputs and the use of an incremental simulation-based technique to diagnose failures one at a time.

Finally, Lavo et al. presented a diagnosis methodology based on the STAT (Single Test At a Time) algorithm [157]. It differs from the SLAT algorithm in the fact that the STAT uses a scoring mechanism to narrow the resulting candidates. Furthermore, the STAT algorithm utilizes the results from the passing and the complex failing tests to improve the scoring of the candidates. However, the main drawback of the STAT algorithm is the big size of diagnosis results.

CHAPTER 3. DIAGNOSIS OF BRIDGING DEFECTS

As bridging defects are common defects affecting CMOS circuits, their diagnosis becomes relevant for present and future technologies. There are mainly two different approaches when diagnosing bridging faults: voltage based [112]-[122] and current based techniques [123]-[132]. The voltage based methodologies must face two challenging problems: the Byzantine's general problem [3] and feedback bridges [2]. In case of current based techniques, fault signatures are easy to generate. The Byzantine's general problem disappears because no logic information is managed. However, feedback bridging faults still generate difficulties. Furthermore, the distinction between the leakage and the defect current becomes more challenging for every new technology.

The first part of this chapter presents the analysis of the current behaviour of bridging faults. Based on this analysis, a current based diagnosis methodology for this class of faults is proposed. Experimental results on real devices corroborate the feasibility of the method. Finally, the last part of the chapter describes how the use of logic information by means of Shmoo plots is also useful for the diagnosis of bridging faults.

3.1 CURRENT BEHAVIOUR OF BRIDGING FAULTS

When modelling the current behaviour of bridging faults, the easiest way is by means of the simple I_{DDQ} bridging fault model. As previously seen in Chapter 2, it assumes that when the bridged nodes are set to the same logic value related to the fault free case, the current consumption of the device is the leakage current. However, when the bridged nodes are set to different logic values, a current path is generated between power and ground and non-desired current is flowing through the bridged networks. Assume the example in Figure 3.1. The bridge is connecting the output of a 2-input NAND gate and an inverter. The input combinations exciting the bridge and increasing the quiescent current consumption are shown in Table 3.I.

The simple I_{DDQ} bridging fault model has mainly two drawbacks for diagnosis purposes. On the one hand, the increasing leakage current for nanometer technologies complicates the distinction of defect currents. On the other hand, its behaviour description is so simple that a fault may have many equivalences in a similar way as the SA fault model. Assume that both the inverter and the NAND gate of Figure 3.1 drive in turn inverters, as illustrated in Figure 3.2. A bridge between the outputs of these two inverters is equivalent to the previous example. The input combinations activating the bridge are the same in both cases, as observed comparing Table 3.I and Table 3.II.

The discrimination between these two faults is possible provided that the bridged network strengths are considered. For the example in Figure 3.1, there are three different network excitations, as depicted in Figure 3.3. Every excitation adds an equivalent resistance between power and ground, generating thus different quiescent currents. If a set of patterns are applied so that all possible combinations of the bridged networks are excited, the I_{DDQ} measurements would follow the behaviour of Figure 3.4a, where four current levels are clearly observed. The lowest level corresponds to

those patterns which do not excite the bridge. The three upper ones correspond to the patterns which activate the bridge. In these cases, apart from the leakage current, extra current is flowing through the bridged networks. According to Figure 3.4a, letters *a*, *b* and *c* relate the current level with their corresponding excited network in Figure 3.3. The highest current level corresponds to the case where both pMOS transistors of the NAND gate are in the on state (Figure 3.3b). In this case, the equivalent resistance composed by the parallel pMOS transistors of the NAND gate, the bridge resistance and the nMOS transistor of the inverter is lower than in the other two configurations.

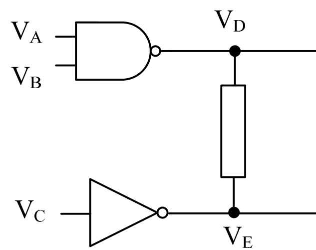

Figure 3.1. Bridging fault example.

TABLE 3.I
I_{DDQ} IN FIGURE 3.1

V_A	V_B	V_C	V_D	V_E	I_{DDQ}
0	0	0	1	1	Leakage
0	0	1	1	0	High
0	1	0	1	1	Leakage
0	1	1	1	0	High
1	0	0	1	1	Leakage
1	0	1	1	0	High
1	1	0	0	1	High
1	1	1	0	0	Leakage

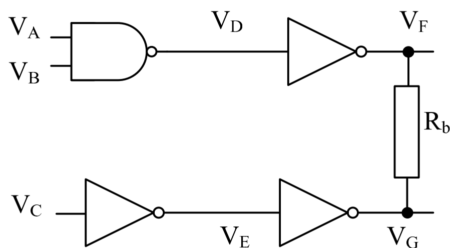

Figure 3.2. Bridging fault between two inverters.

TABLE 3.II
I_{DDQ} IN FIGURE 3.2

V_A	V_B	V_C	V_F	V_G	I_{DDQ}
0	0	0	0	0	Leakage
0	0	1	0	1	High
0	1	0	0	0	Leakage
0	1	1	0	1	High
1	0	0	0	0	Leakage
1	0	1	0	1	High
1	1	0	1	0	High
1	1	1	1	1	Leakage

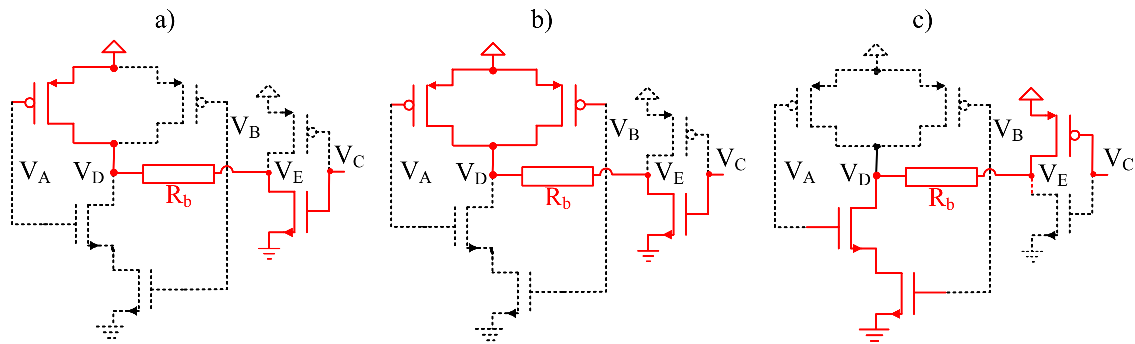

Figure 3.3. Network excitations for example in Figure 3.1 a) One pMOS transistor on (NAND gate) b) Both pMOS transistors on c) nMOS network on.

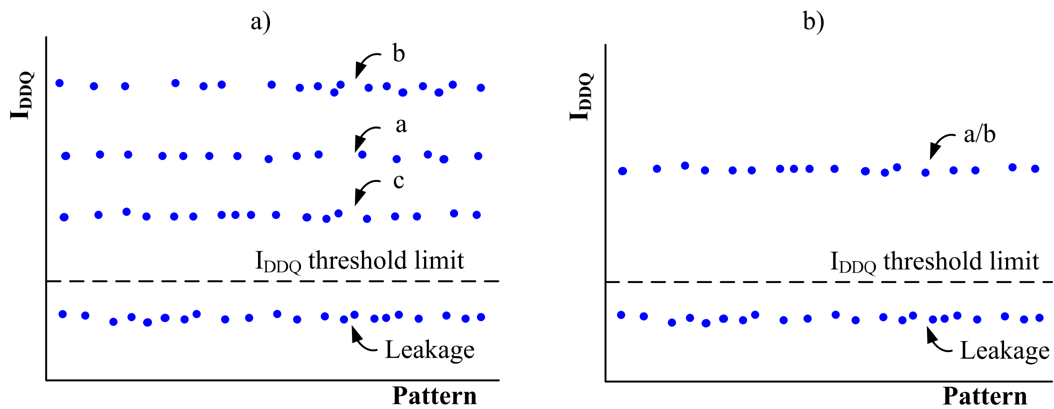

Figure 3.4. I_{DDQ} measurements a) Example from Figure 3.1 b) Example from Figure 3.2.

Regarding the bridge between the outputs of the inverters, assuming identical inverters, there is only one equivalent network excitation, as described in Figure 3.5. For that reason, the I_{DDQ} measurements would only show two current levels, the lowest one corresponding to the leakage current and the upper level when the bridge is activated, as depicted in Figure 3.4b.

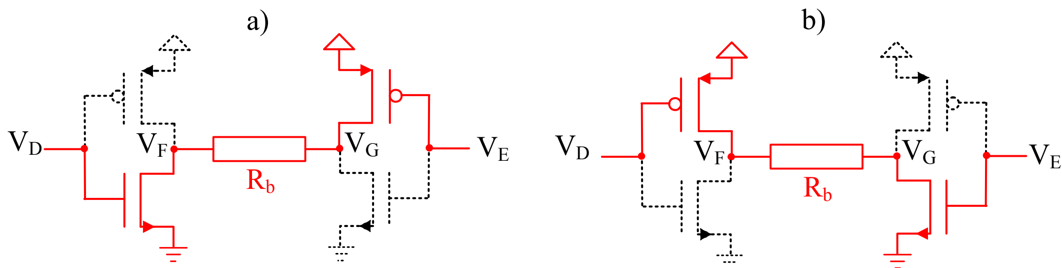

Figure 3.5. Equivalent network excitations from example in Figure 3.2.

Reordering the I_{DDQ} measurements in increasing order, the current signatures [43]-[44] corresponding to the two previous examples are presented in Figure 3.6. On the one hand, the current signature corresponding to the bridge between the output of the NAND gate and the inverter has three current steps. However, the one from the bridge

between the inverters has only one current step. Notice that the two bridges, equivalent under the assumption of the simple I_{DDQ} bridging fault model, are now distinguishable.

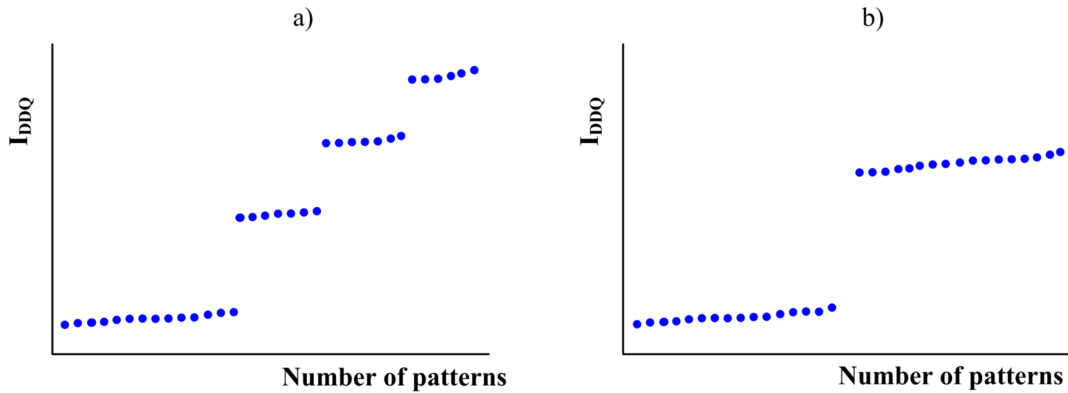

Figure 3.6. Current signatures a) Example from Figure 3.1 b) Example from Figure 3.2.

3.1.1 BRIDGE CURRENT AND DOWNSTREAM CURRENT

It has been observed how it is possible to discriminate between bridging faults if the current information given by the network strengths is properly treated. However, the current flowing through the bridged networks does not necessary characterise accurately the behaviour of this class of faults. It is known that a bridge may cause voltage degradation on the bridged nodes. This voltage degradation causes in turn the gates driven by the bridged nodes (downstream gates) to consume more current than expected, as long as the proper conditions are given. Hence, the total current (I_t) caused by a bridging fault comprises two components: the bridge current (I_b) and the downstream current (I_d), as described in (3.1) [158]-[160].

$$I_t = I_b + I_d \qquad (3.1)$$

On the one hand, the bridge current is the additional current flowing through the non-desired connected transistor networks. On the other hand, the voltage degradation on the bridged nodes causes the gates driven by these nodes to consume more current than expected. The non-desired current consumed by these gates is the so-called downstream current. Consider the example in Figure 3.7a. It is similar to the one in Figure 3.1, but now the inverter is driving in turn a NAND gate. When the bridge is activated, the current flowing through V_D and V_E is the bridge current. Due to voltage degradation on V_E, there may also be downstream current flowing through the NAND gate provided that V_F is set to logic 1. The three possible network excitations in the

presence of downstream current (V_F = 1) are described in Figure 3.7b, c and d, respectively.

The magnitude of the downstream current depends on different factors, namely: the bridged networks, the topology of the downstream gate and the bridge resistance. The relationship between the downstream current and the voltage of the bridged node is similar to the current behaviour in the presence of a floating node caused by an interconnect full open. If an intermediate voltage value is induced (between $V_{TH(nMOS)}$ and [V_{DD} - $V_{TH(pMOS)}$]), downstream current is generated. The amount of current depends on the exact voltage value, as observed in Figure 3.8a.

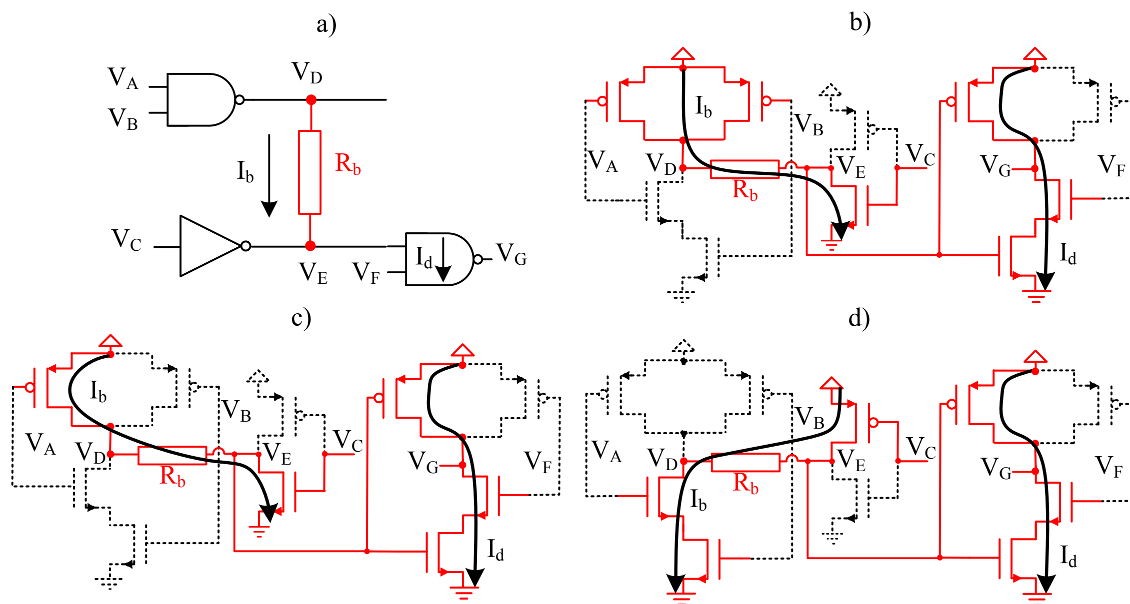

Figure 3.7. Bridging fault with downstream current a) Gate level b) Both pMOS transistors on (NAND gate) c) One pMOS transistor on c) nMOS network on (NAND gate).

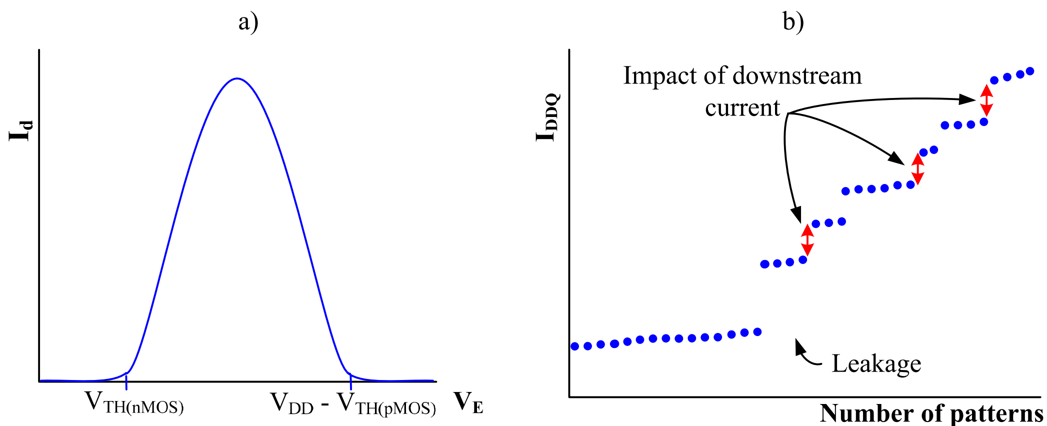

Figure 3.8. Example in Figure 3.7 a) Downstream current vs. node voltage b) Current signature.

To the author's knowledge, the contribution of the downstream current to the total current consumption has not been previously considered for diagnosis purposes, although it may have significant impact on diagnosis results. Neglecting the downstream current, the current signatures for the examples in Figure 3.1 and Figure 3.7 would be identical. Nevertheless, regarding the example in Figure 3.7a, for every network combination, there are two possibilities depending on the V_F value. If V_F is set to logic 0, there is not downstream current. In this case, the total current is then the same as in Figure 3.1. However, for patterns setting V_F to logic 1, there is downstream current, which increases the total current caused by the bridge. In this sense, every of three upper current levels may unfold into two sub-levels, as illustrated in Figure 3.8b. Notice that the current signature is quite different since seven current levels are now reported.

SPICE simulations have been carried out to quantify the impact of the downstream currents. For that purpose and without loss of generality, the example in Figure 3.7a is still used. Identical pMOS transistors for the NAND gate and a 0.18 µm technology are considered. Figure 3.9a illustrates the results for the bridge excitation when both pMOS transistors of the NAND gate are on (Figure 3.7b). At nominal conditions (V_{DD} = 1.8 V), when V_F is set to logic 0, there is not downstream current ($I_t = I_b$) and the bridge is generating around 400 µA. However, if V_F is set to logic 1, the downstream contribution is adding 10% more current. In case only one pMOS transistor is on, the impact of the downstream current is lower (around 10 µA), as indicated by the red lines in Figure 3.9b. However, when the nMOS network of the NAND gate is excited, around 35 µA are added due to the downstream current, as observed by the green lines in Figure 3.9b. Extrapolating these simulation results to current signatures, it is lead to the conclusion that six current steps, instead of the three expected ones should be observed, as long as all the possible configurations are activated. Notice that in general, if the bridged nodes have big fan-out, the downstream current may cause the appearance of a high number of current steps

3.1.2 IMPACT OF V_{DD}

The downstream current may complicate the diagnosis of bridging defects. However, the inclusion of the downstream current requires defect information, which is typically not available. Thereby, trying to minimize its impact seems the most feasible

option for diagnosis purposes. This section demonstrates that this can be obtained at low power supply values [159]-[160].

It is already known that the relationship between I_{DDQ} and V_{DD} gives information to discriminate faulty from good devices [161]. When applied to bridging defects, the behaviour of the two current components (bridge and downstream current) is different related to V_{DD}. The difference lies in the fact that the bridge current comes from transistors being in the ohmic state, whereas the downstream current comes from transistors more likely operating in the saturated region. To analyze this fact, consider, without loss of generality, the example in Figure 3.10a. The outputs of two identical inverters (*INV1* and *INV2*) are bridged. One of them is driving in turn another inverter (*INV3*). The downstream current is determined by the current flowing through *INV3*, as shown in Figure 3.10b.

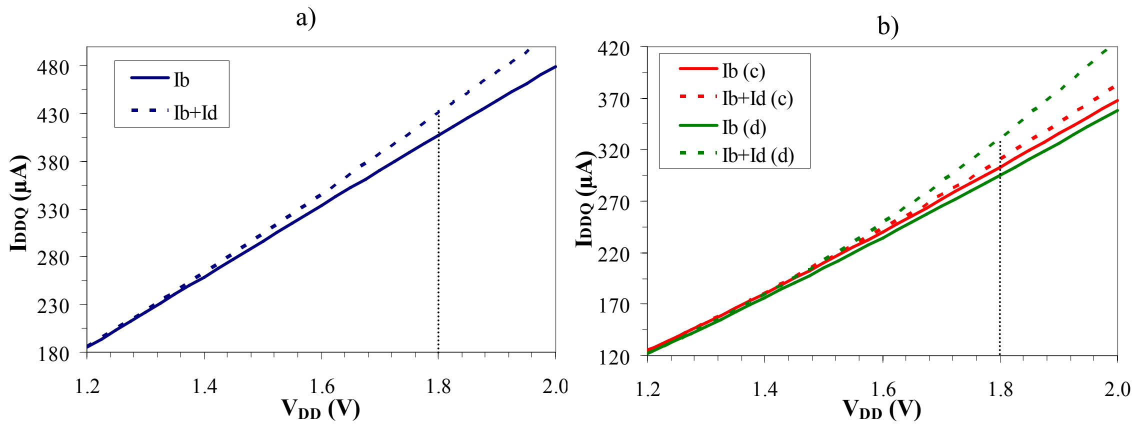

Figure 3.9. I_{DDQ} vs. V_{DD} SPICE simulation results a) Network excitation from Figure 3.7b b) Network excitations from Figure 3.7c (in red) and Figure 3.7d (in green).

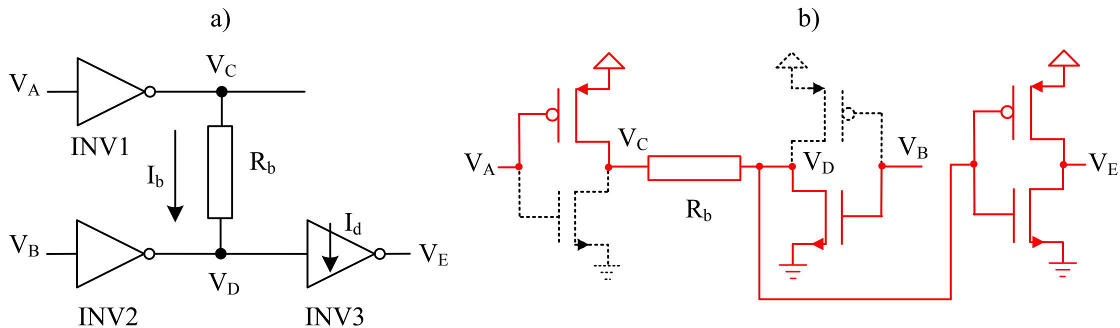

Figure 3.10. Bridging fault between two inverters a) Gate level b) Transistor level.

The transistors of *INV3* work in the saturated region due to the intermediate voltage value of V_D. Assuming compensated pMOS and nMOS transistors for the three inverters and low resistance for R_b, V_D is set close to $V_{DD}/2$. Considering the Shockley

model, the bridge and the downstream currents are determined by the following equations (3.2) and (3.3):

$$I_b = I_{OHMIC} = k\left(\left(V_{GS} - V_{TH}\right)V_{DS} - 0.5V_{DS}^2\right) \approx \frac{k}{8}\left(3V_{DD}^2 - 4V_{DD}V_{TH}\right) \quad (3.2)$$

$$I_d = I_{SAT} = \frac{k}{2}\left(V_{GS} - V_{TH}\right)^2 \approx \frac{k}{2}\left(V_{DD}/2 - V_{TH}\right)^2 \quad (3.3)$$

being V_{TH} the threshold voltage and k the drivability factor equals to

$$k = \mu \frac{\varepsilon_{ox}}{T_{ox}} \frac{W}{L} \quad (3.4)$$

where μ denotes the effective mobility, ε_{ox} the dielectric constant of the gate oxide, T_{ox} the gate oxide thickness, W the channel width and L the channel length. If V_{DD} decreases, both currents decrease also. However, the downstream current decreases more abruptly. If V_{DD} approximates to the minimum value where the defect free circuit can still operate properly (around twice the V_{TH}), the downstream current brings to zero (3.5), while the bridge current does not, as observed in (3.6). Both equations are derived from (3.3) and (3.2) replacing V_{DD} with $2V_{TH}$, respectively.

$$I_d \approx \frac{k}{2}\left(\frac{2V_{TH}}{2} - V_{TH}\right) = \frac{k}{2}(0) = 0 \quad (3.5)$$

$$I_b \approx \frac{k}{8}\left(3\left(2V_{TH}\right)^2 - 8V_{TH}^2\right) = \frac{k}{2}V_{TH}^2 \quad (3.6)$$

A similar behaviour is obtained using the alpha-power model for MOS transistors [162], which is more accurate than the Shockley model. For the same example, the current expressions are determined by (3.7) and (3.8)

$$I_b = I_{OHMIC} = \frac{I_{D0}}{V_{D0}} V_{DS} \left(\frac{V_{GS} - V_{TH}}{V_{DD} - V_{TH}}\right)^{\alpha'/2} \propto \frac{V_{DD}}{2} \quad (3.7)$$

$$I_d = I_{SAT} = I_{D0}\left(\frac{V_{GS} - V_{TH(nMOS)}}{V_{DD} - V_{TH(nMOS)}}\right)^{\alpha'} \propto \left(\frac{V_{DD}/2 - V_{TH(nMOS)}}{V_{DD} - V_{TH(nMOS)}}\right)^{\alpha'} \quad (3.8)$$

where α' is the velocity saturation index, V_{D0} the drain saturation voltage at $V_{GS} = V_{DD}$ and I_{D0} the drain current at $V_{GS} = V_{DS} = V_{DD}$. Notice that for low V_{DD} values ($V_{DD} \approx 2V_{TH}$), the saturated current brings proportional to zero (3.9).

$$I_d \propto \left(\frac{2V_{TH(nMOS)}/2 - V_{TH(nMOS)}}{2V_{TH(nMOS)} - V_{TH(nMOS)}} \right)^{\alpha'} = \left(\frac{0}{V_{TH(nMOS)}} \right)^{\alpha'} = 0 \qquad (3.9)$$

Simulations also corroborate this dependency related to V_{DD}. Figure 3.9 shows the SPICE simulation results for the bridging fault example from Figure 3.7 at different power supply values. Notice how the downstream current is minimized as V_{DD} decreases, to the point that the downstream current becomes negligible (around $V_{DD} = 1.4$ V) and the bridge current (I_b) is practically equal to the total current (I_b+I_d).

Experimental evidence of this behaviour is illustrated in Figure 3.11 and Figure 3.12. The current signature for a real defective device from a 0.18 µm technology has been obtained at nominal ($V_{NOM} = 1.8$ V) and at very low voltage ($V_{VLV} = 1.2$ V). This device is suspected to contain a bridging defect. Observe how at V_{NOM} (Figure 3.11) the current signature has a high number of current steps. However, at V_{VLV} (Figure 3.12), the downstream components are minimized and the highest spread current level from Figure 3.11 (generating more than 1.5 mA) has disappeared and it is included in the previous current level, which is generating around 550µA.

3.2 MULTIPLE LEVEL I_{DDQ} BASED DIAGNOSIS

This section describes the multiple level I_{DDQ} based diagnosis methodology for bridging faults. It is a cause-effect methodology, since it requires the use of a fault dictionary. This technique is based on the rich current information provided by the different excitations of the bridged networks. Furthermore, I_{DDQ} measurements at low voltages are used to minimize the impact of downstream currents [160].

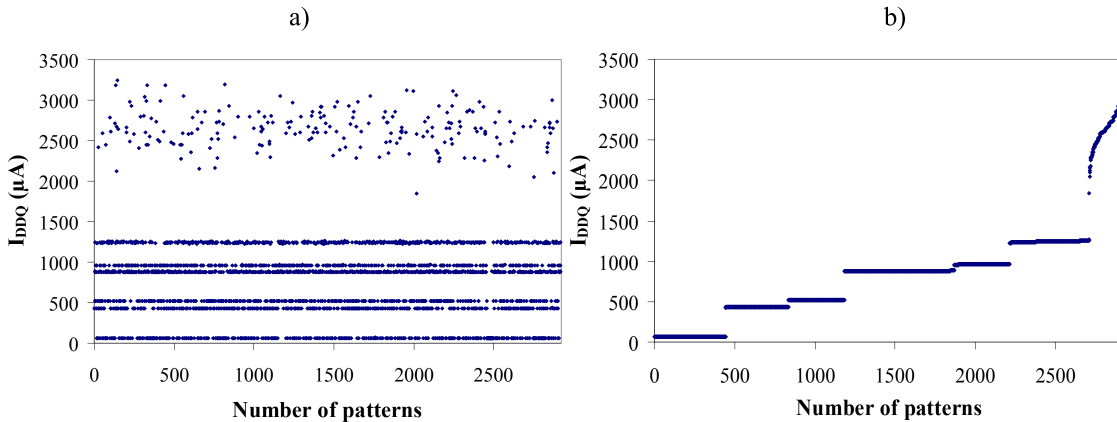

Figure 3.11. Current measurements at V_{NOM} (1.8 V) for a defective device a) Non-ordered b) Ordered.

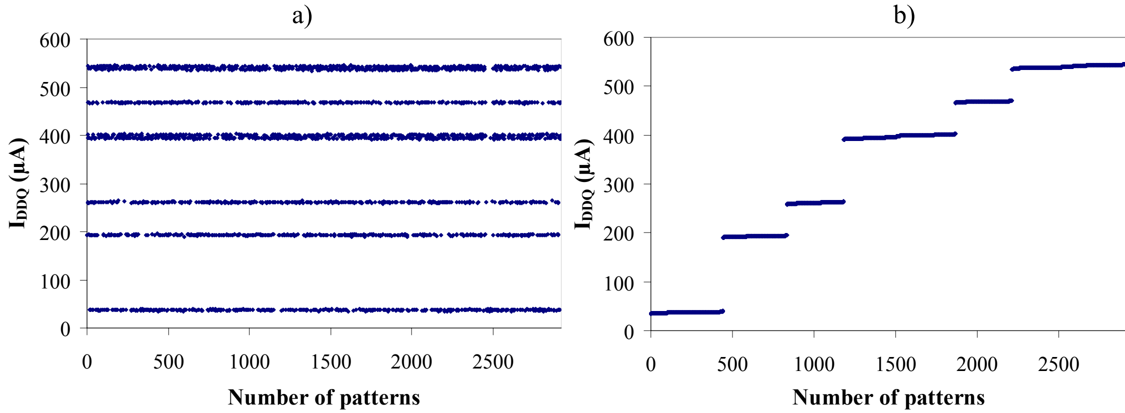

Figure 3.12. Current measurements at V_{VLV} (1.2 V) for a defective device a) Non-ordered b) Ordered.

3.2.1 SIMPLE LINEAR REGRESSION

The purpose of the multiple level I_{DDQ} based fault methodology is to differentiate between the current added by the different excitations of the bridged networks. For that purpose, the simple linear regression model is applied in order to relate the current measurements obtained on the tester and the corresponding currents predicted by the simulation of the bridging faults stored in a dictionary.

The simple linear regression [163] is a model with a single regressor variable x that has a relationship with the response y. It is a linear relationship, as described in (3.10):

$$y = \beta_0 + \beta_1 x + \varepsilon \qquad (3.10)$$

where β_0 and β_1 are unknown constants and ε is the random error component. The error is assumed to have mean zero and unknown variance. β_0 and β_1 are called regression coefficients. β_1 is the regression line slope, i.e., it is the change in the mean of the distribution of y produced by a unit change in x. β_0 is the intercept point, i.e., the mean of the distribution of the response y when x = 0. The parameters β_0 and β_1 are estimated using sample data. Supposing n pairs of data (y_1, x_1), (y_2, x_2), …, (y_n, x_n), the least squares method is used to estimate β_0 and β_1. This method minimizes the sum of the squares of the differences between the observations y_i and the regression line, see Figure 3.13. The expression is described in (3.11)

$$S(\beta_0, \beta_1) = \sum_{i=1}^{n} (y_i - \beta_0 + \beta_1 x_i)^2 \qquad (3.11)$$

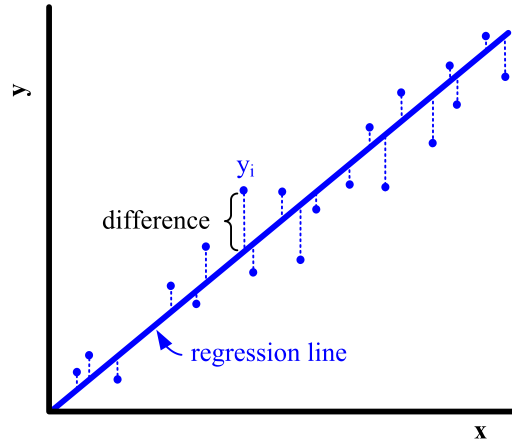

Figure 3.13. Differences between the observation y_i and the regression line.

The estimators of β_0 and β_1 (denoted by $\hat{\beta}_0$ and $\hat{\beta}_1$) must accomplish the following relationships:

$$\left.\frac{\partial S(\beta_0,\beta_1)}{\partial \beta_0}\right|_{\hat{\beta}_0,\hat{\beta}_1} = -2\sum_{i=1}^{n}\left(y_i - \beta_0 + \beta_1 x_i\right) = 0 \tag{3.12}$$

$$\left.\frac{\partial S(\beta_0,\beta_1)}{\partial \beta_1}\right|_{\hat{\beta}_0,\hat{\beta}_1} = -2\sum_{i=1}^{n}\left(y_i - \beta_0 + \beta_1 x_i\right)x_i = 0 \tag{3.13}$$

Simplifying these two equations results in:

$$n\hat{\beta}_0 + \hat{\beta}_1\sum_{i=1}^{n}x_i = \sum_{i=1}^{n}y_i \tag{3.14}$$

and

$$\hat{\beta}_0\sum_{i=1}^{n}x_i + \hat{\beta}_1\sum_{i=1}^{n}x_i^2 = \sum_{i=1}^{n}y_i x_i \tag{3.15}$$

Solving this system of equations for $\hat{\beta}_0$ and $\hat{\beta}_1$ yields:

$$\hat{\beta}_1 = \frac{\sum_{i=1}^{n}y_i x_i - \frac{\left(\sum_{i=1}^{n}y_i\right)\left(\sum_{i=1}^{n}x_i\right)}{n}}{\sum_{i=1}^{n}x_i} \tag{3.16}$$

and

$$\hat{\beta}_0 = \bar{y} - \hat{\beta}_1\bar{x} \tag{3.17}$$

where

$$\bar{x} = \frac{1}{n}\sum_{i=1}^{n} x_i \quad (3.18)$$

and

$$\bar{y} = \frac{1}{n}\sum_{i=1}^{n} y_i \quad (3.19)$$

are the mean values of x_i and y_i, respectively. From (3.17) and (3.16) it is possible to derive the value of the least-squares estimators $\hat{\beta}_0$ and $\hat{\beta}_1$.

3.2.1.1 COEFFICIENT OF DETERMINATION

In a linear regression model, for a given data set, the proportion of variability, which is explained by the model, is known as the coefficient of determination (R^2) [163]. Its expression is given as follows:

$$R^2 = \frac{SS_R}{SS_T} = 1 - \frac{SS_{Res}}{SS_T} \quad (3.20)$$

where SS_R is the model sum of squares, SS_{Res} the error sum of squares and SS_T the total sum of squares. Their corresponding expressions are determined by (3.21), (3.22) and (3.23), respectively.

$$SS_R = \sum_{i=1}^{n}\left(\hat{y}_i - \bar{y}_i\right)^2 \quad (3.21)$$

$$SS_{Res} = \sum_{i=1}^{n}\left(y_i - \hat{y}_i\right)^2 \quad (3.22)$$

$$SS_T = \sum_{i=1}^{n}\left(y_i - \bar{y}_i\right)^2 \quad (3.23)$$

where $\hat{y}_i$ is the y value estimated by the model. The coefficient of determination gives an idea of the proportion of variation of y which can be explained by x. R^2 is comprised in the range [0,1]. Values of R^2 close to 1 imply that most of the variability in y is explained by the regression model. On the contrary, values of R^2 close to 0 mean that none of the variability of y is explained by x. The information given by R^2 should be considered with caution. The coefficient of determination does not measure the slope of

the regression line. It neither measures the appropriateness of the linear model, since R^2 may be large even though *y* and *x* are nonlinearly related.

3.2.1.2 APPLICABILITY OF LINEAR REGRESSION TO BRIDGING FAULTS

Assuming a bridge between two nets on a defective device, the application of the linear regression model consists of relating, for every test pattern, the current measured on the tester with the current predicted by the simulation of the bridging fault. In this way, the model in (3.10) can be rewritten for this particular application as:

$$I_{DDQ(measured)} = I_{DDQ(leakage)} + \beta_1 I_{DDQ(predicted)} \tag{3.24}$$

Provided that the same bridge present in the defective device is simulated (target bridge), if the current measurements are plotted against the predicted (simulated) ones, they are expected to follow a linear model. However, the application of the linear model to this case has the peculiarity that the number of different values obtained by simulation is limited. Assuming nominal parameters during simulations, the different predicted currents depend on the number of different network strengths. Hence, the pair values relating the measurements against the predicted currents should resemble the plot in Figure 3.14a. A set of test patterns reports the same predicted current value with different (although similar) measured values. This set of patterns is exciting the same bridged networks, that is why they correspond to a current level on a current signature. The differences between the measured values on the same group are mainly caused by leakage current variability. Calculating the least-squares estimators, the regression line slope (β_1) is expected to be close to 1. On the other hand, the intercept point of the regression line should not be the origin, but the leakage current of the circuit ($\beta_0 = I_{DDQ(leakage)}$). The reason is that $I_{DDQ(measured)}$ is the sum of the leakage current and the current caused by the bridging defect, when excited. Nevertheless, for the prediction value ($I_{DDQ(predicted)}$), only the bridge current (I_b) is simulated.

The coefficient of determination should be close to 1, but it can not be exactly 1. This model cannot explain the variability related to 'pure' error, which in this application is caused by leakage current variability. For this reason, it is expected that a set of patterns predicting the same value reports different measured values on the tester.

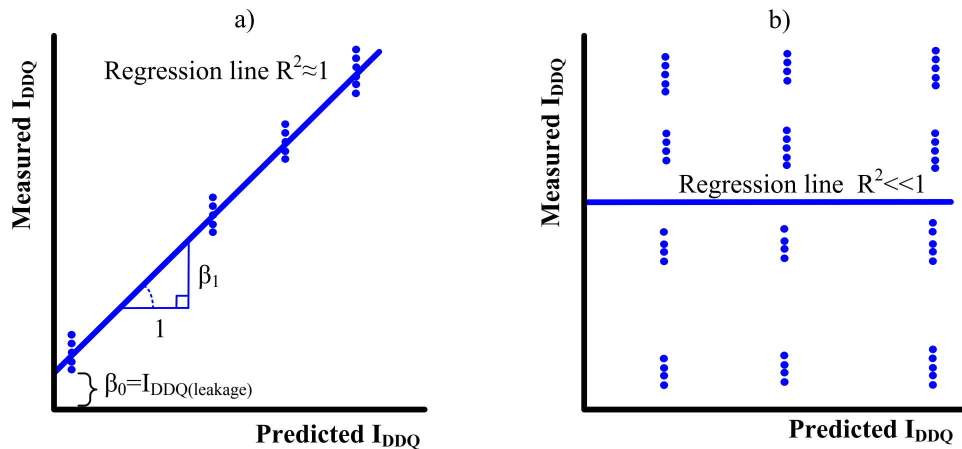

Figure 3.14. Predicted vs. measured current a) Target bridge b) Non-target bridge.

Assume now the prediction of a bridge between two nets different from the ones involved in the bridge of the device. In this case, for every test pattern, a non-related current value is predicted for every measured one. Therefore, for every current predicted by simulation, *n* different groups of points are obtained, where *n* corresponds to the number of network strengths excited by the test patters, as illustrated in Figure 3.14b. Notice that the points are not aligned anymore, but a scattered plot is obtained. The coefficient of determination has then a low value and the regression line slope is far from the unity.

The application of the linear regression model to bridging faults makes possible to determine which bridge is causing the experimental behaviour measured on the tester. Confident results can be obtained with a relative low number of data points (I_{DDQ} measurements) as long as the excitation of different networks is assured.

3.2.2 MULTIPLE LEVEL I_{DDQ} FAULT MODEL

Assume a generic bridge connecting *Net A* and *Net B* as pointed out in Figure 3.15. For every combination of the inputs of *Gate 1* and *Gate 2*, driving *Net A* and *Net B*, respectively, the active networks are different. In some cases, the bridge is not activated and no current is added by the fault. Assume that the current added by the bridge for every input combination is known by simulation. The next step consists in knowing for every test pattern (TP_i) which is the current predicted by simulation ($I_b(NW_{TPi})$). For that purpose, transistor information of *Gate 1* and *Gate 2* is required to know the activated bridged networks (NW_{TPi}) for every test pattern. This predicted value is then related with the current measured for the real device ($I_{DDQ}(TP_i)$) for the same test

pattern. For an *n* number of patterns, there are *n* pairs of values relating the tester current with the simulated current.

Now the linear regression is carried out for these *n* samples and the coefficient of determination (R^2) and the regression line slope (β_1) are calculated. When applying this method to a set of suspicious bridges, only one candidate should be reported with a R^2 and β_1 close to 1. The rest of candidates are expected to be reported with low R^2 and/or different β_1 values. All these steps required for the application of the multiple level I_{DDQ} fault model are described in the diagram of Figure 3.15

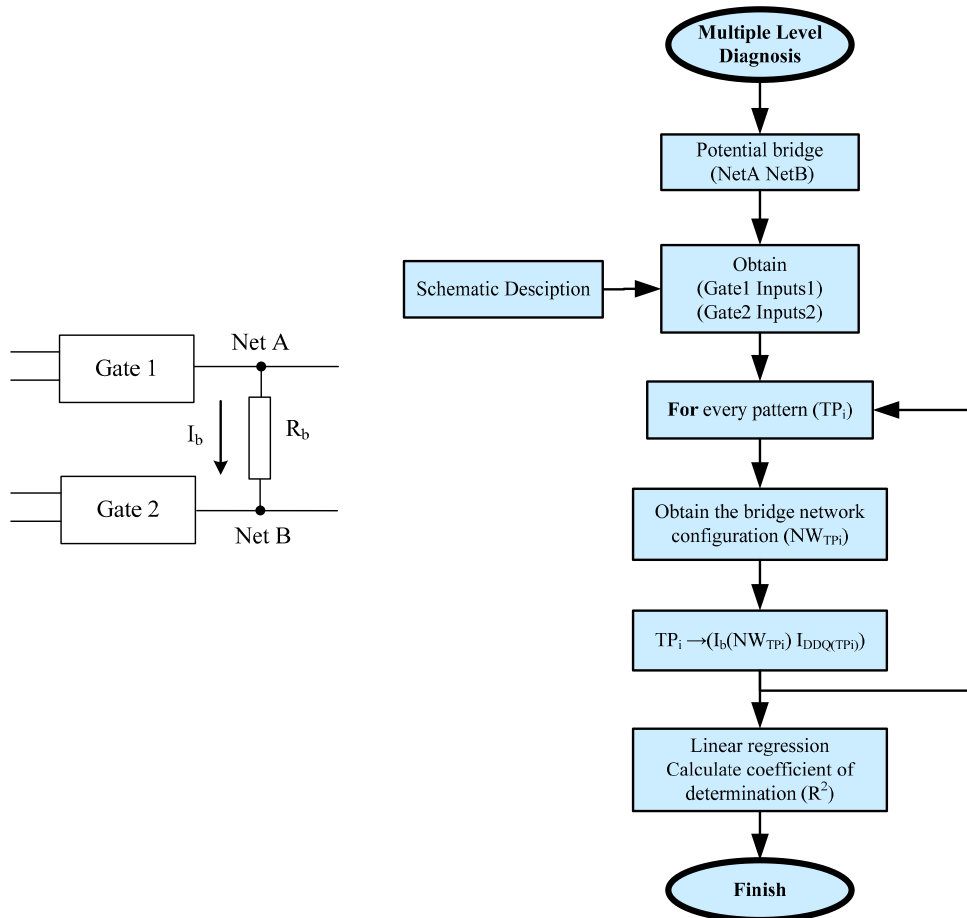

Figure 3.15. Multiple level I_{DDQ} fault model diagram.

3.2.3 FAULT DICTIONARY

The application of this methodology requires a database of predictions of currents caused by the bridge. For this reason, a fault dictionary is used. This fault dictionary consists in storing the current results obtained by SPICE simulations between every possible combination of instances (for a given technology) with their outputs bridged. The simulations consider the different bridged networks configurations. Thus, the

information corresponding to the bridge current (I_{bi}) is saved for every different network excitation (NW_i), as described in Figure 3.16. Notice that the downstream current is not considered in the simulations.

When carrying out the simulations, the bridge resistance value must be determined. However, the resistance value is an unknown parameter. Based on previous works, most of the bridges have been found to be low resistive [9]. In fact, this thesis is focusing on devices that did not pass a logic (SA) test. Thus, running the simulations with negligible resistance value is a realistic assumption that will address most of the bridges.

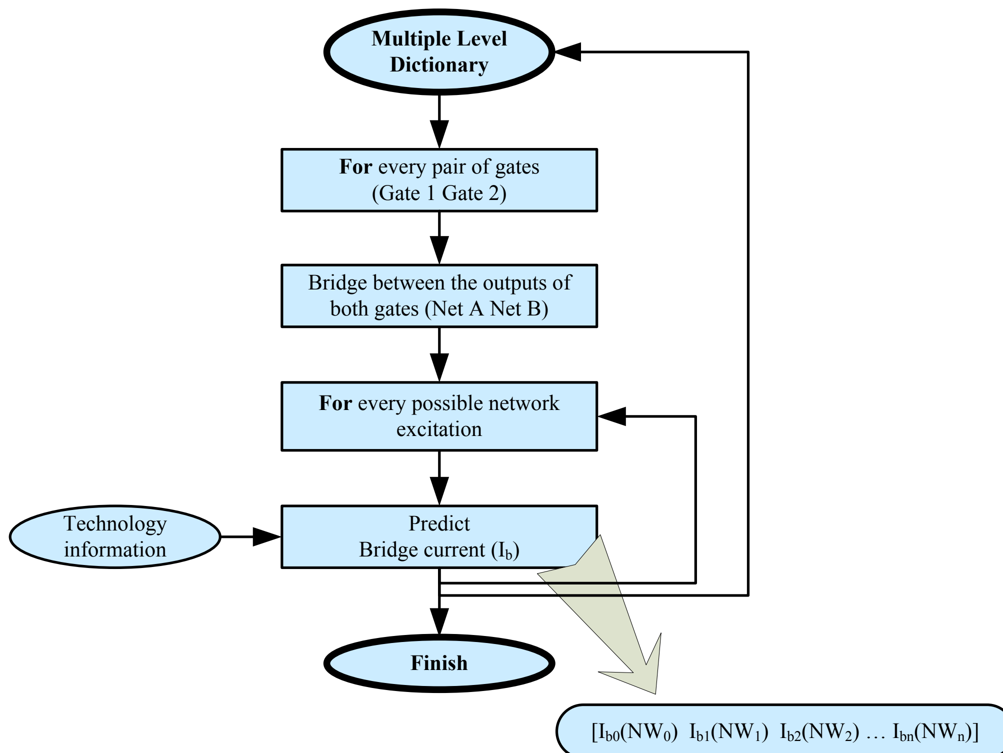

Figure 3.16. Fault dictionary.

The construction of the dictionary can be time consuming. However, it must be made only once for every technology. Furthermore, if a new instance is lately added to the technology, the fault dictionary can be updated.

3.2.4 Impact Of Downstream Current

It has been previously reported (Section 3.1) the impact of downstream current in the presence of bridging defects. Regarding the application of the multiple level I_{DDQ} fault model, the presence of downstream current may degrade diagnosis results. Figure 3.17 illustrates the measured current against the predicted current data points for a

general case in the presence of downstream current. It causes higher measured currents than the predicted ones. Therefore, compared to the same case without downstream current (Figure 3.14a), the coefficient of determination R^2 is lower and the regression line slope (β_1) is higher than the expected unity value. In those cases, I_{DDQ} tests as well as simulations carried out at low V_{DD} values are desirable, since the downstream components are reduced and their impact on diagnosis results minimized, as presented in Section 3.1.

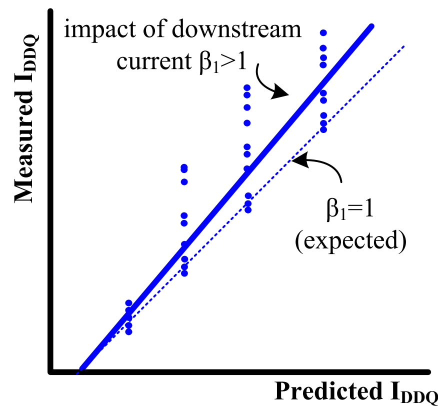

Figure 3.17. Predicted vs. measured I_{DDQ} values in the presence of downstream current.

3.2.5 DIAGNOSIS ALGORITHM

The diagnosis algorithm applied to the defective devices consists of two steps: a logic based diagnosis followed by the current based diagnosis. The first step is carried out by the *Faloc* diagnosis tool [164] from *NXP Semiconductors*.

For a circuit composed of *l* nets, there are $\binom{l}{2}$ possible bridges, which is unfeasible even for small circuits. The use of layout information decreases the number of possible bridges, but it is still high. Therefore, during the first step, the diagnosis tool simplifies the problem. During the application of the current based diagnosis the problem is then limited to a few potential bridges. Hence, the results given by the diagnosis tool is the starting point for the second step, where the current diagnosis methodology is applied for the localization of bridging faults.

3.2.5.1 LOGIC BASED DIAGNOSIS

Faloc (‘*Fa*ult *Loc*alisation’) is a diagnosis tool from *NXP Semiconductors* which provides fast fault localization for real devices failing on a test system or during logic simulation. Faulty test vector and device pin numbers are analysed in order to isolate the source of a particular production or design error. This software relies on the stuck-at, the

failing net, the failing branch, the bridging and the delay fault models. *Faloc* generates a listing file (*.lis*) which contains a compact summary of the diagnosis results. For each possible fault candidate, two quality values are evaluated: Matching and Prediction. On the one hand, the Matching value (*M*) quantifies the tester failing results which actually match with the faulty signature of a particular fault (see Figure 3.18). On the other hand, the Prediction value (*P*) quantifies how many failures predicted by a particular fault are really observed on the tester. The definition of both quality values are described in (3.25) and (3.26), respectively. The higher the calculated quality values for a possible fail candidate, the higher is the probability that this fail candidate causes the reported failing patterns. The ideal case is when $M = P = 100\%$. The tool gives a list of candidates ordered in decreasing order based on the values of Matching and Prediction.

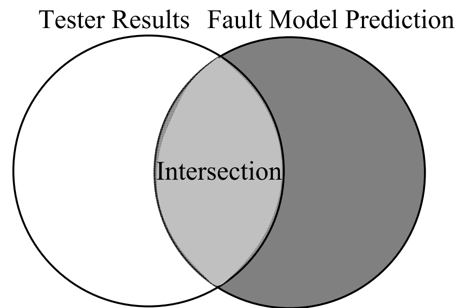

Figure 3.18. Graphical representation of the quality parameters.

$$\text{Matching } (M) = \frac{|\text{Tester Results} \cap \text{Fault Model Prediction}|}{|\text{Tester Results}|} x100\% \qquad (3.25)$$

$$\text{Prediction } (P) = \frac{|\text{Tester Results} \cap \text{Fault Model Prediction}|}{|\text{Fault Model Prediction}|} x100\% \qquad (3.26)$$

3.2.5.2 CURRENT BASED DIAGNOSIS

The candidate list reported by the diagnosis tool is the starting point for the proposed current based diagnosis. Figure 3.19 describes the diagram flow for the diagnosis of bridging defects. The first step consists of deciding if the faulty device is suspected to contain a bridging fault, once the logic diagnosis results haven been evaluated. If so, an I_{DDQ} test is applied. By analyzing the I_{DDQ} measurements, the next decision is made. If the current behaviour still resembles a bridge behaviour, the next step is taken. In the presence of downstream current, these measurements are taken at low power supply value. Subsequently, from the *.lis* file from *Faloc*, the candidates

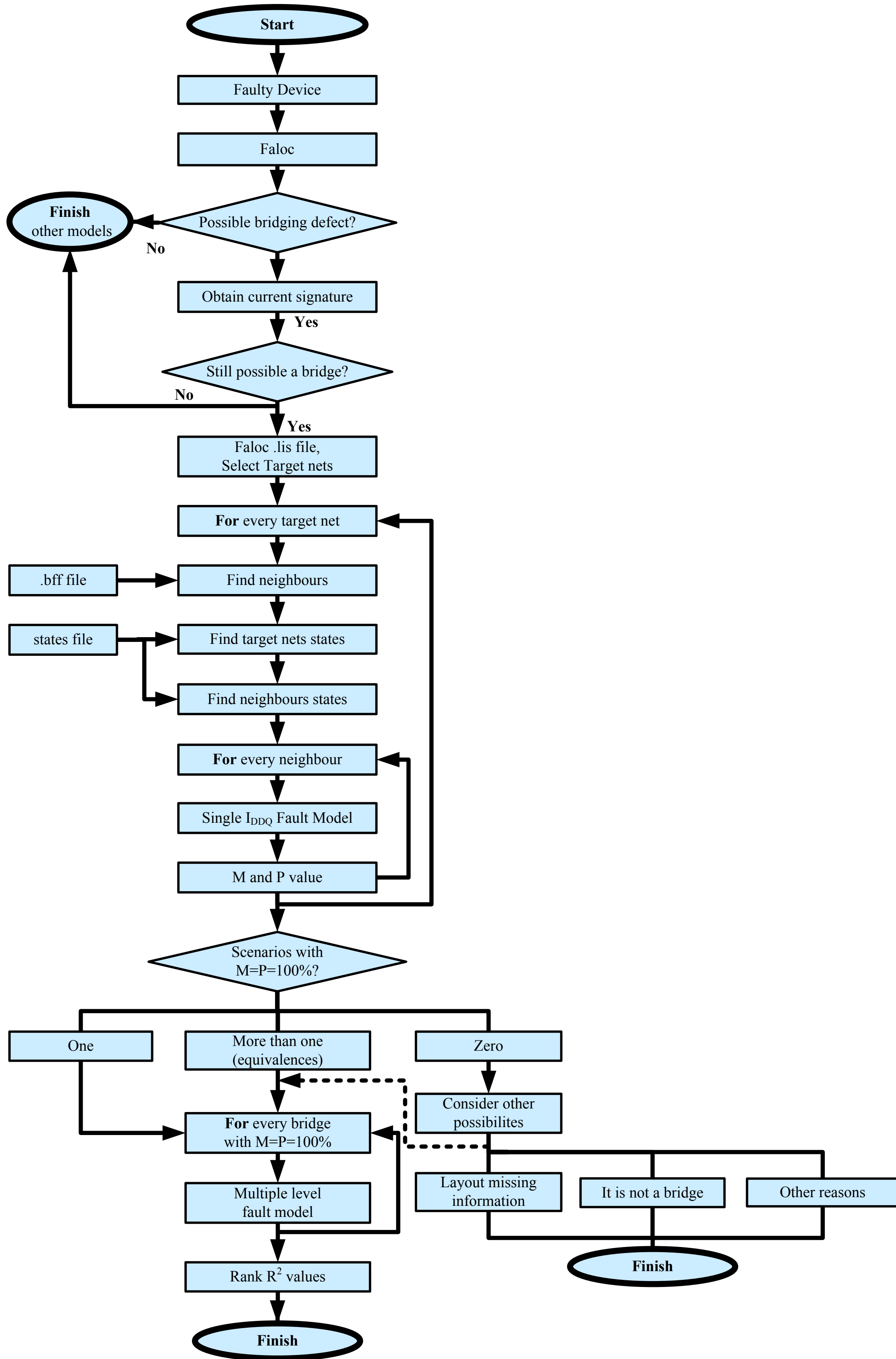

Figure 3.19. Diagnosis flow for bridging defects.

(target nets) which are susceptible to belong to the bridge are selected. Next, for every target net, the neighbours routed closer than a certain minimum distance are found, i.e. the nets to which the target net can be bridged. In this step, layout information (*.bff* file) is used to reduce the candidate pairs. Subsequently, for every I_{DDQ} pattern, the logic states of the target net and its neighbours are saved. With this information, the simple I_{DDQ} bridging fault model for all the candidate pairs is first applied and the results using the same quality parameters (Matching and Prediction) are reported. For all the candidates with the highest values (100%) for both M and P, the information about the gates and the inputs of these gates driving the potential bridged nets is saved. The simple I_{DDQ} bridging fault model has still been considered because its use is feasible for the scope of this thesis (0.18 μm and 90 nm technologies) and reduces even more the number of fault candidates to be considered by the multiple level I_{DDQ} based fault model, which decreases the diagnosis time.

Finally, the multiple level I_{DDQ} based fault model is applied and R^2 and β_1 calculated. In case of more than one candidate, it is possible now to discriminate between equivalent bridges under the assumption of the simple I_{DDQ} bridging fault model. If there is only one, the multiple level I_{DDQ} based fault model should corroborate the results. In case no bridge is reported with M = P = 100%, no success is expected applying the multiple level I_{DDQ} based fault model. Different possibilities can be considered, which are explained in Section 3.2.7.

3.2.6 EXPERIMENTAL RESULTS

Let us demonstrate the usefulness of the proposed method by showing some experimental results obtained for real defective devices. Device 60 is a *Vector4* device from a 0.18 μm technology of *NXP Semiconductors*. The results of the I_{DDQ} test are depicted in Figure 3.20. Three current levels are observed. In the first step, once saved the logic failure information, the diagnosis tool reported that the most probable fault explaining the logic behaviour is a SA1 fault at port A of a complex gate or an equivalent internal fault inside the same gate. In the second step, after the application of the simple I_{DDQ} bridging fault model, two faults can still explain the behaviour of this device. They are logically equivalent and are a) an internal bridge between port *B* and an internal net and b) a bridge between V_{DD} and port *A*, as illustrated in Figure 3.21a and 3.21b, respectively. Both scenarios logically behave in the same way because port *B*

is managed by a strong buffer, dominating the internal net. The multiple level I_{DDQ} bridging fault model has been applied to both scenarios. The plots of the current measured on the tester (y-axis) against the predicted current (x-axis) are illustrated in Figure 3.22a and 3.22b, respectively. Observe that both the coefficient of determination R^2 and β_1 are close to 1 for the internal bridge. However, for the bridge between V_{DD} and port *A*, R^2 is only 0.5 and β_1 0.4.

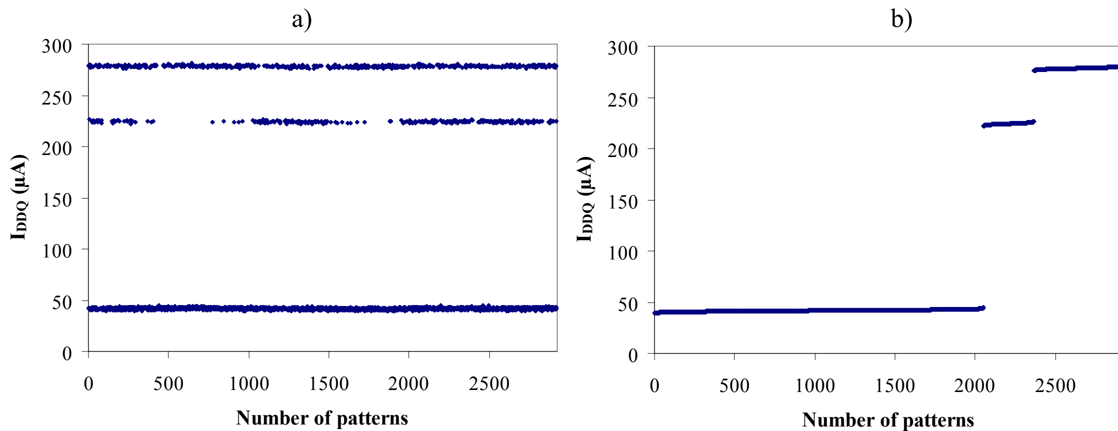

Figure 3.20. Current measurements for Device 60 a) Non-ordered b) Ordered.

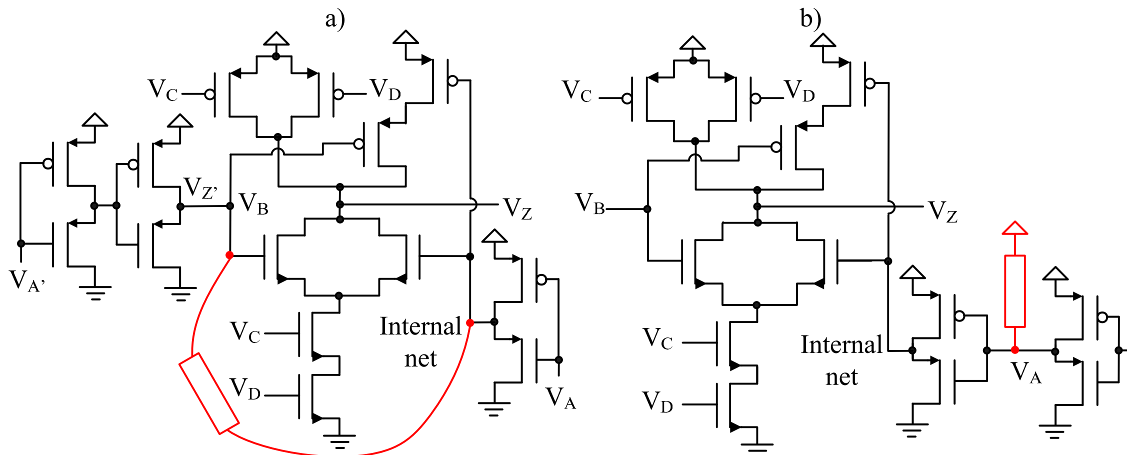

Figure 3.21. Bridge candidates a) Internal b) Between port A and V_{DD}.

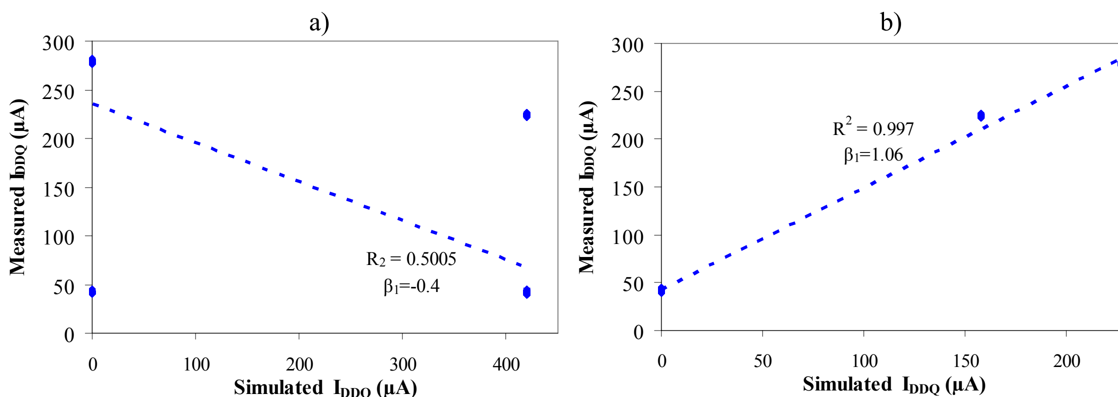

Figure 3.22. Linear regression for the bridge candidates a) Internal b) Between port A and V_{DD}.

Another *Vector4* device is presented next where the use of I_{DDQ} measurements at low power supply value is determinant for the correct diagnosis of the defect. This device (Device 92) reported different number of failing vectors based on the power supply voltage. When carrying out the I_{DDQ} test at V_{NOM}, many downstream components were observed, which were minimized at V_{VLV} (see Figures 3.23 and 3.24). The logic diagnosis could not precisely explain the behaviour of this device. Based on the logic behaviour, the most probable fault reported by the diagnosis tool was a failing branch at the output of the inverter or a failing net at the output of the 2-input NAND gate (V_B), see Figure 3.25a. After applying the current based methodology (using the I_{DDQ} measurements at VLV), there was only one scenario reported with R^2 and β_1 close to one. It is a bridge between the input and the output of the 2-input NAND gate, as described in Figure 3.25. The measured against the predicted currents at V_{VLV} are illustrated in Figure 3.26b. The aspect of the current signature at V_{NOM} is due to the downstream currents of four NAND gates driven by V_A. For that reason, applying the diagnosis methodology at V_{NOM}, it is obtained R^2 = 0.849 and β_1 = 1.40. Notice the impact of the downstream currents in Figure 3.26b.

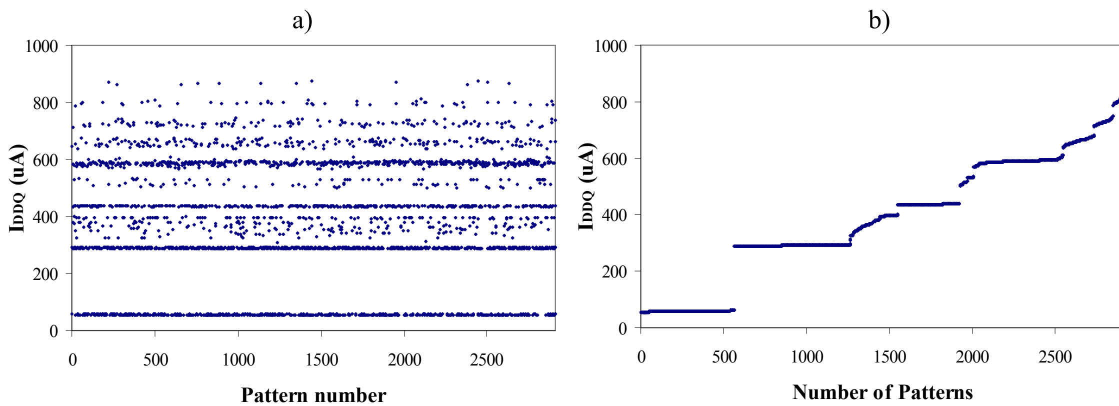

Figure 3.23. Current signature at V_{NOM} for Device 92 a) Non-ordered b) Ordered.

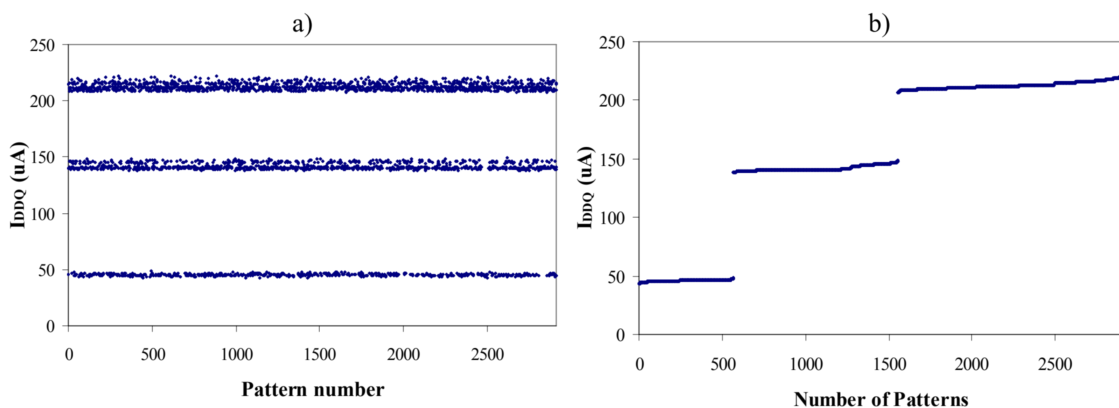

Figure 3.24. Current signature at V_{VLV} for a Device 92 a) Non-ordered b) Ordered.

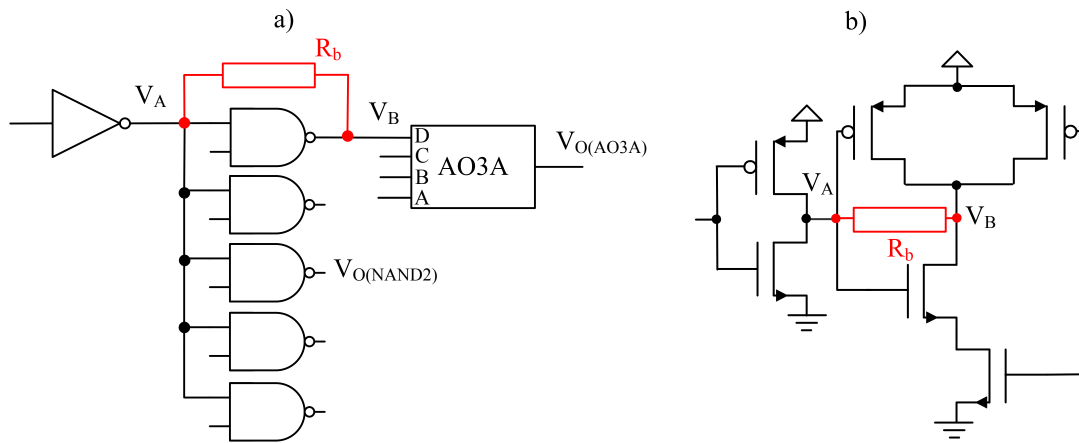

Figure 3.25. Bridge in Device 92 a) Gate level b) Transistor level.

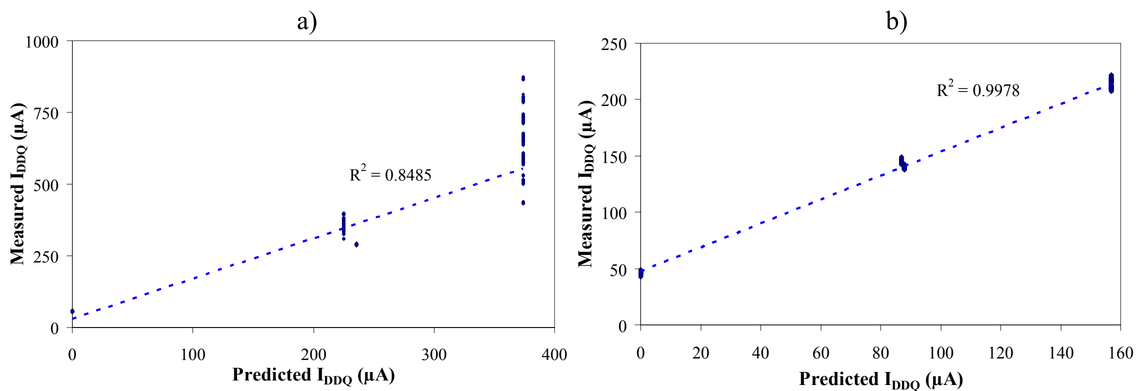

Figure 3.26. Linear regression of the bridge candidate for Device 92 a) V_{NOM} b) V_{VLV}.

3.2.7 LIMITATIONS

There are some circumstances under which a bridge may not be properly diagnosed with the proposed methodology. One of the limitations is due to the simplification of the number of potential bridges considered based on layout information. This step reduces significantly the time required for the diagnosis procedure. However, the bridge (*.bff)* file used in this work containing the potential bridges has some simplifications. It only looks for possible bridges on the interconnect layers. It means that bridges between different metal layers are neglected [124]. Potential bridges in the polysicilicon layer are neither considered. Furthermore, metal tracks belonging to the instance cell does not belong to the interconnect, thus they are also neglected by the bridge extractor. All these reasons may cause some bridges not to be diagnosed simply because they are not in the bridge file. Improvements in extractor tools should lead to the overcoming of this limitation.

The fault dictionary only considers bridges between two nets. It could handle bridges between more nets, but the size of the dictionary would be prohibitive. A few cases have been found where the bridge is involving more than two nets, see the results in Chapter 5. However, the efficient processing of these suppositions is out the scope of this thesis. Furthermore, bridges causing feedback loops generating oscillations or unexpected behaviours may not be properly addressed by the method in its present form.

The bridge resistance has also an impact on the diagnosability of bridging defects. However, few resistive bridges are expected to be found on the set of defective devices under study. Two are the reasons of this fact. On the one hand, the majority of the bridges affecting ICs are low resistive. On the other hand, the set of defective devices are expected to have hard fails, since they did not pass the SA test. Anyway, the impact of the bridge resistance is analysed next. The fault dictionary is built based on the assumption of negligible resistance value. Figures 3.27a and 3.28a show two particular examples of resistive bridging faults. SPICE simulations have been carried out for a 0.18 μm technology activating all the possible networks and sweeping the bridge resistance value. Figures 3.27b and 3.28b summarize these simulations results. The bridge currents for different resistances obtained by simulation are plotted against the bridge current assuming negligible bridge resistance (also from simulation). Certainly, comparing the results assuming a short (R_b = 0) against itself results in a perfect alignment of the data points. However, as it is compared to higher resistance values (in the order of kΩs), the points are not aligned anymore. When R_b = 2 kΩ, the misalignment is not significant. The equivalent resistances of the transistor networks still dominate the electrical behaviour. However, when the bridge resistance approximates the equivalent resistance of the transistor networks, the current flowing through the bridge depends on the bridge resistance. When the bridge resistance is higher, it dominates the electrical behaviour so that the flowing current is almost independent of the excited transistor networks, as observed in Figures 3.27b and 3.28b for high R_b values. In these cases, the sample points do not follow a line anymore and neither R^2 nor β_1 approximate the expected unity value. Both values are lower as the bridge resistance increases. Similar results have been obtained for bridges involving different instances.

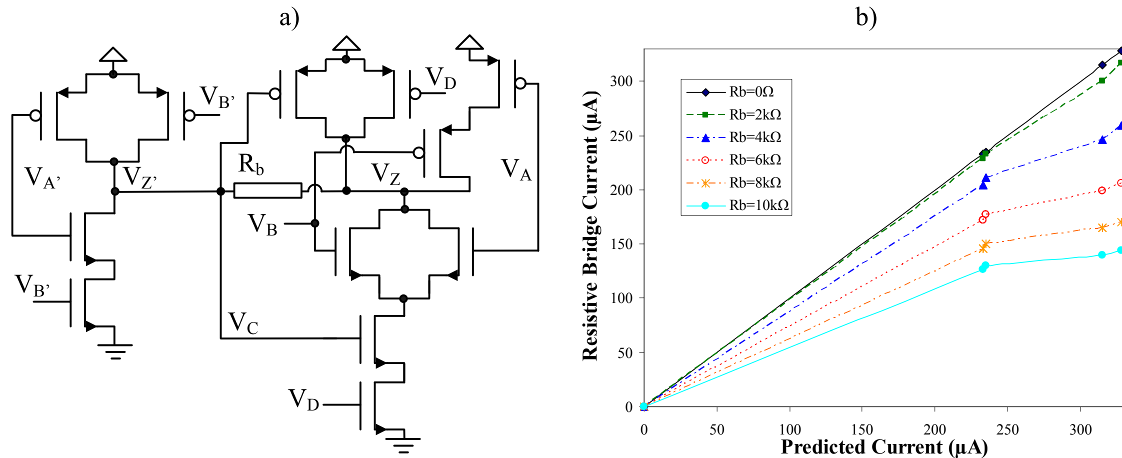

Figure 3.27. Resistive bridging fault example I a) Transistor level b) Simulation results.

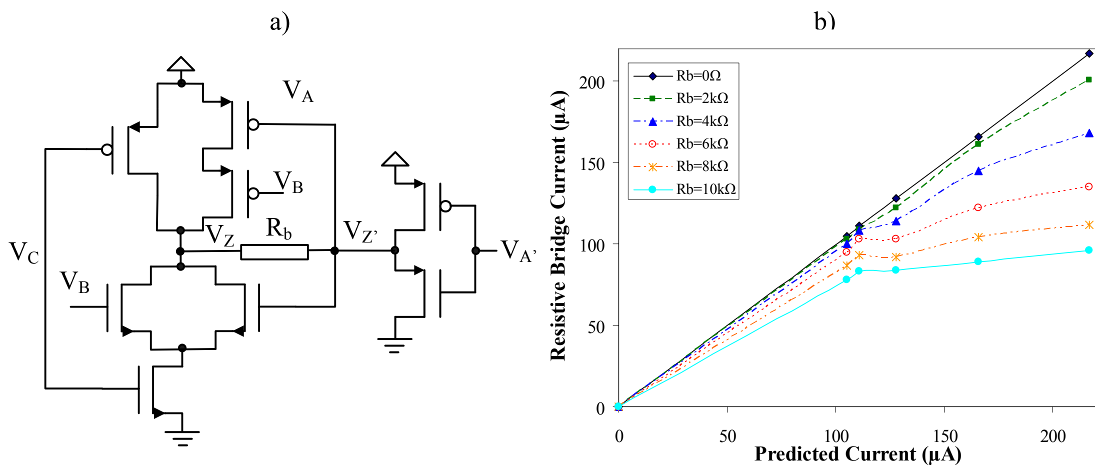

Figure 3.28. Resistive bridging fault example II a) Transistor level b) Simulation results.

Simulation results show that up to a few kΩs, the application of the linear regression model is still valid. The voltage degradation on the bridged nets is not so marked for resistive bridges. Therefore, they may even pass the logic test. In fact, as intermediate voltages are less probable in resistive bridge, they are not expected to cause downstream current. Anyway, in the the next section shmoo plots are presebted as an alternative method for the diagnosis of resistive bridges.

Finally, another factor to be commented for the diagnosis procedure is the impact of leakage current with the shrinking of technology dimensions. The applicability of this method is subjected to the distinction between currents caused by the bridges and leakage currents. It is known that the distinction of defect currents is more difficult for every new technology. However, in this thesis it is proven that it has success for 0.18 µm and 90 nm technology devices (see Chapter 5). The continuity of its applicability depends on different factors: device performance (it may be not feasible to high

performance devices), design techniques that decreases leakage currents in test mode and the use of statistical processing of data prior or during the application of the diagnosis methodology.

3.3 EFFECTIVENESS OF SHMOO PLOTS FOR BRIDGING DEFECTS

Shmoo plots have been used as a vehicle to test defective circuits as well as to help in the diagnostic phase [165]. They can be useful especially as an alternative to current methodologies. Variations in the circuit supply voltage cause defects to have different defective behaviours depending on the clock period length. In this field, it is widely known that VLV testing has been postulated to improve the coverage of resistive bridges [91]. However, some resistive bridges may show a different behaviour. Some works have reported examples where lowering the power supply does not improve the detection of such faults [166]-[167]. Nevertheless, no exhaustive explanation about the circumstances causing this behaviour has been reported. In this section, it is explained the reasons for this behaviour and how it can be easily observed by means of Shmoo plots [168].

3.3.1 SHMOO PLOTS

For the generation of Shmoo plots, a set of input test patterns is fed into the DUT (Device Under Test) for different supply voltages with values ranging from below to above the nominal V_{DD}. At each particular V_{DD}, the circuit is run at different frequencies below and above the nominal speed. For each pair of working conditions (V_{DD} and frequency), the correctness of the circuit is recorded as a pass/fail response. As an example, observe a typical Shmoo plot for a fault free circuit in Figure 3.29a obtained by simulation of a 0.35 µm *AMS* technology. Speed information is shown on the x-axis as the period of the clock signal.

3.3.2 RESISTIVE BRIDGES AT LOW V_{DD}

The resistive nature of bridging defects [9] may result in a wide variety of faulty behaviours. In that direction, VLV testing has been demonstrated to be effective for the detection of resistive bridges. In this sense, consider the circuit in Figure 3.30, where the output of the inverter is bridged to V_{DD}. Assuming a logic 1 at the input of the inverter,

it is well known [136] that a quiescent analysis (long periods in Shmoo plots) concludes that a decrease in the V_{DD} value makes the voltage at the output (V_B) more likely to be interpreted as a high (incorrect) value by the next gates. The reason for this behaviour is the increase of the on-resistance (R_{on}) of the nMOS transistor owing to the decrease of V_{DD} while keeping a constant R_b. As a result, the lower the V_{DD}, the more likely the output voltage (V_B) to be interpreted as incorrect (logic high, in this case). There is a V_{DD} threshold (dependent on R_b) from which the logic quiescent behaviour of the defective circuit is correct, as illustrated in the Shmoo plot in Figure 3.29b, corresponding to the circuit in Figure 3.30 when R_b = 12.5 kΩ. In relation to timing effects (short period times in Shmoo plots), the bridge may turn the defective circuit into slower or faster than the defect-free case. In our example, the defective circuit may become slower, as derived from the comparison between Figures 3.29a and 3.29b.

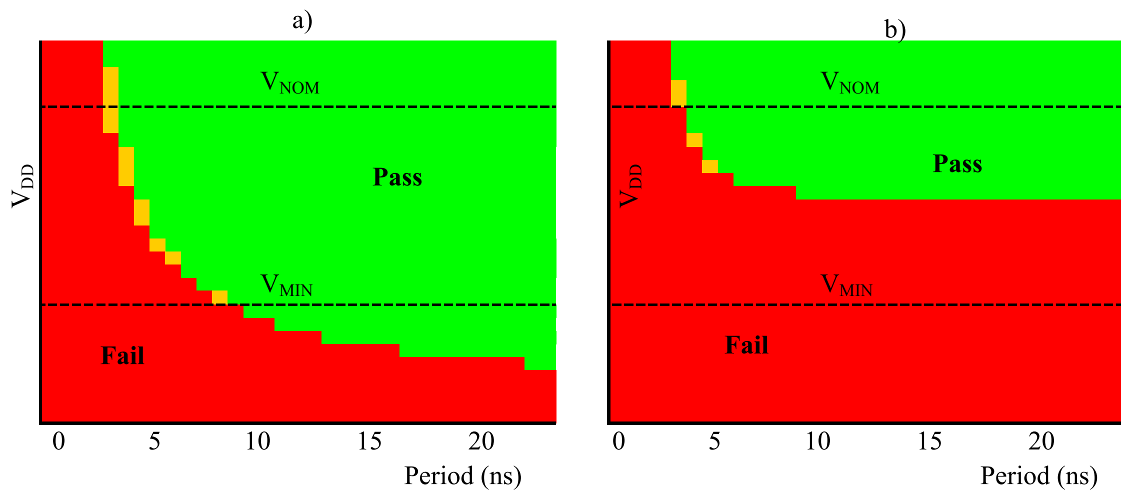

Figure 3.29. Shmoo plot a) Fault free b) Bridging fault with R_b=12.5kΩ.

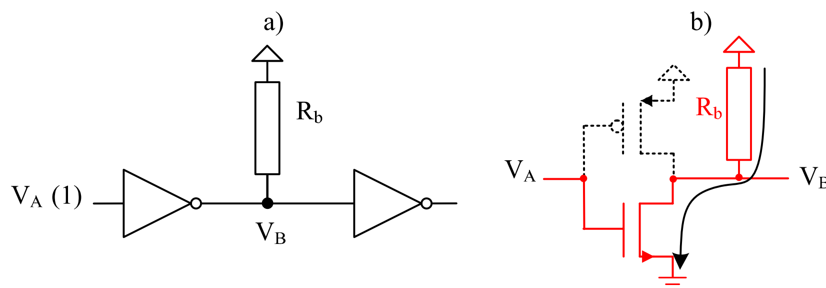

Figure 3.30. Bridging fault a) Gate level b) Transistor level.

3.3.3 RESISTIVE BRIDGING FAULTS AT HIGH V_{DD}

The typical behaviour reported in Figure 3.29b is not always followed by bridging faults [167]. To show this fact, consider the circuit in Figure 3.31. Let us analyse the

behaviour of the output (V_D) of the inverter with a high voltage at its input. In the fault-free case, V_D is pulled down to ground by the nMOS transistor. However, in presence of the bridge, V_D is also connected to V_{DD} through the pMOS transistor of the other inverter. Depending on the strength of both nMOS and pMOS transistors (and of course on R_b) V_D will range between V_{DD} and V_{GND} and, most likely in real designs, will have an intermediate voltage value. The logic interpretation of the intermediate voltage depends on the logic threshold of the downstream gates fed by V_D (an inverter in this example). It is well accepted that, for an inverter, the logic threshold (V_{LTH}) is an almost constant fraction of V_{DD}, i.e., $V_{LTH} = kV_{DD}$, with k around 1/2 if it is a balanced inverter.

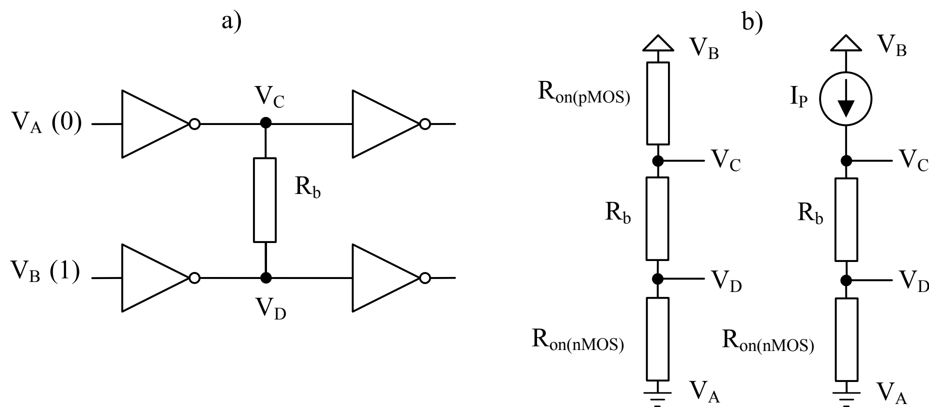

Figure 3.31. Bridging fault connecting two inverters a) Gate level b) Equivalent circuits.

3.3.3.1 IMPACT OF MOBILITY SATURATION

Figure 3.31b shows two possible equivalent circuits modelling the example in Figure 3.31a. Since the V_D value is around $1/2V_{DD}$, the nMOS transistor works in the ohmic region. In the case of a sufficient high V_{DD}, which is true for the practical V_{DD} considered, the pMOS transistor is also in the ohmic region. Thus, the modelling of each transistor with its equivalent on-resistance (left side of Figure 3.31b) is an appropriate approximation for the circuit. The voltage at V_D can be then easily derived by analysing the resistive divider made up of $R_{on(pMOS)}$, R_b and $R_{on(nMOS)}$. By assuming the alpha-power model for the transistors [162], V_D is found to be:

$$V_D = \frac{V_{DD}}{\left(\dfrac{\dfrac{I_{D0(nMOS)}}{V_{D0(nMOS)}}}{\dfrac{I_{D0(pMOS)}}{V_{D0(pMOS)}}}\right)\left(\dfrac{V_{DD}-V_{TH(nMOS)}}{V_{DD}-V_{TH(pMOS)}}\right)^{\alpha'/2} + 1 + R_b\dfrac{I_{D0(nMOS)}}{V_{D0(nMOS)}}\left(V_{DD}-V_{THn}\right)^{\alpha'/2}} \tag{3.27}$$

where $V_{TH(nMOS)}$ and $V_{TH(pMOS)}$ are the threshold voltages of the nMOS and pMOS transistors, respectively and α' is the carrier velocity saturation index. Derived from (3.27), the dependence of V_D on V_{DD} is shown in Figure 3.32a (solid lines) for $\alpha' = 1$ and $\alpha' = 2$. All the parameters in (3.27) have been assumed to be constant. With this assumption, V_D has the chance to cause a logic error only at low V_{DD} values, since the higher the V_{DD}, the lower the V_D. This is not the behaviour found by means of SPICE simulations using experimental-based models for a standard 0.35 µm technology from *AMS*. In this direction, the inclusion of the second-order effect such as the mobility saturation velocity of carriers can model the observed V_D against V_{DD} dependence (see the two dashed lines in Figure 3.32a). Indeed, the assumption of the behaviour followed by μ_n (3.28) causes a different V_D against V_{DD} behaviour, where the higher the V_{DD}, the higher the V_D.

$$\mu_n = \frac{\mu_{n0}}{\left(1 + \mu_{n0} \frac{V_{DS}}{V_{SAT} L_{neff}}\right)} \qquad (3.28)$$

The mobility saturation of electrons is achieved at voltages lower than in the case of holes. This causes the on-resistance of the nMOS transistors to increase stronger with V_{DD} after mobility saturation. For this reason, the strength of the pMOS transistor becomes greater than the strength of the nMOS, and V_D goes proportionally closer to V_{DD}. The Shmoo plot for the example in Figure 3.31a is illustrated in Figure 3.32b. The circuit fails for high V_{DD}s and pass for low V_{DD}s.

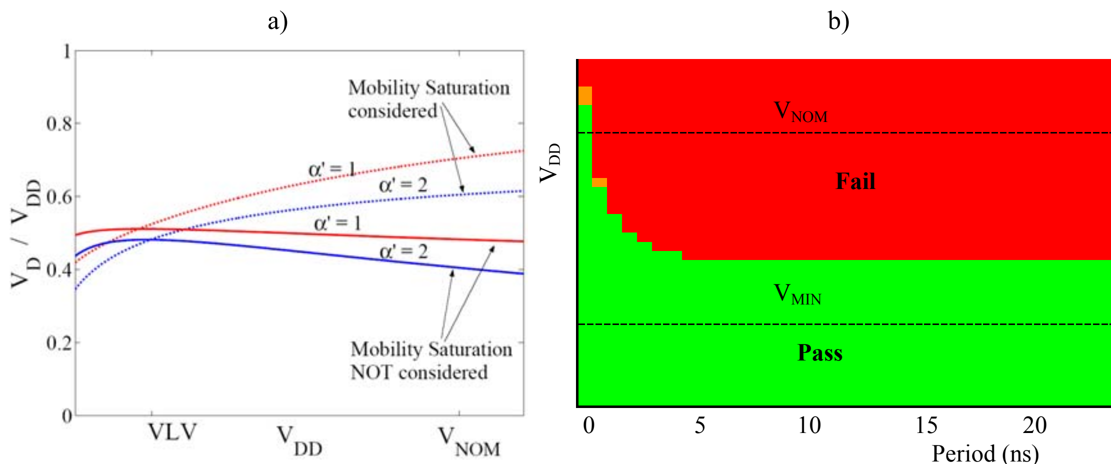

Figure 3.32. Example in Figure 3.31 a) V_D vs. V_{DD}, derived from (3.27) b) Shmoo plot (R_b = 1 kΩ).

3.3.3.2 BRIDGES CONNECTING BASIC LIBRARY GATES

The behaviour where the bridge is better detected at high V_{DD} values is not only limited to a particular bridge between two inverters, but it may appear for any balanced nMOS and pMOS transistor networks able to generate voltages on the bridged nodes around $1/2V_{DD}$. For that purpose, one of the inverters from Figure 3.31a has been replaced by different NAND and NOR gates with 2, 3 and 4 inputs, as in Figure 3.33. The faulty circuits have been simulated using the same *AMS* technology. Shmoo plots detecting the bridges at high V_{DD} values were found in the case of the 2-input and the 3-input NAND gates. Figure 3.34 shows the Shmoo plot for the case of a two input-NAND gate. Notice that for long periods, the bridge is detected at low and high voltages. However, for intermediate V_{DD} values the bridge is not detected. Similar behaviours are obtained for the rest of NAND gates. In the case of NOR gates, the p-network and n-network connected by the bridge are not balanced. V_E is driven by two or more parallel nMOS transistors. Therefore, these bridges are only detected at low V_{DD} values, reporting the classical behaviour.

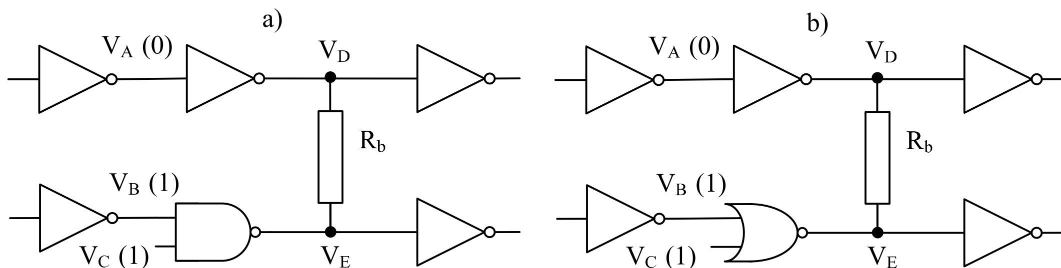

Figure 3.33. Bridging fault a) Including a NAND gate b) Including a NOR gate.

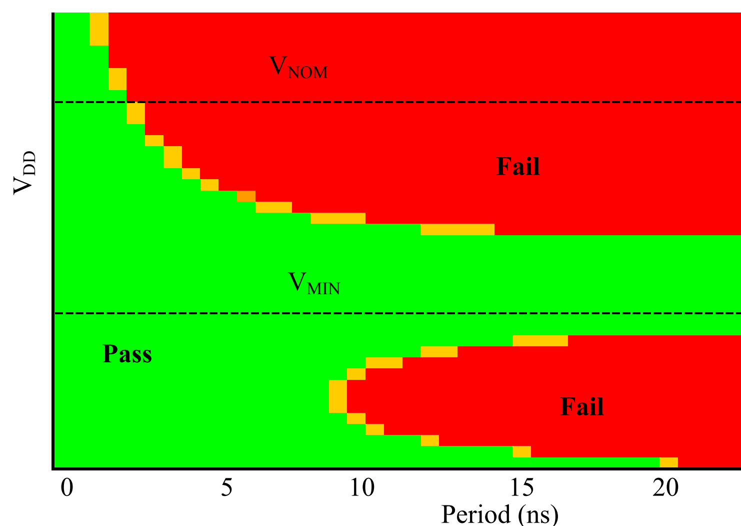

Figure 3.34. Shmoo plot for the circuit in Figure 3.33a (R_b = 1.85 kΩ).

3.3.4 EXPERIMENTAL RESULTS

The results for a real defective device reporting this behaviour is here presented. It is a *Vector4* device (Device 92) from a 0.18 µm technology. This device has been previously presented in Section 3.2.6. It reported different logic behaviours depending on the power supply value. Once applied the current based diagnosis methodology, the device is suspected to contain a bridging defect. The bridge connects one of the inputs and the output of the same 2-input NAND gate, as illustrated in Figure 3.25. Three different network excitations are possible for this bridge, as described in Figure 3.35a, 3.35b and 3.36a, respectively. Two of them always cause logic failures during the voltage test (long periods of the Shmoo plot), no matter the power supply value, as illustrated in Figure 3.35c. However, when both pMOS transistors of the NAND gate are on, logic failures are detected at low and at high V_{DD} values. Nevertheless, this network configuration passes the voltage test at nominal conditions, as described in Figure 3.36, obtaining a similar behaviour to the quiescent analysis (long periods) of the Shmoo plot reported by simulation in Figure 3.34.

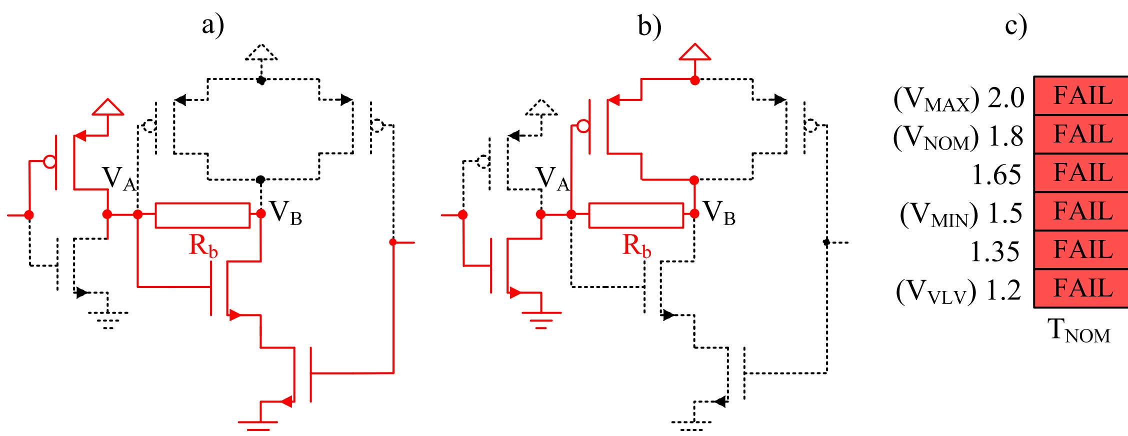

Figure 3.35. Bridge in Device 92 a) Bridge excitation I b) Bridge excitation II c) Experimental logic behaviour for bridge excitations I and II.

SPICE simulations have been carried out with the corresponding 0.18 µm technology from *NXP Semiconductors*, which corroborate the consistency of the experimental results. Figure 3.37 illustrates the simulation results of the voltages of the bridged nodes and the outputs of the downstream gates ($V_{O(NAND)}$ and $V_{O(AO3A)}$ respectively, see Figure 3.25a for more information) for the bridge configuration described in Figure 3.36a. In the fault free case, V_A ($V_{O(NAND)}$) is set to logic 1 (logic 0) whereas V_B ($V_{O(AO3A)}$) is set to logic 0 (logic 1). However, due to the bridge, there is

voltage degradation on the bridged nodes. The behaviour is similar to the one shown in Figure 3.32a, where the voltage of the bridged nodes increases relatively as V_{DD} increases. The voltage degradation on the bridged nodes may cause the propagation of logic errors through the *NAND* and the *AO3A* gates, respectively. Based on the results from Figure 3.37, a logic error is propagated through the *NAND* gate for V_{DD} values higher than 1.93 V (blue shaded area) whereas a logic error is propagated through the *AO3A* for V_{DD} values lower than 1.64 V approximately (red shaded area). Therefore, simulations results show that this bridge configuration is not causing a logic error for V_{DD} between [1.64 V, 1.93 V]. These simulation results are consistent with the fact that at nominal V_{DD} (1.8 V), the tester did not capture logic faulty behaviour for this bridge configuration (Figure 3.36b).

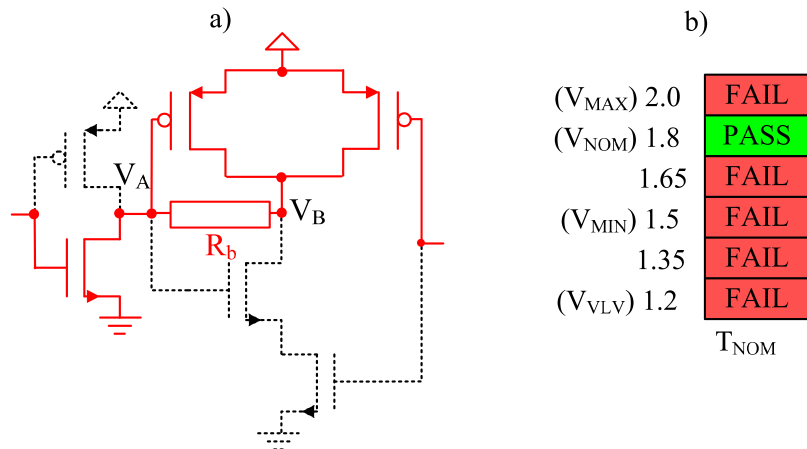

Figure 3.36. Bridge excitation III in Device 92 a) Transistor level b) Experimental logic behaviour.

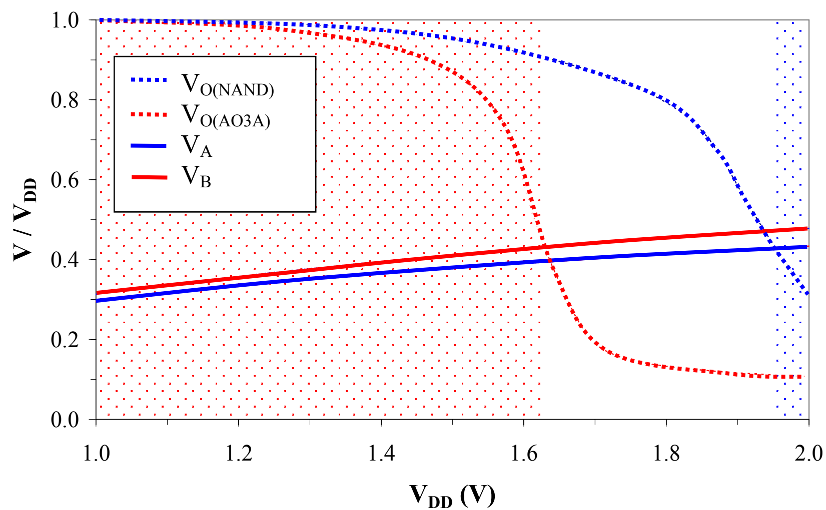

Figure 3.37. Simulation results for the bridge configuration in Figure 3.36a.

3.4 CONCLUSIONS

Diagnosis methodologies developed for bridging faults using voltage based techniques are less efficient in the presence of the Byzantine problem. However, current based techniques overcome this problem provided that the downstream current is treated properly. In this chapter, the downstream current has been analyzed in the presence of bridging faults and its impact has been demonstrated to be minimized at low power supply values [159]-[160]. Furthermore, an effect-cause current diagnosis methodology has been proposed, which considers the strength of the bridged networks excited by every different test pattern [160]. In the presence of downstream current, it is desirable to apply the methodology using I_{DDQ} measurements obtained at low power supply voltages. The feasibility and the usefulness of the diagnosis procedure have been demonstrated and it is expected to remain valid for future technologies as long as current measurements preserve their utility.

On the other hand, an alternative method based on shmoo plots has been demonstrated to be useful also for diagnosis purposes. Traditionally, low voltage has been considered as an advantageous condition for the detection of bridging defects. However, in presence of bridges connecting balanced n- and p-networks, it has been found that the higher the V_{DD} value, the more likely the defective node to be logically interpreted as incorrect by the next gates [168]. Its direct translation into Shmoo plots can be extremely useful for the diagnosis of such defects.

CHAPTER 4. DIAGNOSIS OF INTERCONNECT OPEN DEFECTS

An open defect is missing material causing an electrical discontinuity. This class of defects is frequent in today's CMOS technologies. Hence, the diagnosis of open defects has become of relevant importance. In this field, the diagnosis of interconnect opens [133]-[137] is focusing the major interest since they are the most probable opens to be found in CMOS devices [52]. The majority of interconnect open defects are full opens [54], which cause floating lines [55]-[59]. The behaviour of these floating lines

depends on: the capacitances between the floating line and its neighbouring structures, the transistors capacitances and the trapped charge. In this sense, in the first part of the chapter it is presented an experimental chip, where open defects have been intentionally injected. Results of the fabricated chip related to the impact of parasitic capacitances on the behaviour of both full and resistive open defects are then analyzed. Based on these experimental results, a methodology for the diagnosis of interconnect full open defects is presented in the second part of the chapter. Finally, the behaviour of full open defects in nanometer technologies is analyzed. The gate oxide thickness becomes so thin that the gate tunnelling leakage currents impact the behaviour of interconnect open defects. This factor, which has not been previously analyzed, may become of major importance in future technologies for both test and diagnosis purposes.

4.1 IMPACT OF PARASITIC CAPACITANCES ON INTERCONNECT OPEN DEFECTS

An experimental circuit has been designed and fabricated for the analysis of interconnect open defects [169]. A photograph of one of the samples is illustrated in Figure 4.1a. The chip is composed of two independent designs. The part comprising the present work is detailed in Figure 4.1b. All the experiments applied to these devices have been carried out in the *LIDE III laboratory* of the *Electronic Engineering Department* of the *UPC*.

a) b)

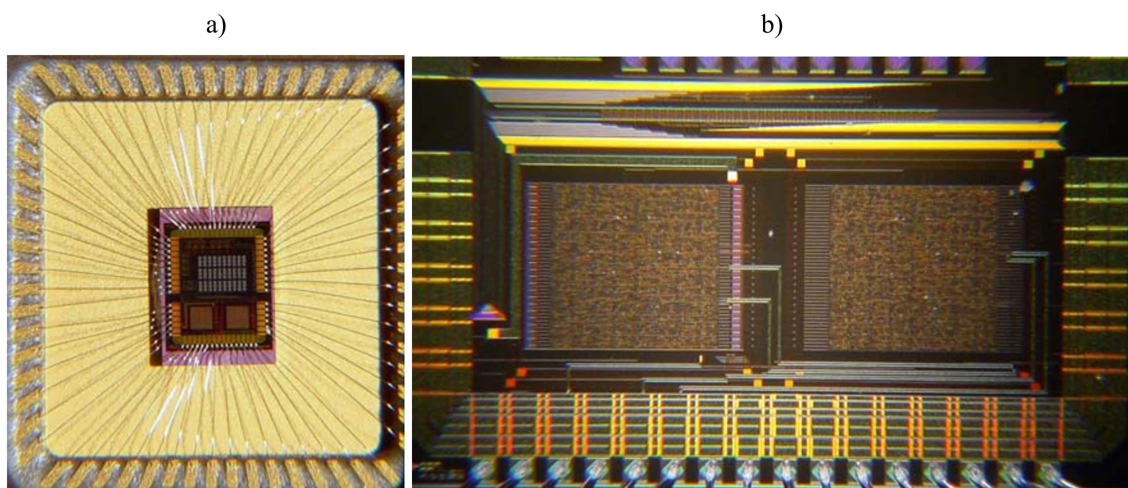

Figure 4.1. Fabricated circuit a) General view b) Detailed view

4.1.1 DESIGN DESCRIPTION

The chip has been designed in 0.35 µm C35 CMOS technology from *AMS*. This technology comprises four metal layers. The goals of the design, focused on both, full open as well as resistive open defects, are summarized as follows:

1. To determine the influence of the capacitive coupled neighbouring lines on the floating line caused by a full open.
2. To determine the impact of the state history of the defective line owing to a resistive open at test application time.
3. To analyze the delay detectability of resistive opens.

The design comprises a group of lines (test lines) routed in parallel as in a bus. A diagram of the circuit is shown in Figure 4.2. There are two types of test lines, i.e., defective and defect-free lines. The defective lines can be divided into two groups, a) those intentionally broken by design, and therefore containing a full open, and b) those containing a transmission gate, which behave as a resistive open. Defect-free lines are inserted in parallel between the defective lines. All the test lines are driven by inverters and, in turn, they drive inverters, too. On the one hand, the inverters controlling each line are fed by the output of an edge triggered flip-flop (FF). On the other hand, every inverter driven by a test line drives, in turn, the *D* port of an edge triggered scan flip-flop. A more detailed description of the design for the two first test lines is illustrated in Figure 4.3.

The two sets of flip-flops constitute a scan register and a hold register. The scan register is composed of scan flip-flops (*SFF*) and the hold register is made up of flip-flops (*FF*) (see Figure 4.3). Both registers have as many flip-flops as test lines. The scan register has two operation modes: shift register mode (*SE* active high) and normal mode (*E* active high). In the shift register mode, the required input vector is scanned in. The normal operation mode captures the values propagated through the test lines (signals D_i in Figure 4.2 and Figure 4.3). The hold register launches the values (P_i signals) on the test lines (Q_i signals) at the required moment, which are subsequently captured by the scan flip-flops.

The circuit uses eight pins, seven of which are inputs (*IN*, *SE1*, *E1*, *E2*, *CLK*, *V1*, *V2*) and one of which is an output (*OUT*). Their functionalities are described in the following paragraphs.

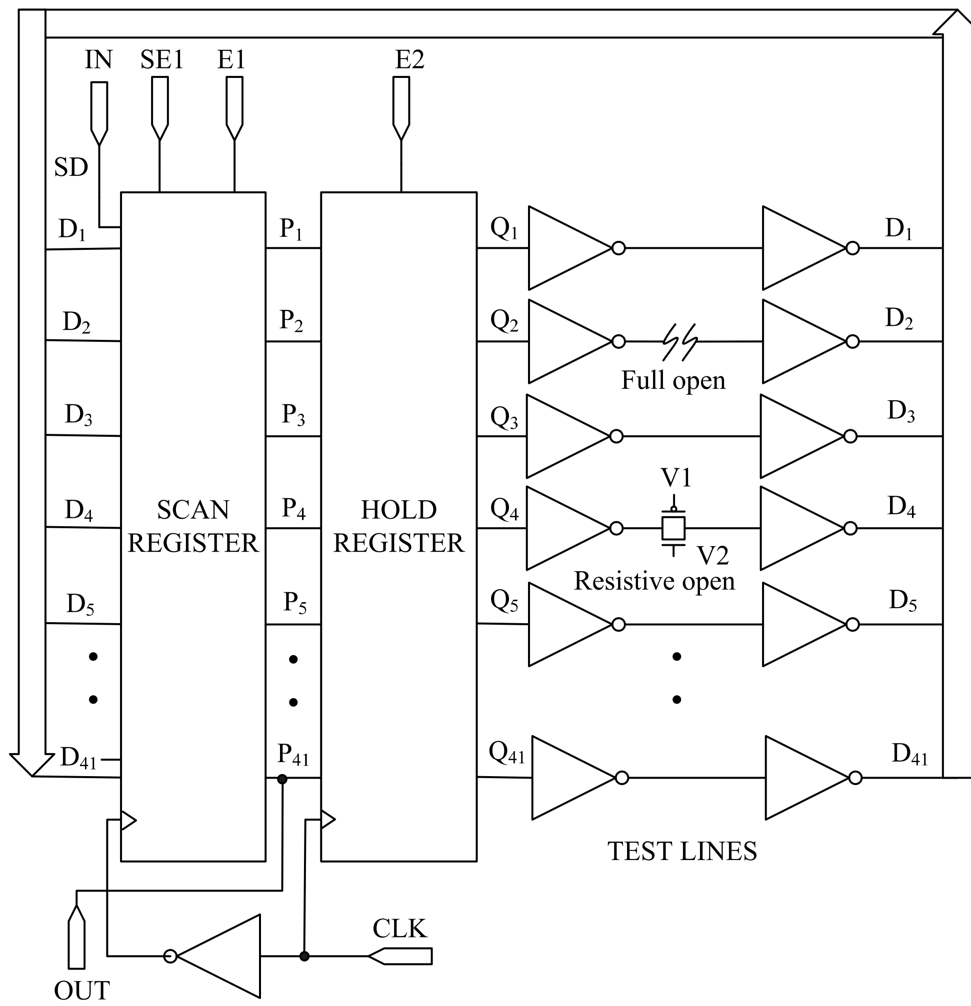

Figure 4.2. Circuit diagram

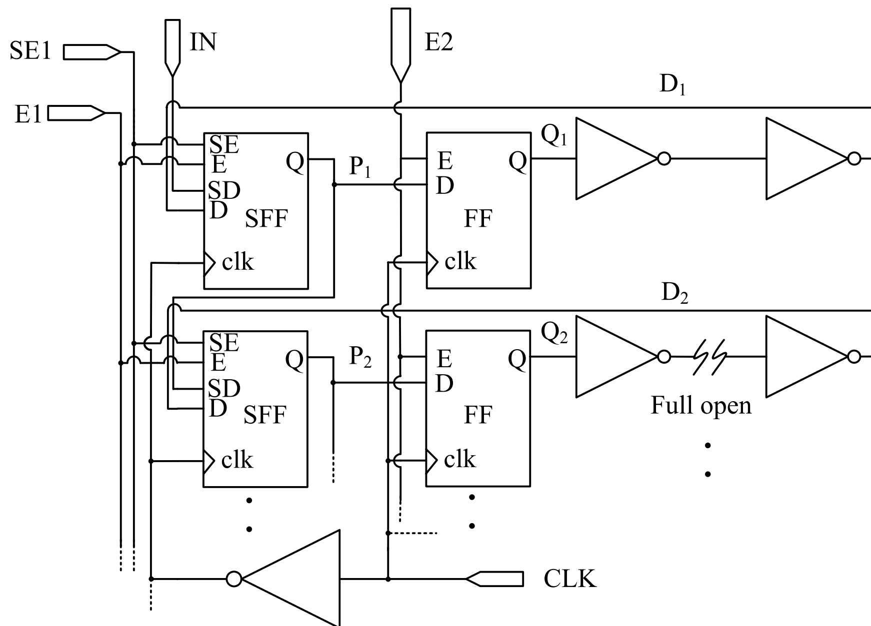

Figure 4.3. Circuit detail for the two first test lines

- *IN*: Digital input. This input controls the scanning in of the test vectors.
- *OUT*: Digital output. The test lines voltages captured by the scan register are scanned out by means of this pin.
- *SE1*: Digital input. This signal is the Enable of the shift register mode of the scan register (active high).
- *E1*: Digital input. Enables the normal operation mode of the scan register (active high).
- *E2*: Digital input. Enables the hold register (active high).
- *CLK*: Digital input. It is the system clock.
- *V1* and *V2*: Analog inputs to control the voltage at the transistor gate terminals of the transmission gates.

The clock signal is complemented in the scan register, as shown at the bottom of Figure 4.2 and 4.3. In this way, the hold register is active with the rising edge and the scan register is active with the falling edge of the clock (Figure 4.4 and 4.5). Once the test vector has been scanned in (activated at the falling edge of the clock), the hold register launches the test vector at the input of the inverters feeding the test lines. The signals are propagated along the test lines, and at the falling edge of the same clock period, the scan register captures the values of the test lines. Complementing the clock signal at the input of the scan register allows the test vectors to be launched and the results to be captured in the same clock period. Furthermore, due to this configuration and modifying the duty cycle of the clock, it is possible to control the delay between the launch and the capture phase of the test, as observed in Figure 4.4a and 4.4b. The case where the duty cycle of the clock signal is 50% is illustrated in Figure 4.4.a. However, Figure 4.4.b considers the case where the duty cycle is lower than 50%. Therefore, the delay between the launch and the capture phase is smaller in the latter case. With this strategy, experiments with different delay between the launch and the capture can be performed. It is especially advantageous for dynamic tests since the circuit delay may be measured by proper selection of the clock signal period and the duty cycle. It is only necessary to modify the delay between the rising and the falling edge of the clock signal.

4.1.1.1 Circuit Operation

An illustrative example of the circuit operation is presented next (see Figure 4.5). For ease of understanding, some internal signals have also been considered. The example consists of setting every test line to logic 1 (a series of forty-one logic 1s) as the input sequence fed to the interconnecting structure in the first pattern and setting every test line to logic 0 (a series of forty-one logic 0s) in the second pattern. The procedure is divided into different steps, as listed below:

1. Scan-in pattern1: At the first forty-one falling edges of the clock and with the scan register programmed in shift mode (*SE1* in high state), the test vector is scanned in at the inputs of the hold register (a sequence of logic 1s).
2. Launch pattern1: At the rising edge of the next clock period, the hold register launches the first pattern on the test lines (*E2* in high state).
3. Propagation pattern1: The first pattern is propagated along the test lines. This is observed in the timing diagram due to the delay between the rising transitions of signals Q_3 and D_3. It is the delay added by the inverters (see Figure 4.2).
4. Capture pattern1: At the falling edge of the same clock period, the values of the test lines are captured by the scan register in normal mode (*E1* in high state).
5. Scan-in pattern2/Scan-out pattern1: At the next forty-one falling edges of the clock signal and with the scan register in shift mode, the circuit response for the first pattern is scanned out (*SE1* in high state). At the same time, the second patter (a sequence of 0s) is scanned in.
6. Launch pattern2: Once pattern2 is scanned in, at the rising edge of the next clock period, the hold register launches the second pattern on the test lines (*E2* in high state).
7. Propagation pattern2: The second pattern is propagated along the test lines in a similar way as in step 3.
8. Capture pattern2: At the falling edge of the same clock period, the values of the second pattern are captured by the scan register in normal mode (*E1* in high state).
9. Scan-out pattern2: The second pattern is scanned out at the next falling edges of the clock (with the scan register in shift mode).

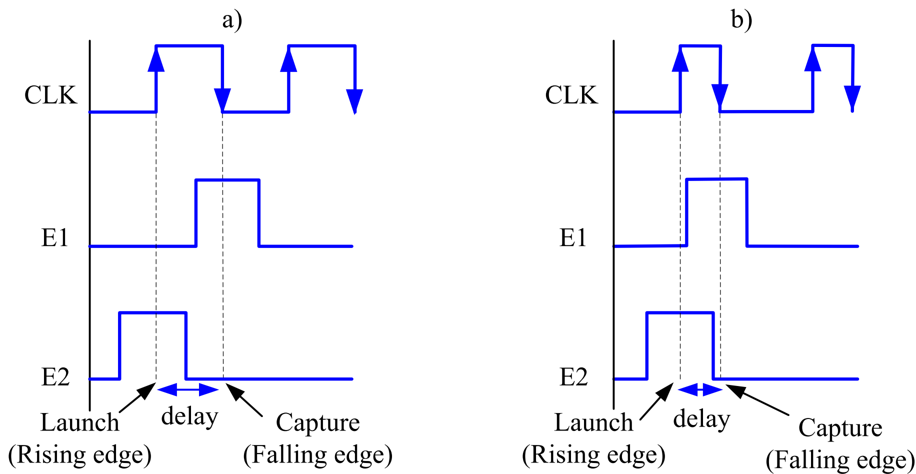

Figure 4.4. Delay control between launch and capture a) Duty cycle b) Reduced duty cycle.

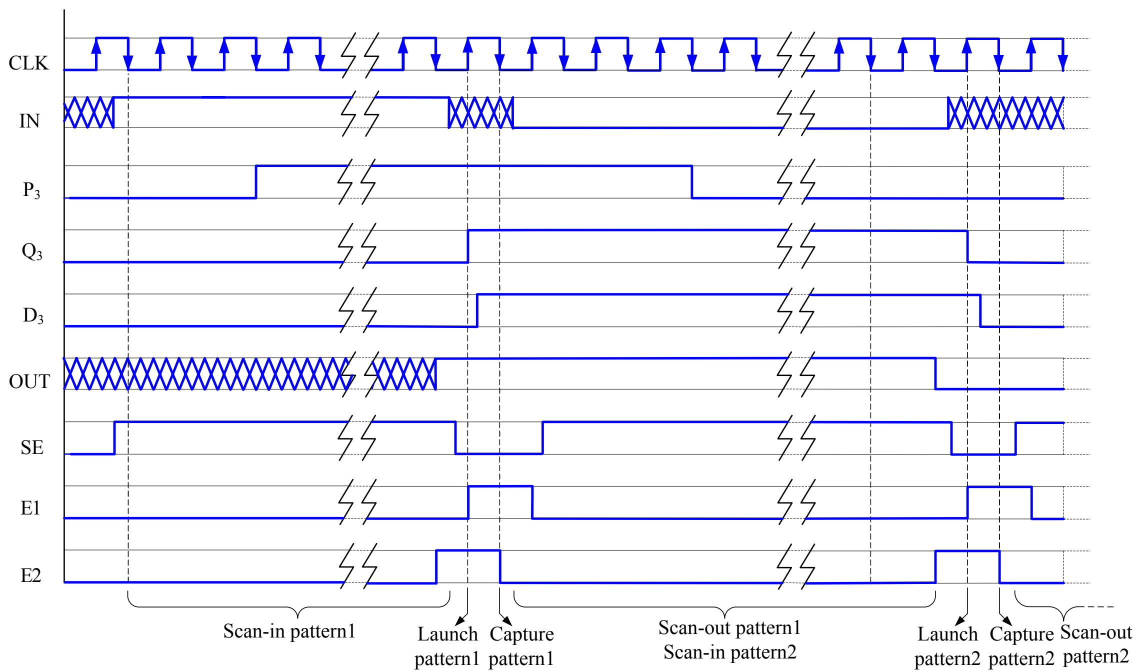

Figure 4.5. Timing diagram for the scanning in of a series of 1s in the first pattern and a series of 0s in the second pattern.

4.1.1.2 CIRCUIT TOPOLOGY

The test lines are routed as close as the technology allows to obtain significant coupling effects. The open defects intentionally added are placed at different locations along the test lines. The design considers both vertical (between different metal layers) and horizontal (in the same metal layer) coupling capacitances and full open and resistive open defects. The different coupling configurations are depicted in Figure 4.6. On the one hand, the horizontal coupling is considered in Metal1 and Metal4. In this way, the influence of coupling capacitances to substrate and well, maximized in case of Metal1 and minimized in Metal4 is taken into account. On the other hand, the influence

of vertical coupling is considered in Metal3, with the neighbours routed in Metal2 and Metal4. The metal widths and the spacing between metal tracks are described in Table 4.I.

Full open defects have been placed on the metal lines by means of intentional breaks. However, resistive open defects have been emulated with the help of transmission gates, see Figure 4.7 for more detail. The change in voltage at the gate terminals of the transmission gates ($V_{g(nMOS)}$ and $V_{g(pMOS)}$) causes a variation of the effective resistance of the defective line. These transistor gates voltages are independent and externally controllable by the analog inputs *V1* and *V2* of the design, as already illustrated in Figure 4.2.

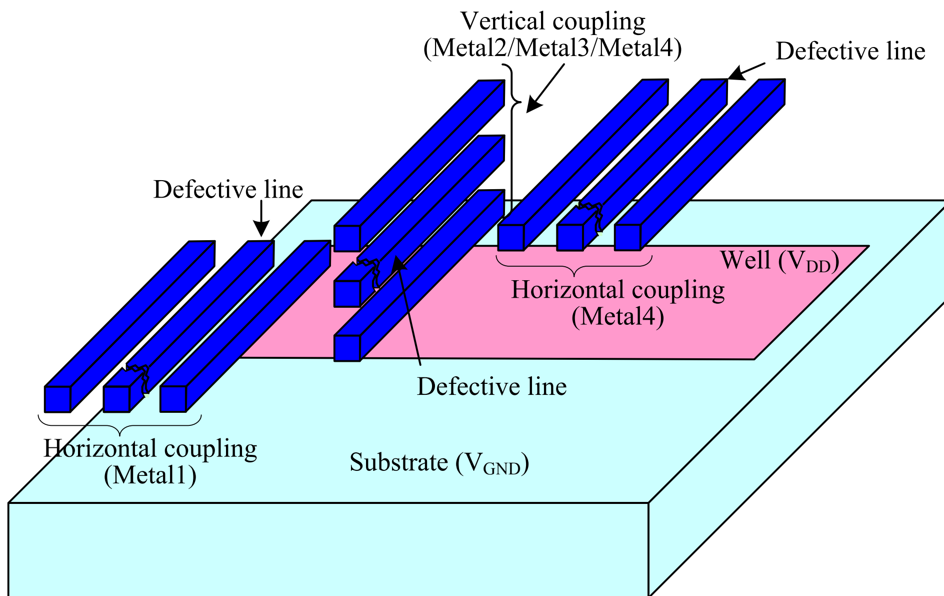

Figure 4.6. Coupling configurations considered in the design.

TABLE 4.I
METAL TRACKS: LAYOUT INFORMATION

Metal layer	Metal width (µm)	Metal spacing (µm)
Metal1	0.50	0.45
Metal2	0.60	0.50
Metal3	0.60	0.50
Metal4	0.60	0.60

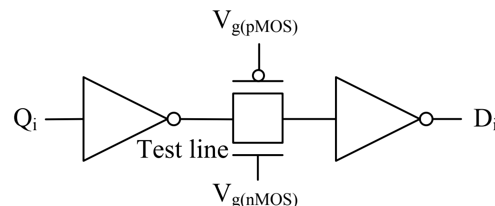

Figure 4.7. Transmission gate as a resistive open.

Experiments have been carried out with the fabricated design [169]-[170]. These experiments have been intentionally applied in order to achieve the goals of the above

design. For this purpose, an Automatic Test Equipment (ATE) HP82000 tester with a proper set-up specially created for this design has been used. All the experiments have been performed under the same ambient conditions. Temperature and V_{DD} have been controlled to be 25º C and 3.3 V, respectively.

4.1.2 STATIC COUPLING EFFECT

This section summarizes the impact of the neighbouring coupling capacitances on the static behaviour of open defects. It is already known that the voltage of floating wires due to full open defects depends on the parasitic coupling capacitances between the floating wire and its respective neighbours [48]-[52], [55], [57], [78], [136], [171]-[172]. In this section, this influence is experimentally quantified, and from these results, some conclusions are drawn to improve the detectability of such defects.

4.1.2.1 EXPERIMENTAL RESULTS

Ten full open defects have been intentionally added in our experimental design, thus generating ten floating nodes (*FN*). The layout information about these floating nodes and their respective pair of coupled neighbours (N_1 and N_2) is shown in Table 4.II. L_{CN1} and L_{CN2} refer to the coupling length between the floating node and neighbours N_1 and N_2, respectively.

TABLE 4.II
FULL OPENS: LAYOUT INFORMATION

Floating node (FN)	Metal layer			Length (µm)	
	FN	N_1	N_2	L_{CN1}	L_{CN2}
FN1	Metal3	Metal4	Metal2	75	105
FN2	Metal3	Metal4	Metal2	460	490
FN3	Metal3	Metal4	Metal2	2660	2690
FN4	Metal4	Metal4	Metal4	30	0
FN5	Metal4	Metal4	Metal4	3250	3200
FN6	Metal4	Metal4	Metal4	2890	2880
FN7	Metal4	Metal4	Metal4	5990	5990
FN8	Metal1	Metal1	Metal1	30	0
FN9	Metal1	Metal1	Metal1	2620	2610
FN10	Metal1	Metal1	Metal1	6030	6030

The experiment consists in capturing the state of the floating node voltages for every possible combination of their corresponding coupled neighbours. This experiment

has been performed on fifteen different devices to evaluate the process variation effects. The experimental results (measured with the ATE) are summarized in Table 4.III, where sub-indices *i* and *j* (appearing in H_i and L_j) refer to the number of devices which obtained a high logic (*H*) and a low logic (*L*) value, respectively. For instance, for the floating node *FN1*, when both neighbours are set to logic 1, H_{15} is reported (see Table 4.III), which means that the whole set of fifteen devices captured a high logic value. However, in the case of *FN2*, when its neighbours are set to (N_1 N_2) = (0 1), three devices captured a high logic value (H_3) on the floating node and twelve captured a low logic value (L_{12}), being reported in Table III as H_3L_{12}.

It is observed that when both neighbours have the same logic value (N_1 N_2) = (1 1) or (0 0), the floating node is pulled up or pulled down with the help of their coupling capacitances. However, when the neighbours have different logic values, the floating nodes voltages fall near the high and low input logic voltages (V_{IHmin} and V_{ILmax}) of the inverter, and consequently they have an unpredictable value. For this reason, different results are obtained for each device. For some of the devices, a high logic state is captured while for the rest of the devices a low logic value is generated. These results are repetitive since for every device the same test has been applied different times and on different days and the results have always been the same. Therefore, environmental noise is not the reason for this behaviour.

TABLE 4.III
FULL OPENS: EXPERIMENTAL RESULTS

Floating node (FN)	**Neighbours values (N1 N2)**			
	11	**00**	**01**	**10**
FN1	H_{15}	L_{15}	L_{15}	L_{15}
FN2	H_{15}	L_{15}	H_3L_{12}	H_3L_{12}
FN3	H_{15}	L_{15}	H_9L_6	H_9L_6
FN4	H_{15}	L_{15}	L_{15}	H_{15}
FN5	H_{15}	L_{15}	H_1L_{14}	H_1L_{14}
FN6	H_{15}	L_{15}	$H_{13}L_2$	$H_{13}L_2$
FN7	H_{15}	L_{15}	$H_{14}L_1$	$H_{14}L_1$
FN8	H_{15}	L_{15}	L_{15}	H_{15}
FN9	H_{15}	L_{15}	$H_{12}L_3$	$H_{12}L_3$
FN10	H_{15}	L_{15}	H_8L_7	H_8L_7

Furthermore, there are no differences between results when (N_1 N_2) = (0 1) or (1 0), since the coupling capacitances between N_1 and N_2 related to the floating node are nearly the same, as shown in Table 4.II. However, the results for *FN4* and *FN8* are different from those of the other floating nodes because one of the neighbours does not influence the floating node. Their logic value depends on the first neighbour only. Notice that for the two cases only a coupling length of 30 µm is sufficient to control the logic state of the floating line.

Logic testing modifying both the power supply and temperature has also been applied to the devices. In fact, tests carried out at low power supply voltage and at high (80ºC) and low (5ºC) temperatures reported the same results as at nominal conditions (Table 4.III).

Quiescent current measurements have also been made and found to show coherent behaviour with the previous results based on the voltage response. Indeed, I_{DDQ} measures have been performed and an increase up to 20% of the device normal I_{DDQ} value has been found in the case of the neighbours set to different logic values (0 1) or (1 0).

4.1.2.2 EXPERIMENTAL RESULTS DISCUSSION

In a defective node, the parasitic capacitances influencing the behaviour of the floating node are illustrated in Figure 4.8a. The parasitic coupling capacitance between each line and ground ($C_{SUBSTRATE}$) and power (C_{WELL}) planes, and coupling capacitances to other lines (C_{Ni}) are considered [78], [172]. Another set of capacitances influencing the open interconnect line is made up of the transistor capacitances connected to the floating wire (as an example, an inverter has been considered in Figure 4.8a). These capacitances are driven by the open line and consist of gate_drain (C_{gd}), gate_source (C_{gs}) and gate_bulk (C_{gb}). The values of these transistor parasitic capacitances vary with the conduction state of the transistors. Another influencing factor in the final electrical behaviour of the open line is the trapped charge in the floating structure. Previous works [55], [60]-[61], [78] evaluate this influence. For full opens, the ratio between the parasitic coupling capacitances presented so far, together with the capacitances of the next driven gates and the initial trapped charge determines the static voltage value of the floating node.

In order to analyze the effect of the above factors, a detailed study of one of the cases designed in our fabricated chip (Figure 4.8b) is now presented. Let us assume that the full open defect may be located at any place along the (defective) line *L2*, which belongs to Metal4 (cases *FN4-FN7* in Table 4.II). There are two neighbours which are coupled to the floating node. Since the coupling lengths are very similar for both neighbours, their coupling capacitances are approximately the same, i.e. $C_{N1} = C_{N3}$. This equivalence does not hold for the parasitic capacitances between the defective line and substrate and well (C_{GND} and C_{VDD}), since they depend on the layout, and by design $C_{N1} = C_{N3} > C_{GND} > C_{VDD}$. The neighbouring parasitic capacitances are larger than the capacitances to substrate and well, since the floating node belongs to Metal4 and it is far from substrate and well.

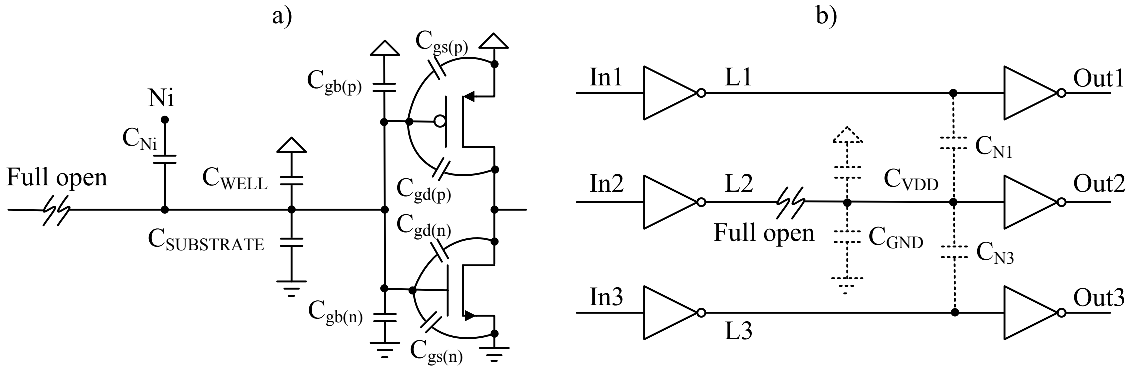

Figure 4.8. Full open defect a) Parasitic coupling capacitances b) In a bus interconnect line.

For every logical combination of the neighbours (*L1*, *L3*), the defective behaviour caused by a full open defect has been analyzed (Figure 4.8b). The impact of the defect location (L_{Fline}) is also taken into account. The V_{ILmax} and V_{IHmin} values of the load inverter must be considered related to the floating line voltage (V_{Fline}), since this relationship determines the logic interpretation of V_{Fline}. This dependency is illustrated in Figure 4.9 [173]. For the case in Figure 4.9a, if the neighbours are set to different logic values, the voltage level at the output of the load inverter is unpredictable. When the floating line is influenced by the neighbouring lines (*L1* and *L3*), the behaviour is different for the pull-up case (*L1 L3*) = (1 1) and the pull-down case (*L1 L3*) = (0 0). Different critical lengths ($L_{C(H)}$ and $L_{C(L)}$) separate the region where the open behaves in an unpredictable way from the region where the open follows the influencing lines. Notice that for small lengths lower than $L_{C(H)}$, the detectability of the open cannot be assured. However, if the situation is like the one in Figure 4.9b, when the neighbours

have different logic values or (*L1 L3*) = (0 0), the logic behaviour of the floating line can be modelled as a SA0. However, for the pull-up case (*L1 L3*) = (1 1), the logic interpretation of the floating line cannot be assured for coupling lengths higher than $L_{C(L)}$. The complementary case is depicted in Figure 4.9c. The behaviour of the floating line can be modelled as a SA1 for the pull-up case and when the neighbours have opposite logic values. Nevertheless, for the pull-down case, the logic interpretation can not be assured for coupling lengths higher than $L_{C(H)}$.

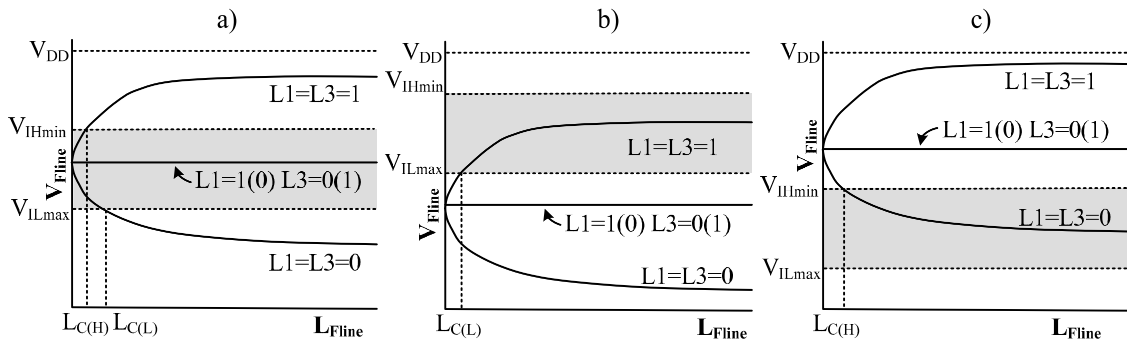

Figure 4.9. Logic interpretation of the floating line voltage.

The simulation results assuming that the lines are routed in Metal4 are illustrated in Figure 4.10. These results corresponds to the same case as the one shown in Figure 4.9a. The trapped charge has been assumed negligible. For long wires, the parasitic coupling capacitances are so important that they can determine the logic value of the floating node. When both neighbouring lines are set to 1 (0), they pull the floating line to a high (low) voltage value. However, if the neighbours are set to different logic values, the floating lines remains in an unpredictable (intermediate) value between the logic thresholds (V_{ILmax} and V_{IHmin}) of the inverter. As the coupling length decreases, the parasitic capacitances decrease too, reducing the coupling effect. Therefore, although both neighbours are set to 1 (0), the parasitic capacitances of the transistors become relatively more important and the voltage value of the floating line decreases (increases), approaching V_{IHmin} (V_{ILmax}). At a particular point, the coupling capacitances can be so small that the influence of the neighbours becomes low enough to cause the transistor capacitances to condition the state of the floating line. In this particular case, the floating node voltage is set between V_{ILmax} and V_{IHmin}, quite close to V_{IHmin}.

When both neighbours are set to the same logic value, (*L1 L3*) = (1 1) or (0 0), there is a corresponding critical length ($L_{C(H)}$ $L_{C(L)}$) which separates the region where the open behaves in an unpredictable way from the region where the floating net follows the

influencing neighbouring lines. In Figure 4.10, for $L_{Fline} > L_{C(L)}$, the open defect can be detected with both the pull-up and the pull-down cases. However, when $L_{C(L)} > L_{Fline} > L_{C(H)}$, the defect can only be detected by means of the pull-up case. Furthermore, for short lengths ($L_{Fline} < L_{C(H)}$) the detectability of the defect cannot be guaranteed. For different logic values on the neighbours, the inverter output is unpredictable, since the floating node voltage lies between V_{ILmax} and V_{IHmin}, independently of the coupling length.

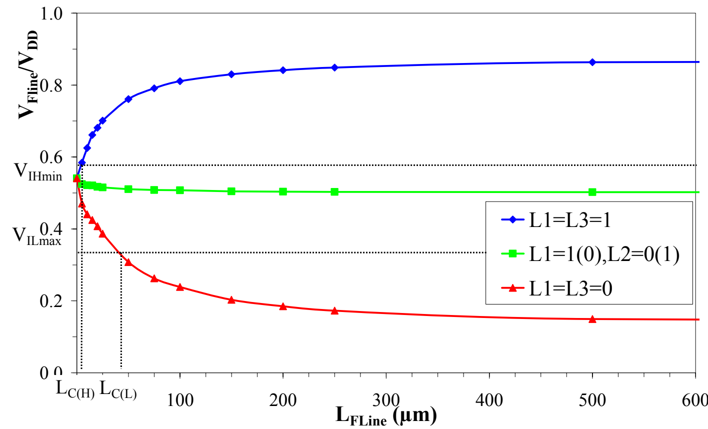

Figure 4.10. V_{Fline} for different interconnect lengths (Metal4).

The experimental results, summarized in Table 4.III, show that the designed full opens belong to the influencing region ($L_{Fline} > L_{C(L)}$), since if both neighbours are set to 1 (0), the floating node is pulled-up (pulled-down). Experimental results are consistent, but not equal to the simulation behaviour. The influencing neighbours with the same logic value pull the floating line consistently. Opposite values in the influencing lines give unpredictable logic values at the receiving logic gate. When the neighbours have different logic states, the floating node voltage lies between V_{ILmax} and V_{IHmin}. That is the reason why for the same designed floating node (*FN*), different repetitive results are obtained depending on the manufactured device (*FN2-3*, *FN5-7* and *FN9-10*). In case of fan-out, this intermediate voltage may be interpreted differently by the receivers (Byzantine problem).

In this experiment the unpredictability for defects located near the end of the line $L_{Fline} < L_{C(H)}$ has not been observed. In Table III it is shown how the floating node controlled with a coupling length of 30 µm, which is lower than the critical length reported by simulation, is still fully influenced by its neighbours. This behaviour can be explained by three considerations. First, parametric variations in the physical

dimensions of the design (metal widths, metal heights and metal spacing) causing variations in the parasitic capacitances between nets. Second, variations in the transistors threshold voltages of the driven inverters. Finally, the trapped charge on the floating node, which has been assumed zero during simulation. The trapped charge would shift simulation results as the ones in Figure 4.10, modifying the critical lengths.

Modifying the nominal conditions of the test has also been considered during the simulation stage. Figure 4.11 illustrates the simulation results of the V_{Fline} at low power supply voltage (V_{DD} = 1.3 V). Notice how the results are quite similar to the ones at nominal conditions. In fact, $L_{C(L)}$ decreases at low V_{DD}, which improves the detectability of the open, especially in the pull-down case. In Figure 4.12a, the relationship between $L_{C(L)}$ and V_{DD} is illustrated. Observe how the lower the V_{DD}, the lower $L_{C(L)}$. This fact is caused by the fact that the unpredictable region (voltages between the logic thresholds of the inverter) decreases for low V_{DD} values, as reported in Figure 4.12b. However, due to the configuration of the opens injected in the design, no real improvement is observed on the experiment carried out on the tester at low voltages because the open is already detected at nominal conditions.

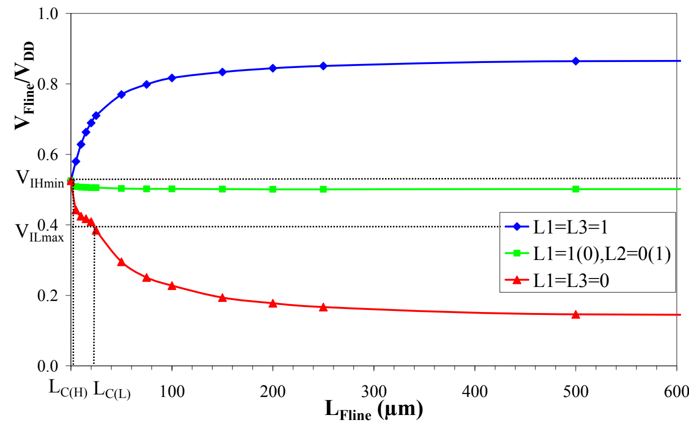

Figure 4.11. V_{Fline} for different interconnect lengths (Metal4) with V_{DD}= 1.3 V.

The other parameter which was modified during the simulations was temperature. Figure 4.13a shows the inverter transfer characteristic for the technology used at different temperatures. Most of the characteristic moves to the right as temperature increases. However, for low input voltages the transfer function moves slightly to the left. From the transfer characteristic of Figure 4.13a, the behaviour of V_{ILmax} and V_{IHmin} can be derived, as illustrated in Figure 4.13b. Both V_{ILmax} and V_{IHmin} increase with temperature. The unpredictable region widens on the V_{IHmin} side and makes narrower on the V_{ILmax} side if temperature increases. These two effects compensate partially each

other. Therefore, the temperature effect is expected not to be important and not to improve noticeably the full open detectability. Table 4.IV summarizes the $L_{C(L)}$ results for the two ends of the temperature range. The effect is not as important as the V_{DD} effect seen previously. For that reason, the experimental results obtained on the tester were not modified when applying the test at different temperatures.

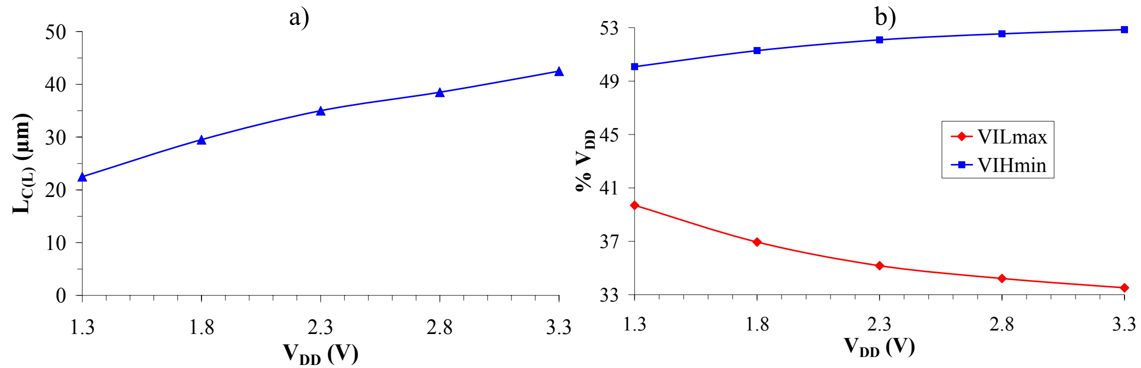

Figure 4.12. Simulation results a) $L_{C(L)}$ vs. V_{DD} b) Logic thresholds of the inverter vs. V_{DD}.

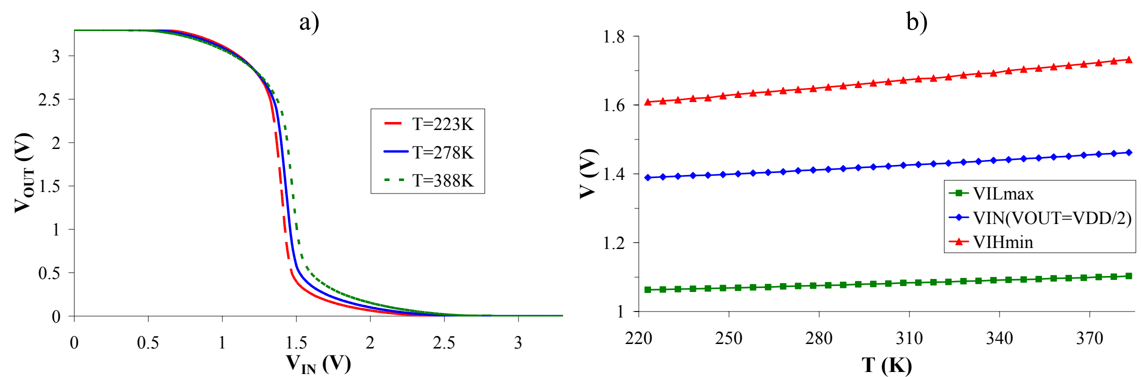

Figure 4.13. Simulation results at different temperatures a) V_{IN} vs. V_{OUT} b) Logic thresholds.

TABLE 4.IV
CRITICAL LENGTH ($L_{C(L)}$)VS TEMPERATURE

Temperature (K)	$L_{C(L)}$ (µm)
223	45
383	41

Finally, the current behaviour in the presence of a full open is analyzed. For that purpose, let us consider the case of the floating node voltage lying between the logic thresholds (V_{ILmax} and V_{IHmin}) of the inverter, being its logic behaviour unpredictable. In this case, abnormal current flows through the transistors driven by the floating node and the highest value is reached approximately when the input is close to $V_{DD}/2$, depending on the relationship between the physical parameters of the nMOS and pMOS transistors.

An evaluation of its impact is obtained from the I_{DDQ}-V_{Fline} simulation relationship for the inverter used in the experimental design (see Figure 4.14). Notice that an extra current up to 112 μA might be added to the circuit consumption due to the open. This current increase is consistent with the extra current up to 100 μA measured in our experiments for intermediate voltages in the floating nodes when the neighbours are set to different logic values. Therefore, when full open defects are difficult to detect by means of a voltage-based test strategies, detectability may be enhanced by inspection of the current behaviour.

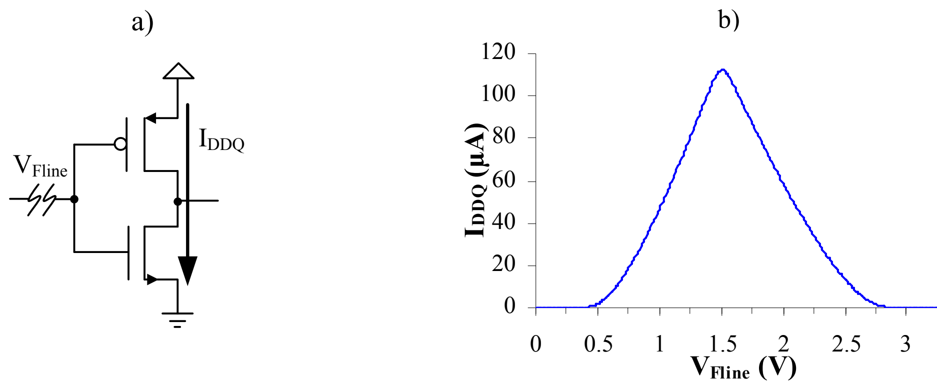

Figure 4.14. Floating line driving an inverter a) Transistor level b) I_{DDQ} vs. V_{Fline}.

4.1.2.3 TEST RECOMMENDATIONS FOR FULL OPENS

The experiments carried out with full open defects show the influence of the location of the defect and the parasitic coupling capacitances on their electrical behaviour. Distance between layers is expected to decrease in the future in the same way as metal widths. Therefore, parasitic capacitances between structures from different layers are expected to remain reasonably constant. On the contrary, distance between nets is expected to shrink and metal thickness is expected to increase. Both effects increase the parasitic capacitances between nets of the same metal layer. Thus, the impact of neighbouring lines of the same layer will become more relevant in future technologies [174]. This fact is observed in the behaviour of a floating node due to a full open defect. The voltage of the floating node (assuming a load inverter) is determined by the capacitive divider already presented in (2.2). From this expression, it can be defined the pull-up ratio $\eta(N_1, N_2, \ldots, N_l)$ as the capacitive divider shown in (4.1):

$$\eta(N_1, N_2, ..., N_l) = \frac{\sum_{i=1}^{i=l} C_{Ni} \cdot I(N_i) + C_{WELL} + C_{gb(p)} + C_{gs(n)} + C_{gd}(V_{FLine})}{\sum_{i=1}^{i=l} C_{Ni} + C_{SUBSTRATE} + C_{WELL} + C_{gb} + C_{gs} + C_{gd} + C_{gd}(V_{FLine})} \quad (4.1)$$

The pull-up ratio is a non-dimensional parameter and is ideally ranged between 0 and 1. If $\eta(N_1, N_2, ..., N_l) = 0$, V_{FLine} is set to 0 and if $\eta(N_1, N_2, ..., N_l) = 1$, V_{FLine} is set to V_{DD} (without considering the possible effect of the trapped charge).

When logic testing for full opens, the ideal case is setting V_{FLine} either to a high logic or to a low logic value (the pull-up ratio close to 0 or 1), far from the Byzantine unpredictable zone of intermediate voltages. However, among all the factors affecting $\eta(N_1, N_2, ..., N_l)$: the power rails capacitances, the neighbour capacitances and the transistor capacitances, only the neighbours' state can be modified, since it is pattern dependent. Therefore, minimizing or maximizing $\eta(N_1, N_2, ..., N_l)$ means obtaining the lowest or the highest coupling capacitances related to the neighbours set to a high logic value. In order to improve the detectability and diagnosability of interconnect full open defects, when applying a logic test, the strategy proposed consists of:

1. Testing for a SA1 at the target node: Maximize the pull-up ratio $\eta(N_1, N_2, ..., N_l)$.
2. Testing for a SA0 at the target node: Minimize the pull-up ratio $\eta(N_1, N_2, ..., N_l)$.

As already commented, the maximization and minimization of $\eta(N_1, N_2, ..., N_l)$ depends on the logic state of the neighbouring lines. However, the defect location modifies also the neighbourhood affecting the floating node. Therefore, for every different open location, the maximization and minimization of $\eta(N_1, N_2, ..., N_l)$ may be different. For every location, there is a different optimal neighbourhood state which minimizes or maximizes $\eta(N_1, N_2, ..., N_l)$. Without loss of generality, let us consider the example illustrated in Figure 4.15a, where a defective net with five coupled neighbours with a full open placed at three different locations is considered. The number of neighbours influencing the floating node depends on the location of the defect. Thus, if the open is located at *OPEN1*, all the neighbours have effective coupling to the floating node (Figure 4.15b). However, if the *OPEN2* location is considered, N_1 and N_2 do not influence the floating node, as shown in Figure 4.15c. Finally, if the open is considered at *OPEN3*, only (partially) N_4 and N_5 are coupled to the floating node, as illustrated in Figure 4.15d. Assuming, for instance, a logical incompatibility between neighbours N_1 and N_5, the optimal state of the neighbours to detect the full open defect is not the same

for all the locations, as described in Table 4.V. When the open is located at *OPEN1*, the optimal case lies in setting all the neighbours to the opposite logic (defect-free) value expected in the floating node except at N_5 (due to the incompatibility with N_1). However, for the *OPEN2* and *OPEN3* locations, N_1 does not influence the floating node. The incompatibility between N_1 and N_5 does not affect the detectability of the defect and all the influencing neighbours can be set to the same logic value, as listed in Table 4.V.

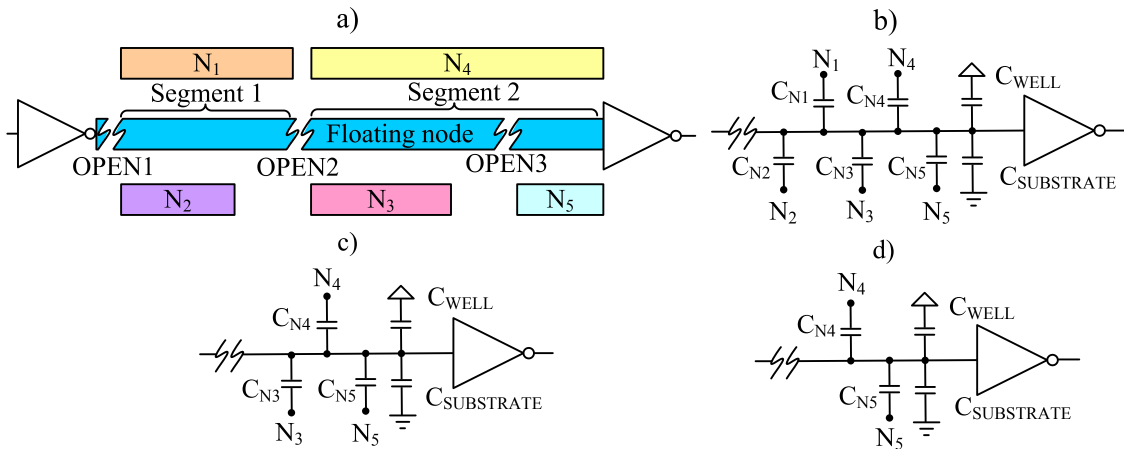

Figure 4.15.Full open a) Layout b) Coupling capacitances for the open location OPEN1 c) OPEN2 d) OPEN3.

TABLE 4.V
LOGIC BASED TEST FOR THE EXAMPLE IN FIGURE 4.15

Floating node (FN)	Defect location					
	OPEN1		OPEN2		OPEN3	
Neighbours	FN = 0	FN = 1	FN = 0	FN = 1	FN = 0	FN = 1
N_1	1	0	X	X	X	X
N_2	1	0	X	X	X	X
N_3	1	0	1	0	X	X
N_4	1	0	1	0	1	0
N_5	0	1	1	0	1	0

An interconnect line is divided into different segments, each of them having a different optimal set of neighbourhood states in order to assure the optimization of the $\eta(N_1, N_2,\ldots, N_l)$. Based on the layout information considered in Table 4.V, the floating line of Figure 4.15a is divided into two segments. In the first segment (*Segment 1*), the optimal state consists in setting all the neighbours except N_5 to the same logic value. On the other hand, for the second segment (*Segment 2*), N_3, N_4 and N_5 should be set to the

same logic value, without taking N_1 and N_2 into consideration. Notice that a third segment could be included going from location *OPEN3* up to the end of the line. However, the optimal combination of states for this segment is included on that of Segment 2. The number of segments to be considered depends on the layout and on the number of constraints due to logic incompatibilities between nets.

The segment division suggested above for logic testing must also be applied to I_{DDQ} testing in order to increase the detectability of full open defects. Following with the example considered in Figure 4.15, Table 4.VI summarizes the optimal neighbours' state in order to obtain the appropriate $\eta(N_1, N_2, \ldots, N_l)$ value, which cause a current increase. Notice that other combination of logic values would obtain similar results.

TABLE 4.VI
I_{DDQ} BASED TEST FOR THE EXAMPLE IN FIGURE 4.15

Neighbours	**Defect location**		
	OPEN1	**OPEN2**	**OPEN3**
N_1	0	X	X
N_2	0	X	X
N_3	1	0	X
N_4	1	0	0
N_5	1	1	1

4.1.3 DYNAMIC COUPLING EFFECT

This section summarizes the impact of neighbouring coupling capacitances on the dynamic behaviour of open defects. The electrical scenario assumed for the dynamic characterization of open defects is similar to the one considered for crosstalk impact analysis, the latter is a particular case of the former (null resistance of the defect).

Similar to full open defects, ten resistive opens have been intentionally added in our design. As previously reported, the resistive opens have been implemented by transmission gates with controllable transistor gate voltages. The effective resistance of the defective line can thus be modified. The layout information about the resistive nodes (*RN*) and their respective coupled neighbours is summarized in Table 4.VII. L_{CN1} and L_{CN2} refer to the coupling length between the floating line and neighbours N_1 and N_2, respectively.

4.1.3.1 EXPERIMENTAL RESULTS

This sub-section summarizes the experimental results obtained for resistive opens. With the aim of understanding, the results are discussion into two parts, namely: 1) setting the neighbouring lines to constant logic values, and 2) changing the state of the neighbours.

TABLE 4.VII
RESISTIVE OPENS: LAYOUT INFORMATION

Resistive node	Metal Layer			Length (μm)	
	RN	N_1	N_2	L_{CN1}	L_{CN2}
RN1	Metal3	Metal4	Metal2	0	0
RN2	Metal3	Metal4	Metal2	650	650
RN3	Metal3	Metal4	Metal2	3080	3080
RN4	Metal4	Metal4	Metal4	0	0
RN5	Metal4	Metal4	Metal4	350	320
RN6	Metal4	Metal4	Metal4	3000	2990
RN7	Metal4	Metal4	Metal4	5940	5940
RN8	Metal1	Metal1	Metal1	0	0
RN9	Metal1	Metal1	Metal1	3190	3180
RN10	Metal1	Metal1	Metal1	5860	5860

1) Quiescent Neighbouring Lines

In this experiment, the neighbours do not change their state and remain at a high logic value. However, a rising transition is applied to the defective line through the output of its feeding inverter and the delay at the output is measured. The schema of the experiment is illustrated in Figure 4.16. The transistor gate voltages of the transmission gates resembling resistive opens are modified to obtain different resistance values.

The details of each resistive open have been previously presented in Table 4.VII. The delay measures for the resistive open defects belonging to Metal3, Metal4 and Metal1 are illustrated in Figure 4.17. The x-axis refers to the voltage values of the nMOS and pMOS transistor gates of the transmission gate. These values are related to the equivalent resistance of the transmission gate. In this way, as we move from right to left on the x-axis, the equivalent resistance of the transmission gate increases.

Two facts are observed from the results of this experiment: First, the impact of the open resistance on delay. As expected, the higher the resistance, the larger the delay. Second, the impact of the defect location, and therefore the influence of the neighbouring coupling capacitances. Notice that the range located at the rightest x-axis end (negligible resistance of the open defect) is similar to the one obtained for a crosstalk characterization of a non-defective interconnect line.

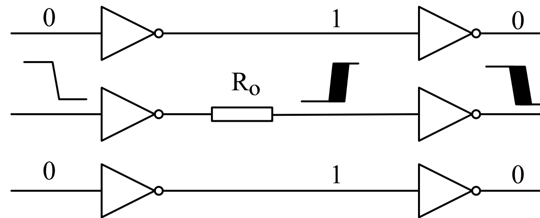

Figure 4.16. Quiescent neighbouring lines experiment.

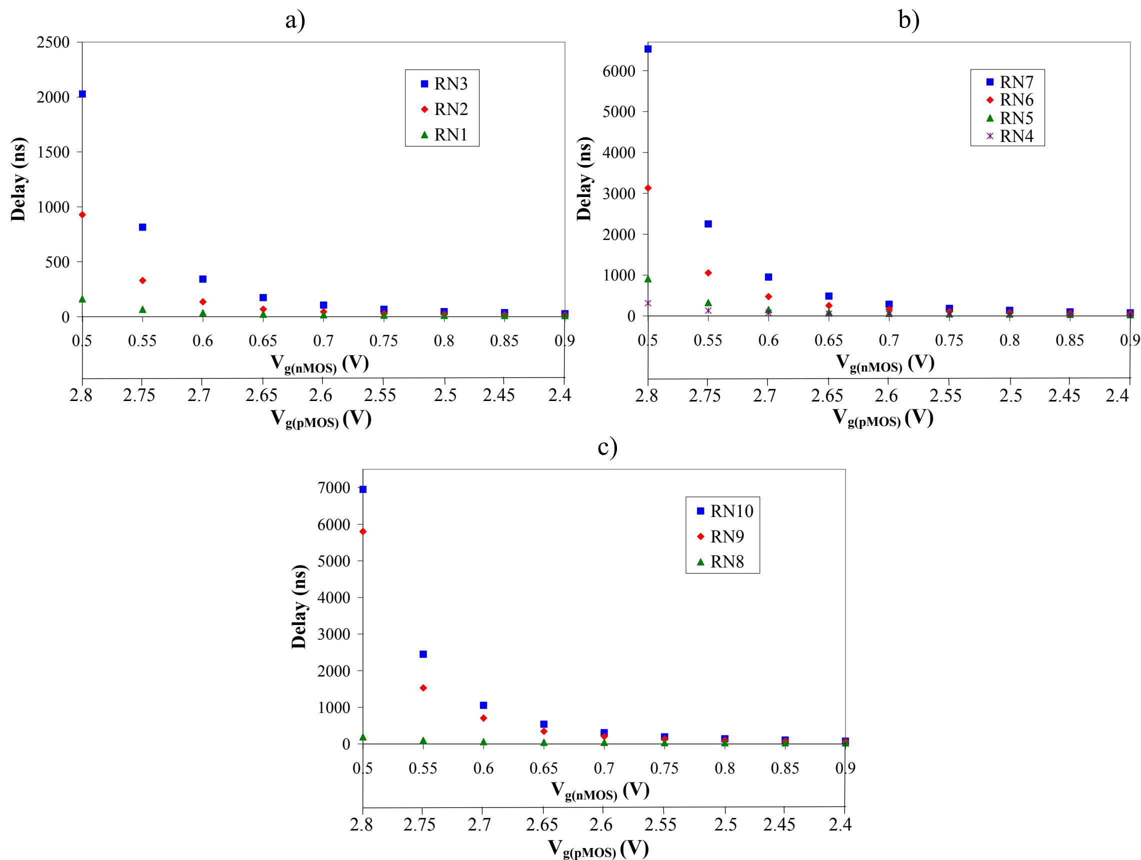

Figure 4.17.Delay results for resistive opens with different couplings a) Vertical b) Horizontal (Metal4) c) Horizontal (Metal1).

Every set of resistive opens in the same metal layer has the same features. The only difference is the open location. As a consequence, given a resistance value, the higher the coupling capacitances, the greater the delay. Based on the data shown in Table 4.VII, these cases are *RN3* for Metal3, *RN*7 for Metal4 and *RN10* for Metal1, as

also observed in Figure 4.17a, b and c, respectively. Finally, the measured delays are relatively greater for Metal1 than the ones corresponding to Metal4. This is due to the coupling capacitances to well and substrate, since Metal1 is closer than Metal4, and therefore these coupling capacitances are larger for Metal1. However, this behaviour is not followed by the set of Metal3 opens with vertical coupling. In these cases, the Metal2 neighbours are partially blocking the coupling capacitances to substrate and well. In practice, these vertical coupling capacitances may be less relevant since layouts usually alternate directions between layers.

2) Neighbouring Lines Changing Their State

The goal of this experiment is the evaluation of the dynamic impact caused by the capacitive coupled neighbours when changing their states. Figure 4.18 illustrates the three performed experiments. The gate voltages of the transmission gates are controlled to obtain different resistance values in a similar way as in the previous experiments. For a rising transition in the defective line, all possible combinations for the neighbours are considered (taking the symmetry of the layout into account).

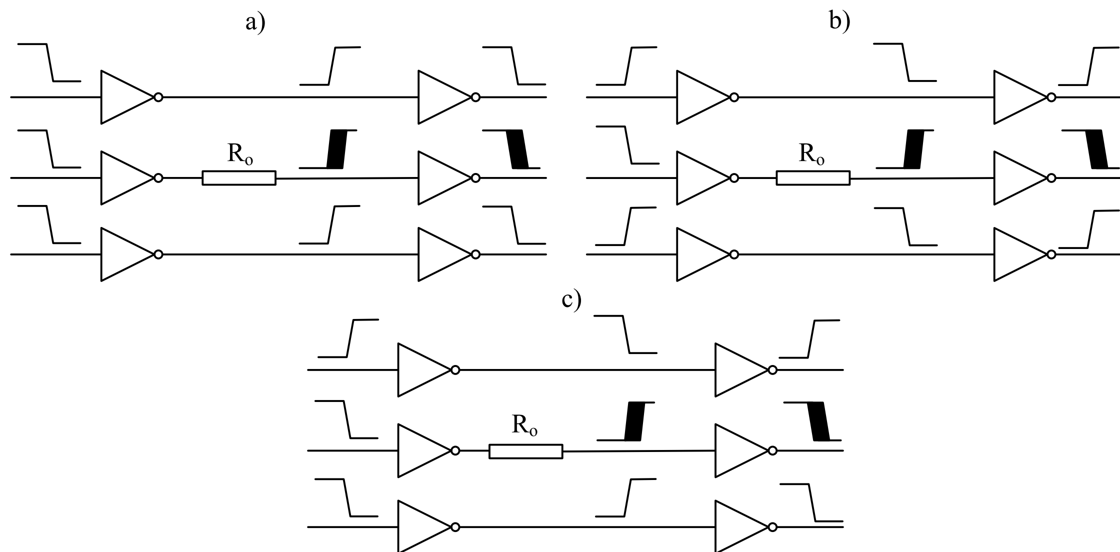

Figure 4.18. Experiment for the neighbouring lines changing their state a) The same transition as the defective line b) Different transitions a) One the same, the other different transition.

The measured delays for the present experiments are presented in Figure 4.19. Two different locations of the resistive open, *RN7* and *RN5*, are considered. In both cases, for any given defect resistance, the delay is greater if the neighbouring lines have the opposite transition to the defective one. However, if all the neighbours have the same transition as the target line, the variation of the delay on the resistance of the

defect is noticeably lower since they help the defective node to reach the final state. When the neighbouring lines have transitions of different sign, an intermediate behaviour is observed.

Figure 4.19a shows the results for a defective case where the total coupling capacitance is higher than the one in the case illustrated in Figure 4.19b. Comparing both sets of results, for the same resistance value, the time constant of the system is lower. Thus, the delay observed in Figure 4.19b is smaller than the corresponding delay in Figure 4.19a. For lower coupling capacitances, the value of the resistive open must be higher to cause the same delay.

The impact of transitions at neighbouring lines on the delay at the resistive node can be critical. Indeed, if all the transitions (in neighbours and in the defective node) have the same direction, the effect of the defect can be masked. On the contrary, benefit can be taken from the transitions at the neighbouring lines. If the opposite transition is generated between the neighbouring lines and the defective line, an increase in the delay is obtained.

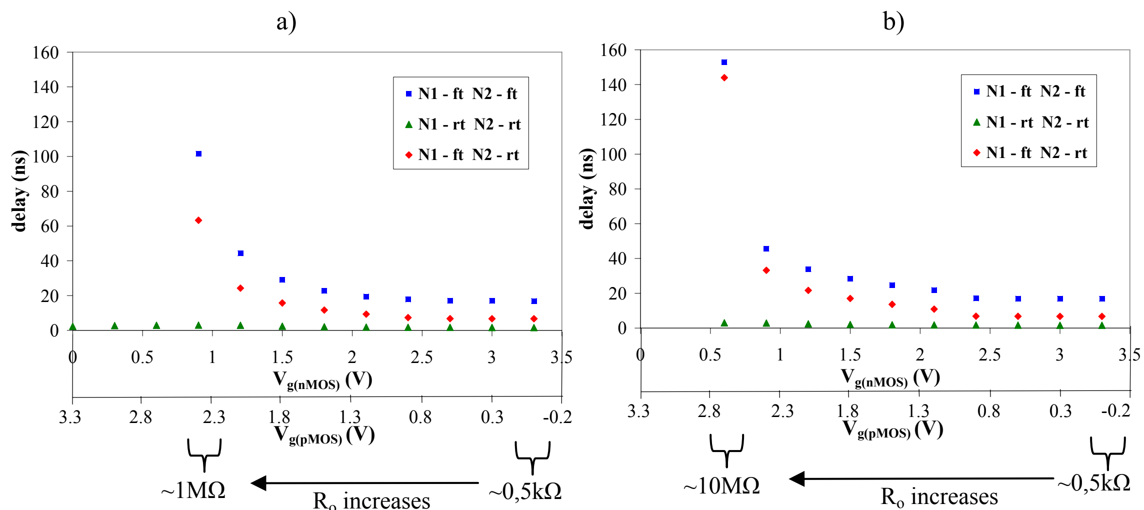

Figure 4.19. Experimental results for a) RN7 b) RN5 (N1: neighbour 1, N2: neighbour 2, rt: rising transition, ft: falling transition).

4.1.3.2 EXPERIMENTAL RESULTS DISCUSSION

Due to the presence of a weak open in an interconnect line, the signal takes longer to propagate through that line. The higher the defect resistance, the larger the delay. When a transition is generated on the defective line, the signal propagates through the next gate with an extra delay, as illustrated in the simulation results shown in Figure 4.20 for a defective line driving an inverter.

In this section, the experimental results obtained for resistive opens are analyzed. The discussion is divided similar to the sub-section where the experimental results were presented: 1) quiescent neighbouring lines and 2) neighbouring lines changing their state.

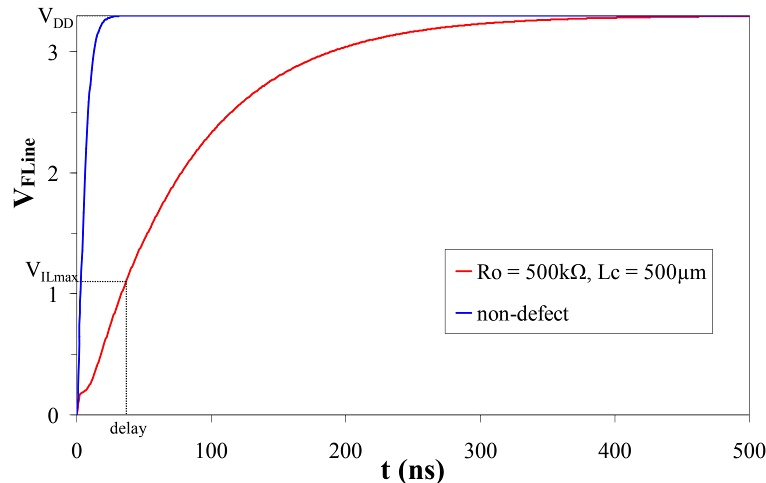

Figure 4.20. Simulation result for two lines driving an inverter (0.35 µm technology).

1) Quiescent neighbouring lines

The two neighbours do not change their logic values and a transition is applied to the defective line. Figure 4.21a illustrates a simplification of the experiment carried out with resistive opens. In this particular case, *L1* (*L3*) is permanently connected to the logic low (high) value. Transistors can be modelled as ideal switches provided that their on-resistance is significantly lower than typical open defect resistance. The equivalent electrical circuit of the three lines is simplified to a simple RC (dis)charging circuit, as shown in Figure 4.21b. The time required by the defective line to reach its final logic (low) value can be easily predicted in terms of $R = R_{L2} + R_o$ and $C = C_{VDD} + C_{GND} + C_{N1} + C_{N3}$. The timing behaviour corresponds to a quasi-exponential charging of the capacitance network. In Figure 4.22, the SPICE simulation of the extraction of the fabricated circuit is indicated with the label '*Quiescent neighbours*'.

2) Neighbouring lines changing their state

The experimental results show that transitions at neighbouring lines influence the timing behaviour of the defective node. Figure 4.23 illustrates the case where the two neighbouring lines are both driven by the opposite transition to the defective line. The time constant of *L1* and *L3* is orders of magnitude smaller than the time constant of the

defective line *L2*. This causes the defective node to be pulled up to an electrical voltage (*vo*) (see Figure 4.22). This initial voltage corresponds to the capacitive divider connected to the defective node (Figure 4.24.a). Starting from this initial voltage (*vo*), the evolution of *L2* follows a quasi-exponential discharging behaviour (Figure 4.24.b). Notice that the time constant is still the same derived from $R = R_{L2} + R_o$ and $C = C_{VDD} + C_{GND} + C_{N1} + C_{N3}$. However, if the neighbours have the same transition as the defective node, *vo* is pulled down (Figure 4.22), being closer to the final state. This behaviour has been experimentally obtained in Figure 4.19. Therefore, depending on the direction of the transition of the neighbours related to the transition at the defective node, it is pulled to an initial voltage value (*vo*) which may help or disturb, in terms of the required delay, its expected transition.

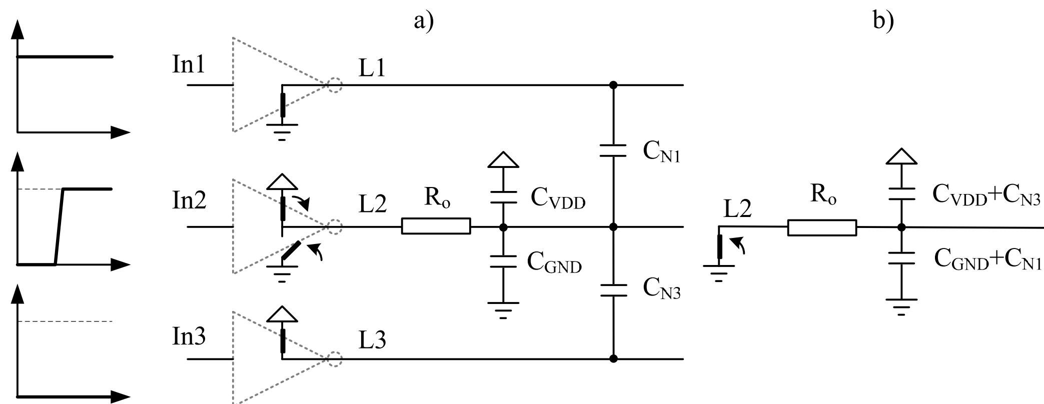

Figure 4.21. Transition at the defective line a) Neighbours at fixed voltages b) Equivalent circuit.

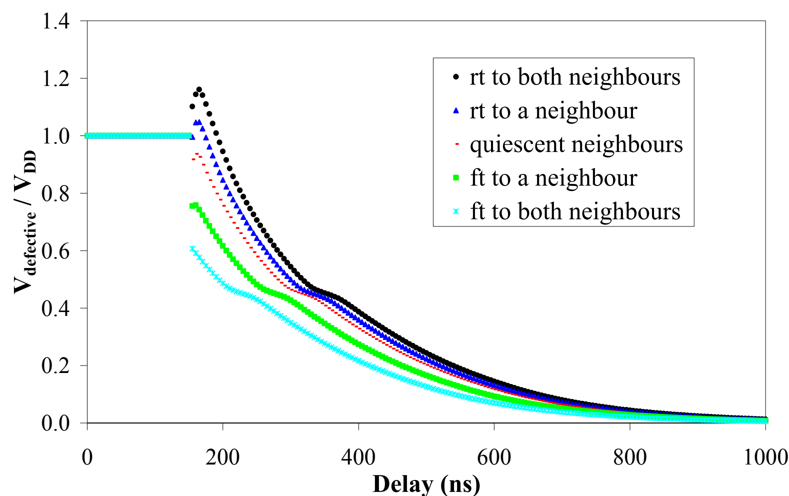

Figure 4.22. SPICE simulation results for the extracted fabricated design, $R_o = 20\ M\Omega$, ft: falling transition, rt: rising transition.

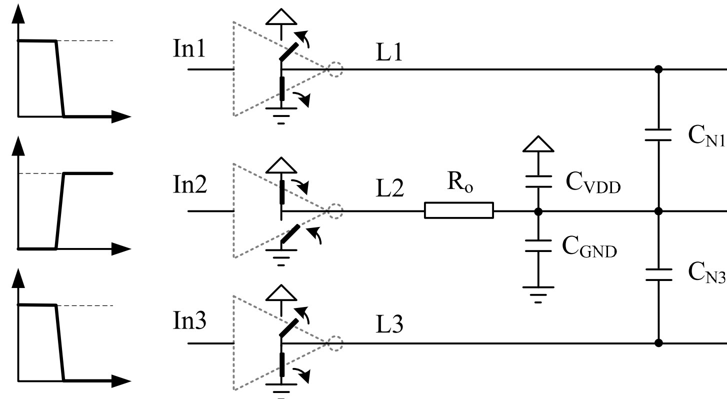

Figure 4.23. Opposite transition for the defective line and its neighbours.

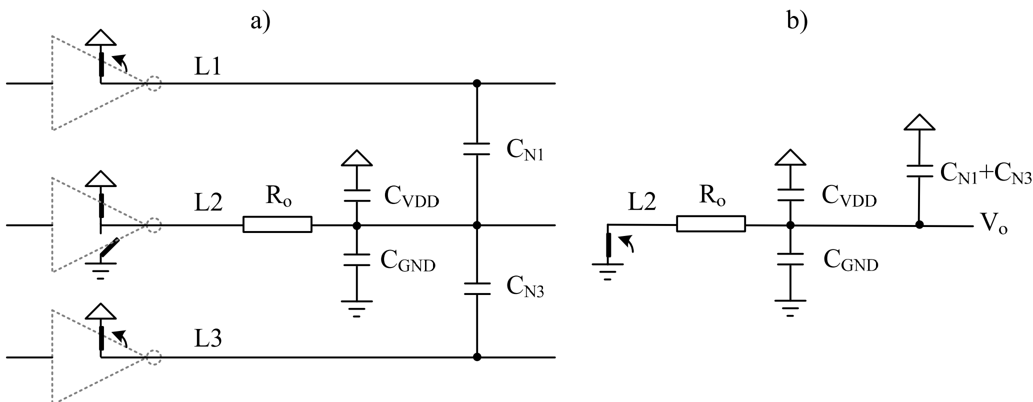

Figure 4.24. Neighbours with opposite transition related to the defective node a) Generation of an initial voltage at the defective node b) Discharging equivalent circuit.

4.1.3.3 TEST RECOMMENDATIONS FOR RESISTIVE OPENS

As already presented in the previous sub-section, the timing behaviour of the defective node follows a quasi-exponential charging or discharching behaviour, where the time constant of the delay due to the defect (τ) depends on the resistance value (R_o) and the equivalent defective downstream node capacitance $C_{eq-d}(N_1, N_2,...,N_l)$, as shown in (4.2):

$$\tau = R_{open} C_{eq-d}(N_1, N_2, ..., N_l) \tag{4.2}$$

where $C_{eq-d}(N_1, N_2,...,N_l)$ depends on all the capacitances located from the defect location up to the end of the line. For the $C_{eq-d}(N_1, N_2,...,N_l)$ calculation, it is required the definition of an indicator function $I'(N_i)$. This function considers the effective crosstalk capacitances between nets. It depends on the state of the neighbours as well as on the skew between the transitions of the target net and its neighbours. As a first consideration, assuming null skew, $I'(N_i)$ can be approximated as follows [175]-[179] (4.3):

$$I'(N_i)\begin{cases}0 \text{ for the same transition in } N_i\\ 1 \text{ for } N_i \text{ in quiescent state}\\ 2 \text{ for the opposite transition in } N_i\end{cases} \tag{4.3}$$

The expression for $C_{eq-d}(N_1, N_2,...,N_l)$ yields:

$$C_{eq-d}(N_1, N_2,...,N_l) = \sum_{i=1}^{i=l}\left(C_{Ni}\cdot I'(N_i)\right) + C_{substrate} + C_{well} + C_{gb} + C_{gs} + C_{gd} \tag{4.4}$$

The defective node has been supposed to drive an inverter and to be coupled to l neighbours. Notice that the expression for $C_{eq-d}(N_1, N_2,...,N_l)$ is similar to the denominator of (2.2). In order to obtain the highest delay due to the resistive open, we should set the neighbours' state in such a way that $C_{eq-d}(N_1, N_2,...,N_l)$ is maximized.

Location plays a similar role as seen in the case of full open defects. Every defect location may have a different optimal dynamic neighbours' state. Hence, the methodology based on the segment division of the defective node is also suitable to test for resistive opens. Let us consider again the example shown in Figure 4.15, but now assuming a resistive open instead of a full open defect. The optimal excitation of the neighbouring lines in order to maximize $C_{eq-d}(N_1, N_2,...,N_l)$ is shown in Table 4.VIII, where *rt* refers to a rising transition and *ft* to a falling transition.

TABLE 4.VIII
DELAY TEST FOR RESISTIVE OPENS

	Defect location					
Resistive node	**OPEN1**		**OPEN2**		**OPEN3**	
Neighbour	**RN =rt**	**RN = ft**	**RN =rt**	**RN = ft**	**RN =rt**	**RN = ft**
N_1	ft	rt	X	X	X	X
N_2	ft	rt	X	X	X	X
N_3	ft	rt	ft	rt	X	X
N_4	ft	rt	ft	rt	ft	rt
N_5	rt	ft	ft	rt	ft	rt

It is observed how the logic incompatibility between N_1 and N_5 causes the neighbours' state to be different between the *OPEN1* location and the *OPEN2* and *OPEN3* locations, respectively. For *OPEN1*, it is more advantageous to generate a transition at N_1 than setting both neighbours to logic opposite constant values, although this means that the opposite transition is generated at N_5.

4.1.4 HISTORY EFFECT

When carrying out the experiments with resistive opens, a non repetitive nature of some measurements was observed, even though the test and its conditions were fixed. In fact, the response to some test pattern sequences were influenced by the previous applied test patterns. This phenomenon is said to be the history or memory effect [180]. Some experiments have been conducted to evaluate the impact of this effect.

4.1.4.1 EXPERIMENTAL RESULTS

In order to analyze the history effect, an experiment has been applied to the resistive open *RN7*. Its goal is to compare the evolution of the defective node (V_{def}) starting from different initial voltage values. For this reason, V_{def} has been initialized to different values, as explained next. The delay test is then applied. Figure 4.25 illustrates a simplification of the electrical circuit considered.

The experiment considers a rising transition at V_x. The delay between the launch and the capture phase is 50 ns. Proper sequences of 0s and 1s has been previously applied to the defective node, from 0% to 100% of 1s to initialize V_{def} to different values. The results for different resistances are listed in Table 4.IX, where '*d*' denotes the detection of the defect, and '•' denotes a test escape.

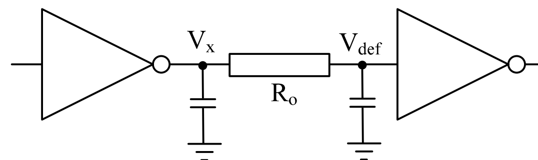

Figure 4.25. Defective line with quiescent neighbouring lines.

From Table 4.IX, it is observed that the higher the initialization voltage value, the smaller the delay. If the value of the resistance is not high enough to cause V_{def} to evolve sufficiently slowly (R_{o1} in Table 4.IX), V_{def} reaches the final state, escaping the test. This fact is also observed for the sequence of 100% of 1s for any open resistance ranging from R_{o1} to R_{o4}. In this case, independently of the resistance value, V_{def} is already in its final state. As the percentage of initialising % of 1s decreases, the required excursion of V_{def} to achieve its final state increases. Resistive defects which were not detected are now detected. Finally, when the initialization consists only in 0s, the initial state is the furthest one from the final state. The excursion is now the highest one. In this case, only the lowest resistive defect is not detected, since the added delay does not cause the circuit timing response to exceed the clock period.

TABLE 4.IX
HISTORY EFFECT RN7

Sequence of 0s and 1s pulses	R_o 100 kΩ < R_{o1} < R_{o2} < R_{o3} < R_{o4} < 100 MΩ			
%1s	R_{o1}	R_{o2}	R_{o3}	R_{o4}
100	•	•	•	•
90	•	•	•	d
80	•	•	•	d
70	•	•	•	d
60	•	•	d	d
50	•	•	d	d
40	•	•	d	d
30	•	•	d	d
20	•	•	d	d
10	•	•	d	d
0	•	d	d	d

4.1.4.2 EXPERIMENTAL RESULTS DISCUSSION

For the analysis of the history effect, the effect of the quiescent neighbouring lines has been modelled by their coupling capacitances, as already shown in Figure 4.25. The (resistive) defective line behaves as a low-pass filter. If the time constant due to the defect is lower than the signal period, the floating node reaches its final state before the next clock period is generated. However, if the time constant is higher than the signal period, the defective node does not reach its final state when the next transition has already been generated. Therefore, for every clock cycle, the defective node does not start from the ideal logic 0 or 1 value, but from some intermediate value, as illustrated in Figure 4.26a. The steady state behaviour of the defective node depends on the ratio between the percentage of 0s and 1s previously applied (V_{def} has then a history-dependent value). The simulation results for the evolution of V_{def} for an input sequence where 70% of the values are logic 1s are illustrated in Figure 4.26a. Notice how, when starting from 0 V, the value of V_{def} increases until it reaches the region close to 70% of V_{DD}. The evolution of V_{def} for some sequences with different percentages of logic 1s is shown in Figure 4.26b. The differences between the final reached states of V_{def}, which will subsequently behave differently when a delay test is applied, are observed.

The history effect must be taken into consideration when testing for resistive opens. The time required by the defective node to reach its final state as a response to an input transition depends on its initial voltage value, as illustrated in Figure 4.26a and Figure 4.26b. The history effect might cause the defective node to reach its final state faster, and thus be able to escape the test, as with some of the results presented in Table 4.IX.

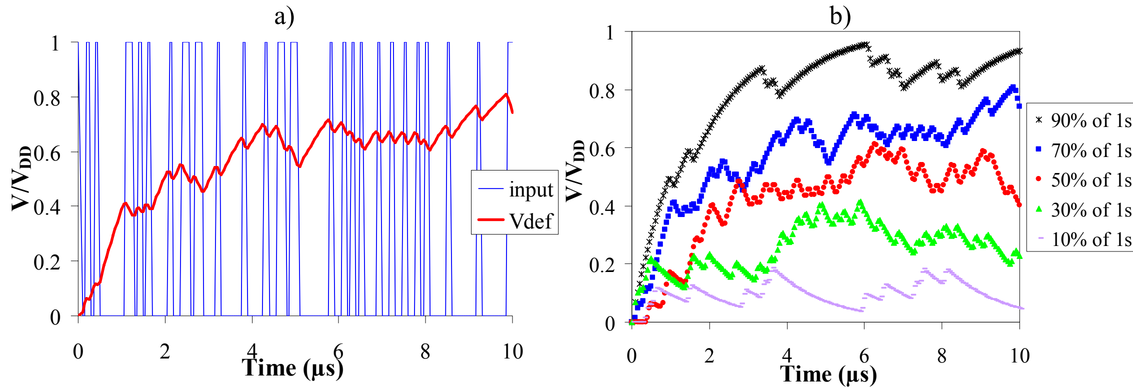

Figure 4.26. Evolution of V_{def} a) Input sequence of 70% of logic 1s b) Different input sequences.

4.1.4.3 TEST RECOMMENDATIONS FOR RESISTIVE OPENS

The history effect must be minimized when applying delay as well as logic test. Otherwise, resistive open defects may escape the test. For this reason, when applying a test to a specific target net, it must be ensured that:

- Logic test: The target net remains at low (high) logic value a sufficient number of clock cycles before applying a SA0 (SA1) test to the target net.
- Delay test: When testing for a rising (falling) transition, the target net remains to a low (high) logic value a sufficient number of cycles before the initialisation pattern is applied. In this way, it is assured that the target net must cover the maximum excursion to reach its final logic state.

The time constant of the system reported in (4.2) may determine the required time (number of clock cycles) to be sure that the defective node is at the expected initial voltage prior to the test. This time constant depends on the defect location, the resistance value and the neighbours' state. For every clock period, as the neighbours' state changes, $R_oC_{eq\text{-}d}(N_1, N_2,...,N_l)$ modifies its value. Supposing a waiting time of n cycles before applying the test to the target node, its evolution is a succession of quasi-exponential (dis)charging behaviours with a different time constant for every clock period, $R_oC_{eq\text{-}d}(N_1, N_2,...,N_l)_{(1)}$, $R_oC_{eq\text{-}d}(N_1, N_2,...,N_l)_{(2)}$, $R_oC_{eq\text{-}d}(N_1, N_2,...,N_l)_{(3)}$, …, $R_oC_{eq\text{-}}$

$_{d}(N_1, N_2,...,N_l)_{(n)}$. For that reason, in order to estimate the initialization time before applying the test to the target node, two parameters should be previously calculated. On the one hand, a critical resistance value (R_c), which is the maximum resistance value to be detected during the test. On the other hand, if the calculation of n different $C_{eq-d}(N_1, N_2,...,N_l)$ corresponding to every different clock cycle is not desired, the worst scenario can be assumed. The slowest evolution of the defective node occurs for the maximum value of $C_{eq-d}(N_1, N_2,...,N_l)$, $C_{eq-d}(N_1, N_2,...,N_l)_{(max)}$. It can be considered the value of $C_{eq-d}(N_1, N_2,...,N_l)_{(max)}$ for all the cycles. Therefore, setting the target node $3R_cC_{eq-d}(N_1, N_2,...,N_l)$ to its initial logic value prior to the application of the test should be sufficient to minimize the effect of the history effect on the detectability of resistive opens.

4.1.5 MAXIMUM DELAY OWING TO INTERCONNECT RESISTIVE OPENS

An interconnecting resistive open defect weakens the signal propagated along the affected line and, as a consequence, it becomes more vulnerable to parasitic coupling capacitances. The resulting delay of the defective line depends on the open resistance as well as on the parasitic capacitances to the faulty net. Traditionally, it has been reported that the maximum delay is obtained when the resistive open is located at the beginning of the net [81]. This behaviour is accomplished as long as the open resistance (R_o) is orders of magnitude higher than the equivalent on-resistance (R_{on}) of the transistor network driving the faulty net. However, this behaviour is not followed by low resistive opens. Indeed, when the open resistance and the on-resistance are in the same order of magnitude, the maximum delay is found in the case of the open located at an intermediate point of the line.

4.1.5.1 EXPERIMENTAL RESULTS

For the Metal 4 configuration, an experiment like the one in Figure 4.26 has been carried out with the transmission gates in a low resistive state, so that their equivalent resistances are in the order of magnitude of a few kΩs, similar to the on-resistance of the downstream inverters. The results of the delay test are shown in Table 4.X. Observe how the maximum delay is obtained for the middle location of the defect, whereas the minimum delay is obtained for the resistive open located at the far end of the line (close to the downstream gate). This is not the usual behaviour, since it is expected that a resistive open causes the maximum delay when it is located at the beginning of the net

(close to the driving gate). The next subsection is focused on analysing and justifying this behaviour observed experimentally.

4.1.5.2 INTERCONNECT RESISTIVE OPEN BEHAVIOUR

Without loss of generality, let us consider the example in Figure 4.27a, where an inverter drives a faulty line owing to a resistive open. The value of the coupling capacitances located before or after the open (modelled in Figure 4.27a as αC and $(1\text{-}\alpha)C$, respectively) depends on the open location (α). For high resistive opens, V_x can be assumed to evolve instantaneously compared to V_{def}. The delay due to the driver is then negligible and the total delay can be approximated by a first order model, where the delay caused by the open [71] is expressed by (4.5):

$$\tau_{total} \approx \tau_{open} = R_o(1-\alpha)C \qquad (4.5)$$

TABLE 4.X
DELAY TEST RESULTS

Open location (α)	Delay (ns)
0	5.65
0.5	5.80
0.9	5.65
0.99	5.60

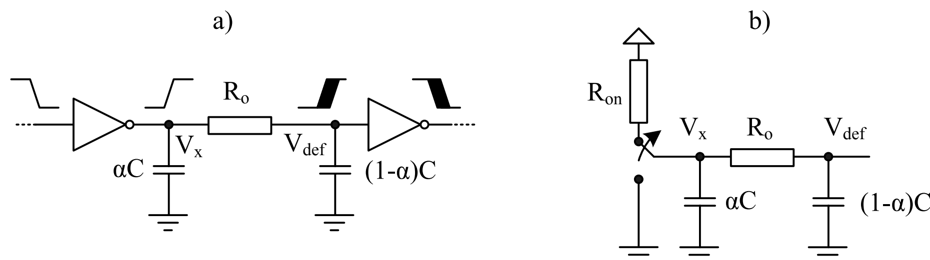

Figure 4.27. Rising transition at the faulty line a) Gate level b) Equivalent circuit.

From (4.5) it is derived that the maximum delay is obtained as the open is located at the beginning of the net ($\alpha = 0$). Nevertheless, for low resistive opens, the previous approximation does not give accurate results. In this case, the voltage on V_{def} is already evolving when V_x has not yet arrived to its final state. Thus, the instantaneous V_x value impacts the on-resistance of the transistor driving the faulty net which, in turn, impacts the time constant of the whole system. Consider the second order approximation to model the behaviour of the resistive open. Then, from Figure 4.27b, the following relationships are found:

$$I_{R_{on}} = I_{\alpha C} + I_{R_{open}} \quad (4.6)$$

$$I_{R_{on}} = \frac{V_{DD} - V_x}{R_{on}} \quad (4.7)$$

$$I_{R_{open}} = \frac{V_x - V_{def}}{R_{open}} \quad (4.8)$$

$$I_{\alpha C} = V_x \alpha C s \quad (4.9)$$

$$I_{(1-\alpha)C} = V_{def}(1-\alpha)Cs = I_{R_{def}} \quad (4.10)$$

Solving this system of equations for V_{def} yields:

$$V_{def} = \frac{V_{DD}}{R_{on}R_{open}(\alpha - \alpha^2)C^2 s^2 + (R_{open}(1-\alpha) + R_{open})Cs + 1} \quad (4.11)$$

For ease of understanding, assume that $R = R_{on} = R_o$, then the expression for V_{def} in the time domain is determined by (4.12).

$$V_{def} = V_{DD}\left(1 + \frac{2(\alpha-\alpha^2)}{\beta(2-\alpha+\beta)} e^{\frac{-2+\alpha-\beta}{2RC(\alpha-\alpha^2)}t} - \frac{2(\alpha-\alpha^2)}{\beta(2-\alpha-\beta)} e^{\frac{-2+\alpha+\beta}{2RC(\alpha-\alpha^2)}t}\right) \quad (4.12)$$

where

$$\beta = \sqrt{5\alpha^2 - 8\alpha + 4} \quad (4.13)$$

The V_{def} value depends on the time (t) and the open location (α). Considering $R = R_{on} = R_o = 2\ k\Omega$, Figure 4.28a and Figure 4.28b illustrate two three-dimensional plots based on (4.12) for two different capacitance values, (C = 100 fF and C = 1 pF, respectively). The contour lines represent the delay to reach a particular voltage value on V_{def}. (in steps of 10% of V_{DD}). Notice how in both cases, in order to reach V_{def}/V_{DD} up to 0.3, the maximum delay is not obtained at the beginning of the net ($\alpha = 0$), but for an intermediate open location. For values higher than 0.3, the maximum delay is obtained at the beginning of the net. From the analysis of the dependence of (4.12) on the capacitance value (C), its impact is quite negligible.

Similar to (4.12), it is possible to obtain a more general equation assuming $R_{on} \neq R_o$. However, the expression is so tedious that it was not worthy to be reported. On

the one hand, the plot in Figure 4.29a illustrates an example when $R_{on} < R_o$. The range of V_{def} values where the maximum delay is not obtained for an open located at the beginning of the net has decreased related to the example in Figure 4.28b. This behaviour is only reported when $V_{def}/V_{DD} \leq 0.1$. On the other hand, an example when $R_{on} > R_o$ is depicted in Figure 4.29b. In this case, maximum delays when $\alpha \neq 0$ are obtained for V_{def}/V_{DD} values up to 0.35. Therefore, the lower the ratio R_o/R_{on}, the higher the range of V_{def} values where the maximum delay is not obtained for $\alpha = 0$.

a) b)

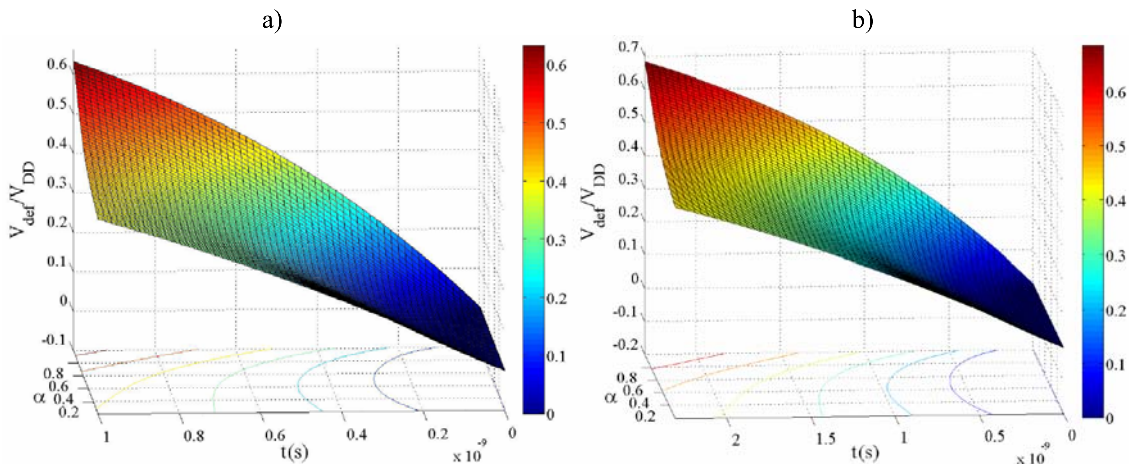

Figure 4.28. Three-dimensional plot based on (4.12) when $R_{on}= R_o= 2$ kΩ a) C = 500 fF b) C = 1 pF.

a) b)

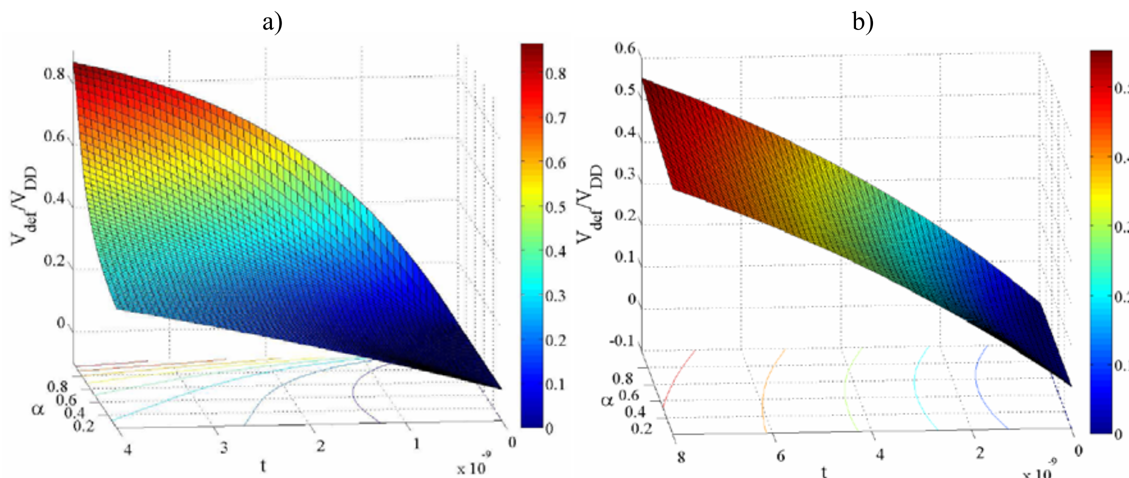

Figure 4.29. Three-dimensional plot (C = 1 pF) a) $R_{on}= 2$ kΩ, $R_o= 10$ kΩ b) $R_{on}= 10$ kΩ, $R_o= 2$ kΩ.

So far, the timing behaviour of the defective node (V_{def}) has been presented. Nevertheless, it has not still been evaluated whether this behaviour propagates to the outputs of the circuit. Given an on-resistance and an open resistance, let us denote $V_{def(max)}$ as the maximum V_{def} value where the maximum delay is not obtained for an open located at the beginning of net. This behaviour is propagated along the circuit for a rising (falling) transition provided that the threshold voltage of the nMOS (pMOS)

transistor driven by the faulty net is lower (higher) than $V_{def(max)}$. From here on, a rising transition on the defective net is assumed (it is straightforward to extract the conclusions for a falling transition). When $R_o >> R_{on}$, $V_{def(max)}$ is much lower than $V_{TH(nMOS)}$ of the transistor driven by the faulty net. This fact explains why in these cases the open location generating the maximum delay is always for $\alpha = 0$. Figure 4.30a depicts the relationship between $V_{def(max)}$ and the ratio R_o/R_{on}. As already commented, the lower R_o/R_{on}, the higher $V_{def(max)}$. Assuming that the threshold voltage of an nMOS transistor is approximately 20% of the power supply voltage, it is observed that the propagation of this phenomenon along the circuit is only accomplished up to open resistances twice the on-resistance value. However, the exact location of the open where the maximum delay is obtained depends on R_o/R_{on} and the total capacitance. As an example, Figure 4.30b shows the relationship between V_{def} and the open location reporting the highest delay for different R_{on} values.

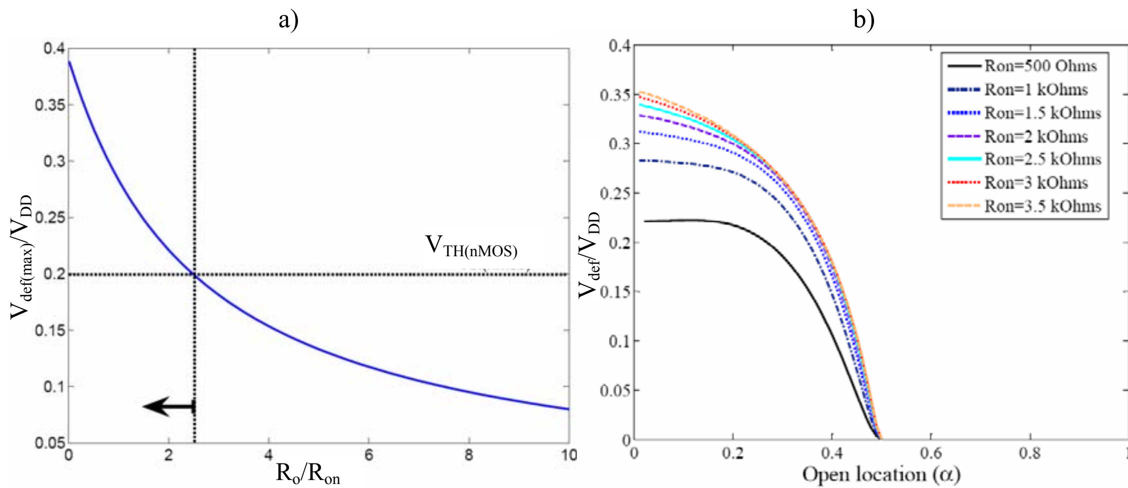

Figure 4.30. a) $V_{def(max)}$ vs. the ratio R_o/R_{on} when R_{on}= 1 kΩ and C = 100 fF b) Relationship between V_{def} and α for the maximum delay when R_o=1 kΩ and C=100 fF.

The results presented so far relies on the equivalent circuit from Figure 4.27, where the on-resistance is assumed to be constant. However, it is widely known that the equivalent resistance of a MOS transistor is not constant, and depends on V_x. Therefore, SPICE simulations of the circuit in Figure 4.27a have been carried out based on a 0.35 µm technology from *AMS*. The resistive open has been assumed to be low resistive (in the range of kΩ). The delays obtained related to the open location (on the x-axis) and the open resistance (on the y-axis) are illustrated in Figure 4.31 for two different capacitances. The contour lines represent the measured delay in nanoseconds. Notice

that for low resistive opens (up to 5 kΩ when C = 100 fF and 5.7 kΩ when C = 1 pF), given an open resistance value, the highest delay is obtained for the open located in an intermediate point of the faulty line. The geometric locus of maximum delay locations for each given resistance is represented by the dotted line. The open location causing the maximum delay moves to the beginning of the net as the open resistance increases. For high resistive opens, there is not an intermediate location causing the maximum delay anymore. Given such high open resistances, the delay decreases monotonously and the location generating the highest delay is always at the beginning of the net. Similar results are obtained assuming a falling transition at the defective line and considering other basic gates.

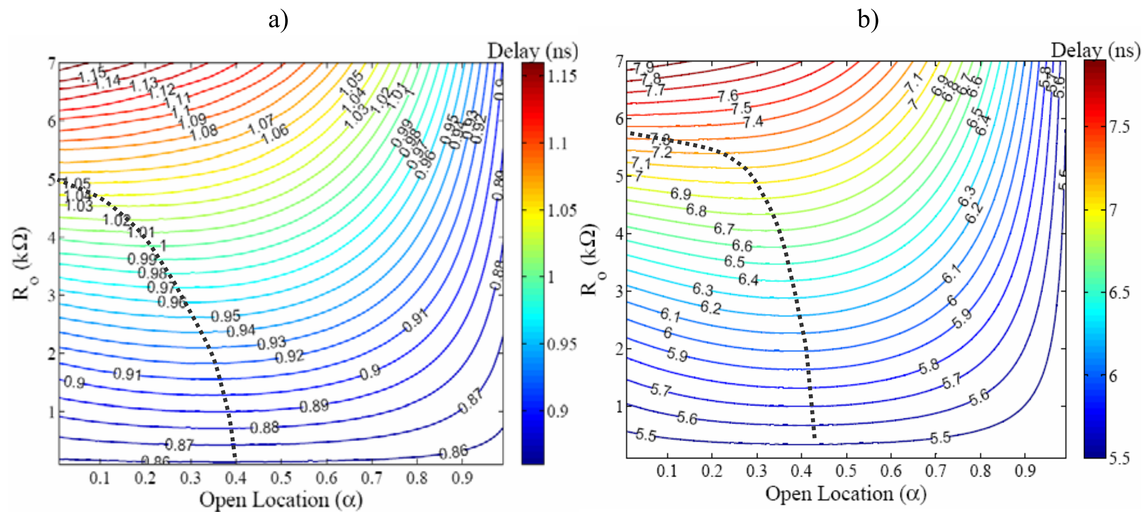

Figure 4.31. Delay vs. Open location and R_o for the example in Figure 4.27a. The dotted line represents the set of open locations causing the highest delay a) C = 100 fF b) C = 1 pF.

For low resistive opens, the open location generating the highest delay not only depends on the relationship between the open resistance and the equivalent on-resistance of the transistors network driving the faulty net, but also on the threshold voltage of the transistors driven by the faulty net and on the parasitic capacitances (length of the faulty net). The delays obtained by simulations of the example in Figure 4.27a depending on the open location (on the x-axis) and on the length of the faulty net (on the y-axis), routed in Metal1, are shown in Figure 4.32. The open resistance has been considered R_o = 3 kΩ. The contour lines represent the delay in nanoseconds. The dotted line describes the open locations generating the highest delay for a given line length. Notice that the intermediate open location causing the highest delay depends

slightly on the length of the line. Indeed, the maximum delay obtained for an intermediate open location is more noticeable as the length of the line increases.

To corroborate the experimental results shown in Table 4.X, the corresponding SPICE simulations have been carried out for the designed circuit, assuming different open locations. The simulation results at the nominal, low and fast corners of the process for the AMS technology together with the experimental results measured with the tester are shown in Figure 4.33 Notice how the experimental results are consistent with the ones obtained by simulation.

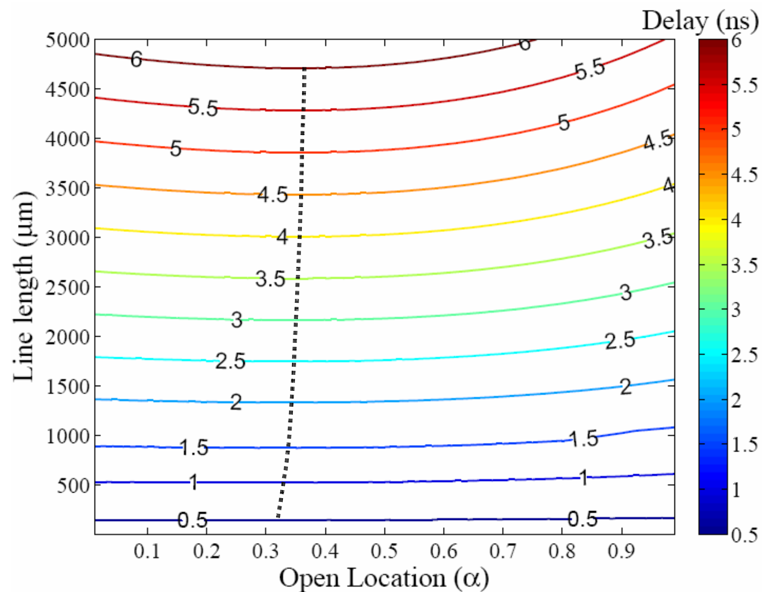

Figure 4.32. Delay vs. Open location and line length for the example from Figure 4.27a (R_o=3 kΩ). The dotted line represents the set of open locations causing the highest delay given a line length.

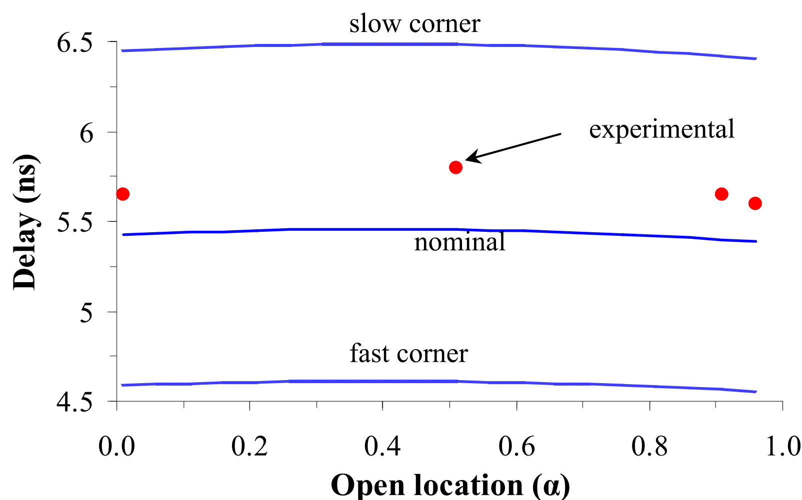

Figure 4.33. SPICE vs. experimental delay for the transmission gates is in a low resistive state.

4.2 DIAGNOSIS OF INTERCONNECT OPENS BASED ON THE FOS MODEL

The diagnosis of open defects has been addressed in a number of previous works. However, the diagnosis of this class of defects is difficult because insufficient layout information from the circuit has been considered is most of them [133]-[134], [152], [154], [156]-[157]. For diagnosis tools, if only logic information and gate level description of the circuit are considered, a non-negligible amount of equivalent physical locations can be found for each given suspicious signal. Some recent works have also focussed on pinpointing the faulty segment, instead of just diagnosing the defective signal using layout information [135]-[137].

The experimental results obtained from the fabricated circuit showed the strong impact of parasitic coupling capacitances on the voltage of floating lines. In this direction, this section presents the Full Open Segment (FOS) model [181] for the diagnosis of interconnect full open defects. The main advantage is that this model assumes that the full open can be located in any point in the interconnect architecture between the output of the driver and the input of any of the downstream gates. Thus, vias and interconnecting metal lines are considered.

4.2.1 FULL OPEN SEGMENT MODEL

The FOS model [181] is derived from the topology of the circuit. It divides the defective line into a set of segments, which are subsequently used for the computation of the floating node voltage. In order to proceed to the division of the defective line, topological information of the line itself and of the surrounding signals are extracted from the physical design. The required data relates to the dimensions and relative locations between the wires to compute the coupling capacitances [182]. The physical topology determines the partition of the defective line into segments. Within a given segment, the relative distances between wires and their dimensions are kept constant. In order to illustrate the FOS model, assume the line shown in Figure 4.34. According to its topology, it is made up of some pieces of metal belonging to different layers having different distances (height) to substrate or well. In this example, three metal layers going from the lowest metal level (*M1*) up to the third layer (*M3*) are shown. In order to compute the coupling (parasitic) capacitances of the line to substrate or well, four

parameters for each piece of metal composing the line need to be computed: namely, the length of the piece of wire (*L*), the thickness (*TH*) and the width (*W*) at each metal level and the height of the dielectric for each metal level (*H*).

In Figure 4.35 it is shown an example of the surrounding interconnect lines coupled to the target line. Four different neighbours are drawn. The top-view of the same example is depicted in Figure 4.36. Neighbour 1 (labelled N_1) is made of Metal1 (*M1*). It is placed at a distance d_1 from the floating node and has a coupling length to the floating line of L_{CN1}. Neighbour N_2 is made of three metal layers, namely: *M3*, *M2* and *M1*. It has a total coupling length of L_{CN2} and it is placed at a distance d_2 from the floating line. Neighbour N_3 is made of a unique metal level but composed of two pieces of wires located at different distances, d_3 and $d_{3'}$ from the floating node. On the other hand, neighbour N_4 is made of three different metal layers similar to N_2. No vias are depicted in Figure 4.36 since their contribution to the electrical behaviour of the floating line is negligible (low resistance). Only neighbours made of the same metal layer as the target line are drawn for this example. Nevertheless, the methodology can be applied to coupling lines between different metal levels provided that the corresponding layout information is available.

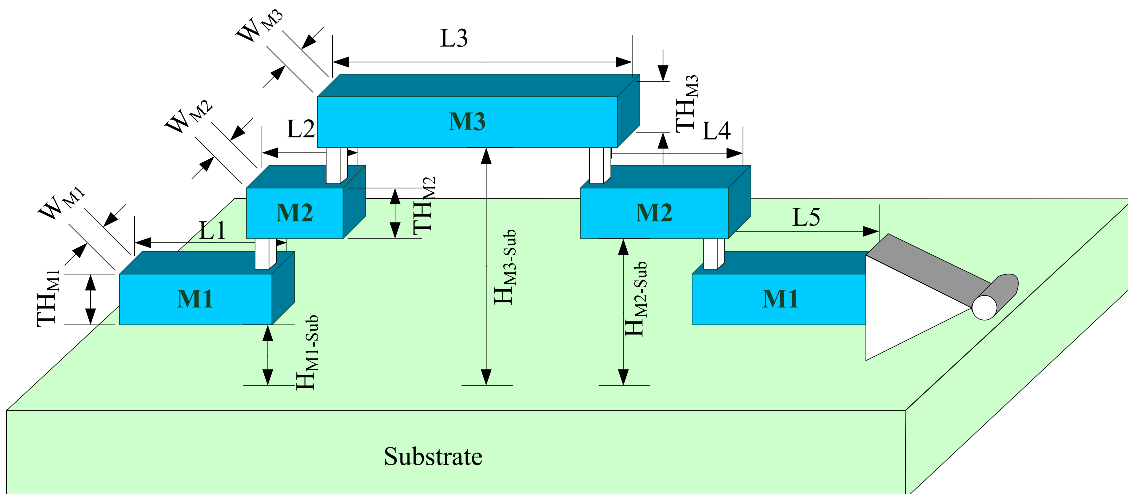

Figure 4.34. Topological information of an interconnect line.

According to the topological information shown in Figure 4.34 and Figure 4.36, the electrical behaviour of the floating node can be evaluated, since the coupling capacitances to the neighbouring lines and to substrate and well can be easily computed. The trapped charge is also referenced in Figure 4.36 as well as the capacitances added by the next gate(s) placed at the end of the line. This information may be determinant in

the resulting voltage of the floating line in the case of short lines or open defects located at the far end of the line.

The target node is proposed to be divided into several segments (*Seg_i*) as illustrated in Figure 4.37. Segment breaks are caused by a change in the neighbourhood. Examples of these changes are the discontinuation of a neighbouring line (breaks segment *Seg_1* and *Seg_2*), a change in distance to a neighbouring line (break segments *Seg_5* and *Seg_6*) or a change in the coupling area due to a change in the thickness of the coupled lines (break segments *Seg_7* and *Seg_8*). Hence, the coupling capacitance per unit length is constant within a segment. The neighbouring lines routed in different metal layers from the target line are discarded. Anyway, this distance boundary can be adapted to each particular design. Therefore, each segment consists of the target line and at the most, two neighbouring lines. In Figure 4.37, nine segments have been obtained.

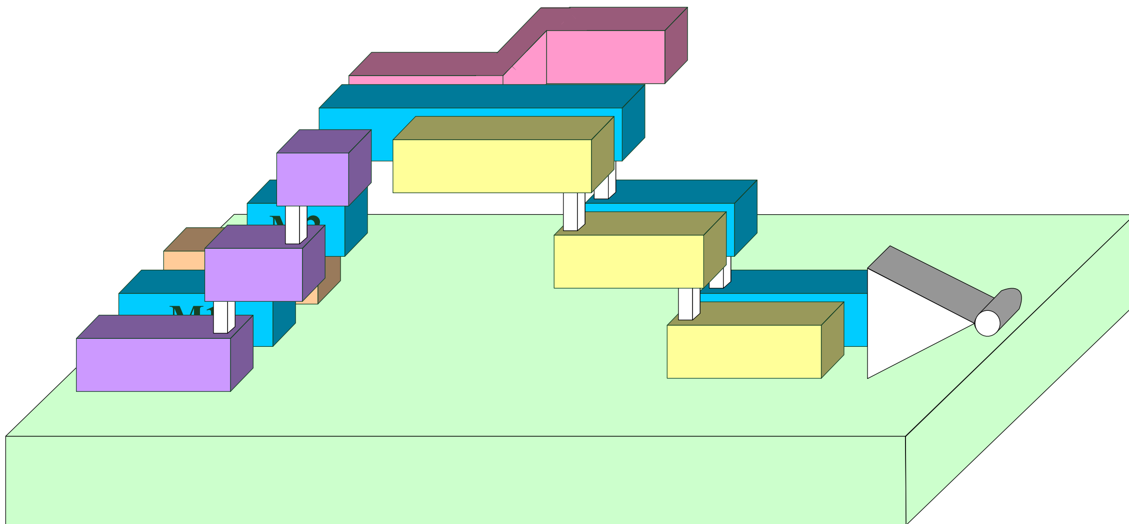

Figure 4.35. Interconnect line and its neighbouring lines.

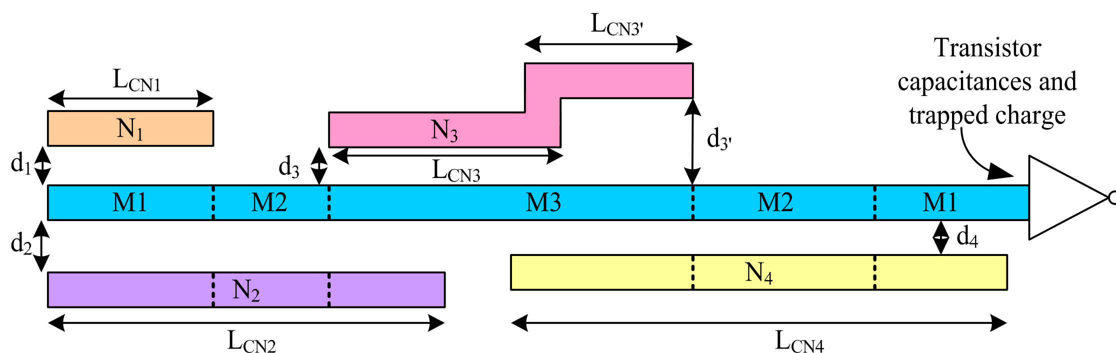

Figure 4.36. Top-view of the layout of the interconnect line and its neighbouring lines.

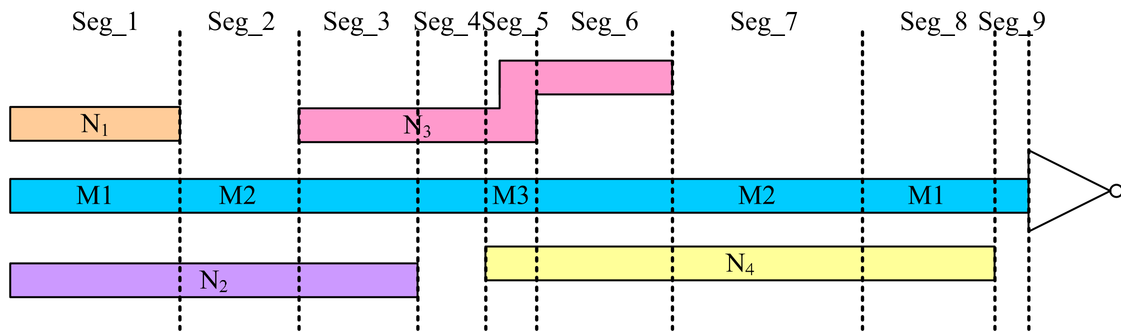

Figure 4.37. Segment division based on the topology of the surrounding circuitry.

Once the target line has been divided into the appropriate set of segments, the two resulting coupling capacitances to the power rails are extracted in order to compute the node voltage for each particular test pattern. Notice that depending on the logic value of the neighbouring lines and on the type of substrate or well area over which lies the line in a particular segment k, the coupling capacitance can have only contributions to V_{DD} (C_{up}), only to V_{GND} (C_{down}) or, most probably, contributions of both signs.

4.2.2 FLOATING LINE VOLTAGE

The voltage of floating lines is not controlled by the previous gates but by the neighbouring lines. As a result, consistent fail behaviour is not observed, which makes these defects hard to analyse with electrical failure localisation tools. Thereby, the voltage of the floating line must be calculated to determine its logic interpretation. The actual voltage depends on the capacitive divider made up of the capacitances lying between the location of the full open and the end of the line. Hence, it can be constructed a function for this floating line voltage in which the logic state of the neighbours for a particular test pattern and the location of the open denoted by the segment is considered.

Assume a defective line with extracted coupling capacitances as illustrated in Figure 4.38. The full open defect is located in segment k. Each segment is described with one resulting coupling capacitance connected to V_{DD} and one to V_{GND}. The terms in the capacitive divider consists of the contribution of the next segments after the open (segment i, with $i > k$) and the defective segment (k) itself. The contribution of the next segments is a constant figure determined by C_{up} and C_{down} and the state of the neighbouring lines, while the contribution of the segment containing the defect depends on the internal location (x) of the open in the segment. The defect location can range

between the beginning of the segment ($x = 0$) up to its end ($x = L_k$). Since it is a linear dependence, it is sufficient to calculate only the values at the beginning and at the end of the segment, performing then an interpolation of these results for any other intermediate position. In this way, it is possible to determine the voltage of the floating line (V_{Fline}) assuming an open at the end of segment k and for a test pattern (TP) by the following expression:

$$V_{Fline}(k,TP) = \frac{\sum_{i=k+1}^{N} C_{up_i}}{\sum_{i=k+1}^{N} C_{up_i} + \sum_{i=k+1}^{N} C_{down_i}} V_{DD} \tag{4.14}$$

while if the open is not at the end of segment k, the linear dependence is used obtaining the expression in (4.15):

$$V_{Fline}(x,k,TP) = V_{Fline}(k-1,TP) + \frac{x}{L_k}\left(V_{Fline}(k,TP) - V_{Fline}(k-1,TP)\right) \tag{4.15}$$

where x is the location of the open defect in segment k, going from 0 up to its total segment length (L_k). This equation enables to calculate the voltage of the floating line and to predict the observed logic value by the receiving gates.

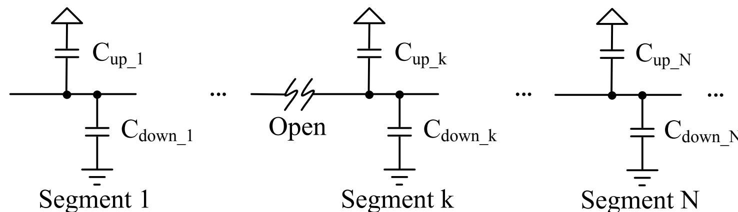

Figure 4.38. Full open located in segment k of an interconnect line divided into N segments.

4.2.3 FAN-OUT

Floating lines with only one receiver have been so far considered. Nevertheless, the floating line may drive multiple downstream gates (fan-out). In this case, the capacitive divider must include the capacitances generated by the treelike lines connected to the floating net between the open location and the end of the fan-out branches. Consider the example in Figure 4.39, where the floating line is driving two inverters. Five neighbours are coupled to the floating line. The corresponding top view for this example is described in Figure 4.40. Assuming an open at the beginning of the net (*OPEN1*), the parasitic capacitances to all the neighbours must be considered. If the open is located on the via connecting the metal tracks on *M3* and *M2* (*OPEN2*), only the

neighbours coupled to the fan-out branches must be considered (neighbours $N4$ and N_5). Finally, if the open is located at the beginning of one of the fan-out branches (*OPEN3*), the neighbour coupled to the other branch (N_5 in this case) is neglected and only N_4 is considered. The equivalent circuits assuming these three open locations are shown in Figure 4.41.

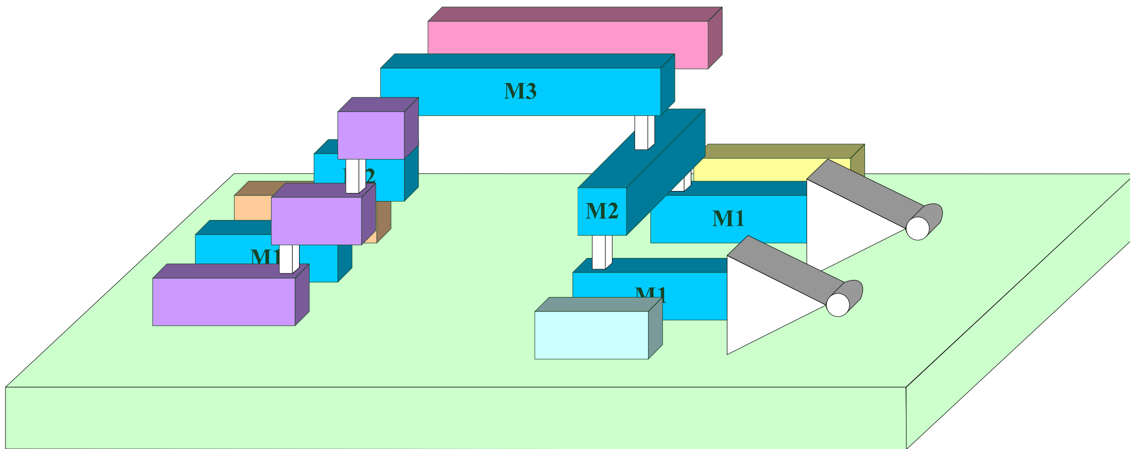

Figure 4.39. Generic interconnect line with fan-out and its neighbouring lines.

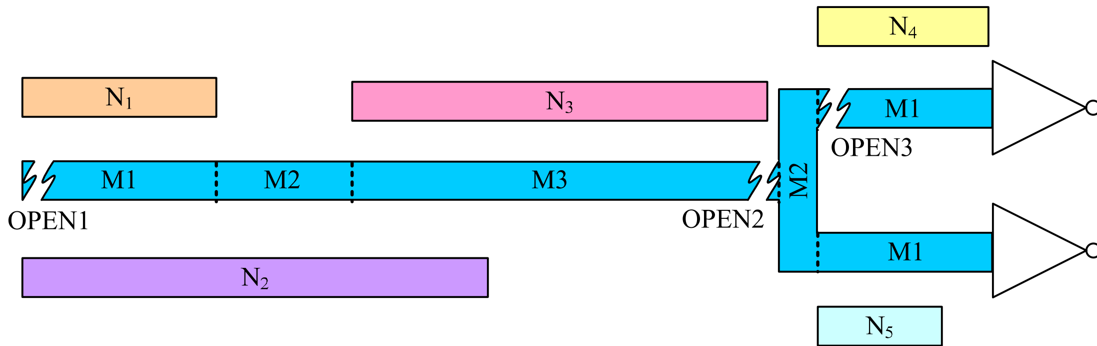

Figure 4.40. Top view of the interconnect line with fan-out and the surrounding circuitry.

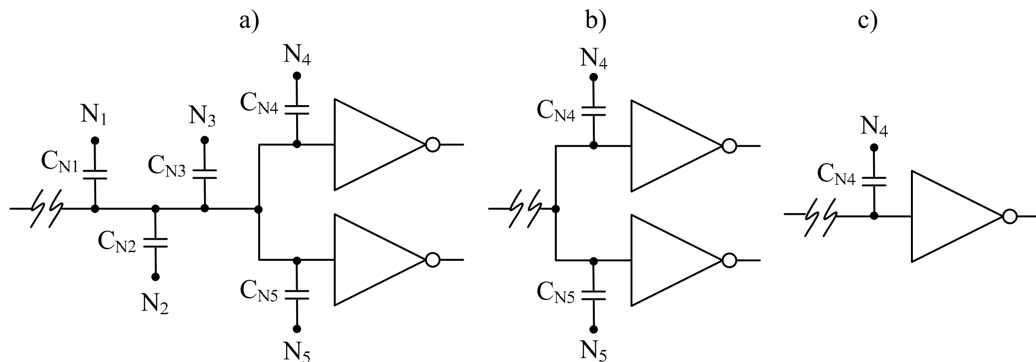

Figure 4.41. Equivalent circuits for the examples in Figure 4.40 a) OPEN1 c) OPEN2 c) OPEN3.

4.2.4 Voltage Based Diagnosis Of Full Open Defects

Utilising the full open segment (FOS) model, diagnosis of full open defects can be performed on interconnect lines. For this analysis, one needs a line suspected to contain an open, e.g. determined with a fault localization tool, and the failing results of a voltage test. The information given by the voltage test allows knowing which logic level on the target line has been interpreted by the rest of the circuit, for each applied test pattern (*TP*). The matching between this measured logic value and the computed $V_{Fline}(k, TP)$ is the basis of the proposal for the diagnosis of full open defects. As an example, assume a circuit with three applied test patterns, namely, TP_1, TP_2 and TP_3. The results for the calculated $V_{Fline}(k,TP)$ are depicted in Figure 4.42 for the whole set of segments (nine, in this example). From the results of the applied voltage test, it is determined that TP_1 and TP_3 caused the logic value of the floating node to be interpreted as a high logic value, while TP_2 caused the voltage of the floating node to be interpreted as a low logic value. To explain the observed logic results a location is required where the predicted voltage of the floating line for logic 1 results is always above those of logic 0 results. In other words, it is required an open location where the voltage predictions for TP_1 and TP_3 are above the one for TP_2. In Figure 4.42, the locations that fulfil this requirement are segments *Seg_4*, *Seg_5* and part of *Seg_6* (grey shaded area), which are thus the likely locations of the open fault.

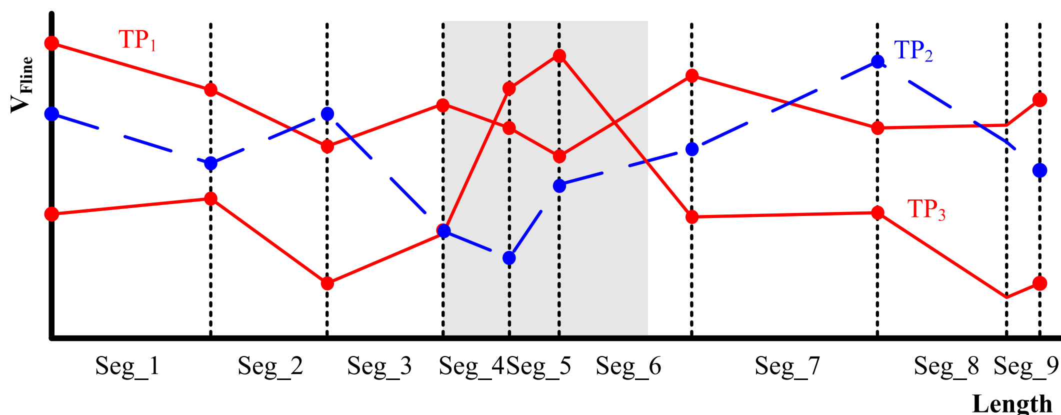

Figure 4.42. Voltage prediction of the floating line based on the FOS model. Test patterns interpreted as logic 1 drawn in solid red while patterns interpreted as logic 0 drawn in discontinuous blue.

The logic threshold of the downstream gates is usually not predictable, since they depend on the trapped charge, the temperature and process parameters, which may have wide variability. Only the relative values of the V_{Fline} are important since they are insensitive to the common contributions mentioned above. In this direction, the

contribution of the trapped charge does not change the relative position of the floating line voltages and thus is eliminated from the voltage computation.

4.2.5 CURRENT BASED DIAGNOSIS OF FULL OPEN DEFECTS

It may happen that the range of locations where the predicted voltage behaviour fits the tester results is not precise enough. In those cases, quiescent current information (I_{DDQ}) can be used to specify the location of the open more accurately. Knowing the downstream gate and its input port driven by the floating line, it is possible to carry out an electrical simulation, which relates the current consumed by the downstream gate and the voltage of the floating line, as pointed out in Figure 4.43a. For each given segment and test pattern, V_{Fline} has been previously computed. Hence, from I_{DDQ} vs. V_{FLine} characteristic obtained by simulation, a current prediction can be calculated. If an I_{DDQ} test is applied to the same pattern set used in the voltage test, it is possible to plot, for each segment and each particular test pattern, the current measured on the tester against the predicted current and determine then the coefficient of determination (R^2) in a similar way as previously seen for bridging defects. If the segment assumes the real location of the open, the set of points should be aligned as in Figure 4.43b. The coefficient of determination should be close to 1. However, if the segment does not assume the real open location, a scattered plot should be expected reporting a low R^2 value.

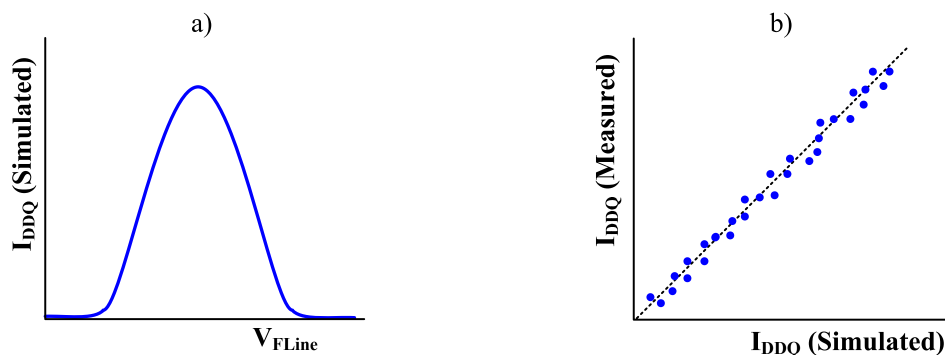

Figure 4.43. Simulated I_{DDQ} a) Vs. V_{Fline} b) Vs. Measured I_{DDQ} caused by V_{Fline}.

4.2.6 DIAGNOSIS ALGORITHM

The diagnosis algorithm consists of three main steps. The FOS method assumes that the suspicious nets potentially containing a full open are known. Hence, the first step is carried out by the *Faloc* diagnosis tool. The possible scenarios given by the tool

is the starting point for the FOS methodology, as reported in the diagnosis flow from Figure 4.44.

Assuming that it is possible that an open defect is present on the faulty device, from the *.lis* file where the *Faloc* results are reported, the candidates (target nets) which are susceptible to contain a full open defect are selected. The second step consists in locating the open based on voltage information. For every target net, the layout information from the own target net and its coupled neighbours are obtained. Once the layout information is accessible, the division of the defective line into different segments based on the FOS methodology is carried out. Subsequently, pattern information is used to predict the voltage of the floating line for every segment. In this manner, for every target net, a similar plot to the one in Figure 4.42 is generated. In case there is more than one possible location consistent with the voltage information, the third step of the methodology is applied, which consists of taking advantage of current information. The current consumed by the downstream gate for every pattern is predicted and compared with the corresponding current measured during the I_{DDQ} test. Then, it is straightforward to calculate the coefficient of determination. Subsequently, the open locations are ranked in a decreasing order according to the coefficient of determination.

4.2.7 EXPERIMENTAL EXAMPLE

In this section, the results obtained from the application of the FOS diagnosis methodology to a CMOS 0.18 μm *NXP Semiconductors* circuit (Device 82) are presented. A logic test has been applied where a set of 2920 SA patterns have been used. Around 36 failing vectors are captured by the tester during the logic test. With this information, the diagnosis tool (*Faloc*) reported as the first fail scenario a failing net, which is an interconnect line with a total metal length L = 250 μm. This line is driving the *B* port of a 4-input OR gate, as described in Figure 4.45. The interconnect line is routed comprising five metal layers and has 31 neighbouring lines. Figure 4.46a illustrates the layout of the line and its neighbours. After the FOS division, the line has been divided into 420 segments. From the data obtained in the ATE, only one test pattern makes the floating line to have a voltage value interpreted as logic 1 (red line in Figure 4.46b), the rest (in blue) have been interpreted as logic 0. There are two possible

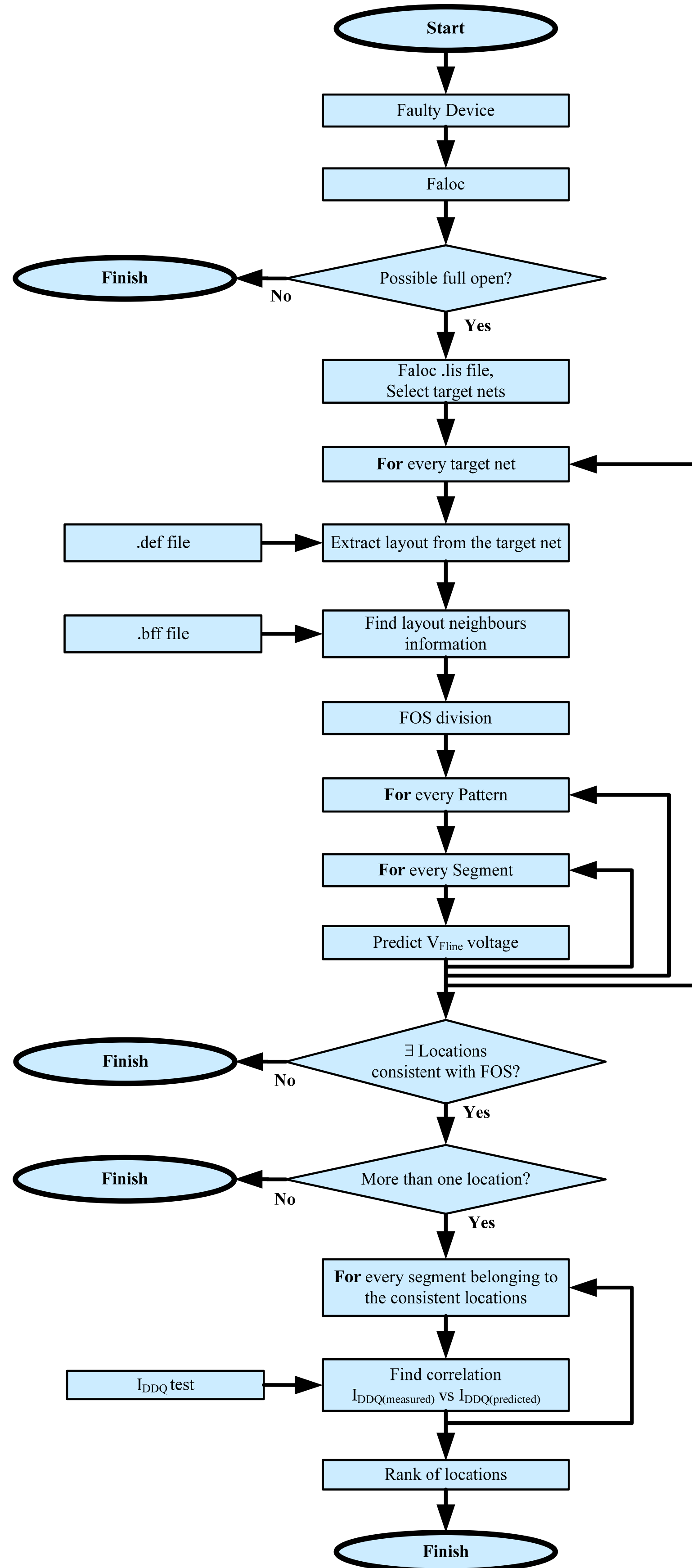

Figure 4.44. Diagnosis flow for full open defects applying the FOS methodology.

areas where the full open can be located (*A* and *B* in Figure 4.46b) since, in both areas, the voltage prediction of the pattern interpreted as logic 1 is higher than the voltage predictions of all the patterns interpreted as logic 0.

In order to discriminate between the two ranges of possible locations, the information related to the quiescent current consumption (I_{DDQ}) has been also taken into account. The downstream gate is a 4-input OR gate and the input driven by the defective node is the *B* port. An electrical simulation has been done to compute the current vs. input voltage relationship, as illustrated in Figure 4.47a. For each given segment and failing test pattern, the V_{Fline} has been computed and, according to Figure 4.47a, the expected current has been obtained (I_{DDQ} prediction) and compared to the measured values (Figure 4.47b) for that particular test pattern. Notice that some patterns are causing higher currents than the currents predicted by simulation in Figure 4.47a. This is due to current consumption of downstream gates driven by the 4-input OR gate (second stage of downstream current).

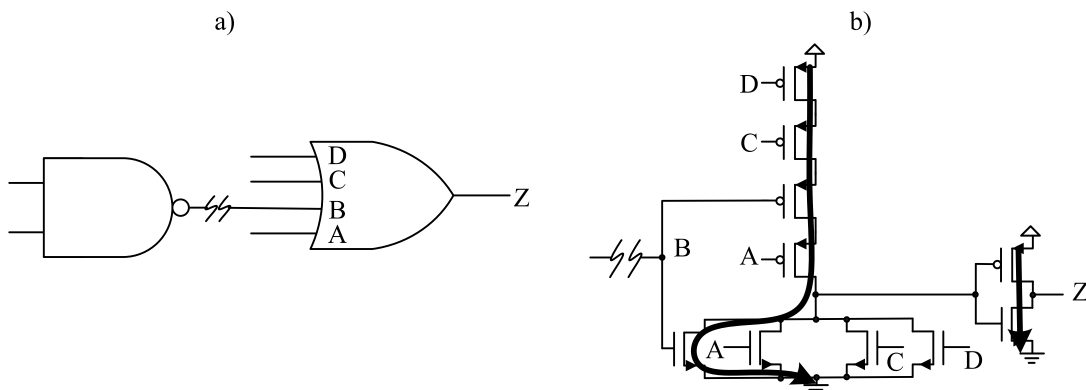

Figure 4.45. Full open in Device 82 a) Gate level b) Transistor level.

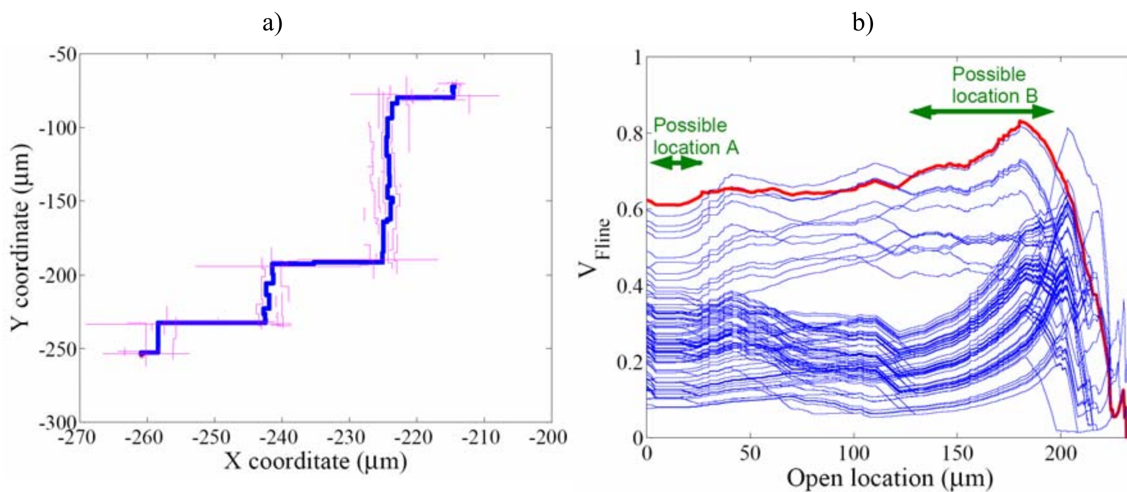

Figure 4.46. Device 82 a) Layout of the failing net and the coupled neighbours. b) Predicted normalized voltage of the failing net

Once obtained all the required information, it is possible to plot for each segment $I_{DDQ(predicted)}$ vs. $I_{DDQ(measured)}$ for every test pattern and determine then the coefficient of determination (R^2) of these data samples. Examples of these plots are shown in Figure 4.48a, b, and c for segment 1 which belongs to *A* (see Figure 4.46b), segment 250 which belongs to *B*, and segment 400 which belongs to a different arbitrary location, respectively. In general, if the coefficient of determination is calculated for every segment, the plot in Figure 4.48d is obtained.

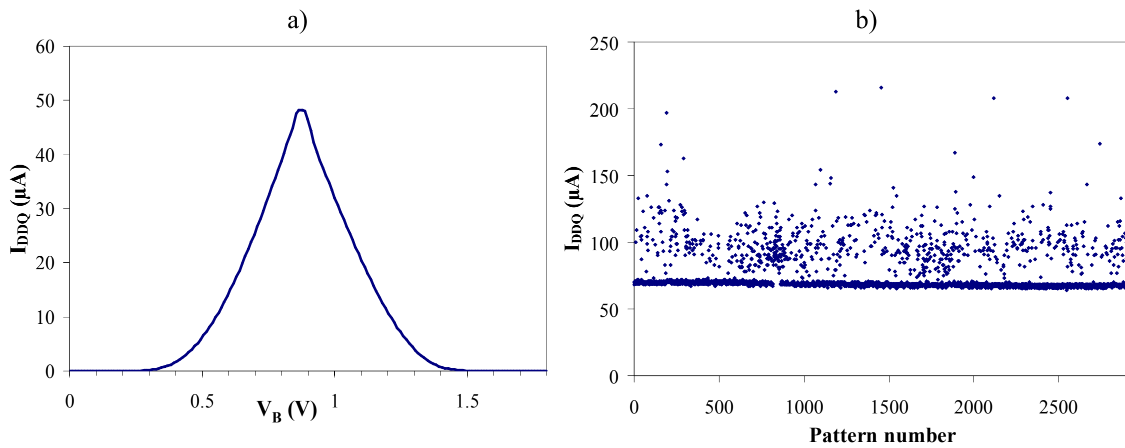

Figure 4.47. I_{DDQ} a) Simulation results related to V_B for OR gate b) Measurements for Device 82.

According to the correlation of determination, one of the two possible locations (*A*) is more likely to contain the full open defect. Based on this information, some extra test patterns have been added to the analysis. These patterns have caused high quiescent current consumption although they are not useful in terms of voltage testing, since they do not make observable the voltage of the failing net. The only test pattern causing a high logic value on the failing net (red line in Figure 4.46b) has also caused high current consumption on the defective device. Therefore, it is assumed that, for this test pattern, the voltage at the floating net has an intermediate value that causes the OR gate to have both n-network and p-network in an on-state. The selected (four) extra test patterns have also caused high current consumption in the circuit. Hence, the predicted voltage at the floating line for the extra test patterns should also lie around intermediate voltages close to the one obtained with the pattern causing a high logic value (red line in Figure 4.46b). The predicted voltage for the extra test patterns has been added to the V_{Fline} graph with green solid lines (see Figure 4.49). The close position between the four extra lines at location *A* agrees with the experimental behaviour.

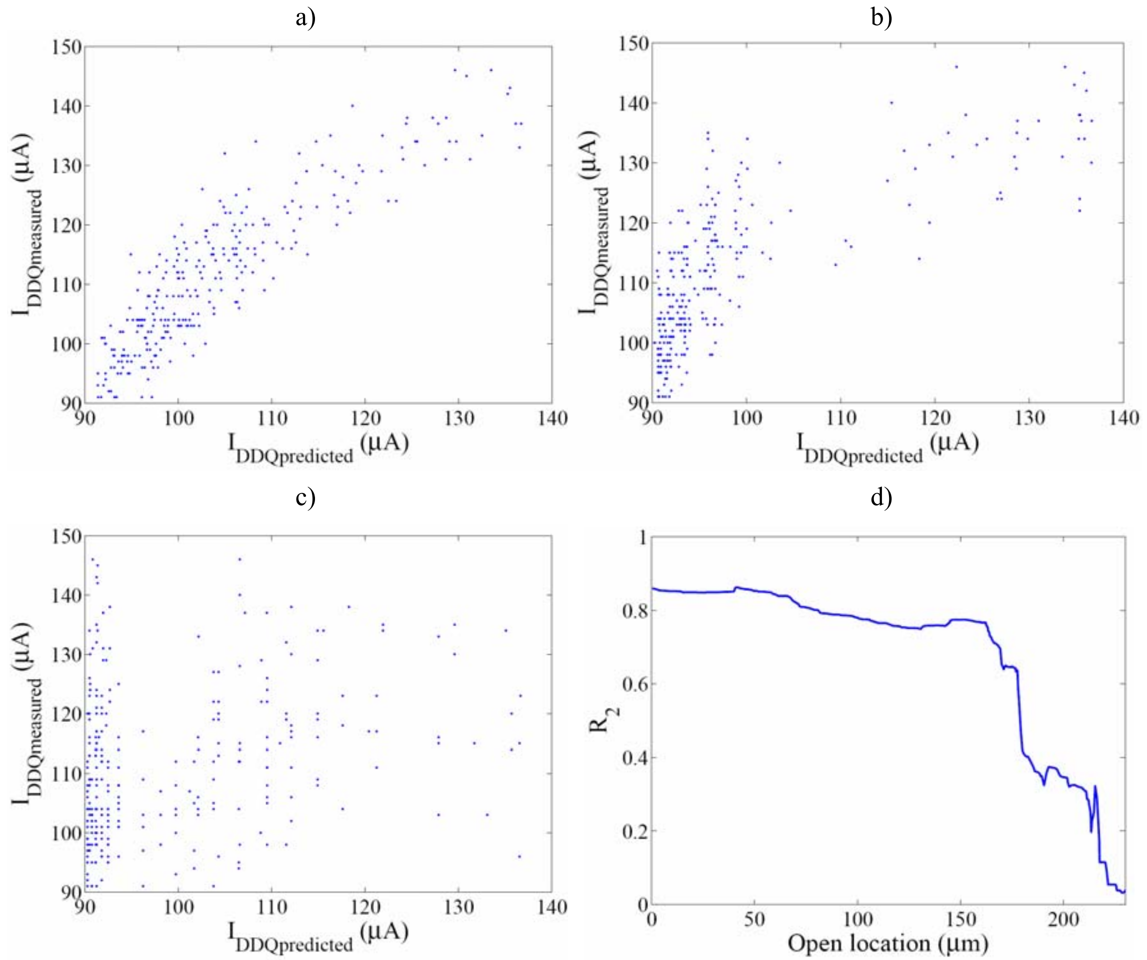

Figure 4.48. I_{DDQ} measured vs. I_{DDQ} predicted a) Segment 1 located in zone A of Figure 4.46b, b) Segment 250 located in zone B c) Segment 400 located in a different arbitrary location d) R^2 for the current measurements depending on the open location

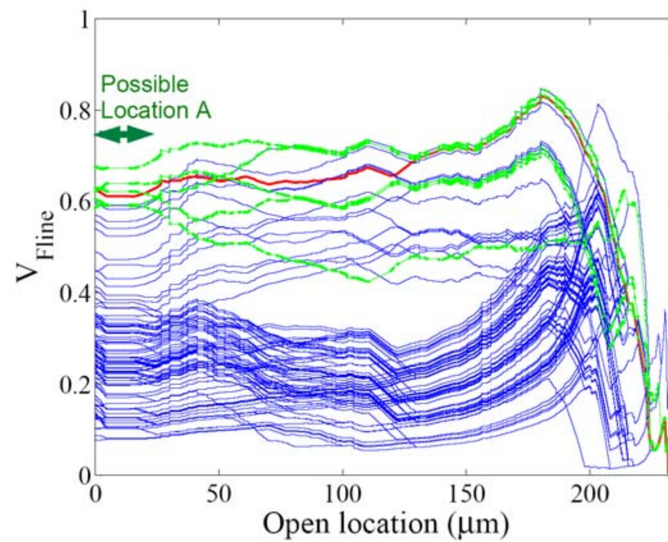

Figure 4.49. Device 82 - Predicted voltage of the failing net including patterns causing high I_{DDQ}.

4.3 TUNNELLING LEAKAGE CURRENT IMPACT ON INTERCONNECT OPENS

The characterization of a full open is determined by the parasitic capacitances to the floating line and the trapped charge. This is true for old and present technologies. However, for future technologies, another factor must be considered, the gate leakage currents. The traditional characterization of the voltage of the floating node by means of the capacitive divider determines the initial state of the node. However, the impact of the gate leakage currents in nanometer technologies introduces a transient response on the floating net until it arrives to the steady state, determined by the topology of the downstream gate(s) and by technology parameters [183]. For a 0.18 µm technology, this transient response is reported to be in the order of magnitude of seconds. However, the continuous reduction of the oxide thickness results in a increment of the gate tunnelling leakage currents, accelerating some orders of magnitude the transient evolution of the floating net for present and future technologies. This fact can become crucial for the behaviour of interconnect full open defects, especially for the ones located at the end of the line with low impact of parasitic coupling capacitances from neighbouring structures.

4.3.1 DIRECT TUNNELLING GATE LEAKAGE CURRENT

The shrinking of feature size in present technologies has led to an important change in the leakage components of CMOS transistors. There are several short channel effects such as drain induced barrier lowering (DIBL) and large threshold voltage roll-off that increment the relationship between the transistor off-state current (I_{OFF}) versus the transistor on-state current (I_{ON}) consumptions [184]. In order to overcome these trends, the ITRS (International Technology Roadmap for Semiconductors) [174] predicts the need of ultrathin gate oxides to maintain the high performance for future CMOS circuits. However, such devices will present a higher gate leakage current (I_g) through the gate oxide due to direct tunnelling mechanisms. This gate leakage current is expected to become the major component of the static power consumption of a thin-oxide nanometer CMOS transistor. In defective circuits, this phenomenon may have also an important impact on the resulting behaviour. In order to analyze the impact of the tunnelling gate leakage current in MOS transistors, in Figure 4.50a [185] it is

illustrated the $Si/SiO_2/Si$ structure used in the implementation of a gate terminal. There are three main direct tunnelling leakage components in the structure; (a) the electron conduction-band tunnelling (*ECB*), (b) the electron valence-band tunnelling (*EVB*), and (c) the hole valence-band tunnelling (*HVB*). Each mechanism has an impact degree depending on the region of operation of the nMOS or pMOS transistor. For each one of the mechanisms, the density of the leakage current can be modelled according to (4.16) [186]:

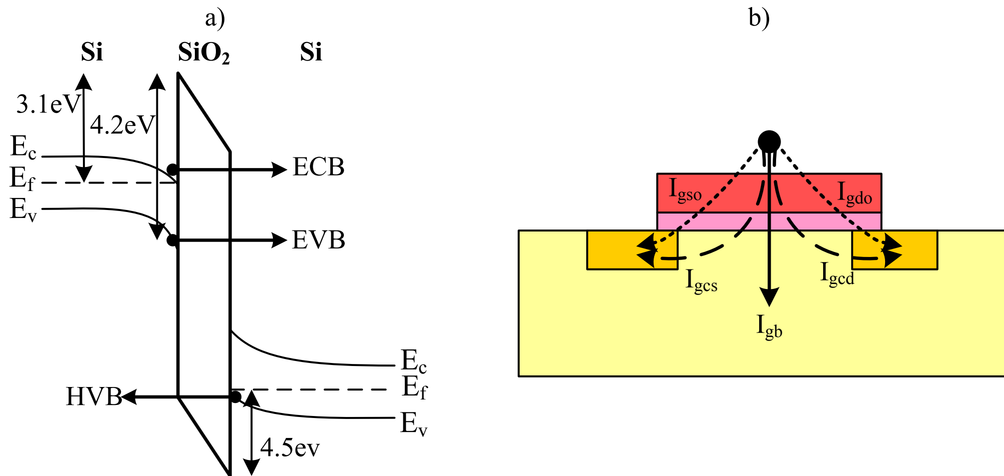

Figure 4.50. Tunnelling current components a) $Si/SiO_2/Si$ structure [185] b) Flowing paths [187] .

$$J_n = AE_{ox}^2 \cdot \exp\left\{ \frac{-B\left[1-\left(1-\left(V_{ox}/\phi_{ox}\right)\right)^{3/2}\right]}{E_{ox}} \right\} \tag{4.16}$$

where constants *A* and *B* are defined as:

$$A = \frac{q^3}{16\pi^2 \hbar \phi_{ox}} \tag{4.17}$$

and

$$B = \frac{4\sqrt{2m^*}\phi_{ox}^{3/2}}{3\hbar q} \tag{4.18}$$

being V_{ox} the voltage drop across the oxide, $E_{ox} = V_{ox}/T_{ox}$ the electric field across the oxide, T_{ox} the thickness of the oxide , q the charge of a free electron, $\hbar = h/2\pi$, φ_{ox} the tunnelling barrier height (3.1 eV for nMOS and 4.5 eV for pMOS structures) and m^* the effective (carrier) mass of an electron ($0.4m_o$) or a hole ($0.32m_o$), where m_o is the free electron mass. According to the difference in the barrier height between *HVB* (4.5eV) and *ECB* (3.1eV), the leakage gate current in pMOS transistors can be between one and

two orders of magnitude lower than in nMOS transistors of the same size, for the same technology.

Although there are three main components contributing to the direct tunnelling gate currents, only two of them must be taken into account due to their magnitude [188]. Indeed, in the case of OFF state or channel inversion, only electron tunnelling from the conduction band (*ECB*) mainly contributes to the gate leakage of nMOS transistors. Conversely, hole tunnelling from the valence band (*HVB*) contributes to the gate leakage of pMOS transistors. The electron tunnelling from the valence band (*EVB*) generates the substrate current in both nMOS and pMOS devices. However, it is more than ten times smaller than the rest and, for this reason, it can be neglected. Another issue to consider is the flowing path of the leakage gate current. For this purpose, Figure 4.50b illustrates the different components of I_g: I_{gb} is the gate-to-substrate leakage current; I_{gso} and I_{gdo} are the parasitic leakage currents through gate-to-source/drain extension overlap regions and I_{gc} is the gate-to-inverted channel tunnelling current. Part of I_{gc} is collected by the source (I_{gcs}) while the rest goes to the drain (I_{gcd}). This I_{gc} partition into I_{gcs} and I_{gcd} is modelled according to the following expression [187]:

$$I_{gc} = \frac{J_{g0} WL\left(1 - e^{-B^* k' L}\right)}{B^* kL} \tag{4.19}$$

where J_{g0} is the gate tunnelling current density with $V_{DS} = 0$ (modelled by (4.16)), B^* is followed by:

$$B^* = B\frac{T_{ox}}{V_{GS}} \tag{4.20}$$

and k' is a parameter that accounts for the influence of V_{DS} in the partition of the gate-to-inverted channel leakage current, whose expression is:

$$k' = \left(V_{GS} - V_{TH} - \frac{V_{DS}}{2}\right)\frac{V_{DS}}{\left(V_{GS} - V_{TH}\right)L} \tag{4.21}$$

4.3.2 FLOATING GATE WITH LEAKAGE CURRENT

The analysis of the effect of the leakage gate current on a single CMOS gate with a full open is considered in this subsection. For that purpose, the impact on a defect-free inverter is first assumed, as shown in Figure 4.51. Depending on the *ON* or *OFF* state of the transistors, the direct tunnelling components are depicted in Figure 4.51a and Figure

4.51b. Note that their magnitude can be derived from equations (4.16) and (4.19), giving place to higher leakage currents for nMOS transistors than for pMOS transistors. The gate-to-channel current of the pMOS transistors is almost negligible compared to the rest of leakage components. In the case that the global input line of the inverter has a full open, the gate node of the two transistors become floating. Under this circumstance, the voltages at the input and at the output of the inverter have probably intermediate values not longer belonging to the logic range. Figure 4.52 illustrates this situation, where the intermediate input voltage creates channel in both nMOS and pMOS transistors. Otherwise, the gate-to-channel components would not be present since they only appear for an inverted created channel. Notice that the leakage current components and the voltage difference between the terminals of the transistors have an exponential dependence and, thus, may vary within a wide range of values. Nevertheless, all the components are depicted in Figure 4.52.

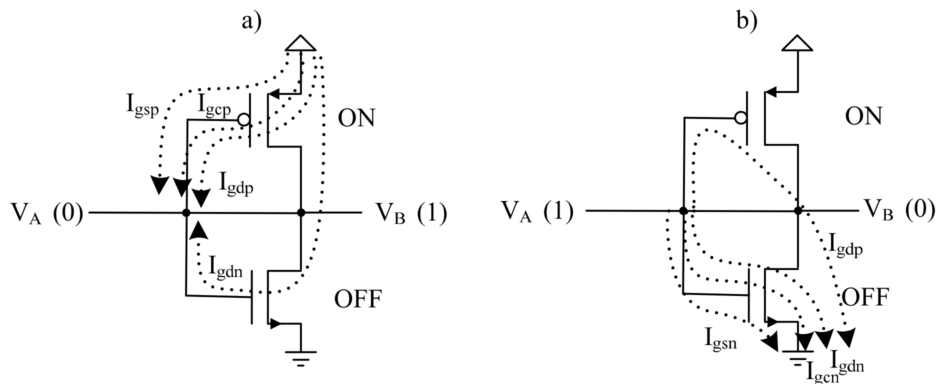

Figure 4.51. Direct tunnelling current components for a defect-free inverter a) $V_A = 0$ b) $V_A = 1$.

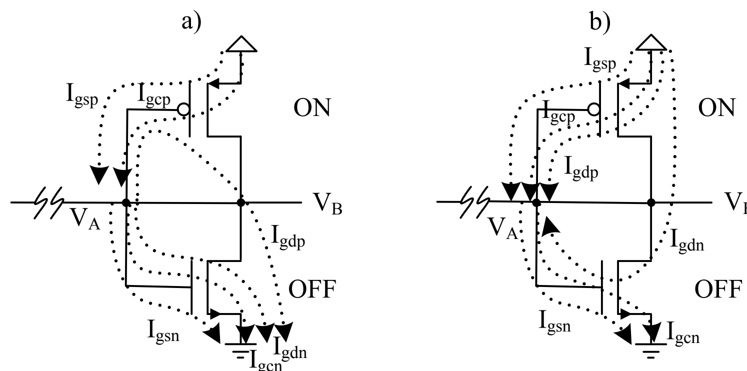

Figure 4.52. Direct tunnelling current components for a defective inverter a) $V_A > V_B$ b) $V_A < V_B$.

4.3.2.1 DYNAMIC ANALYSIS

In order to characterise the defective behaviour of a CMOS gate affected by an open defect at one of its input nodes, suppose an inverter with its input node disconnected from the driver. On the initial state, the capacitive divider created by all

the parasitic capacitances to the floating node and the initial charge (trapped plus injected) determine the voltage value of the floating net. In old technologies, this is the steady state of the floating net till another test pattern is applied and the capacitive divider is modified. However, for nanometer technologies, the floating node is not electrically isolated from the rest of the circuit due to the leakage currents flowing through the gate terminals of the transistor pair. Therefore, once the initial state is determined, the tunnelling leakage currents cause the floating node to evolve from its initial state to a different final state. This final voltage is characterised by the null current flowing into and out of the floating node. When a new pattern is applied, this process is repeated. SPICE simulations using the 90 nm PTM (Predictive Technology Model) have been performed to observe this behaviour [189]. The transistors making up the inverter have the minimum lengths and widths of the technology with $L_n = L_p$ and $W_p = 2W_n$. Figure 4.53 shows the dynamic evolution of the floating node (V_A) due to the tunnelling leakage currents and the response of the inverter (V_B) for the two extreme initial voltages at the input node V_{A0} (0 and V_{DD}). A parasitic capacitance of 2 fF has been assumed at the floating net.

As it is observed, the final state of the defective node does not depend on its initial voltage. Note that, once the defective circuit reaches its steady state, the logic response of the defective circuit is determined by the quiescent voltage at the floating net.

The time required by the floating net to reach the steady state depends also on the total capacitance of the net. Table 4.XI shows the time required by the floating net to reach the 99% of the final quiescent voltage depending on the capacitance connected to the floating net. The set of capacitances selected has been derived from the parasitic capacitance created by an interconnecting wire of the length listed in Table 4.XI.

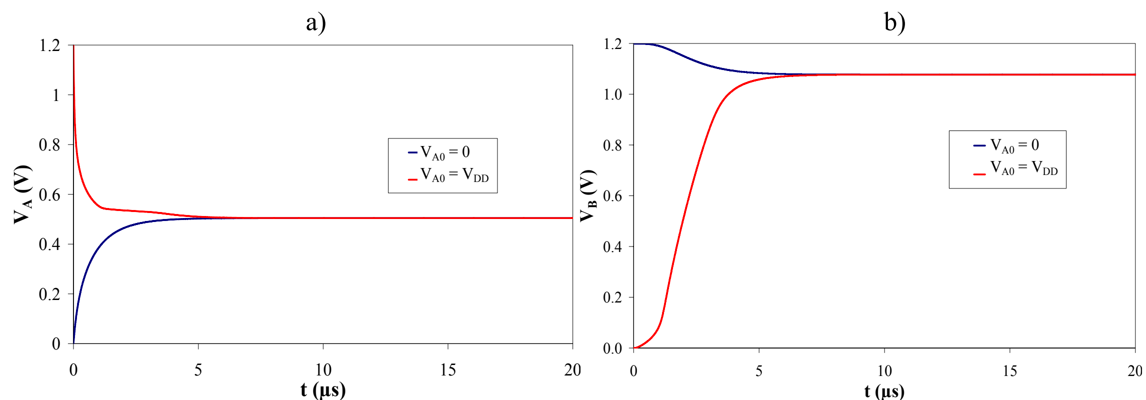

Figure 4.53. Transient response of an inverter with its input floating (90 nm PTM) a) Input b) Output.

TABLE 4.XI
TIME REQUIRED TO REACH THE STEADY STATE

Technology node (nm)	**L_{eq} = 0 µm**	**L_{eq} = 10 µm**	**L_{eq} = 100 µm**	**L_{eq} = 500 µm**	**L_{eq} = 1 mm**
	Time (µs)				
90	22.3	30.1	99.9	410	797
65	10.6	15.8	62.7	271	531
45	7.8	13.4	63.7	287	566

4.3.2.2 STEADY STATE ANALYSIS

According to the leakage current components illustrated in Figure 4.52, the voltage at the input node may evolve from its initial voltage to a resulting final quiescent state due to the existence of the leakage currents flowing into and out of the node. The final state of the floating (input) node is determined by the technology of the circuit (that determines the parameters of (4.16) and (4.19)) and by the topology of the transistors of the gate fed by the floating line. The condition that determines the final steady state is derived from the fact that the addition of all the current components flowing into and out of the floating input node (I_{IN}) must be zero. Figure 4.54a illustrates the resulting current (I_{IN}) at the (input) floating node versus the input and output voltages of the inverter for a particular 0.18 µm technology. The pairs (V_A, V_B) where the resulting current is zero are shown in the figure as a level curve (I_{IN} = 0). They correspond to the possible final states of the defective gate.

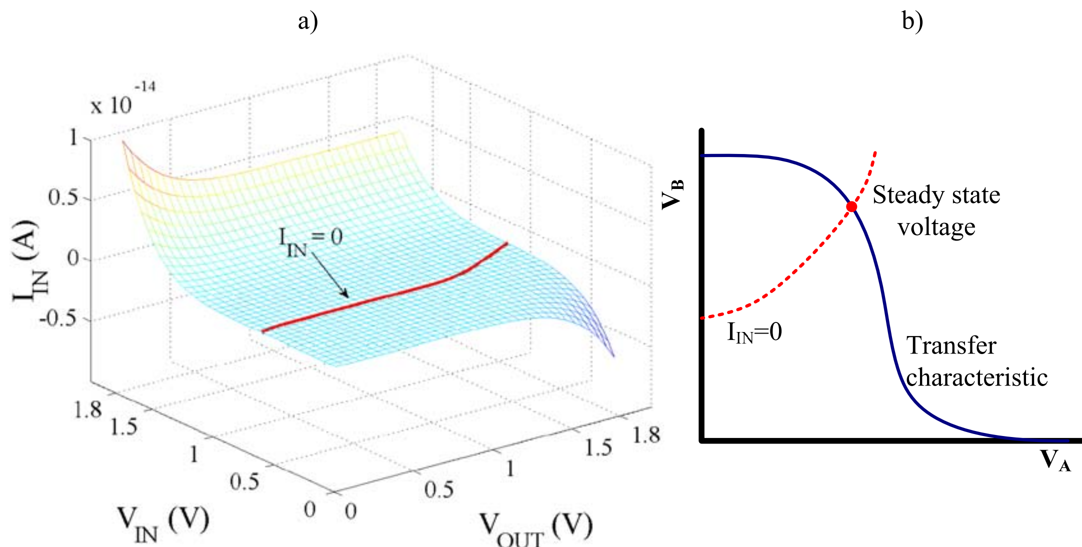

Figure 4.54. I_{in} a) At the floating input of the defective inverter from Figure 4.52 (0.18 µm technology) b) Steady state of the floating line.

Since the values of the tunnelling current is several orders of magnitude lower than the drain current of the transistors, the defect-free static transfer curve of the inverter is assumed not to be modified. With this assumption, the intersection point between the (V_A, V_B) pairs resulting in I_{IN} = 0 and the transfer characteristics of the defect-free inverter determines the final steady state of the defective inverter, as qualitatively illustrated in Figure 4.54b. The transient evolution and time required to reach the final steady state depends on the initial voltage value, the total capacitance to the floating node, the downstream transistors and on the technology used.

4.3.2.3 IMPACT OF THE NEIGHBOURHOOD

Changes on the neighbourhood's state may also influence the behaviour of the floating node. In normal operation of the circuit, at every test cycle, a new test pattern is applied, which sets a different state for the neighbouring lines coupled to the floating node. As a consequence, at every test cycle, the floating line is pulled up or pulled down, depending on the neighbourhood's state. From that point, the floating node starts evolving due to the gate leakage currents until what comes first, the steady state of the floating node or the application of the next pattern, which pulls the floating node to a new initial state. Subsequently, the same process is repeated.

The impact of the neighbouring lines depends, on the one hand, on the the total neighbouring parasitic capacitance to the floating line. On the other hand, the impact also depends on the new neighbourhood's state set by the test pattern applied. The SPICE simulation results showing this impact are illustrated in Figure 4.55. The floating node is assumed to drive an inverter. The total capacitances to the power rails are 2 fF and the neighbouring capacitance (C_N) is considered to have two different values, 1 fF and 10 fF. In Figure 4.55a, the logic state of the neighbour changes every 25 μs. However, the simulation results plotted in Figure 4.55b assume that the neighbour is changing their logic state every 100 ns. Notice how, after a change on the logic value of the neighbouring line, the floating node evolves due to the impact of the gate leakage currents. However, before arriving to the steady state, a transition is generated on the neighbouring line, which causes a pull-up or a pull-down of the floating node depending on the transition type. Observe how in Figure 4.55b, the floating node has less time to evolve than in Figure 4.55a, since the neighbouring line changes its state more frequently.

After the pull-up/down, the floating nodes starts evolving again approaching the steady state voltage until the next transition is generated on the neighbouring line. Finally, the voltage of the floating node keeps centred around the steady state voltage, but alternating between a higher and a lower value due to the pull-up and the pull-down caused by the neighbour. Notice how the impact of the neighbouring capacitance is higher when C_N = 10 fF than when C_N = 1 fF.

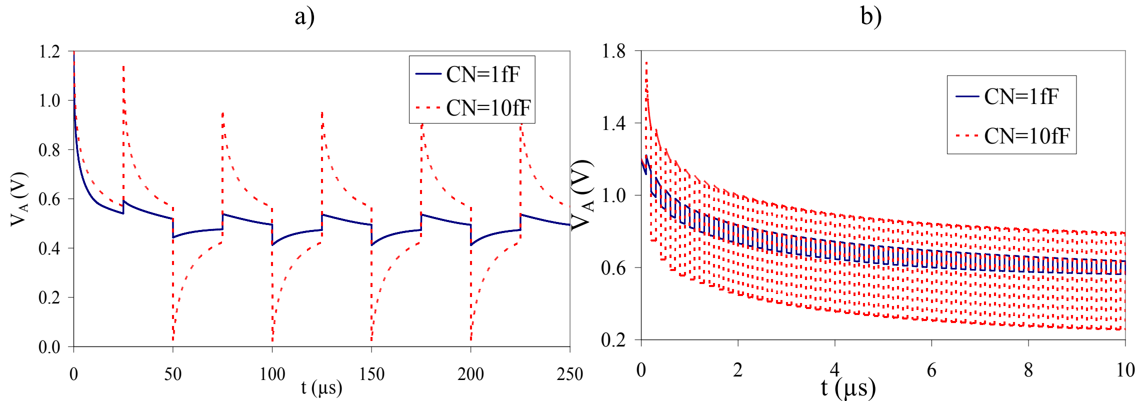

Figure 4.55. Transient response of an inverter with its input floating (90 nm PTM). Coupled neighbour changes its state every a) 25 µs b) 100 ns

4.3.3 SIMULATION RESULTS

Simulations have been carried out in order to analyze the impact of the technology and the topology of the transistors on the behaviour of full open defects under the effect of tunnelling leakage currents [189]. The results of these simulations, based on PTMs, are summarized in this section.

Consider an inverter with a full open defect at its input, as depicted in Figure 4.52. Simulations with different PTM (90 nm, 65 nm and 45 nm) technology nodes have been performed to obtain the transfer function of the inverter and the geometric locus where the sum of all the gate currents of the transistor pair is equal to zero (I_{IN} = 0). These results are illustrated in Figure 4.56a. Notice that in the steady state (intersection between the transfer function of the inverter and the corresponding geometric locus), the floating net is interpreted as logic 0 (SA0 at the input node) regardless of the technology node. Although there are slightly differences in the transfer functions, the geometrical loci (where I_{IN} = 0) are very similar for the three technologies.

The results presented in Figure 4.56a assumed a balanced inverter. However, the impact of unbalanced inverters has also been evaluated. Figure 4.56b reports the results for different transistor width relationships (W_p/W_n) for the 90 nm PTM technology node.

The width of the nMOS transistor (W_n) has been kept constant while the transistor width of the pMOS transistor (W_p) has been modified. As expected, the transfer function shifts to the right as the width of the pMOS transistor increases related to the width of the nMOS transistor. The geometrical locus depends also on the width relationship. For low V_{OUT} values, it is shifted to the right as W_p increases. This behaviour is explained by the fact that the higher the W_p, the higher the tunnelling leakage current supplied by the pMOS transistor. Therefore, for a given V_B value, the voltage of the floating net (V_A) must be higher to compensate this current increase on the pMOS transistor and obtain $I_{IN} = 0$. As shown, W_p/W_n has hardly impact for high V_B values. For that reason, although the final voltage of the floating node is different for every W_p/W_n value, it is always interpreted as logic 0.

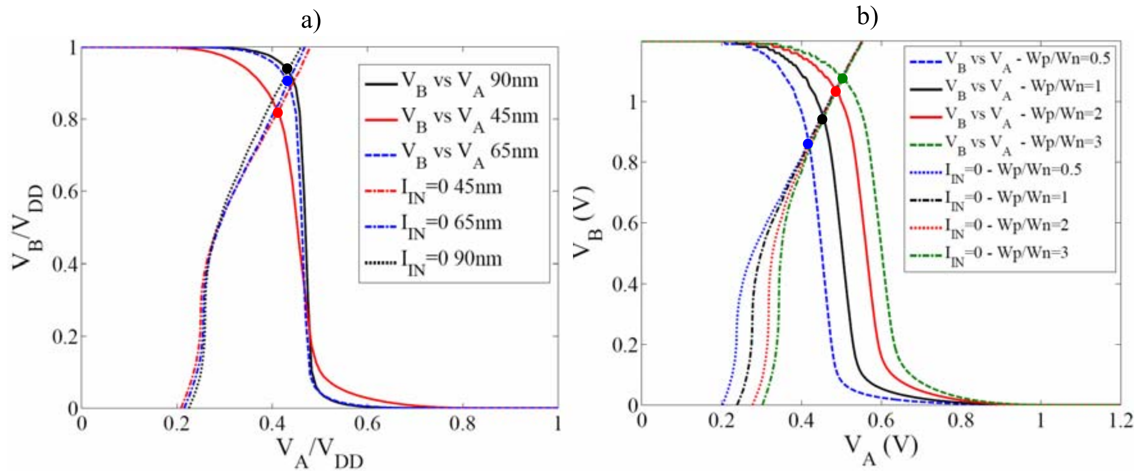

Figure 4.56. Steady state of the floating net driving an inverter a) Technology nodes b) W_p/W_n relationships (90 nm PTM).

The control of the gate oxide thickness is critical to maintain predictable gate currents in nanometer technologies. Based on the ITRS [174], the oxide thickness control has an expected variability of $3\sigma_{Tox} \leq 4\%$. Any deviation from the nominal value ($T_{ox(nom)}$) may modify the floating net voltage on the steady state as derived from the analysis presented so far. In order to evaluate its impact, simulations considering the corner values for oxide thickness ($T_{ox(nom)} \pm 3\sigma_{Tox}$) of the transistor pair driven by the floating net have been carried out. These results are plotted in Figure 4.57. The transfer function of the inverter remains almost unaltered. Nevertheless, the geometrical locus of $I_{IN} = 0$ is modified for low V_B values. When $T_{ox(nMOS)}$ is higher (lower) than $T_{ox(pMOS)}$, the tunnelling leakage current flowing through the nMOS transistor decreases (increases) relatively related to the nominal case. Thereby, this fact is compensated by increasing

(decreasing) the voltage on the floating net. Anyway, the intersection points of the $I_{IN} = 0$ curves with the transfer function of the inverter is shifted just slightly and the voltage of the floating net is always interpreted as low logic value (SA0).

So far, only inverters have been analysed. However, similar results are obtained when considering the rest of basic cells (NAND and NOR gates in Figure 4.58a and Figure 4.58b, respectively). For this technology, once the steady state is reached, the voltage of the floating net is always interpreted as logic 0, as illustrated in the simulation results from Figure 4.58c.

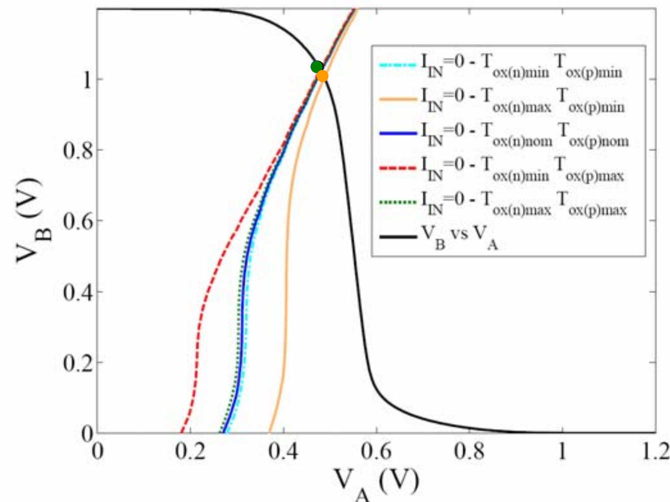

Figure 4.57. Steady state of the floating net driving an inverter with T_{ox} variability (90 nm PTM)

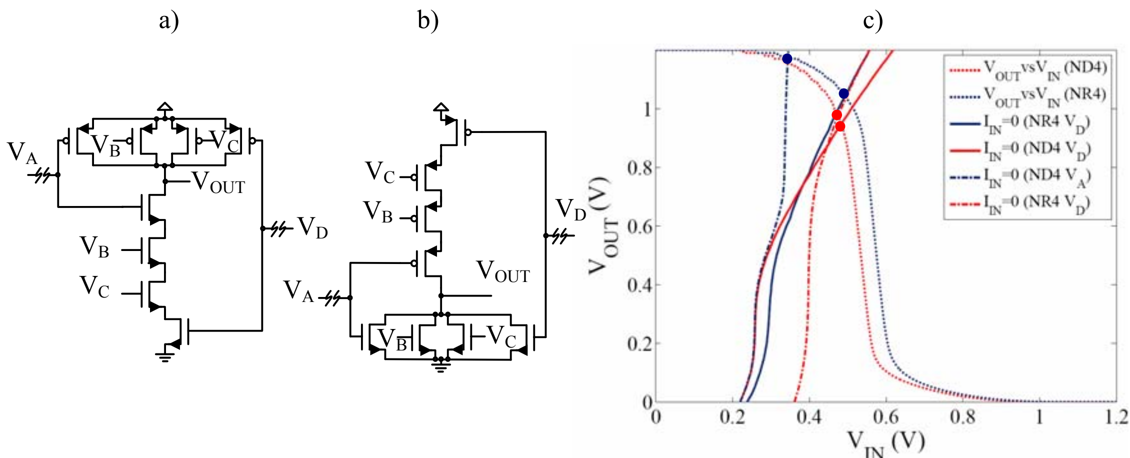

Figure 4.58. a) Full open defects in 4-input NAND gate b) 4-input NOR gate c) Steady state of the floating net for the 4-input NAND and NOR gates (PTM 90 nm technology)

Although the serial connection of transistors in NAND and NOR gates has an impact on the curves of $I_{IN} = 0$, it does not modify the logic interpretation of the floating net. The port affected by the full open has also an influence on the gate leakage currents.

However, it neither modifies the steady state interpretation. Simulations assuming that the full open is at port *A* and at port *D* of the 4-input NAND and NOR gate have been considered. Notice how if the open is at port *A* of the NAND (NOR) gate, the source of the floating nMOS (pMOS) transistor is not connected to V_{GND} (V_{DD}) as in the case of the inverter. However, if the open is located at port *D* of each gate, the drain of the nMOS (pMOS) transistor is not connected to V_{OUT} as it is in the inverter.

4.3.4 EXPERIMENTAL RESULTS

Experimental results for an industrial device of a 0.18 μm technology are presented. It is suspected to contain a full open. The defective device (device 27b) has shown two different logic behaviours. At nominal conditions, the ATE reports a failing logic behaviour, which after using the diagnosis tool, is explained by means of a SA1 at the *B* input port of a multiplexer, as described in Figure 4.59. However, connecting the power supply of the device for a few seconds prior to the test, then the failing logic behaviour obtained on the tester changes. In this case, the diagnosis tool reports the same location of the fault (port *B* of the multiplexer), but now behaving as a SA0. Furthermore, it has been experimentally measured that this device has dependent I_{DDQ} behaviour. Figure 4.60a illustrates the I_{DDQ} test results. Two extra current levels are clearly observed. Nevertheless, although resembling a bridging fault behaviour, there is no bridge explaining both the logic and the current behaviour of this device. Furthermore, peak current values are observed for the first patterns. Nevertheless, waiting for a few seconds before measuring the I_{DDQ} on the ATE for every test pattern causes this peak current value to disappear, as reported in Figure 4.60b. The logic and the transient current behaviour is expected to be explained by a full open defect at port *B* of the multiplexer under the impact of gate tunnelling currents, as presented next.

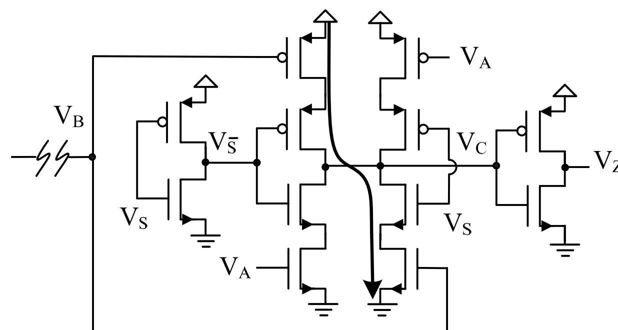

Figure 4.59. Multiplexer containing a full open at port B.

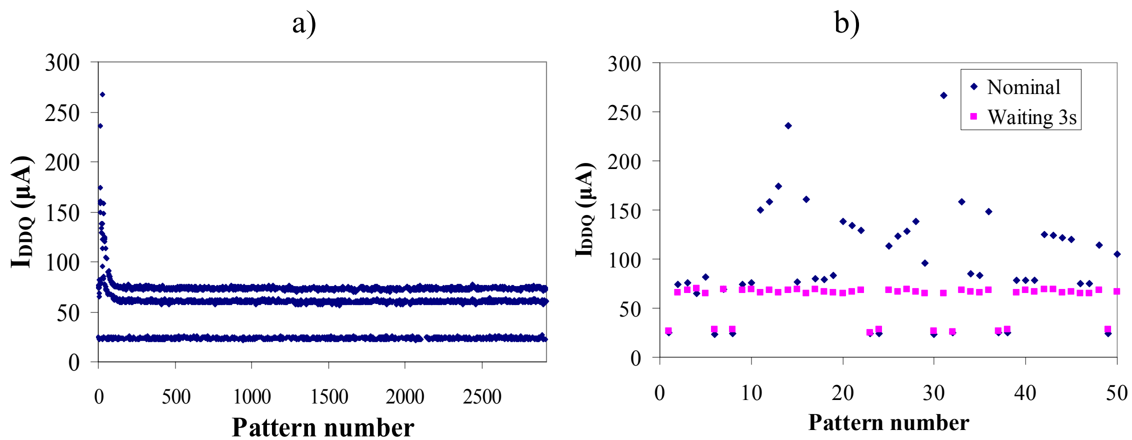

Figure 4.60. I_{DDQ} test a) Nominal conditions b) First 50 patterns, nominal and waiting 3 s.

To analyse the transient current behaviour of this device more accurately, current measurements have been carried out to two specific patterns. After applying the test pattern, I_{DDQ} measurements have been obtained along the time. Figure 4.61a illustrates the time dependent current results for these two patterns. Both patterns activate the defect (port *S* set to logic 1 in Figure 4.59) and set the faulty net to the opposite logic value related to the defect-free case. Notice that both patterns have a very similar I_{DDQ} behaviour over the time. Initially, the current consumption increases and, after reaching a maximum level, starts decreasing. However, the current does not decrease down to the defect-free value, but it remains higher than twice this value. The timing evolution also impacts the logic behaviour of the fault, since it behaves as a SA1 at nominal conditions. However, allowing the faulty net to reach its final steady state, it behaves as a SA0. The experimental behaviour characterized for this device agrees with the prediction derived from the impact of gate tunnelling leakage currents on a floating net. The capacitive divider created by the floating node and all the parasitic capacitances and the trapped charge determines the voltage value of the floating net at the beginning of its transient evolution. This initial voltage is interpreted as logic 1 although the defect free value is logic 0, thus, causing a SA1 faulty behaviour. Furthermore, high current is expected, as shown in the simulation results from Figure 4.61b. However, the gate tunnelling leakage current causes the floating net to evolve to a steady state different from the initial one (SA0). Figure 4.62a illustrates the steady state voltage prediction assuming a full open at port *B* of the multiplexer. Notice how the voltage at the input is

interpreted as logic 0, which is consistent with the SA0 behaviour obtained experimentally.

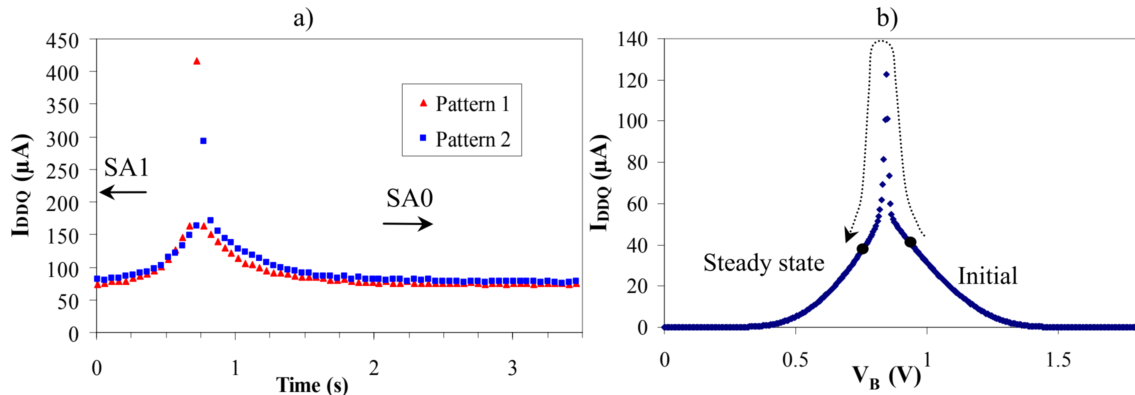

Figure 4.61. Device 27b a) I_{DDQ} time dependent behaviour b) I_{DDQ} vs. V_B.

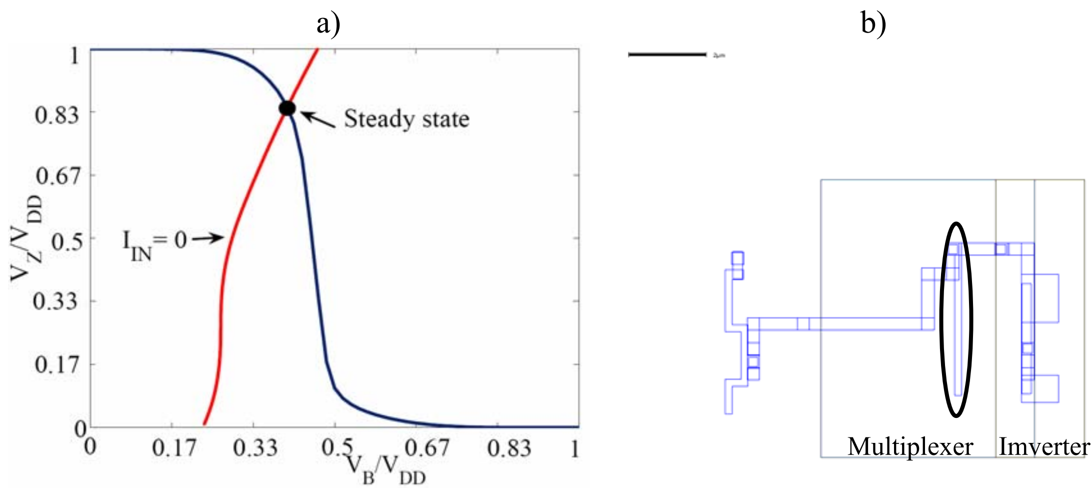

Figure 4.62. Device 27b a) Steady state of the floating B port of the multiplexer b) Layout.

When the faulty net voltage (V_B) ranges between $V_{TH(nMOS)}$ and (V_{DD} - $V_{TH(pMOS)}$), there is current flowing from the power V_{DD} rail through the gate to the ground rail, reaching its maximum approximately at $V_{DD}/2$. Therefore, the behaviour experimentally measured in Figure 4.61a can be explained by the evolution from the *initial* to the *steady state* point of Figure 4.61b, where the SPICE simulation relationship between the voltage of port *B* and the downstream current consumed by the multiplexer is shown. Furthermore, the current peak from Figure 4.61a is consistent with the one obtained by the simulation of the defective circuit. As far as the analysis of the gate leakage current is concerned (Figure 4.62), the voltage at the floating node is interpreted as logic 0, but having an intermediate value. Extrapolating the voltage prediction to the current simulation from Figure 4.61b, it is observed how the steady state voltage lies close to the current peak, giving a non-negligible value around 40 µA. The defect current

(40 µA) plus the leakage current generates approximately 70 µA, which is consistent with the experimental results obtained on the tester (the tail of Figure 4.61a). The impact of the neighbourhood on the initial state is experimentally observed in Figure 4.60a, although it has no impact on the logic interpretation. The two extra current levels are caused by two different initial states of the floating net after the application of a new test pattern. If the layout of the defective multiplexer is considered (see Figure 4.62b), it is noticed how the floating net is expected to be short, mainly comprising polysilicon. No big impact of the neighbours is expected. This is consistent with the fact that in the initial state, after the application of every test pattern, the floating net is always interpreted in the same way (SA1). Furthermore, two extra current levels are observed in Figure 4.60a, although their difference is not high.

From the layout, only three neighbours (polysilicon) may be coupled to the floating line. They are the S port of the multiplexer and two internal nets of the same multiplexer ($\bar{S}$ and C). When the defect is activated, ports S and $\bar{S}$ have always the same logic value (1 and 0, respectively). However, the logic value V_C depends in turn on the logic value of the floating node. Therefore, there are only two possible states for the neighbourhood, which is consistent with the number of extra current levels from Figure 4.60a.

It has been shown how the proposed analysis predicts the final state of a full open defect due to the impact of gate tunnelling leakage currents without the need of analysing the transient behaviour. Figure 4.61a shows that the time required for the device to reach the final steady state is around 2 s. The transient behaviour depends on the initial state, the parasitic capacitances to the floating node, the topology of the downstream gates and the technology used.

4.4 CONCLUSIONS

The experimental results obtained with the fabricated design in a 0.35 µm technology have shown the importance of the parasitic coupling capacitances for the logic interpretation of floating nodes caused by full open defects. Furthermore, the experiments with resistive opens have demonstrated the effect of the history effect and also the impact of the location of the resistive defect on the delay. It has been

demonstrated how the highest delay is not obtained at the beginning of the net if the open is low resistive.

The work developed with the experimental chip has been the starting point for the development of a new methodology to diagnose interconnect full open defects. The FOS methodology divides the interconnect line into different segments based on the topology of the faulty line. This method has been demonstrated to be useful in real devices. Although developed to be applied with logic information, the FOS method has been proved to be useful also with current information.

The effectiveness of the FOS method decreases when the open is located at the end of line and the neighbouring coupling capacitances are very small. In those cases, the impact of gate leakage currents may become of major importance for both test and diagnosis purposes. For present and future technologies, the gate oxide thickness becomes so thin that the gate tunnelling leakage currents impact the behaviour of floating nodes. They cause transient evolutions on the floating line until reaching the steady state, which depends only on the technology and the topology of the downstream gate. Experimental evidence of this fact has been presented for a device suspicious to contain a full open defect at the end of the line. The impact of gate tunnelling current could be also observed on failing nets containing a full open defect at the beginning of the line. However, the parasitic coupling capacitances increases the transient evolutions orders of magnitude related to the same case but with the open located at the end of the line. In future tecnologies, these transient evolutions may become observable even for long interconnect lines.

CHAPTER 5. EXPERIMENTAL RESULTS

This chapter summarizes the experimental results of the different methodologies presented in Chapter 3 and 4, which have been applied to different industrial designs. Two sets of devices belonging to different technologies have been the field of study. On the one hand, a group of *Vector4* devices from a 0.18 μm technology of *NXP Semiconductors* was used to assure the feasibility of the developed methodologies. On the other hand, a group of 90 nm technology devices, also from *NXP Semiconductors,* has been utilised to observe the impact of scalability on the multiple level I_{DDQ} methodology for the diagnosis of bridging faults.

5.1 *VECTOR4* DEVICES

The *Vector4* design is a *NXP Semiconductors* test chip specially designed to speed up the introduction of new IC production processes and monitoring the existing ones. The *Vector4* is representative of normal products to cover all types of problems that might arise during fabrication processes.

The work is focused on diagnosing defects on random logic, which are difficult to analyze because it is hard to pinpoint the specific failing cell. The *Vector4* design is composed of six different cores of random logic. The rest of cores of the *Vector4* are neglected, since they are out of the scope of this thesis.

The selection of the samples studied in this thesis were carried out in San Jose (USA) by members of *NXP Semiconductors* staff. Subsequently, the tests of the devices have been carried out in the *LIDE III* laboratory of the *Electronic Engineering Department* of the *UPC*.

5.1.1 STRESS TESTING

As much information as possible is desired prior to the diagnosis procedure of a faulty device. For that reason, different stress conditions have been considered during the collection of experimental measurements on the tester. It is known that modifying the power supply value during logic test improves the detection of defects. In this way, apart from the nominal V_{DD} value (V_{NOM}), some other logic tests have been carried out with different power supply values. Therefore, the logic test have been repeated using V_{DD} values lower as well as higher than V_{NOM}, as summarized in Table 5.I.

TABLE 5.I
V_{DD} TEST

V_{VLV} (V)	V_{MIN} (V)	V_{NOM} (V)	V_{MAX} (V)
1.2	1.5	1.8	2.0

Speed test is useful when trying to detect defects of resistive nature. In this way, different system clock periods have been considered when carrying out the logic test. Table 5.II summarizes the different values considered during speed test. The nominal period (T_{NOM}) is 100 ns.

TABLE 5.II
SPEED TEST

T_{NOM} (ns)	$1.5T_{NOM}$ (ns)	$2T_{NOM}$ (ns)	$10T_{NOM}$ (ns)
100	150	200	1000

Some defects may change their behaviour with temperature. Furthermore, transistor characteristics are modified with temperature. Therefore, transistors involved by the defect may change their behaviour under different temperature conditions.

A climate chamber has been used to carry out tests at different temperatures. Three different temperatures have been considered, see Table 5.III: the nominal one at room temperature (25 ºC), another at high temperature (85 ºC) and finally, one at low temperature (3 ºC). The climate chamber is able to reach lower temperatures. However, as the air is extracted out of the chamber, there is no humidity control. Therefore, some frost problems may appear for temperatures below 0˚C.

TABLE 5.III
TEMPERATURE TEST

T_{ROOM} (ºC)	T_{COLD} (ºC)	T_{HOT} (ºC)
25	3	85

I_{DDQ} test is also considered. No external monitor is used to measure current consumption. Hence, the resolution of the measurements is determined by the power supply of the tester. In this case, it is 1 μA, which is sufficient for the *Vector4* devices fabricated in 0.18 μm technology.

Given a test condition (V_{DD}, frequency, temperature, etc), the same test has been applied different times in different moments. Therefore, it can be observed if there is repeatability on the behaviour of the faulty devices. It has been observed how some cores reported different number of failing vectors (*non-repeatable*) without following any clear dependency with any of the factors considered during the tests. They reported non-repeatable results, probably related to the Byzantine's problem. Furthermore, another set of cores also showed no dependency with any of the parameters. In these cases, the logic behaviour seemed to be modified if the same test was applied different times consecutively or if prior to the test, the power supply was connected allowing the circuit to evolve until it reached the steady state. These cores are the so called *evolving* cores.

5.1.2 DIAGNOSED CORES CLASSIFICATION

Applying the diagnosis methodologies described in Chapter 3 and 4, thirty-three faulty cores have been diagnosed, as summarized in Figure 5.1a. Twenty-five cores have been reported to contain a bridge, whereas eight cores are reported to contain a full open. Four of these full opens have been diagnosed based on the FOS model whereas the other four have been diagnosed based on the impact of gate leakage currents. All the stress conditions reported in the previous subsection have been applied to these cores during the logic tests. The logic test consists of a set 2920 SA patterns. If the same logic result is always obtained for the same core independently of the test condition, the cores are reported to be *stable*. However, if for one or more test conditions the logic results are different, then the core is reported to be *non-stable*. The classification based on the logic stability for the diagnosed cores is illustrated in Figure 5.1b. Notice that the majority of the bridges are reported to be stable, whereas six out of the eight cores containing a full open are non-stable.

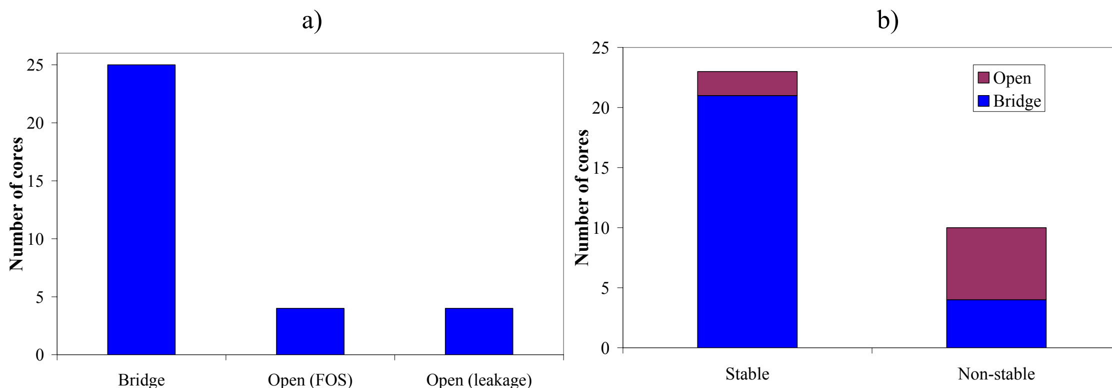

Figure 5.1. Classification of the faulty cores a) Fault type b) Logic stability.

Table 5.IV summarizes the logic dependencies for the non-stable cores. The evolving behaviour is explained by the impact of the gate leakage currents in the presence of a full open defect, as explained in section 4.3. Two opens report non-repeatable results. This is mainly due to intermediate voltages on the floating net causing the Byzantine problem. Furthermore, one open has temperature dependency. This is also probably due to intermediate voltages on the floating node. The logic thresholds of the downstream gates are modified with temperature so that the logic interpretation of intermediate voltages may be different when modifying the temperature. Related to bridges, two of them report logic dependency with the power

supply voltage, whereas the other two report dependencies with more than one factor (*combined*).

TABLE 5.IV
NON-STABLE CORES

Device	Core	Fault	Dependency
46	3	Open (Leakage)	Temperature
82	4	Open (FOS)	Non-repeatable
88	2	Bridge	Combined
92	6	Bridge	V_{DD}
148	5	Open (Leakage)	Evolving
9b	6	Bridge	V_{DD}
14b	3	Bridge	Combined
26b	5	Open (Leakage)	Evolving
27b	2	Open (Leakage)	Evolving
39b	3	Open (FOS)	Non-repeatable

The next subsections present in more detailed the diagnosis results for every different methodology: Diagnosis of bridges based on the multiple level I_{DDQ} methodology, diagnosis of interconnect full open defects based on the FOS model and diagnosis of interconnect full open defects based on the impact of gate leakage currents.

5.1.3 DIAGNOSIS OF BRIDGING DEFECTS

The methodology described in section 3.2 has been applied to the devices suspected to contain a bridging defect. For that purpose, an I_{DDQ} test has been applied to the faulty cores using the same SA patterns considered during the logic test. The I_{DDQ} values measured on the tester for every pattern is stored so that this information is subsequently used for the proper diagnosis of the bridging fault. Furthermore, current measurements at both V_{NOM} (1.8 V) and V_{VLV} (1.2 V) are carried out to observe the impact of the downstream current. In the presence of downstream current, the diagnosis procedure is carried out with both set of measurements so that a comparison between both cases can be made.

A summary of the results for the defective cores, which were suspicious to contain a bridge, is shown in Table 5.V and 5.VI. The first three columns give the information about the faulty core. The next six columns summarises the results reported by the

TABLE 5.V
SUMMARY OF BRIDGING DEFECTS DIAGNOSIS RESULTS: VECTOR4

Device information			Diagnosis tool (Faloc)						Multiple level I_{DDQ} based diagnosis						
											N = 2920		N = 50		
#	Core	Stable	FS1	Net 1	Net 2	M (%)	P (%)	Equiv	Net A	Net B	β_1	R^2	β_1	R^2	I_d
10	3	Yes	Bridge	n_2882	n_2091	100	100	No	n_2882	n_2091	1.198	0.995	1.195	0.997	No
11	3	Yes	SA	n_26512	--	100	100	Yes	n_26512	V_{GND}	1.090	0.999	1.085	0.999	No
14	3	Yes	Bridge	n_389	n_1601	100	100	No	n_389	n_1601	1.198 (1.184)	0.981 (0.994)	1.234(1.216)	0.980 (0.996)	Yes
35	2	Yes	SA	n_132612	--	100	100	Yes	n_132612	V_{DD}	1.060	1.000	1.061	0.999	No
38	3	Yes	Failing net	n_553	--	100	52	Yes	n_553	tq[6]	1.124	0.999	1.125	0.999	No
47	3	Yes	SA/Bridge	n_2574	--	100	100	Yes	n_2574	V_{DD}	1.191	0.999	1.175	0.999	No
53	3	Yes	Failing branch	n_31130	--	100	100	Yes	n_31021	Internal	0.927	0.980	0.901	0.979	No
60	2	Yes	SA	ASI_Q_7_	--	100	100	Yes	n_1455	Internal	1.027	0.995	1.036	0.992	No
68	6	Yes	SA/Bridge	n_21471	--	100	100	Yes	n_21471	V_{DD}	1.008	0.999	1.007	0.999	No
76	2	Yes	Bridge	XD_15_	n_9630	100	100	No	XD_15_	n_9630	0.9383	0.999	0.928	0.949	No
78	2	Yes	Failing net	n_171560	--	100	100	Yes	n_171560	n_17536	1.085 (1.106)	0.980 (0.999)	1.091 (1.133)	0.968 (0.999)	Yes
80	5	Yes	Bridge	n_21245	n_20695	100	100	No	n_21245	n_20695	1.069	0.989	1.097	0.954	No
88	2	No	Failing net	n_1688	--	99	96	No	n_891	Internal	4.080 (3.512)	0.910 (0.972)	3.901 (3.426)	0.842 (0.963)	Yes

TABLE 5.VI
SUMMARY OF BRIDGING DEFECTS DIAGNOSIS RESULTS (SECOND PART): VECTOR4

Device information			Diagnosis tool (Faloc)						Multiple level I_{DDQ} based diagnosis						
											N = 2920		N = 50		
#	Core	Stable	FS1	Net 1	Net 2	M (%)	P (%)	Equiv	Net A	Net B	β_1	R^2	β_1	R^2	I_d
92	6	No	Failing branch	n_6156	--	100	100	No	n_6156	n_16865	1.400 (1.062)	0.848 (0.998)	1.387 (1.053)	0.842 (0.997)	Yes
101	5	Yes	Bridge	n_2112	n_2113	100	100	No	n_2112	n_2113	1.383 (1.163)	0.937 (0.999)	1.375 (1.165)	0.81 (0.999)	Yes
112	3	Yes	SA	n_26512	--	100	100	Yes	n_26512	V_{GND}	1.093	0.999	1.094	0.999	No
129	3	Yes	SA	n_26512	--	100	100	Yes	n_26512	V_{GND}	1.149	0.999	1.144	0.999	No
131	3	Yes	SA	n_2918	--	100	100	Yes	n_2918	V_{GND}	1.200	0.999	1.205	0.999	No
133	3	Yes	Failing net	n_553	--	100	52	Yes	n_553	tq[6]	1.104	0.998	1.108	0.997	No
144	2	Yes	SA/Bridge	n_22488	--	100	100	Yes	n_22488	V_{DD}	1.088	0.999	1.090	0.999	No
6b	5	Yes	2 members	i_237210	n_6222	--	--	No	n_6315 & n_6222	V_{GND}	1.196	0.999	1.200	0.999	No
9b	6	No	Bridge	n_25307	n_25311	100	100	No	n_25307	n_25311	2.131 (1.556)	0.942 (0.965)	2.147 (1.546)	0.940 (0.969)	Yes
14b	3	No	SA/Bridge	n_711	--	100	100	Yes	n_711	V_{DD}	1.224 (1.185)	0.937 (0.949)	1.256 (1.098)	0.880 (0.901)	Yes
21b	3	Yes	SA	n_5076	--	100	100	No	n_5076	V_{DD}	1.070 (1.032)	0.999 (0.999)	1.092 (1.050)	0.999 (0.999)	Yes
36b	1	Yes	Bridge	n_1438	DSP.ZI_3	94	100	No	n_1438	DSP.ZI_3	1.169	0.999	1.171	0.999	No

diagnosis tool (*Faloc*) in the first stage of the diagnosis process, namely: the class of fault reported with the highest quality measurements (*Fail Scenario 1*), the nets involving this fault (*Net 1* and *Net 2*), the Matching (*M*) and Prediction (*P*) quality values and the existence of some other equivalent faults reported with the same quality values (*Equiv*). The rest of columns refers to the results obtained related to the multiple level I_{DDQ} based diagnosis. The two first columns (*Net A* and *Net B*) report the nets suspected to belong to the bridging fault. The next two columns show the value of the regression coefficient (β_1) and the coefficient of determination (R^2) for the bridge connecting *Net A* and *Net B* using the whole set of I_{DDQ} measurements ($N = 2920$). The following two columns report the same results, but considering only the first 50 I_{DDQ} measurements ($N = 50$). All these results are calculated using I_{DDQ} values at V_{NOM}. Finally, in the last column the presence of downstream current (I_d) is described. If so, the value of β_1 and R^2 at V_{VLV} is reported between brackets in the previous columns.

As reported previously, the application of the multiple level I_{DDQ} based diagnosis was successful for 25 cores. Most of the diagnosed bridges belong to cores which are classified as stable cores. However, there are four cores which are non-stable. The majority of bridges are expected to cause stable logic behaviour. However, if the bridged networks have similar strengths, the Byzantine behaviour may arise and the logic threshold of the downstream gates may determine the logic interpretation of the bridged nodes, causing non-stable logic behaviour. For instance, among the four faulty cores reporting a bridging fault with non-stable logic behaviour, three of them are between transistor networks with similar strength, as illustrated in Figure 5.2a, b and d. This fact is specially observed in Device 88. The output of the 2-input NOR gate has fan-out, so that there are several downstream currents components present even at low power supply voltages (although they have been minimized). That is why for this core, β_1 has higher values than the unity (see Table 5.V). Device 92 has already been presented in 3.2.6. The third faulty core (Figure 5.2c) is explained by means of a bridge between the output of a 2-input NOR gate and V_{DD}. It is not expected such a non-stable logic behaviour from this class of bridge. Every current level has spread values not completely explained by downstream current. Finally, the fourth bridge (Figure 5.2d) connects the outputs of two 4-input NAND gates. The bridged networks have then similar strengths, generating intermediate voltages explaining the non-stable behaviour.

Summarizing the results from Table 5.IV and Table 5.V, it can be concluded that there are eight bridges causing downstream contributions among the twenty-five diagnosed bridges. Notice how for these eight cores, the use of I_{DDQ} measurements at low V_{DD} values improves the diagnosis results. Depending on the importance and the frequency of the downstream contribution, the improvements are more marked for some cores than for others. The proportion eight out of twenty-five bridges causing downstream currents can be considered a low percentage. However, if the typology of the bridge is considered, the importance of the downstream current increases. The classification of the diagnosed bridges is illustrated in Figure 5.3. Twelve out of the twenty-five bridges involve power rails, that is, either to power supply or ground, six bridges are between an input and the output of the same gate, five bridges are between two nets on the interconnect and finally, two are internal bridges inside a cell. Discarding the bridges to power rails, then seven out of thirteen bridges present downstream current components, which is quite significant when diagnosing bridging faults between two signals. For every specific core, more information can be found in Annex A.

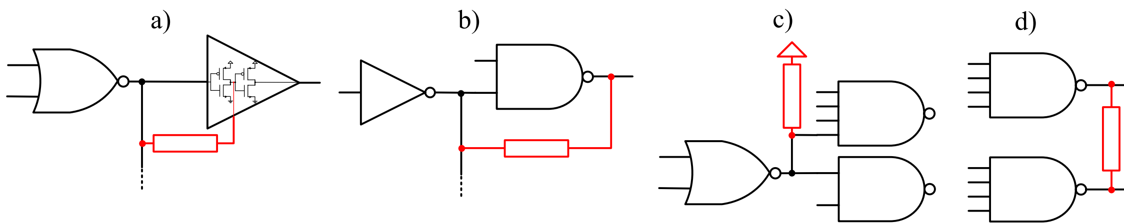

Figure 5.2. Bridging faults with non-stable logic behaviour. Device a) 88 b) 92 c) 9b d) 14b.

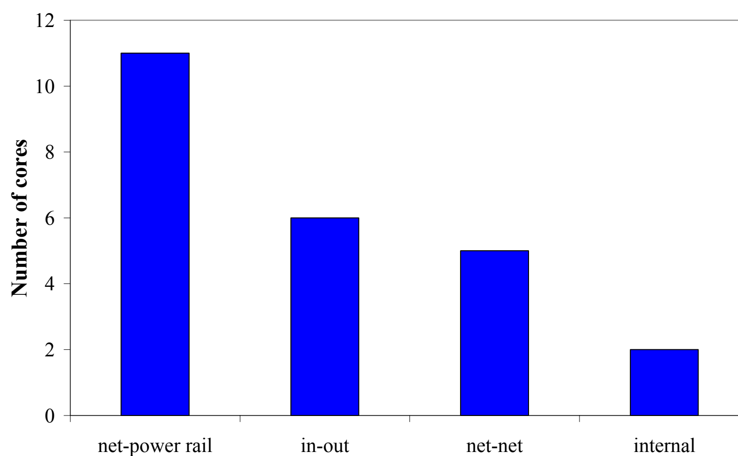

Figure 5.3. Bridging faults classification.

5.1.3.1 FAILURE ANALYSIS

The failure analysis has been carried out for three of the bridges to corroborate the feasibility of the method. The first one is Device 10. A bridge between one of the inputs and the output of an *AO3A* gate was found in this case, as described in Figure 5.4a. The layout of the two nets is illustrated in Figure 5.4b. Based on this information, the most probable location for the bridge is in Metal2, limited by the red square described in the layout. A picture of the device for this suspicious zone is shown in Figure 5.4a, where the defective Metal 2 is observed. Cross-sections have been carried out in the suspicious zone. The three FIB (Focussed Ion Beam) cross-sections described in Figure 5.5a correspond to the photographs illustrated in Figure 5.5b, c and d, respectively. Notice the partial patterning of Metal 2, which connects the two nets, corroborating the bridge predicted by the methodology.

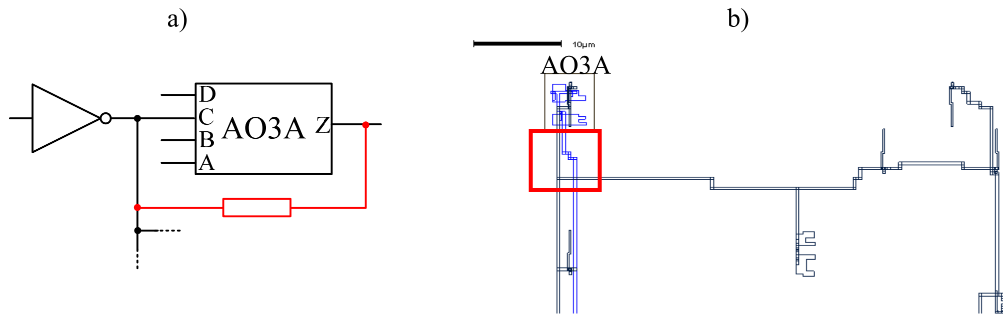

Figure 5.4. Device 10 a) Gate level b) Layout.

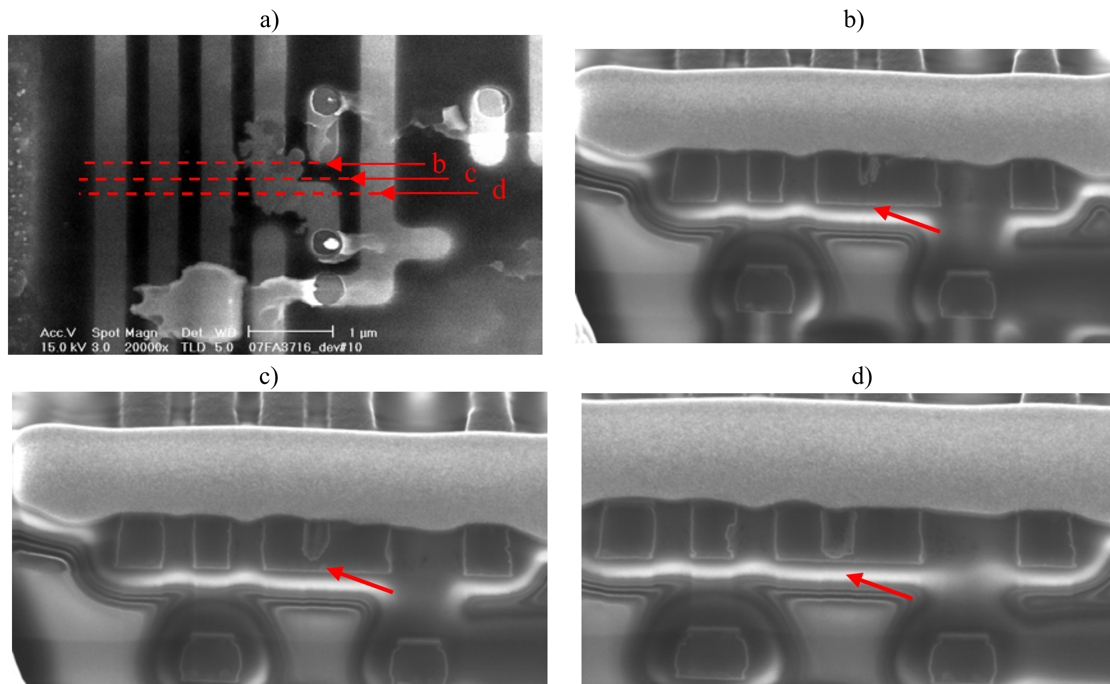

Figure 5.5. Device 10 a) Failure Analysis b) Cross-section a c) Cross-section b d) Cross-section c. Pictures obtained in the NXP FA laboratory.

The second case is Device 36b. The diagnosis process predicted a bridge between the outputs of a buffer and a complex gate, as reported in Figure 5.6a. The probable location of the bridge is in Metal 4, as denoted by the red square in Figure 5.6b. The picture corresponding to the probable location is illustrated in Figure 5.7. Observe the spot connecting the two nets.

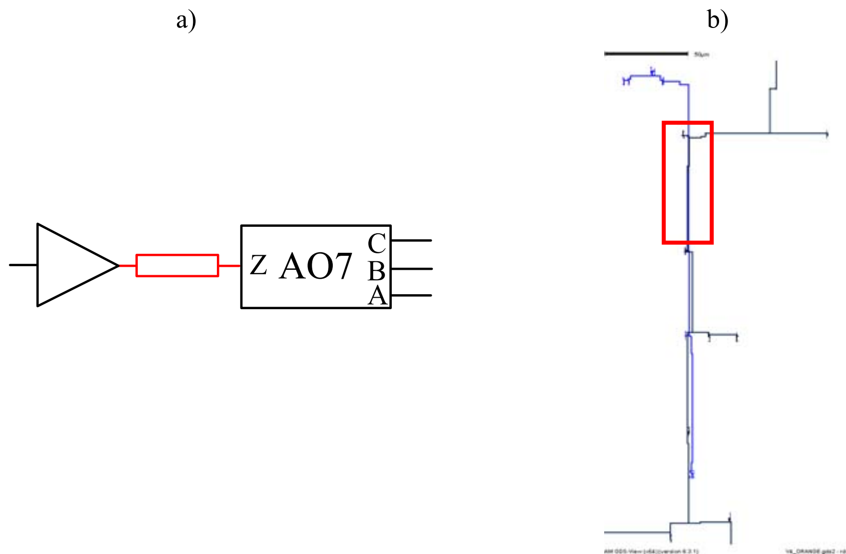

Figure 5.6. Device 36b a) Gate level b) Layout.

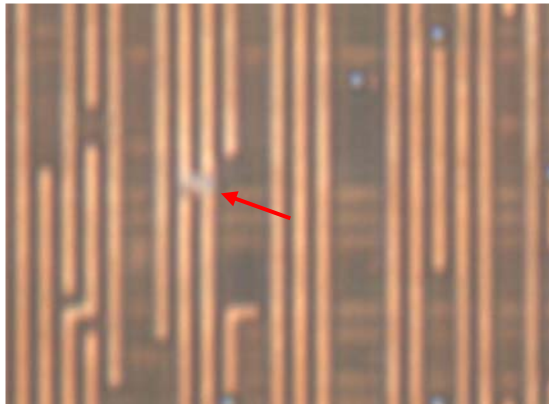

Figure 5.7. Device 36b – Failure analysis.

Finally, the third case is Device 76. The diagnosis methodology reported a bridge involving three nets, as described in Figure 5.8a. The probable location of the bridge is in Metal 4, as denoted by the red square in Figure 5.8b. The pictures corresponding to the suspicious zone are illustrated in Figure 5.9a and b. Notice how in Metal 5 (Figure 5.9a) the defect is already visible. Nevertheless, the spot connecting the three nets is more evident viewing the Metal 4 layer (Figure 5.9b).

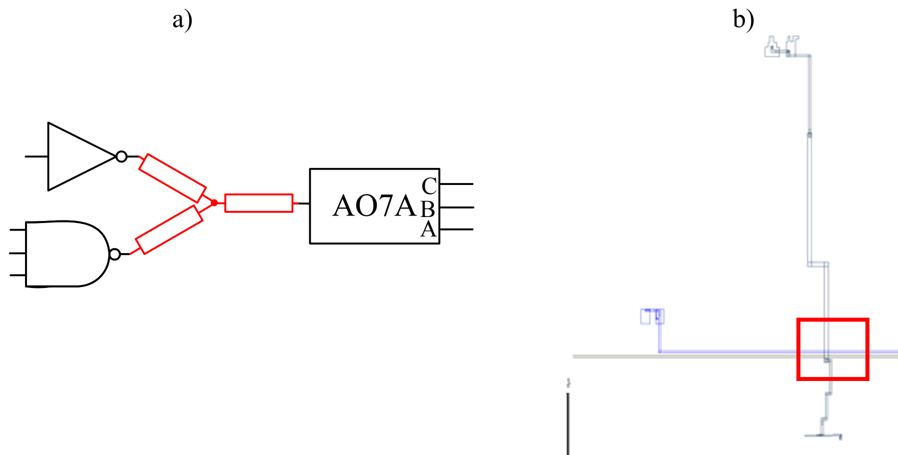

Figure 5.8. Device 76. a) Gate level b) Layout.

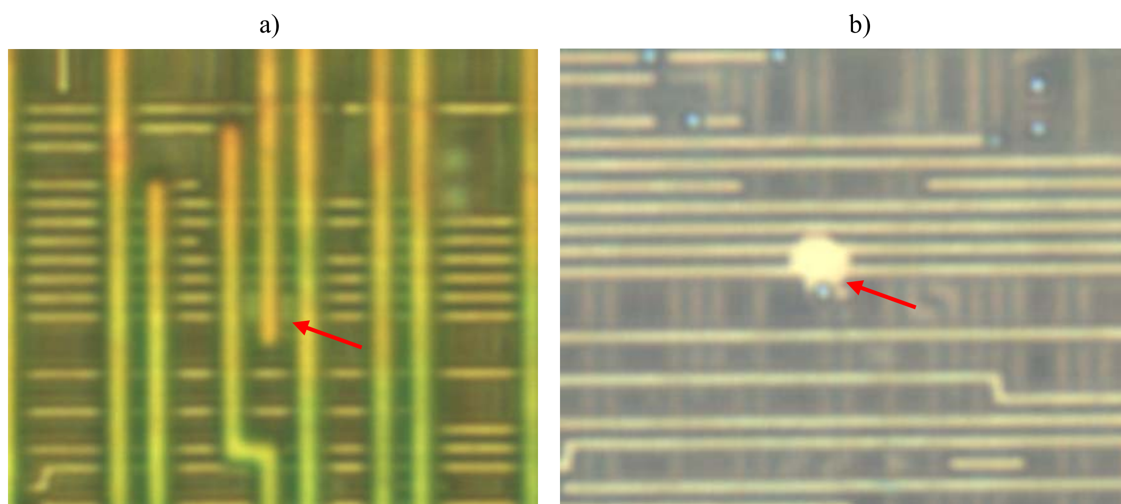

Figure 5.9. Device 76 - Failure analysis a) Metal 5 b) Metal 4. Pictures obtained in the NXP FA laboratory

5.1.4 DIAGNOSIS OF FULL OPEN DEFECTS BASED ON THE FOS MODEL

This section summarizes the diagnosis results based on the FOS methodology presented previously in section 4.2. One experimental case (Device 82) was already shown in 4.2.7, where an interconnect full open defect in a line driving a 4-input OR gate was diagnosed at the beginning of the net. Three more full open defects have been diagnosed by the present method, which are presented next.

5.1.4.1 DEVICE 87

The failing core 2 of Device 87 is a stable core, reporting 353 failing vectors. When carrying out the logic diagnosis with the help of the diagnosis tool, the most probable faults explaining this behaviour are four different fail scenarios (FSs) reported with M = 100% and P < 100%. All of them are failing nets, pinpointing to different locations of the circuit, but logically related. The first scenario, which is reported with

the highest P = 68% is a failing net (n_613) at the input port *A* of an *AO4* complex gate, which is driven in turn by an *AO3* gate, as described in Figure 5.10a. The *AO3* gate has fan-out, as observed in Figure 5.10b. However, in the first FS, the diagnosis tool reported that only the input port of the *AO4* gate was failing. Therefore, the interconnect full open defect should be located along the branch which is driving the *AO4* gate, denoted in light blue in the layout description of the net illustrated in Figure 5.10b.

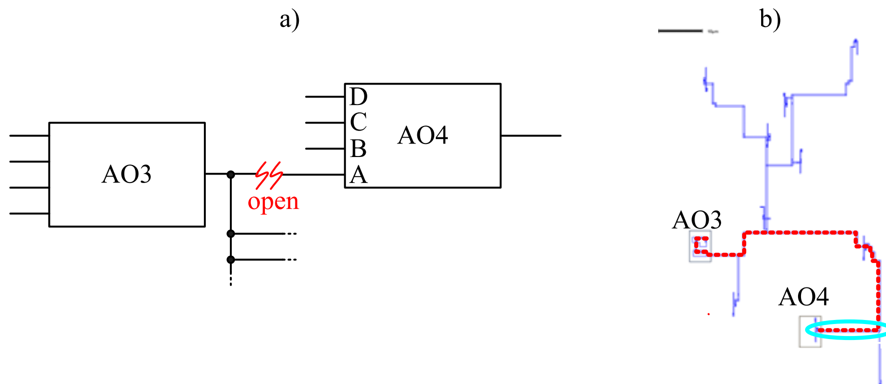

Figure 5.10. Device 87 a) Gate level b) Layout.

The interconnect path considered during the FOS methodology is the one from the *AO3* gate to the *AO4* gate, as shown by the dotted red line in Figure 5.10b. The layout of the failing net (thick blue) and its corresponding coupled neighbours (pink) are depicted in Figure 5.11a. The voltage prediction for the sensitizing patterns assuming a full open defect along net *n_613* is illustrated in Figure 5.11b. On the one hand, red lines (red patterns) are the voltage predictions corresponding to the patterns where the voltage of the defective line was interpreted as logic 1 by the tester. On the other hand, blue lines (blue patterns) are the voltage predictions corresponding to the patterns where the voltage of the defective line was interpreted as logic 0. Notice how the blue and the red lines are mixed for most of open locations, except at the end of the line, where the red patterns have higher voltage predictions than the blue ones, see the zoom at the end of the line in Figure 5.12a. It is for an open located in the last 10 µm of the line where the predicted behaviour matches the experimental results obtained on the tester, corroborating the results of the first scenario reported by the diagnosis tool.

The voltage prediction of the red patterns is higher and differentiated from the low predictions of the blue patterns. This means that the floating line is pulled up or pulled down close to the ideal V_{DD} and V_{GND} values and far from intermediate voltages. This fact causes the device to behave logically stable without the appearance of the

Byzantine problem and without extra current consumption during the I_{DDQ} test. This is corroborated by I_{DDQ} measurements obtained on the tester, as illustrated in Figure 5.12b. Only the leakage current is reported.

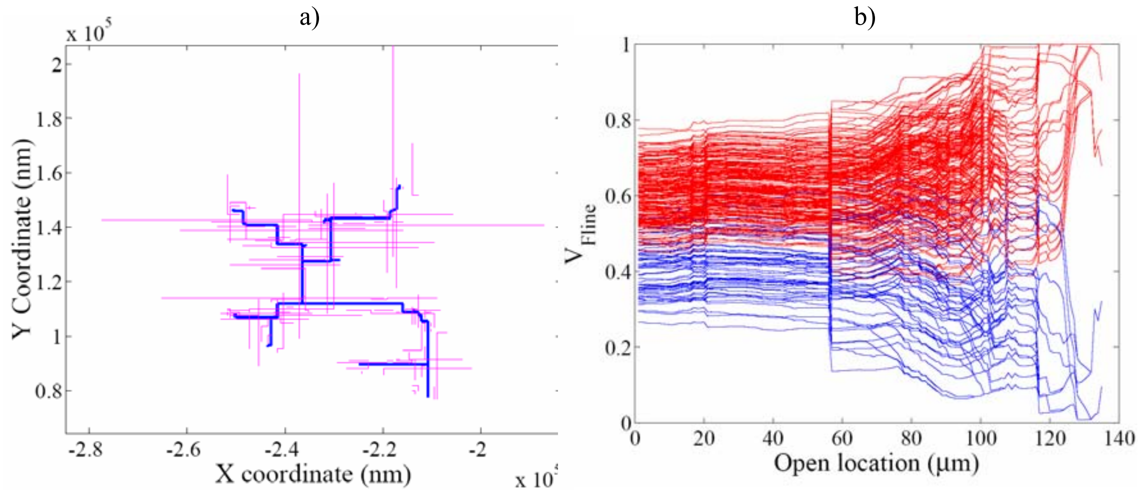

Figure 5.11. Device 87 a) Failing net and coupled neighbours b) Predicted voltage of the failing net.

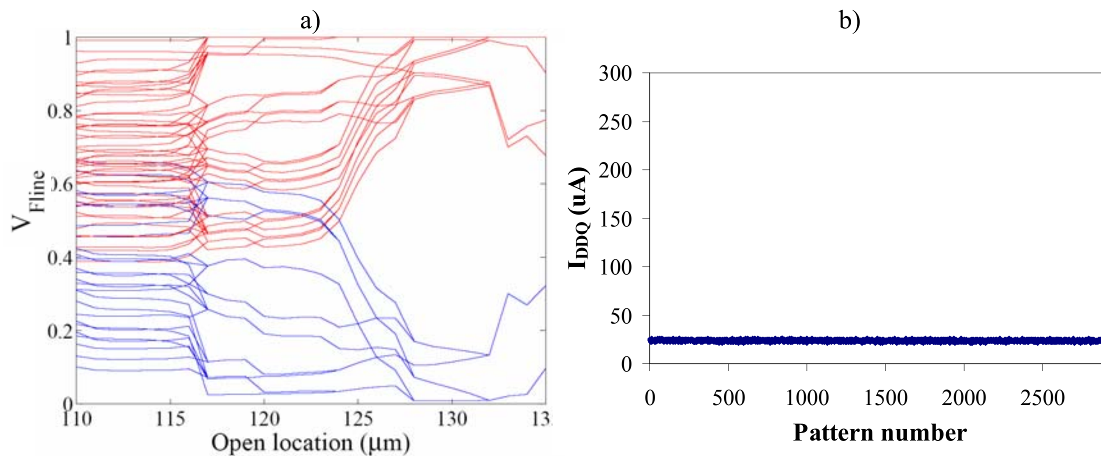

Figure 5.12. Device 87 a) Predicted voltage of the failing net (zoom) b) I_{DDQ} measurements.

5.1.4.2 DEVICE 39B

The failing core 4 of Device 39b is a non-stable core, reporting about 1500 failing vectors. The number of failing vectors is not always the same, but the differences are low. The logic diagnosis considers three possible FSs, all of them with M = 100% and P < 100%. The two first scenarios have the same P value (51%). They are equivalent and are a failing input branch (net *SR_12*) at the *D* port of a flip-flop (*FF*) or an internal fault inside the same *FF*. The *FF* is driven by an *AO3A* complex gate, which has fan-out. In this sense, the third FS, reported with lower P (17%), considers the same whole net as the failing net. Thereby, the third FS pinpoints to the stem of the net and not to one of the branches, as denoted in Figure 5.13. Therefore, applying the FOS

methodology to the path going from the *AO3A* complex gate to the *FF*, both FS1 and FS3 are covered simultaneously.

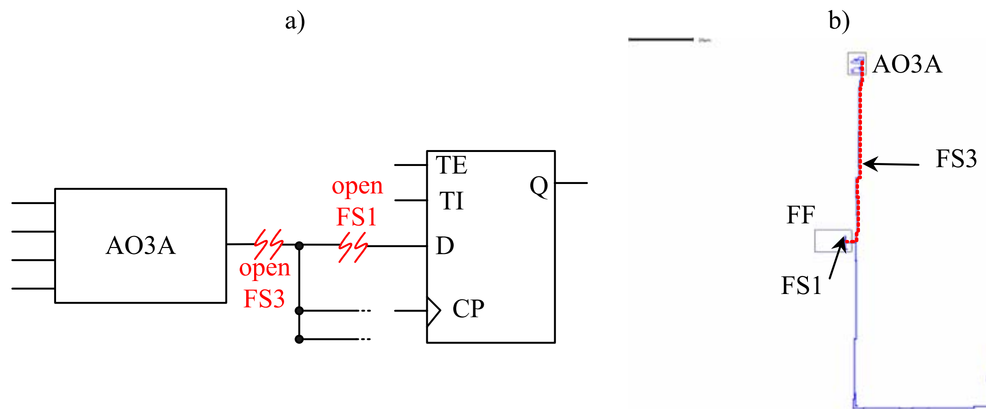

Figure 5.13. Device 39b a) Gate level b) Layout.

The failing net has a total metal length $L = 178\ \mu m$. However, the path considered for the diagnosis procedure (from the *AO3A* gate to the *FF*) has a length of 68 μm. The layout of the failing net and the portion of the coupled neighbours is illustrated in Figure 5.14a. The failing net is the thick blue line and it is made of three different metal layers. The portions of metal tracks (depicted in pink) correspond to 88 coupled neighbouring signals. However, more than half of them are shielded by others neighbouring lines being closer to the failing net. Thus, in the procedure only the 38 non-shielded neighbouring signals are considered. In this way, the path has been divided into 124 segments. The voltage prediction computed for the test patterns that detected a logic 1 (red patterns) or a logic 0 (blue patterns) on the defective net is illustrated in Figure 5.14b. Notice how the blue and red patterns are mixed together. Nevertheless, zooming the region at end of the path (Figure 5.15a), it is observed how when the stem divides into two branches, for the branch driving the *FF* the predicted results are consistent with the experimental results, since the red patterns are predicted with higher voltages than the blue ones. Thereby, it is derived that the open is located at the branch connected to the *FF*, and the other two FSs are discarded. If no success had been reported by the present methodology, the internal fault inside the *FF* would have been considered as the most probable fault explanation for the behaviour of this core.

I_{DDQ} current measurements have been done on the defective device and no high current has been measured, as observed in Figure 5.15. The diagnosed open result is consistent with the negligible quiescent current measured, since the predicted voltages

have no intermediate values and no high current is expected under these circumstances. The fact that this core is non-stable may be caused by external factors, since the slightly differences in the logic behaviours were reported in different days, but during the same test session, the logic behaviour was always the same.

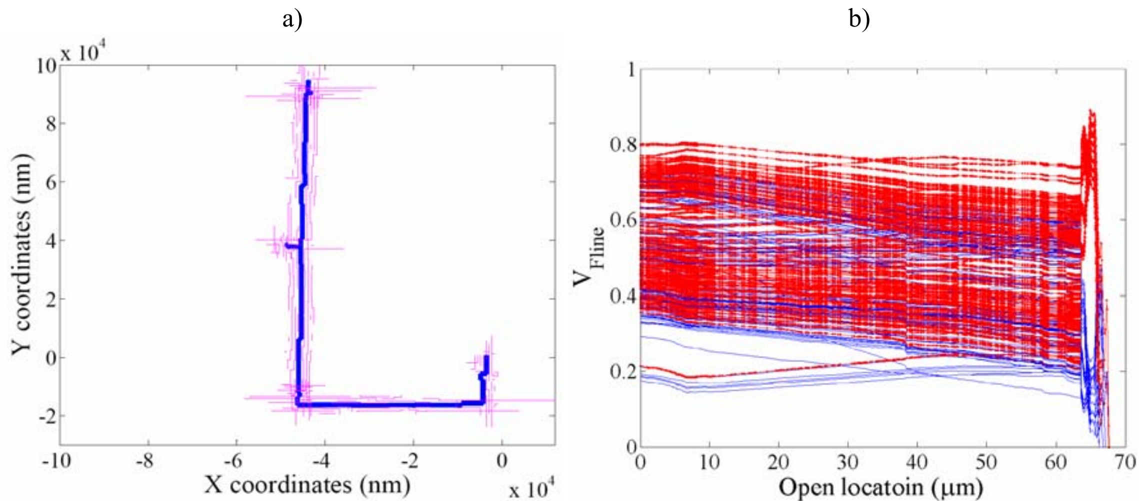

Figure 5.14. Device 39b a) Failing net and neighbours b) Predicted voltage of the failing net.

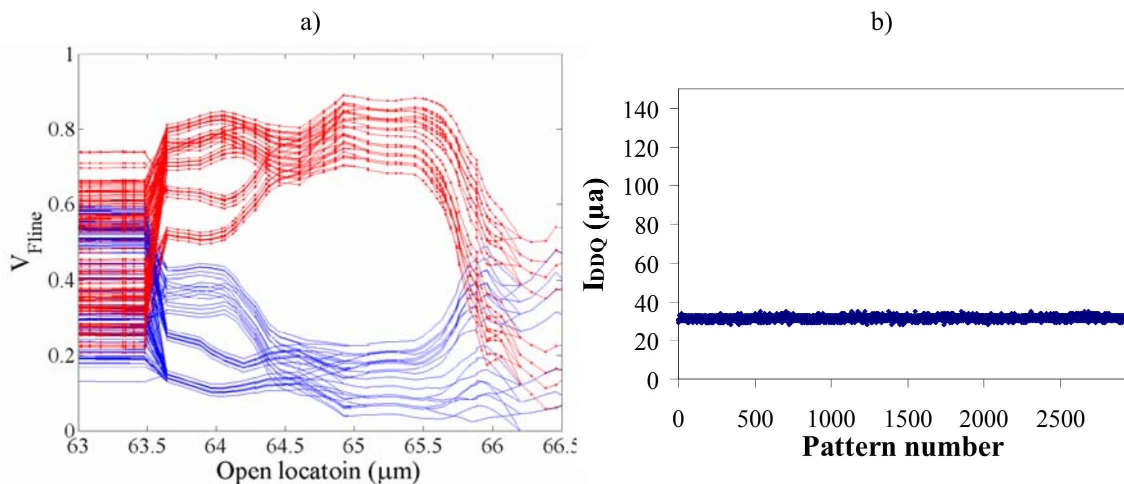

Figure 5.15. Device 39b a) Predicted voltage of the failing net (zoom) b) I_{DDQ} measurements.

5.1.4.3 DEVICE 109

The failing core of Device 109 is core 5. It has stable logic behaviour. Once captured the 54 failing vectors and used the diagnosis tool, two FSs are reported with M = P = 100%. Both scenarios are related. The first one is a SA1 at port *A* of an *AO3A* complex gate (net *R6_5_*) or its equivalent internal faults inside the AO3A gate. The second FS is a bridge between the *B* and the *D* ports of the same AO3A gate, as described in Figure 5.16a. Analysing both the logic and the current behaviour, it can be lead to the conclusion that a bridging fault between the two input ports of *AO3A* does

not give consistent results. Hence, the bridge is discarded. Two possibilities are left, an interconnect full open fault in port *A* or the internal fault inside the *AO3A* gate. Port *A* of the *AO3A* is driven by a *FF*, which in turn drives another instances. If the *FF* has fan-out, then the full open should be located along the branch driving only the *AO3A* gate. This branch is the portion of the net surrounded in light blue in the layout of the net from Figure 5.16b. The path from the driver (*FF*) to the *AO3A* gate comprises about 700 µm. However, the area of interest (the branch driving the *AO3A* gate) is composed of the last 200 µm. The layout of the branch and its coupled neighbours is described in Figure 5.17a. The voltage predictions of the failing net for this range of locations are illustrated in Figure 5.17b. Notice that there are not blue patterns. As the net is reported to behave as a SA1, all the reported patterns are red. In this way, it cannot be assured the matching between the predicted and the experimental behaviour. Nevertheless, it is observed how in the region between 120 and 180 µm the voltage predictions of the red patterns are higher than in the rest of locations.

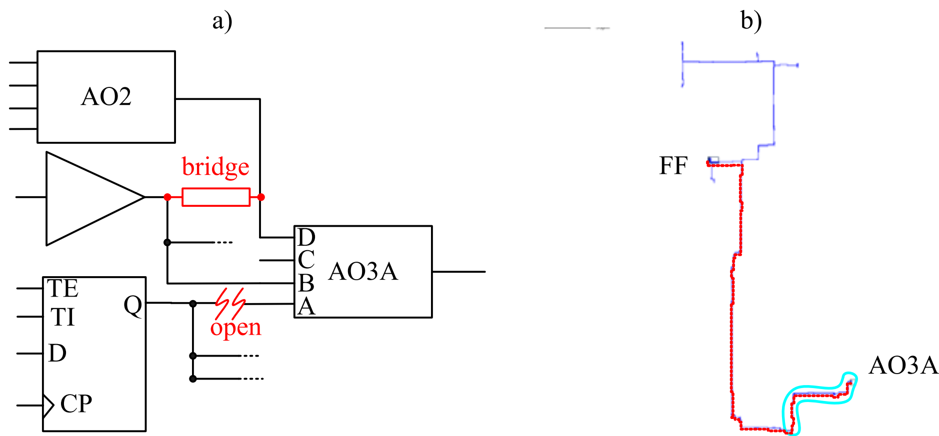

Figure 5.16. Device 109 a) Gate level b) Layout.

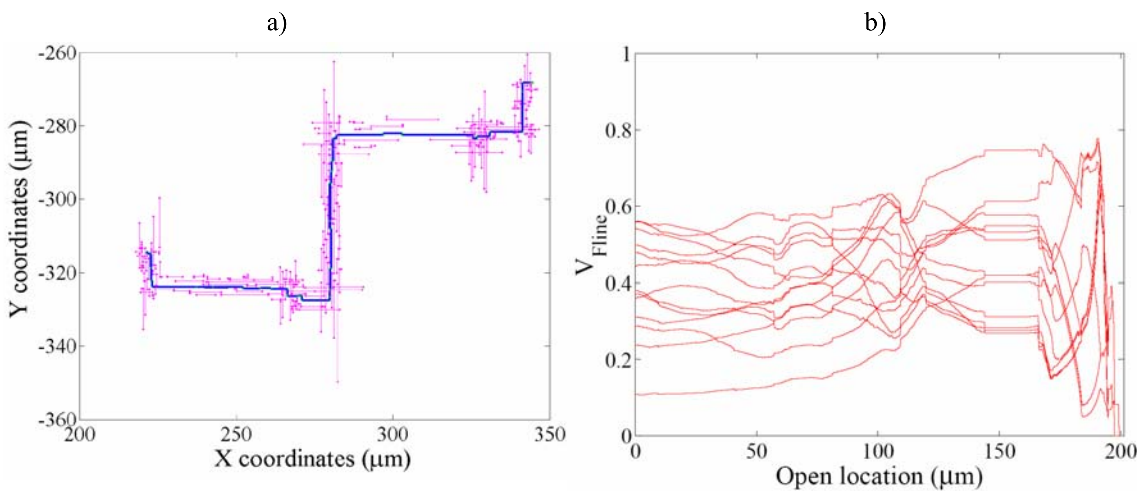

Figure 5.17. Device 109 a) Failing branch and neighbours b) Predicted voltage of the failing net.

In this case, it is determinant the use of current information. The I_{DDQ} measurements obtained on the tester for the present device is plotted in Figure 5.18a. Notice how the I_{DDQ} test results do not resemble the current behaviour of a bridging defect, as it was reported in FS2 (subsequently discarded). However, spread high current values are observed from 35 to 160 μA, assuming voltage degradation on the faulty net.

Once obtained the voltage prediction for every test pattern, with the use of SPICE simulations, it is possible to predict also the current added by the open fault. The comparison between the experimental and the predicted current determines the appropriateness of this fault to explain the behaviour of the faulty core. The transistor description of the *AO3A* gate is shown in Figure 5.18b. As the failing net in driving the input port *A*, there may be two stages of downstream current. The first stage corresponds to the inverting stage of the signal, which is always activated. The first stage is responsible for the I_{DDQ} values up to 85 μm in Figure 5.18a. The second stage depends on the logic state of the rest of the inputs and it is responsible for the highest I_{DDQ} values (up to 150 μm). The simulation results in Figure 5.19a show the current consumption related to the voltage value of port *A* for the two stages of downstream current. Finally, in Figure 5.19b the coefficient of determination between the predicted against the experimental current values is presented. The range of locations comprised between 130 and 175 μm has a R^2 quite higher than the rest of locations. Furthermore, around 165 μm the R^2 is even higher. Notice how this range of location corresponds approximately to the same range where the voltage predictions of the red patterns were higher. In Figure 5.20a, the voltage predictions of the patterns which caused the highest I_{DDQ} values, but do not sensitize logically the fault, are also plotted (green patterns). All these extra patterns are expected to set the floating net to a similar state, around the voltages which cause the current peak in Figure 5.19a. Observe how the voltage prediction for these patterns are similar in the region with the highest R^2 (130-175 μm), which corroborates the location of the open fault.

Based on the results and considering the layout, the most likely place for the full open is between two vias (via3 and via4), as marked in red in Figure 5.20. However, it cannot be discarded the surroundings, marked in dotted red.

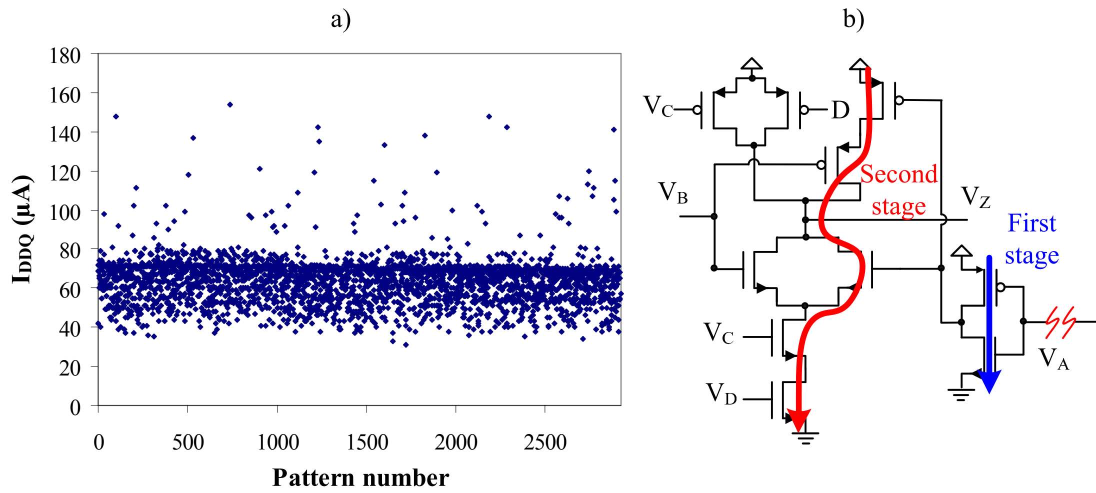

Figure 5.18. Device 109 a) I_{DDQ} measurements b) Current contributions from an AO3A gate.

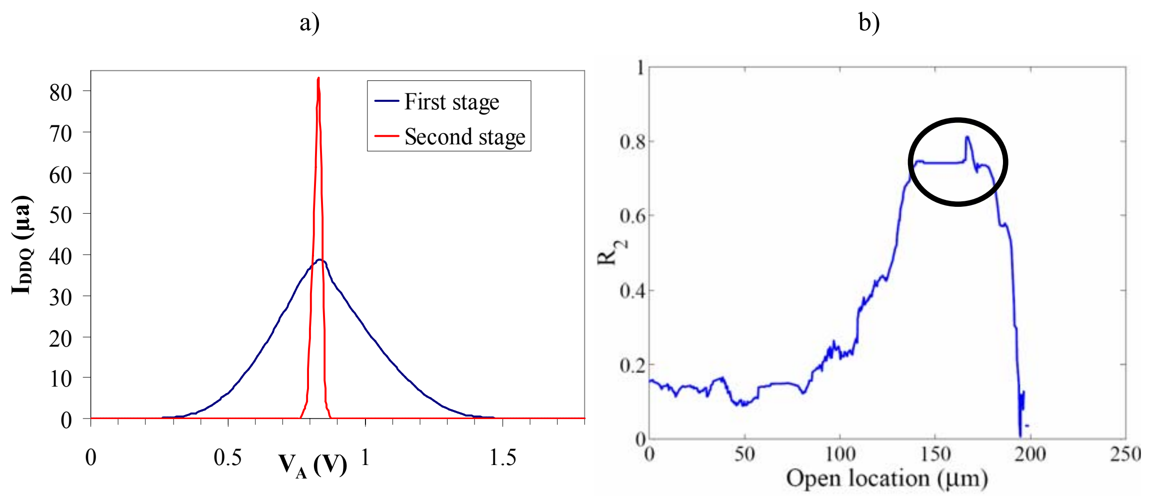

Figure 5.19 Device 109 a) SPICE current results related to V_A. b) Coefficient of determination between the measured I_{DDQ} and the predicted I_{DDQ} derived from V_{Fline}.

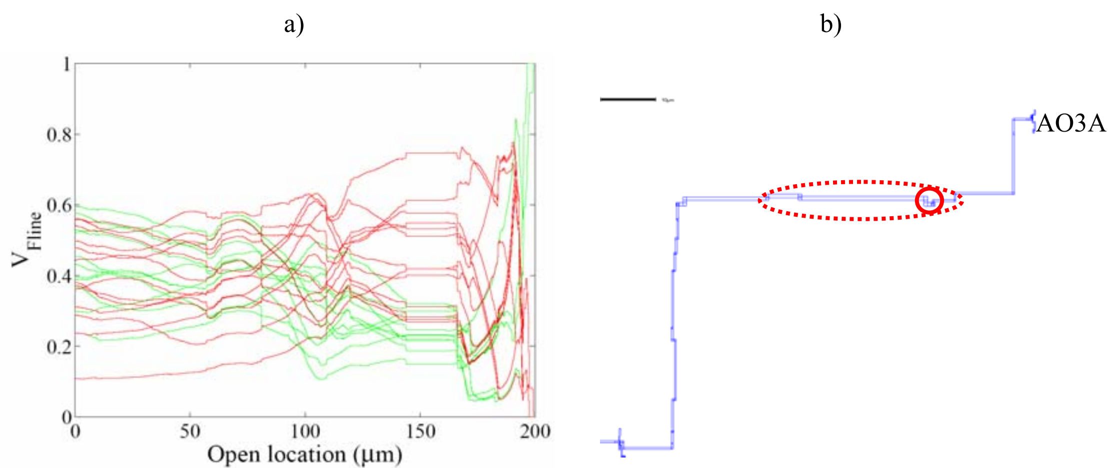

Figure 5.20 Device 109 a) Predicted voltage for patterns causing high I_{DDQ} b) Open location

5.1.5 TUNNELLING LEAKAGE CURRENT ON INTERCONNECT OPENS

This section presents the diagnosis results based on the impact of tunnelling leakage currents on the behaviour of interconnect open defects in a similar way as it was previously presented for Device 27b in Section 4.3.4.

5.1.5.1 DEVICE 46

The core 3 of Device 46 did not pass the logic test. At nominal conditions, around 170 failing vectors were captured. The diagnosis tool reported two equivalent fail scenarios as the most probable ones. They are a failing branch at the input of an inverter or a failing net at the output of the same inverter, respectively (see Figure 5.21a). Both have the same quality measurements, M = 100% and P = 54%. However, once carried out the I_{DDQ} test, two stages of downstream current are observed. Thus, it is lead to the conclusion that the most probable scenario seems to pinpoint to the output of the inverter, as described in Figure 5.21b. The current measurements are shown in Figure 5.22a. When the defect is not excited, a bit more of 100 μA is reported. Nevertheless, when the defect is excited, spread current values around 200 μA and between 300 and 450 μA are obtained. No bridge is able to explain the behaviour of this core. However, the current behaviour is consistent in the presence of an open defect. On the one hand, when the logic path is activated through one of the two downstream gates (*AO2* or *AO5*), I_{DDQ} values around 200 μA are measured. On the other hand, when both paths are activated, the I_{DDQ} values between 300 and 450 μA are obtained.

With this logic and current behaviour, the output net of the inverter is suspected to contain a full open defect. To observe the impact of gate leakage currents on the floating net, an I_{DDQ} test has been obtained waiting seconds before every measurement. The results are illustrated in Figure 5.22b. Apart from the level corresponding to the leakage current, three current levels are observed, corresponding to the different conditions of the downstream gates. The lower level (around 165 μA) corresponds to the case where the logic path through the *AO2* gate is activated (*a* in Figure 5.21b). The level generating around 180 μA corresponds to the case where the path through the *AO5* gate is activated, denoted by *b*. Finally, the higher level (about 265 μA and denoted by *c* in Figure 5.21b) is reported when both paths are activated. The timing I_{DDQ} behaviour for three different patterns considering the different activation conditions of the downstream gates is illustrated in Figure 5.23a. The path through the *AO2* gate is

activated by *pattern 15*. The path through the *AO5* gate is activated by *pattern 3* and both paths are activated by *pattern 19*. Notice how the steady state is reached after a few second of transient behaviour (around 15 seconds). Once reached the steady state, the logic behaviour changes so that the floating net behaves as a SA0, which is consistent with the predicted voltage in the steady state shown in Figure 5.23b. For the different conditions of the downstream gates, different steady state voltages are predicted. Nevertheless, the differences are just a few tenths of mV.

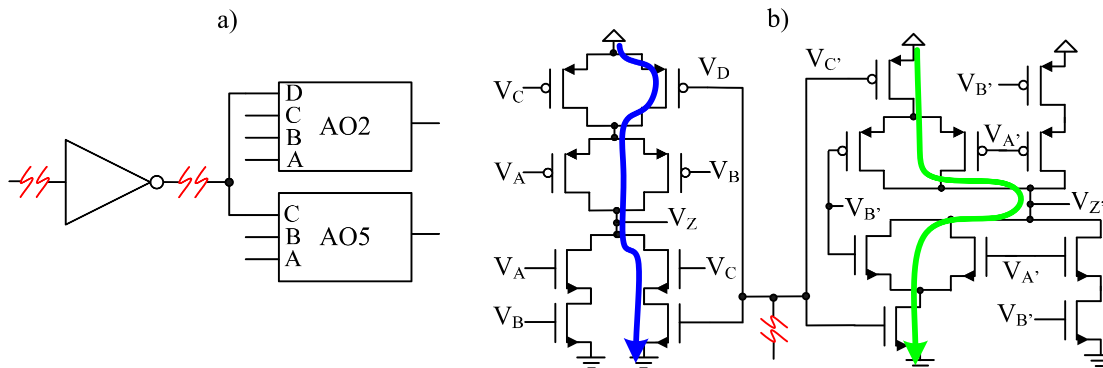

Figure 5.21. Device 46 a) Gate level b) Transistor level.

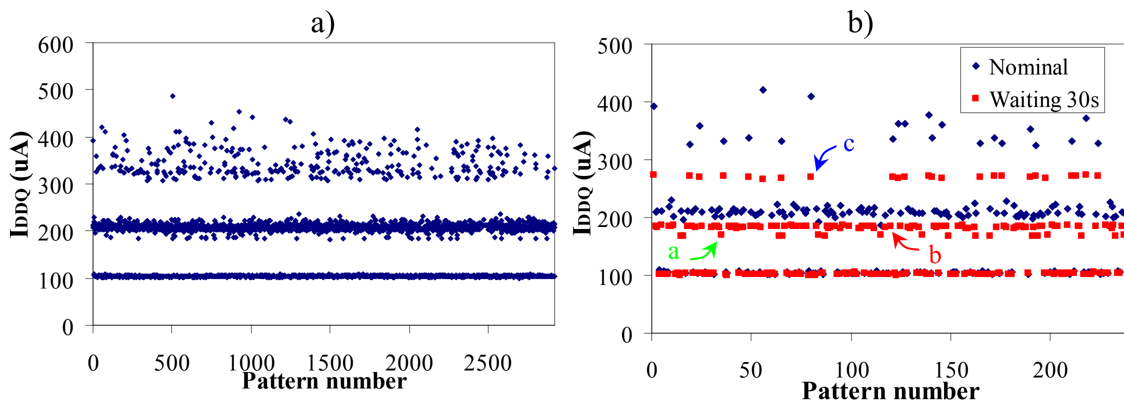

Figure 5.22. I_{DDQ} measurements for device 46 a) Nominal conditions b) First 250 patterns, nominal conditions and waiting 30 s before carrying out the measurement.

Once predicted the steady state voltage, SPICE simulations are used to predict the I_{DDQ} caused in the steady state. Assuming nominal parameters, the *AO2* is expected to cause around 40 μA, whereas the *AO5* 35 μA, as depicted in Figure 5.24a. Notice how these currents are lower than the ones experimentally measured. Nevertheless, process variation causing a steady state voltage a few tenths of mV higher that the nominal one should cause similar I_{DDQ} values to the ones measured on the tester. Furthermore, in Figure 5.23a there is experimental evidence of this fact. Assuming nominal parameters, in the SPICE simulation results (Figure 5.24a) the current peaks of the two gates are

approximately obtained for the same input voltage. However, the I_{DDQ} timing behaviour of *pattern 19* shows that the two current peaks are not overlapped, as expected with nominal parameter. As the voltage of the floating net evolves, the corresponding current peaks are reached at different times, and therefore, at two different voltages of the floating line.

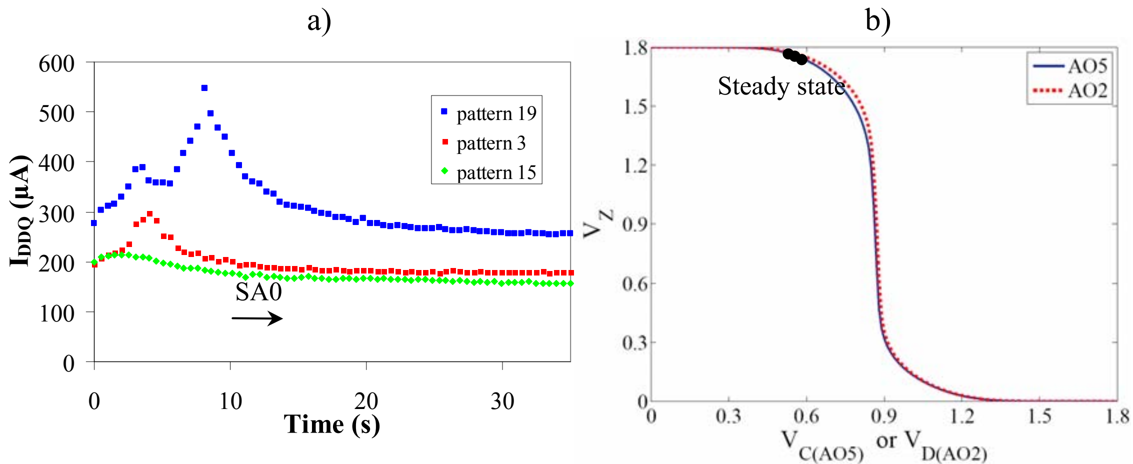

Figure 5.23. Device 46 a) I_{DDQ} time dependent behaviour b) Steady state of the floating net.

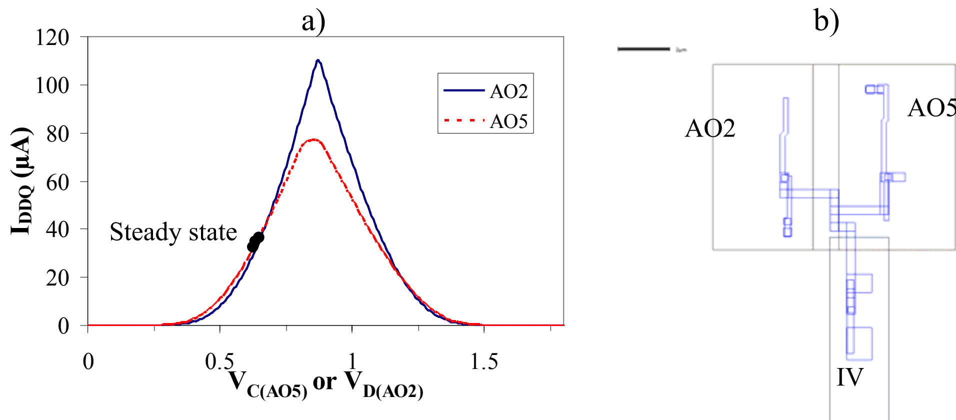

Figure 5.24. Device 46 a) Simulation results: I_{DDQ} vs. $V_{C(AO5)}$ or $V_{D(AO2)}$. b) Layout.

In conclusion, this failing core is expected to contain a full open defect at the output net of the inverter, which is driving in turn the *AO2* and the *AO5* gates, as described in the layout (Figure 5.24b).

5.1.5.2 DEVICE 148

The failing core 5 of Device 148 reported different logic behaviours after certain evolution time. During the nominal test, around 1680 failing vectors were captured. The diagnosis tool reported only one fail scenario with M = 100%. The second one has M < 100% and the rest of scenarios required two faults to explain the faulty logic behaviour. The first fail scenario (M = 100%, P = 55%) is explained by means of two

failing branches at the output of a multiplexer (*MUX21_1*), which in turn drive two multiplexer (*MUX21_2* and *MUX21_3*), as illustrated in Figure 5.25a. The net drives port *A* and port *B* of *MUX21_2* and *MUX21_3*, respectively. Furthermore, the selection ports (*S*) of the downstream multiplexers are driven by the same net. Thus, one path is always activated through the ports driven by the suspicious net, as indicated in the transistor description of Figure 5.25b. On the other hand, if the logic test is applied after certain evolution time, 777 failing vectors are captured. The diagnosis tool reported in this case one fail scenario with M = P = 100%, which is explained by means of a SA0 fault in the same net.

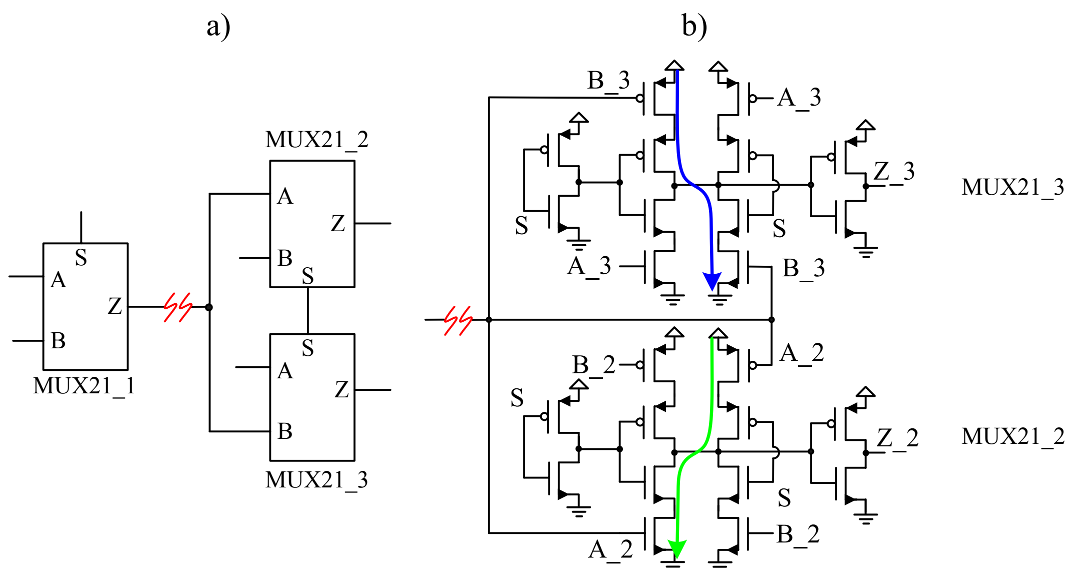

Figure 5.25. Fail Scenario 1 in Device 148 a) Gate level b) Transistor level.

The I_{DDQ} values obtained on the tester reported spread high values (see Figure 5.26a), since there is always a path activated through one of the multiplexers. Most of the values are in the range 130-250 μA. Nevertheless, there are a few patterns causing higher current values (up to 2 mA). Assuming voltage degradation in the suspicious net, since the output of the multiplexers (*MUX21_2* and *MUX21_3*) have fan-out, the second stage of downstream currents can explain these pattern causing higher I_{DDQ} values. Waiting for a few seconds before carrying out the I_{DDQ} measurements, the spread current values become two current levels, depending on the multiplexer activated, as shown in Figure 5.26b. There are around 20 μA of difference between both levels, which depend on the path activated, as observed relating Figure 5.25b and Figure 5.26b.

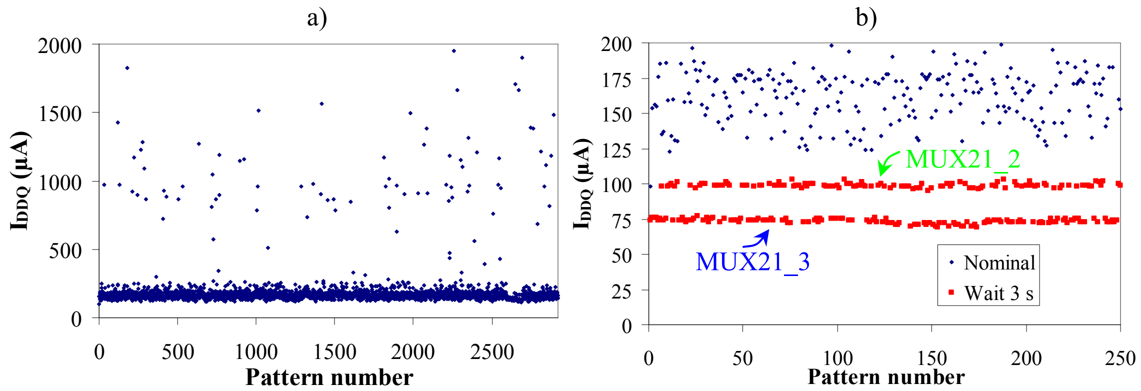

Figure 5.26. I_{DDQ} test for Device148 a) Nominal conditions b) First 250 patterns, nominal conditions and waiting 3 s.

To corroborate the time dependent I_{DDQ} behaviour, current measurements have been applied along the time for two different patterns (see Figure 5.27a). *Pattern 8* set the suspicious net to logic 1 in the fault free case, whereas *pattern 10* set it to logic 0. For *pattern 10*, the logic value is propagated through port *A* of *MUX21_2*, while for *pattern 8* is propagated through port *B* of *MUX21_3*. Notice how the current evolution is different for both patterns. Once reached the steady state, the I_{DDQ} values correspond to the two current levels observed in Figure 5.26b. Nevertheless, the logic behaviour is the same no matter the multiplexer through which the signal is propagated. After a few seconds, the net behaves as a SA0.

The prediction of the steady state of the floating net is consistent with the behaviour experimentally measured. Figure 5.27b shows the voltage prediction, which is interpreted as logic 0 at the inputs of the multiplexers. Assuming nominal parameters, as the multiplexer description is symmetrical, the results are exactly the same no matter the input port (port *A* or *B*) where the open is assumed. This means that the prediction of I_{DDQ} caused by the open is also theoretically independent of the input port of the multiplexer, as illustrated in Figure 5.28a. However, it has been experimentally observed that the current consumed by the faulty core depends on the path activated. Notice how in the steady state, SPICE simulations predicted around 40 µA. However, variations lower than 50 mV in the steady state voltage may cause differences of 20 µA. Therefore, process variability may cause the steady state voltage to be slightly different for every multiplexer, resulting in this I_{DDQ} discrepancy. Furthermore, in Figure 5.27a, it is observed how the I_{DDQ} decreases with time for *pattern 8*, whereas it increases slightly for *pattern 10*. This means that *pattern 10* sets the floating net to an initial voltage

higher than the final voltage but lower than the voltage causing the highest current consumption. On the other hand, *pattern 8* sets the floating net to a voltage slightly lower than the final one. Both cases are represented in Figure 5.28a.

As a conclusion, the behaviour of this faulty core is explained by a full open defect at the stem of the output of *MUX21_1*, which is driving in turn the other two multiplexers, as described in the layout description of Figure 5.28b.

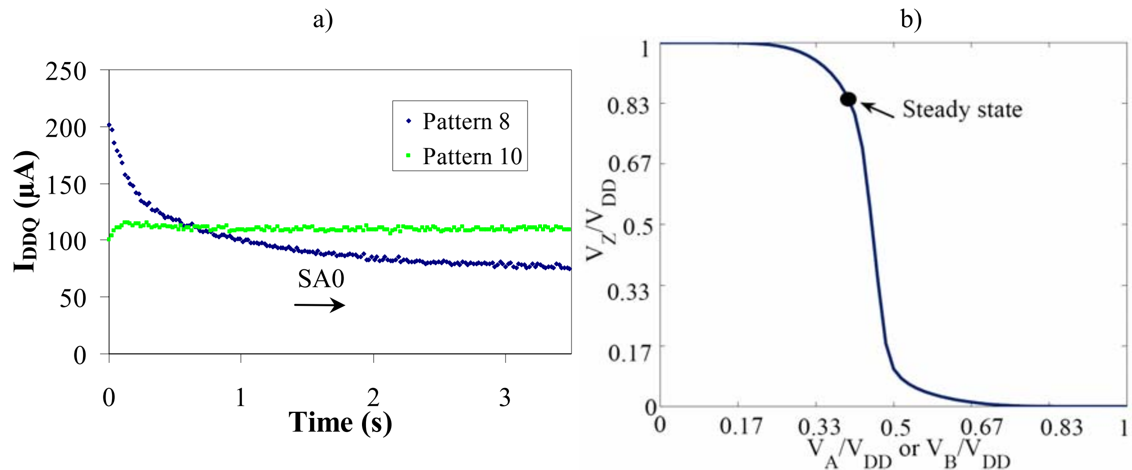

Figure 5.27. Device 148 a) I_{DDQ} time dependent behaviour b) Steady state of the floating net.

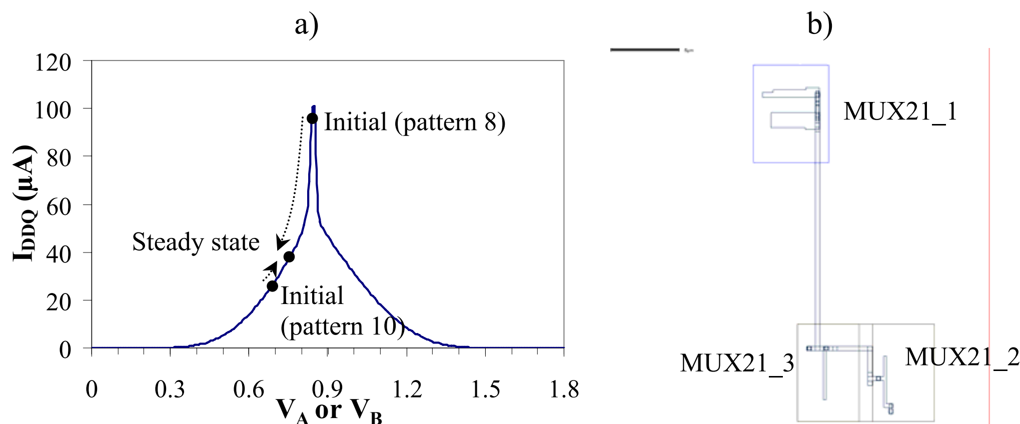

Figure 5.28. Device 148 a) Simulation results: I_{DDQ} vs. V_A or V_B b) Layout.

5.1.5.3 DEVICE 26B

The core 5 of Device 26b presented different logic behaviours after certain evolution time. At nominal conditions (328 failing vectors), the diagnosis tool reported with M = P = 100% that the failing behaviour is explained by means of a SA1 at the output of a 2-input *NAND* gate or the equivalent SA0 faults at its inputs. However, letting the device on for a few seconds before applying the test, the logic behaviour is modified (109 failing vectors in this case), so that the diagnosis tool reported as the first FS a SA1 with M = P = 100% at port *A* of the same *NAND* gate. Therefore, both

scenarios pinpoint to the same location (port *A*, as described in Figure 5.29), but with different logic behaviour. Furthermore, the I_{DDQ} behaviour confirms that the defect is related to port *A* of the *NAND* gate. The I_{DDQ} measurements for this core are illustrated in Figure 5.30a. The high current values are obtained when the path through the port *A* of the *NAND* gate is activated. Although resembling a bridging defect, no bridge can explained the logic and the current behaviour of the present core. In fact, the two current levels correspond to two stages of downstream current. The lower one corresponds when the logic path through port *A* of the *NAND* is activated. The higher one is when both the logic path through port *A* of the *NAND* and the logic path through port *C* of the *AO3A* instance are activated, as depicted in Figure 5.30a.

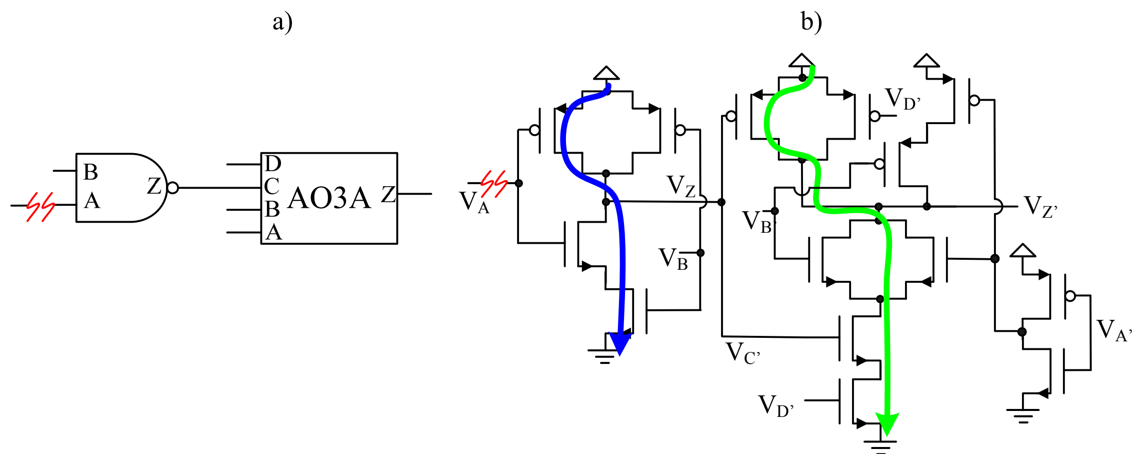

Figure 5.29. Device 26b a) Gate level b) Transistor level.

This faulty core has I_{DDQ} time dependent behaviour, as illustrated in Figure 5.30b. Waiting for a few seconds before carrying on every I_{DDQ} measurement on the tester causes the two levels of downstream current to become one, although still causing high current, but just around 10 µA. The analysis of the transient current behaviour for two patterns exciting the defect is shown in Figure 5.31a. The current consumption decreases with time. However, it does not decrease down to the defect-free value, but it adds around 10 µA, achieved after 12s. Notice how there are two inflection points caused by the two stages of downstream current for *pattern 13*. Furthermore, the logic behaviour once reached the steady state changes, since it behaves as a SA0. For *pattern 25*, only the path through the NAND gate is activated. Thus, only one inflection point is observed and lower current is generated in the initial state. The SPICE simulation results with the I_{DDQ} consumption related to the voltage of port *A* is illustrated in Figure 5.31b. Observe the impact of the second stage of downstream current (*AO3A* gate). The

currents obtained by simulation are consistent with the experimental measurements illustrated in Figure 5.30a, where about 75 µA are added by the first stage and around 35 µA by the second stage of downstream current.

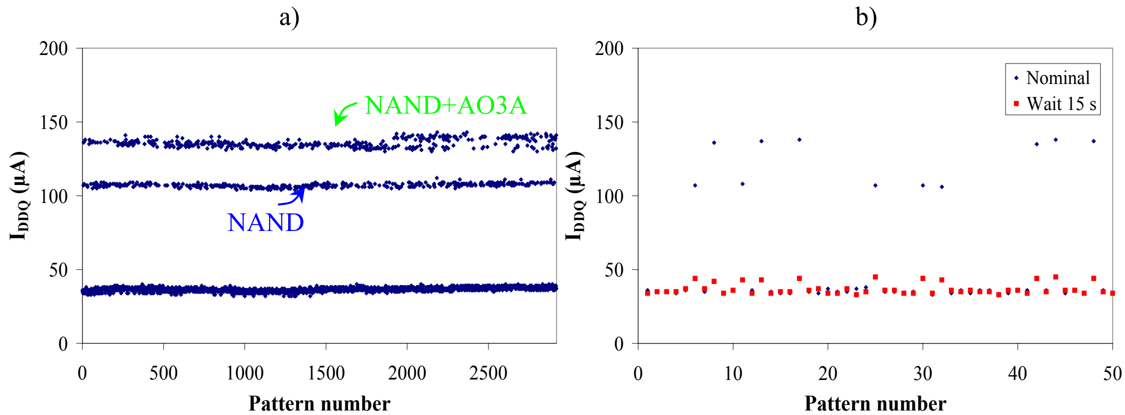

Figure 5.30. I_{DDQ} test for Device26b a) Nominal conditions b) First 250 patterns, nominal conditions and waiting 3 s.

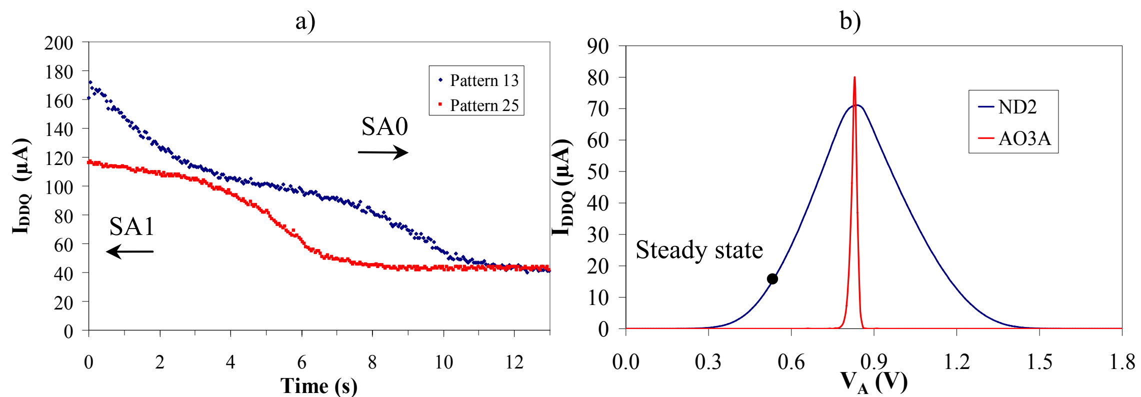

Figure 5.31. Device 26b a) I_{DDQ} time dependent behaviour b) Simulation results: I_{DDQ} vs. V_{in}

The steady state of the floating net is predicted to corroborate the experimental behaviour of the faulty core. Figure 5.32a shows the prediction of the steady state voltage assuming a full open defect at port *A* of the *NAND* gate. Notice how the predicted voltage is around 0.55V, which is interpreted as logic 0, being consistent with the SA0 behaviour reported by the experimental results once reached the steady state. Furthermore, this voltage prediction causes around 17 µA in the simulation results reported in Figure 5.31b, which is similar (although slightly higher) to the current added by the defect in the experimental results.

Relating all this information with the layout of the design, the full open defect explaining the faulty behaviour of this core should be located in the short branch driving the 2-input NAND gate, as depicted in Figure 5.32b.

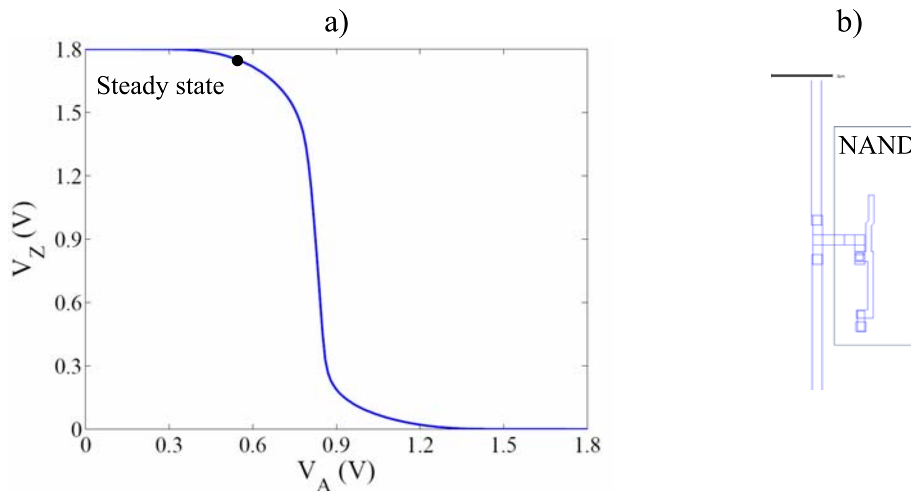

Figure 5.32. Device 26b a) Steady state of floating net b) Layout.

5.2 90 NM TECHNOLOGY DEVICES

A set of 90 nm technology defective devices from *NXP Semiconductors* has been studied. The number of pins of these devices exceeds the capability of the HP82000 tester placed in the *Electronic Engineering Department* of the *UPC*. Thus, both the logic and the current tests have been carried out by *NXP Semiconductors* using a Agilent 93000 tester. These defective devices did not pass the SA test. The logic tests have been applied at V_{MAX} (1.32 V) at two different temperatures (room temperature and high temperature) and for some of them also at V_{VLV} (0.9 V). Furthermore, some of these tests have been applied twice to see if there is repeatability on the results. The selection of the samples as well as the tests were carried out by members of *NXP Semiconductors* staff.

5.2.1 DIAGNOSIS OF BRIDGING DEFECTS

The methodology described in section 3.2 has been applied to the devices suspected to contain a bridging defect. For that purpose, I_{DDQ} measurements at low power supply voltage (0.9 V) have been obtained for the first 20 SA patterns. A summary of the results for the defective cores, which are suspicious to contain a bridge is shown in Table 5.VII. The results are organized in a similar manner as the ones previously presented for the *Vector4* cores. The multiple level I_{DDQ} based diagnosis is successful to report eleven bridges for the defective cores. The majority (nine out of eleven) are stable devices. There are five bridges between interconnect nets (see Figure 5.33), five bridges involving internal nets, and a bridge between a net and a power rail.

Nevertheless, four out of the five internal bridges involve an internal net and a power rail.

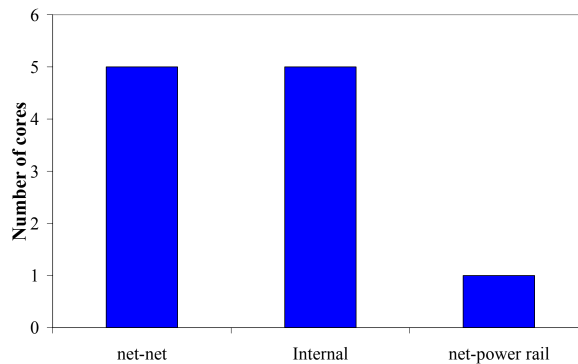

Figure 5.33. Bridge classification for the 90 nm technology devices.

5.3 CONCLUSIONS

It has been demonstrated the feasibility of the methodologies developed in Chapter 3 and 4. In fact, the multiple level I_{DDQ} based diagnosis have been successfully applied to faulty devices from 0.18 µm and 90 nm technologies. Furthermore, the diagnosis of full opens based on the FOS model and the impact of gate leakage current have been successfully applied to a set of 180 µm technology devices.

TABLE 5.VII
SUMMARY OF BRIDGING DEFECTS DIAGNOSIS RESULTS: 90 NM TECHNOLOGY DEVICES

Device	Diagnosis tool (Faloc)							Multiple level I_{DDQ} based diagnosis			
	Stable	FS1	Net 1	Net 2	M (%)	P (%)	Equivalences	Net A	Net B	β_1	R^2
1	Yes	SA	n_14341	--	100	95	Yes	n_14193	n_14268	0.821	0.998
2	Yes	SA	n_47712	--	100	100	Yes	internal	V_{GND}	1.025	0.999
3	Yes	SA	n_39151	--	100	100	No	internal	V_{DD}	1.118	0.987
4	Yes	SA	n_015	--	100	100	Yes	internal	V_{GND}	1.029	0.999
5	Yes	SA	z_3x[4]	--	100	100	No	internal	V_{GND}	1.025	0.996
6	Yes	SA	n_38171	--	100	100	No	n_38171	V_{DD}	0.89	0.999
7	No	Bridge	n_4896_10	mask_reg_2	100	72	No	n_4896_10	mask_reg_2	0.98	0.995
8	Yes	Bridge	web_neg	n_5801	100	100	No	web_neg	n_5801	1.055	0.999
9	No	Failin net	n_9455_16	--	99	11	No	n_9455_16	n_10001_16	0.870	0.996
10	Yes	Failing net	n_14636	--	100	100	No	n_14636	Internal	0.977	0.978
11	Yes	Bridge	n_10789	n_10489	100	55	No	n_10789	n_10489	0.964	0.998

CHAPTER 6. CONCLUSIONS AND FUTURE WORK

Transistor dimensions are scaled down for every new technology. Such high level of integration has increased the complexity of the ICs manufacturing process, arising new complex failure mechanisms in nanometer technologies. In this context, the importance of fault diagnosis increases due to reduced time to market and the high cost of failure analysis. The development of new diagnosis methodologies which overcome the paradigms arisen in future technologies is then required. This thesis has presented the analysis of existing and new failure mechanism and proposed new diagnosis methodologies to improve the location of faults. The work has been focused on two classes of faults: bridges and opens.

Although extensive work has been developed for the diagnosis of bridging faults, most of this research has focused on logic based techniques. Nevertheless, they are less efficient in the presence of the Byzantine problem. On the other hand, some works have paid attention to the rich information obtained during the I_{DDQ} test for the diagnosis of bridging faults. However, the impact of downstream current has not been previously analyzed for diagnosis purposes. In this thesis, the impact and the dependence of the downstream current with the power supply voltage have been analyzed and experimentally measured. For that reason, it has been proposed to carry out I_{DDQ} measurements at low power supply voltages for diagnosis purposes. Furthermore, the multiple level I_{DDQ} based diagnosis has been presented. This diagnosis technique takes benefit from the currents generated by the different network excitations. This methodology has been successfully applied to real defective devices from 0.18 µm and 90 nm technologies with low number of current measurements (down to 20 measurement for the 90 nm technology devices).

There is great concern about the feasibility of current methodologies due to the increasing leakage current and process variability. However, observing the results obtained for the 90 nm technology devices, the feasibility of the method is assured for the near future. In long term, research work is still required for the continuity of the methodology. On the one hand, improvements in controlling process variability may extend the feasibility of this technique. On the other hand, the development of new materials or new design alternatives may soften the increase of leakage current. Anyway, as the limit of application is achieved, the use of statistical processing of data is an alternative to extend the application of such methodology.

As an alternative to current based techniques, it has been demonstrated that shmoo plots can also be useful for diagnosis purposes. Low voltage has been traditionally considered as an advantageous condition for the detection of bridging faults. However, it has been demonstrated that in presence of bridges connecting balanced n- and p-networks, the higher the power supply value, the more likely the defective node to be logically interpreted as incorrect by the next gates. What is more, in some cases the bridge is detected at both low and high power supply voltages, but not at nominal conditions. Experimental evidence of this fact has been presented. This behaviour causes many bridge configurations to generate special pass/fail regions on the shmoo

plots, which has its direct translation into diagnosis applications . Research work is still required in this direction. The outlines have been given in this thesis. However, an extensive characterization of the different behaviours of bridging faults and the impact of process variability on these behaviours can open a new field of study to improve the diagnosis of such faults.

The other main part of the thesis has been based on open faults. The characterization of both full and resistive open has been experimentally done by means of a fabricated circuit in a 0.35 μm technology. On the one hand, experimental results with full opens have allowed the quantification of the impact of the neighbouring coupling capacitances to the floating net. On the other hand, for resistive opens, experiments have demonstrated the effect of the history effect caused by the patterns previously applied and also the impact of the open location on the delay. Traditionally, it has been reported that the highest delay is obtained when the resistive open is located at the beginning of the net. Nevertheless, in this thesis it has been shown how this is true for high resistive opens. In case of low resistive open, the highest delay is obtained for an intermediate location, depending on the relationship between the open resistance, the on-resistance, the parasitic capacitances to the defective net and the logic threshold of the downstream gates. Experimental measurements with the fabricated chip have proved this behaviour.

The results obtained with full open defects of the fabricated design have been the basis for the development of a new methodology for the diagnosis of interconnect full open defects. The FOS methodology divides the interconnect line into different segments based on the topology of the faulty line. Knowing the logic state of the neighbouring lines, the voltage of the floating net is predicted and then compared with the experimental results obtained on the tester. This method has been successfully applied to a set of 0.18 μm devices. Although developed to be applied with logic information, the FOS method has been proved to be also useful with current information. As the impact of the parasitic neighbouring capacitances is expected to increase in the future, the FOS methodology is indicated for nanometer technologies. The main limitation of the methodology is for short nets. When the end of the net is approaching, the voltage prediction is not accurate and the results are not valid, since transistor parasitic capacitances are not taken into account. Research work to improve

the FOS model is still required. The impact of process variability has not been considered by the methodology in its present form, which may impact the voltage predictions of the floating net.

The impact of the gate tunnelling leakage currents on the behaviour of full open defects has been analyzed as well. To the author's knowledge, this behaviour has not been previously reported. In old technologies, the oxide thickness was high enough so that the gate leakage currents were negligible. As technology dimensions are scaled down, the oxide thickness is thin enough so that the gate tunnelling leakage currents influence the behaviour of floating lines. They cause transient evolutions on the floating node until reaching the steady state, which is technology dependent. It has been experimentally demonstrated that these evolutions are in the order of seconds for a 0.18 μm technology. However, for future technologies, simulation results show that the transient evolutions decrease some orders of magnitude, down to a few μs. The impact of gate leakage currents have both testing and diagnosis implications. Due to this factor, some full open defects present in 0.18 μm technology devices have been diagnosed.

The two methodologies (FOS and gate leakage currents) are complementary, so that one the combination of both models are expected to characterize the behaviour of full open defects accurately for nanometer technologies. At nominal conditions, every time that a pattern is applied to the faulty device, the voltage of the floating line is determined by the neighbourhood state, which is predicted by the FOS model. If sufficient time passes to make observable the impact of the gate leakage currents after the application of a test pattern, then the steady state is only determined by technology parameters and the downstream gates. In case of full opens at the end of the line, neighbouring coupling capacitances are low, so that the transient evolution is faster related to the case when the open is located at the beginning of the line. Research work is still required on that direction, especially for the transient behaviour of the floating net prior to achieve the steady state. For future technologies, predictions of the exact location of the open can be studied relating the FOS model with the transient logic behaviour of the floating net due to the gate leakage currents.

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ANNEX A. BRIDGING FAULTS RESULTS

This annex presents a fast explanation of the devices (*Vector4* and 90 nm technology devices) used for the diagnosis of bridging and open faults. It also summarizes the details of the devices diagnosed to contain a bridging fault, which have been previously presented in sections 5.1.3 and 5.2.1.

A.1 *Vector4* devices

The *Vector4* is a *NXP Semiconductors* chip designed in order to speed up the introduction of new IC production processes and monitoring the existing ones. The *Vector4* is representative of normal products to cover all types of problems that might arise during fabrication processes. Therefore, it contains all types of commonly used modules. Furthermore, there is the controller block, which is the technical heart of the device. The function of the controller is to activate or de-activate blocks and to generate input data for the memories. It comprises 80 pins in QFP80 package.

The device is easy to analyze in order to find the problems as soon as possible. For that reason, the different modules are separately accessible from the outside. This work is focused on random logic, which is difficult to analyze because it is hard to pinpoint the specific failing cell. In this sense, the *Vector4* design is composed of six different cores of random logic. There are layout differences between them. Some of them have metal spread on the routing. The rest of cores are neglected.

Next, a summary of the results of the bridging faults diagnosed with the multiple level I_{DDQ} based diagnosis is presented. In the presence of downstream current, the values of R^2 and β_1 reported in the tables are the ones obtained at very low voltage.

A.1.1. Device 10

TABLE A.I
DIAGNOSIS RESULTS FOR DEVICE 10

Logic Diagnosis (Faloc)					
FS1	**Net1**	**Net2**	**M(%)**	**P(%)**	**Equiv.**
Bridge	n_2882	n_2091	100	100	No
Bridge		**Single Level I_{DDQ} Diagnosis**		**Multiple Level I_{DDQ} Diagnosis**	
Net1	**Net2**	**M(%)**	**P(%)**	**β_1**	**R^2**
n_2882	n_2091	100	100	1.195	0.997

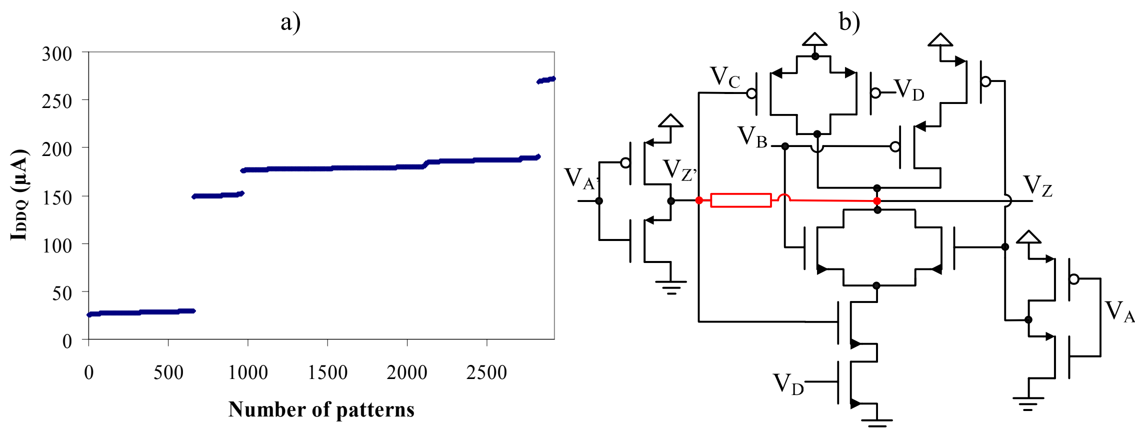

Figure A.1. Device 10 a) Current signature b) Transistor level

A.1.2. Device 11

This device has another faulty core which is adding more than 2 mA of DC (Direct Current) current. That is why the lowest current level is generating more than 2.5 mA. Nevertheless, this DC component is not caused by the bridge, but it is caused

by another defect from the other faulty core. Furthermore, this case shows some kind of systematic problem, since there are two more devices reporting the same bridge (Devices 112 and 129) and also with a current signature with an extra DC current component (although with different value) caused by another defective core.

TABLE A.II
DIAGNOSIS RESULTS FOR DEVICE 11

Logic Diagnosis (Faloc)					
FS1	**Net1**	**Net2**	**M(%)**	**P(%)**	**Equiv.**
SA	n_26512	--	100	100	yes
Internal	i_123701	--	100	100	--
Bridge		**Single Level I_{DDQ} Diagnosis**		**Multiple Level I_{DDQ} Diagnosis**	
Net1	**Net2**	**M(%)**	**P(%)**	**β_1**	**R_2**
n_26512	V_{GND}	100	100	1.085	0.999

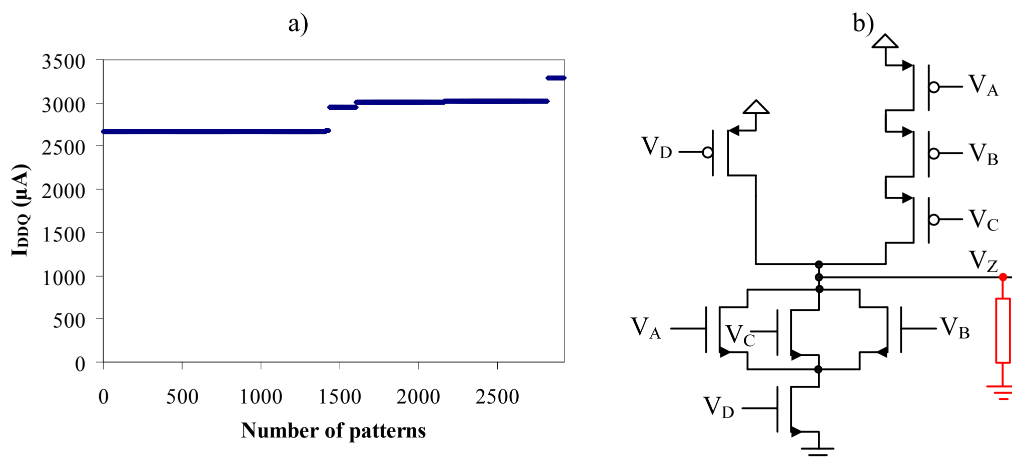

Figure A.2. Device 11 a) Current signature b) Transistor level.

A.1.3. Device 14

TABLE A.III
DIAGNOSIS RESULTS FOR DEVICE 14

Logic Diagnosis (Faloc)							
FS1	**Net1**	**Net2**	**M(%)**	**P(%)**		**Equiv.**	
Bridge	n_389	n_1601	100	100		no	
Bridge		**Single Level I_{DDQ} Diagnosis**		**Multiple Level I_{DDQ} Diagnosis**			
Net1	**Net2**	**M(%)**	**P(%)**	**β_1**		**R^2**	
				V_{NOM}	**V_{VLV}**	**V_{NOM}**	**V_{VLV}**
n_389	n_1601	100	100	1.234	1.216	0.980	0.996

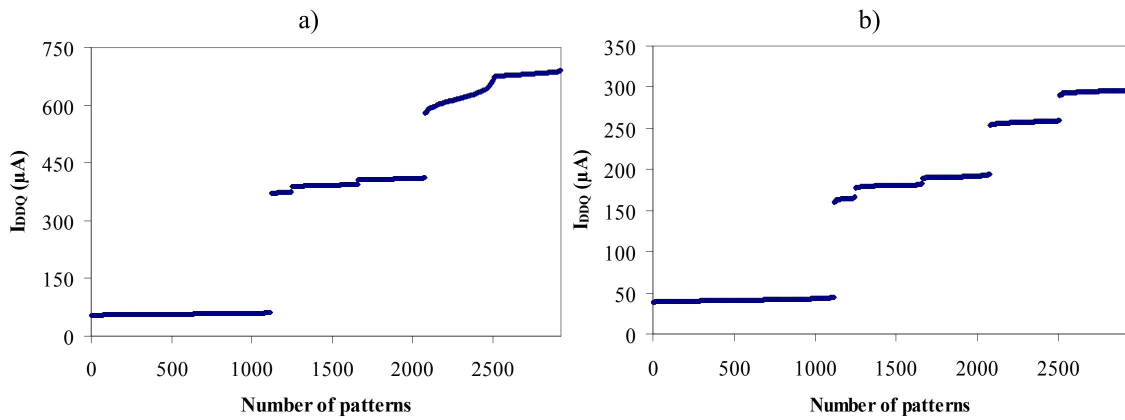

Figure A.3. Device 14 - Current signature a) V_{NOM} b) V_{VLV}.

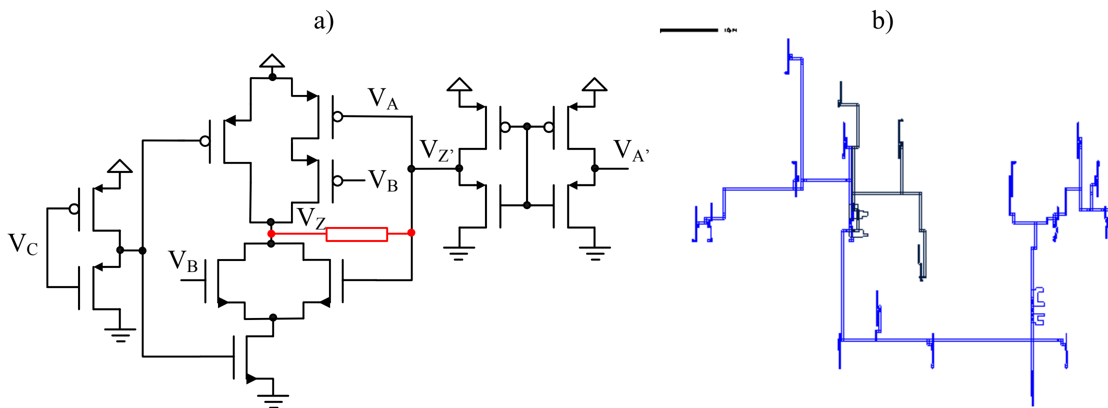

Figure A.4. Device 14 a) Transistor level b) Layout.

A.1.4. Device 35

TABLE A.IV
DIAGNOSIS RESULTS FOR DEVICE 35

Logic Diagnosis (Faloc)					
FS1	**Net1**	**Net2**	**M(%)**	**P(%)**	**Equiv.**
SA	n_132612	--	100	100	yes
SA	n_16072	--	100	100	--
Internal	i_3726	--	100	100	--
Bridge		**Single Level I_{DDQ} Diagnosis**		**Multiple Level I_{DDQ} Diagnosis**	
Net1	**Net2**	**M(%)**	**P(%)**	**β_1**	**R^2**
n_132612	V_{DD}	100	100	1.061	0.999

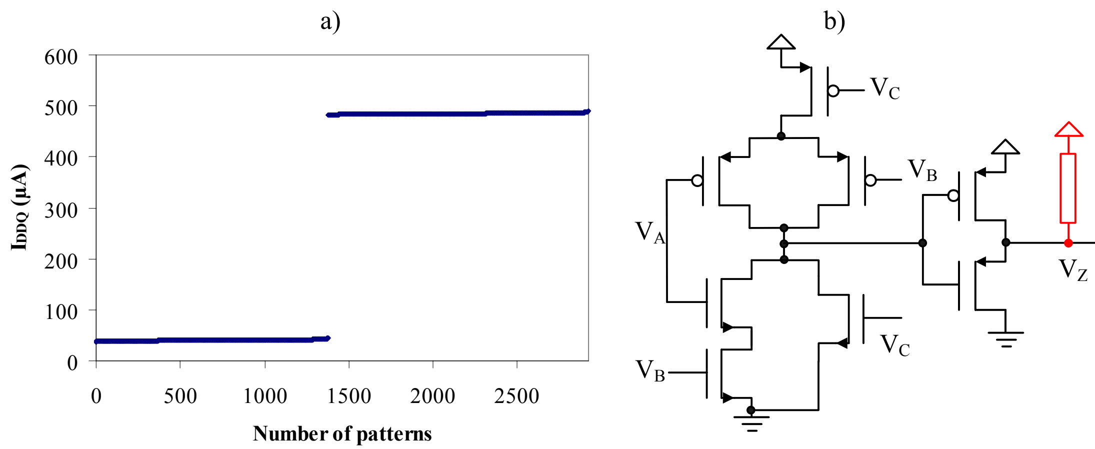

Figure A.5. Device 35 a) Current signature b) Transistor level.

A.1.5. Device 38

TABLE A.V
DIAGNOSIS RESULTS FOR DEVICE 38

Logic Diagnosis (Faloc)					
FS1	**Net1**	**Net2**	**M(%)**	**P(%)**	**Equiv.**
Failing net	n_553	--	100	52	yes
Failing net	i_44133	--	100	52	--
Bridge		**Single Level I_{DDQ} Diagnosis**		**Multiple Levels I_{DDQ} Diagnosis**	
Net1	**Net2**	**M (%)**	**P(%)**	**β_1**	**R^2**
n_553	tq[6]	100	100	1.125	0.999

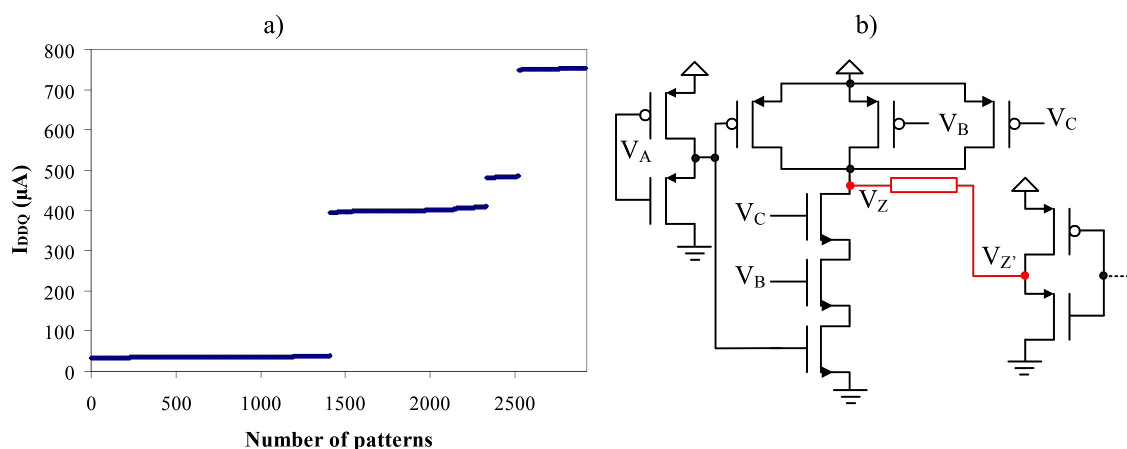

Figure A.6. Device 38 a) Current signature b) Transistor level.

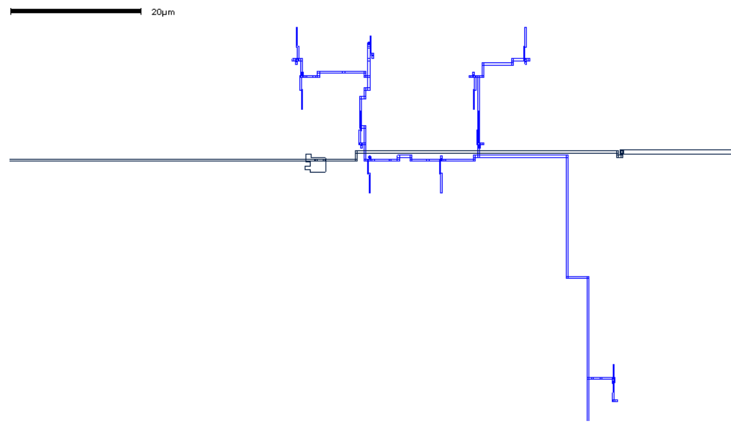

Figure A.7. Device 38- Layout.

A.1.6. Device 47

TABLE A.VI
DIAGNOSIS RESULTS FOR DEVICE 47

Logic Diagnosis (Faloc)					
FS1	**Net1**	**Net2**	**M(%)**	**P(%)**	**Equiv.**
SA	n_2574	--	100	100	yes
SA	n_30430	--	100	100	--
SA	n_30330	--	100	100	--
Bridge	n_2574	n_25479	100	100	--
Bridge		**Single Level I_{DDQ} Diagnosis**		**Multiple Levels I_{DDQ} Diagnosis**	
Net1	**Net2**	**M(%)**	**P(%)**	**β_1**	**R^2**
n_2574	V_{DD}	100	100	1.175	0.999

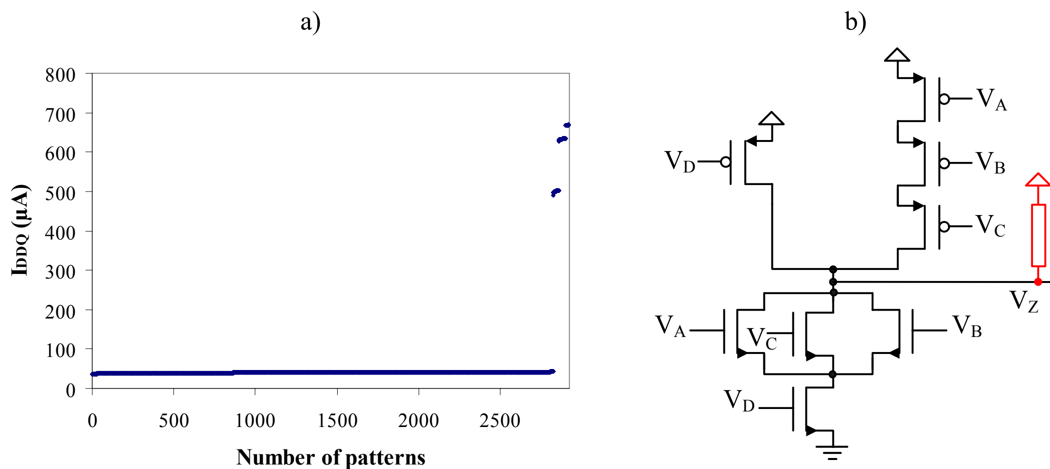

Figure A.8. Device 47 a) Current signature b) Transistor level.

A.1.7. Device 53

TABLE A.VII
DIAGNOSIS RESULTS FOR DEVICE 53

Logic Diagnosis (Faloc)					
FS1	**Net1**	**Net2**	**M (%)**	**P (%)**	**Equiv.**
Failing branch	i_10065	--	100	100	no
Bridge		**Single Level I_{DDQ} Diagnosis**		**Multiple Levels I_{DDQ} Diagnosis**	
Net1	**Net2**	**M (%)**	**P (%)**	**β_1**	**R^2**
n_31021	Internal net	100	100	0.901	0.979

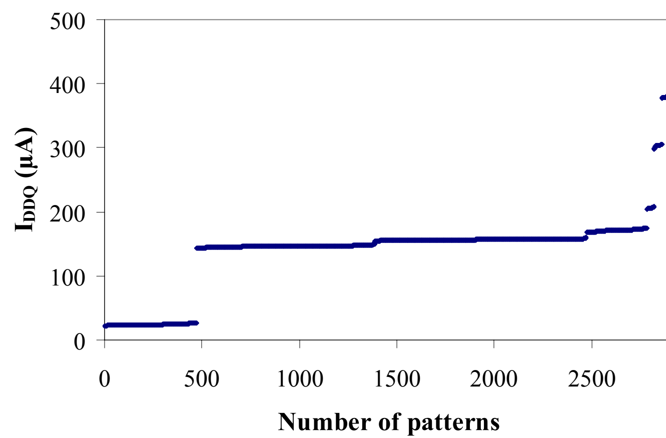

Figure A.9. Device 53 – Current signature.

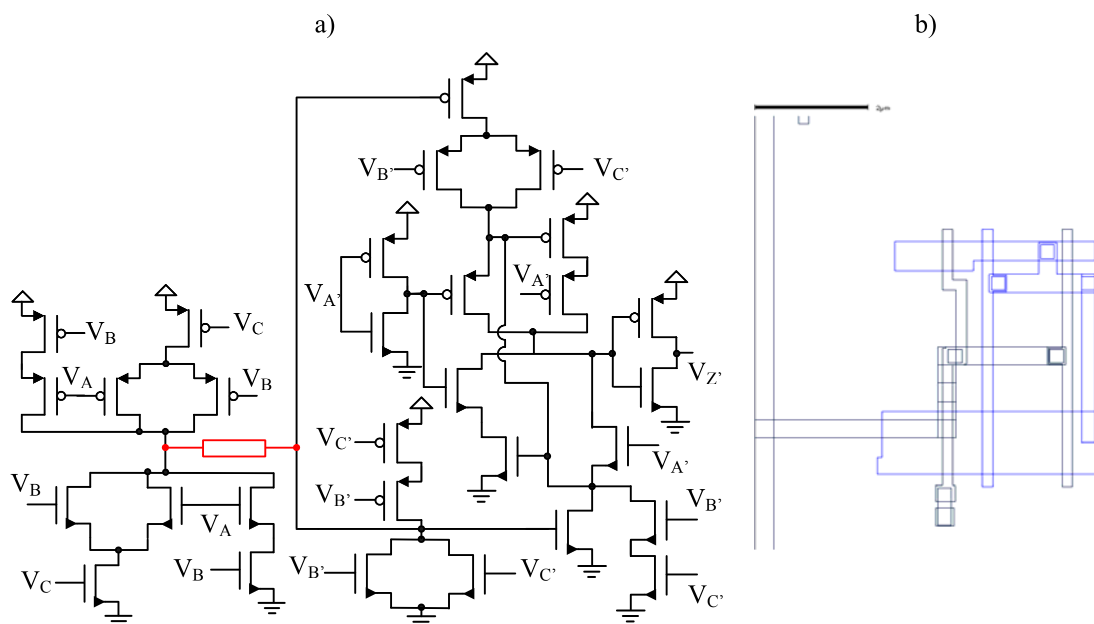

Figure A.10. Device 53 a) Transistor level b) Layout.

A.1.8. Device 60

TABLE A.VIII
DIAGNOSIS RESULTS FOR DEVICE 60

Logic Diagnosis (Faloc)					
FS1	**Net1**	**Net2**	**M (%)**	**P (%)**	**Equiv.**
SA	ASI_Q_7_	--	100	100	yes
Internal	i_357	--	100	100	--
Bridge		**Single Level I_{DDQ} Diagnosis**		**Multiple Levels I_{DDQ} Diagnosis**	
Net1	**Net2**	**M (%)**	**P (%)**	**β_1**	**R^2**
n_1455	Internal net	100	100	1.036	0.992

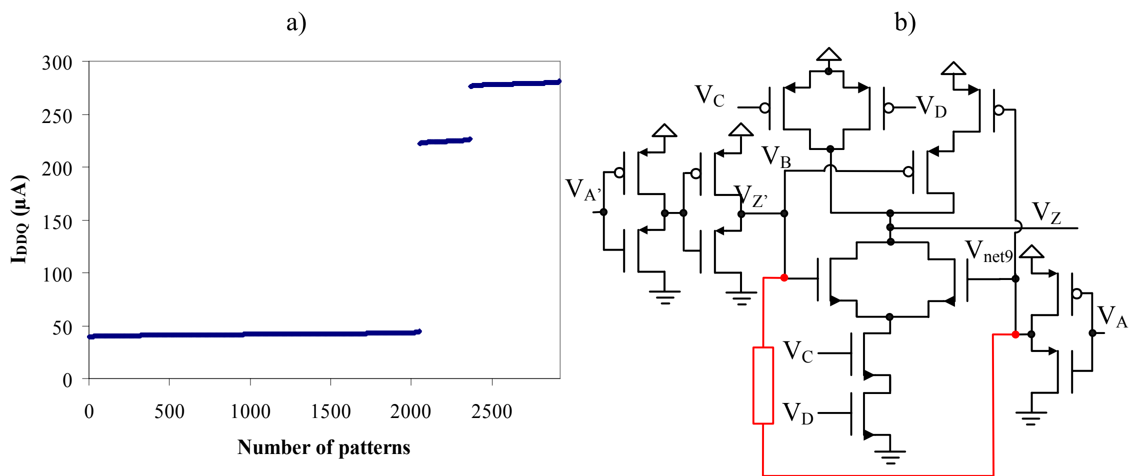

Figure A.11. Device 60 a) Current signature b) Transistor level.

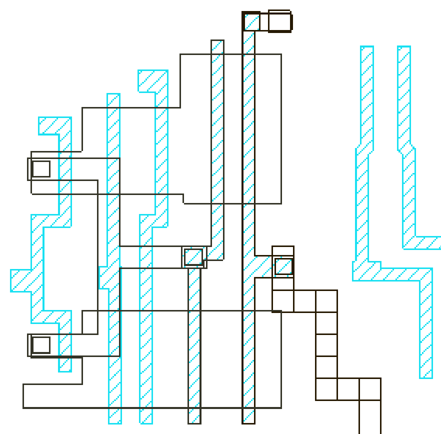

Figure A.12. Device 60 – Layout.

A.1.9. Device 68

TABLE A.IX
DIAGNOSIS RESULTS FOR DEVICE 68

Logic Diagnosis (Faloc)					
FS1	**Net1**	**Net2**	**M(%)**	**P(%)**	**Equiv.**
SA	n_21471	--	100	100	yes
SA	n_8913--	--	100	100	--
Bridge	n_21471	n_13705	100	100	--
Bridge	n_21471	n_17300	100	100	--
Bridge		**Single Level I_{DDQ} Diagnosis**		**Multiple Levels I_{DDQ} Diagnosis**	
Net1	**Net2**	**M(%)**	**P(%)**	**β_1**	**R^2**
n_21471	V_{DD}	100	100	1.007	0.999

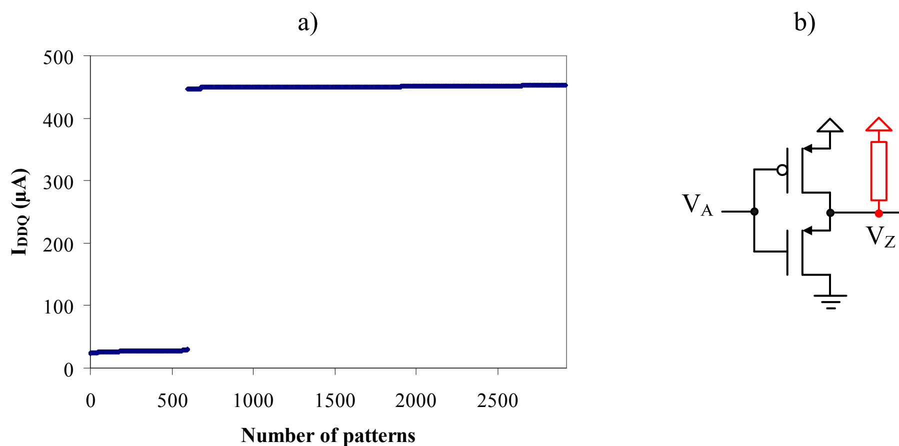

Figure A.13. Device 68 a) Current signature b) Transistor level.

A.1.10. Device 76

TABLE A.X
DIAGNOSIS RESULTS FOR DEVICE 76

Logic Diagnosis (Faloc)					
FS1	**Net1**	**Net2**	**M(%)**	**P(%)**	**Equiv.**
Bridge	XD_15_	n_9630	100	100	no
Bridge		**Single Level I_{DDQ} Diagnosis**		**Multiple Levels I_{DDQ} Diagnosis**	
Net1	**Net2**	**M(%)**	**P(%)**	**β_1**	**R^2**
XD_15_	n_9630	100	100	0.928	0.949

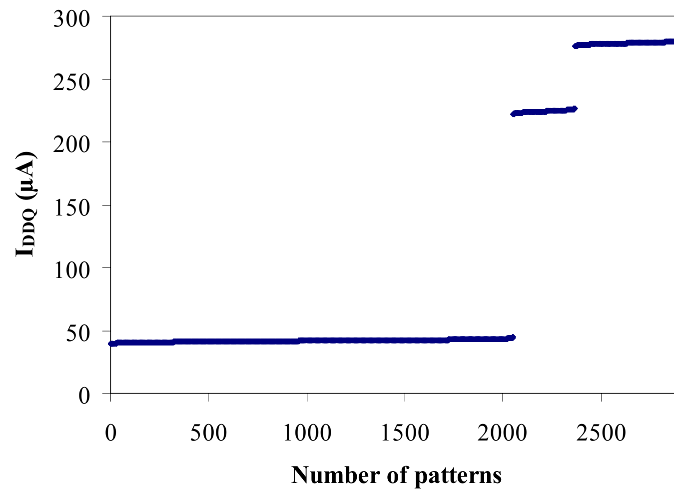

Figure A.14. Device 76 – Current signature.

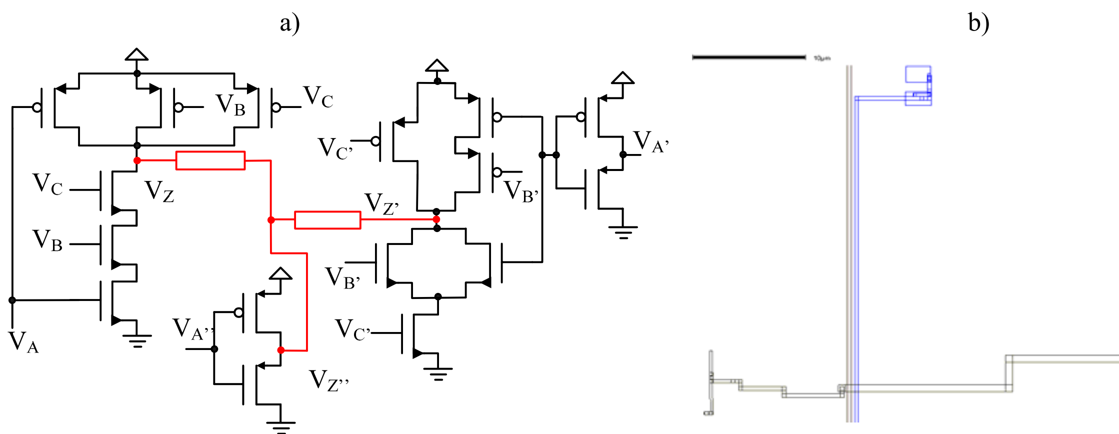

Figure A.15. Device 76 a) Transistor level b) Layout.

A.1.11. Device 78

TABLE A.XI
DIAGNOSIS RESULTS FOR DEVICE 78

Logic Diagnosis (Faloc)							
FS1	**Net1**	**Net2**	**M(%)**	**P(%)**		**Equiv.**	
Failing net	n_171560	--	100	100		yes	
Internal net	i_18097	--	100	100		yes	
Bridge		**Single Level I_{DDQ} Diagnosis**		**Multiple Level I_{DDQ} Diagnosis**			
Net1	**Net2**	**M(%)**	**P(%)**	**β_1**		**R^2**	
				V_{NOM}	**V_{VLV}**	**V_{NOM}**	**V_{VLV}**
n_171560	n_17536	100	100	1.091	1.133	0.968	0.999

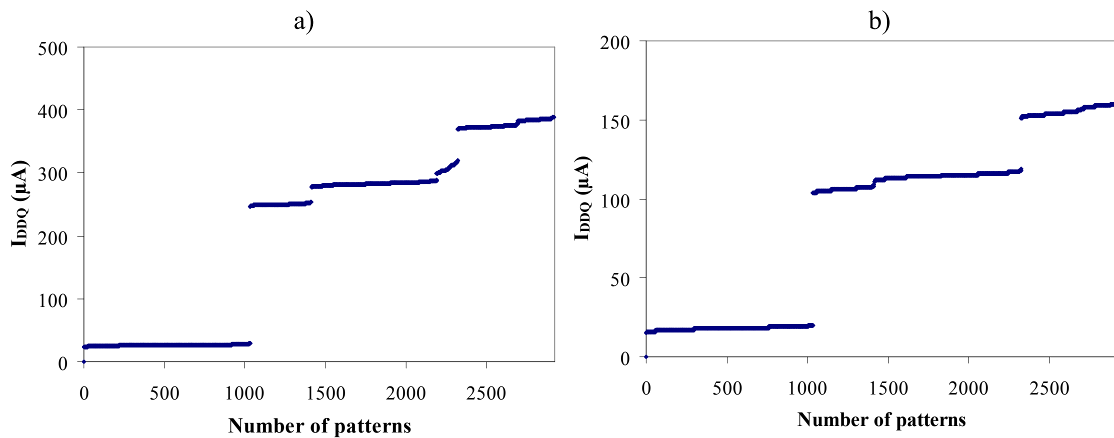

Figure A.16. Device 78 – Current signature a) V_{NOM} b) V_{VLV}.

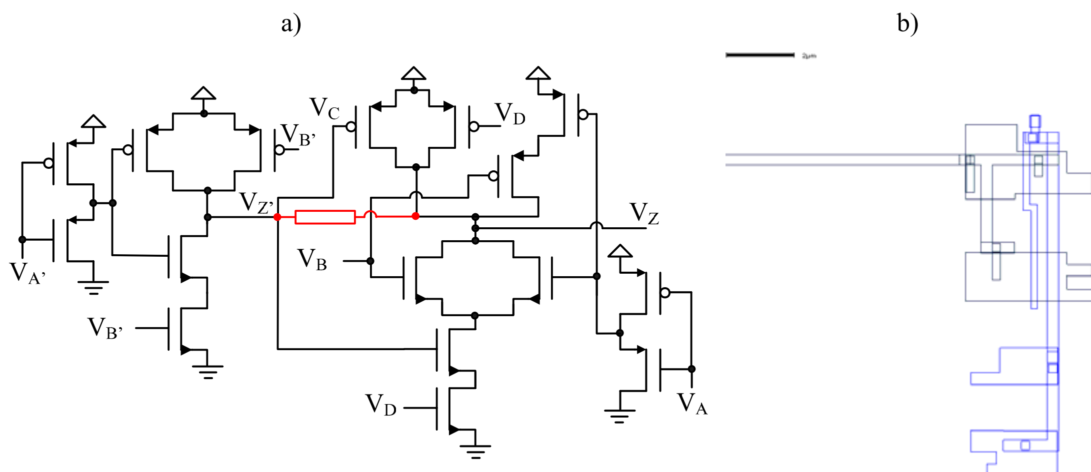

Figure A.17. Device 78 a) Transistor level b) Layout.

A.1.12. Device 80

TABLE A.XII
DIAGNOSIS RESULTS FOR DEVICE 80

Logic Diagnosis (Faloc)					
FS1	**Net1**	**Net2**	**M(%)**	**P(%)**	**Equiv.**
Bridge	n_21245	n_20695	100	100	No
Bridge		**Single Level I_{DDQ} Diagnosis**		**Multiple Levels I_{DDQ} Diagnosis**	
Net1	**Net2**	**M(%)**	**P(%)**	**β_1**	**R^2**
n_21245	n_20695	100	100	1.097	0.954

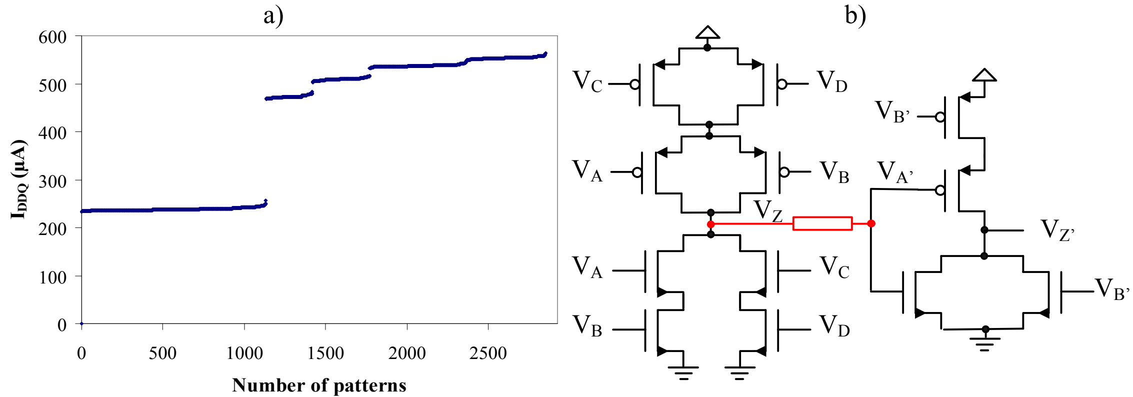

Figure A.18. Device 80 a) Current signature b) Transistor level.

Figure A.19. Device 80 - Layout.

A.1.13. Device 88

TABLE A.XIII
DIAGNOSIS RESULTS FOR DEVICE 88

Logic Diagnosis (Faloc)							
FS1	**Net1**	**Net2**	**M(%)**	**P(%)**		**Equiv.**	
Failing net	n_1688	--	99	96		No	
Bridge		**Single Level I_{DDQ} Diagnosis**		**Multiple Level I_{DDQ} Diagnosis**			
Net1	**Net2**	**M(%)**	**P(%)**	**β_1**		**R^2**	
				V_{NOM}	**V_{VLV}**	**V_{NOM}**	**V_{VLV}**
n_891	Internal net	100	100	3.901	3.426	0.892	0.963

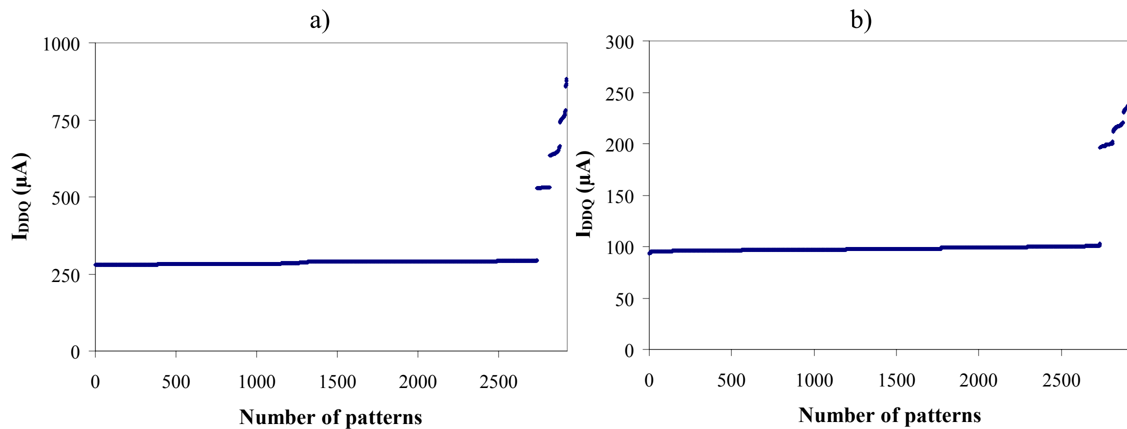

Figure A.20. Device 88 – Current signature a) V_{NOM} b) V_{VLV}.

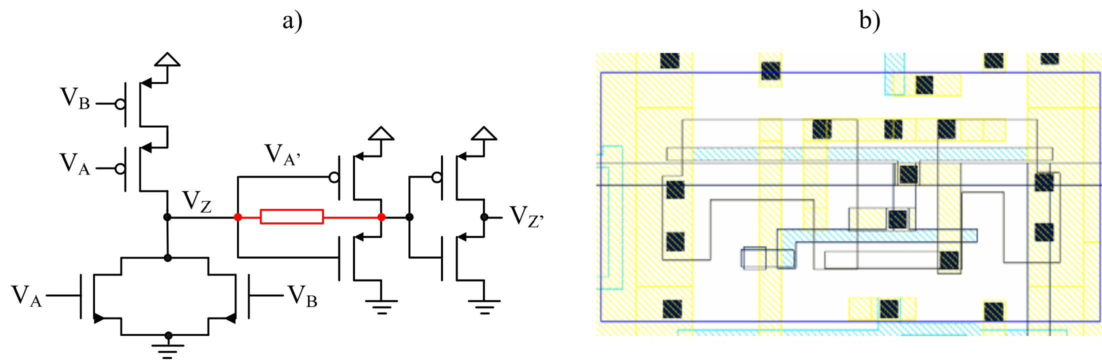

Figure A.21. Device 88 a) Transistor level b) Layout.

A.1.14. Device 92

TABLE A.XIV
DIAGNOSIS RESULTS FOR DEVICE 92

<table>
<tr><th colspan="8">Logic Diagnosis (Faloc)</th></tr>
<tr><th>FS1</th><th>Net1</th><th>Net2</th><th>M(%)</th><th colspan="2">P(%)</th><th colspan="2">Equiv.</th></tr>
<tr><td>Failing branch</td><td>n_6156</td><td>--</td><td>100</td><td colspan="2">100</td><td colspan="2">no</td></tr>
<tr><th colspan="2">Bridge</th><th colspan="2">Single Level I_{DDQ} Diagnosis</th><th colspan="4">Multiple Level I_{DDQ} Diagnosis</th></tr>
<tr><th rowspan="2">Net1</th><th rowspan="2">Net2</th><th rowspan="2">M(%)</th><th rowspan="2">P(%)</th><th colspan="2">β_1</th><th colspan="2">R^2</th></tr>
<tr><th>V_{NOM}</th><th>V_{VLV}</th><th>V_{NOM}</th><th>V_{VLV}</th></tr>
<tr><td>n_6156</td><td>n_16865</td><td>100</td><td>100</td><td>1.387</td><td>1.0543</td><td>0.842</td><td>0.997</td></tr>
</table>

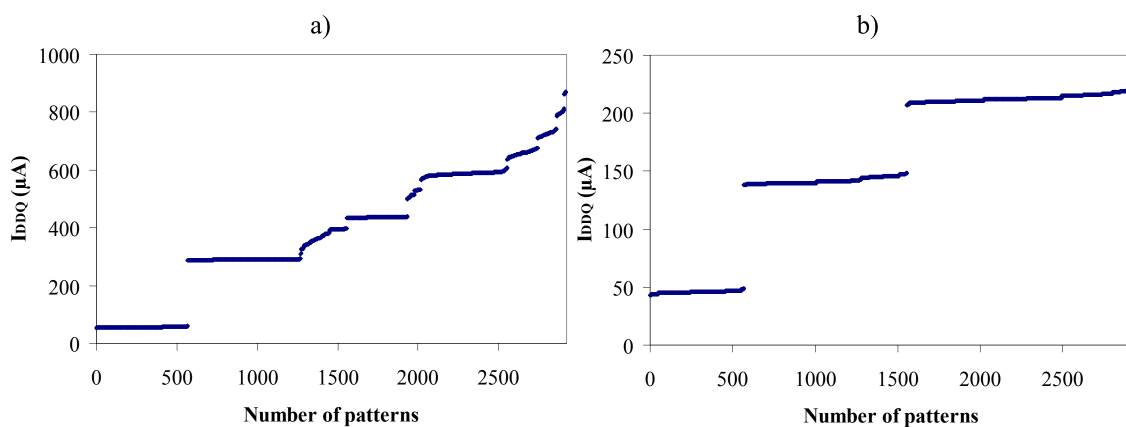

Figure A.22. Device 92 – Current signature a) V_{NOM} b) V_{VLV}.

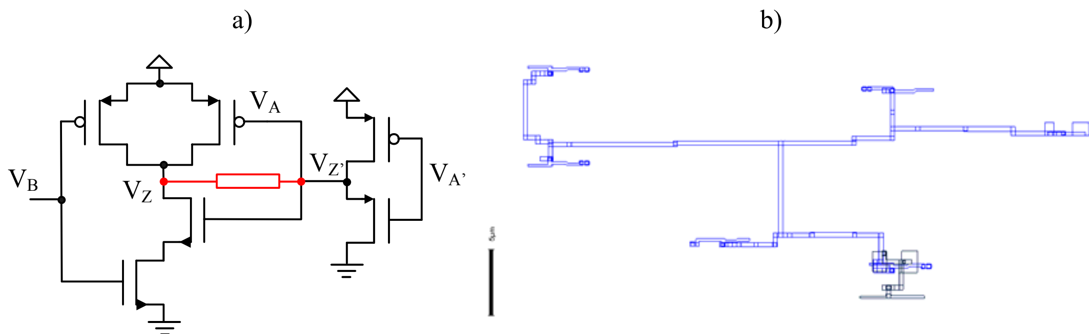

Figure A.23. Device 92 a) Transistor level b) Layout.

A.1.15. Device 101

TABLE A.XV
DIAGNOSIS RESULTS FOR DEVICE 101

Logic Diagnosis (Faloc)							
FS1	**Net1**	**Net2**	**M(%)**	**P(%)**		**Equiv.**	
Bridge	n_2112	n_2113	100	100		no	
Bridge		**Single Level I_{DDQ} Diagnosis**		**Multiple Level I_{DDQ} Diagnosis**			
Net1	**Net2**	**M(%)**	**P(%)**	**β_1**		**R^2**	
				V_{NOM}	**V_{VLV}**	**V_{NOM}**	**V_{VLV}**
n_2112	n_2113	100	100	1.375	1.165	0.810	0.999

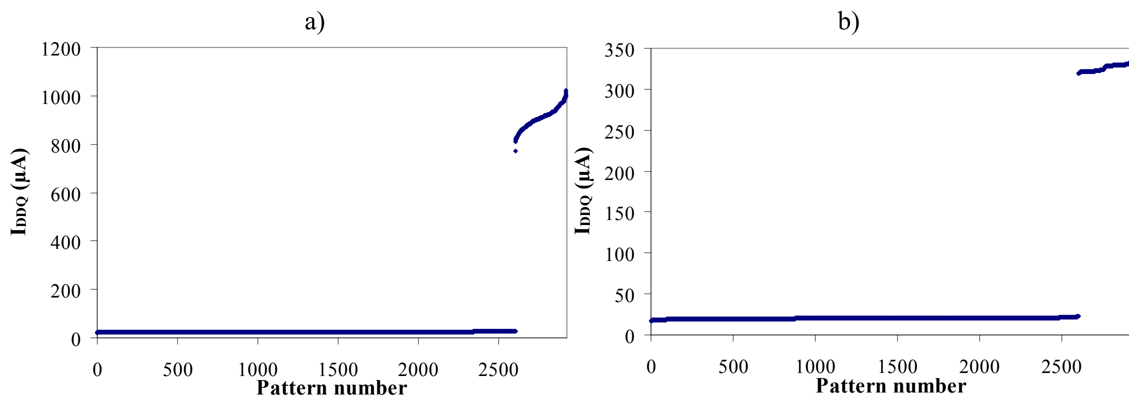

Figure A.24. Device 101 – Current signature a) V_{NOM} b) V_{VLV}.

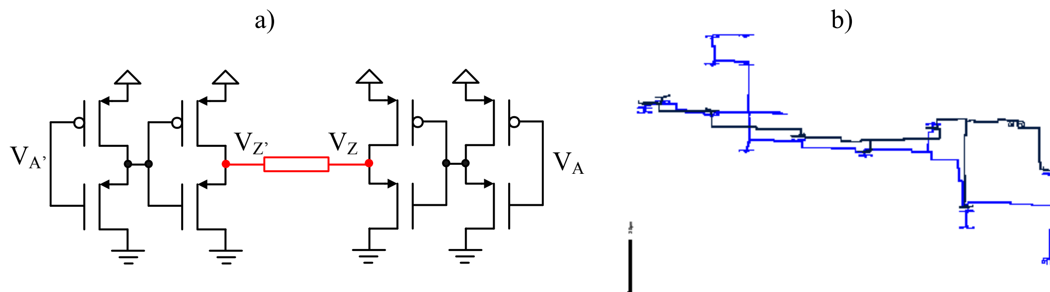

Figure A.25. Device 101 a) Transistor level b) Layout.

A.1.16. Device 112

Similar to Device 11, this device has another faulty core which is adding almost 3 mA of DC current.

TABLE A.XVI
DIAGNOSIS RESULTS FOR DEVICE 112

Logic Diagnosis (Faloc)					
FS1	**Net1**	**Net2**	**M(%)**	**P(%)**	**Equiv.**
SA	n_26512	--	100	100	Yes
Internal	i_123701	--	100	100	--
Bridge		**Single Level I_{DDQ} Diagnosis**		**Multiple Levels I_{DDQ} Diagnosis**	
Net1	**Net2**	**M(%)**	**P(%)**	**β_1**	**R^2**
n_26512	V_{GND}	100	100	1.094	0.999

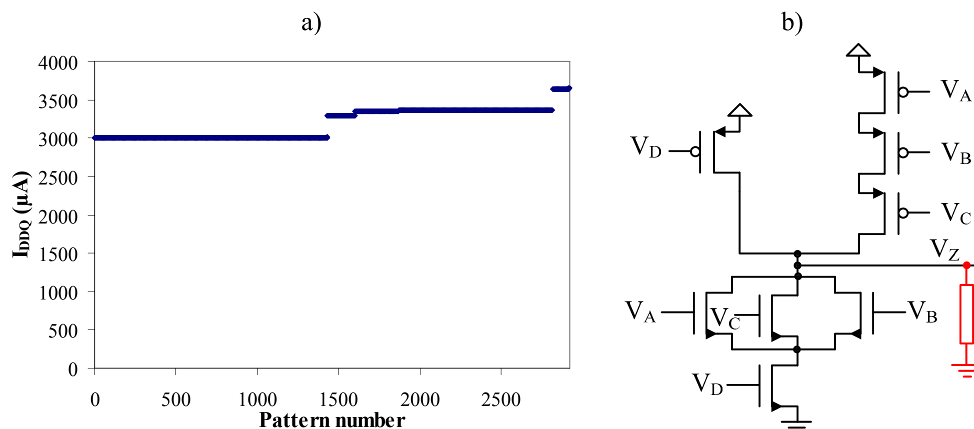

Figure A.26. Device 112 a) Current signature b) Transistor level.

A.1.17. Device 129

Similar to Device 11 and 112, this device has another faulty core which is adding DC current. However, in this case it is quite lower than in the other cases, just between 100-200 µA.

TABLE A.XVII
DIAGNOSIS RESULTS FOR DEVICE 129

Logic Diagnosis (Faloc)					
FS1	**Net1**	**Net2**	**M(%)**	**P(%)**	**Equiv.**
SA	n_26512	--	100	100	Yes
Internal	i_123701	--	100	100	--
Bridge		**Single Level I_{DDQ} Diagnosis**		**Multiple Levels I_{DDQ} Diagnosis**	
Net1	**Net2**	**M(%)**	**P(%)**	**β_1**	**R^2**
n_26512	V_{GND}	100	100	1.144	0.999

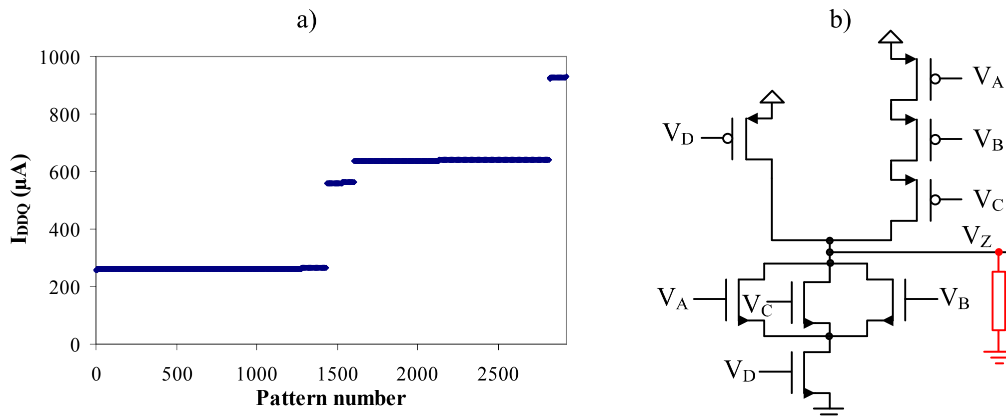

Figure A.27. Device 129 a) Current signature b) Transistor level.

A.1.18. Device 131

TABLE A.XVIII
DIAGNOSIS RESULTS FOR DEVICE 131

Logic Diagnosis (Faloc)					
FS1	**Net1**	**Net2**	**M(%)**	**P(%)**	**Equiv.**
SA	n_2918	--	100	100	yes
SA	n_25047	--	100	100	yes
Bridge		**Single Level I_{DDQ} Diagnosis**		**Multiple Levels I_{DDQ} Diagnosis**	
Net1	**Net2**	**M(%)**	**P(%)**	**β_1**	**R^2**
n_2918	V_{GND}	100	100	1.205	0.999

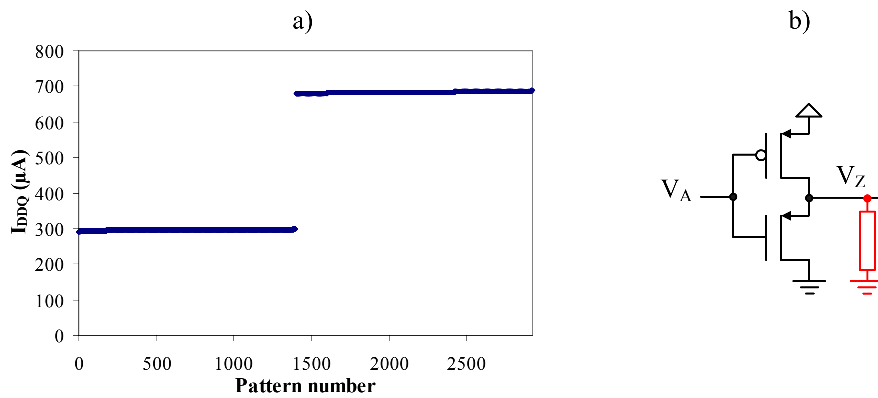

Figure A.28. Device 131 a) Current signature b) Transistor level.

A.1.19. Device 133

Notice that the bridging fault is the same one reported in Device 38.

TABLE A.XIX
DIAGNOSIS RESULTS FOR DEVICE 133

Logic Diagnosis (Faloc)					
FS1	**Net1**	**Net2**	**M(%)**	**P(%)**	**Equiv.**
Failing net	i_44133	--	100	52	yes
Failing net	n_553	--	100	52	--
Bridge		**Single Level I_{DDQ} Diagnosis**		**Multiple Levels I_{DDQ} Diagnosis**	
Net1	**Net2**	**M(%)**	**P(%)**	**β_1**	**R^2**
n_553	tq[6]	100	100	1.108	0.997

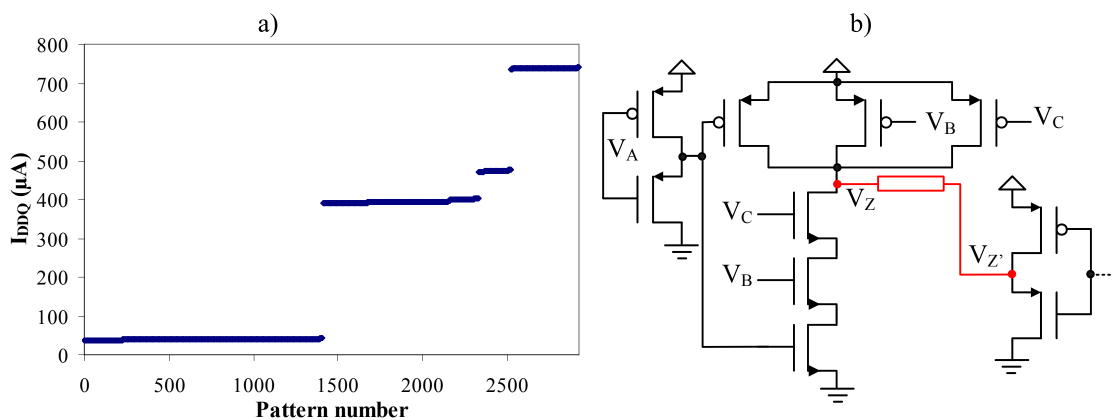

Figure A.29. Device 133 a) Current signature b) Transistor level.

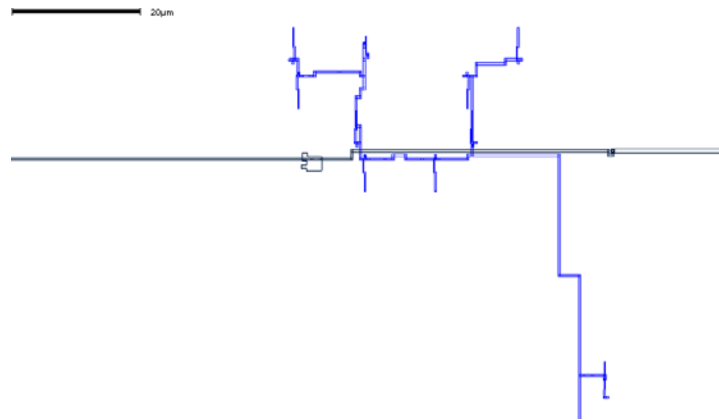

Figure A.30. Device 133 - Layout.

A.1.20. Device 144

The logic diagnosis reported 10 equivalent scenarios, halve of them also reported as SA faults and the rest as bridging faults. For ease of simplicity, they are not described in Table A.XX.

TABLE A.XX
DIAGNOSIS RESULTS FOR DEVICE 144

Logic Diagnosis (Faloc)					
FS1	**Net1**	**Net2**	**M(%)**	**P(%)**	**Equiv.**
SA	n_22488	--	100	100	yes
Bridge		**Single Level I_{DDQ} Diagnosis**		**Multiple Levels I_{DDQ} Diagnosis**	
Net1	**Net2**	**M(%)**	**P(%)**	**β_1**	**R^2**
n_22488	V_{DD}!	100	100	1.090	0.999

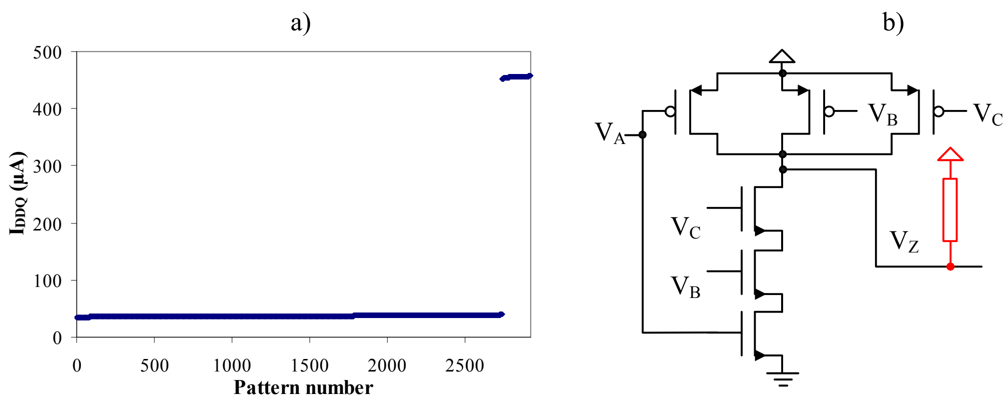

Figure A.31. Device 144 a) Current signature b) Transistor level.

A.1.21. Device 6b

TABLE A.XXI
DIAGNOSIS RESULTS FOR DEVICE 6B

Logic Diagnosis (Faloc)						
FS1	**Net1**		**Net2**	**M(%)**	**P(%)**	**Equiv.**
2 members	i_237210		n_6222	--	--	No
Bridge			**Single Level I_{DDQ} Diagnosis**		**Multiple Level I_{DDQ} Diagnosis**	
Net1	**Net2**	**Net3**	**M(%)**	**P(%)**	**β_1**	**R^2**
n_6315	n_6222	V_{GND}	100	100	1.200	0.999

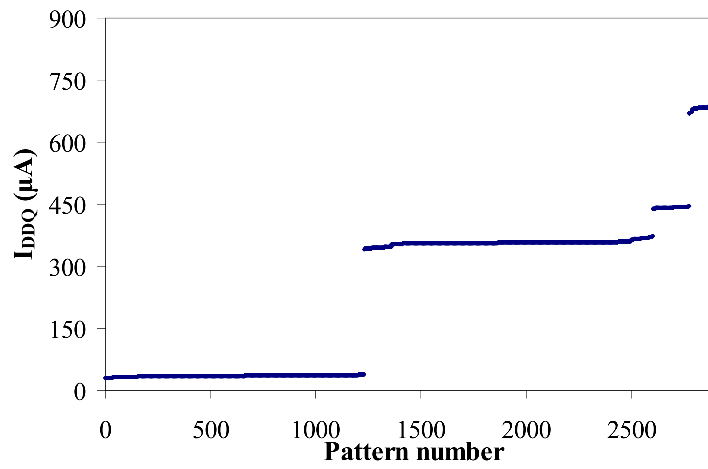

Figure A.32. Device 6b – Current signature.

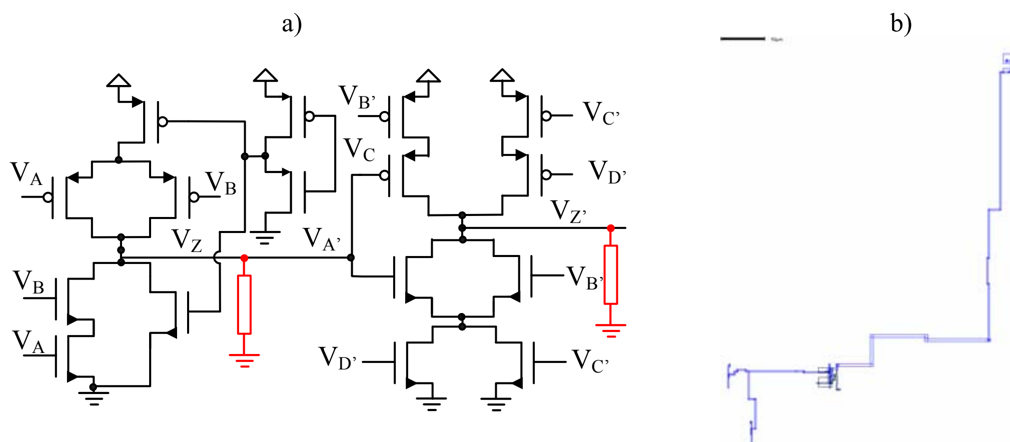

Figure A.33. Device 6b a) Transistor level b) Layout.

A.1.22. Device 9b

TABLE A.XXII
DIAGNOSIS RESULTS FOR DEVICE 9B

Logic Diagnosis (Faloc)					
FS1	Net1	Net2	M(%)	P(%)	Equiv.
Bridge	n_25307	n_25311	100	50	no

Bridge			Single Level I_{DDQ} Diagnosis		Multiple Level I_{DDQ} Diagnosis			
					β_1		R^2	
Net1	Net2	Net3	M(%)	P(%)	V_{NOM}	V_{VLV}	V_{NOM}	V_{VLV}
n_25307	n_25311	100	100	100	2.147	1.546	0.940	0.969

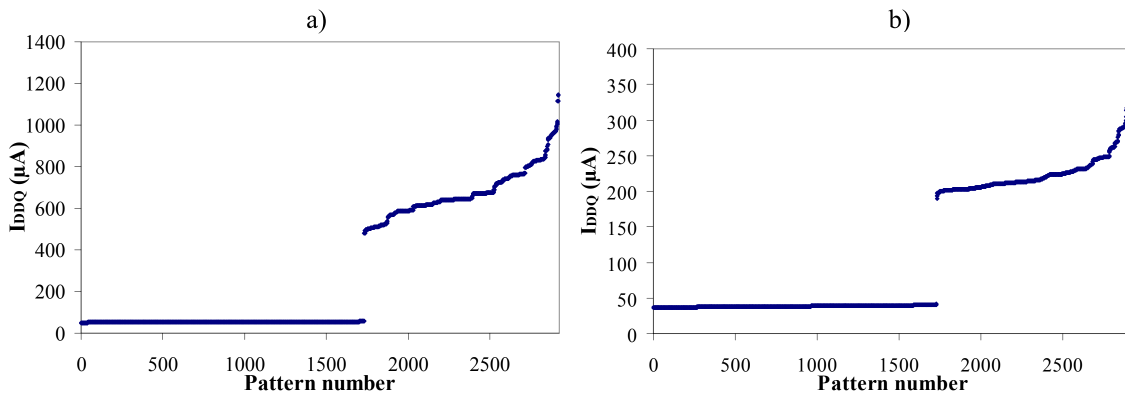

Figure A.34. Device 9b – Current signature a) V_{NOM} b) V_{VLV}.

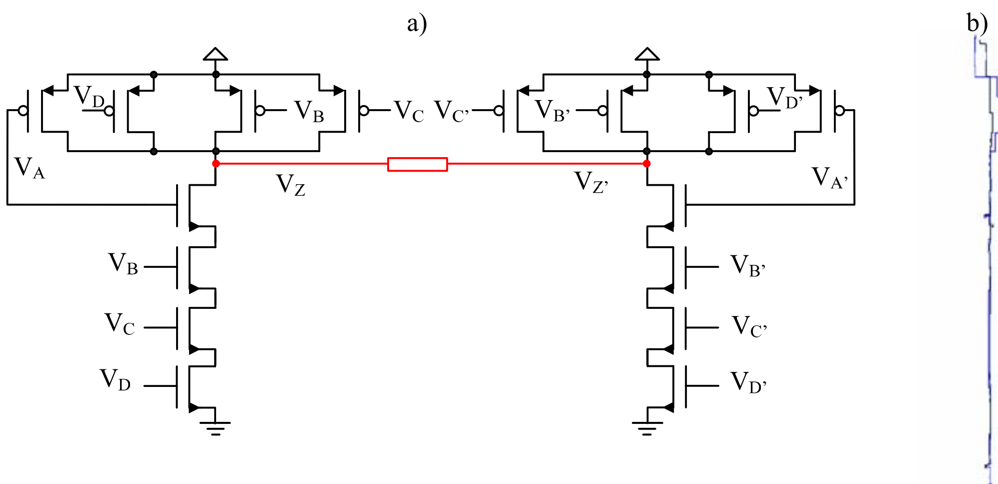

Figure A.35. Device 9b a) Transistor level b) Layout.

A.1.23. Device 14b

TABLE A.XXIII
DIAGNOSIS RESULTS FOR DEVICE 14B

<table>
<tr><th colspan="9">Logic Diagnosis (Faloc)</th></tr>
<tr><th>FS1</th><th colspan="2">Net1</th><th>Net2</th><th>M(%)</th><th colspan="2">P(%)</th><th colspan="2">Equiv.</th></tr>
<tr><td>SA</td><td colspan="2">n_711</td><td>--</td><td>100</td><td colspan="2">100</td><td colspan="2">yes</td></tr>
<tr><td>Bridge</td><td colspan="2">n_711</td><td>n_712</td><td>100</td><td colspan="2">100</td><td colspan="2">--</td></tr>
<tr><td>Bridge</td><td colspan="2">n_711</td><td>n_405</td><td>100</td><td colspan="2">100</td><td colspan="2">--</td></tr>
<tr><th colspan="3">Bridge</th><th colspan="2">Single Level I_{DDQ} Diagnosis</th><th colspan="4">Multiple Level I_{DDQ} Diagnosis</th></tr>
<tr><th rowspan="2">Net1</th><th rowspan="2">Net2</th><th rowspan="2">Net3</th><th rowspan="2">M(%)</th><th rowspan="2">P(%)</th><th colspan="2">β_1</th><th colspan="2">R^2</th></tr>
<tr><th>V_{NOM}</th><th>V_{VLV}</th><th>V_{NOM}</th><th>V_{VLV}</th></tr>
<tr><td>n_711</td><td>V_{DD}</td><td>100</td><td>100</td><td>100</td><td>1.256</td><td>1.098</td><td>0.880</td><td>0.901</td></tr>
</table>

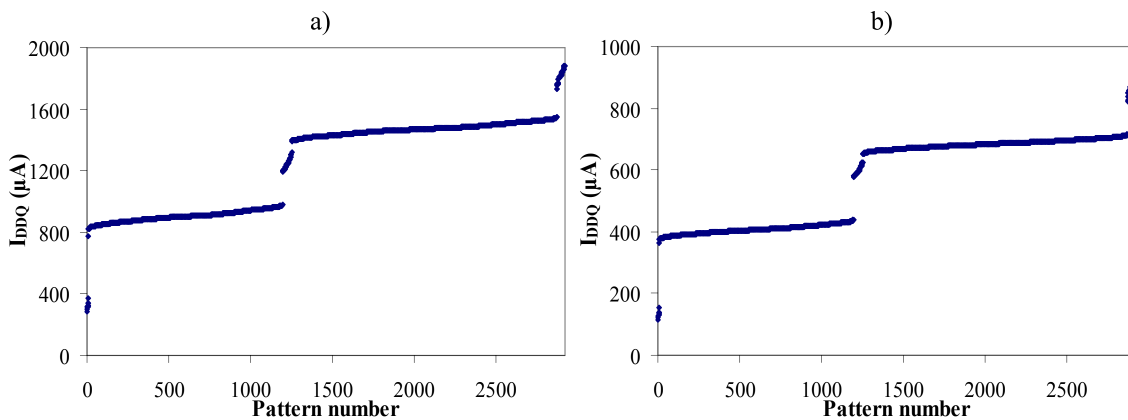

Figure A.36. Device 14b – Current signature a) V_{NOM} b) V_{VLV}.

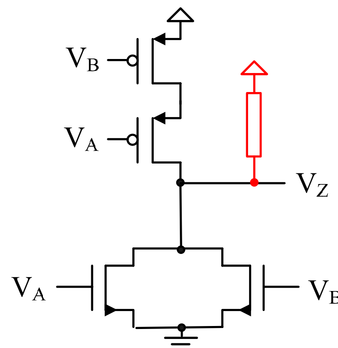

Figure A.37. Device 14b - Transistor level.

A.1.24. Device 21b

TABLE A.XXIV
DIAGNOSIS RESULTS FOR DEVICE 21B

Logic Diagnosis (Faloc)					
FS1	**Net1**	**Net2**	**M(%)**	**P(%)**	**Equiv.**
SA	n_5076	--	100	100	no

Bridge			Single Level I_{DDQ} Diagnosis		Multiple Level I_{DDQ} Diagnosis			
					β_1		R^2	
Net1	**Net2**	**Net3**	**M(%)**	**P(%)**	V_{NOM}	V_{VLV}	V_{NOM}	V_{VLV}
n_5076	V_{DD}	100	100	100	1.092	1.050	0.999	0.999

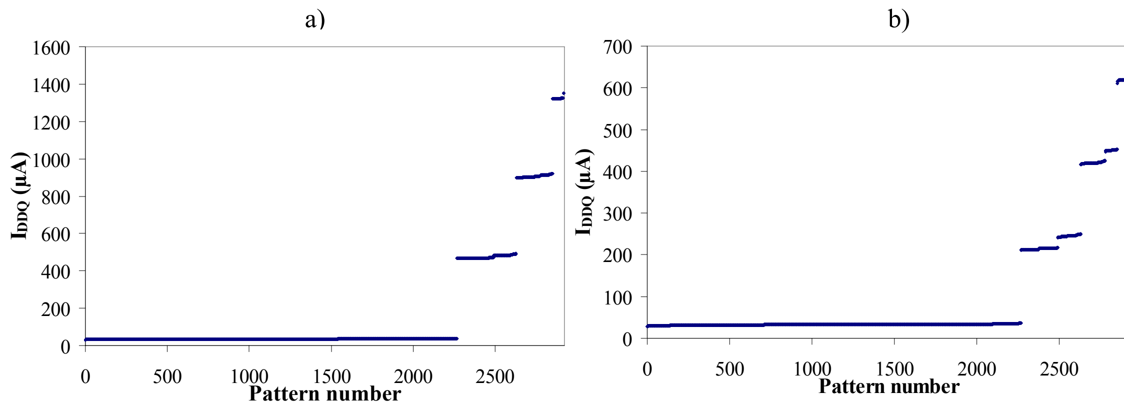

Figure A.38. Device 21b – Current signature a) V_{NOM} b) V_{VLV}.

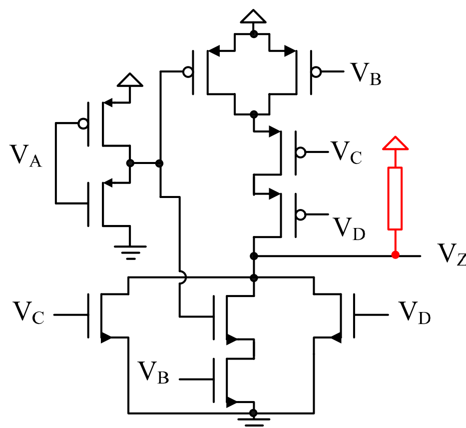

Figure A.39.Device 21b - Transistor level.

A.1.25. Device 36b

TABLE A.XXV
DIAGNOSIS RESULTS FOR DEVICE 36B

Logic Diagnosis (Faloc)					
FS1	**Net1**	**Net2**	**M(%)**	**P(%)**	**Equiv.**
Bridge	n_1438	DSP.ZI_3_	94	100	no
Bridge		**Single Level I_{DDQ} Diagnosis**		**Multiple Levels I_{DDQ} Diagnosis**	
Net1	**Net2**	**M(%)**	**P(%)**	**β_1**	**R^2**
n_1438	DSP.ZI_3_	100	100	1.171	0.999

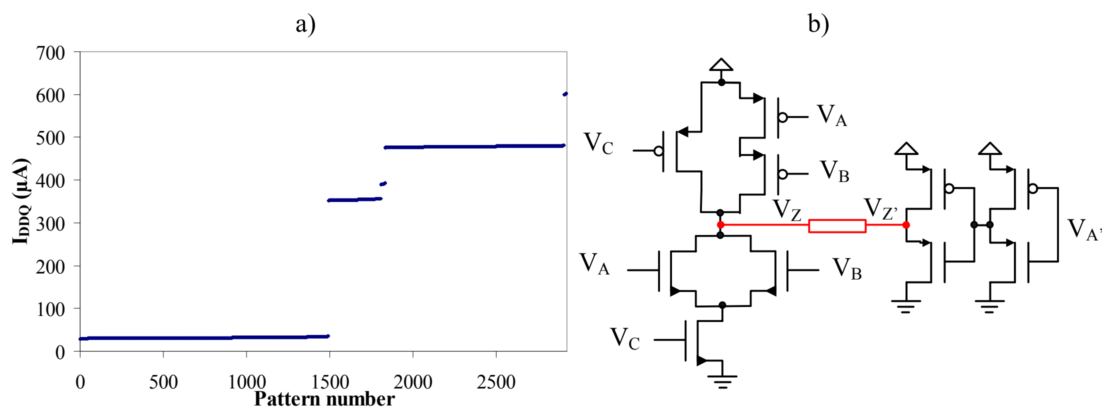

Figure A.40. Device 36b a) Current signature b) Transistor level.

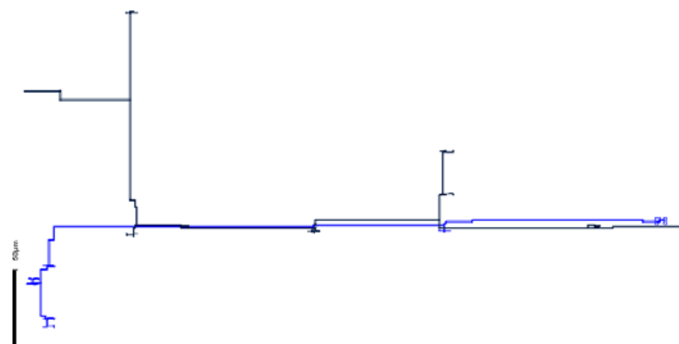

Figure A.41. Device 36b - Layout

A.2 90 nm Technology *Devices*

The 90 nm technology devices from *NXP Semiconductors* considered in this work are used for mobile phone applications. This technology comprises six metal layers. The number of pins of the samples exceeds the capability of the HP82000 tester placed in the *Electronic Engineering Department* of the *UPC*. Thus, both logic and current tests have been carried out by *NXP Semiconductors* with an Agilent 93000 tester. The cores

did not pass the SA test. The logic tests have been applied at V_{MAX} (1.32 V) at two different temperatures (room and high temperature) and for some of them also at V_{VLV} (0.9 V). Furthermore, some of these tests have been applied twice to see if there is repeatability on the results.

Similar to the *Vector4* devices, a summary of the results of the bridging faults diagnosed with the multiple level I_{DDQ} based diagnosis is presented next.

A.2.1. Device 1

This device is reported with more than 14 internal equivalent faults, which are not described in Table A.XXVI

TABLE A.XXVI
DIAGNOSIS RESULTS FOR DEVICE 1

Logic Diagnosis (Faloc)					
FS1	**Net1**	**Net2**	**M (%)**	**P (%)**	**Equiv.**
SA	n_14341	--	100	96	yes
Bridge		**Single Level I_{DDQ} Diagnosis**		**Multiple Levels I_{DDQ} Diagnosis**	
Net1	**Net2**	**M (%)**	**P (%)**	**β_1**	**R^2**
n_14193	n_14268	100	100	0.821	0.998

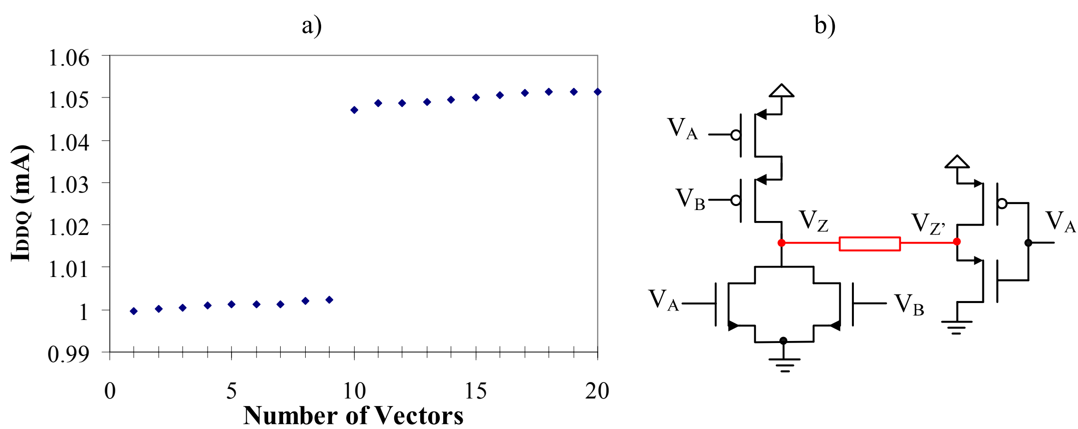

Figure A.42. Device 1 a) Current signature b) Transistor level.

A.2.2. Device 2

TABLE A.XXVII
DIAGNOSIS RESULTS FOR DEVICE 2

Logic Diagnosis (Faloc)					
FS1	**Net1**	**Net2**	**M (%)**	**P (%)**	**Equiv.**
SA	n_47712	--	100	100	yes
SA	n_47707	--	100	100	--
Internal	i_69746	--	100	100	--
Bridge		**Single Level I_{DDQ} Diagnosis**		**Multiple Levels I_{DDQ} Diagnosis**	
Net1	**Net2**	**M (%)**	**P (%)**	**β_1**	**R^2**
internal	V_{GND}	100	100	1.025	0.990

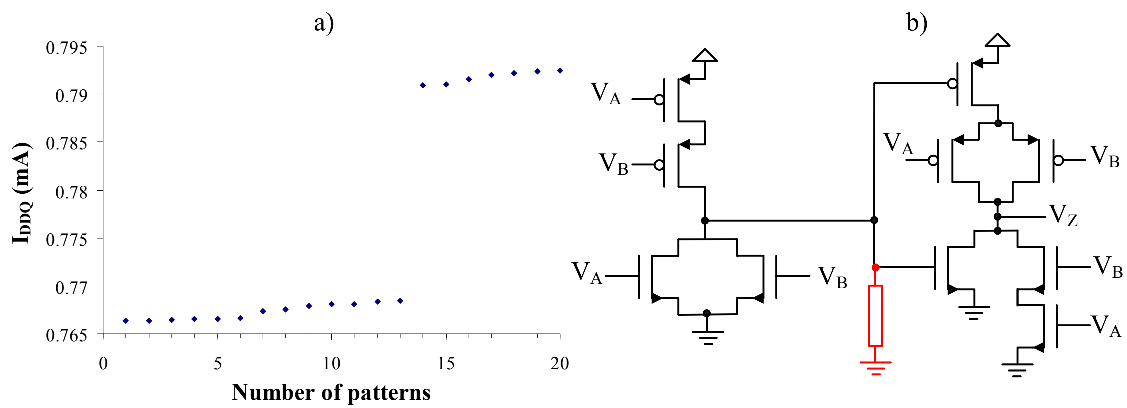

Figure A.43. Device 2 a) Current signature b) Transistor level.

A.2.3. Device 3

TABLE A.XXVIII
DIAGNOSIS RESULTS FOR DEVICE 3

Logic Diagnosis (Faloc)					
FS1	**Net1**	**Net2**	**M (%)**	**P (%)**	**Equiv.**
SA	n_39151	--	100	100	no
Bridge		**Single Level I_{DDQ} Diagnosis**		**Multiple Levels I_{DDQ} Diagnosis**	
Net1	**Net2**	**M (%)**	**P (%)**	**β_1**	**R^2**
internal	V_{GND}	100	100	1.118	0.990

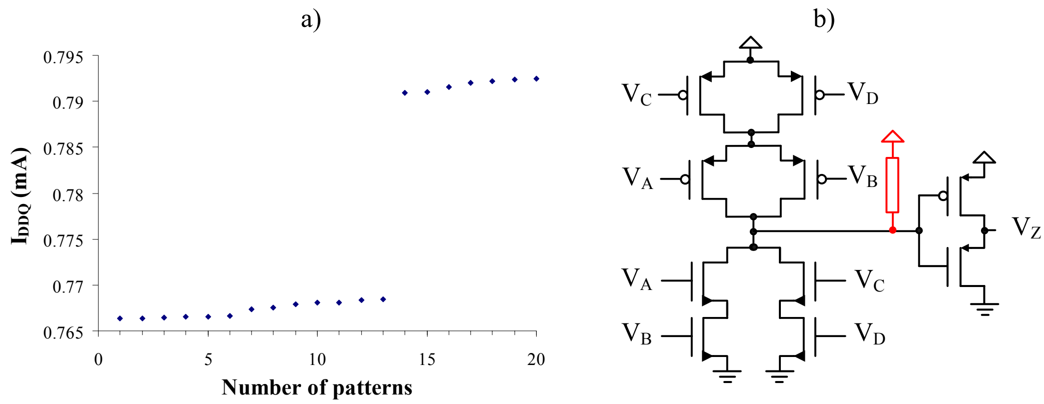

Figure A.44. Device 3 a) Current signature b) Transistor level.

A.2.4. Device 4

TABLE A.XXIX
DIAGNOSIS RESULTS FOR DEVICE 4

Logic Diagnosis (Faloc)					
FS1	**Net1**	**Net2**	**M(%)**	**P(%)**	**Equiv.**
SA	n_015	--	100	100	yes
internal	i_025	--	100	100	--
Bridge		**Single Level I_{DDQ} Diagnosis**		**Multiple Levels I_{DDQ} Diagnosis**	
Net1	**Net2**	**M(%)**	**P(%)**	**β_1**	**R^2**
Internal	V_{GND}	100	100	1.029	0.990

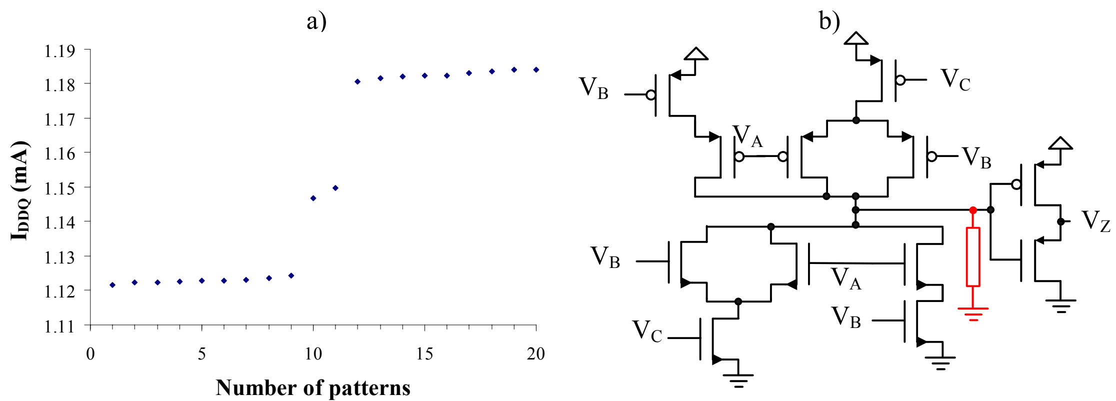

Figure A 45. Device 4 a) Current signature b) Transistor level.

A.2.5. Device 5

TABLE A.XXX
DIAGNOSIS RESULTS FOR DEVICE 5

Logic Diagnosis (Faloc)					
FS1	**Net1**	**Net2**	**M(%)**	**P(%)**	**Equiv.**
SA	z_3x[4]	--	100	100	no
Bridge		**Single Level I_{DDQ} Diagnosis**		**Multiple Levels I_{DDQ} Diagnosis**	
Net1	**Net2**	**M(%)**	**P(%)**	**β_1**	**R^2**
internal	V_{GND}	100	100	1.025	0.996

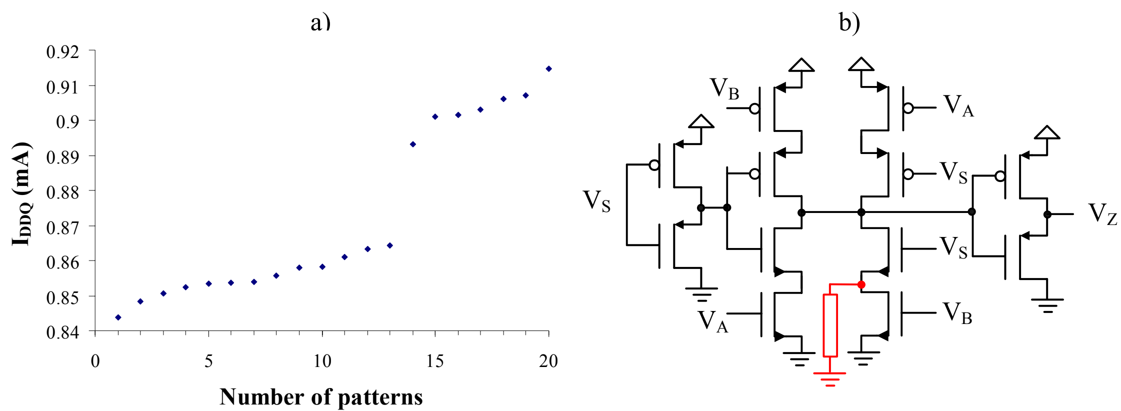

Figure A 46. Device 5 a) Current signature b) Transistor level.

A.2.6. Device 6

TABLE A.XXXI
DIAGNOSIS RESULTS FOR DEVICE 6

Logic Diagnosis (Faloc)					
FS1	**Net1**	**Net2**	**M(%)**	**P(%)**	**Equiv.**
SA	n_38171	--	100	100	no
Bridge		**Single Level I_{DDQ} Diagnosis**		**Multiple Levels I_{DDQ} Diagnosis**	
Net1	**Net2**	**M(%)**	**P(%)**	**β_1**	**R^2**
n_38171	V_{DD}	100	100	0.890	0.999

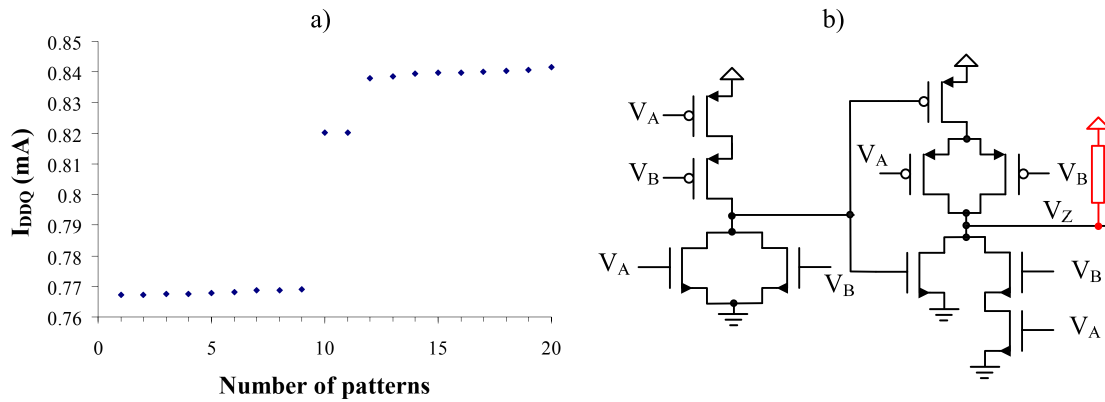

Figure A 47. Device 6 a) Current signature b) Bridge.

A.2.7. Device 7

TABLE A.XXXII
DIAGNOSIS RESULTS FOR DEVICE 7

Logic Diagnosis (Faloc)					
FS1	**Net1**	**Net2**	**M(%)**	**P(%)**	**Equiv.**
Bridge	n_4896_10	/reg_2	100	72	No
Bridge		**Single Level I_{DDQ} Diagnosis**		**Multiple Levels I_{DDQ} Diagnosis**	
Net1	**Net2**	**M(%)**	**P(%)**	**β_1**	**R^2**
n_4896_10	/_reg_2	100	100	0.980	0.995

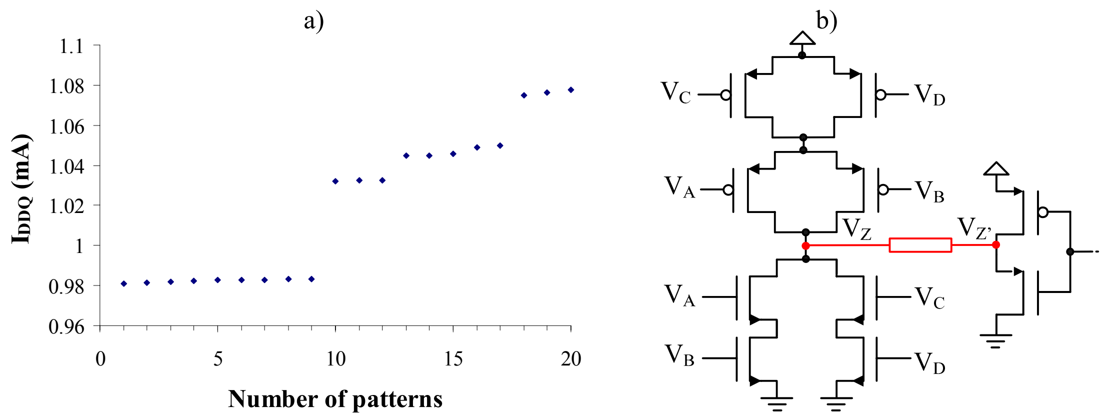

Figure A 48. Device 7 a) Current signature b) Transistor level.

A.2.8. Device 8

TABLE A.XXXIII
DIAGNOSIS RESULTS FOR DEVICE 8

Logic Diagnosis (Faloc)					
FS1	**Net1**	**Net2**	**M(%)**	**P(%)**	**Equiv.**
Bridge	web_neg	n_5801	100	100	no
Bridge		**Single Level I_{DDQ} Diagnosis**		**Multiple Levels I_{DDQ} Diagnosis**	
Net1	**Net2**	**(%)**	**P(%)**	**β_1**	**R^2**
web_neg	n_5801	100	100	1.055	0.999

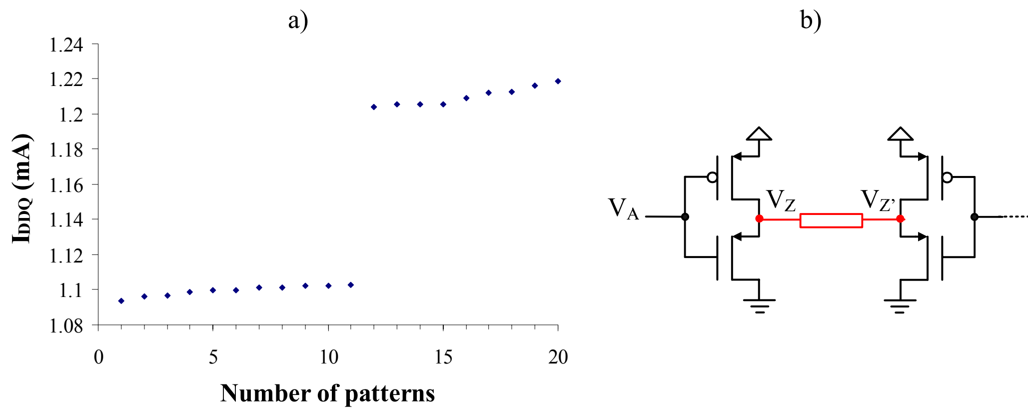

Figure A 49. Device 8 a) Current signature b) Transistor level.

A.2.9. Device 9

TABLE A.XXXIV
DIAGNOSIS RESULTS FOR DEVICE 9

Logic Diagnosis (Faloc)					
FS1	**Net1**	**Net2**	**M(%)**	**P(%)**	**Equiv.**
Failing net	n_9455_16	---		11	no
Bridge		**Single Level I_{DDQ} Diagnosis**		**Multiple Levels I_{DDQ} Diagnosis**	
Net1	**Net2**	**M(%)**	**P(%)**	**β_1**	**R^2**
n_9455_16	n_10001_16	100	100	0.87	0.996

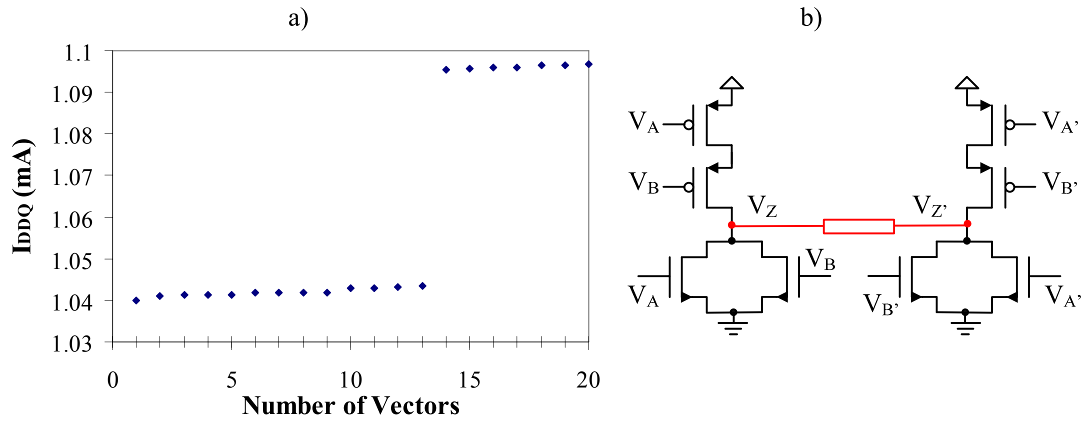

Figure A 50. Device 9 a) Current signature b) Transistor level.

A.2.10. Device 10

TABLE A.XXXV
DIAGNOSIS RESULTS FOR DEVICE 10

Logic Diagnosis (Faloc)					
FS1	**Net1**	**Net2**	**M(%)**	**P(%)**	**Equiv.**
Failing net	n_14636	--	100	100	no
Bridge		**Single Level I_{DDQ} Diagnosis**		**Multiple Levels I_{DDQ} Diagnosis**	
Net1	**Net2**	**M(%)**	**P(%)**	**β_1**	**R^2**
n_14636	internal	100	100	0.977	0.978

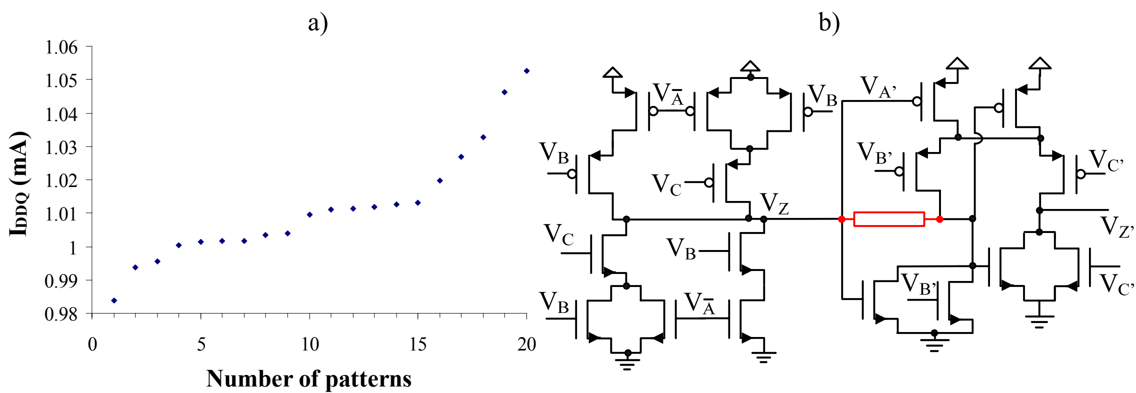

Figure A 51. Device 10 a) Current signature b) Transistor level.

A.2.11. Device 11

TABLE A.XXXVI
DIAGNOSIS RESULTS FOR DEVICE 11

Logic Diagnosis (Faloc)					
FS1	Net1	Net2	M(%)	P(%)	Equiv.
Bridge	n_10789	n_10489	100	55	no
Bridge		Single Level I_{DDQ} Diagnosis		Multiple Levels I_{DDQ} Diagnosis	
Net1	Net2	M(%)	P(%)	β_1	R^2
n_10789	n_10489	100	100	0.964	0.998

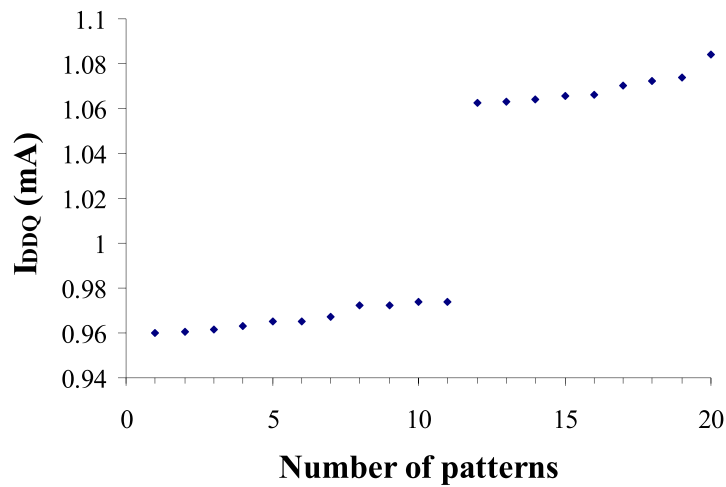

Figure A 52. Device 11 – Current signature

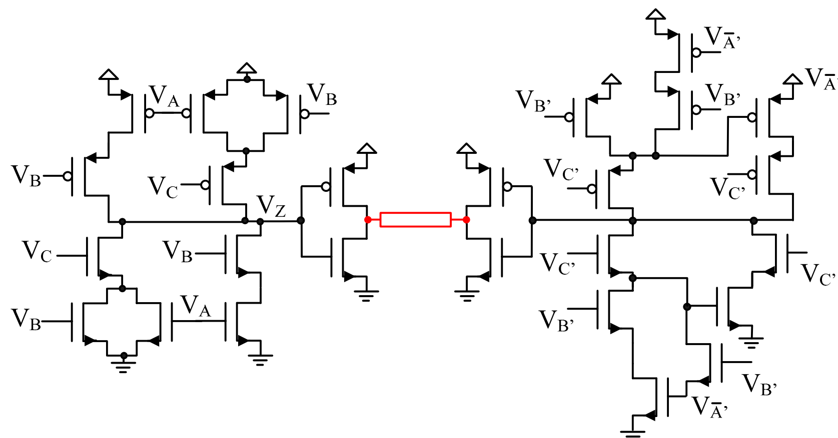

Figure A 53. Device 11 - Transistor level.

ANNEX B. HARDWARE AND SOFTWARE INFORMATION

This annex summarizes the main features of the instrumentation and software used during the development of the thesis.

B.1 Tester

In production mode, testing and measurements are performed using a test system or platform, consisting of a tester and sometimes, a handler. The tester performs the electrical testing itself, while the handler, if exists, takes care of transferring the unit to the test site and positioning it for testing, as well as reloading it back after the testing process is completed. This test system is also called automatic test equipment (ATE). The testing process executed by the tester is controlled by the test program or test

software. It tells the tester the electrical excitation which needs to be applied to the DUT, as well as the correct timing of applying them. ATE consists of various instruments or cards used for testing memory, digital, mixed signal and SOC (System On Chip) components, both at the wafer and packaged stages.

B.1.1. HP82000

During the work of this thesis, two HP82000 testers have been used (see Figure B.1). The main different between them is that one has only one mainframe while the second tester has two mainframes. The main characteristics of both testers are summarized in Table B.1. The HP82000 tester has a per-pin architecture. This means that each channel has its own timing and level generation for both the drive and the receive sides.

Figure B.1. HP82000 tester

TABLE B.I
TESTER INFORMATION

Features	Tester 1	Tester2
Mainframes	2	1
Channels	120	88
Power Supplies	2	2
Power Supply pins	8	8
Power supplies model	HP6624A	HP6626A
Vector memory	64 k	1 M
Boards	100 MHz	100 MHz
Receive data memory	256 k	256 k

The testing process is controlled from a workstation, where the test software is launched. The interface between the workstation and the mainframe is carried out by means of the HP-IB interface bus. The software of the HP82000 allows you to work both interactively and programmatic.

B.1.2. DUT Interface

The load board and the DUT (or piggy) board (Figure B.2) provide the interface between the ATE and the DUT. The design of these boards must satisfy three goals: enable testing the DUT as defined in the test plan, minimize distortion of the DUT's performance, and be flexible enough to handle future test needs.

The load board usually consists of a printed circuit board (PCB) with contactors, which holds the DUT board. The DUT board, which is mounted on the load board, is a smaller PCB, which contains a socket or contactor holding the DUT. The load board is more or less a standard board, so that it can be used for different types of ICs. However, the DUT board is usually customized, so that it is only useful for a specific IC. Furthermore, in the case of the tests carried out for the *Vector4* devices, there is another board, the V_{DD} board. Its features is similar to the DUT board, it is mounted on the load board. However, it takes care of the connections to power supplies and ground.

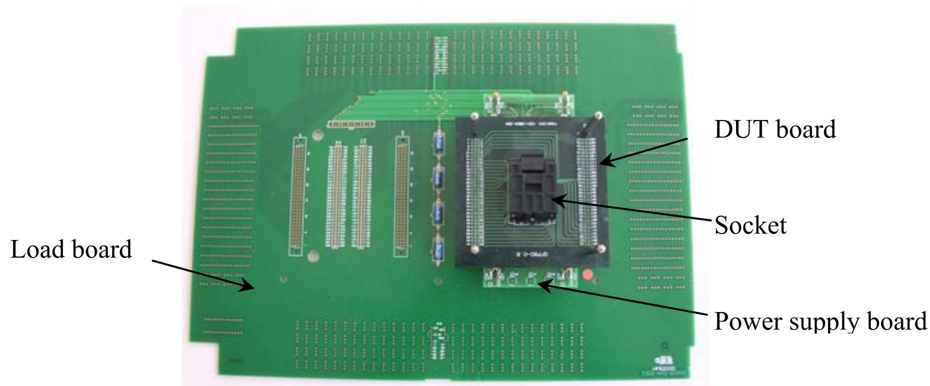

Figure B.2. Boards

B.1.3. Agilent 93000

As the number of pins of the 90 nm technology devices exceeds the number of channels of the HP82000, it is not possible to test it with such tester. Therefore, a more advance ATE was used to test these samples, the Agilent 93000, see Figure B.3. There are many improvements related to the HP82000, it has more channels, more flexibility, improved software, it allows faster clock frequency and it has water cooling.

Figure B.3. Agilent 93000 tester

B.2 Climate chamber

The climate chamber *Dycometal CCK-81* (see Figure B.4a) has been used for testing the devices at different temperatures. The temperature chamber cannot be used directly. Some kind of interface is required to take the DUT inside the temperature chamber or extract the temperature conditions chamber to the DUT. Eventually, the second option has been considered as the proper one. A hermetic methacrylate box has been built in order to isolate the DUT from the environment. Two isolating tubes are connected between the temperature chamber and the methacrylate box. One tube allows the air from the climate chamber reaching the methacrylate box. The other tube is the returning path to increase system efficiency. An air compressor inside the temperature chamber facilitates the air flowing. Furthermore, a thermometer is placed inside the Methacrylate box to control the temperature of the DUT. A system diagram is depicted in Figure B.4b.

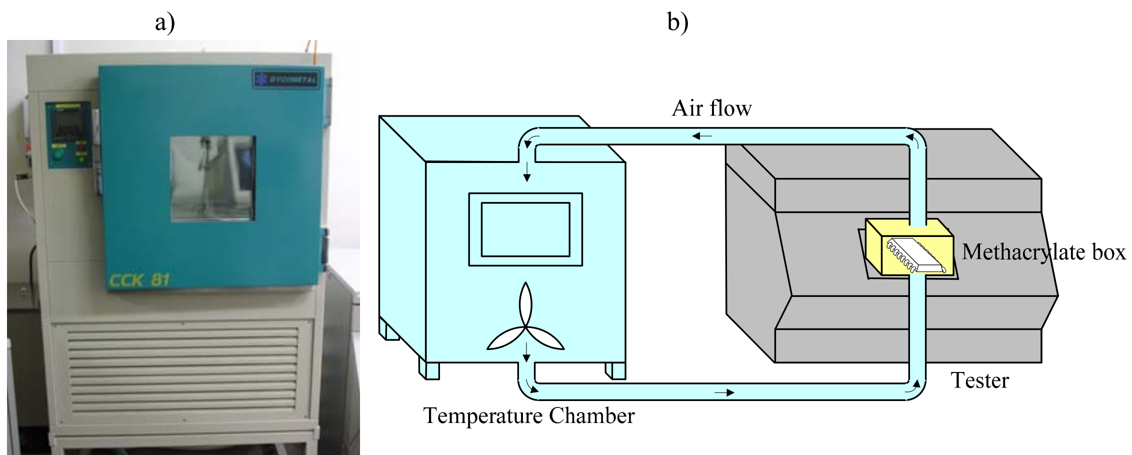

Figure B.4. Climate chamber a) Photograph b) System

The climate chamber is able to reach temperatures below zero. However, as the air is extracted out of the temperature chamber, the humidity control disappears. Hence, some frost problems may appear in the methacrylate box for temperatures below 0˚C.

B.3 Diagnosis tool

The diagnosis tool used is called *Faloc*. *Faloc* is the abbreviation for '*Fa*ult *Loc*alisation'. This *NXP Semiconductors* tool provides fast fault localization for real devices which fail on a test system or during logic simulation. Faulty test vector numbers and device pin numbers are analysed in order to isolate the source of a particular production or design error. This software relies on the stuck-at, the failing net, the failing branch, the bridging and the delay fault models. *Faloc* generates a listing file (.lis) which contains a compact summary of the failing flip flops, a probability matrix including the quality values, a fail report with net names, instance names, module names and layout coordinates. For each possible fault candidate, two quality values are evaluated: Matching and Prediction. On the one hand, the Matching value (*M*) quantifies the tester failing results, which actually match with the faulty signature of a particular fault (see Figure 3.18). On the other hand, the Prediction value (*P*) quantifies how many failures predicted by a particular fault are really observed on the tester. The definition of both quality values are described in *(3.25)* and *(3.26)*, respectively.

B.4 Bridge tool

CatBridge is a software from NXP *Semiconductors* that provides bridging fault information that is derived from a layout database. CatBridge is able to extract all possible bridges from a given layout description. The extraction process only takes into account net segments within the same layer. The extracted bridges are written to a bridging fault file (*.bff*) which has been subsequently used for both the diagnosis of bridging (multiple level I_{DDQ} bridging fault methodology) and open faults (FOS methodology).