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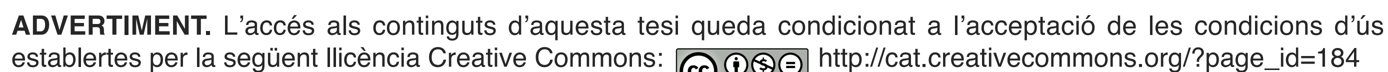

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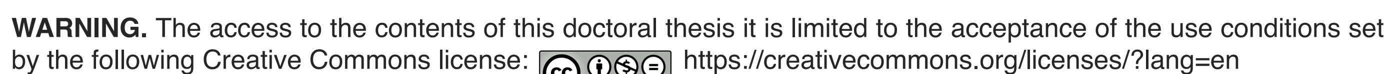

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Novel silicon detector technologies for the HL-LHC ATLAS upgrade

Ph.D. Thesis

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Abstract

The Large Hadron Collider (LHC) at the European Organization for Nuclear Research (CERN), Geneva, will interrupt its operation in 2023 to be upgraded to high luminosity (HL-LHC) and provide proton-proton collisions with a center of mass energy of $\sqrt{s} = 14\,\text{TeV}$ at a luminosity of $10^{35}\,\text{cm}^{-2}\text{s}^{-1}$.

ATLAS, one of the two general purpose experiments at the LHC , will have to be upgraded to meet the new requirements given by the larger luminosity. Among other things the ATLAS upgrade foresees the replacement of the Inner Detector with a full silicon Inner Tracker (ITk), with finer granularity and improved radiation tolerance, and the introduction of the High Granularity Timing Detector (HGTD) that will provide timing information of tracks and vertices. Combining the measurements of ITk and HGTD it will be possible to resolve vertices close in space but separated in time, improving the ATLAS reconstruction performance.

In this thesis two novel silicon detector technologies are investigated for applications in the HGTD and ITk, the Low Gain Avalanche Detectors (LGAD) and the HV-CMOS technologies.

The LGAD technology consists of planar n-on-p silicon detectors with a highly doped *p-type* implantation underneath the *n-type* electrode. It was originally developed for radiation hard tracking detectors but the fine segmentation of the electrode proved to affect the charge multiplication mechanism and no gain has been observed on segmented devices. On the other hand, thin LGAD detectors have shown a time resolution of about 30 ps on the detection of minimum ionizing particles and it was chosen as baseline technology for the HGTD sensors. Studies of LGAD sensors, before and after irradiation were first performed in the context of this thesis.

The HV-CMOS technology was originally aimed to provide active pixel sensors with the advantage, compared to the standard hybrid devices, of the AC coupling capability. However, during the R&D effort, it become clear that monolithic HV-CMOS devices offered the most promising advantages: moderate radiation hardness and cost reduction. This thesis includes the characterization of the first full scale HV-CMOS chip prototype for the ATLAS experiment. This technology is currently taken into account as a drop-in option for the outer layer of the ITk pixel detector.

Resumen

El Large Hadron Collider (LHC) en la Organización Europea para la Investigación Nuclear (CERN), Ginebra, interrumpirá su operación en 2023 para ser mejorado a High Luminosity LHC (HL-LHC) y proporcionar colisiones entre protones con una energía en el centro de masa de $\sqrt{s} = 14\,\text{TeV}$ con una luminosidad de $10^{35}\,\text{cm}^{-2}\text{s}^{-1}$.

ATLAS es uno de los experimentos alojados en el LHC que tendrá que ser mejorado para cumplir los nuevos requisitos impuestos por la mayor luminosidad. Las obras de mejora de ATLAS prevén la sustitución del Inner Detector por un detector de trazas interamente de silicio, el Inner Tracker (ITk), con una granularidad más pequeña y una mayor resistencia a la radiación, y la introducción del High Granularity Timing Detector (HGTD), que proporcionará información temporal de las trazas y de los vértices. Combinando las medidas de ITk y HGTD será posible resolver vértices cercanos en el espacio pero con suficiente separación temporal, lo cual mejora las prestaciones de ATLAS.

En esta tesis se investigan dos nuevas tecnologías de detectores de silicio para aplicaciones en el HGTD y el ITk, la tecnología de Low Gain Avalanche Detector (LGAD) y la de HV-CMOS.

La tecnología LGAD consiste en detectores planares de silicio n-on-p con un implante altamente dopado de tipo p debajo del electrodo de tipo n. Originalmente fue desarrollada para detectores de trazas resistentes a la radiación, pero la segmentación del electrodo demostró afectar al mecanismo de multiplicación y no se ha observado ganancia en los primeros dispositivos. Por otro lado, detectores LGAD delgados han mostrado una resolución temporal de aproximadamente 30 ps y fueron elegidos como de base para los sensores del HGTD. Estudios de sensores LGAD, antes y después de la irradiación, se realizaron por primera vez en el contexto de esta tesis.

La tecnología HV-CMOS originalmente aspriaba a producir sensores con píxel activo, con la ventaja, en comparación con los dispositivos híbridos estándar, de poder optar por el acoplamiento capacitivo. Sin embargo, durante el proceso de IyD, resultó claro que los dispositivos monolíticos en tecnología HV-CMOS ofrecen las ventajas más prometedoras: una moderada resistencia a la radiación y la reducción de costos. Esta tesis incluye la caracterización de la primera muestra a escala completa de un chip HV-CMOS para el experimento ATLAS. Actualmente, esta tecnología se tiene en cuenta como una opción de inserción para la capa externa del detector de píxeles del ITk.

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Chapter 1

Introduction

The Standard Model (SM) of particle physics accurately describes the interactions between elementary particles through three of the four elementary forces: electromagnetic, weak and strong nuclear forces, leaving out the gravitational interaction. Since its formulation in the mid-1970s the SM has been validated thanks to the discovery of heavy quarks (*bottom*, *top* and *charm*), the Z and $W^{\pm}$ bosons and the gluon whose properties where predicted by the model before they were first observed. The last particle that was missing to complete the SM particle zoo was the Higgs boson, observed by the ATALS and CMS experiments at the CERN Large Hadron Collider (LHC) in 2012 [1].

Despite the success of the theory, there are still open questions that cannot be answered by the standard model. Experimentally observed neutrino masses and mixing angles need to be added ad-hoc, gravity cannot be integrated, the model suffers from the hierarchy problem (fine tuning) and no SM particle is a valid candidate for dark matter.

A wide spectrum of extended models has been proposed by theoreticians, the so called Beyond the Standard Model (BSM) theories, with the purpose to solve the SM issues. The most popular of them is Supersymmetry (SUSY). SUSY consists in a family of theories that assign to each SM particle a super-symmetric partner with identical quantum numbers except the spin that differs by half a unit. Supersymmetric particles with masses at the TeV scale could solve the hierarchy problem given by the Higgs boson mass. Moreover, some SUSY theories allow the unification of gauge couplings and the incorporation of gravity. Furthermore, if the lightest SUSY particle is stable and weakly interacting with SM particles it can be a candidate for dark matter.

Among other BSM theories proposed to provide explanations to the unsolved problems of particle physics it is worth to mention String Theory, Technicolor and M-Theory.

All the BSM theories reproduce the SM predictions and describe the current experimentally observed phenomena. More experiments are needed to reject or validate these theories and constrain their parameters' phase space. Two kinds of experiments are performed by the high energy physics community to explore the BSM domain: searching for discrepancies with SM predictions through precision measurements and searching for evidences of new particles or interactions at high energy colliders. With the first category belong experiments such as MEG [2], where lepton flavor violating muon decay is searched for, and BELLE-II [3], where CP violating decays of B mesons are observed in a large data set looking for rare decay channels whose branching ratio is enhanced by some BSM models. The experiments based at the Large Hadron Collider (LHC) instead profit from the extremely high energy available in the interactions to search for direct evidence of new particles produced in the collisions. At the same time, due to the large number of interactions generated at LHC, heavy quarks are produced abundantly and precision measurements of bottom and top flavored hadron's properties can be performed.

It is expected that at the end of the LHC lifetime statistical uncertainties will be the major contribution to the total uncertainty on the measurements of rare phenomena. For this reason, LHC will be upgraded to High Luminosity LHC (HL-LHC), where collisions will be produced at the same center of mass energy $\sqrt{s} = 14\,\mathrm{TeV}$ but with an instantaneous luminosity of $5 \div 7 \cdot 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, about five times larger than the LHC design luminosity. In order to maintain the physics performance, the experiments located at LHC will have to be upgraded to face the new requirements given by the larger number of interactions per bunch crossing and the larger radiation damage that will be accumulated during the lifetime of the HL-LHC.

The situation of the innermost detector system is specially compromised. On one hand, it has to cope with a much higher rate, which suggest smaller sensor pitches, on the other hand, the radiation hardness has to reach unprecedented levels. ATLAS decided to fully replace the current inner detector with a full silicon tracker. The large area involved in such a tracker motivated the research of commercial based silicon technologies (CMOS process) for a cost effective solution.

In particular, depleted CMOS detectors AC-coupled to the front-end chip were originally explored as a replacement for the traditional hybrid planar devices. However, the cost reduction of this approach was marginal since the gluing process with high uniformity proved to be complicated. At the same time, active CMOS sensors bump-bonded to front-end chips were found to be not sufficiently radiation hard for the innermost layers. However, monolithic depleted CMOS devices offer significant cost reduction, that is particularly important for large area coverage, as it is the case for the outer layers, where the radiation hardness requirements are relaxed.

The characterization of the first full size monolithic depleted CMOS prototype for ATLAS is presented in this thesis.

The 3D sensor technology is the baseline solution for the innermost layer of the ATLAS pixel detector upgrade for HL-LHC. The pixel size of the detector will be significantly reduced from the current $50 \times 250\,\mu\text{m}^2$ and $50 \times 400\,\mu\text{m}^2$ to $50 \times 50\,\mu\text{m}^2$ or $25 \times 100\,\mu\text{m}^2$. However, even with the excellent position resolution that will be achieved with such a detector, the high pile-up in HL-LHC will significantly degrade the performance in terms of jet and vertex reconstruction, lepton isolation and b-tagging, with respect to the current detector, in the forward region.

For this reason, a timing detector that can be used to mitigate the effect of pile-up has been proposed and initially approved by ATLAS. The High Granularity Timing Detector (HGTD) will be based on the Low Gain Avalanche Detector (LGAD) technology, initially developed at the Centro Nacional de Microelectrònica (CNM). The LGAD sensors consist of silicon planar sensors with a multiplication layer that enhance the signal.

This technology was initially developed for tracking applications, since the multiplication layer could improve the sensor performance after irradiation compensating the loss of charge due to radiation damage. Although this approach did not prove successful for the small pixel sizes needed by tracking applications, thin LGAD sensors were proposed for timing application.

The first results of LGAD sensors timing resolution before and after irradiation were obtained in the framework of this thesis.

Chapter 2

Solid State Detectors

Solid state detectors have been introduced in the field of experimental particle physics in the late seventies of the twentieth century. Since then they became increasingly common thanks to the outstanding performance in terms of position resolution and radiation hardness, two crucial factors for experiments at particle colliders. Nevertheless gas-based tracking detectors have not been totally replaced by solid state detectors. Since they are more cost effective they are used in the outer layers of big experiments. This is the case at the Large Hadron Collider (LHC), where large volumes have to be covered and the requirements in terms of resolution and radiation hardness can be relaxed as the distance from the interaction point increases.

In the past decades the scientific community proposed significant technological advances in the solid state detectors field, from strip detectors to pixel devices as well as new technologies like monolithic devices and 3D detectors are introduced. To meet the growing experiments demand, the silicon industry grew and improved the manufacturing techniques allowing to produce thinner and larger wafers and detectors with a finer segmentation and better radiation hardness. At the same time, the progress on application-specific integrated circuits (ASICs) driven by the electronic industry has been crucial to provide adequate readout systems.

This chapter summarizes the fundamental aspects of silicon detectors, possible application in high energy physics experiments and describes how radiation affects their performance.

2.1 Solid State Detector Working Principle

In a solid state detector, and in most detectors in general, the signal is given by the current associated to the drift of the ionization charges produced by the charged particles passing through the sensor. The high density, the fast readout and the high segmentation are characteristics that make these kind of devices suitable for the

detection of high energy particles in relatively small spaces. For this reason they are the common choice for tracking detector of experiments at colliders, where a large number of particles is created at the interaction point after each collision.

2.1.1 The Band Model of Solids

The fundamental theory of solid state detectors is the band model of solids. The main feature of this theory is that the energy levels of the atoms within a solid are merged to form collective energy levels called bands. Due to the Pauli exclusion principle each band can host a finite number of electrons, the lowest energy levels will be fully filled while over a certain value the occupancy will be null.

The highest fully filled band is named valence band and the lowest empty or partially filled band is named conduction band. When the conduction band is partially filled the solid is a conductor, otherwise the energy gap, $E_g = V_C - V_V$, between these bands is used tu distinguish semiconductors and insulators, see figure 2.1. Insulators' energy gap is usually larger than 3 eV while all the materials with a lower energy gap are called semiconductors [4]. Silicon, the most common semiconductor used in radiation detectors has a $E_g \sim 1.2$ eV.

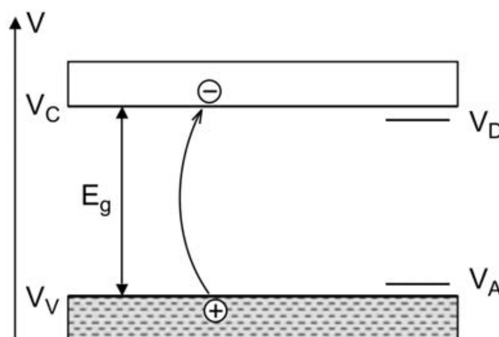


Figure 2.1: Scheme of the band structure of solid state materials. V_C and V_V are potentials of the conduction and valence levels, V_A and V_D the acceptors and donors ones [4].

The most common semiconductors are silicon and germanium, both have four valence electrons so that four covalent bonds are formed around each atom. Electrons can be excited from the valence band to the conduction band becoming free to move in the crystal lattice and leaving vacancies in their original positions. These vacancies, called holes, are positively charged and can then be filled by other electrons of the valence band leaving holes in their original positions. The holes therefore move through the crystal lattice as well, behaving as carriers of positive charge.

Electron-hole pairs are continuously generated in a semiconductor by thermal

excitation, as well as destroyed since a certain number of free electrons will recombine with holes. The concentration of electrons in the conduction band can be calculated by

$$n = \int_{E_C}^{\infty} g_e(E) f(E) \, \mathrm{d}E, \tag{2.1}$$

where $g_e(E)$ is the density of states, $f(E)$ is the Fermi-Dirac distribution and the integral is calculated from the minimum energy level of the conduction band E_C to infinity. In an analogous way the concentration of holes p can be calculated integrating from zero to the maximum energy level in the valence band E_V:

$$p = \int_{0}^{E_V} g_h(E) f(E) \, \mathrm{d}E. \tag{2.2}$$

Electrons and holes are fermions obeying to the Fermi-Dirac distribution

$$f(E) = \frac{1}{1 + e^{(E-E_F)/kT}}, \tag{2.3}$$

with E_F being the Fermi energy, k the Botlzmann constant and T the absolute temperature. The density of states for electrons and holes can be calculated assuming they are free to move within the semiconductor but cannot escape it. This is represented by a box potential that is zero inside the boundaries of the semiconductor and infinity outside of it and can be written as

$$g_e(E) = \frac{1}{2\pi} \left(\frac{m_n}{\hbar^2} \right)^{3/2} \sqrt{E - E_C} \tag{2.4a}$$

$$g_h(E) = \frac{1}{2\pi} \left(\frac{m_h}{\hbar^2} \right)^{3/2} \sqrt{E_V - E} \tag{2.4b}$$

where m_n and m_h are the effective masses of electrons and holes, and $\hbar$ the reduced Planck constant. Integrating equation 2.1 and 2.2 the electron and hole concentrations result to be

$$n = 2 \left(\frac{m_n kT}{\hbar} \right)^{3/2} e^{-(E_F - E_V)/kT} = N_C e^{-(E_C - E_F)/kT} \tag{2.5a}$$

$$p = 2 \left(\frac{m_p kT}{\hbar} \right)^{3/2} e^{-(E_F - E_V)/kT} = N_V e^{-(E_F - E_V)/kT} \tag{2.5b}$$

where N_C and N_V are the effective density of states in the conduction and valence band. The product of the density for electrons and holes reads

$$np = n_i^2 = N_C N_V e^{-E_g/kT} \tag{2.6}$$

where n_i indicates the electron and hole density in an intrinsic semiconductor, where

they are assumed to be equal, and E_g is the energy gap. Typical values for n_i in silicon at room temperature are of the order of $1.5 \cdot 10^{10}\,\mathrm{cm}^{-3}$ [5].

The balance between the two charge carriers in intrinsic semiconductors can be modified adding dopants to the pure crystal. Introducing atoms with one more or one less valence electron an excess of electrons or holes is created. From the band structures point of view the presence of atoms with three valence electrons (acceptors), such as boron or gallium, introduces an energy level slightly above the valence band that can be populated by free electrons creating an excess of holes. The presence of atoms with five valence electrons (donors), such as phosphorus or arsenic, introduces extra electrons that cannot populate the valence band. These electrons will then fill an energy level slightly below the conduction band with en effective energy gap of about 0.05 eV in silicon. The extra electrons are easily promoted to the conduction band creating an excess of free electrons in the semiconductor. Doped semiconductors with an excess of holes are called *p-type* while those with excess of electrons are called *n-type*.

Doped semiconductors remain electrically neutral because the electric charge of the extra electrons or holes is balanced by the nuclei having one more or less proton than silicon. The total sum of positive and negative charge density have therefore to be equal, if N_A and N_D are the acceptors and donors concentrations, the electrical balance can be written as:

$$N_D + p = N_A + n. \tag{2.7}$$

In a *p-type* semiconductor $p \gg n$ and $N_D = 0$. Combining the last equation with equation 2.6 the charge carrier density can be written in terms of dopant concentration as

$$p \simeq N_A \text{ and } n \simeq \frac{n_i^2}{N_A}. \tag{2.8}$$

Conversely in an *n-type* semiconductor $n \simeq N_D$ and $p \simeq n_i^2/N_D$. Meaning that in a doped semiconductor the concentration of the majority charge carriers is approximately equal to the dopant concentration.

Under the effect of an electric field E, free electrons and holes move with a drift velocity of

$$v_{e/h} = \mu_{e/h} E, \tag{2.9}$$

where $\mu_{e/h}$ is the mobility of electrons or holes, whose typical values for high purity silicon at room temperature are $1350\,\mathrm{cm}^2/\mathrm{Vs}$ and $450\,\mathrm{cm}^2/\mathrm{Vs}$, respectively [6, 7]. The drift velocity cannot grow indefinitely and will reach a saturation value for large electric field. In an intrinsic semiconductor electrons and holes have the same density n_i and both contributes to the current density as $J = e\,n_i(\mu_e + \mu_h)E$. The current density can be expressed in terms of resistivity as $J = E/\rho$. The resistivity of a

semiconductor is therefore given by

$$\rho = \frac{1}{en_i\left(\mu_e + \mu_h\right)}. \tag{2.10}$$

In doped semiconductors the current contribution of minority charge carriers can be neglected and the charge carrier density can be replaced by the dopant density as shown in equation 2.8. As a result equation 2.10 can be written as

$$\rho_{n-type} = \frac{1}{eN_D\mu_e}, \tag{2.11a}$$

$$\rho_{p-type} = \frac{1}{eN_A\mu_h}. \tag{2.11b}$$

Both intrinsic and doped semiconductors have a too large density of free carriers to be used as particle detectors. But, combining semiconductors with opposed doping, a region without free charges can be created and exploited for particle detection.

2.1.2 The PN-Junction

When two semiconductors with opposite doping are in close contact a *pn-junction* is formed. The *pn-junction* behave as a semiconductor diode. Ideally, it has zero resistance when forward bias is applied and infinite resistance for reverse bias. In the real case, the *pn-junction* does not significantly conduct until a turn-on forward bias is reached, while in reverse bias a non null leakage current is present. If the reverse bias exceeds the break down value, a rapid increase of current is shown.

Due to the difference in concentration type at the junction interface, some of the electrons will diffuse from the *n-type* to the *p-type* and some holes will diffuse in the opposite way. Once in the *p-type* region the electrons will easily recombine with the holes that are in excess, while the holes in the *n-type* region will be filled by electrons.

The semiconductors that were originally electrically neutral become charged because of the charge flow from one semiconductor type to the other. The *p-type* region close to the junction acquires a negative charge while the *n-type* region results positively charged. This creates an electric field around the contact interface that eventually will counterbalance the charge migration and push away any free charge located in this volume called depletion zone or space charge region. The characteristics of the *pn-junction* are shown in a schematic view in figure 2.2.

The *pn-junction* is the base for any semiconductor detector, since it generates a region with no free charge that can be altered by using different geometries and applying an external bias voltage. The ionizing radiation passing through the depletion zone releases a number of electron-hole pairs that are then pushed away by the electric field present in that region generating a current pulse that reveals the passage

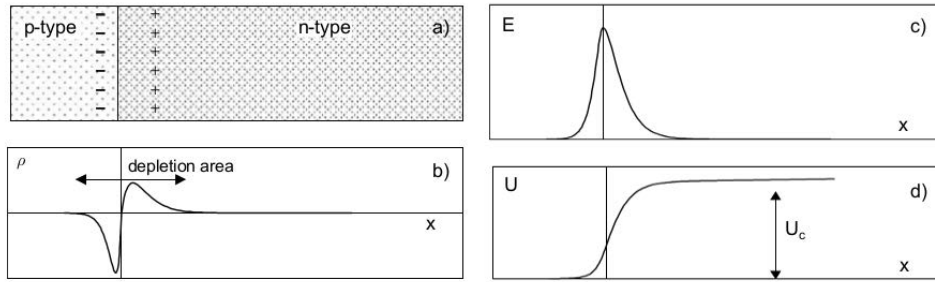


Figure 2.2: Scheme of a *pn-junction* (a), charge distribution (b), electric field (c) and potential energy (d) [4].

of a particle in that area.

The depletion region can be made thinner or wider applying a direct or reverse bias voltage. In general a reverse bias is applied, the holes in the *p-side* will be attracted towards the electrode away from the depletion zone and similarly for the electrons in the *n-side*, it has the effect to maximize the depletion zone and to increase the electric field in it, see figure 2.3. Since only the charge generated inside the depleted volume contributes to the signal, applying a reverse bias improves the intrinsic performance of the junction as a detector. However, the break down voltage V_{BD} defines the limit to the maximum applicable bias value, after which the diode breaks down and starts to be conductive.

The width of the depletion depth is given by

$$d = \sqrt{\frac{2\varepsilon V}{e}\left(\frac{N_A + N_D}{N_A N_D}\right)} \tag{2.12}$$

where ε is the dielectric constant, V the applied voltage and e the electron charge. In case the dopant concentration is not symmetric but there is a much higher concentration of dopants on one side with respect to the other the equation 2.12 reduces to

$$d = \sqrt{\frac{2\varepsilon V}{eN_{D/A}}} = \sqrt{2\varepsilon\rho\mu_{e/h}V}, \tag{2.13}$$

where on the right side the dopant densities have been replaced using equations 2.11a and 2.11b. Note that the depleted region grows into the less doped semiconductor.

Equation 2.13 can be rearranged to find out the bias voltage required to fully deplete a sensor whose properties, such as thickness, resistivity and charge carrier mobility are known.

As previously said, electrons and holes are continuously generated in a semiconductor by thermal excitation, usually they recombine but if they are generated within

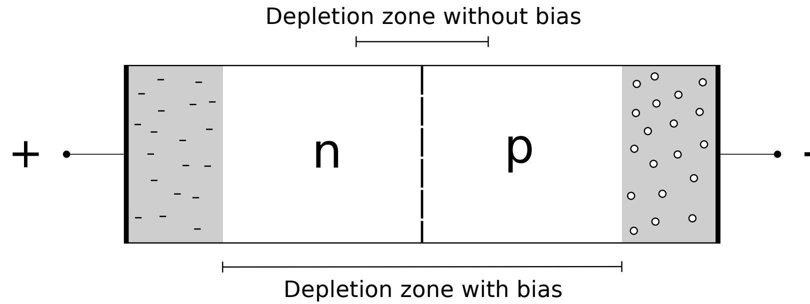


Figure 2.3: Scheme of a *pn-junction* under the effect of a reverse bias.

the space charge region of a *pn-junction*, they are drifted apart by the electric field contributing to a current, named leakage current. The leakage current is therefore dependent linearly on the depleted volume, that increases with $\sqrt{V}$ while the relation with the temperature, that acts on the rate of electron-hole pair generation, is

$$I_{leak} \propto T^2 e^{-E_g/2kT}. \tag{2.14}$$

A lower temperature implies a lower leakage current leading to a less noisy detector. This property is of particular significance when dealing with irradiated devices where radiation induced damage in the bulk leads to large leakage current.

2.2 Silicon Detectors

The basic element of a silicon detector is a reverse biased *pn-junction* where the electron-hole pairs generated in the bulk by the ionizing radiation are collected by heavily doped *p-type* and *n-type* regions acting as electrodes. The bulk is usually lowly doped as well, in figure 2.4 a sketch of a detector with *p-type* bulk is shown.

One of the properties that make silicon detectors so popular is, beyond the radiation hardness, the opportunity to have highly segmented electrodes that is also used to classify different detectors types. If the electrode is left unsegmented, the whole detector consist of a single *pn-junction* and it is called pad diode. This diodes are usually used for prototype tests as their construction and handling is simpler, or for applications where segmentation is not required.

A detector in which the electrode is divided into parallel strips is called a strip detector. One end of each strip is then connected to the readout system. This kind of detector can give position information with high resolution on the segmented direction depending on the width of the strips. To have position information on both direction two not aligned strips detectors are usually used, although double sided strip detectors are possible and have been used, for example, in the CDF vertex tracker [8].

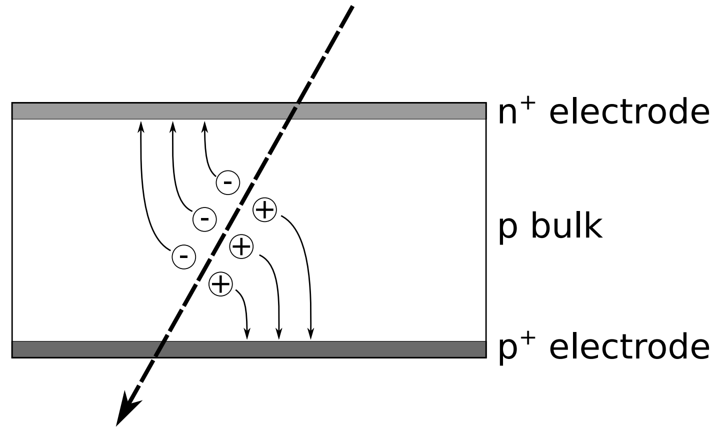


Figure 2.4: Sketch of an n-on-p pad diode.

In a strip detector the hit is reconstructed in the intersection of the strips that fire. This solution can lead to ambiguity when more than one parallel strip have a signal, being this because of simultaneous particles or noise. Pixel detectors are instead silicon detectors where one electrode is segmented in both directions generating a matrix of pixels. In this way each pixel contains 2D information on the position of the hit resolving possible ambiguities that a strip detector would have in a particle-crowded environment, see figure 2.5.

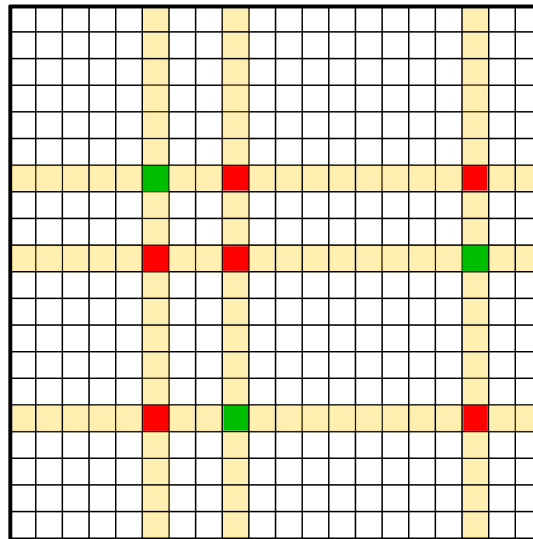


Figure 2.5: Scheme of an event with three particles in a 20×20 silicon detector. In green the pixels hit by the particles and in yellow the corresponding strips. In the case the detector is made of two perpendicular strip detectors the red pixels would be reconstructed as well as possible hit introducing ambiguity.

In pixel detectors the number of electronic channels needed to read out the sensor is much larger than that of strip detectors covering the same size. In addition, the

signals cannot be easily probed on the side of the sensor. Traditionally, a readout chip is pixel-by-pixel interconnected to the sensor, through a process named bump-bonding, making what is called a hybrid detector.

Recently, pixel silicon detectors have been produced in CMOS technology with in-pixel front-end electronics integrating readout chip and sensor in the same substrate. Devices adopting this solution are called monolithic devices. In monolithic devices the front-end electronics is partially hosted inside the pixel, the analog signal is processed and digital information is delivered to the periphery of the sensor and from the periphery to the readout system.

Hybrid detectors have the advantage that the sensor and the front-end can be produced in different technologies to achieve a better performance in terms of radiation hardness. Monolithic devices instead do not require bump-bonding, that is an expensive process making this option cheaper than hybrid detectors, suitable when the requirements on radiation hardness are not very strict and a large area has to be covered.

2.2.1 Signal Generation by Charged Particles

When charged particles travel trough matter they interact with the atoms of the material losing part of their energy. They may lose energy interacting with the electrons of the atoms or with the nuclei, these are respectively called ionizing or non-ionizing energy loss. The former is responsible of the generation of electron-hole pairs and therefore of the signal in a silicon detector, the latter instead introduces defects in the crystal and is the origin of the radiation damage, discussed in section 2.2.4.

For relativistic charged particles in the energy range of $0.1 \lesssim \beta\gamma \lesssim 1000$ the mean rate of energy loss, shown in figure 2.6, is described by the Bethe equation [9]:

$$\left\langle -\frac{\mathrm{d}E}{\mathrm{d}x} \right\rangle = Kz^2 \frac{Z}{A} \frac{1}{\beta^2} \left(\frac{1}{2} \log \frac{2m_e c\beta^2\gamma^2 T_max}{I^2} - \beta^2 - \frac{\delta(\beta\gamma)}{2} \right) \tag{2.15}$$

where $K = 4\pi N_A r_e^2 m_e c^2$ with N_A the Avogadro's number, r_e the classical electron radius and $m_e c^2$ the rest mass of the electron, Z is the atomic number, A is the atomic mass, I is the mean excitation energy of the medium, T_{max} is the maximum transferable energy in a single collision, $\beta = v/c$, $\gamma = 1/\sqrt{1-\beta^2}$ is the Lorentz factor and $\delta(\beta\gamma)$ is a correction factor for higher energy particles.

The Bethe equation has a minimum at $\beta\gamma \sim 3$ that hardly increases over some orders of magnitude. This simplifies the treatment of high momentum particles that can be considered as minimum ionizing particles (*mip*). These particles lose a small fraction of their energy travelling through the material and can be considered

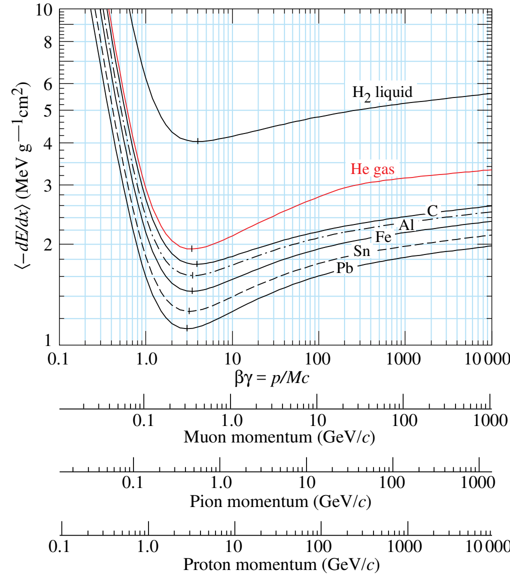


Figure 2.6: Mean energy loss rate as a function of the particle $\beta\gamma$ in different materials. Conversion from $\beta\gamma$ to momentum is given for muons, pions and protons. Radiative effects are not included [9].

mip during all the interactions. In silicon a *mip* has an average stopping power of $\left\langle \frac{\mathrm{d}E}{\mathrm{d}x} \right\rangle = 1.66\,\mathrm{MeV\,cm^2/g}$. The probability distribution of the energy loss follows approximatively a Landau distribution. This distribution is asymmetric and has a long tail which affects the calculation of the mean energy loss. It is more common to quote the most probable value (MPV) of the distribution:

$$\Delta_p = \xi \left(\ln \frac{2m_e c^2 \beta^2 \gamma^2}{I} + \ln \frac{\xi}{I} + 0.2 - \beta^2 - \delta(\beta\gamma) \right) \tag{2.16}$$

with $\xi = (K/2)\, Z/A\, (x/\beta^2)\,\mathrm{MeV}$ where x is the detector thickness in $\mathrm{g/cm^2}$. The energy loss in a detector is therefore function of the particle energy and of the detector thickness, being $\Delta_p/x \propto a \ln x + b$. The MPV scaled to the mean energy loss of a *mip* in silicon is shown in figure 2.7.

The energy deposited in a detector by ionization generates a number of electron-hole pairs proportional to the detector thickness and inversely proportional to the energy needed to create an electron-hole pair. The average energy needed to create each pair in silicon is 3.6 eV, about three times larger than the energy gap (1.12 eV). The extra energy is spent in the generation of phonons for momentum conservation. A *mip* crossing a 300 μm thick silicon detector has a $\Delta_p/x \sim 1.13\,\mathrm{MeV\,cm^2/g} = 260\,\mathrm{eV}/\mu\mathrm{m}$, being $\rho_{Si} = 2.33\,\mathrm{g/cm^3}$, that is equivalent to ~ 72 electron-hole pairs/μm.

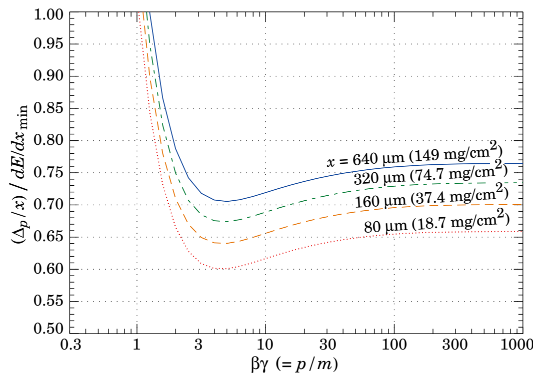


Figure 2.7: Most probable energy loss scaled to the mean energy loss of a *mip* in silicon for different thickness of the silicon substrate [9].

2.2.2 Signal Generation by Photons

The interaction of photons with solid state detectors have to be treated in a different way. Photons do not interact with the material along their path but have a probability to be absorbed that depends on their energy and on the specific material and thickness. Photons interact via three different processes:

- *Photoelectric Effect*: The photon is absorbed by an atom which releases an electron with energy equal to the one of the impinging photon minus the ionizing energy. The cross section of the photoelectric effect strongly depends on the atomic number ($\sigma_{pe} \propto Z^n$ with n ranging from 4 to 5) and is characterized by discontinuities due to the ionization thresholds of the atomic levels. The cross section is dominating in silicon at energies $\lesssim 100\,\mathrm{keV}$ beyond which it quickly decreases in several orders of magnitude.

- *Compton Scattering*: In the energy range between $\sim 100\,\mathrm{keV}$ and $\sim 10\,\mathrm{MeV}$ Compton scattering is the main absorption process where the photon scatters with an atomic electron. The final state consists of a lower energy photon and a recoil electron whose energy and direction are defined by momentum conservation.

- *Pair Production*: When the photon energy is larger than twice the electron rest mass (1.022 MeV), e^+/e^- pairs can be created in the interaction with the material.

The signal in the silicon detector is not directly induced by the photon, but it is due to the charged particles (i.e. electrons and positrons) produced or released by the photon that will afterword ionize along their path generating electron-hole pairs and hence a signal in the detector.

The free electrons and holes in the detector bulk move under the effect of the electric field in the depleted volume with a drift with a velocity $\vec{v}_{drift}$, that is proportional to the electric field E and to their mobility $\mu_{e/h}$, see equation 2.9. The current induced by the charge drift in a readout electrode is given by the Shockley-Ramo theorem:

$$i(t) = q\vec{v}_{drift} \cdot \vec{E}_W, \tag{2.17}$$

where q is the moving charge and $\vec{E}_W$ is the weighting field of the readout electrode, obtained by applying unit potential to the electrode and zero potential to all the others and solving the Laplace equation, $\nabla^2 \Phi_W = 0$.

The time integral of the current results in the collected charge $Q = \int i(t)\,\mathrm{d}t$. If all the charges reach the electrodes within the integration time, the collected charge will be equal to the deposited charge. This is often not the case, especially in irradiated devices, where radiation induced defects may act as traps for the charge carriers.

2.2.3 Detector Applications

The high energy physics community took advantage of the properties of silicon detectors to produce devices for different applications. In particular the ability of producing segmented electrodes have been exploited to produce position sensitive detectors for tracking applications. Moreover, the short charge collection time gives silicon detectors a good timing resolution when coupled to readout electronics suitable for this purpose.

Tracking Detectors

The opportunity to produce thin devices with electrode segmentation of the order of tens of micrometers makes silicon detectors suitable for tracking applications. The energy lost by a *mip* in a device is typically very small compared to the energy of the particle making possible to add several layers of silicon detectors for a better reconstruction of the particle trajectory. The ionizing particles will leave a signal in each detector layer where the resolution will depend on the electrode segmentation: the finer the segmentation, the better the resolution.

When a particle leaves a signal in a pixel the impact position within the pixel is unknown, the coordinates of the pixel center is assigned to the hit with an uncertainty that depends on the pixel pitch in each direction. Since the particle could have crossed the pixel in any point with equal probability the resolution is given by the standard deviation of the uniform distribution $\sigma = pitch/\sqrt{12}$.

The particle can leave a signal in more than one pixel. This may occur because its path effectively crosses the volume corresponding to neighbouring electrodes, because

the electron-hole pairs diffuse to a neighbour pixel, or because delta electrons are produced. A delta electron is a secondary electron with large enough energy to travel a significant distance and can deposit its energy in the nearby pixels. The contiguous fired pixels are clustered and the position assigned to the particle together with its uncertainty depend on the clustering algorithm that is used. Often the readout chip records a parameter called Time Over Threshold (TOT), that is a measure of the time the signal has been larger than the threshold value, expressed in clock cycle units. The TOT is related to the deposited charge with a non linear relation, conversion functions or look-up tables are used to transform TOT to charge. The charge can afterwards be used to improve the clustering algorithm.

Timing Detectors

Silicon detector design can be optimized to produce devices with good timing resolution. The time resolution σ_t is given by the square sum of four different contributions:

$$\sigma_t^2 = \sigma_{TW}^2 + \sigma_{Landau}^2 + \sigma_{jitter}^2 + \sigma_{TDC}^2. \tag{2.18}$$

The energy loss in a detector is a stochastic process. The amount of deposited charge by a *mip* in a detector is approximately described by a Landau distribution, as mentioned above. Two simultaneous signals of different amplitudes cross a fixed threshold at different times, with the larger signal arriving earlier than the smaller one. This effect is called time walk and its contribution to the time resolution can be expressed as [10]

$$\sigma_{TW} = \left[\frac{V_{th}}{S/t_{rise}}\right]_{RMS}, \tag{2.19}$$

with V_{th} the threshold value, S the signal amplitude and t_{rise} the signal rise time. The time walk can be minimized using Constant Fraction Discriminators (CFDs) where the time of the event is assigned to the time the signal crosses a value corresponding to a fraction of its own amplitude, or, with less accuracy, using information on the signal amplitude or TOT. With CFDs the time-walk is reduced to fluctuations due to the resolution of the signal digitizer.

Not only the energy deposited into the detector follows a stochastic process but the distribution of charge along the *mip* trajectory is stochastic as well. The *mip* deposits its energy in clusters, the charge of the cluster contributes to the current by drifting through the electrodes. When a cluster reaches an electrode it stops contributing to the current generating an equivalent noise charge. The σ_{Landau} term takes into account the contribution to the time resolution given by this phenomenon that can be reduced minimizing the sensor thickness [11].

The third term describes the signal jitter due to noise fluctuations. This contri-

bution is proportional to the signal over noise ratio

$$\sigma_{jitter} = \frac{t_{rise}}{S/N}. \tag{2.20}$$

The last term describes the resolution of the Time to Digital Converter (TDC) and is the standard deviation of the uniform distribution:

$$\sigma_{TDC} = \frac{TDC_{bin}}{\sqrt{12}}, \tag{2.21}$$

where TDC_{bin} is the bin size of the digitizer.

A good timing resolution with silicon sensors can be achieved (of the order of tens picoseconds) if σ_{Landau} is reduced minimizing the active thickness, and optimized electronics is used to reduce the σ_{TW} and the σ_{TDC} contributions. In addition, thin devices with charge multiplication further improve the S/t_{rise} ratio with beneficial effects on σ_{jitter} and σ_{TW}. Such devices have been produced based on the Low Gain Avalanche Detector (LGAD) technology in the context of the High Granularity Timing Detector (HGTD) and will be discussed in chapter 4 of this thesis.

2.2.4 Radiation Damage

As mentioned above, ionization is not the only interaction mechanism between the particles and the detector. The particles can interact with the nucleus losing energy via non-ionizing interactions with the silicon lattice atoms. If the transferred energy is large enough the nucleus can be displaced from its lattice position, and, if it recoils with enough energy, it can displace the nuclei of the neighbouring atoms as well.

The displacement of an atom from its lattice position is called bulk defect. It can be partially recovered with annealing, described later with more detail, but has permanent effects resulting in the introduction of new energy levels that modify the effective doping and may act as generation or recombination centres. These recombination centres may trap the charge generated by the ionizing particles reducing the signal amplitude and degrading the performance of the detector.

The damage induced to the lattice differs from particle type and energy. In a collider experiment a wide spectrum of particles of any energy interact with the detectors. An absolute measurement of the radiation induced damage can be obtained by means of the Non-Ionizing Energy Loss (NIEL) hypothesis [12]. It assumes that the damage induced by a given fluence of any particle can be scaled to the equivalent fluence of a 1 MeV neutron taken as reference particle.

The correction factor is obtained by weighting the fluence with the energy dependent damage cross section $D(E)$, shown in figure 2.8, and normalizing it to the

integrated fluence and the damage cross section of the reference particle

$$k = \frac{\int D(E)\Phi(E)\,\mathrm{d}E}{D_n(1MeV)\int \Phi(E)\,\mathrm{d}E}, \tag{2.22}$$

giving the equivalent fluence

$$\Phi_{eq} = k\Phi = k\int \Phi(E)\,\mathrm{d}E. \tag{2.23}$$

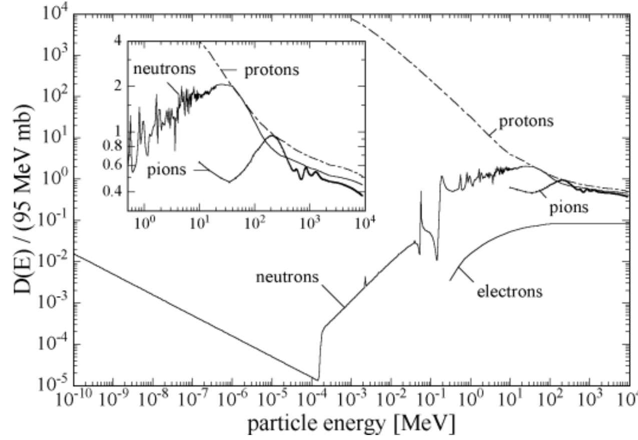


Figure 2.8: Displacement damage function $D(E)$ normalized to 95 MeV mb for neutrons, protons, pions and electrons. The normalization is such to show the damage equivalent to 1 MeV neutrons [13].

Using the NIEL hypothesis it is possible to evaluate the 1 MeV equivalent fluence on a detector at any point of its lifetime in the experiment, as well as the one induced on prototypes at irradiation facilities. This allows to evaluate the behaviour of the sensors in the experiment studying the damages on sensors exposed to the equivalent fluence at irradiation facilities.

In this thesis different irradiated sensors will be described. These sensors have been irradiated with thermal neutrons in the TRIGA reactor of the Jozef Stefan Institute in Ljubljana ($k = 0.9$). All the fluences will be quoted in 1 MeV equivalent neutrons by means of the NIEL hypothesis in the rest of the thesis.

Doping Concentration

The effect of radiation damage in the detector bulk can be described as a change of effective doping. Before irradiation the effective doping of a *p-type* sensor may be described as the difference of the acceptor and donor dopants concentrations $N_{eff,0} = N_A - N_D$. After irradiating the detector to a fluence Φ the effective doping

concentration is given by the formula

$$N_{eff}(\Phi) = N_{eff,0} - N_c\left(1 - e^{-c\Phi}\right) + g_c\Phi. \quad (2.24)$$

N_c and c describe the size and speed of the acceptor removal phenomenon while g_c describes the radiation induced acceptor introduction [14]. With $g_c = 2 \cdot 10^{-2}\,\mathrm{cm}^{-1}$ [15], while $N_c \sim N_{eff,0}$ and $c = 0.36 \cdot 10^{-14}\,\mathrm{cm}^{-2}$ have been measured on samples with $20\,\Omega\mathrm{cm}$ substrate resistivity [16].

From equation 2.10 a change in the effective doping concentration lead to a change of resistivity that affect the depth of the depleted volume for a given bias voltage, see equation 2.13.

Trapping

The charged defects in the bulk may also act as trapping centers for charge carriers. Since the release time is typically larger than the collection time, the trapped charge will not contribute any more to the signal, reducing the signal amplitude. The collected charge is therefore a function of the fluence

$$Q(\Phi) = Q_0 e^{-t_c/\tau} \quad \text{with} \quad \tau = (\beta_T\Phi)^{-1}. \quad (2.25)$$

In this equation Q_0 is the initial charge, i.e. the charge collected before irradiation, t_c is the collection time and τ is the trapping time that is inversely proportional to the fluence by a factor β_T that depends on the charge carrier and on the radiation type [17].

The trapping time is similar for electrons and holes but, since the collection time of holes is larger than the one of electrons because of the different mobility, trapping is more effective on holes whose contribution to the signal will eventually become negligible at large enough fluence.

Leakage Current

The damage induced by the radiation also has the effect of creating new energy levels in the silicon. When these energy levels are located within the band gap, they reduce the energy needed to promote an electron to the conduction band and therefore act as a generation center. This leads to an increase of leakage current I_{leak} that is proportional to the fluence and to the depleted volume V

$$I_{leak}(\Phi) - I_{leak}(0) = \alpha\Phi V, \quad (2.26)$$

where the proportionality factor α is the current-related damage rate. The value of α after an annealing of 80 minutes at 60°C is $3.99 \cdot 10^{-17}$ A/cm [13], see figure 2.9 .

The increase of leakage current can be compensated by lowering the operational temperature of the detector, see equation 2.14. While silicon detectors can normally be operated at room temperature, in irradiated devices the increase of leakage current can have a self-heating effect that leads to thermal runaway. For this reason a proper cooling is mandatory when silicon devices are used in a radiation harsh environment.

Annealing

Not all the radiation induced defects are fixed, their evolution with time is called annealing. The annealing process is temperature dependent and can be accelerated warming up the irradiated sensor or slowed cooling it down.

As shown in figure 2.9, annealing is always beneficial on the current-related damage rate parameter α, mitigating the radiation induced increase of leakage current.

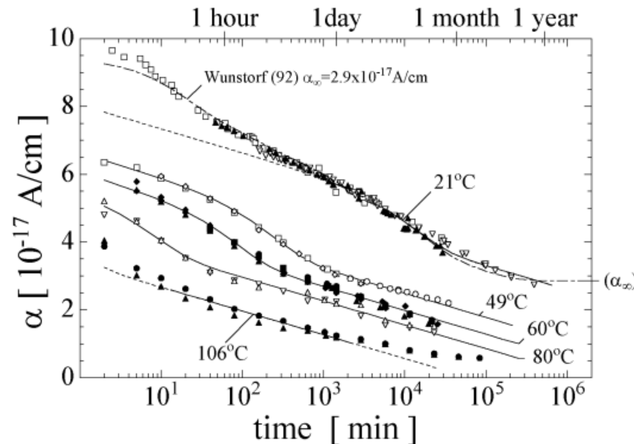


Figure 2.9: Simulation (dashed lines) and measurements (points) of the current-related damage parameter α time evolution for different annealing temperatures [13].

On the effective doping concentration N_{eff} instead, it initially has a beneficial effect given by a reduction of N_{eff} resulting in a larger resistance an hence a larger depletion depth at the same bias voltage. Afterwards, the effect is opposite with a long term reverse annealing where N_{eff} is pushed to larger values, see figure 2.10.

Irradiated sensors are usually annealed for 80 minutes at 60 °C before the rise of the reverse annealing. Later, they are kept at low temperature both during operation and storage.

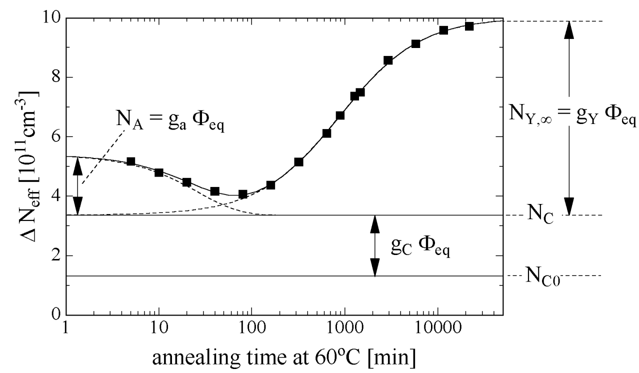


Figure 2.10: Evolution of the radiation induced change in the effective doping concentration ΔN_{eff} with respect to the annealing time at 60°C for a diode irradiated to the fluence of $1.4 \cdot 10^{13}\,\mathrm{n_{eq}/cm^2}$ [13].

Chapter 3

The ATLAS Experiment

The Large Hadron Collider (LHC) is the largest and most powerful particle accelerator ever built, capable of delivering unprecedented luminosity and collision energy. It is located at the European Organization for Nuclear Physics (CERN) in Geneva, Switzerland.

The LHC accelerates protons in bunches of 10^{11} particles with a temporal separation of 25 ns on two independent circular pipes where the particles run in opposite directions. The two pipes have four intersection points where proton-proton (p-p) collisions are generated at a frequency of 40 MHz with a center of mass energy of 14 TeV at the design luminosity of $10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. The LHC also provides heavy ions collisions, in particular of lead nuclei, at 5.5 TeV per nucleon pair, at the design luminosity of $10^{27}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$.

LHC is the last stage of a complex of accelerators at CERN, each machine accelerate the particles to its maximum capabilities before injecting them to the next stage. The protons colliding in LHC come from an hydrogen bottle from which the gaseous hydrogen atoms are extracted and ionized before being accelerated in bunches by a linear accelerator (LINAC 2) to the energy of 50 MeV. Afterwards they are accelerated by the proton synchrotron booster to 1.4 GeV that sends the bunches of particles to the Proton Synchrotron (PS) where they reach the energy of 25 GeV. From the PS the protons are transferred to the Super Proton Synchrotron (SPS) where they are accelerated to 450 GeV before being injected in the two beam pipes of LHC where they travel in opposite direction until they reach the collision energy, see figure 3.1.

For the heavy ions the acceleration process is similar to the protons one. Lead ions are vaporized and initially accelerated by the LINAC 3 linear accelerator, subsequently they are stored in the Low Energy Ion Ring (LEIR) before being injected in the PS from where they follow the same path described for protons.

Two general purpose experiments are hosted at two opposite collision points of LHC. The ATLAS (A Toroidal LHC ApparatuS) and CMS (Compact Muon Solenoid)

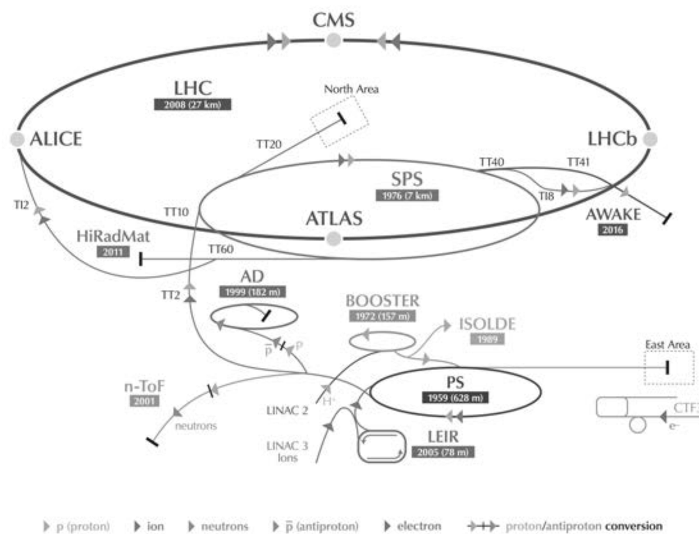


Figure 3.1: Scheme of the CERN accelerators complex [18].

experiments. Both ATLAS and CMS look at the final state of the p-p and heavy ions collisions produced by the LHC, searching for new physics, as well as to perform precision measurement on the Standard Model parameters.

The LHC periodically stop operations for maintenance and improvements. It is foreseen that during the long shut-down that will take place in 2023 the machine will be upgraded to High Luminosity LHC (HL-LHC) improving the luminosity capability of about a factor five to $5 \div 7 \cdot 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. The experiments at LHC will also have to upgrade their detectors to face the new requirements lead by the higher luminosity, to face a larger occupancy and pile-up level in a very radiation harsh environment.

In this chapter the physics program of ATLAS at LHC and HL-LHC is shown with a description of the ATLAS experiment together with the ATLAS upgrade plan. More details are given about the Inner Tracker (ITk) and the High Granularity Timing Detector (HGTD), where the silicon detector technologies object of this thesis find their application.

3.1 ATLAS Physics at LHC and HL-LHC

Before the LHC time the experimental particle physics knowledge was mostly determined by the measurements performed at LEP and Tevatron. The experiments located at these accelerators contributed significantly to the field with, among other achievements, the discovery of the Z and $W^{\pm}$ vector boson and heavy quarks predicted by the SM.

After the LEP and Tevatron era the observed Standard Model particle zoo was

almost complete. The fermion sector includes three leptons e, μ and τ, with the corresponding neutrinos ν_e, ν_μ and ν_τ and six quarks u, d, c, s, t and b. To each fermion also corresponds an antiparticle partner. The gauge bosons of the SM are the photon and the Z and $W^\pm$ vector bosons in the electroweak sector and the gluon in the strong nuclear sector.

The SM predicted the existence of an additional particle, the Higgs boson, a scalar boson required by the mass generating mechanism to provide rest mass to elementary particles. The experiments at LEP and Tevatron did not observe the Higgs boson but defined exclusion mass regions.

With the larger collision energy, the LHC allowed to explore the mass regions that previous experiments did not yet exclude and, as previously stated, brought to the discovery of the Higgs boson in 2012 by both the ATLAS and CMS experiments.

The physics program of LHC experiments is not concluded with the observation of the Higgs boson. The large statistics of high energy collisions allow to perform precision measurements of SM parameters and the unprecedented energy of the collisions could show evidences of new physics as predicted by BSM theories in the case these are true. The upgrade of LHC to HL-LHC will allow to further explore new physics scenarios with larger statistics needed to suppress uncertainties on rare processes.

In the following sections some examples of the physics measurements achievable by ATLAS at LHC and HL-LHC are given.

3.1.1 Vector Bosons

A precise measurement of the $W^\pm$ boson mass is a tool to prove the consistency of the SM theory [19]. Previous observation established the $W^\pm$ mass to the value of $80.387 \pm 0.016\,\text{GeV}$. LHC measurements could reduce the uncertainties of about an order of magnitude. ATLAS first measurements with a sample of $4.6\,\text{fb}^{-1}$ at $\sqrt{s} = 7\,\text{TeV}$ from Run-1 give $m_W = 80.370 \pm 0.019\,\text{GeV}$ [20]. The statistical uncertainty is of $7\,\text{MeV}$ and with the full LHC data set will become negligible, while the main contribution to the uncertainty is given by the physics-modelling systematic uncertainty, in particular from the uncertainties on the partons distribution functions (PDFs).

Therefore, this measurement would not profit by the larger statistics available at HL-LHC since the statistical uncertainty is already the smaller contribution to the total uncertainty that can only be improved with improvements on the systematics.

3.1.2 The Top Quark

The top quark will be produced in large quantities at the LHC, so that not only the mass but production cross section, branching ratios and coupling constants can

be precisely measured. For the mass measurement the cleanest channel would be from the $t\bar{t}$ pair production with the tops decaying in $t \to Wb$ and one W decaying leptonically and the other hadronically. These events have a clear signature given by two b-tagged jets, one lepton and missing transverse energy. The top mass would be measured from the top with three jets in the final state.

A first measurement of the top mass with ATLAS data from Run-1 at $\sqrt{s} = 7\,\text{TeV}$ returns $m_t = 174.5 \pm 2.4\,\text{GeV}$ [21], compatible with the combined measurement of CDF and D0 at Tevatron, $m_t = 172.6 \pm 1.4\,\text{GeV}$ [22]. Again, the largest contribution to the uncertainties comes from the theoretical model and a larger amount of data would marginally improve this measurement.

Rare decay modes of the top quark have an enhanced branching ratio in many BSM theories that foresee flavor changing neutral currents. In these theories, decays such as $t \to Zq$, with $q = u$ or c, may be observed, but, depending on the actual branching ratio, the full statistics of HL-LHC may be needed.

3.1.3 The Higgs Boson

The main achievement of the experiments at LHC so far has been the discovery of the Higgs boson. The updated measurement of its mass, averaging the results of both ATLAS and CMS in all decay channels gives $m_H = 125.18 \pm 0.16\,\text{GeV}$ [9].

After the determination of the Higgs boson mass the precise measurements of other parameters are being carried out. Among them, the determination of the spin and the CP quantum numbers is of primary importance to confirm that the observed boson is the one responsible of mass generation. Branching ratios, coupling to the other particles and self coupling can also be measured. Due to the low production rate, the measurements of couplings and branching ratios will highly benefit by the tenfold increase of statistics in HL-LHC.

3.1.4 Beyond Standard Model Physics

Supersymmetry (SUSY) provides the most promising class of theories beyond standard model for which evidence could be found at the LHC. If SUSY particles had masses at the electroweak scale, the LHC should have been able to produce them in large quantities. These supersymmetric particles would have afterwards decayed in steps to the lightest supersymmetric particle that, if R-parity is preserved, will be stable. As well as neutrinos, SUSY particles will not interact with the ATLAS detectors, the evidence of SUSY at the LHC experiments would be given by an excess at large values of missing transverse energy not justifiable by any SM interaction.

At the time of writing no evidence of SUSY particles has been observed. The ATLAS and CMS experiments increased the exclusion region in the gluino-neutralino

and in the squark-neutralino mass planes [23]. The upgrade to HL-LHC can extend the up to 3 TeV the mass reach for SUSY particles.

Besides SUSY, LHC and HL-LHC could bring to the discovery of particles whose existence is foreseen by other theories such as technicolor resonances, heavy quarks and leptoquarks.

3.2 Overview of the ATLAS Detector

ATLAS is a large size general purpose detector located in a cavern approximately 100 m underground around the interaction point 1 of the LHC. It has a shell structure with cylindrical and forward-backward symmetry with respect to the beam axis. Each shell corresponds to a specific purpose detector system for charged particle tracking, electromagnetic and hadronic calorimetry and muon detection. The magnet configuration comprises a thin superconducting solenoid surrounding the tracking system and three large superconducting toroids, two at the end-caps and one barrel surrounding the calorimeters providing bending power for the muon spectrometer.

The ATLAS detector is 44 m long with a diameter of 25 m for a total weight of about 7000 tonnes. A sketch of it is shown in figure 3.2.

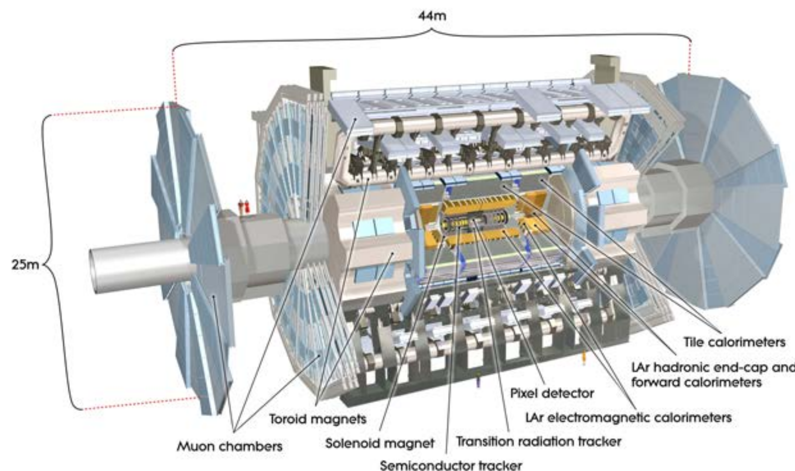


Figure 3.2: Cut-away view of the ATLAS detector. Its total dimensions are 25 m in height and 44 m in length for an overall weight of about 7000 tonnes [24].

For a better description of the detector system the definition of the coordinate system and the nomenclature used to describe the ATLAS detector and the particle produced in the p-p collisions is given. As origin of the coordinate system the nominal intersection point is taken, while the beam direction defines the z-axis and the x-y plane is transverse to the beam direction. The x-axis points to the centre of the LHC ring and the y-axis is defined as pointing upwards. The azimuthal angle ϕ is measured

around the beam axis, and the polar angle θ is the angle from the beam axis. The pseudorapidity is defined as $\eta = -\ln\tan(\theta/2)$ and the transverse momentum p_T, the transverse energy E_T, and the missing transverse energy E_T^{miss} are defined in the x-y plane. The distance ΔR in the pseudorapidity-azimuthal angle space is defined as $\Delta R = \sqrt{\Delta\eta^2 + \Delta\phi^2}$ [24].

3.3 Inner Detector

The Inner Detector (ID) is the innermost ATLAS detector system. It measures with high resolution the trajectory of the charged particles produced in the p-p collisions. The high resolution tracks are extrapolated to their origin, associating each track with a primary collision vertex or to a late decay (secondary vertex). The ID is submerged in a 2 T solenoidal magnetic field, described in section 3.6, that bends the particle trajectories giving information on their momentum.

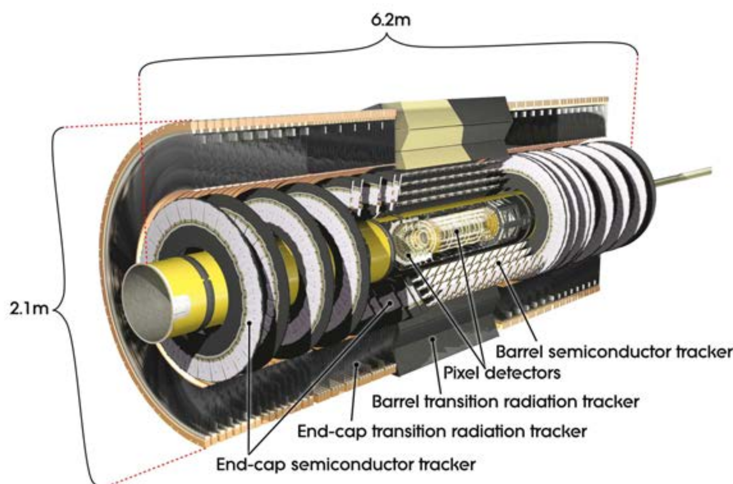


Figure 3.3: Cut-away view of the ATLAS Inner Detector [24].

The ID consists of three sub-detectors: the Pixel Detector [25] which includes the Insertable B-Layer (IBL) [26], the SemiConductor Tracker (SCT) [27] and the Transient Radiation Tracker (TRT) [28], see figure 3.3. The ID extends over a length of 6.2 m with a total diameter of 2.1 m. The Pixel and SCT sub-detectors provide precision tracking in the pseudorapidity region $|\eta| < 2.5$. They are arranged in concentric cylinders around the beam axis in the barrel region and, in the end-cap region, they consist of disks perpendicular to the beam axis.

3.3.1 Pixel Detector

The Pixel Detector originally consisted of three barrel layers at the radius of 5.1, 8.9 and 12.3 cm with a length of 80 cm. In 2015 the IBL [26] was installed adding an inner layer at 3.2 cm from the beam axis and covering the z region $\mid z \mid < 33.2$ cm. At the two ends of the Pixel Detector three end-cap discs of radial extension 8.9 cm $< R <$ 15.0 cm are placed at $\mid z \mid =$ 49.5, 58.0 and 65.0 cm.

The sensors in the three outer layers of the Pixel Detector and end-caps are standard n-in-n planar sensors with pixel size of $50 \times 400\,\mu\text{m}^2$. Each pixel module is made of 2×8 FE-I3 readout chips [29] bump-bonded to a sensor tile of area $63.4 \times 24.4\,\text{mm}^2$ and 250 μm thickness. A flexible printed circuit board is glued on top of the sensor tile to connect the module hybrids with the outer world.

The innermost layer, the IBL, has been installed with the aim of improving the impact parameter resolution and the identification capability of long-lived particles such as b hadrons. In addition it guarantees fulfilment of the Pixel Detector benchmark requirements after radiation damage.

In IBL two different pixel sensor technologies are present. The central part (75%) is made of n-in-n planar sensors while n-in-p 3D sensors are placed at the ends of the barrel (25%). Both sensor types have a pixel size of $50 \times 250\,\mu\text{m}^2$ and are interconnected to the FE-I4 readout chip [30].

The Pixel Detector is the ATLAS sub-detector closest to the interaction point and, as a consequence, the most exposed to radiation damage, see figure 3.4. The IBL was designed to survive an integrated luminosity of $550\,\text{fb}^{-1}$, the estimated luminosity accumulated before the replacement of the Inner Detector for the HL-LHC upgrade. This luminosity is equivalent to a total fluence of about $5 \cdot 10^{15}\,\text{n}_{\text{eq}}/\text{cm}^2$, including a safety factor of 1.5.

3.3.2 SemiConductor Tracker

The SCT is a microstrip detector distributed in four barrel layers and nine end-caps per side. The barrels have radii of 30.0, 37.3, 44.7 and 52.0 cm for a length of 149 cm. Each layer consists of two strip sensors with a small stereo angle of 40 mrad to provide 2D information of the track position. The end-caps are located at different distances from the nominal interaction point in the range 85 cm $<\mid z \mid<$ 272 cm with an outer radius of 56 cm and different inner radii from 27 to 44 cm, with a larger inner radius at larger $\mid z \mid$. The SCT covers with instrumented detectors the pseudorapidity region $\mid \eta \mid < 2.5$.

The microstrip sensors that build the SCT are made of p-in-n silicon sensors of different pitches. The barrel sensors all have 80 μm pitch wile the end-cap sensors

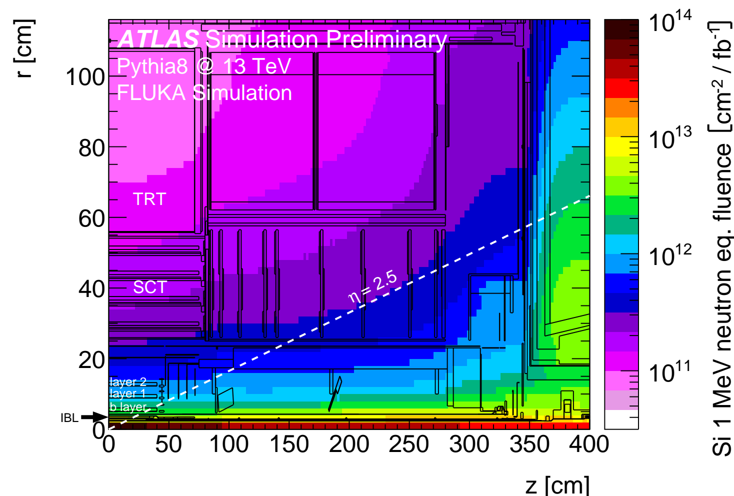


Figure 3.4: $1\,\mathrm{MeV}\,\mathrm{n_{eq}}/\mathrm{cm}^2$ fluence per fb^{-1} of integrated luminosity in the ATLAS Inner Detector. The minimum bias *p*-*p* events are simulated at 13 TeV center of mass energy with an inelastic cross section of 78.8 mb. Particle tracking and interactions with the detector material are simulated with the FLUKA 2011 code using the Run-2 geometry description of the ATLAS detector [31].

ranges from 50.9 to 90.4 μm.

3.3.3 Transient Radiation Tracker

The TRT is the only element of the Inner Detector that is not based on silicon sensors. It is a gas detector that consists of 4 mm diameter straw-tubes filled with an gas mixture of xenon, carbon dioxide and oxygen (70/27/3) having a 31 μm diameter gold-plated tungsten anode wire in the center. Between the walls of the straw-tube and the tungsten wire there is an electric potential difference of about 1500 V which allows to collect the ionization charge and to measure the track position with a 130 μm resolution per straw.

The TRT barrel is made of totally 52544 straws of 1.44 m length along the beam direction covering the radius $56\,\mathrm{cm} < R < 107\,\mathrm{cm}$. The two end-caps instead are made of 122880 straws each distributed along the beam axis and covering the radius $64\,\mathrm{cm} < R < 100\,\mathrm{cm}$ at $85\,\mathrm{cm} <| z |< 271\,\mathrm{cm}$.

3.4 Calorimeters

In particle physics a calorimeters is a detector whose purpose is to measure the energy of impinging particles, which are usually stopped in the detector, generating a signal that depends on the amount of energy deposited. Two types of calorimeter

exists. Homogeneous calorimeters are sensitive in the entire detector volume and all the deposited energy contributes to the signal. Sampling calorimeters consist of two different elements, an absorber and a sensitive part. The sampling calorimeter approach allows to design more compact detectors that have to be carefully calibrated to obtain the particle energy from the measured energy deposited.

The ATLAS calorimeter system consists of three sampling calorimeter sub-detectors surrounding the Inner Detector: the Electromagnetic, the Hadronic and the Forward calorimeters, see figure 3.5. Together the calorimeter system covers the pseudorapidity region $|\eta| < 4.9$.

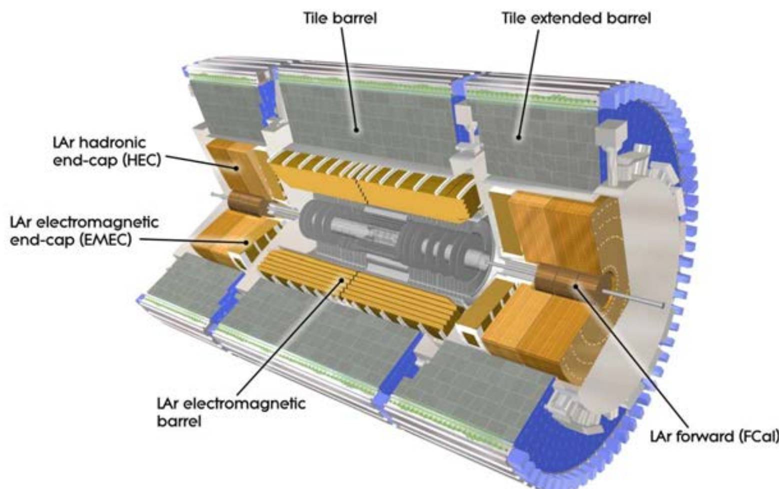


Figure 3.5: Cut-away view of the ATLAS calorimeter system [24].

3.4.1 Electromagnetic Calorimeter

The Electromagnetic Calorimeter (ECAL) is the closest element to the interaction point of the calorimeter system. It is designed to absorb electrons and photons in the energy range $50\,\text{MeV} \lesssim E \lesssim 3\,\text{TeV}$ and measure their energy and impinging direction. Moreover it also participates to the reconstruction of hadronic jets that start their shower in the ECAL volume.

The ECAL consists of lead absorber and liquid argon detector distributed in accordion shaped layers covering the pseudorapidity range $|\eta| < 3.2$ with a barrel ($|\eta| < 1.475$) and two end-cap wheels per side ($1.375 < |\eta| < 2.5$ and $2.5 < |\eta| < 3.2$). The accordion shaped structure allows full ϕ coverage without azimuthal cracks.

The thickness of electromagnetic calorimeters is usually measured in units of radiation length X_0, defined as the distance after which the particle energy is reduced by a factor $1/e$. The ATLAS ECAL has a thickness greater than $22\,X_0$ in the barrel

and greater than $24\,X_0$ in the end-caps, ensuring the full confinement of the electromagnetic showers.

3.4.2 Hadronic Calorimeter

The Hadronic Calorimeter (HCAL) measures the energy of particles that escape the electromagnetic calorimeter. These are usually high energy jets originating from quark and gluon hadronization. The HCAL absorbs all the remaining standard model particles from the collisions except for muons, which also leave a track in the muon spectrometer, and neutrinos that leave the ATLAS detector without depositing energy in any sub-detector.

The HCAL consists of two parts, the Tile Calorimeter (TileCal) in the central region and the Hadronic End-Cap Calorimeter (HEC) in the forward region. The TileCal uses steel as absorber medium and scintillator tiles as active region. The charged particles of the hadronic showers crossing the scintillator tiles generate photons that are collected by photomultipliers. The TileCal covers the pseudorapidity region $|\eta| < 1.7$ with a central barrel in the $|\eta| < 1.0$ region and two extended barrels covering the region $0.8 < |\eta| < 1.7$. It extends radially from 2.28 m to 4.25 m and is split in three sections of 1.5, 4.1 and 1.8 interaction lengths (λ) in the central barrel, and 1.5, 2.6 and $3.3\,\lambda$ in the extended barrels, where λ is the distance after which the number of element of the hadronic shower is reduced by a factor $1/e$.

On the other hand, the HEC uses copper as absorption medium and liquid argon as active one. It covers the pseudorapidity region $1.5 < |\eta| < 3.2$ with two wheels on each side.

3.4.3 Forward Calorimeter

The Forward Calorimeter (FCAL) consists of an electromagnetic and two hadronic parts placed at the $3.1 < |\eta| < 4.9$ range to maximize the calorimeter acceptance at low radii. In all the FCAL sub-detectors liquid argon is used as detector medium while the absorbers are copper based in the electromagnetic part and tungsten based in the hadronic ones. The electromagnetic part of the FCAL has a depth of $27.6\,X_0$ while the two hadronic parts measure 3.62 and $3.55\,\lambda$ [32].

3.5 Muon Spectrometer

Muons cross both the electromagnetic and hadronic calorimeters without being stopped. To tag muon tracks and improve their momentum resolution a dedicated Muon Spectrometer surrounds the calorimeters. The Muon Spectrometer, see figure 3.6, consists of four sub-detectors covering the region $|\eta| < 2.7$: the Monitored Drift-Tube (MDT)

Chambers, the Cathode Strip Chambers (CSC), the Resistive Plate Chambers (RPC) and the Thin Gas Chamber (TGC).

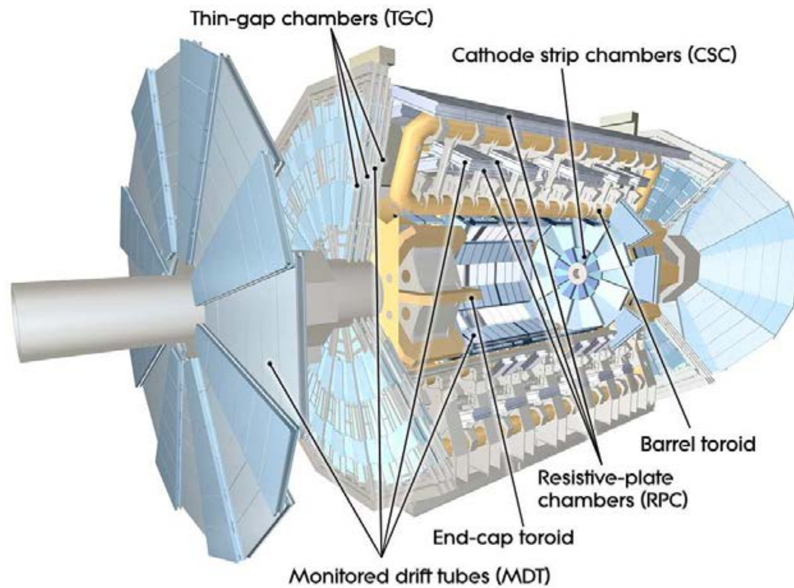


Figure 3.6: Cut-away view of the ATLAS muon system [24].

3.5.1 Monitored Drift-Tube Chambers

The MDT consists of drift chambers that provide the muon momentum resolution measuring the curvature of the muons' tracks in the magnetic field produced by the toroid magnets described in section 3.6. The drift chambers unit elements are 400 μm thick aluminium drift tubes with a diameter of 3 cm filled with a mixture of argon and carbon dioxide (91/7). The length of the drift tubes varies from 0.9 to 6.2 m. A total of 1150 chambers are installed summing up to 354000 drift tubes achieving a position resolution of $35 \div 40\,\mu$m for 6 or 8 layers chambers. The MDT chambers are distributed over three barrel layers located at approximately 4.5, 8 and 10 m from the beam axis and three end-cap layers at $\mid z \mid$ approximately 7.5, 14 and 21.5 m covering the region $\mid \eta \mid < 2.7$.

During the 2016/17 winter shut-down, new MDT tubes with a smaller diameter of 1.5 cm were installed to improve the muon momentum reconstruction [33].

3.5.2 Cathode Strip Chambers

The CSC consists of two end-caps covering the pseudorapidity range $2.0 <\mid \eta \mid< 2.7$ to improve the muon momentum measurement in the forward region with multi-wire proportional chambers with segmented cathodes reaching a position resolution of

$60\,\mu$m. It is formed by 32 chambers of four layers each filled with a mixture of argon and carbon dioxide (80/20).

The chambers are arranged to form two disks placed at $\mid z \mid = 7$ m extending radially between 88 and 208 cm.

3.5.3 Resistive Plate Chambers

The RPCs are used for muon triggering while providing an additional position measurement along the MDT in the non-bending plane. They consist of resistive parallel plates made of phenolic-melaminic plastic laminate kept at a distance of 2 mm. The volume between the plates is filled with a mixture of $C_2H_2F_4$/Iso-C_4H_{10}/SF_6 (94.7/5/0.3) and the two plates are biased at about 10 kV. The RPCs cover the pseudorapidity region $\mid \eta \mid < 1.05$.

3.5.4 Thin Gap Chambers

The TGCs are multi-wire proportional chambers covering the forward region in the range $1.05 < \mid \eta \mid < 2.4$. They carry out two functions in the end-cap muon spectrometer: extend the muon trigger capability and determine the azimuthal coordinate to complement the MDT measurement.

The chambers are characterized by a wire to cathode distance of 1.4 mm and an inter-wire distance of 1.8 mm. The chamber volume is filled with a mixture of carbon dioxide and n-C_5H_{12} (55/45) and the wire is biased at about 2.9 kV. Each chamber provides a spatial resolution of 1 mm and a time resolution of 5 ns.

3.6 Magnet System

The ATLAS magnet system consists of four large superconducting magnets. A solenoid magnet surrounding the Inner Detector and aligned to beam axis provides a 2 T axial magnetic filed for charged particles momentum determination, and a barrel and two end-cap toroids which produce a toroidal magnetic field of approximately 0.5 T and 1 T to bend muon tracks in the MDT region.

3.6.1 Central Solenoid

The Central Solenoid provides a 2 T axial magnetic field at the nominal current of 7.73 kA. The design of the magnet has been carried out with the goal of minimizing the material budget to reduce the disturbance on the calorimetric measurements. The coil is wound with a Al-stabilized NbTi conductor developed for this application in

order to achieve high magnetic field with reduced thickness. In terms of radiation length, the total thickness of the solenoid is of $\sim 0.66\,X_0$ [34].

The inner diameter of the solenoid is of 2.47 m and the outer one is of 2.56 m, the axial length is of 5.8 m. The total mass is of 5.7 tonnes and the stored energy is 40 MJ.

3.6.2 Barrel Toroid

The Barrel toroid consists of eight coils 25.3 m long and 10.7 m high, placed at about 9 m from the beam axis. The coils are made of Nb/Ti/Cu conductor, the same material used for the End-Cap Toroids, and carry a nominal current of 20.5 kA generating a toroidal magnetic field in the MDT region with a peak of 3.9 T and storing an energy of 1.08 GJ.

3.6.3 End-Cap Toroids

The role of these toroids is to generate the magnetic field to enhance the bending power in the end-cap regions of the muon spectrometer. Each End-Cap Toroid consists of eight flat coils elements extending from a radius of 83 cm to 5 m for a total weight of 239 tonnes per side. The magnetic field in the bore range from 0.2 to 3.5 T at the nominal current of 20.5 kA.

3.7 Forward Detectors

In addition to the detector systems around the interaction point, other detectors are located in the very forward region, far from the interaction point and very close to the beam axis. These detectors have been designed for dedicated measurements, such as luminosity determination and diffractive physics.

3.7.1 ALFA

The ALFA detector is located at 240 m from the interaction point in four Roman Pots, two per each side, that can be moved from the garage position to the measurement one for dedicated data taking runs. Its purpose is to measure elastic p-p scattering. The protons that reach the ALFA detectors arrive intact and with an energy close to the one of the beam, they are detected by a system of scintillating fibres arranged orthogonally to provide a 30 μm resolution in both directions.

3.7.2 LUCID

The LUCID detector measures inelastic p-p scattering in the forward region to measure the integrated luminosity delivered to ATLAS as well as to provide online monitoring of the instantaneous luminosity. It is a Cherenkov light detector consisting of aluminium tubes filled with C_4F_{10} surrounding the beam pipe at $\mid z \mid = 17\,\mathrm{m}$.

3.7.3 AFP

The ATLAS Forward Proton (AFP) is a forward detector meant to be readout together with the ATLAS central detector system to look for diffractive events where one or both the protons leave intact from the collision with a small deflection angle. The protons are detected by AFP in the forward region while the main detector observes the central event.

The AFP detector system consists of four Roman Pots, two on each side at about 210 m from the interaction point, hosting a tracking and timing detector. The silicon tracker (SiT) consists of four silicon 3D pixel detectors planes mounted in each Roman Pot, providing proton tracking with a position resolution of about $10\,\mu$m and $30\,\mu$m in x and y respectively. The pixel detectors are a copy of the 3D detectors used in IBL. The time of flight (TOF) detector is based on Cherenkov radiating quartz bars coupled to a multi channel siclicon photomultiplier. The TOF is expected to provide timing information with a resolution of 20 ps to match the protons detected by AFP with the correct primary vertex.

AFP has been installed in two stages, in 2016 the one-arm AFP was installed with only the tracker elements of two Roman Pots of the same side have been placed, and in 2017 the full detector was installed. While the TOF was not installed AFP took data at low luminosity where unambiguous matching with the primary vertex is possible.

3.8 Trigger System

The readout of all the ATLAS sub-detectors has to be performed such that the information from interesting collisions is recorded, while the events that do not belong to relevant physics interactions are descarded.

The ATLAS Trigger System is designed to select the relevant interactions, based on the physics program, discarding online most of the less interesting data. The trigger algorithms to be used have to adapt to the different conditions that may occur during the data taking time. For example, during Run-1 collisions were occurring every 50 ns at a center of mass energy of $\sqrt{s} = 7\,\mathrm{TeV}$, while in Run-2 both collision

frequency and energy have been doubled together with the peak luminosity that reached a value of about $1.6 \cdot 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, larger than the LHC design luminosity.

The trigger system is organized in a multilevel architecture, see figure 3.7. The first trigger level (L1) is synchronous with the 40 MHz bunch crossing clock and has a latency of $2.5\,\mu$s and an output rate of 100 kHz rejecting over 99% of the events. It processes coarse information from dedicated detectors in the muon detector system and in the calorimeters looking for high energy activity. Within the latency of L1 no tracking information is available and regions of interest (ROI) are roughly defined by sectors of the muon system and calorimeters.

The High Level Trigger (HLT) has been upgraded for Run-2 integrating the Level-2 and the Event Filter in a single more efficient and flexible processor [35]. At the HLT a preliminary reconstruction of physics objects is available with candidate particle identification and direction information extracted from the calorimeters. The output rate of the HLT is of 1 kHz, imposed by the data storage constraints.

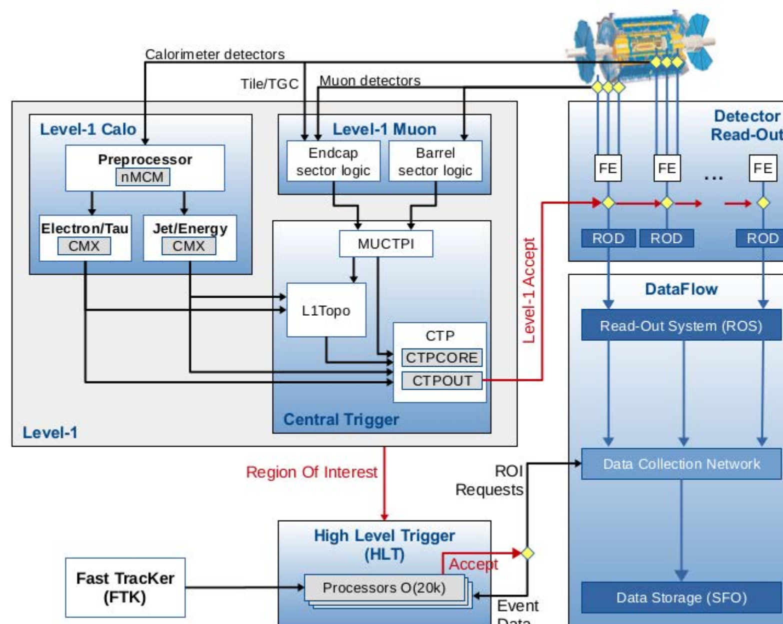


Figure 3.7: Schematic of the ATLAS trigger and data acquisition system [35].

In dedicated low luminosity runs the Minimum Bias Trigger Scintillators (MBTS) are used to provide unbiased trigger signals. The low luminosity runs are taken for specific measurements and studies such as luminosity measurement calibration, forward physics program or heavy ion collisions. The MBTS is mounted in the face plate of the electromagnetic end-cap calorimeter.

3.9 The ATLAS Upgrade

The High Luminosity LHC will set new challenging requirements on the ATLAS detectors. It is foreseen to start operating in 2026, providing *p*-*p* collisions at unprecedented peak luminosity, leading to an average of ~ 200 inelastic *p*-*p* collisions per each bunch crossing. The goal of the HL-LHC upgrade is to extend the dataset from $\sim 400\,\mathrm{fb}^{-1}$, collected at the end of the LHC era, to $\sim 4000\,\mathrm{fb}^{-1}$ by the end of the HL-LHC program, approximately in 2036.

The increase of the dataset over an order of magnitude in a reasonable time scale is only achievable rising the luminosity of the colliding machine. The upgrade will not affect the collision energy so that HL-LHC will not push further the energy frontier but the large increase of the data sample will allow to significantly reduce the statistical uncertainties extending and improving the LHC physics program [19].

At the time of the upgrade the performance of many of the ATLAS sub-detectors will be degraded by radiation damages and will have to be replaced. The harsher radiation environment and the higher number of tracks per event at the HL-LHC lead to substantial upgrades in the ATLAS detector systems to achieve at least the same performance as at the LHC [36].

The Inner Detector will be replaced with a new, more radiation hard and with finer granularity, full silicon detector, the Inner Tracker (ITk). The forward calorimeters and muon wheels will be replaced to face the larger flux and hence larger radiation damage while the barrel calorimeters and muon systems are expected to handle the higher luminosity without significant performance degradation.

3.9.1 Inner Tracker

The ATLAS tracking system needs to be upgraded in order to maintain a similar detector performance after the HL-LHC upgrade, where a larger pile-up and fluence have to be sustained. The larger pile-up will be faced with a finer granularity, while more radiation hard detectors are needed for the larger fluence. The baseline of the ITk detector will be discussed with its expected performances.

The ITk is a full silicon detector that consists of two subsystems: an inner Pixel Detector and an outer Strip Detector. The layout of the ITk includes four strip layers and five pixel layers in the barrel region, extended by six strip end-caps discs and a system of pixel end-cap rings to guarantee a tracker coverage up to $\mid \eta \mid = 4$, see figure 3.8.

The ITk has been designed to provide efficient pattern recognition and track reconstruction in order to deliver high track reconstruction efficiency and low rate of fake tracks. Robustness against losses of individual readout channels or entire

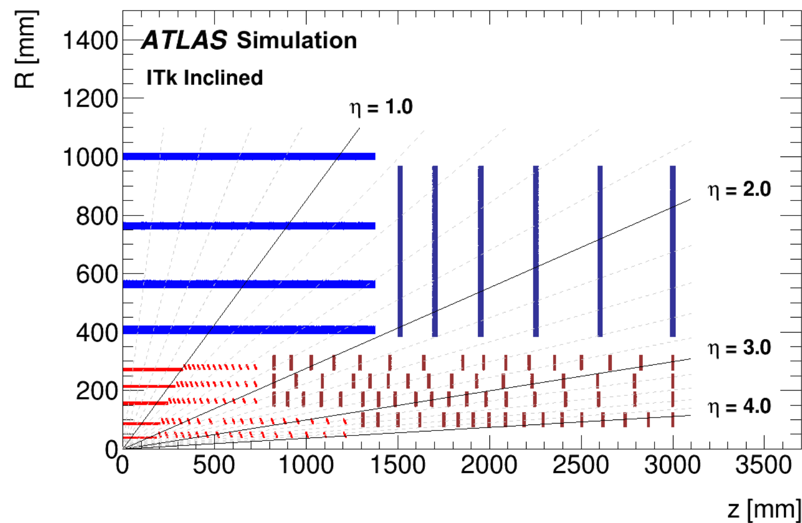


Figure 3.8: Layout of one ITk quadrant. The Strip Detector active elements are shown in blue while Pixel Detector ones are shown in red. Light colors are used for the barrel modules and dark colors for the end-cap modules [37].

modules that may occur over the detector lifetime has been also considered and a 15% or module failure can be afforded [38].

In the Strip Detector the modules are doubled with the two strip sensors having a small stereo angle among them. In the barrels, the modules are oriented to have the strips running almost parallel to the beam axis, while in the end-caps they follow the radial direction to measure the ϕ coordinate with high resolution. The stereo angle allows to additionally measure the z and R coordinates in the barrel and end-cap respectively.

Since the HV-CMOS detector technology discussed in this thesis is of particular interest for the Pixel Detector, it is described with more detail in the next section.

Pixel Detector Specification

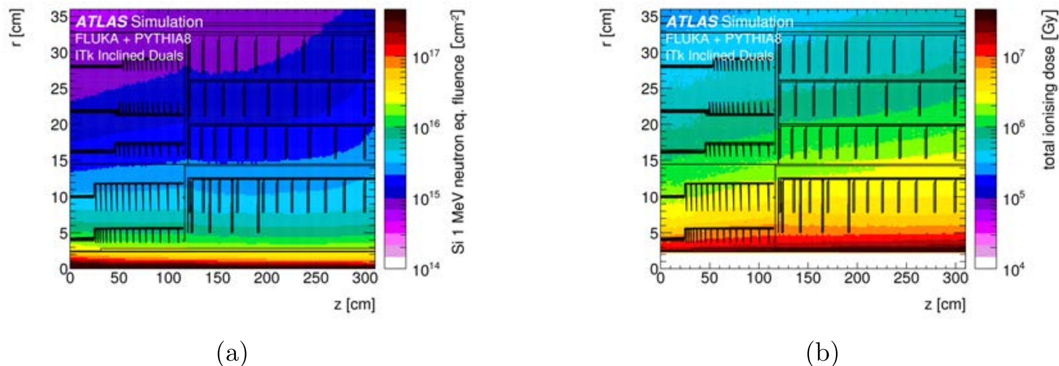
Different silicon sensor technologies are being considered for the Pixel Detector. In particular hybrid 3D and planar sensors, similar to those used in IBL, and monolithic or hybrid active pixel sensors.

Initially all the options were investigated for all layers. Eventually the hybrid approach, taking advantage from the IBL and ID experience, was selected. Depleted monolithic active pixel sensors are not yet excluded for the outermost layer where the radiation hardness requirement is less strict, and a large surface has to be covered favouring a more cost effective solution.

Both the sensor and the readout chip had to be redesigned to guarantee good

tracking performance over the lifetime of the HL-LHC. The ITk pixel modules have a reduced pixel size with respect to the IBL, $50 \times 50\,\mu\text{m}^2$ or $25 \times 100\,\mu\text{m}^2$, to improve track resolution and two-tracks separation. The readout chip has been designed to allow operation at a lower threshold to compensate signal loss due to radiation damage, the readout architecture has been improved to withstand the higher hit density and the chip power consumption per pixel has been reduced allowing to contain the material budget due to cables and cooling system. Moreover, the radiation tolerance has been increased moving from the IBM 130 nm technology used for the FE-I4 chip [30] to the TSMC 65 nm CMOS technology chosen by the RD53 collaboration [39] that is providing a readout chip for both the ATLAS and CMS Pixel Detectors upgrade.

However, a technology able to provide sensors and readout chips for the innermost layers of the ITk Pixel Detector sufficiently radiation hard to survive the full HL-LHC lifetime is not yet available. For this reason the detector design foresees the replacement of the two innermost layers at about $2000\,\text{fb}^{-1}$ integrated luminosity. The radiation hardness constraints are therefore defined by layer zero and layer three, the innermost layer to not be replaced, see figure 3.9 and table 3.1.



(a) (b)

Figure 3.9: Equivalent $1\,\text{MeV/cm}^2$ neutron fluence (a) and total ionizing dose (b) distribution in the ITk Pixel Detector normalized to $4000\,\text{fb}^{-1}$ [38].

The charge collection is degraded with fluence due to radiation damage, but it can be partially recovered by increasing the sensor bias voltage. For example, 3D detectors have an efficiency of 99% already at 1 V before irradiation, while a bias voltage of about 100 V has to be applied to achieve an efficiency of 97% after irradiation to $1.4 \cdot 10^{16}\,\text{n}_{\text{eq}}/\text{cm}^2$ [40]. The leakage current plays a relevant role in this situation because it increases with radiation and voltage, see section 2.2.4 and can lead to a thermal runaway if the power consumption exceed the cooling capability.

The choice of sensor technology for each detector region has to take into account the power dissipation together with efficiency over the lifetime. The baseline tech-

Luminosity [fb^{-1}]	Layer	Location	R [cm]	z [cm]	Fluence [10^{14} n_{eq}/cm^2]	Dose [MGy]
2000	0	flat barrel	3.9	0.0	131	-
			4.0	24.3	-	7.2
		inclined barrel	3.7	25.9	123	-
			3.7	110.0	-	9.9
		end-cap	5.1	123.8	68	6.3
2000	1	flat barrel	9.9	24.3	27	1.5
		inclined barrel	8.1	110.0	35	2.9
		end-cap	7.9	299.2	38	3.2
4000	2-4	flat barrel	16.0	44.6	28	1.6
		inclined barrel	15.6	110.0	30	2.0
		end-cap	15.3	229.2	38	3.5

Table 3.1: Maximal fluence and ionizing dose for the different ITk Pixel Detector parts in the scenario with replacement of the inner layers at the integrated luminosity of 2000 fb^{-1}. All the values include a safety factor of 1.5 [38].

nology for the innermost layer is given by 3D sensors, while for the other layers the installation of planar sensors is foreseen, see figure 3.10.

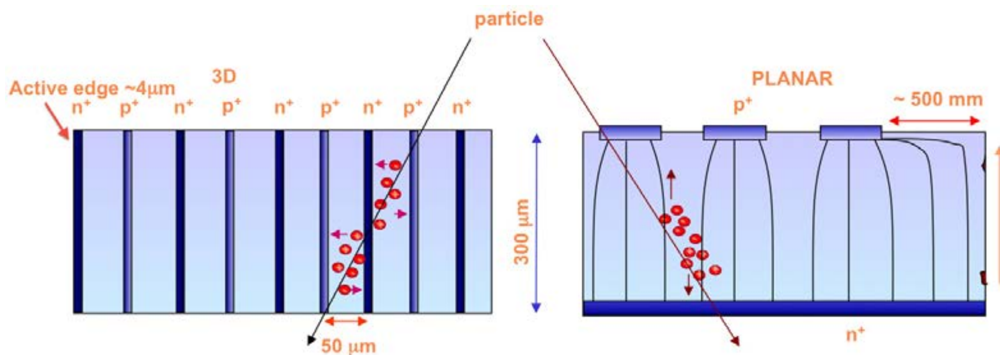


Figure 3.10: Schematic view of the electrode arrangement in 3D and planar pixel sensors [38].

The planar sensors will be fabricated in the n-in-p technology, although n-in-n, that is used in the current Pixel Detector was also investigated, but n-in-p has the advantage of a simpler and hence cheaper fabrication. After irradiation planar devices need a bias voltage much larger than 3D detectors [41]. The leakage current can be mitigated by reducing the sensor thickness and consequently reducing the volume contribution to the leakage current, but loosing charge at the same time, since it is proportional to the active thickness.

Both planar and 3D options require hybridization through bump-bonding to the RD53 chip. Although the bump-bonding process is commonly used in the microelectronics industry, the hybridization of the ITk pixel sensors may be challenging due to the 50 μm pitch. Solder bumps with a 25 μm diameter will be used against the

standard 100 μm ones.

The hybridization results to be more challenging than for the ATLAS IBL since the target thickness of the chip is 150 μm and of the sensor is 100 μm or 250 μm for planar or 3D sensors. The bump density increases by a factor five but the bump distance remain unchanged affecting only the total number of bumps.

Hybrid pixel modules require dedicated processing that are of little interest outside the high energy physics community making them expensive and with a reduced production rate. These are obstacles to the development of large area detectors like the ITk. The option of a commercial technology that does not require hybridization has been investigated. In particular, monolithic pixel devices based on depleted CMOS technologies have been studied in detail.

In the outer layer the use of monolithic CMOS devices is not expected to affect the tracking performances with respect to hybrid devices with the same pixel size. Moreover, the use of monolithic devices would help in terms of material budget, since thinning below 150 μm is possible and a single substrate contains both the sensor and front-end parts.

At the time of writing this thesis monolithic depleted CMOS devices are an option as a drop-in solution for the last pixel layer of ITk. The CMOS modules must have the mechanical size, input/output interface, voltage supply and power consumption compatible with the servicing of hybrid pixel module, to make the installation possible in case the technology qualifies for the ITk requirements.

ITk Performances

The measurements provided by the Inner Tracker are fundamental to obtain the particle trajectory, the polar (θ_0) and azimuthal (ϕ_0) angles of the track and the particle momentum p_T measured from the track curvature. In particular, the Pixel Detector is critical for the determination of the transverse (d_0) and longitudinal (z_0) impact parameters of the tracks. The resolution on the measurements of these parameters influences the detector performance in terms of b-tagging, and lepton or jet reconstruction.

In figure 3.11 the track parameter resolutions for the nominal ITk with $50 \times 50\,\mu\text{m}^2$ pixels int the Pixel Detector is shown together with the one of the ATLAS Pixel Detector in Run-2 after the installation of IBL. A significant improvement can be observed in the z_0 and θ_0 due to the reduced pixel size along the direction parallel to the beam axis (50 μm against 250 μm), while on d_0 and ϕ_0 the resolution is similar if not worse because there is no reduction of the pixel size and the IBL is placed at 3.3 cm from the beam axis while for the first ITk pixel layer this distance will be of 3.9 cm. The p_T resolution is generally improved by about a factor 2 at all p_T values mostly because

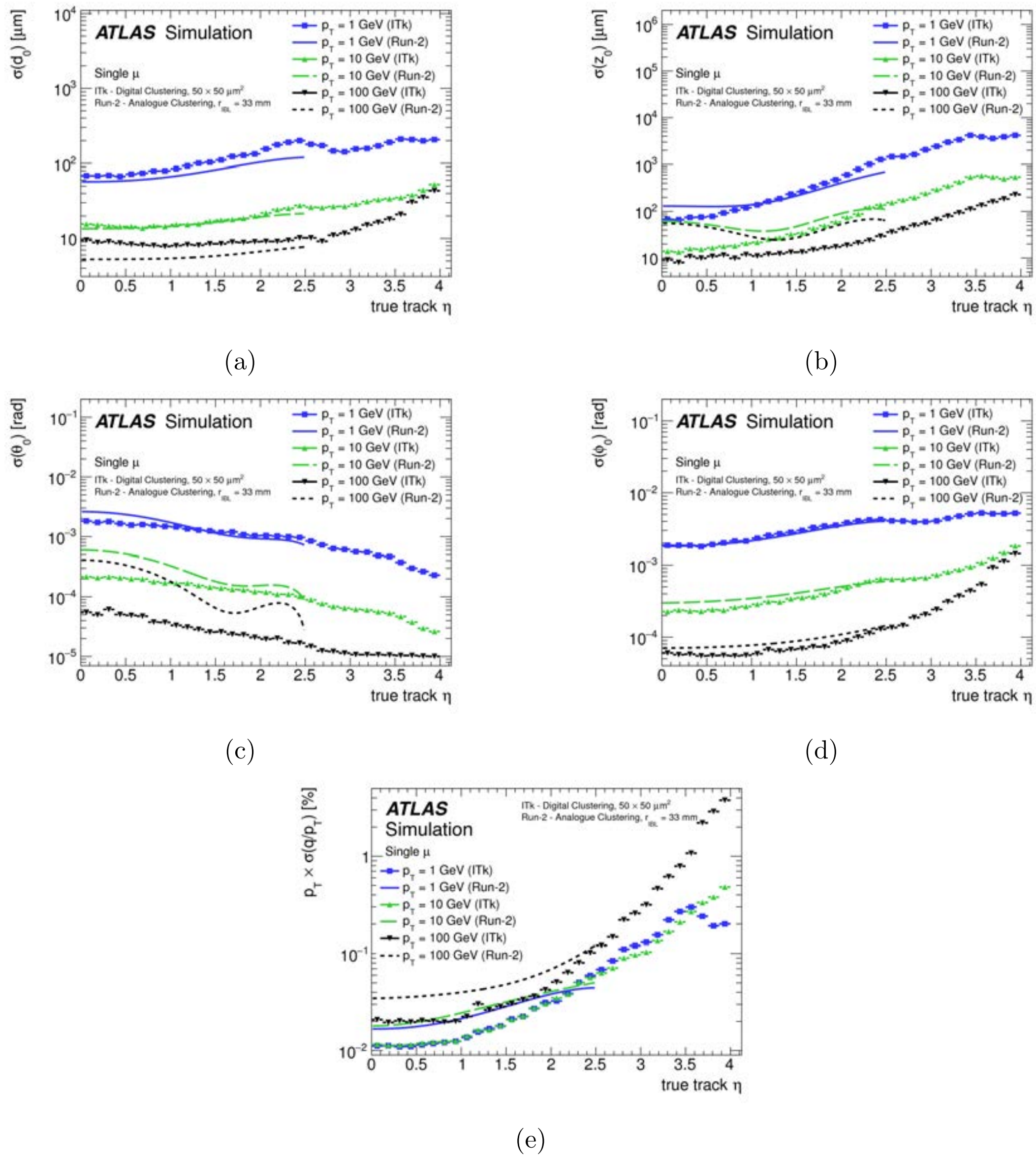


Figure 3.11: Overview of the track parameter resolution as a function of η for the ITk Pixel Detector with $50 \times 50\,\mu\text{m}^2$ pixel size. The plots refer to simulations of muon tracks of p_T 1, 10 and 100 GeV. Comparison with the performance of Run-2 Inner Detector with IBL is also shown [38].

of the higher resolution at large R of the ITk Strip Detector compared to the TRT.

Additionally, the plots of figure 3.11 show the larger η coverage of ITk that extends up to $|\,\eta\,| = 4$. However, the resolution at large η is not good enough to ensure efficient pile-up rejection in a track crowded environment. An additional detector will be installed in the calorimeter end-cap, the High Granularity Timing Detector (HGTD), to provide high resolution timing information to the tracks. With this additional

information a time coordinate will be associated to the tracks hitting the HGTD and time separation can be used to mitigate the effect of pile-up [42].

3.9.2 The High Granularity Timing Detector

The upgrade to HL-LHC will lead to an increase of pile-up, rising the average number of interactions per bunch-crossing ($\langle\mu\rangle$) from 80 to about 200. With so many interactions per bunch crossing, pile-up becomes one of the major challenges for the experiments at HL-LHC. The primary vertices will be spread around the nominal position of the interaction point over about 45 mm RMS along the beam axis, producing an average of 1.8 collisions/mm at $\langle\mu\rangle = 200$. To be able to efficiently resolve tracks belonging to different primary vertices, the resolution of the longitudinal track impact parameter has to be much smaller than the inverse of the average pile-up density, that is about 550 μm. The ITk provides a z_0 resolution well below this value in the central region, but for particles in the forward region with low transverse momentum the resolution on the z_0 measurement can go as high as 5 mm, see figure 3.11b.

The development of radiation hard silicon based timing detectors allows to measure the time of arrival of particle in a radiation harsh environment with resolution of the orders of tens of nanoseconds. Adding timing information to the tracks may allow to resolve nearby vertices whose distance is lower than the tracker resolution if the time separation is sufficiently large. Timing information is complementary to the track and p_T measured by the tracker and calorimeter, adding redundancy in the region where the track impact parameter resolution is high and compensating for the degraded resolution where it is not sufficient to separate vertices.

The HGTD aims to measure the time of arrival of particles crossing the forward region, with pseudorapidity in the interval $2.4 \leq |\eta| \leq 4$, with a time resolution better of approximately 30 ps during the whole HL-LHC period. In the nominal configuration the time spread of the collisions is 175 ps RMS, so that the HGTD would reduce the pile-up by a factor 6 adding the timing coordinate to the tracks.

In addition, the HGTD will enhance the physics performance capability of the ATLAS detector in the forward region, allowing the efficient reconstruction and tagging of forward jets and leptons with performance comparable to the one in the central region. Moreover, the HGTD can be used to monitor the luminosity delivered to ATLAS both online and offline and also to provide minimum-bias trigger.

Physics motvation

The main goal of the HGTD is to mitigate the effect of pile-up in the assignment of tracks to primary vertices that has a relevant impact on the physics measurements through jet reconstruction, b-tagging and lepton isolation. A track is associated to

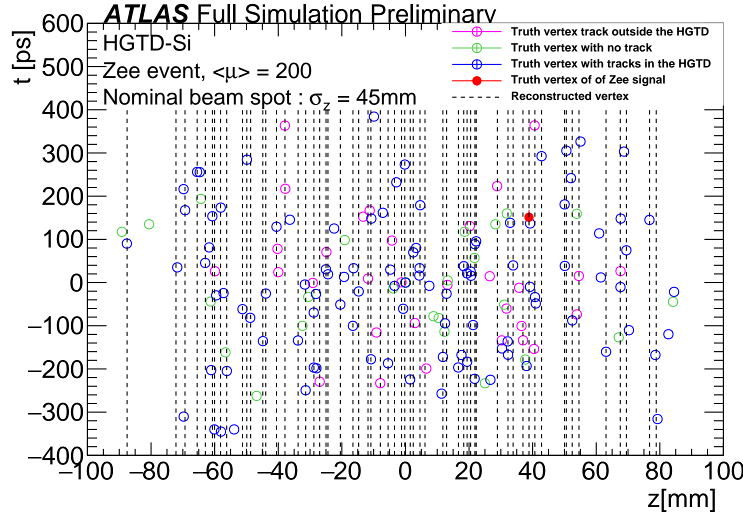


Figure 3.12: Event display showing the time and z position of all vertices in a $Z \rightarrow e^+e^-$ event from the full simulation with $\langle\mu\rangle = 200$. Only tracks reconstructed with a transverse momentum greater than 1 GeV are used. The red circle is the truth hard-scatter vertex, the pink circles are the truth vertices with no reconstructed track in the HGTD acceptance, green circles are truth vertices without reconstructed tracks and the blue circles are the truth vertices with at least one track in the HGTD. The dotted lines are the positions of the reconstructed vertices. The error bar on the y-axis is the expected precision of the vertex timing determination in the HGTD, in most cases smaller than the symbol size.

a vertex if its impact parameter z_0 is compatible with the vertex position z_{vertex}. The compatibility is evaluated by the equation $\mid z_0 - z_{vertex} \mid < 2\sigma_{z_0}$ where σ_{z_0} is the longitudinal impact parameter resolution of ITk and $2\sigma_{z_0}$ is chosen to include 95% of the tracks in this selection.

As shown in figure 3.11b, the z_0 resolution can be of the order of millimetres at low p_T and high $\mid \eta \mid$. In the HL-LHC the average number of interaction per bunch crossing is 200. The pile-up density has a most probable value of 1.44 vertices/mm with a tail fading out at about 3.5 vertices/mm, see figure 3.13. This means that tracks with large η and low p_T, such as those produced by light quark and gluon jets or prompt electrons, are not reconstructed with sufficient resolution to permit unambiguous track to vertex assignment with the use of the tracker only. Being able to measure the time of the tracks would make possible to preserve the track to vertex capability on the forward region by use of two dimensional selection criteria, using both the impact parameter z_0 and time of the tracks, introducing the timing selection $|t_0 - t| < 2\sigma_t$ where t_0 is the vertex time, t the track time and σ_t the track time resolution, assumed to be ~ 30 ps for all the tracks in the HGTD field of view.

The HGTD can also help to mitigate the contamination of jets of interest coming

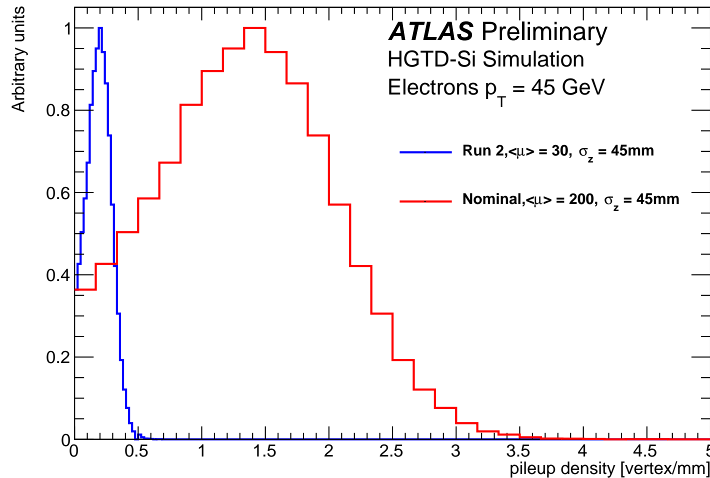


Figure 3.13: Local pile-up vertex density for different values of $\langle\mu\rangle$.

from hard-scattered vertices with pile-up interactions. The contamination can come from other hard QCD pile-up vertices or from random combination of background particles. This contamination can reduce the precision of Standard Model measurements and by consequence the sensitivity to the discovery of new physics. The HGTD extends to larger η values the hard-scatter jet reconstruction efficiency allowing to maintain similar pile-up jet suppression performance as in the central barrel over a large part of its acceptance [43].

The efficient identification of secondary vertices from b-jets and rejection of light quark ones is fundamental to pursue the physics program at the HL-LHC. The b-tagging algorithms [44] look for tracks in the neighbourhood of a primary vertex. With a larger window along the beam axis it is more probable to select tracks from nearby pile-up interactions, increasing the number of misidentified b-jets. Including timing information from the HGTD in simulated $t\bar{t}$ events at $\langle\mu\rangle = 200$ has shown to improve the light jet rejection of the multivariate algorithm by approximately 20% for b-tagging efficiency of 85% and 50% for b-tagging efficiency of 70% in the region $|\eta| > 2.4$.

Also the lepton isolation efficiency [45] is improved with the HGTD. By assigning time to the leptons in the forward region it is possible to reject tracks that originate from different interactions but are close in space. The isolation efficiency would drop significantly when using only the ITk with the increase of the pile-up during the HL-LHC period. The addition of timing information reduces the drop keeping the efficiency above 80% at high pile-up density even at the end of the HL-LHC when the timing resolution of HGTD will be degraded by radiation damage.

The benefits of a fast high-granularity detector are not limited to a cleaner and more efficient determination of the events of interest to carry out the physics program of ATLAS at the HL-LHC. Some of the measurements, such as the Higgs boson production cross section and coupling constants, are limited by the uncertainty on the luminosity determination [46]. The high granularity and the short signal duration result in a linear relation between the average number of hits in the HGTD detector and the number of p-p interactions. The fast readout allows to measure the instantaneous luminosity and monitor bunch-by-bunch variations.

The HGTD will occupy the area of the Minimum-Bias Trigger Scintillators (MBTS) that have been used during Run-1 and Run-2 to record minimum-bias events at low-μ data taking conditions. The MBTS would not be able to cope with the harsher condition of the HL-LHC and, as mentioned above, will be removed to free space for the HGTD. Since the HGTD is read out on every bunch crossing, it can be used for on-line luminosity measurement, and can be used by the Level-0 trigger in low luminosity runs to trigger minimum-bias events, as well as to implement more precise trigger algorithms based on forward jets. Improving the MBTS performances thanks to the improvements over orders of magnitude both in granularity and in timing resolution.

The improved performance of event reconstruction introduced by the HGTD has the effect of enhancing the physics analysis potential of ATLAS. The suppression of pile-up jets is beneficial for b-tagging expecially at large $\mid \eta \mid$, increasing by 50% the light-jet rejection for a b-tagging efficiency of 70%. The better b-tagging reflects in a beneficial effect for measurements involving vector boson fusion (VBF) processes, like searches for heavy Higgs bosons produced with VBF that gives jets at large rapidity with a small cross section. The improved lepton efficiency can enhance the precision of SM fundamental measurements such as the weak mixing angle.

The High Granularity Timing Detector Layout and Requirements

The detector is based on thin Low Gain Avalanche Detectors (LGAD) sensors providing a single hit timing resolution of $30 \div 50\,\mathrm{ps}$. The sensors are arranged in arrays of pixels with a pitch of approximately $1\,\mathrm{mm}$ to get a sufficient granularity, to ensure an occupancy lower than 10%, and a low capacitance, to reduce the electronic noise that has negative effects on time resolution. The sensors will be bump-bonded to an application-specific integrated circuit (ASIC). The hybrids are then glued and wire-bonded to a flexible circuit board to build the HGTD module.

The modules are mounted on support plates of different shapes and sizes for the different radii, forming a disk extending from $r = 120\,\mathrm{mm}$ to $640\,\mathrm{mm}$, see figure 3.14. Each disk is instrumented on both sides, and two layers of disks per each side of the detector will be installed at $z = \pm 3.5\,\mathrm{m}$, outside the tracker volume and in front of

the end-cap and forward calorimeters.

The arrangement of the modules is such to have an overlap between the sensors on either side of the support plate of 80% in the inner region ($r < 320$ mm), and 20% in the outer one resulting in an average hit multiplicity of three and two respectively. The larger number of hits in the inner region is needed to keep the per-track time resolution within the requirements after irradiation, see section 2.2.4.

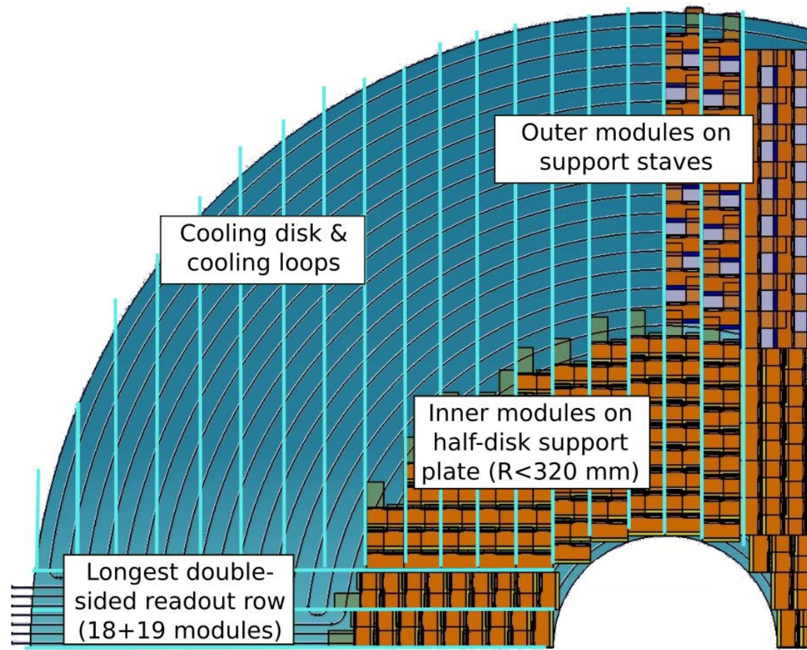
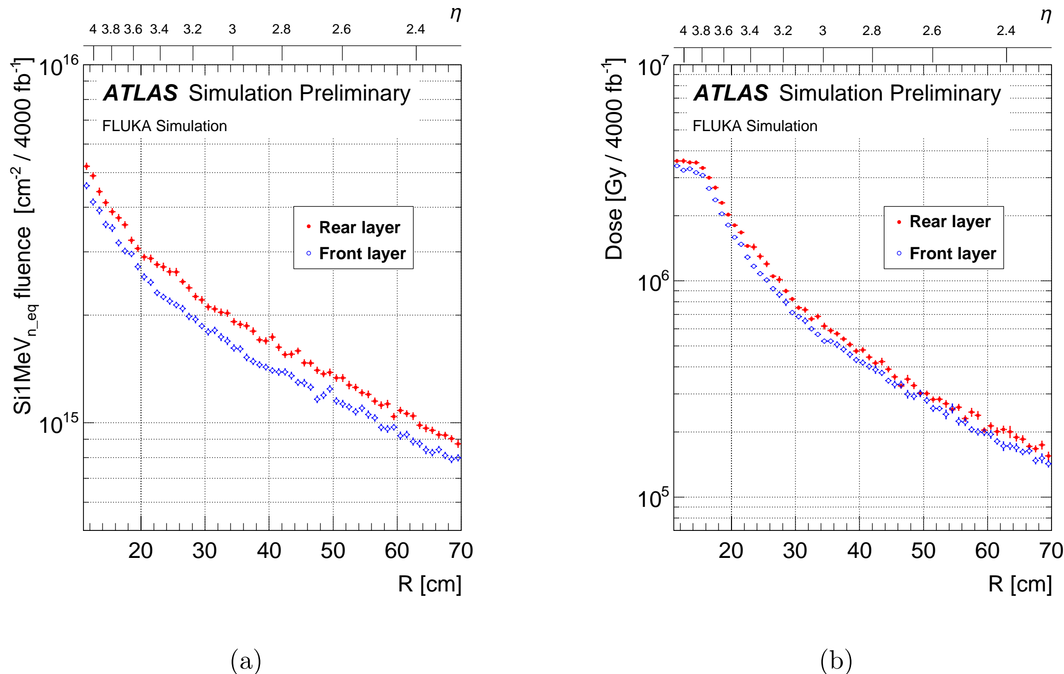


Figure 3.14: Drawing of one quadrant of the HGTD showing the module assemblies and the cooling pipes. Moldules with $r < 320$ mm are mounted on a half-disk support plate, modules at larger radii are mounted on staves [42].

Some of the specifications of the ATLAS HGTD sub-detector are constrained by the space availability. The inner radius cannot be lower than 110 mm because of the presence of the calorimeter cryostat, while the outer radius can go to a maximum of 1100 mm including the space for the detector electronics and servicing. The current layout foresees an active region between 120 mm $\leq r \leq$ 640 mm, equivalent to a pseudorapidity acceptance of $2.4 \leq |\eta| \leq 4$.

The sensors closest to the beam will be exposed to a fluence of $7.4 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$, including a safety 1.5 factor, during the HL-LHC lifetime, see figure 3.15. To keep the performance of both sensors and electronics within the HGTD requirements the inner part should be replaced after an integrated luminosity of 2000 $\mathrm{fb^{-1}}$ reducing the exposition of the innermost sensors to $3.7 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$ while the one of the closest to not be replaced is $3.2 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$.



(a) (b)

Figure 3.15: Equivalent $1\,\mathrm{MeV/cm^2}$ neutron fluence (a) and total ionizing dose (b) distribution in the HGTD after $4000\,\mathrm{fb}^{-1}$ and before the application of the safety factors. The front layer is the closest to the center of the detector, the rear layer is the furthest. [42].

The HGTD Sensor

The baseline technology for the HGTD detectors consists of $50\,\mu$m thin LGAD arrays with pixel size of $1.3 \times 1.3\,\mathrm{mm}^2$. Thin detectors with intrinsic gain prove to have a time resolution that suite the HGTD requirements. A detailed discussion on the LGAD technology will be given in chapter 4 where studies on the time resolution and the radiation hardness of LGAD sensors will be presented.

The ALTIROC chip

The HGTD sensors need a fast and radiation hard front-end electronics able to preserve their time resolution over the whole HGTD lifetime. Therefore, the requirements on time resolution and radiation hardness are extended also to ASIC.

The modules located closer to the beam line will be replaced together with the sensors during the HL-LHC period, limiting the exposition to a total ionizing dose of 4.1 MGy including a safety factor of 2.25, see figure 3.15.

The HGTD community is working on the development of the ALTIROC chip (ATLAS LGAD Timing ROC) [47], designed by Omega [48].

The time resolution of a silicon detector, already showed in equation 2.18 high-

lights how three out of four contributions come from the electronics:

$$\sigma_{elec}^2 = \sigma_{TW}^2 + \sigma_{jitter}^2 + \sigma_{TDC}^2. \tag{3.1}$$

The intrinsic resolution of the HGTD sensor is given by the Landau fluctuation that is foreseen to be $\sim 25\,\mathrm{ns}$ for a $50\,\mu\mathrm{m}$ thick sensor with gain [49]. To meet the target time resolution σ_{elec} has to be smaller than this value.

The time walk contribution is expected to be negligible if a correction from time over threshold measurement is applied. The jitter contribution depends on the noise and on the pulse rising time. The chip is designed to achieve a contribution due to jitter lower than 10 ps RMS for signals equivalent to an LGAD gain of ~ 10. The TDC term only depends on the TDC bin size, with a 20 ps large bin its contribution will be less than 6 ps using $20/\sqrt{12}$.

The Time Of Arrival (TOA) will be measured with a fixed threshold discriminator. This measurements suffers from time walk since larger signals would cross a fixed threshold before than lower signals. The time walk can be mitigated applying corrections based on the signal amplitude. The approach chosen for the ALTIROC chip is to use the Time Over Threshold (TOT) as an indirect measurement of the signal amplitude. This solution showed a time walk dispersion after TOT correction of less than 10 ps [47]. A Constant Fraction Discriminator (CFD) would make the TOA determination insensitive to time walk but it has been discarded because of the difficulties due to the implementation of a radiation hard CFD in the ASIC.

The ASIC will have therefore two different TDCs, one for the measurement of the TOA with bin size 20 ps and one for the measurement of the TOT with bin size 40 ps. The size of the TOA and TOT TDCs is of 7 and 9 bits respectively for a range of 2.5 ns and 20 ns.

The time measurement data, consisting of a total of 17 bits (7 bits for the TOA, 9 bits for the TOT and an hit flag bit), is stored in a buffer memory that is read out after a L0/L1 trigger signal. This requires a latency of up to $35\,\mu$s. The hits are then passed to a secondary buffer before being transmitted to the off-pixel common electronics.

While the design of the final HGTD ASIC foresees a total of 225 channels arranged in a matrix of 15×15 pixels with size $1.3 \times 1.3\,\mathrm{mm}^2$, the first prototype, named ALTIROC0_V0 consisting of a 2×2 pixels matrix compatible with 2×2 LGAD arrays produced by CNM has already been used for preliminary tests. The feedbacks from the tests on the ATLIROC0_V0 chip assembly have been used to improve the design of the ALTIROC0_V1 prototype, recently delivered at the time of writing, and of the ALTIROC1 chip, that includes the complete number of pixel channels with time to digital converters and local FIFO memories, submitted to production in summer

2018.

Chapter 4

Low Gain Avalanche Detector

Solid state detectors with intrinsic gain have been developed since the early stages of the semiconductor industry. The most common detectors with built-in charge multiplication (CM) are the Avalanche Photo-Diodes (APDs) first proposed in the 1950s. An APD is a semiconductor device that makes use of the photoelectric effect to generate an electric pulse after photon illumination. It consists of a reverse biased *pn-junction* with intense electric field. The photo-generated electrons can gain high enough energy to initiate an avalanche mechanism via impact ionization. These devices can be operated in linear or Geiger mode. In the linear mode the size of the pulse is proportional to the amount of incident light with typical gain around 100, while in the Geiger mode the gain is typically larger than 1000 and the electric pulse immediately reaches saturation. The main application of APDs are imaging and single photon counting with the APDs operated respectively in linear and Geiger mode.

APDs are optimized to detect photons with wavelengths going from the infra-red to the ultra-violet in a low light environment. Each photon generates an electron through photoelectric effect, with a probability given by the quantum efficiency of the device. The primary electrons are multiplied through an avalanche process resulting in a sizeable signal. A minimum ionizing particles instead, generates charge along its trajectory in the full detector thickness therefore the amount of the primary charge is much larger than in the photon detection case, with about 75 electron-hole pairs per micrometer, see section 2.2.

The Low Gain Avalanche Detector (LGAD) technology adapts the APD design to the detection of *mips*. The main difference is that the LGAD technology targets a gain of $10 \div 20$, lower than the APDs. The charge multiplication is achieved by introducing an additional doping layer of acceptors close to the *pn-junction*. In the n-on-p silicon detector, the LGAD design initiates the multiplication by electrons drifting towards the n^+ electrode and crossing a region of high electric field, while

the holes are not multiplied. This allows to preserve linearity with the initial energy deposition offering a more stable operation and a minimizing the noise from the multiplication process. The multiplication of holes would give a positive feedback initiating a self-sustaining avalanche causing the breakdown of the sensor, leading to non linearities and saturating the front-end electronics.

The LGAD technology has been initially developed by the Centro Nacional de Microelectrònica (CNM) of Barcelona as a potential technology for highly radiation hard tracking detectors. Radiation-induced charge multiplication had been observed in *n-type* epitaxial silicon diodes after proton irradiation to the fluence of $10^{16}\,\mathrm{n_{eq}/cm^2}$ [50]. The idea of LGAD devices for tracking is to have charge multiplication already in non irradiated devices and profit from the signal enhancement due to CM during the lifetime of the detector in a harsh radiation environment, counterbalancing the signal degradation induced by radiation damage. For timing application instead, the use of detectors with intrinsic gain has the effect of enhancing the slew rate (S/t_{rise}) that results in beneficial effects for the time resolution. Since the detector thickness also affect the timing performance, thin LGAD devices for timing have been developed, see section 2.2.3.

The different contributions to the current waveform in an LGAD device are highlighted in figure 4.1, where the current waveform induced on a $300\,\mu$m thick LGAD device from a 660 nm laser pulse illuminating the backside of the sensor is shown.

4.1 LGAD for tracking

As explained in section 2.2.4, silicon based detectors suffer charge trapping when exposed to a high level of radiation fluence. The trapping can lead to a loss of efficiency if the total collected charge is lower than the comparator threshold in the front-end electronics. LGAD devices have been developed as a potential radiation hard solution where the built-in charge multiplication mechanism compensates for the loss induced by radiation damage.

The technology has been firstly developed on single pad devices to optimize the doping profile and the implantation parameters to achieve the desired gain and voltage stability. In CNM LGAD sensors the multiplication effect is obtained by diffusing a *p-type* boron multiplication layer in close contact with the n^+ electrode of an *n-on-p* device whose structure becomes $n^+/p^+/p^-/p^+$, the cross section of such devices is shown in figure 4.2.

The CM layer implantation covers an area slightly smaller than the one covered by the n^+ electrode. A Junction Termination Extension (JTE), consisting of deep *n-type* diffusion of lower doping concentration over the junction edge, is added to

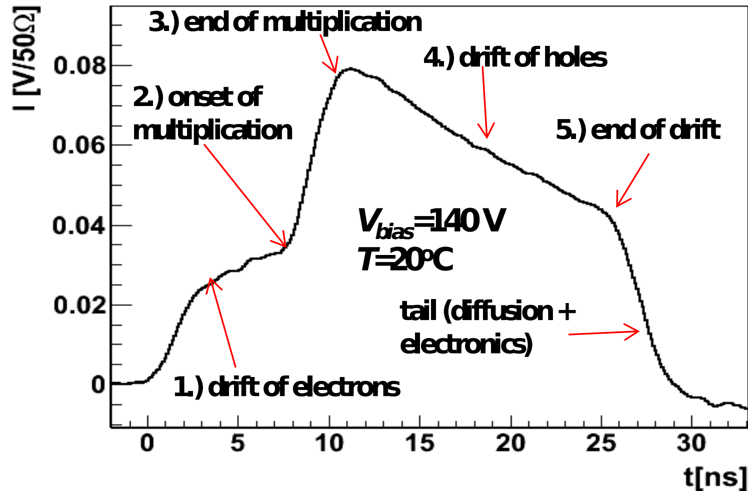


Figure 4.1: Current waveform in a 300 μm thick LGAD device after illumination from the backside with a red laser pulse in a TCT set-up [51]. The red laser is completely absorbed in the first few micrometers generating e-h pairs only close to the backside surface. The holes are immediately collected so that only the electrons contribute to the initial signal (1). Electrons are multiplied after reaching the multiplication layer on the opposite electrode (2). The multiplication is stopped when all the electrons have arrived to the cathode (3). From the multiplied charge only holes contribute to the current (4). The signal goes to the baseline after all the holes have reached the backside of the sensor (5).

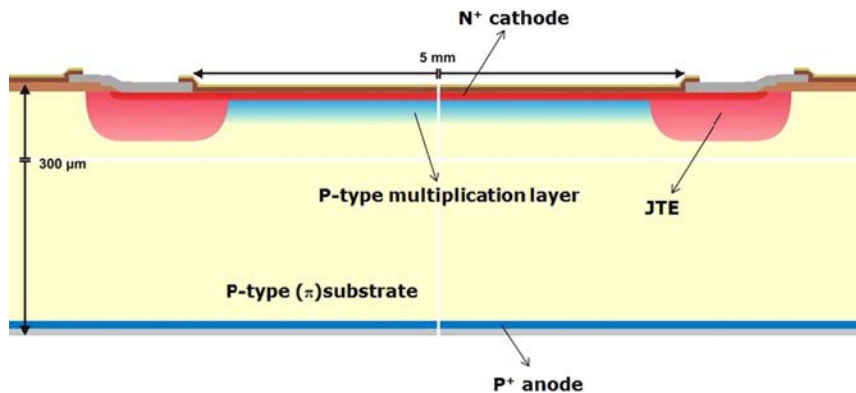


Figure 4.2: Schematic cross section of an LGAD pad diode [52].

avoid peaks of the electric field at the edge of the periphery of the sensor to improve the voltage capability avoiding early breakdown.

A simulation of the electric field distribution in such devices is shown in figure 4.3. It shows how the electric field grows by about two orders of magnitude around the multiplication region and it is kept at lower values in the bulk region below the JTE.

The CNM LGAD run 6827 [53] includes for the first time several structures with

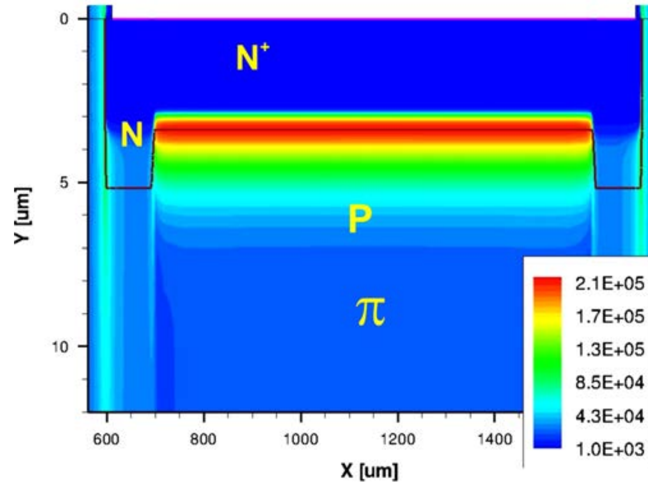


Figure 4.3: Electric field simulation of an LGAD diode from CNM run 6474 with JTE [52].

fine segmentation: strip detectors with a pitch of 80 μm and different widths of the n^+ electrode and p^+ multiplication layer, pixel detectors adapted for different front-end chips with pixel size of $50 \times 250\,\mu m^2$, $50 \times 400\,\mu m^2$ and $100 \times 150\,\mu m^2$, as well as diodes for direct comparison with CNM run 6474, a previous LGAD production containing exclusively single pad diodes where a gain of 8 was reached before irradiation [52]. A total of 14 wafers have been produced in four different substrates (epitaxial wafers with thickness of 9.8 μm, 50.4 μm and 75 μm, and 285 μm thick float zone wafers) with three different implantation depth of the n^+ electrode (shallow, standard and deep). The implantation depth of the n^+ electrode is decisive for the CM mechanism outcome as it can compensate the p^+ multiplication layer effect. A shallower n^+ implantation leads to a higher gain but also a higher noise and lower breakdown voltage, while a deeper implantation results in a higher breakdown voltage but a lower CM. For each wafer type a reference wafer without charge multiplication layer (run 6894) has been produced for a direct comparison of the results.

In CNM production 6827, due to the fine segmentation, the edge termination for the multiplication junction cannot be done implanting a JTE and it is simply given by a wider implantation of the n^+ electrode with respect to the CM layer. The effect of different edge terminations on the electric field at the sensor periphery is shown in figure 4.4, demonstrating that edge terminations with JTE suppress the undesired electric field peak at the sensor edge.

All the studied strip and pixel sensors are from 285 μm thick float zone wafers from run 6827 (LGAD) and run 6894 (reference), listed in table 4.1. LGAD strip sensors from wafer 12 and 14 with shallow and deep diffusion of the n^+ electrode have been studied. The strip pitch is 80 μm, the same for all the strip devices, while

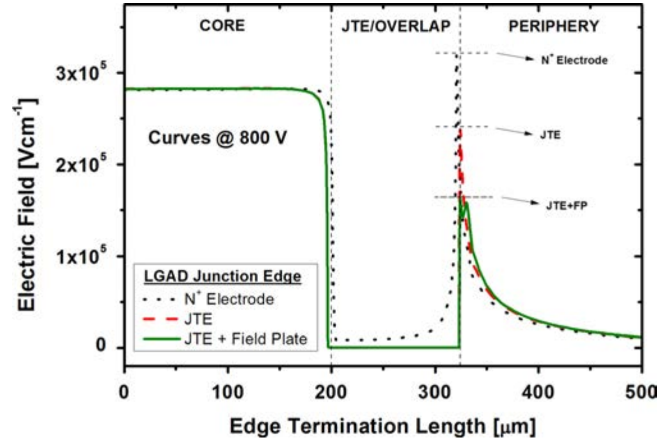


Figure 4.4: Simulated electric field distribution at the edge of an LGAD diode for different termination designs: n+ electrode extension, JTE, and JTE with field plate [52].

the width of the n^+ implant is 24, 32 and 62 μm and the corresponding width of the CM p^+ implant is 6, 14 and 44 μm. All the strip sensors are AC coupled to the readout with a polysilicon bias resistor of 1.5 MΩ per strip and a capacitor made with two overlapping metal pads of $56 \times 100\,\mu m^2$. A *p-stop* implant is placed between the strips for inter-strip insulation. The strips are covered by an aluminium metallization at the front side with the same width as the n^+ electrode. To provide large enough wire-bonding contact pads the aluminium strips are widened to the width of 55 μm for all the geometries. Close to these contacts a 20 μm wide opening on the metal allows light injection in the sensor below the CM layer. Moreover, backside metal is partially removed for back-illumination of the sensor.

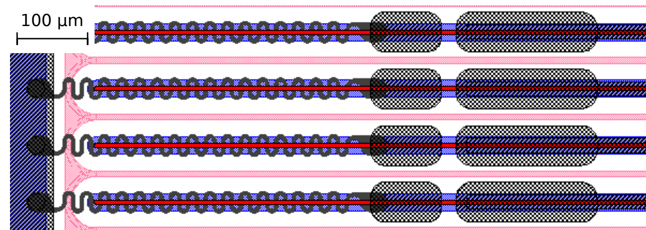


Figure 4.5: Layout of the termination of a strip detector having the width of the CM implant equal to 6 μm and the one of the n^+ implant to 24 μm. The red lines at the center of each strip are the CM implant, the blue fine grids are the n^+ implants, the gray wiggled lines are the polysilicon resistors and the black grid is the top metallization, another underneath metal layer provide the AC coupling. The light red lines at the edges of the strips are the p-stop implants [53].

The tested pixel devices have deep implantation of the n^+ electrode and their layout is compatible with the FE-I3 [29] and FE-I4 [30] readout chips. The FE-I3

	Device name	Type	n^+ width	CM p^+ width	Diffusion of n^+	Max. Volt.
Strip sensors	6894-W14-AC7	Ref.	62 μm	-	Deep	300 V
	6827-W14-AC7	LGAD	62 μm	44 μm	Deep	300 V
	6827-W14-AC1	LGAD	24 μm	6 μm	Deep	150 V
	6827-W14-AC2	LGAD	24 μm	6 μm	Deep	600 V
	6827-W12-AC11	LGAD	32 μm	14 μm	Shallow	200 V
Pixel sensors	6894-W14-FE-I3-1	Ref.	30 μm	-	Deep	220 V
	6827-W14-FE-I3-1	LGAD	30 μm	12 μm	Deep	300 V
	6894-W14-FE-I4-1	Ref.	30 μm	-	Deep	>150 V
	6827-W14-FE-I4-1	LGAD	30 μm	12 μm	Deep	50 V

Table 4.1: Details of the strip and pixel sensors studied. The strip pitch is 80 μm in all cases and the pixel pitch (short side) is 50 μm for both FE-I3 and FE-I4. The width values for the pixels correspond to the short side. The last column refers to the maximum applied voltage during the measurements.

sensor consist of a matrix of 160 rows $\times$ 18 columns pixels whose size is 50 $\times$ 400 μm^2, while the FE-I4 sensor has 336 rows $\times$ 80 columns pixels of 50 $\times$ 250 μm^2. The width of the n^+ electrode and of the CM layers are the same for both pixel geometries, being respectively 30 and 12 μm.

4.1.1 TCT measurements of strip devices

The strip devices have been measured with a multi-channel Transient Current Technique (TCT) set-up at the Hamburg University. The TCT basically consists in the recording and analysis of time resolved current waveforms induced by laser pulses. A description of the TCT technique and its applications are given in appendix A.

The TCT set-up used to perform these measurements is made of a Picoquant pulsed laser that generates light pulses with duration shorter than 100 ps and with a repetition rate of 1 kHz. Infra-red and red lasers of wavelength equal to 1060 and 660 nm respectively have been used.

Red and infra-red light have different absorption lengths in silicon. Red light has an absorption length of 3 μm generating electron-hole pairs just below the illuminated surface. Infra-red light instead has an absorption length of about 1 mm, that is much larger than the sensor thickness. For this reason it can be considered to generate electron-hole pairs uniformly along its path, similarly to a *mip*. The laser light is focused to the sensor surface with a spot size of the order of $\sigma \sim 10\,\mu$m. The strip sensors are mounted on a ceramic substrate which in turn is mounted on an x-y movable table with 0.1 μm precision on both directions, allowing to probe the sensor along the strip direction and across it. The ceramic plate substrate can be mounted in such a way that the illuminated surface is the one with segmented electrodes or flipped to illuminate the sensor from the back side.

About 15 strips and the bias ring are wire-bonded to a readout line connected to ground. The signals of two strips in the central part of the sensor are read out after being amplified by Femto current-sensitive amplifiers [54] with 2 GHz bandwidth and a gain of 40 dB corresponding to an amplification factor of 100. The readout is performed via a Tektronix DPO7254 oscilloscope [55] with 2.5 GHz bandwidth and 40 GS/s sampling rate. The back side of the sensor is read out as well after decoupling the high voltage with a Pulse Lab 5531 bias-T. The bias is provided by a Keithley 6517 high voltage power supply [56]. A sketch of the set-up is shown in figure 4.6.

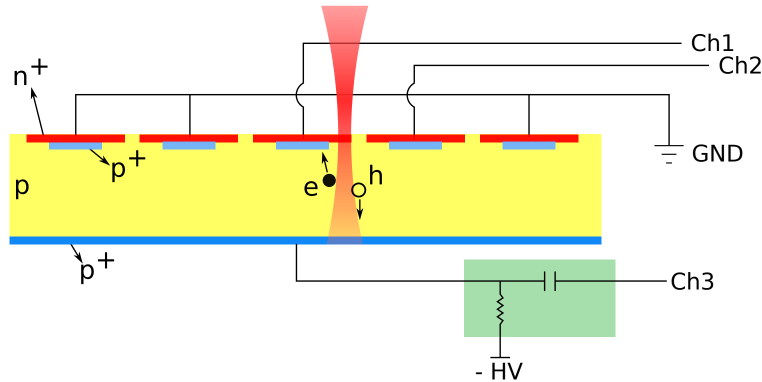


Figure 4.6: Sketch of the multi-channel TCT setup at the Hamburg University in the front-side illumination configuration.

The strip sensors have been first tested with back-side illumination using 660 nm laser light, to allow this, the backside metallization has been partially removed. This configuration is useful to study the CM process. As the red laser only penetrates few micrometers, the ionization is localized just below the p^+ electrode, so that holes are immediately collected and the signal is given by the electrons that drift towards the n^+ electrode. If there is charge multiplication, the electrons will initiate an avalanche after reaching the multiplication region generating secondary charges that induce an additional contribution to the waveform. This extra component is present only in case of CM due to the drift of holes towards the opposite electrode. Compared to the signal of a sensor without charge multiplication, the signal of a sensor with gain is expected to be larger and lasting longer because the additional contribution is given by holes that have a lower drift velocity. In figure 4.7 the TCT waveforms of an LGAD and a reference strip sensor without CM layer for this configuration are shown. The readout is performed on the back-side electrode that is biased at 300 V. The waveform of the LGAD sensor almost perfectly overlaps with the one of the reference sensor.

The measurement has been repeated for all the strip sensors listed in table 4.1 at different bias voltages approaching the breakdown and pointing the laser at different positions with respect to the strip center. All the measurements lead to the conclusion

that the devices do not present charge multiplication.

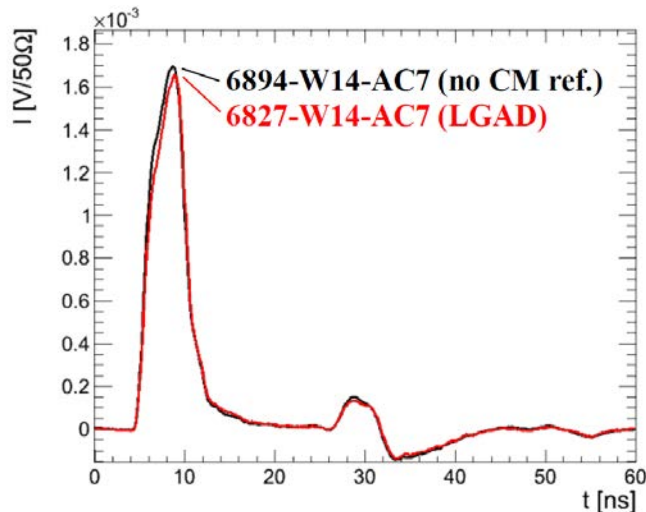


Figure 4.7: TCT current waveform on the back-side electrode of an LGAD and a reference strip detector biased at 300 V for back illumination with 660 nm laser light.

The strip devices have been also measured in the front-side illumination configuration with 1060 nm laser light. Each strip has an opening on the aluminium metallization that runs along the strip center and the light is injected through this window into the sensor. In this configuration the IR laser light produces electron-hole pairs along the whole sensor thickness imitating the behaviour of a *mip*.

The current waveform of two strips and the back-side electrode is integrated to get the total collected charge. Figure 4.8 shows the charge collected on the back-side electrode in a scan across the strips with step size of 2 μm at 300 V by two LGAD sensors and a reference one. The opening on the metallization is about twice as big as the laser spot σ, when the laser point to the center of the strip the tails of the laser hit the metal and are reflected. As a fraction of the light is reflected and does not penetrate into the sensor, a lower charge is collected when the laser is focused on the strip center. This effect is less pronounced for sensor 6894-W14-AC2 where a better focusing was achieved. The effect on the strips boundaries might be caused by small differences in the surface topology, which is characterized by shallow trenches due to the p-stop implantation. This might cause differences in the absorption and transmission properties of the light which might be also sensitive to the laser focus variation.

The charge measured on the LGAD sensors is compatible with the one measured on the reference sensor showing that the CM mechanism did not occur on the LGAD strip sensors from this CNM run. LGAD devices are expected to collect a charge

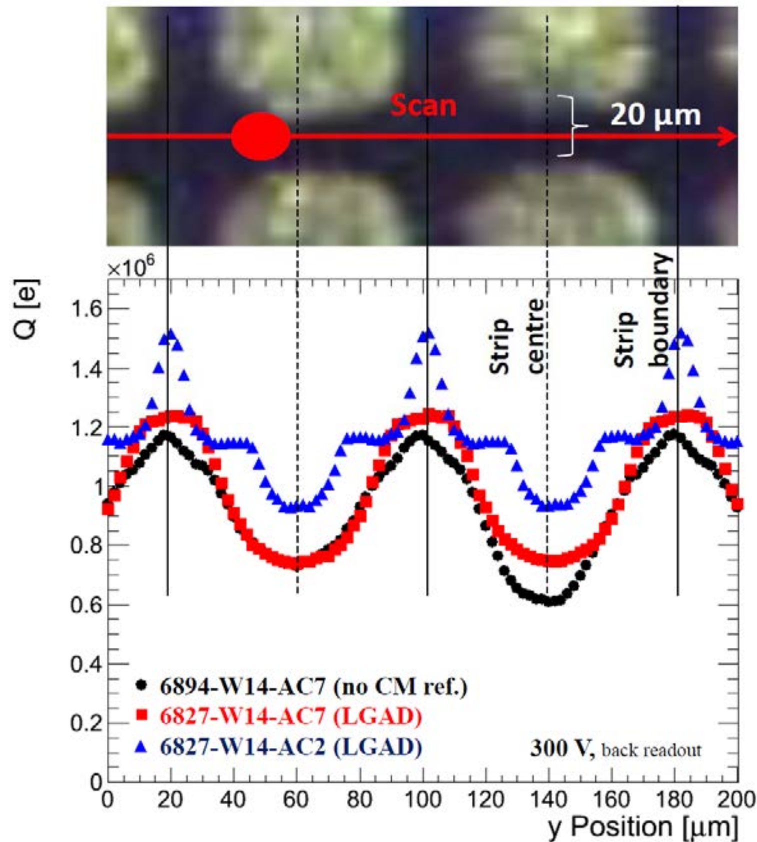


Figure 4.8: Integrated charge as a function of y position for a scan with focused 1060 nm laser light through an opening in the metallization of the strips using back-side readout. The two LGAD samples have been measured at different times and it was not possible to reproduce the laser configuration.

about a factor 10 (the target gain) larger than the one collected by the reference device. The plot of figure 4.8 instead shows an agreement between the LGAD and reference sensors, and, as explained above, discrepancies are probably due to the shadowing of the laser light by the metal layer. In addition the charge is observed to be constant with bias voltage after full depletion, see figure 4.9, while in case of CM the gain is expected to increase with voltage since it would lead to a larger electric field in the multiplication region.

Similar results have been observed on the other samples of table 4.1 measured with the same set-up, in particular no differences have been observed between samples from different wafers with different diffusion of the n^+ layer or between samples with different implant geometries. These measurements point to the failure to obtain strip devices with gain in the CNM run 6827. Further studies on pixel devices from the

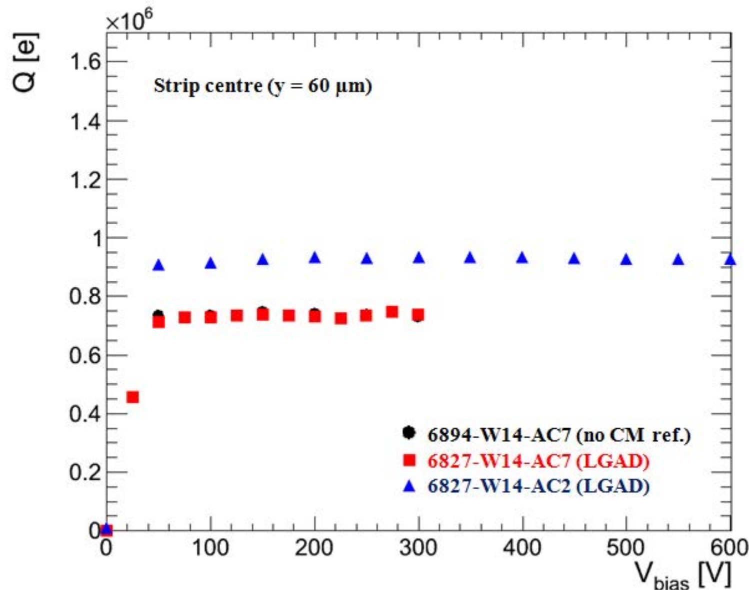


Figure 4.9: Integrated charge as a function of bias voltage for 1060 nm laser light front illumination in the center of a strip using back-side readout. The two LGAD samples have been measured at different times and it was not possible to reproduce the laser configuration.

same production are shown in the following section.

4.1.2 Charge collection study of pixel devices

The CNM LGAD production run 6827 also contains pixel sensors compatible with the ATLAS readout chips FE-I3 and FE-I4. The charge collection of LGAD pixel devices when exposed to a ^{90}Sr β-source has been measured and compared to the one of reference devices without CM layer.

The full module assembly has been performed at IFAE. The sensors have been bump-bonded to FE-I3 and FE-I4 chips, glued on PCBs and wire-bonded. The chip readout is performed through the USBPix setup [57], an FPGA based readout system able to configure and readout both the FE-I3 and FE-I4 chips. The USBPix is connected to a DAQ PC where the STControl data acquisition software is used.

The readout chips do not allow a direct measurement of the charge or of the current waveform. Each readout pixel collects the signal coming from the sensor that is first amplified and then compared to an adjustable threshold. In case the signal is larger than the threshold two values are returned, the time of arrival or time stamp and the Time Over Threshold (TOT), both times are measured in units of 25 ns, that is the LHC bunch crossing clock. The TOT dynamic range is different for the FE-I3 and FE-I4 chips, being of 8 and 4 bits respectively.

The front-end chips can be tuned, calibrating the gain of global and local (one per pixel) amplifiers and of the discriminator threshold, to set the threshold value to a given value of charge. Additionally, the discharge time of the feedback capacitor can be adjusted to target a chosen TOT value.

It is also possible to perform a calibration of each readout channel in order to obtain a pixel-by-pixel TOT to charge conversion. Due to the different local tuning parameters the same TOT value may correspond to different charges for different pixels. With this calibration it is possible to correct the local effect and to use the TOT as an estimator for the collected charge. This calibration is based on a charge injection circuit built in the chip. The value of the injection capacitance can differ from the nominal value by 10% [58] which propagates to the final charge uncertainty.

Before exposing the sensor to a radioactive source to perform the charge collection measurements, a current-voltage (IV) characterization of each sample has been done, see figure 4.10.

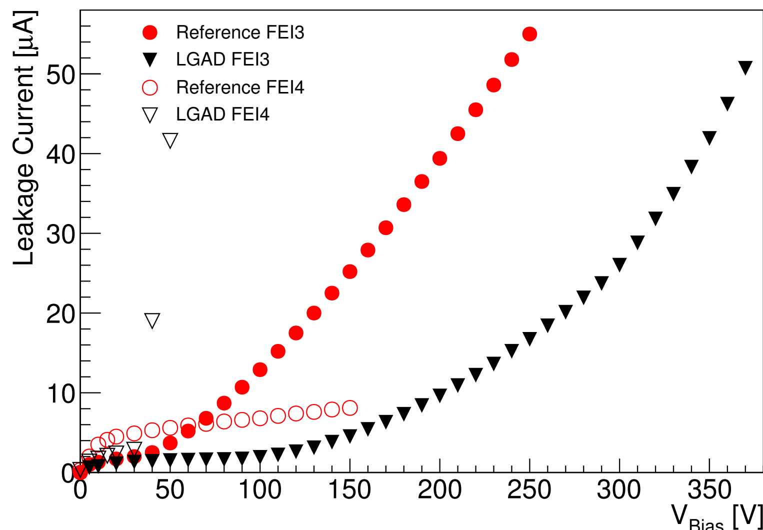


Figure 4.10: Current-Voltage relation of the studied pixel devices after assembly.

The FE-I4 LGAD sensor shows a breakdown voltage lower than 50 V, while the FE-I3 LGAD and both reference sensors can be operated up to few hundreds of volts. Because of the low voltage capabilities of the FE-I4 LGAD sensor it has been excluded from the measurements since CM is expected to appear at larger bias voltage.

The FE-I3 LGAD and reference sensors have been tuned to the same parameters, that are TOT = 30 for a collected charge of 20 ke^- with a threshold set to 3.2 ke^-. The result of the tuning procedure is shown in figure 4.11 where it is visible a larger noise for the device with CM layer that turns into a larger spread of the TOT and threshold distributions with respect to the reference sensor. The larger noise of the LGAD sample is in any case much lower than the threshold and will not affect in

a relevant way the efficiency of the device. In addition, since the TOT to charge conversion will be applied to each readout channel, the broader TOT distribution will be neutralized by the conversion to equivalent charge.

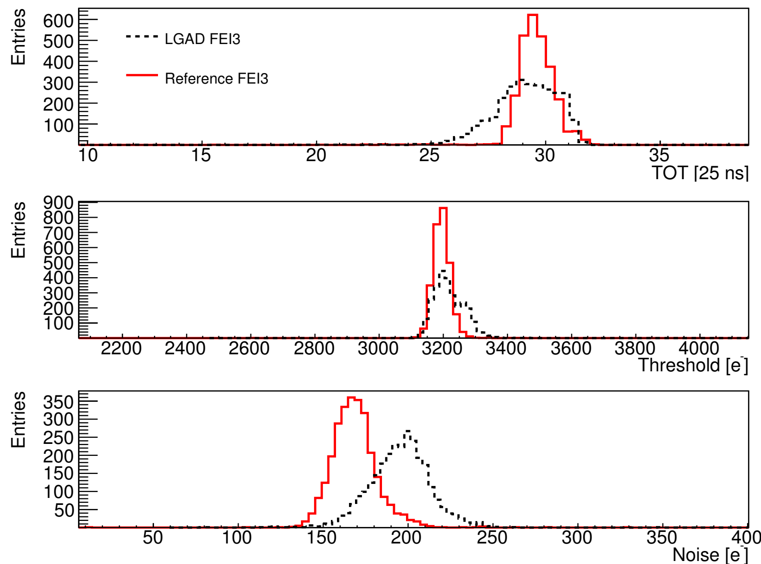


Figure 4.11: Distribution of the TOT, threshold and noise for all the readout channels of the LGAD FE-I3 (dashed black) and of the reference (solid red) devices after tuning.

The two FE-I3 sensors are therefore set to the same working configuration and exposed to the radiation of a ^{90}Sr β-source. A scintillator is placed below the sensor to provide a trigger signal to the readout system during the source scans. These scans have been repeated for increasing values of bias voltage until breakdown is reached.

In a pixel device the electron-hole pairs cloud produced by an ionizing particle is often not confined into the volume of a single pixel generating a signal in two or more neighbouring readout channels. For each trigger the TOT values returned by the chip are converted into equivalent charge and the hits of neighbouring pixels are clustered together. The result is a cluster charge distribution that is fitted with the convolution of a Landau and a Gauss distributions. From each fit, the collected charge MPV is taken. The MPVs of the collected charge are plotted against the bias voltage for both the LGAD and reference sensors in figure 4.12, where the bands indicate the uncertainty due to the charge calibration capacitor.

The reference device reaches a saturation at a bias voltage $V \sim 50\,\mathrm{V}$ with a collected charge of about $22\,\mathrm{ke}^-$, as expected from the depletion voltage. The LGAD device shows a similar behaviour saturating at $V \sim 50\,\mathrm{V}$ with a collected charge compatible with the one of the reference device within the charge calibration uncertainties. Moreover, as explained in the previous section, the gain is expected to increase with increasing bias voltage due to the larger electric field in the multiplication region, but

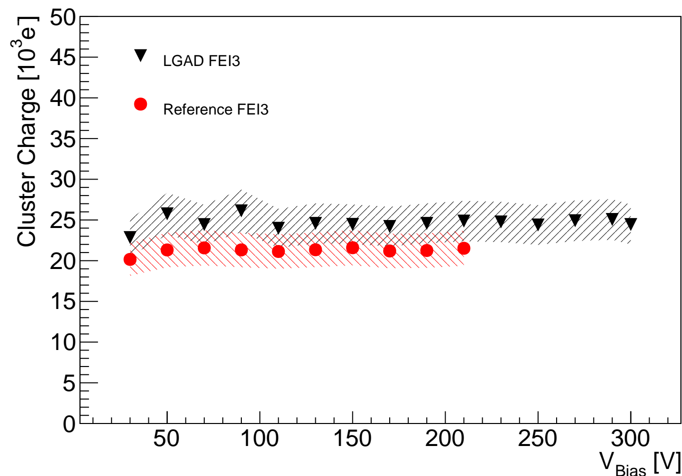


Figure 4.12: Charge collection MPV for FE-I3 LGAD and reference devices as a function of the bias voltage. The bands indicate the charge calibration uncertainties.

no increase in the collected charge is shown up to the breakdown voltage.

The measurements presented in the previous sections show that both strip and pixel devices of CNM production run 6827 do not show charge multiplication. Different geometries and diffusion of the n^+ implant for strip detectors have been tested with red and infra-red laser pulses in a TCT set-up, and an FE-I3 compatible pixel device has been tested with β electrons from a ^{90}Sr source. None of the tested devices showed evidence of charge multiplication. The difference with respect to the previous diode production that successfully showed a gain of 8 in $5 \times 5\,\mathrm{mm}^2$ square diodes [52] is, beside the segmentation of the detector, the absence of the JTE. Edge effects on the electric field due to the absence of the JTE combined with the small size of the charge multiplication implant may be the cause of the absence of gain in devices with fine segmentation. To solve this issue, and to guarantee uniformity in the charge multiplication, CNM is developing a technology called inverse LGAD (iLGAD) where the segmented electrode is the p^+ and a uniform p^+ charge multiplication layer is implanted underneath the n^+ electrode in a *p-type* substrate [59].

4.2 LGAD for timing

As mentioned in section 2.2.3, silicon sensors can be used for timing applications. Avalanche photo-diodes and silicon photo-multipliers can easily achieve a sub-nanosecond timing resolution. However, these devices are optimized for photon detection. To measure the timing of charged particles a light signal has to be generated with a scintillating bar or fibre or with a Cherenkov radiator. Moreover, the radiation toler-

ance of these devices is not sufficient for application in harsh radiation environments, where not only the radiation hardness of the silicon detector but also the scintillating element and light guide, whose transparency is affected by radiation, have to be taken into account.

Low Gain Avalanche Detectors are studied as a radiation hard detector of *mips* for timing applications. In section 2.2.3 the beneficial effects of the reduced thickness and large slew rate have been shown. In detectors with intrinsic charge multiplication the S/t_{rise}, and as a consequence the time resolution, receives additional benefit from the reduced thickness.

In detectors without gain the slew rate does not depend on the detector thickness. The current signal in a silicon detector is given by the Ramo theorem

$$i \propto qvE_w. \tag{4.1}$$

The charge q is given by the number of electron-hole pairs generated by the impinging ionizing particle. A *mip* creates an average number of electron-hole pairs per micrometer of $k \sim 75\,\mathrm{n_{eh}}/\mu\mathrm{m}$, leading to a total charge of $q = ked \sim 75ed$ for perpendicular incidence where d is the detector thickness in μm. The drift velocity v is a linear function of the electric field, hence of the applied bias voltage, at low values of the electric field with a saturation when the field reaches values of $\sim 10\,\mathrm{kV/cm}$. For timing application it is important to minimize the collection time, therefore the detectors are usually operated at large bias voltage where the drift velocity is constant. The weighting field depends on the electrode configuration. For a pad with size larger than the detector thickness the parallel plate model can be used, that is $E_w = 1/d$.

Equation 2.17 can be used to compute the maximum current in a sensor without charge multiplication, that is the initial current when all the charges contribute to it before reaching the electrodes:

$$i_{max} \propto kedv\frac{1}{d} = kev. \tag{4.2}$$

This formula shows that the peak current does not depend on the detector thickness because the weighting field compensates the larger charge.

However, in detectors with intrinsic gain, the slew rate is determined by both the gain and the thickness. In LGAD detectors the doping profile is such that the electrons approaching the cathode experience an intense electric field able to ignite a multiplication avalanche generating additional electron-hole pairs. The current has therefore an additional contribution given by the secondary charges produced in the avalanche. The number of electrons entering the multiplication region in the unit

time is

$$\frac{\mathrm{d}Q}{\mathrm{d}t} = kev. \tag{4.3}$$

Each electron produces a number of pairs depending on the gain G. The rate of charge production in the multiplication layer hence is

$$\frac{\mathrm{d}Q_G}{\mathrm{d}t} = G\frac{\mathrm{d}Q}{\mathrm{d}t} = Gkev. \tag{4.4}$$

Applying the Ramo theorem to evaluate the current increase due to the charges introduced by the multiplication process

$$\mathrm{d}i_G \propto \mathrm{d}Q_G v\frac{1}{d} \propto \frac{G}{d}\mathrm{d}t. \tag{4.5}$$

The slew rate for the signal induced by charge multiplication results to be directly proportional to the gain and inversely proportional to the detector thickness [60]:

$$\frac{\mathrm{d}i_G}{\mathrm{d}t} \propto \frac{G}{d}. \tag{4.6}$$

Thus, devices that are both thin and with intrinsic charge multiplication are expected to have an improved timing resolution.

The LGAD technology developed at CNM Barcelona initially on 300 μm thick devices with a multiplication factor of about 10 showed a time resolution of 120 ps for a *mip* [49]. Thinner detectors were predicted to improve the timing resolution down to 30 ps for a 50 μm thick device with the same gain level [60]. The improved performance is due to a lower Landau fluctuation and a larger slew rate, as explained above. In addition to CNM, two other companies started to produce LGAD sensors, these are the Fondazione Bruno Kessler (FBK) in Italy and Hamamatsu Photonics in Japan.

4.2.1 CNM LGAD production run 9088

The first CNM thin LGAD production (run 9088) has been delivered in May 2016. The production includes a total of 14 wafers, four of them produced on 300 μm thick float zone wafers for comparison with previous productions, the others have been made on 100 mm silicon-on-insulator (SOI) with a nominal thickness of 50 μm on a 300 μm thick support wafer. The effective thickness is reduced to 45 μm due to the implantation of the n^+ and p^+ electrodes in the front and back side respectively.

Each wafer contains different structures, mostly single pad square diodes of active area $1.3 \times 1.3\,\mathrm{mm}^2$ and $3.3 \times 3.3\,\mathrm{mm}^2$ named respectively LGA and LGB, while the largest part of the wafer is used for arrays of diodes designed for the HGTD and

CT-PPS/TOTEM experiments, see figure 4.13.

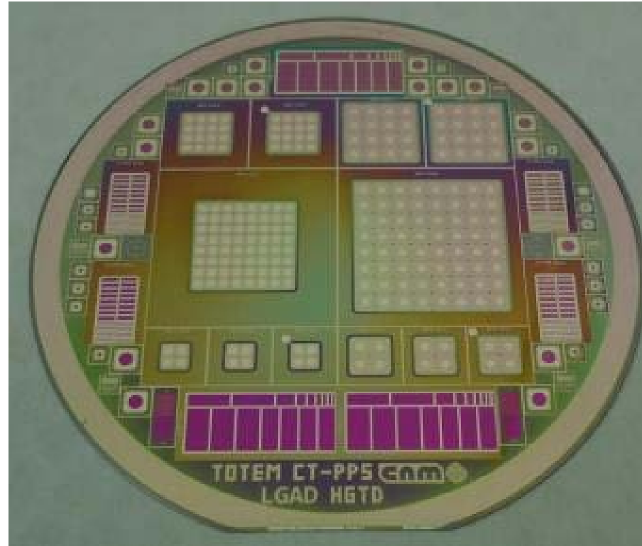
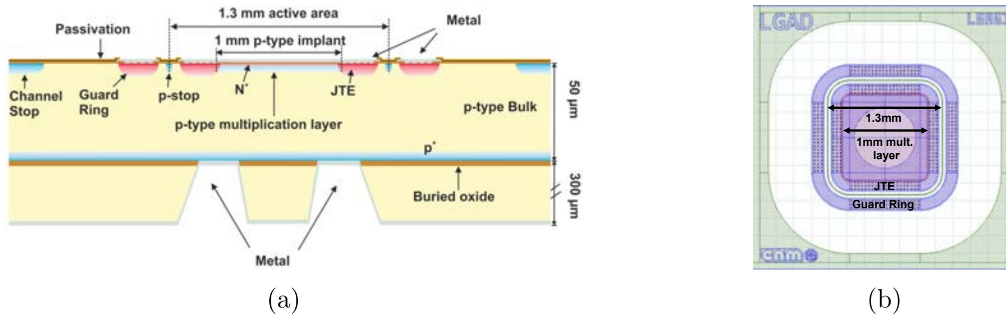


Figure 4.13: Picture of a wafer from CNM LGAD production run 9088.

The doping profile of the diodes is similar to the one described in section 4.1. The central region of the diode hosts the n^+ electrode and the p^+ multiplication layer and is 1 mm wide. It is surrounded by the JTE, that improves the diode voltage capability and defines the electric field at the sensor periphery, a p-stop and a guard ring. The total active area of the diode is defined by the p-stop ring and is 1.3 mm wide, but only the charge collected in the central region will be amplified through the CM avalanche mechanism. The support wafer and the buried oxide layer on the back side are etched to allow to electrically contact the *p-type* electrode. The backside of the wafer is fully metallized while on the top side of LGA and LGB diodes metal contacts are placed on the guard rings and the central region with an opening to allow laser testing, see figure 4.14.

On the ten SOI wafers the implantation of the multiplication layer has been done with three different doses in order to study devices with different performances in terms of gain and voltage capability. The implantation doses of the multiplication layer were 1.8 (low) for wafers 3 and 4, 1.9 (medium) for wafers 5 to 10 and $2.0 \cdot 10^{13}\,\mathrm{cm}^{-2}$ (high) for wafers 11 and 12. Each wafer also contains diodes without multiplication layer to be used as reference.

The measured samples are described in table 4.2. The samples have been characterized with IV and CV measurements on a probe station to verify the voltage capability and the voltage of full depletion. Some of the sensors have been irradiated with thermal neutrons at the TRIGA nuclear reactor of the Jožef Stefan Institute (JSI) in Ljubljana to 3 and $10 \cdot 10^{14}\,\mathrm{n_{eq}/cm^2}$.



(a) (b)

Figure 4.14: Schematic cross section 4.14a and top view 4.14b of the LGA diode in CNM run 9088.

Measured devices	Implantation dose	Fluence $[10^{14}\,\mathrm{n_{eq}/cm^2}]$	Short name
W3-LGA-61	low	0	low,unirr,L1
W3-LGA-71	low	0	low,unirr,L2
W3-LGA-33	low	0	low,unirr,L3
W5-LGA-45	med	0	med,unirr,L1
W5-LGA-81	med	0	med,unirr,L2
W5-LGA-51	med	3	med,3e14,L1
W7-LGA-45	med	3	med,3e14,L2
W5-LGA-43	med	10	med,1e15,L1
W7-LGA-35	med	10	med,1e15,L2

Table 4.2: List of the measured devices with the n^+ implantation dose and irradiation fluence.

The plots in figure 4.15 show the capacitance (CV) and current (IV) values against the bias voltage. The CV curve is represented as $1/C^2$ to better show where depletion occurs. The slope depends on the doping concentration while the asymptotic value is defined by the sensor thickness. Below ~ 32 V the multiplication region is slowly being depleted and $1/C^2$ stays at low values. Subsequently, in about 3 V the high resistivity bulk is depleted and the capacitance drops to a value of 3.9 pF, compatible with a diode of 45 μm active thickness. The capacitance drop happens with of about 1 V of difference in the bias voltage between the low and medium dose samples, compatible with the different concentration of dopants. From the IVs shown in figure 4.15b it is interesting to note that after irradiation the devices can be operated at significantly larger voltages than before irradiation. This will eventually allow to partially recover the LGAD performance after irradiation.

^{90}Sr Characterization

The response of these devices to beta particles from a ^{90}Sr source has been measured at the JSI laboratories in Ljubljana. From these measurements the total collected charge

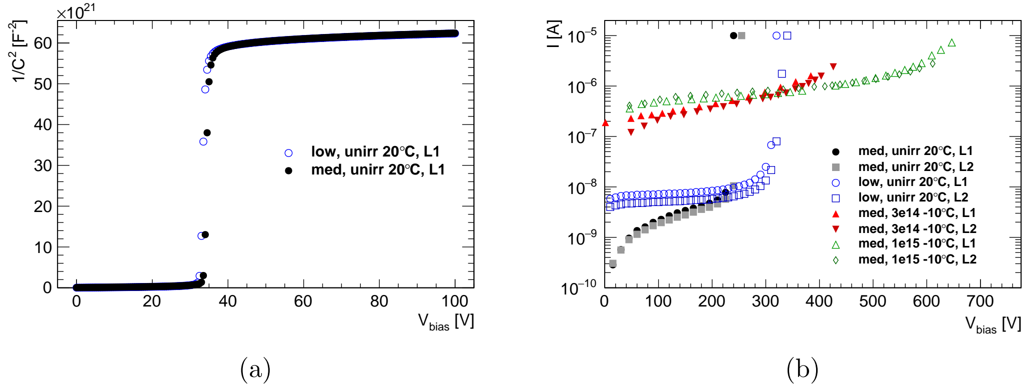


Figure 4.15: Characteristic CV (a) and IV (b) of the LGA diode in CNM run 9088. The CV is shown only for one non irradiated sample of each implantation dose, the IV is shown for all the measured samples, at the temperature of 20°C for the non irradiated and at −10°C for the irradiated ones.

and therefore the gain evolution with bias voltage of irradiated and non irradiated devices can be extracted.

The sensors were mounted on a dedicated aluminium box with small holes on the top and on the bottom of the sensor and placed below the radioactive source on a cold plate that also has an opening at the position of the sample. A small scintillator, roughly of the size of the DUTs, is placed underneath the cold plate and is used to trigger the readout. Only the electrons crossing the central part of the detector reach the scintillator thanks to the opening in the box.

The cold plate was used to maintain a stable working condition at −10°C for the irradiated samples and at 20°C for the non irradiated ones. The signals from the DUT were amplified in two stages by a charge sensitive preamplifier and by a shaping amplifier with a peaking time of 25 ns. The signals were then recorded by an oscilloscope and stored for a later analysis.

In order to have an absolute measure the oscilloscope scale was calibrated with the 59.5 keV photon peak of an americium (^{241}Am) source in a 300 μm thick non-irradiated float zone detector.

For each voltage, the amplitude spectrum of the collected waveforms was fitted with the convolution of a Landau and Gaussian distribution to obtain the MPV of the signal amplitude, that was successively converted to the collected charge MPV through a calibration factor. The gain is obtained comparing the charge MPV with the one of an equivalent 45 μm thick sensor without charge multiplication layer from the same run, measured to be 2.88 ke^{-}.

The results are summarized in figure 4.16 where we can firstly see that devices with the same implantation dose and fluence behave similarly, confirming the good

reproducibility of the LGAD process. The effect of the different implantation can be compared in the non irradiated devices where at the same bias voltage the medium dose devices have a larger gain than the low dose sample. However, the low dose sample can be operated at a larger bias voltage reaching a maximum gain value similar to the one of the medium dose sample.

Irradiation has the effect of effectively removing the acceptor dopants in the silicon substrate, including the multiplication layer [51, 61]. As a consequence the gain of irradiated devices is suppressed. At a bias value of 200 V the gain is only 4 for the $3 \cdot 10^{14}\,\mathrm{n_{eq}/cm^2}$ devices and 1 for the $10^{15}\,\mathrm{n_{eq}/cm^2}$ ones, against the gain of 20 that devices with the same multiplication layer have before irradiation. Nevertheless these devices can be operated at higher bias voltage reaching a gain of about 18 at 425 V and 10 at 650 V respectively.

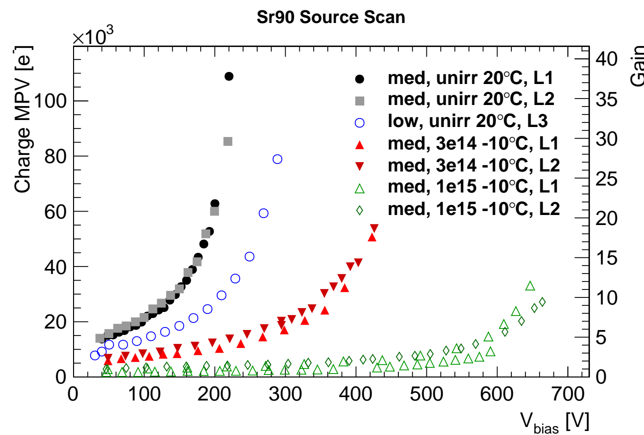


Figure 4.16: Charge collection MPV and gain measured with a ^{90}Sr source.

Beam Test Characterization

The same devices have been tested in the H6B beam line of the CERN-SPS North Area beam test facility with 120 GeV pions for a first measurement of the timing resolution of 45 μm LGAD devices.

The sensors were mounted on a Printed Circuit Board (PCB) originally designed for TCT measurements. The bias is applied to the backside through a low-pass RC filter, the central pad is connected via a bond wire to an SMA connector while the guard ring is floating. A broad band amplifier is connected to the SMA and the amplified signal is then recorded by an Agilent Infiniium DSA91204A oscilloscope [62] with 40 GS/s sampling rate and a band width of 12 GHz. In addition two Silicon Photo-Multipliers (SiPMs) coupled to Cherenkov-light emitters quartz bars have been used as fast (10 ps) timing reference [63]. The quartz bar, with a cross section of

$3 \times 3\,\mathrm{mm}^2$ and a length of 30 mm, were aligned with the beam direction.

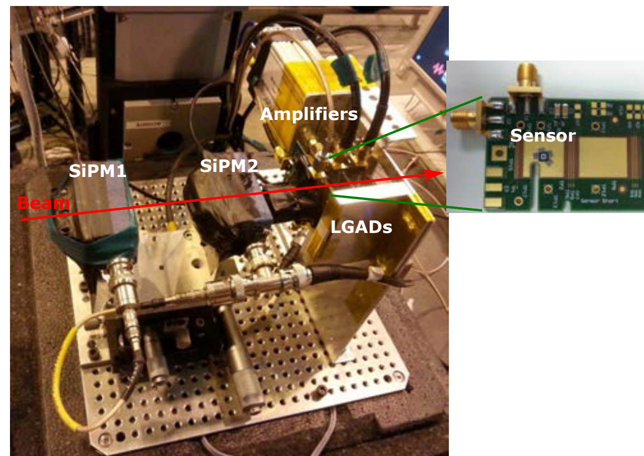


Figure 4.17: The LGAD measurement set-up during the beam test in the H6B beam line of CERN-SPS.

The PCB with the LGAD devices were mounted on an aluminium support frame and together with SiPMs fixed to an aluminium base plate, see figure 4.17. The SiPMs were mounted on a mechanically adjustable pedestal to permit the alignment with the LGAD sensors while the base plate was mounted on a remotely controlled movable stage to align the sensors with the pion beam. It was possible to cover the base plate with a styrofoam box to ensure light tightness and thermal insulation during cooling. The cooling was needed for the operation of irradiated devices and was performed with dry ice bricks placed inside the styrofoam box.

Dry ice is solid state carbon dioxide that sublimate at the temperature of $-75°$C, the cold gaseous CO_2 originated by the sublimation cool down the environment in the styrofoam box. Nevertheless due to a non perfect thermal insulation and the presence of power consuming electronics acting as heat sources, the temperature of the sensors results to be much higher. The irradiated sensors have been measured in two batches, first the ones irradiated to $3 \cdot 10^{14}\,\mathrm{n_{eq}/cm^2}$ and then the ones irradiated to $10^{15}\,\mathrm{n_{eq}/cm^2}$. The temperature on the sensor was estimated comparing the sensor leakage current to the one measured in a laboratory climate chamber at different temperatures, resulting to be respectively $-6°$C and $-15°$C.

Different amplifiers were available: the CIVIDEC C2 TCT amplifiers [64], the Particulars TCT amplifiers [65] and the custom-made AFP pre-amplifiers [63]. Inital tests have been carried out to find the amplifier with the best performance in terms of time resolution. The CIVIDEC C2 TCT showed to perform better than the others and have been therefore used to characterize the LGAD devices. Also the oscilloscope settings have been investigated to find an optimal configuration. The bandwidth of

the oscilloscope was varied from 0.5 GHz to 12 GHz, a too low setting would alter the rising edge of the signal while a too high value would introduce high frequency noise without an improvement of the signal rise time. The best compromise was found to be at 1 GHz, set as default value. The vertical scale setting of the oscilloscope was found to influence the noise level and therefore the time resolution, it was set to 50 mV/div and kept constant for all the measurements.

The ambient noise of the beam area and the non optimal sensor assembly on the PCB, with long bond wires and no shielding, led to run-to-run variation of the noise and the signal. The noise level was varying between 3 and 4 mV, while the signal amplitude and integrated charge had variations up to $30 - 40\%$. However, the impact on the time resolution was only about 10%.

For each run about ten thousand events were recorded. Two LGAD devices were connected to the oscilloscope together with the two SiPMs, although on some runs only one SiPM was available. The readout was triggered with a fixed threshold on the signal of one of the LGAD devices. Thanks to the large signal over noise ratio (S/N) this was possible without introducing a bias in the signal amplitude and improving the purity of the trigger, since the cross section of the quartz bar was nine times larger than the LGAD active area.

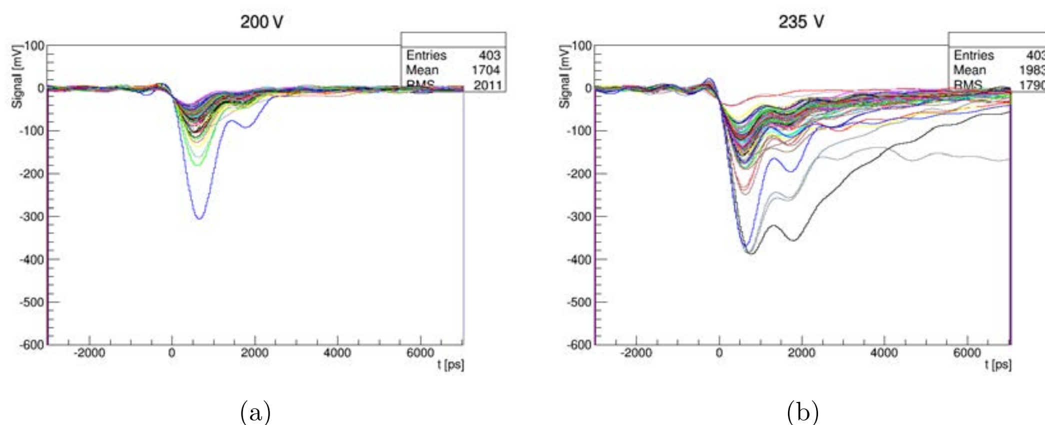
The trigger threshold was typically set to $15 \div 20$ mV. For the runs at the highest voltages this value had to be increased to avoid fake triggers due to micro-discharges in the sensor but since the gain is larger at higher voltages this operation was possible without cutting the signal distribution.

The measurements were stopped when the waveforms showed instabilities such as deformation in the shape or delays returning to the baseline or when the noise level was so high that the lowest threshold to reject the noise would have cut into the low values of the signal distribution.

Example waveforms of a non irradiated device are shown in figure 4.18. The current pulse is characterized by a duration of the order of about one nanosecond followed by a second smaller pulse due to some impedance mismatch in the readout chain.

The waveform shape is given by the superposition of the induced current from the drift of the primary electrons and holes and from the secondary holes. The current is enhanced when the primary electrons reach the multiplication layer generating more charge carriers. This will last as long as there are electrons drifting to the cathode, expected to be about 450 ps, at the drift velocity saturation of 96 μm/ns [66]. This is the intrinsic rise time of the signal. Afterwards the signal consists of the drifting of the multiplied holes until they reach the opposite electrode. The intrinsic pulse is convoluted with the electronics response function whose contributions come from the

sensor capacitance combined with the amplifier impedance and the bandwidth of the oscilloscope.



(a) (b)

Figure 4.18: Waveforms from sample med,unirr,L1 at a bias voltage of 200 V with a gain of 14 (a) and 235 V with a gain of 35 (b).

The amplitude distribution of selected devices and voltages is shown in figure 4.19 and the histograms are fitted with a Landau-Gauss distribution function to extract the amplitude MPV. Figure 4.19a shows the effect of bias voltage on non irradiated devices. At larger voltages the MPV moves to larger values and at the same time the distribution gets broader. Figure 4.19b instead shows the effect temperature and irradiation. At larger fluences, despite the larger bias applied, the pulse amplitude is suppressed while at lower temperature the amplitudes tend to be larger although the diode breakdown occurs at lower voltage. However the amplitude distributions of the med,3e14 device are much broader than before irradiation. The suppression of the amplitude of the med,1e15 sample due to a higher irradiation fluence leads to a lower distribution width as well.

The charge, and hence the gain, follow a behaviour similar to the amplitude MPV. The charge is calculated integrating the waveform from -1 to 4 ns and the gain is obtained dividing the integral by the signal of an equivalent sensor without gain. It was not possible to directly measure a 45 μm thick reference because of the low signal to noise ratio, the charge was calibrated by scaling the signal of a 300 μm thick diode. The gain showed run to run variation up to about $30-40\%$ due to the non stable environment of the test beam area in terms of noise and temperature.

In addition to amplitude (4.20a), charge and gain (4.20b) other important parameters have been extracted from the analysis of the waveforms. Such as the baseline noise N (4.20c) taken as the RMS of the waveform baseline, the signal to noise ratio S/N (4.20d) taken as the signal amplitude MPV divided by the noise RMS, rise time $\tau_{10-90\%}$ (4.20e) taken as the time in which the waveform goes from the 10% to the

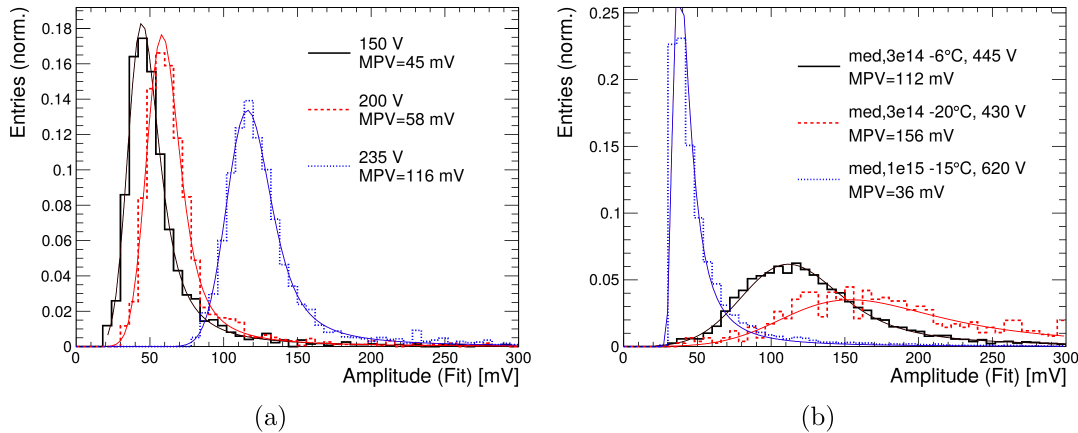


Figure 4.19: Amplitude distribution of sample med,unirr,L1 for different bias voltages (a) and for the irradiated devices at the maximum bias voltage measured (b).

90% of its own amplitude and the jitter σ_{jitter} (4.20f) that from equation 2.20 can be estimated by $\sigma_{jitter} \sim \tau_{10-90\%}/(0.8\, S/N)$.

It is interesting to notice how the amplitude MPV and the gain grow exponentially approaching the breakdown voltage, confirming the ^{90}Sr measurements shown in figure 4.16, while the noise is stable for non irradiated devices and grows slowly for non irradiated ones so that the S/N ratio results enhanced with larger bias voltage. On the other hand, the jitter decreases with increasing bias as well as the rise time. The larger signal over noise ratio, slew rate and lower jitter all contribute to an improvement on time resolution as shown in equation 2.18.

The measurement of time resolution of thin LGAD devices was the main goal of the measurement at the test beam facility. It was measured by the spread of the time of arrival difference (Δt) between two devices, which contains the contribution from both devices.

The signal from the SiPMs used as timing reference was processed by a CFD returning a digital signal. The time of arrival was taken at the fixed threshold value of 250 mV, about half of the signal amplitude. Instead, for the LGAD devices the analog waveform was sampled in 25 ps bins and stored. An offline CFD algorithm has been used to correct for time walk fluctuation. The threshold was then defined for each waveform as a constant fraction of the signal amplitude. The time of arrival was taken as the time the signal was crossing the threshold value interpolating linearly from the measurement points just above and below the threshold. Other algorithms were tested, including more points, using polynomial fit or spline interpolation but no significant improvement was noticed. The threshold of the CFD algorithm was scanned in steps of 5% from 10% to 90% of the signal amplitude and the optimal value was taken. This value changed depending on the device and on the voltage

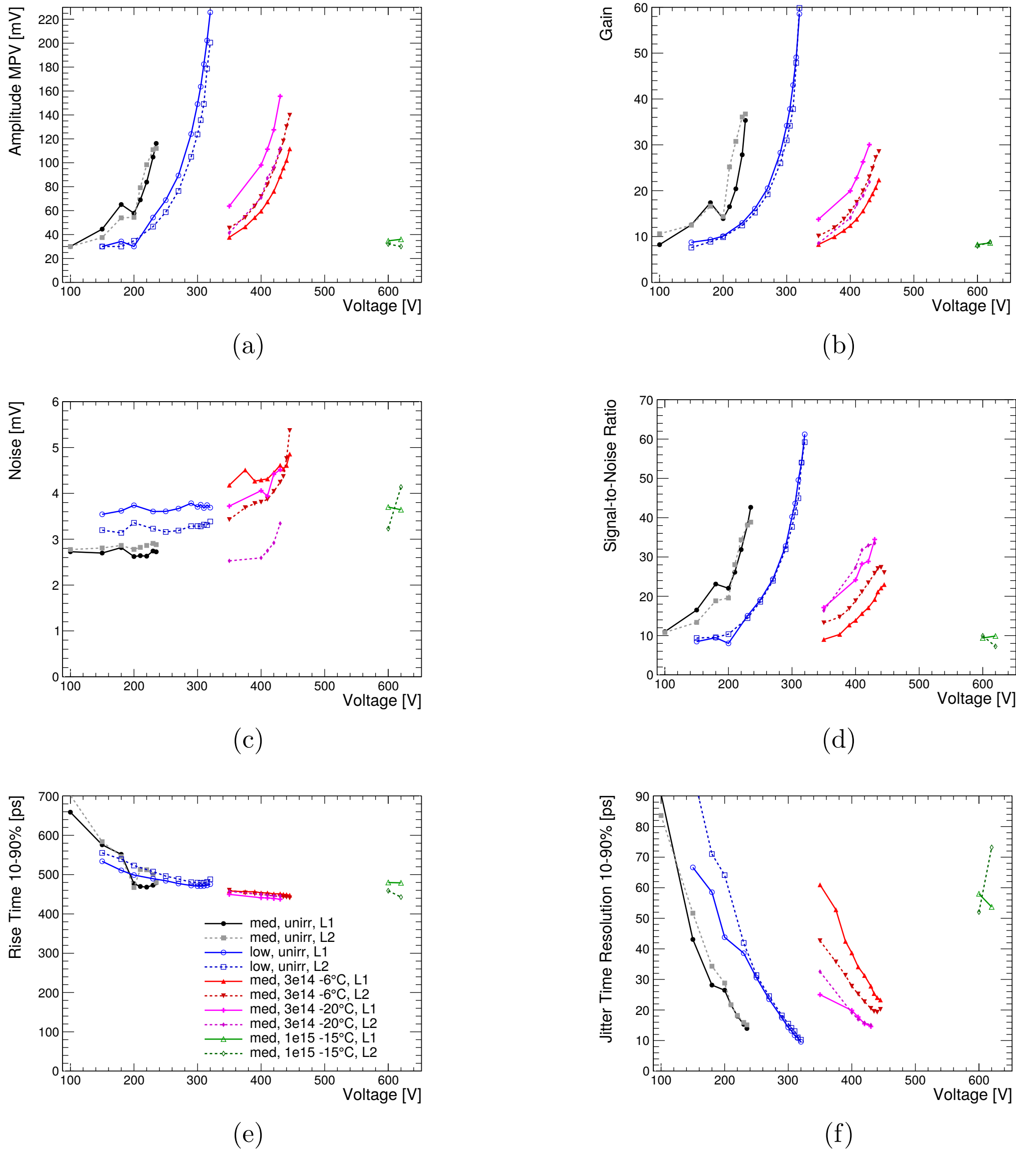


Figure 4.20: Overview of waveform parameters for all the measured devices as a function of voltage.

applied. Probably due to the waveform shape variation that makes the rising edge steeper at different points. For the non irradiated devices the optimal value of the CFD threshold was found to be around 80% at low voltages decreasing to 20% at the maximum measured voltage, while for the irradiated devices it stayed between 80 and 90%.

Figure 4.21 shows the Δt distributions for different devices. The spread of each distribution σ_{total} is obtained by the standard deviation of a Gaussian fit that contains the contribution of the two devices. For some runs two LGAD devices have been

measured together with both SiPMs to extract the time resolution of each SiPM. An analysis of all the possible Δt combinations returned the individual SiPM time resolution as $\sigma_{SiPM1} = 13 \pm 1$ ps and $\sigma_{SiPM2} = 7 \pm 1$ ps, the uncertainties contain the statistical contribution of 0.2 ps and a run by run fluctuation of about 1 ps. The time resolution of the LGAD devices is typically evaluated in combination with SiPM2 that showed a better time resolution. The contribution of the SiPM is subtracted from σ_{total} assuming $\sigma^2_{total} = \sigma^2_{LGAD} + \sigma^2_{SiPM}$. During the beam tests some runs have been taken with the two sensors irradiated to $3 \cdot 10^{14}\,\mathrm{n_{eq}/cm^2}$ in a climate chamber at the temperature of $-20°C$, for these runs it was not possible to include any SiPM in the readout so that the average time resolution of the two devices is measured as $\sigma_{\langle LGAD\rangle} = \sigma_{total}/\sqrt{2}$.

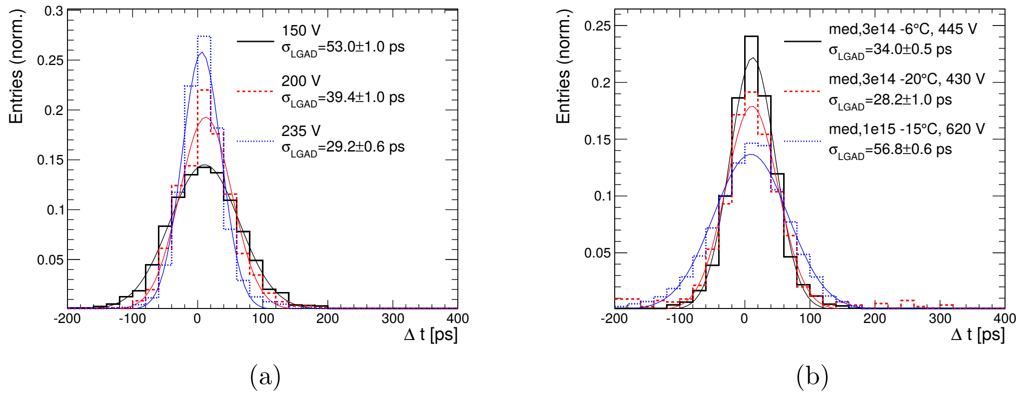
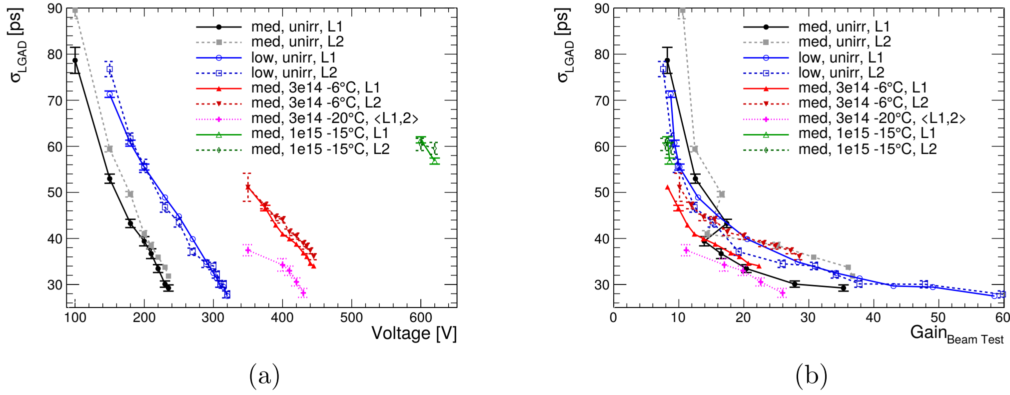


Figure 4.21: Time of arrival difference (Δt) distribution between an LGAD and a SiPM. Device med,unirr,L1 at different voltages (a) and irradiated devices at the maximum measured voltage (b) are shown. The LGAD time resolution σ_{LGAD} is obtained by the width of a Gaussian fit subtracting the SiPM contribution.

The dependence of the time resolution on the bias voltage and on the gain is shown in figure 4.22a and 4.22b respectively. The uncertainties shown are statistical only, a systematic run by run uncertainty of about 10% adds up to about 3 ps at the highest measured voltage.

The decrease of σ_{LGAD} with the applied bias voltage is almost linear and the agreement between devices with the same dose and irradiation is within the uncertainties. The time resolution as a function of gain (instead of voltage) shows that the different curves tend to overlap independently of dose and fluence showing an approximately universal relation between time resolution and gain. The spread between the curves is within the systematic uncertainties of the gain obtained in the beam test measurements, that is, about $30 \div 40\%$. Deviations from this universal trend are expected with significant variation of the noise that can degrade the time resolution and different temperature that affects the impact ionization coefficient at the origin



(a) (b)

Figure 4.22: LGAD time resolution σ_{LGAD} as a function of voltage (a) and gain (b) for all the measured devices.

of the multiplication effect.

The best time resolution measured for each device corresponds to the measurement at the highest voltage. The non irradiated low and medium dose devices reached very similar time resolution of 29 ps at 235 V and 30 ps at 320 V respectively.

After irradiation to $3 \cdot 10^{14}\,\mathrm{n_{eq}/cm^2}$ the medium dose devices can reach a time resolution as good as before irradiation. This value was obtained measuring the devices in the climate chamber at the temperature of $-20°C$ and a bias voltage of 430 V. When measured with dry ice cooling at the same voltage the on-sensor temperature was $-6°C$ and the time resolution degraded by about 8 ps (to 38 ps). This can be explained by the larger noise and lower gain due to the higher temperature.

A complete study of the devices irradiated to $10^{15}\,\mathrm{n_{eq}/cm^2}$ was not possible because of an incident that occurred during a long no-beam period where both samples were installed in the cooling box while cooled with dry ice and biased at 600 V. An increase of the temperature inside the box led to a thermal runaway of the sensors after which both devices showed a reduced breakdown voltage of about 1 V and could not be used for further measurements. The measurement at the largest bias voltage before the incident was with a bias of 620 V where a time resolution of 57 ps has been measured.

However the results point to the possibility to use the LGAD technology for timing detectors with a resolution of 30 ps that can be maintained after irradiation up to $3 \cdot 10^{14}\,\mathrm{n_{eq}/cm^2}$. An improvement of the voltage capability of the diodes and a better retention of the gain would push further the radiation hardness of such devices.

4.2.2 FBK UFSD2 production

After CNM, the Fondazione Bruno Kessler produced LGAD devices under the denomination Ultra-Fast Silicon Detectors (UFSD), a name that highlights the good timing performance of this type of sensor. The FBK UFSD2 production has been manufactured on 150 mm silicon-on-silicon (Si-on-Si) wafers with a thickness of 60 μm wafers. The active thickness is reduced to about 50 μm after the thermal bond on the support wafer and the electrodes implantation [67].

When this production started it was already known that the radiation tolerance of the boron based multiplication layer was not large enough for HL-LHC applications but the boron multiplication layer is partially removed with irradiation degrading the performance of the sensor. Under the effect of irradiation the boron atoms in the gain layer switch from substitutional to interstitial. Interstitial atoms are electrically inactive and do not contribute to the multiplication mechanism any more [68].

The UFSD2 production includes wafers where the boron of the multiplication layer has been replaced by gallium atoms that has a lower probability to become interstitial [69]. In addition, on some wafers, carbon atoms have been added to the multiplication layer volume as carbon has a higher probability to get interstitial with respect to boron or gallium, hence the original doping of the multiplication layer is expected to be better preserved [70].

A total of 19 wafers was produced with different combination of the implantation dose of the boron or gallium as well as two different concentrations of the carbon implants.

Part of the diodes from this production has been irradiated with thermal neutrons at JSI to the fluence of $6 \cdot 10^{14}\,\mathrm{n_{eq}/cm^2}$ and $3 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$. Non irradiated and irradiated diodes have been characterized with current-voltage measurements on a probe station and the response to the pulsed laser of a TCT set-up has been analysed to measure the gain of the devices.

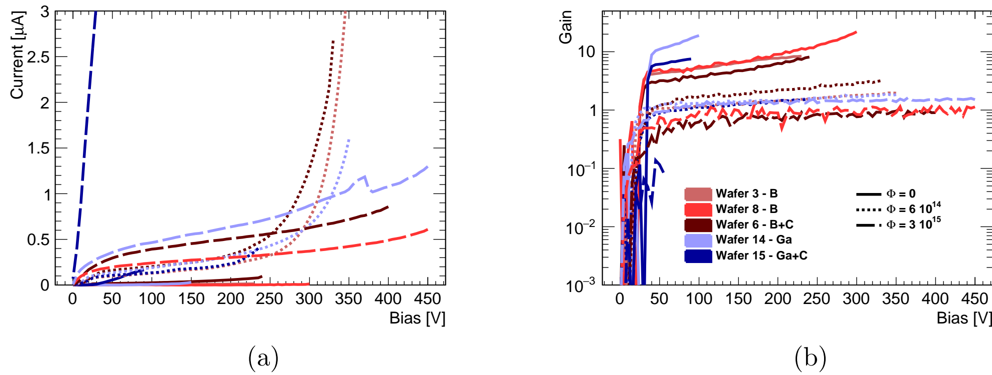
The IV curves shown in figure 4.23a have been measured on the same TCT set-up. The maximum applied voltage is usually just below the breakdown voltage that was determined manually before the TCT measurements. The sensors were mounted on the same PCB described in section 4.1.1. A Peltier element placed behind the aluminium holder for the PCB allows to cool the irradiated sensors while dry air is flushed inside the TCT volume to reduce the humidity level and avoid condensation on the sensor. The measurements have been performed at room temperature for the non irradiated devices and at $-15°C$ for the irradiated ones. The characteristics of the tested samples is shown in table 4.3.

Each LGAD diode of this production is paired to a PIN diode that only differs in the absence of the multiplication implant. The gain shown in figure 4.23b is

Wafer	CM Dopant	CM Dose [au]	Carbon Enriched
3	Boron	1.00	No
6	Boron	1.02	Yes
8	Boron	1.02	No
14	Gallium	1.04	No
15	Gallium	1.04	Yes

Table 4.3: List of the measured devices from the FBK UFSD2 production.

measured comparing the collected charge of the LGAD to the one of a non irradiated PIN diode from the same wafer. To take into account temperature effects, the charge of irradiated sensors is compared to the one of the PIN diode measured at the same temperature.



(a) (b)

Figure 4.23: FBK UFSD2 current-voltage relation (a) and gain (b) measured on the TCT set-up. The measurements of non irradiated devices have been performed at room temperature while irradiated devices were cooled to $-15°C$.

The IVs show the expected behaviour with a slightly larger current for the sensors with carbon implantation among the non irradiated samples. The increase of leakage current with fluence together with the shift to larger value of the breakdown voltage is observed, with the exception of the sensor from wafer 15 irradiated to $3 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$ whose current grows linearly reaching a value of about $3\,\mu$A at 50 V.

Before irradiation the gain of all the measured sensors reaches the target value of ~ 10. After irradiation it is impossible to reach the same gain level. At the fluence of $3 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$ the sensor from wafer 6 has a larger gain with respect to all the others showing a beneficial effect of the carbon implantation together with the boron in the multiplication area. Nevertheless due to the early breakdown only a maximum gain of about 3 was reached. At higher irradiation dose the effect of carbon enrichment on wafer 6 fade out and all the curves fall to a gain of about 1.

4.2.3 CNM LGAD production run 10478

The CNM LGAD production run 10478 consisted of a total of five wafers, two of them, wafer 4 and wafer 5, are 100 mm Si-on-Si wafers where a 50 μm thick high resistivity wafer is bonded to a 300 μm thick support. The remaining wafers were 300 μm thick, high resistivity float zone wafers, for comparison with previous productions. Wafer 5 is a carbon enriched wafer to verify the possible advantage in terms of radiation hardness.

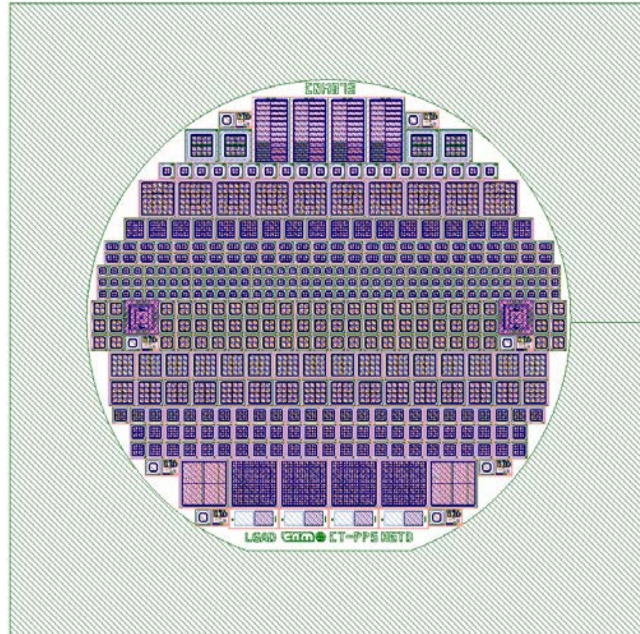


Figure 4.24: Picture of a wafer from CNM LGAD production run 10478.

The mask, shown in figure 4.24, contains several single pad square diodes of $1 \times 1\,\text{mm}^2$, $1.3 \times 1.3\,\text{mm}^2$ and $2 \times 2\,\text{mm}^2$, 2×2, 3×3 and 8×8 matrices of different pixel sizes and 2×1 arrays with different spacing for fill factor studies. Some of the 2×2 matrices are compatible for bump-bonding to the ALTIROC0_V0 chip.

The cross section in figure 4.25 shows that the design of the LGAD diodes is identical to the one of run 9088 with the only difference being in the etching of the support wafer, that is not needed because the electrical contact is achieved through the silicon support wafer.

Fill factor study with TCT

The 2×1 arrays for fill factor studies consist of three different families named RA, RB and RC. While the pixel size is the same, $1 \times 1\,\text{mm}^2$, the distance between the pixels differs, being 45, 55 and 65 μm respectively.

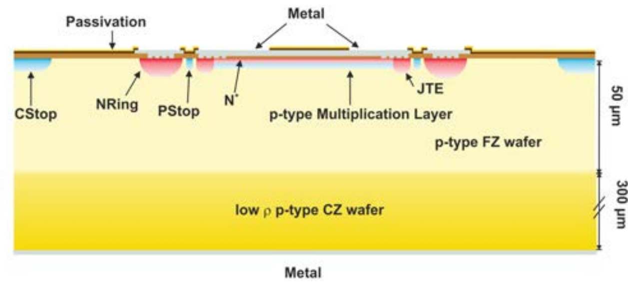


Figure 4.25: Schematic cross section of an LGAD diode from CNM production run 10478.

Three samples from wafer 4, one per each family, have been tested on the TCT set-up with the edge-TCT technique. The dicing of the wafer usually leaves scratches on the side of the sensors so that before assembling them on the PCB the side is polished using $3\,\mu$m grit diamond paper and $3\,\mu$m grit diamond paste.

After polishing the edge that will be illuminated by the laser pulses the sensors are mounted on a TCT specific PCB placing the sensor over an opening to avoid the screening of the laser spot Gaussian tails, see figure 4.26. The gluing is done with a silver-added conducting paste that provide electrical contact to the backside.

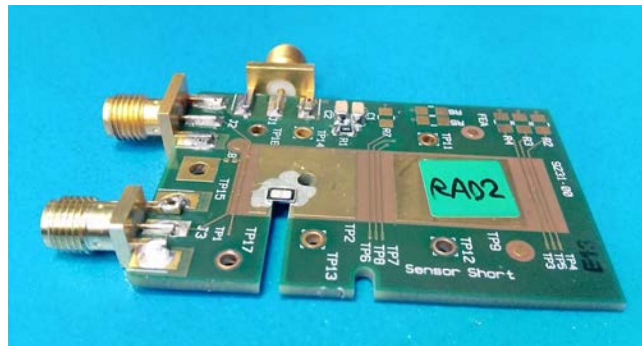


Figure 4.26: Picture of an RA array assembled on the PCB for edge-TCT.

The two pixels of the array are connected via bond wires to two independent readout lines ending each one on an SMA connector. The backside of the sensor is connected through a low pass filter to another SMA connector from where the bias is applied. Before measuring the samples on the TCT set-up, an IV characterization of the samples has been done and is shown in figure 4.27. The early breakdown of sample RA and the higher leakage current of sample RC are not relevant to study the fill factor. Full depletion is reached by all devices and the current level of the RC sample is not critically high.

On the TCT set-up a two-dimension scan was performed on each sample where the response to an infra-red pulsed laser over an area of 100×200 or $100 \times 220\,\mu\mathrm{m}^2$

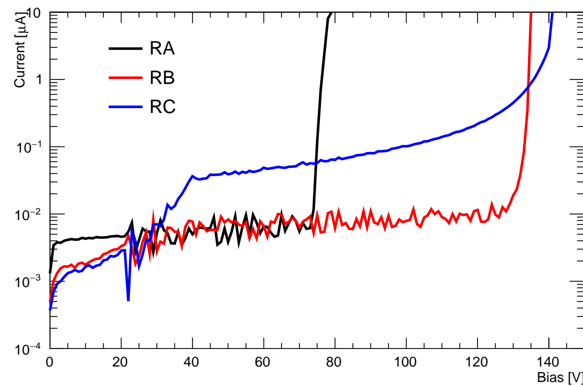


Figure 4.27: Current-Voltage characterization of the RA, RB and RC samples.

was observed in steps of 2 μm on both sides. The measurements were performed at different bias voltages up to a maximum of 130 V besides the RA array whose maximum bias has been 72 V because of the early breakdown.

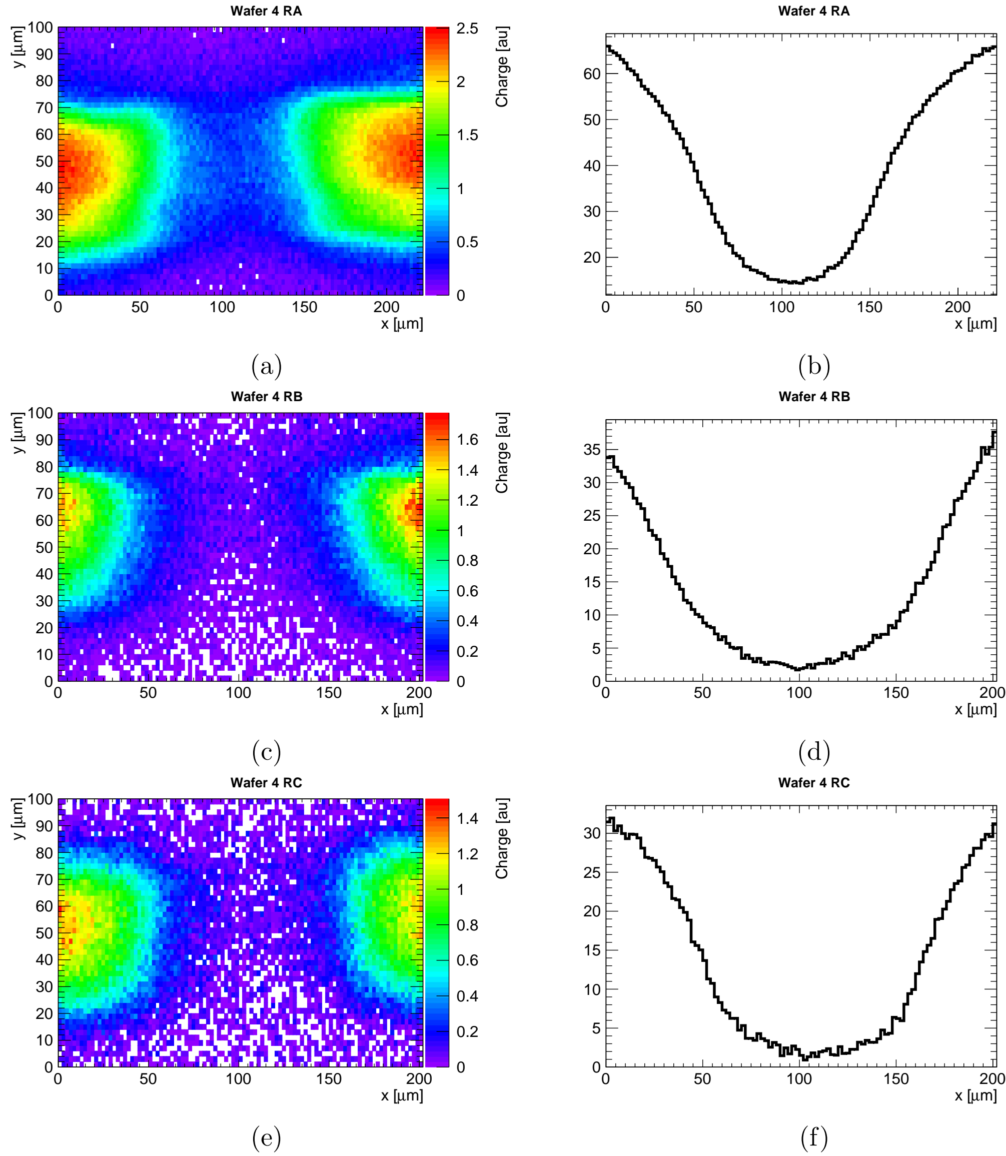
For each scanning point the waveforms of both pixels were recorded, together with the signal of a beam monitoring diode. Due to the long duration of these scans it is important to monitor the laser stability and correct for potential fluctuation in the laser intensity with time.

The waveforms were integrated to obtain the charge observed by each pixel and scaled to the beam monitor reading at that time. A map of the charge collection distribution is generated out of the waveform integrals. On the left side of figure 4.28, the superposition of the charge collected by the two pixels at the maximum measured voltage for each array is shown. In the maps, the y-axis is perpendicular to the sensor surface, with increasing values going from the inside to the top of the sensor, while the x-axis is parallel to the sensor long edge.

An inefficient region in between the pixels is visible in all the samples. To measure the width of this region, a projection of the two dimensional map over the x-axis is performed as shown on the right side of figure 4.28, and the distance between the half-maximum points on the left and on the right sides of the distribution is taken as the width estimator.

The results shown in table 4.4 show that the inefficient region is much larger (by around 60 μm) than the nominal distance between the pixels. The measured difference in width is consistent with the difference between the arrays and is independent of the applied voltage.

These measurements show that the inter-pixel gap is much larger than expected. Further tests with particle beams are needed to determine the size of the gap with perpendicular tracks. Later simulations suggested that the bending of the field lines



(a) (b)
(c) (d)
(e) (f)

Figure 4.28: Charge collection map (left) and their projections along the x-axis of the RA, RB and RC arrays obtained with edge-TCT measurements.

to the JTE deviates the charge trajectory. The charge generated in the proximity of the CM implant edges is deflected to the JTE without being amplified. This study indicates that further development work is likely to be needed to reduce the inter-pixel gap, assumed to be 50 μm in the HGTD performance simulations [42].

4.2.4 HGTD Prototype module Test

CNM LGAD production run 10478 included 25 sensors (21 LGAD and 4 PIN) per wafer compatible with the ALTIROC0_V0 chip, the first prototype of the HGTD

RA Nominal Gap 45 μm		RB Nominal Gap 55 μm		RC Nominal Gap 65 μm	
Bias	Measured Gap	Bias	Measured Gap [μm]	Bias	Measured Gap [μm]
60 V	102 μm	70 V	110 μm	70 V	118 μm
65 V	102 μm	90 V	106 μm	90 V	116 μm
70 V	100 μm	110 V	110 μm	110 V	114 μm
72 V	100 μm	130 V	138 μm	130 V	122 μm

Table 4.4: Summary of the measured gap for the three different arrays at all the measured bias voltages.

readout chip [47]. The sensors consist of 2×2 pixels of $1 \times 1\,\mathrm{mm}^2$ each surrounded by a guard ring. To connect the pixels of the sensor to the readout chip channels with bump-bonding both sensor and chip have to be prepared.

The solder bump, made of a tin-silver alloy, cannot be directly bonded to the metal contacts of chip and sensor, that are made of aluminium. At CNM it is possible to deposit a nickel-gold Under-Bump Metallization (UBM) layer on both chip and sensor that makes the bonding through tin-silver solder bump possible. The electroless and maskless nickel-gold plating technique allows a cheap and efficient deposition of the UBM on the exposed metal pads, present on both the chip and the sensor. In addition to the bump-bonding pads, the chip also contains the wire-bonding pads, needed to connect the chip to the PCB, that have to be protected to avoid undesired shorts between nearby pads that may occur because of the UBM deposition.

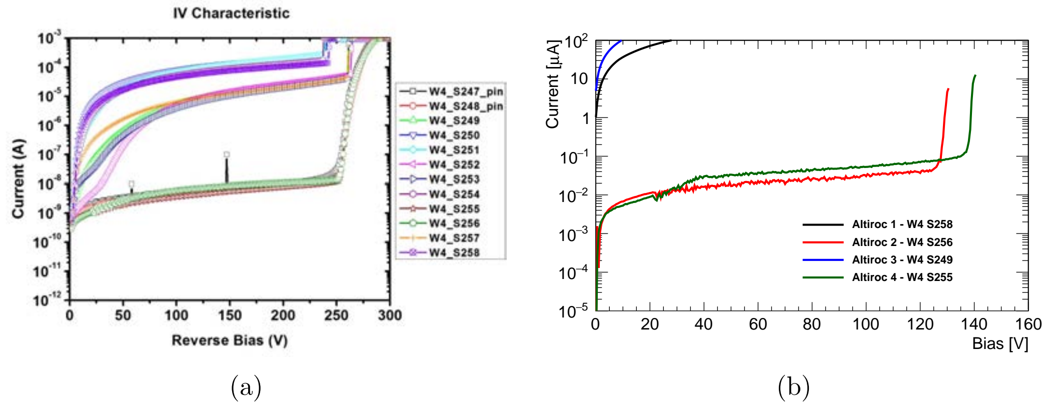
After the deposition of the UBM 80 μm diameter solder bumps are deposited with a PacTech SB^2-SM [71] solder jetting machine on the four pixel pads. Sixteen extra solder bumps are deposited along the guard ring to give stability to the assembly and provide the connection to ground to the guard ring. The flip-chipping is finally done with a SET FC150 flip chip bonder [72] and inspected with X-rays to verify the quality of the connection.

UBM has been deposited on ten LGAD and two PIN ALTIROC0_V0 compatible sensors, while only four ALTIROC0 readout boards were available. IV characterizations of the sensors were performed at different stages of the assembly process for quality control and to select the best ones to be flip-chipped. In figure 4.29a the current-voltage curve after UBM deposition measured at room temperature in a probe station is shown. In this measurement it is not possible to simultaneously connect all the pixels and the IV is measured through the guard ring. Three different families of sensors are identified, all of them with a breakdown voltage of $230 \div 250\,\mathrm{V}$, one with leakage current of the order of nA, one of the order of tens of μA and another of the orders of hundreds of μA.

Ideally the sensors with lower leakage current are selected for bump-bonding, but only two LGADs belong to the first family so that two more sensors from the other

families have been selected.

After flip-chip the IV of the bare hybrid was measured again on the probe station. This time the four pixels and the guard ring of each assembly are connected showing an increase of about an order of magnitude on all the detectors and the breakdown voltage is reduced to about 130 V, see figure 4.29b.



(a) (b)

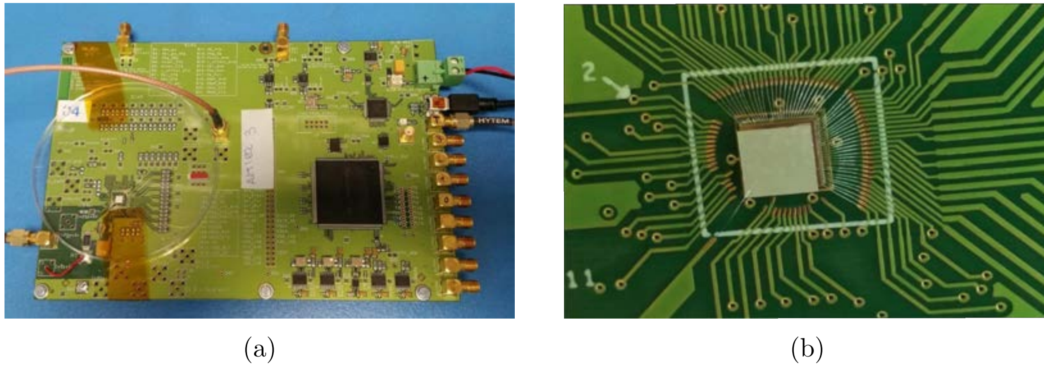
Figure 4.29: IV characteristic curves of ALTIROC0_V0 compatible sensors after UBM (a) and after bump-bonding (b). After UBM the IVs have been measured on a probe station with contacts on the backside and on the guard ring, after bump-bonding it was measured biasing the backside and grounding the four pixels through a wire-bonding pad of the chip.

The four hybrids have been mounted and wire-bonded on the readout PCB designed and provided by Omega shown in figure 4.30. After wire-bonding the IV was measured again without showing any significance difference with respect to the one measured on the bare hybrids.

The PCB was connected to a PC running a software providing communication to the chip and allowing to configure it. The ALTIROC0_V0 chip, see section 3.9.2, only contains the analog part of the electronics including a preamplifier and a discriminator with adjustable threshold. The output of the discriminator is a digital signal whose rising edge corresponds to the time of arrival of the particle and the TOT.

The ALTIROC0_V0 chip can be configured to route the output signal of the preamplifier of a readout channel, before or after discriminator, on a line connected to an SMA connector. The noise level was too high to observe the analog signal before the discrimination but the observation of the discriminator output gives information about the observed charge through the TOT.

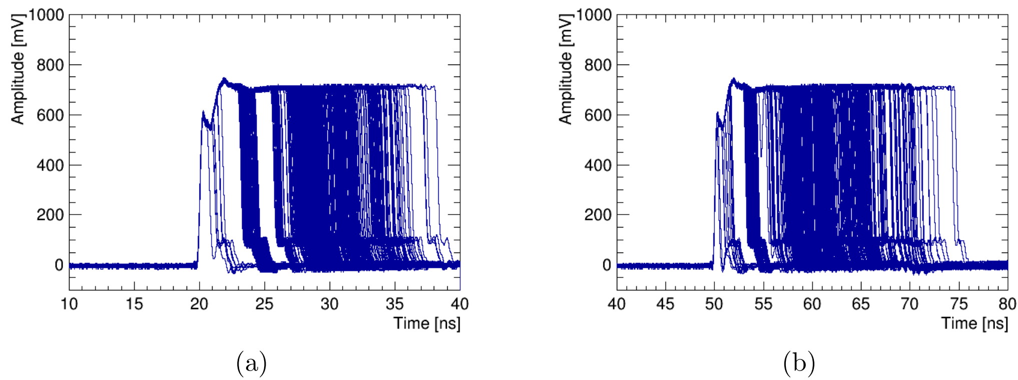
The two assemblies with larger leakage current, see figure 4.29b have not been further characterized due to the high level of the noise. It has not been possible to set a discriminator threshold value able to reject the noise without cutting out the signal.



(a) (b)

Figure 4.30: Picture of an ALTIROC0 PCB (a) and detail of the ALTIROC0_V0 wire-bond (b).

For the other two assemblies, the chip has been configured in order to see the discriminated signal induced by the exposition to ^{90}Sr beta particles. In figure 4.31 the discriminator output of the Altiroc 4 assembly is shown for two different bias voltages. The TOT distribution for different voltages is shown in figure 4.32 showing a shift to larger TOT values with larger voltages as expected from detectors with gain whose multiplication factor increases with the bias voltage.



(a) (b)

Figure 4.31: Collections of waveforms of the Altiroc 4 assembly discriminator output after the exposition to a ^{90}Sr radioactive source at two different bias voltage, 100 V (a) and 130 V (b).

More tests on the ALTIROC0_V0 assemblies have been performed by the chip designer to optimize the chip parameters, such as peramplifier gain and shaping time and the discriminator threshold DAC. In September 2017 the first beam test of the ALTIROC0_V0 prototype has been carried out at the CERN SPS beam test facility on the H6B line with 120 GeV pion beam.

The time resolution of the ALTIROC assembly has been measured comparing the time of arrival measured by the ALTIROC to the one measured by a reference SiPM

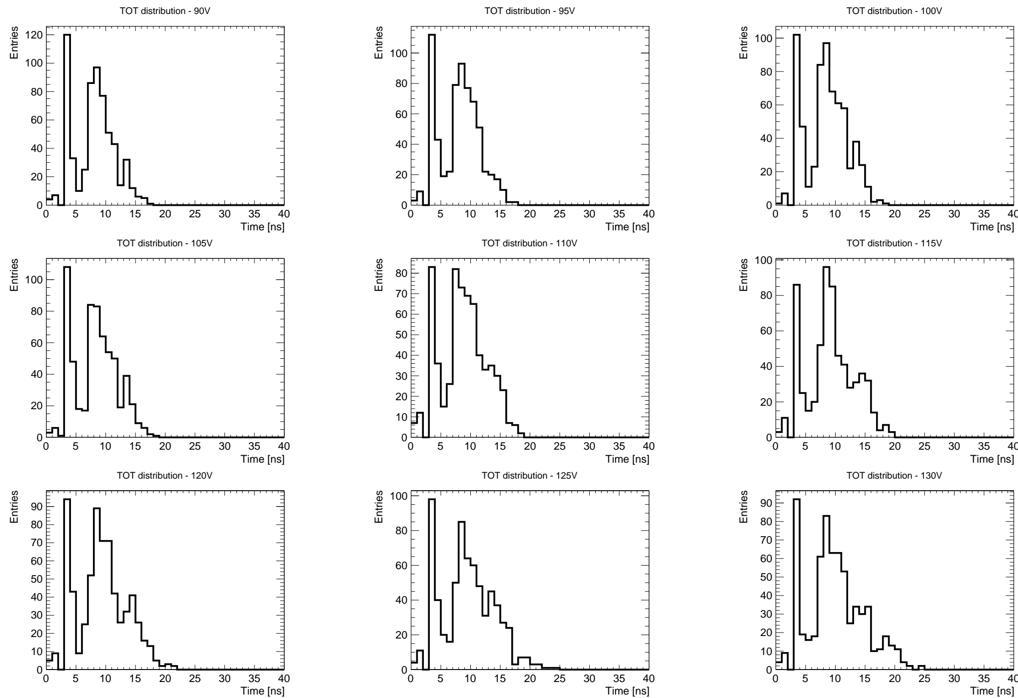


Figure 4.32: TOT distributions at different voltages of the signal induced by a ^{90}Sr source on the Altiroc 4 assembly.

showing a time resolution of 48 ps at the bias voltage of 130 V [73]. The time resolution resulted to be worse than expected, due to the underperforming preamplifier caused by a larger noise and detector capacitance than predicted. An upgraded version of the chip, the ALTIROC0_V1 has recently been delivered, including in the design modifications suggested by the tests performed on the ALTIROC0_V0, expected to improve the timing performance.

Chapter 5

Depleted CMOS Pixel Detectors

Pixel detectors for high energy physics applications have been traditionally developed as hybrid detectors where the sensor and the electronics are produced independently and then bump bonded. Hybrid detectors have the advantage that sensors and read-out chip can be developed in different technologies to optimize the device performance.

Nevertheless, monolithic devices such as Charge Coupled Devices (CCD), DEPFET and CMOS devices are already used by the high energy physics community [74]. The CCD and DEPFET devices are not radiation hard and require very specific processes that make production expensive and not suitable for large scale production. CMOS detectors are instead produced with industrial technologies making possible the production of large surfaces at reasonable cost. However, in standard CMOS technologies charge collection is driven by diffusion that is strongly suppressed after irradiation.

Recently, CMOS technologies with high resistivity substrates and with the capability of sustaining a bias voltage of the order of 100 V became available, allowing the production of depleted CMOS devices with a significant space charge region that makes these devices potentially radiation hard [75].

Depleted CMOS devices would hence allow to cover large surfaces, being cheaper and faster to produce with respect to hybrid devices, with a competitive radiation hardness. Moreover, monolithic devices can be thinned down to thickness of the order of $\sim 50\,\mu$m, allowing the use of pixel devices in environments where the material budget constraint rules out hybrid detectors [76].

Small scale depleted CMOS prototypes have been characterized over the last years [77, 78], but for usage in high energy physics experiments the feasibility of the production of depleted CMOS pixel devices with a surface of the order of cm^2 has to be proven.

In this chapter the characterization of a large scale prototype in the AMS 350 nm HV-CMOS technology, the H35Demo chip, is presented. Edge-TCT measurements on test structures have been carried out to study the evolution of the depletion depth.

While beam test measurements were carried out to understand the performance of the monolithic matrices of the chip.

5.1 The H35Demo Chip

The ATLAS community investigated the possibility of installing depleted CMOS detectors both in the inner and outer layers of the ITk pixel detector, initially considering both the monolithic and AC coupled approach. In AC coupled devices the CMOS sensor is connected to a readout chip with non-conducting glue.

The H35Demo chip [79] is a demonstrator pixel detector designed in the AMS 350 nm HV-CMOS technology [80] by the collaboration of the Kralsruhe Institute of Technology, University of Geneva, University of Liverpool and the Institut de Física d'Altes Energies of Barcelona.

The aim of this demonstrator chip is to investigate the monolithic and AC-coupled options on a large scale prototype of $18.49 \times 24.40\,\mathrm{mm}^2$ total area. The 350 nm technology is not the most radiation hard available. It was chosen to reduce the cost and eventually qualify a more radiation hard solution for the outer layers of the pixel detector.

The standard substrate resistivity of this technology is $20\,\Omega$cm while typical sensor substrate for particle detectors is of the order of the kΩcm to achieve a larger depleted volume at equal bias voltage, see section 2.1.2. Nevertheless, the H35Demo chip has been produced also on wafers with the non standard resistivities of 80, 200 and $1000\,\Omega$cm. All wafers of both standard and non-standard resistivities have a total thickness of $700\,\mu$m.

The chip consists of four different pixel matrices: two standalone matrices for monolithic readout, the nMOS and CMOS matrices, and two analog matrices for AC-coupled readout, see figure 5.1. The pixel size for all the matrices is of $50 \times 250\,\mu$m while the number of pixels is 16 rows $\times$ 300 columns for the standalone matrices and 23 rows $\times$ 300 columns for the analog ones. Two more 3×3 pixels matrices, differing in pixel sizes and in the presence of signal amplification, are present on one side of the chip as test structures. An additional test structure for capacitance measurement is present in the chip.

A total of eight different analog pixel flavors is present in the chip, each one with different characteristics in terms of in-pixel electronics. In the standalone nMOS matrix there are two pixel flavors, with half of the pixel in the matrix having time-walk compensation. The analog matrices have a total of six pixel flavors differing for the amplifiers gain, the use of linear or enclosed transistors and the presence of an extra deep *p-type* well for biasing. The CMOS matrix instead, only contain one pixel

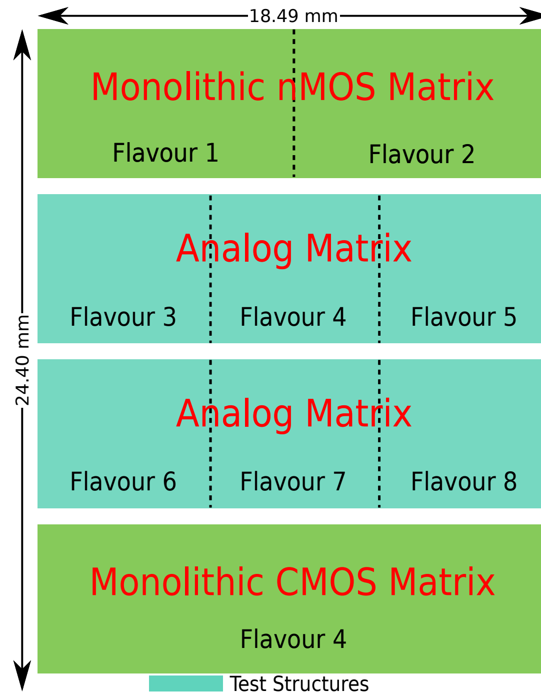


Figure 5.1: Layout of the H35Demo chip showing the four pixel matrices with the different pixel flavors and the position of the test structures.

flavor.

The sensor *pn-junction* is given by a deep *n-type* well in the *p-type* substrate. The ohmic contacts of the junction are given by the *n-type* well and by a p^+ bias ring implanted around the pixel boundaries. Applying a negative voltage to the bias ring the space charge region grows, starting from the deep *n-type* wells going firstly towards the p^+ contacts and later in the direction of the substrate depth. The charges generated inside the depleted volume drift under the effect of the electric field inducing a current pulse on the wells that act as sensing nodes for the in-pixel analog electronics.

Due to the large size of the pixel, a single well filling the whole area would return a large capacitance and hence a large noise level. To reduce the total pixel capacitance in the analog and in the standalone CMOS matrices the pixels contain three deep *n-type* wells, a central well of $30 \times 90\,\mu\text{m}^2$ hosting the electronics and two external wells of $30 \times 50\,\mu\text{m}^2$ that have the function to improve the electric field uniformity along the pixel, see figure 5.2. In the nMOS matrix in-pixel comparators, from nMOS transistors only, are used and one large *n-type* well occupies the entire pixel area to fit the more complex electronics.

In the analog part of the in-pixel electronics both nMOS and pMOS transistors are used, the nMOS transistors are located inside a *p-type* deep well inside the *n-*

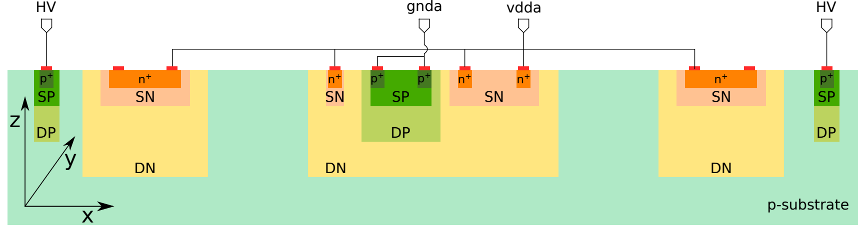


Figure 5.2: Sketch of a cross section of a pixel of the CMOS. The z direction is not in scale, the deep *n-type* wells have a depth of few μm while the total thickness of the sensor is 700 μm.

type deep well while the pMOS transistors are placed directly in the the *n-type* deep well, hence are not isolated from the collecting electrode making them sensitive to crosstalk, see figure 5.2.

Each pixel of the analog and standalone matrices has an output line connected to a $25 \times 25\,\mu\text{m}^2$ metal pad with an opening on the passivation layer for connection to the ATLAS FE-I4 [30] readout chip in order to investigate AC-coupled hybrid solutions. The connection to an external readout chip is mandatory for the analog matrices, while it is optional for the nMOS and CMOS standalone matrices.

5.1.1 Standalone nMOS Matrix

The nMOS matrix consists of 4800 pixels arranged in 16 rows and 300 columns. The readout circuit of each pixel includes an in-pixel comparator that only uses nMOS transistors. The reason behind the exclusive use of nMOS transistors is that, as mentioned above, it is not possible to isolate pMOS transistors in the AMS H35 technology. The pMOS transistors would use as bulk the same *n-type* well that acts as collecting electrode, and the voltage drop induced by the charge collection may lead to fake comparator outputs.

Two pixel flavors are present, distinguished by the different comparators that have been used. In the pixels of columns from 0 to 149 there is a simple comparator based on two fully differential Charge Sensitive Amplifiers (CSA) and an output stage, while in columns from 150 to 299 a more complex comparator with a time walk compensating circuit is implemented. Enclosed Layout Transistors (ELTs) are used in the feedback circuitry of both pixel flavors.

Each pixel has two outputs: one is a pad on the pixel for interconnection to an FE-I4 chip, the other is connected to a digital cell in the periphery. The digital block has a similar column drain readout architecture of an FE-I3 chip [29].

For each hit a time stamp, in units of 25 ns, is stored together with the pixel address until it is read out on a serial line at 320 MHz.

5.1.2 First Analog Matrix

The first analog matrix contains 23 rows $\times$ 300 columns of pixels. The CSA included in the pixels of this matrix uses a folded cascode with an nMOS transistor as input without gain boosting. This amplifier architecture has the advantage of a reduced noise level and a better radiation tolerance, the drawback is a larger power consumption.

The three pixel flavors present in this matrix differ in the transistor design in the feedback block, and in the presence of an additional deep *p-type* well for biasing implanted around each *n-type* well of the pixel. ELTs are used in the feedback circuitry of the pixels of the first 200 columns, while linear transistors are used in the remaining columns. In the first 100 columns extra biasing well are implanted.

5.1.3 Second Analog Matrix

The second analog matrix contains the same number of pixels as the first analog matrix. The pixels of this matrix use charge sensitive amplifiers with a regulated folded cascode with a pMOS transistor as input. Three pixel flavors are present, all of them using ELTs in the feedback circuitry. As in the first analog matrix, the first 100 columns have an additional *p-type* biasing well. The pixels of the first 200 columns have high gain amplifiers, while the one in the last 100 columns have amplifiers with lower gain but larger speed.

5.1.4 Standalone CMOS Matrix

The standalone CMOS matrix has 16 rows and 300 columns of pixels, all of the same flavor. The pixel electronics has the same schematic as those of the central columns of the second analog matrix, that consists in a CSA with a regulated folded cascode amplifier with a pMOS input transistor, but with a different layout. There is no in-pixel comparator, the signal is compared to a threshold in the periphery in case of monolithic readout, or in the FE-I4 readout chip in case of hybrid readout.

The digital block and testing features are analogue to the ones of the nMOS matrix with the only difference that the digital block corresponding to the second 150 columns of the matrix uses as an input stage a CMOS comparator with two thresholds for an additional time-stamp to improve the timing measurement of the hit. One of the thresholds would be used to discriminate the hit, while the other could be set just above the baseline to measure a time-stamp that is not affected by time-walk.

5.1.5 Standalone Readout

The readout of the CMOS and nMOS standalone matrices is the same. The analog output of each pixel is connected to a ReadOut Cell (ROC) in the periphery of the chip where it is compared to the threshold of a discriminator. In case the analog signal is larger than the discriminator threshold the time stamp of the hit is stored in an 8-bits RAM while the address of the pixel is stored in an 8-bits ROM.

The ROCs are arranged in two 40×60 matrices, one connected to the first 150 columns (left matrix) and the other to the last 150 columns (right matrix). Each ROC of a column is connected to a time stamp and address buses. An AND-OR priority circuit avoid conflicts that may arise by simultaneous access to the bus. The buses of each column reach an End Of Column (EOC) cell. The EOC cells are serially connected forming two 16-bits shift registers of 60 elements each. Each EOC cell sample the time stamp and address, and then passes those values to the next EOC cell.

The readout of the ROCs is continuous. Every clock cycle each of the two shift registers sends a time stamp and an address in parallel to the control unit. In the control unit the data are collected and serialized before being transmitted serially to four LVDS lines dedicated to the address and time stamp of the left and right matrices. There is no zero suppression implemented on-chip, so that every time a standalone matrix is read out, the address and time stamp contained in each EOC cell is transmitted. An empty time stamp is passed for all the pixels without a hit.

5.1.6 Test structures

On one side of the chip, close to the dicing line, there are two test structures consisting of 3×3 pixels matrices. The two test structures differ in pixel sizes and electronics content.

The first test structure contains $90 \times 190\,\mu\text{m}^2$ pixels including only a deep *n-type* well that makes the *pn-junction* with the *p-type* substrate. The signal of each pixel is connected to a fast measurement circuit with fall time lower than $\sim 1\,\text{ns}$ placed aside the pixel matrices.

The second test structure contains 3×3 pixels of $50 \times 250\,\mu\text{m}^2$ with the same wells scheme of the pixel flavors 3 and 6 present in the analog matrices, that is a central *n-type* well of $30 \times 90\,\mu\text{m}^2$ and two external *n-type* wells of $30 \times 50\,\mu\text{m}^2$ with deep *p-type* biasing implants around the pixels and between the *n-type* deep well.

The *n-type* wells of the central pixel are connected to a wire-bonding pad, the ones of the surrounding eight pixels are connected to a single wire-bonding pad sharing the readout channel. Other wire-bonding pads are present to provide bias to the test

structure and low voltage to the *n-type* wells.

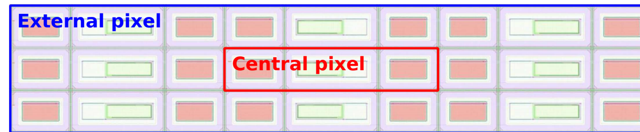


Figure 5.3: H35Demo second test structure layout with the central pixel marked in red and the external pixels in blue.

5.2 Edge-TCT Characterization of the Test Structure

The second test structure of H35Demo devices produced on wafers of different resistivities have been tested with edge-TCT to measure the depletion depth evolution with voltage and with neutron irradiation up to $2 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$.

Three sensors with different wafer resistivities have been used:

- Sensor 1 - 80 Ωcm,
- Sensor 2 - 200 Ωcm,
- Sensor 3 - 1 kΩcm.

The same devices have been measured before irradiation and during a radiation campaign where they have been irradiated with thermal neutrons at the TRIGA reactor of JSI to the cumulated fluence of 2, 5, 10 and $20 \cdot 10^{14}\,\mathrm{n_{eq}/cm^2}$. The edge-TCT measurements have been repeated after each irradiation step.

The samples have been prepared for the edge-TCT measurements by polishing the side of illumination with diamond lapping paper and diamond paste as described in section 4.2.3. A dedicated PCB has been designed to accommodate the chip and provide wire-bonding pad for bias and pixel readout. The minimal wire-bonding scheme consists of the connections for the high voltage and the readout of the central and external pixels. Initial measurements comparing the depletion depth with and without the 3.3 V low voltage bias to the *n-type* wells did not show any significant difference. After irradiation the minimal wire-bonding scheme was adopted, since repeated bonding on the same pad made wire-bonding the process difficult. The PCB has a slit to allow the laser light to reach the sensor without being shielded, see figure 5.4.

The edge-TCT measurements have been performed using infra-red light that penetrates the silicon without a relevant loss of intensity along the test structure, mimicking the ionization of a *mip*. The pulsed light is shot perpendicular to the long pixel direction of the test structure. A scan along the whole thickness of the sensor

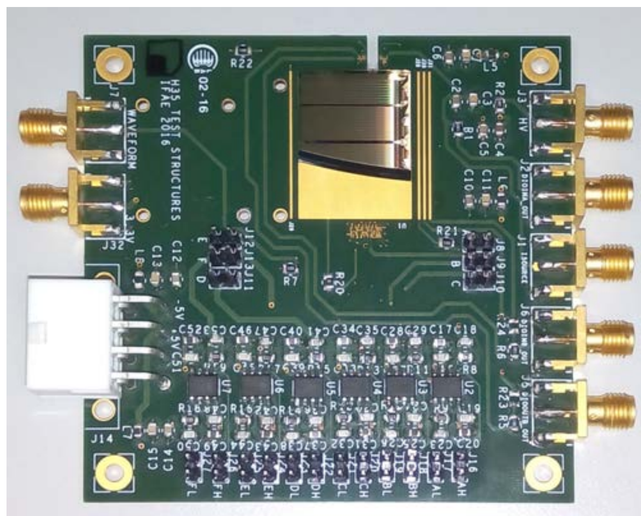


Figure 5.4: Picture of a PCB for the TCT measurements of the H35Demo test structures. Since the test structures are independent from to the rest of the chip, incomplete chips from the wafer periphery could be used, as it is the case of the 200 Ωcm sample.

hitting the center of the test structure is performed at increasing values of the bias voltage, from 0 V to the maximum applicable bias in steps of 10 V.

The laser creates electron-hole pairs along its path, during the scan these will be generated at increasing distances from the sensor surface. If this distance is lower than the depletion depth they will drift under the effect of the electric field inducing a signal on the pixels. If the charge is generated far from the surface, in the not depleted region, it will move inside the sensor bulk by diffusion. Only a fraction of it will reach the depleted volume, the remaining will eventually recombine.

In figure 5.5 the signals induced by the laser pulses at different depths on the central pixel of Sensor 2 biased at 140 V are shown. The scan covers the whole sensitive area of the sample from a starting point above the sensor's top surface, $z = 0\,\mu$m, to finish well beyond the limits of the depleted region, $z = 140\,\mu$m.

Integrating the waveforms induced by the laser pulses in a time window of 8 ns the collected charge is obtained. The charge at different depths is shown as charge collection profiles in figure 5.6. For large enough bias voltages, Sensors 1 and 2 show a plateau from the sensor surface to the end of the depletion depth, pointing out a good charge collection uniformity along the whole depleted volume. The slope of the profile edge at the top surface of the sensors is defined by the laser focus and alignment, while on the other side the laser properties are convoluted with the residual charge collection due to diffusion. The charge collection profiles of Sensor 3 show an unexpected increase of the charge collected by the central pixel until the end

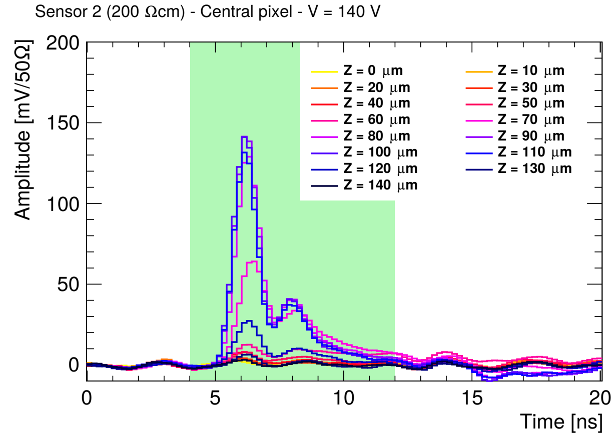


Figure 5.5: Current waveforms at different illumination depths on the 200 Ωcm sample at 140 V bias voltage. The green shadow indicates the integration range for charge computation.

of the depleted volume is reached.

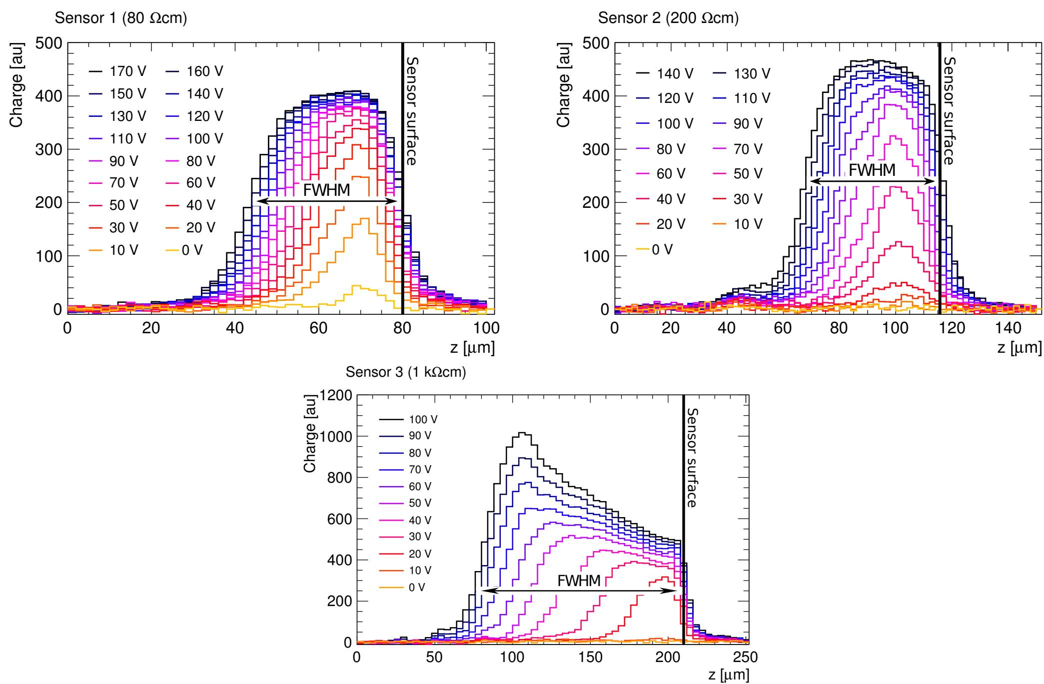


Figure 5.6: Charge collection profiles for the central pixel of the three sensors under study. The vertical lines indicate the position of the sensor top surface, the sensors extend to the left of these lines. The FWHM for the largest applied bias on each sensor is shown. Note the different scales on the plots' x-axis and the different orientation of the z-axis with respect to figure 5.5.

Two dimensional scans have been performed at selected bias voltages to verify the uniformity of charge collection along the pixel. In figure 5.7 the charge collection

maps of Sensors 1 and 3 at the bias voltage of 150 V and 100 V respectively are shown. It is visible that at large depths the central pixel of Sensor 3 collects the charge generated underneath the pixels that are in the front and in the back along the laser trajectory. The sum of the charge collected by the central and the external pixels shows a uniform response for all the measured samples.

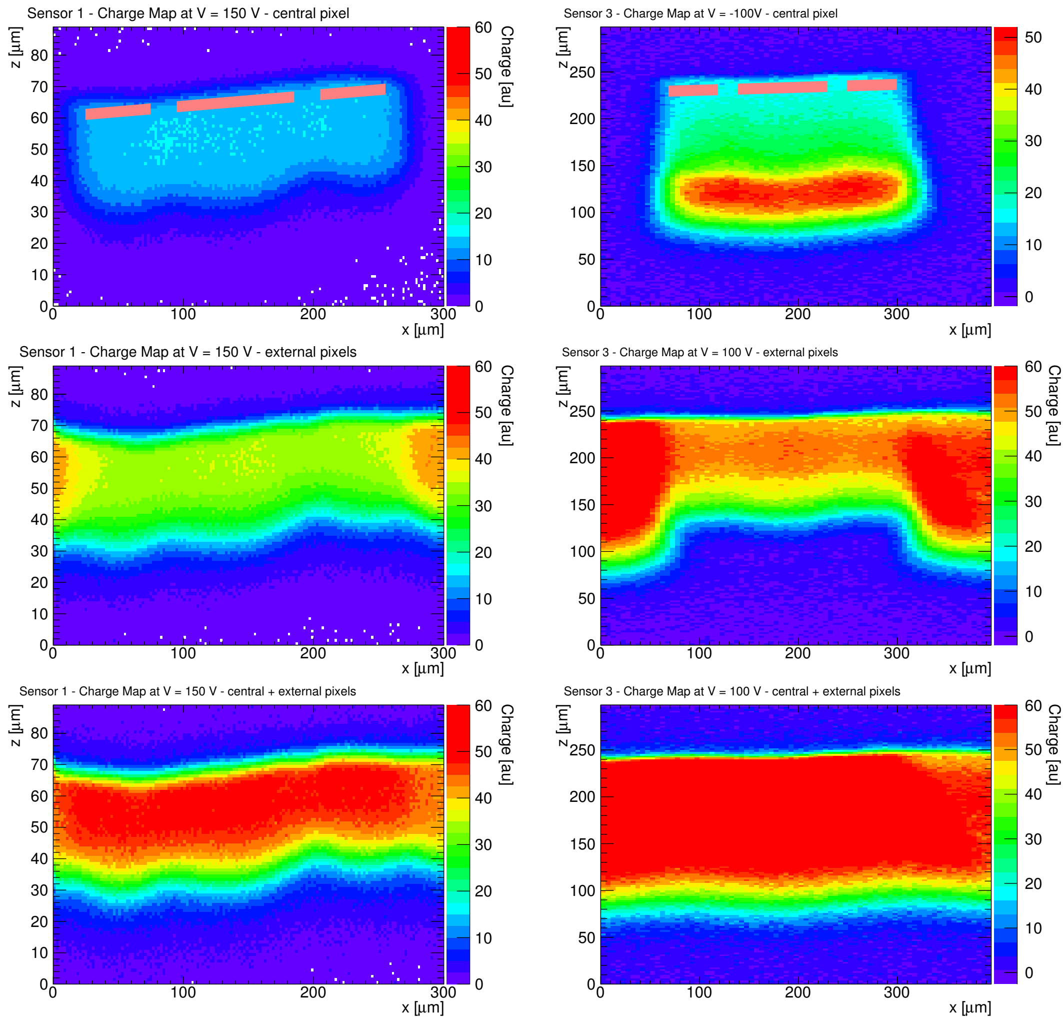


Figure 5.7: Charge collection maps for Sensor 1 (left) and Sensor 3 (right) at a bias voltage of 150 V and 100 V, respectively. From top to bottom, the charge collected by the central pixel, the external pixels and the sum of central and external pixels. The red boxes drawn in the two central pixel maps roughly indicate the position of the deep *n-type* wells.

The depletion depth is measured as the FWHM of the charge collection profiles. For Sensor 3 the half maximum at the sensor top surface side is taken as reference value for the estimation of the depletion depth, see figure 5.6.

In figure 5.8 the depletion depths at different bias voltages for the three samples

are shown. The depth of the depleted volume of a diode is related to the applied bias voltage and the substrate resistivity ρ by the equation:

$$d = d_0 + \sqrt{2\varepsilon\varepsilon_0\mu\rho V} \tag{5.1}$$

where d_0 is the effective depletion depth when no external bias is applied, $\varepsilon\varepsilon_0$ is the silicon permittivity and μ is the electron mobility. The d_0 parameter takes into account both the built-in voltage of the *pn-junction* and the finite laser size, both having positive contributions.

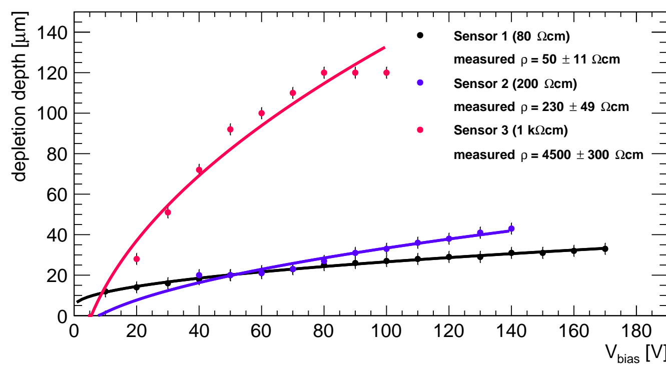


Figure 5.8: Depletion depth against bias voltage for the three samples with different bulk resistivity before irradiation.

Equation 5.1 assumes that the bias voltage is applied from the backside while in the case of the H35Demo chip it is applied from a bias ring on the top surface. Despite this approximation, the measured resistivities obtained by fitting the data in figure 5.8 agree with their nominal values for Sensor 1 and 2, where the fit returns $50 \pm 11\,\Omega$cm and $230 \pm 59\,\Omega$cm respectively. The measured resistivity of Sensor 3 is instead $4500 \pm 300\,\Omega$cm, significantly larger than the nominal one, probably originated by the large tolerance AMS accepts on the high resistivity wafers. The negative value of the d_0 parameter may be due to the fact that bias is applied from the top and the space charge volume initially grows parallel to the sensor surface.

As expected, the higher substrate resistivity results in a deeper depleted region and thus in a larger collected charge, at the same bias, for a *mip* before irradiation, although the maximum bias applicable is reduced with higher resistivities. In any case, it is critical to study the sensors performance after irradiation, see the following section.

5.2.1 Irradiation Campaign

The three sensors were removed from the PCB to be irradiated and afterwards re-mounted to measure the depletion depth after irradiation. This operation has been repeated four times to measure the depletion depth at the fluences of 2, 5, 10 and $20 \cdot 10^{14}\,\mathrm{n_{eq}/cm^2}$.

The same edge-TCT measurements as before irradiation were performed scanning along the thickness of the sensor with an infra-red pulsed laser. After irradiation sensors need to be cooled to reduce the leakage current. A Peltier element, mounted between the stages and the "T" piece that holds the sensors in a horizontal position, is used to cool down the sensor at the temperature of $-15\,°\mathrm{C}$. At the same time, dry air is flushed into the TCT box to avoid condensation of humidity on the sensor.

The results are shown in figure 5.9. Sensors 1 and 2 show an initial increase of the depleted volume depth with irradiation reaching a maximum at $10^{15}\,\mathrm{n_{eq}/cm^2}$ that decreases after exposition to a total fluence of $2 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$. On the other hand, Sensor 3 shows a reduction of the depletion depth since the first irradiation step. However a depletion depth larger than $30\,\mu\mathrm{m}$ can be achieved at any of the tested fluences on all the tested devices. After irradiation a depletion depth larger than about $50\,\mu\mathrm{m}$ can be reached.

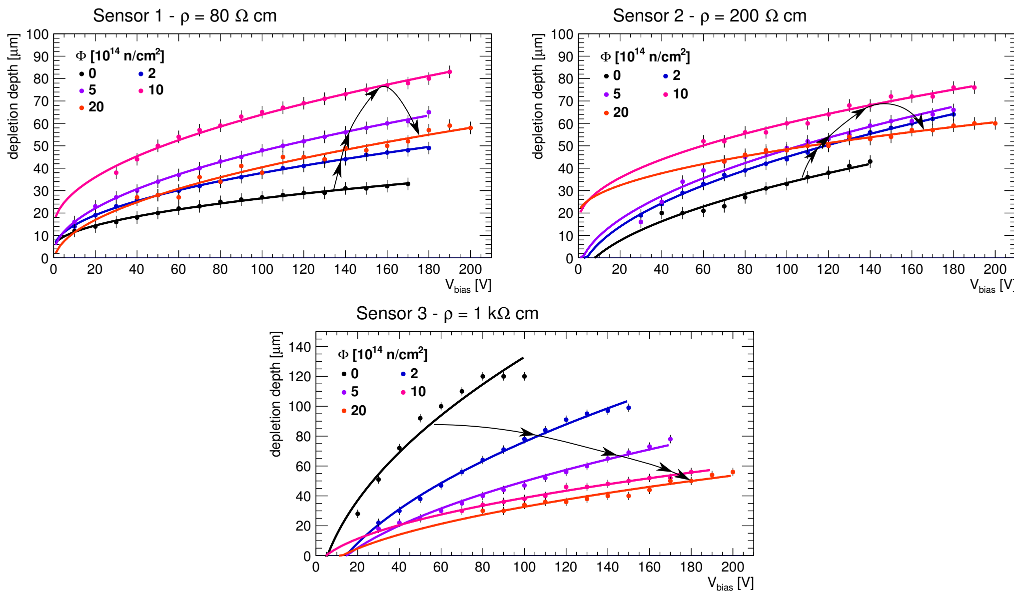


Figure 5.9: Depletion depth against bias voltage for the three samples for different fluence steps up to $2 \cdot 10^{15}\,1\,\mathrm{MeV\,n_{eq}/cm^2}$. The arrows point the consecutive fluence steps.

The effect of radiation on the depletion depth is explained by the change in the

effective substrate resistivity induced by radiation. The substrate resistivity ρ can be expressed in terms of the effective doping concentration N_{eff} by $\rho = 1/\mu e N_{eff}$, where e is the elementary electric charge. Substituting ρ, equation 5.1 becomes:

$$d = d_0 + \sqrt{\frac{2\varepsilon\varepsilon_0}{eN_{eff}}V} \tag{5.2}$$

showing how the evolution of N_{eff} with fluence will determine the evolution of the depletion depth.

The relation between the effective doping concentration and the 1 MeV neutron equivalent irradiation fluence is described by [13]

$$N_{eff}(\Phi) = N_{eff,0} - N_c\left(1 - e^{-c\Phi_{eq}}\right) + g_c\Phi_{eq}, \tag{5.3}$$

where $N_{eff,0}$ is the initial doping concentration, N_c and c describe the size and speed of the acceptor removal effect, effectively reducing the *p-type* dopant concentration, and g_c describes the radiation induced acceptor introduction, as previously discussed in section 2.2.4.

Fitting the depletion depth measurements against the applied bias voltage with equation 5.2 the value of N_{eff} can be extracted for each sensor and fluence. Equation 5.3 can than be used to fit the evolution of N_{eff} with fluence leaving N_c, c and g_c as free parameters, see figure 5.10 and table 5.1.

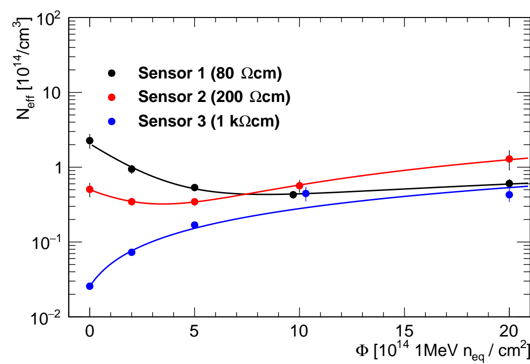


Figure 5.10: Measured effective dopant concentration on the samples under study at each of the tested fluences. The points at $10 \cdot 10^{14}$ 1 MeV n_{eq}/cm^2 of sensors 1 and 3 have been slightly shifted horizontally for better visibility.

Due to the low value of the initial doping concentration $N_{eff,0}$ in Sensor 3, the acceptor removal term is negligible for the fluence range studied, while for Sensors 1 and 2 it dominates until a fluence of about 10^{15} n_{eq}/cm^2.

The parameters of the fit of equation 5.3 shown in table 5.1 match with previ-

	Sensor 1	Sensor 2	Sensor 3
$N_c\,[10^{14}/\mathrm{cm}^3]$	1.8 ± 0.4	0.7 ± 0.5	–
$c\,[10^{14}\,\mathrm{cm}^2]$	0.5 ± 0.2	0.3 ± 0.3	–
$g_c\,[1/\mathrm{cm}]$	0.02 ± 0.01	0.07 ± 0.04	0.03 ± 0.02

Table 5.1: Fitted values of equation 5.3 parameters.

ous measurements on devices of 10, 20, 100 and 2000 Ωcm obtained with the edge-TCT technique at JSI [16, 81]. The measured sensors discussed in these publications come from different productions: the 10 and 20 Ωcm samples have been produced the CHESS-1 and HV2FEI4 chips in the AMS H35 and AMS H18 (180 nm) respectively [82]. The other samples are from different foundries and technologies. The X-Fab HV-SOI 180 nm for the 100 Ωcm sample [83] and the LFoundry HV 150 nm for the 2 kΩcm one [84].

The measurements carried out during the irradiation campaign show that the space charge region of sensors with substrate resistivity of 80 and 200 Ωcm increases with irradiation up to a fluence of $10^{15}\,\mathrm{n_{eq}/cm^2}$ and decreases at larger fluences. For these devices the maximum achievable depletion depth at any fluence, up to a maximum of $2 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$ is always larger than the one obtained before irradiation. The sensor with a substrate resistivity of 1 kΩcm shows instead a notable reduction of the space charge region since the first irradiation step at $2 \cdot 10^{14}\,\mathrm{n_{eq}/cm^2}$.

Nevertheless, it is possible to achieve a depletion depth larger than 30 μm on all the tested devices at any of the tested fluences. This means that only the charge generated by a *mip* inside this volume will contribute to the signal. The gain and threshold of the pixels amplifiers and discriminators will have to be tuned accordingly.

The results of this study point to a different choice of wafer resistivity for different radiation hardness requirements. The high resistivity sample showed a larger depletion depth at fluence lower than $2 \cdot 10^{14}\,\mathrm{n_{eq}/cm^2}$ with respect to the other two samples that, on the other hand showed a lower variability over the full fluence spectrum up to $2 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$ that imply a smaller fluctuation of the input signal to the in-pixel amplifiers over the lifetime of the experiment.

It is important to point out that for this study all the irradiations have been performed with neutrons and the behaviour after exposition to charged hadron should be studied as well.

5.3 Beam Test Characterization of the CMOS matrix

The monolithic matrices of the chip have been characterized with beam tests to study their detection capability of minimum ionizing particles. In this thesis only

the characterization of the CMOS matrix of non irradiated devices with different substrate resistivity is presented. However, a study performed by IFAE at beam tests of devices with 200 Ωcm substrate resistivity irradiated with neutron and proton is going to be published in a short time [85].

5.3.1 Readout System

A dedicated Data Acquisition system (DAQ) has been developed at IFAE to configure and readout the CMOS and nMOS monolithic matrices. The DAQ system, shown in figure 5.11, is based on a Xilinx ZC706 FPGA development board [86] and a custom designed carrier board that hosts the chip, called Standalone PCB.

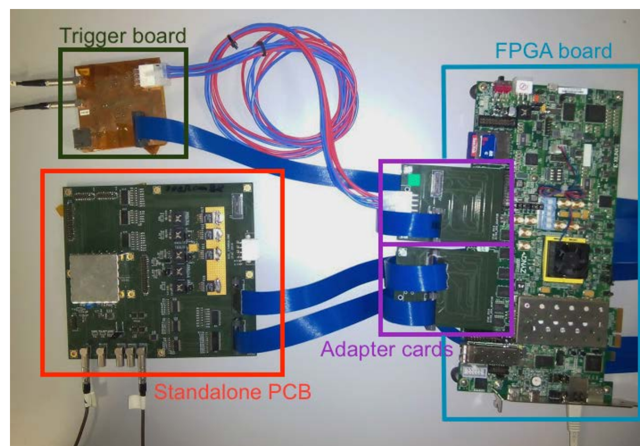


Figure 5.11: The readout system for configuration and readout of the H35Demo chip monolithic matrices developed at IFAE.

The Standalone PCB includes low voltage regulators to provide low voltage bias to the matrices of the chip and Linear Variable Differential Transformers (LVDTs) for communication. A number of connectors are present on each board to provide bias, input and output of test signals and communication line for commands and data.

In a first version of the Standalone PCB only the nMOS and CMOS monolithic matrices where connected. On the chip, the bias grid covers the four matrices providing bias also to the analog matrices that were not properly grounded. The leakage current of the sensor was observed to be of the order of milliamperes due to floating potentials in the analog matrices. A second version of the Standalone PCB has been produced to provide a proper electrical connection to all the matrices of the chip with the effect of reducing the leakage current of about three orders of magnitude.

A trigger board has been developed to add external trigger capability to the system, that is needed to integrate the H35Demo chip readout with the system of the particle tracking telescopes used in beam test measurements. The board allows

to take synchronized data with other readout systems in a trigger-busy scheme. A busy signal is raised by the H35Demo DAQ system after receiving a trigger and is released when all the H35Demo data are read out and the system is ready to receive a new trigger. While the busy signal is high the external readout system is inhibited to issue new triggers keeping the data of both system synchronized.

The readout hardware is completed by a pair of adapter cards that allow to connect the Xilinx board to the trigger board and the Standalone PCB.

A specific firmware has been developed for the FPGA board used in the DAQ system to program the shift registers of all the four matrices of the H35Demo chip independently and readout one of the monolithic matrix at the time. The readout could be selected between continuous and triggered acquisition mode. In the triggered mode the trigger delay, the event block and the dead time can be adjusted to define the time window to be readout. For a more efficient data transmission, zero suppression and Direct Memory Access (DMA) have been implemented in the firmware.

A control software written in C++ with a graphical interface developed in QT is used to steer and synchronize the operation of the FPGA board, external power supplies and a pulse generator for debugging, tuning and data taking. A screenshot of the software is shown in figure 5.12.

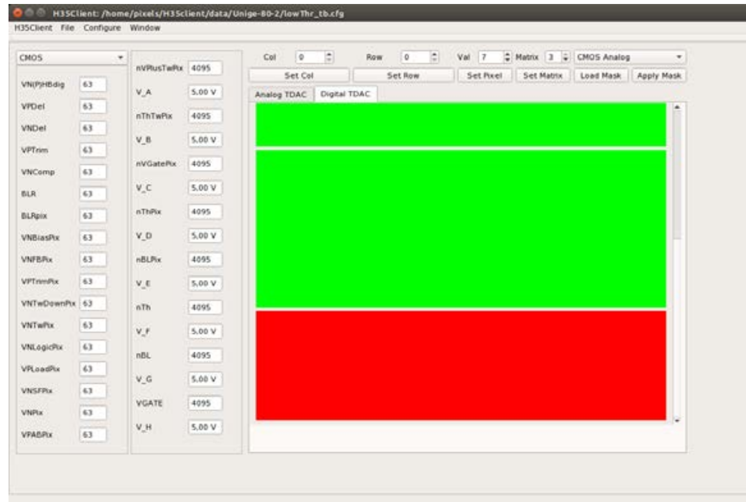


Figure 5.12: Screenshot of the H35Demo steering software showing the global DAC values of a CMOS matrix.

The communication between the different elements is performed using a TCP/IP protocol with the server running on the integrated operative system of the Xilinx board. Examples of the readout operation are shown in figure 5.13. An analog scan (a), that consists in the repeated injection of a test pulse in the discriminator input of each pixel of the matrix to test the response uniformity, and the hit map (b) after

exposition to a ^{90}Sr radioactive source of the CMOS matrix are shown.

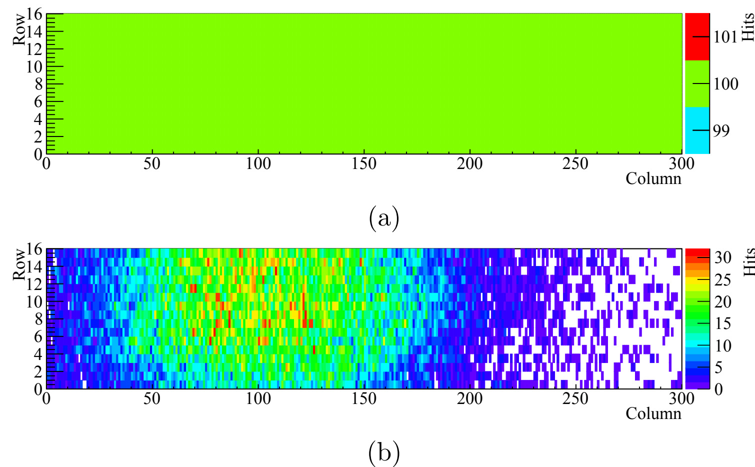


Figure 5.13: Response of the CMOS monolithic matrix to 100 test pulse injections in each pixel (a) and to ^{90}Sr electrons (b).

5.3.2 Threshold Tuning

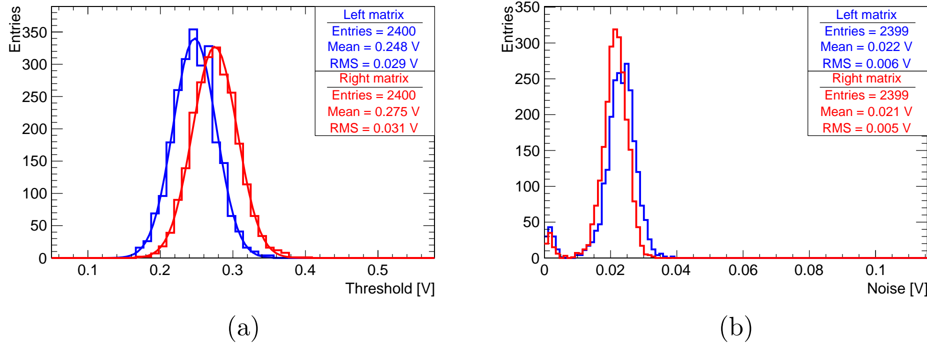
The signal shape and the threshold of the CMOS matrix can be adjusted through the regulation of dedicated Digital to Analog Converters (DACs) acting on the amplifier and discriminator circuits. The signal height is regulated through the feedback current of the in-pixel preamplifier (VNFBPIx) and the gain of the preamplifier that is regulated by the difference between nBLPix and ThPix. A global threshold (Th) is set for the whole matrix and a trim register can be used to adjust the threshold value for each pixel.

As described in section 5.1.4, two independent digital blocks are present dividing the matrix readout in two sub-matrices, hereafter labelled as left and right. Two global parameters are used to enable the in-pixel threshold trimming. The measurements described in this thesis have been performed using the default value for these bits in the configuration register, so that in-pixel trim registers were enabled only in the right matrix. However, the dynamic range of the trim registers resulted to be very limited not allowing a proper pixel-by-pixel threshold tuning. In addition, the minimum value of the trim register is non null, causing a shift to larger values of the left matrix average threshold, see figure 5.14.

Since in the left part of the CMOS matrix it is possible to achieve, on average, lower threshold values than in the right part, the tuning strategy used in this work aims at optimizing the global parameter in order to achieve the lowest possible threshold on the left side of the CMOS matrix. The difference in the left and right threshold distributions can be used to measure the chip performance at two different threshold

values simultaneously.

The threshold of each pixel is verified with the injection of test pulses of different amplitudes and then fitting the turn-on curve with an error function (S-function). The abscissa of half-height defines the threshold value and the width gives the noise level. An example of the threshold tuning verification on a device with substrate resistivity of 200 Ωcm is shown in figure 5.14.



(a) (b)

Figure 5.14: Threshold (a) and noise (b) distribution of the pixels of a CMOS matrix with substrate resistivity equal to 200 Ωcm.

The threshold and noise mean and RMS of the CMOS matrix of the tested devices is shown in table 5.2. The lowest threshold was reached on the 200 Ωcm sample with a value of 1300 e^-. The larger threshold of the 20 and 80 Ωcm samples is due to some pixels with a larger noise value with respect to the core of the distribution. Since the H35Demo chip does not allow to mask noisy pixels a larger threshold has to be set to avoid noise induced hits.

	Left Matrix				Right Matrix			
Resistivity	Threshold		Noise		Threshold		Noise	
[Ωcm]	Mean [e^-]	RMS [e^-]	Mean [e^-]	RMS [e^-]	Mean [e^-]	RMS [e^-]	Mean [e^-]	RMS [e^-]
20	1600	140	90	40	1700	140	80	40
80	1560	150	110	25	1800	180	104	20
200	1300	150	120	30	1500	160	110	25

Table 5.2: Threshold and noise distribution parameters of the tested H35Demo devices after tuning.

5.3.3 Beam Test Results

The CMOS monolithic matrix of the H35Demo chip has been tested at the Fermilab MTEST facility with 120 GeV protons. The UniGe FE-I4 telescope [87] was used as reference to measure the particles trajectories. The telescope is based on six ATLAS FE-I4 planar pixel sensors from the IBL production arranged in two arms.

The modules are rotated to achieve a resolution of about 10 μm on both directions perpendicular to the beam and are read out by the RCE data acquisition system [88].

The telescope issues a trigger when the first and the last telescope planes have simultaneous hits. After the trigger is issued the six telescope planes are integrated in a time window of 400 ns equivalent to 16 LHC clock cycles. In the H35 readout system the data contained in a time window of about 10μs is stored. A large time window is needed to readout the full event of the H35Demo chip since the output of all the pixels of the matrix is transmitted and on-chip zero suppression is not implemented. To synchronize the data of the two readout systems the trigger-busy scheme described in section 5.3.1 is used.

During the beam tests the H35Demo chips were sequentially tested in the telescope set-up as DUTs with the beam impinging at perpendicular incidence on the sensor surface. The sensors were operated at room temperature with a fan blowing on the backside of the Standalone PCB for active heat removal. The chips where tuned to the threshold values shown in table 5.2 and synchronous data of the FEI4 telescope and the H35Demo chip were stored. Different datasets have been taken for different bias voltages of the DUTs.

For each event, adjacent hits are clustered and considered as a single detection of the particle position. Since the H35Demo chip does not provide information about the charge deposited in each pixel, the average position of the clustered hits is taken as position of each cluster. The cluster size distributions were studied for all the devices. Since the particles of the beam cross the sensor perpendicularly, a cluster larger than one is expected only when they hit the pixels boundaries and charge sharing among neighbour pixels occurs. The fraction of events with cluster size equal to two is about $8 \div 9\%$ for the 80 and 200 Ωcm samples while it is around 15% for the 20 Ωcm, see figure 5.15.

The hit efficiency of each sensor was measured comparing the number of tracks reconstructed by the telescope to the number of tracks with an associated hit, or cluster, in the sensor. The hit to be matched is searched around the point obtained interpolating the telescope reference track at the DUT plane position. The efficiency is measured as a function of the bias voltage for all the devices and it is shown in figure 5.16.

The two higher resistivity sensors achieve an efficiency larger than 99% at bias voltage as low as 50 V, the lowest measured bias. It is instead necessary to apply a bias voltage of 160 V to the 20 Ωcm sample in order to obtain the same efficiency. This is explained with the lower resistivity that has to be compensated with a larger bias to achieve a large enough depletion depth. This was shown in equation 5.1, the depletion depth is proportional to the square root of the resistivity times the bias

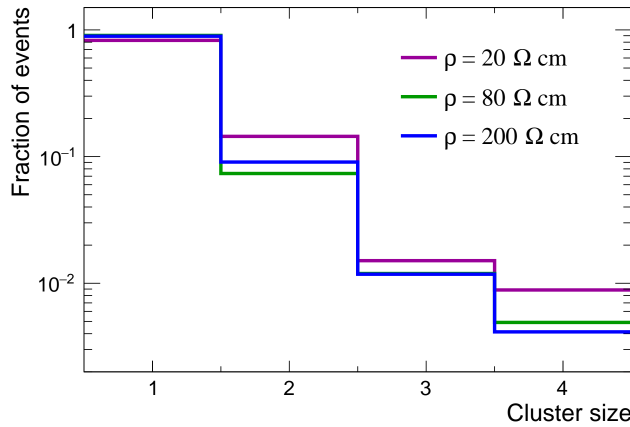


Figure 5.15: Cluster size distribution of H35Demo chip on different substrate resistivity measured with the Fermilab MTEST proton beam at perpendicular incidence.

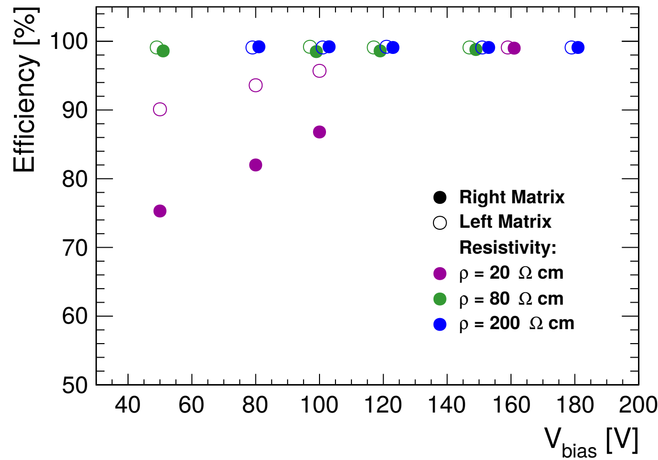


Figure 5.16: Hit detection efficiency of the CMOS matrix as a function of the bias voltage for different substrate resistivity. Some points are shifted horizontally for a better visualization, the applied bias is a multiple of 10 V.

voltage.

The different thresholds play a role as well, as it results evident by the different efficiency of the left and right halves of the CMOS matrix on the 20 Ωcm sample. Increasing the bias voltage the efficiency increases and the difference between the left and right matrices is reduced since the Landau-shaped signal distribution shifts to larger values while the threshold remains fixed.

For all the tested devices the efficiency is uniform over the whole matrix with the exception of the pixels of the top row as shown in figure 5.17 for one of the DUTs. The top row is the one close to the second analog matrix that may introduce noise. In fact, a larger threshold and noise is usually observed on these pixels making them slightly less efficient. The empty bins on the left side of the matrix are an artefact

due to the acceptance of the telescope.

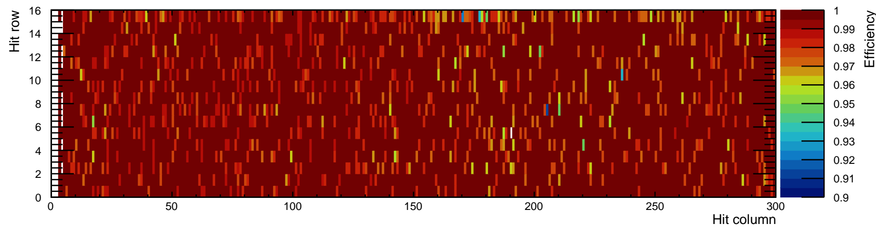


Figure 5.17: Efficiency map of the CMOS matrix of the 200 Ωcm sample at a bias of 180 V.

The beam test characterization of non irradiated H35Demo chip showed that the three tested substrate resistivity can achieve 99% efficiency within the voltage capability of the sensors before irradiation.

The 80 and 200 Ωcm samples reach full efficiency at the lowest measured bias voltage, that are 50 V and 80 V respectively. At these voltages the depletion depth measured with edge-TCT on test structures is about 20 μm for the 80 Ωcm samples, and 30 μm for the 200 Ωcm one. For the 20 Ωcm sample a larger bias is needed to compensate the initially lower depletion depth.

Characterization of proton and neutron irradiated samples from a 200 Ωcm wafer have been performed by IFAE. The study, in preparation for publication, highlights that after irradiation several issues arises but a hit efficiency of 99% is eventually found on sensors irradiated with neutrons to the fluence of $10^{15}\,\mathrm{n_{eq}/cm^2}$ at a bias of 150 V and an efficiency larger than 98% is found for proton irradiated sensors to the same fluence.

Conclusions and Outlook

In this thesis the research and development of Low Gain Avalanche Detectors (LGAD) and High Voltage CMOS (HV-CMOS) devices have been presented.

The LGAD technology has been initially developed by the Centre Nacional de Microelectrònica (CNM) for radiation hard tracking devices. The technology consists in the implantation of an highly doped *p-type* multiplication layer underneath the *n-type* electrode on a *p-type* substrate. Measurements of the first prototypes of highly segmented LGAD devices, with readout electrodes on the *n-type* side, did not show the expected charge multiplication. The small pitch of strip and pixel detectors, needed for a good position resolution, does not allow the implantation of the JTE that improves the electric field confinement and uniformity avoiding edge effects. Thus, the LGAD technology for tracking has been modified to the so called inverse LGAD, not discussed in this thesis. Inverse LGAD devices have the segmentation and the charge multiplication layer on the opposite electrodes with the segmented electrodes on the *p-type* side. The avalanche mechanism therefore takes place on a diode-like structure with a simpler geometry, avoiding the limitations introduced by segmentation [89]. However, the radiation hardness implications of this approach will have to be understood.

Thin detectors with built-in multiplication are expected to have a good time resolution, and LGAD devices produced on wafers with a $50\,\mu$m thick active layer showed a time resolution of about 30 ps with a gain of 30. This is the target resolution of the High Granularity Timing Detector (HGTD) that adopted the LGAD technology as baseline for their detectors. Dedicated productions to optimize the LGAD technology for timing measurements in a radiation harsh environment have been done by CNM and by two others manufacturers, the Fondazione Bruno Kessler (FBK) and Hamamatsu Photonics (HPK).

The measurements presented in this thesis show a strong suppression of the gain for fluences larger than about $10^{15}\,\mathrm{n_{eq}/cm^2}$. The analysis also showed a strong correlation between gain and time resolution with difference devices, differing in fluence and doping concentration, following an universal trend. A better voltage stability is required to apply a larger bias after irradiation in order to recover the gain, and as a

consequence the timing performance.

Detectors with modified charge multiplication implants have been tested in this thesis, replacing the boron multiplication layer with a gallium one and comparing standard and carbon enriched wafers. The boron based multiplication layer in carbon enriched wafers resulted to slightly better retain after irradiation to $6 \cdot 10^{14}\,\mathrm{n_{eq}/cm^2}$, but at larger fluence no significant improvement was shown, and the voltage capability of these devices showed to be the limiting factor for reaching the target time resolution after irradiation.

Recent time measurements on LGAD devices produced by HPK on wafers with 50 and $35\,\mu$m active thickness showed a time resolution of the order of 50 ps after neutron irradiation to a fluence of $6 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$ in a laboratory set-up using β electrons from a ^{90}Sr source [90]. However, successive measurements of the time resolution of CNM and HPK devices, after irradiation to $3 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$, in beam tests showed a similar performance for both technologies [91], compatible with the results first presented in reference [92] and part of this thesis. The latest beam test results show that $50\,\mu$m thick LGAD devices have a timing resolution of about 60 ps after irradiation to $3.5 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$. If these results are confirmed, the HGTD time resolution would be degraded to about 34 ps in the most exposed regions, slightly worse than the design requirement of 30 ps. The effect on the HGTD performance has not been evaluated yet.

The CMOS technology was originally developed for the electronics industry. It is widely used for the construction of integrated circuits and has applications from microprocessors to imaging sensors. The standard CMOS technology only allowed the use of bias voltages of a few volts, making it of little interest for the high energy physics community where higher voltages are needed to create a large enough depletion depth, especially after irradiation when charge collection by diffusion is not possible.

Recently, many producers allowed to apply bias voltages of about 100 V in the so called HV-CMOS processes. This gave the opportunity to produce active pixel sensors, where the analog electronics is contained in the pixel and with a space charge region of considerable size. Some foundries allow to fit more complex electronics within the pixel, otherwise placed in the periphery of the sensor, for the production of depleted CMOS monolithic detectors. With this kind of detectors the hybridization of sensors and readout chips is avoided, reducing cost and production time. Therefore the coverage of larger surfaces with HV-CMOS monolithic detectors is more easily achievable.

In the ATLAS framework, the depleted CMOS detectors are being considered as a drop-in solution for the outermost layer of the Inner Tracker (ITk) pixel detector. In this thesis the characterization of a large scale prototype produced in the AMS

H35 technology, the H35Demo chip, has been presented.

The evolution of the depletion depth with irradiation has been studied with edge-TCT on samples with different substrate resistivities. Beam tests have been performed on one of the monolithic matrices of the chip. An efficiency of 99% has been measured on samples with wafer resistivity of 20, 80 and 200 Ωcm before irradiation. Although this technology is not considered radiation hard the chip showed good performances after irradiation with protons and neutrons to $10^{15}\,n_{eq}/cm^2$ [85] (not discussed in this thesis), reaching an efficiency larger than 98%.

These are very promising results that will have to be reproduced on a chip with the same characteristics of the RD53 chip (in terms of pixel size, power consumption and readout scheme) to be qualified for ITk.

The next full size HV-CMOS prototype was planned to be submitted in the AMS 180 nm technology (H18). Unfortunately, the AMS foundry stopped the H18 production line but other producers are available. The AMS H18 processes is based on a IBM technology that is used also by other foundries and the production of a chip in the HV-CMOS 180 nm technology has been already submitted to TSI semiconductor [93].

In summary, significant progress has been made in this thesis on two novel silicon sensor technologies to face the new challenges of the HL-LHC era. The first studies of LGAD sensor before and after irradiation have been presented, and the characterization of the first full size HV-CMOS monolithic prototype has been carried out. Both technologies are likely to be installed in the ATLAS upgrade for the HL-LHC.

More monolithic HV-CMOS prototypes are going to be submitted in the near future to qualify this technology for the outermost layer of ITk. The qualification process is expected to last about a year, after which a decision will be taken by the ATLAS collaboration.

The LGAD technology has been adopted as the baseline for the HGTD sensors. Whose approval by the ATLAS collaboration has been largely based on the LGAD sensor studied in this thesis and whose performance are shown in [92]. New LGAD productions are going to be delivered before the end of 2018. They features larger arrays, 5×5 and 15×15, to test the yield on full-size sensors and test structures with technology variations to reduce the inter-pixel gap and improve the voltage capability.

Appendices

Appendix A

Transient Current Technique

In the high energy physics community sensors characterization is usually performed using radioactive sources and test beams. Radioactive sources have the advantage that can be used in table-top set-ups, but the low energy radiation is emitted in a large solid angle and, even if collimated, do not provide good position resolution. The latter, combined with a pointing telescope, provides tracking information of *mips* with good position resolution. The drawback is that test beams are only available in a limited number of facilities and usually for a short period of time.

The Transient Current Technique (TCT) consists in the measurement of time-resolved current waveforms induced by the drift charges inside a sensor. The current is proportional to the number of charges, their drift velocity and the weighting field of the readout electrode obeying the Shockley-Ramo theorem, see equation 2.17. Different detector properties can be extracted by the analysis of the waveforms. For example, the waveform integral returns the collected charge.

The TCT gives the opportunity to perform measurements with good position resolution ($\lesssim 10\,\mu$m) on a table-top set-up. In a TCT set-up the signal is generated by low energy photons that, contrary to charged particles, do not ionize along their path but penetrate the sensor until they are eventually absorbed with a probability that depends on the detector material and on the photon wavelength, see section 2.2.2. To mimic the behaviour of charged particles a pulsed laser source is used to illuminate the sensor with a large number of photons in a short time interval.

In this section the scanning TCT set-up from Particulars [65] available at the IFAE Pixel group laboratory, shown in figure A.1, is described.

The minimal TCT set-up consists of a laser source, an optical system to focus the laser beam, a current amplifier and a waveform digitizer. The light produced by the laser source is focused on the sensor active region where it generates free electron hole pairs. The free charge produced in the depleted volume drifts inducing a current pulse that is amplified and digitized.

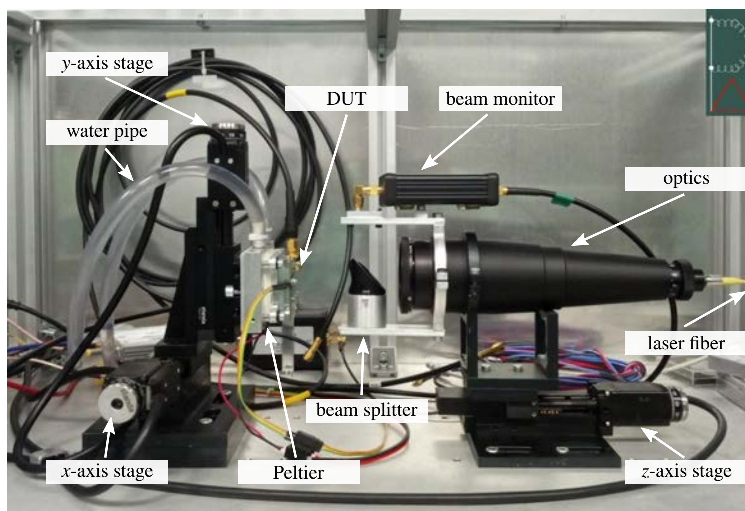


Figure A.1: Transient current technique set-up at IFAE.

The IFAE TCT set-up also has a set of movable stages that allows to move the sensor on the plane perpendicular to the laser beam and to move the optical system along the beam axis. A Peltier element and controller is used to regulate the operational temperature of the DUT. A dry air filter is included to keep moisture under control and avoid condensation when the DUT is operated at low temperature. Finally, a beam monitor system verifies the beam stability during long lasting measurements.

Laser Sources

Two different laser sources are available at IFAE. An infra-red source with a wavelength of 1064 nm and a red one with a wavelength of 660 nm. The absorption depth, that is the distance after which the number of photons is reduced by a factor $1/e$, in silicon is about 1 mm for the infra-red light and about $3\,\mu$m for red light [94].

The red laser creates electron hole pairs only on the proximity of the surface behaving as an α-particle that is immediately stopped. On the other hand, the infra-red laser can be compared to a *mip*. Since the typical thickness of the silicon detectors used as DUT is between 50 and $300\,\mu$m, the intensity drop within the detector can be neglected, being the ionization uniform along the full thickness.

The duration and repetition rate of the laser pulses can be adjusted through a control software. The duration is set to the minimum achievable value of 500 ps while the repetition rate is usually set to 100 Hz. The source is coupled with an optical fiber that is plugged into an optical system providing a beam spot of $8 \div 10\,\mu$m. The laser sources also provide an electric signal synchronous to the laser pulse to trigger the readout system.

Amplifiers

Two pairs of broadband current amplifiers optimized for TCT measurements are available at IFAE. A pair of Particulars AM-02 amplifiers [65] with a gain of 53 dB and a bandwidth of 2 GHz with a low band cutoff frequency of 10 kHz and a pair of CIVIDEC C2-TCT amplifiers [64] operating in the same frequency band with a gain of 40 dB. The current input/output ratio can be obtained through the formula $G_{db} = 20 \log_{10} (I_{Out}/I_{In})$, resulting in an amplification factor of 100 for the CIVIDEC amplifiers and about 450 for the Particulars ones. Usually, the CIVIDEC amplifiers are preferred because of the lower noise.

TCT Readout

After being amplified the signals are digitized to be stored in the DAQ PC. The digitizer used is a DRS4 Evaluation Board [95] with 700 MHz analog bandwidth, a sampling rate of 5 GSPS for a 200 ns sampling depth. It has four input channels, one of them being used for triggering.

Movable Stages

Three single axis Standa motorized translational stages [96] allow to remotely control the DUT and the focus position. The focusing lens system is mounted on one of the stages. With the stage moving axis aligned with the laser beam direction in order to move forward or backward the focus position. The other two stages are mounted orthogonally to each other and to the beam axis. They hold the mounting plate that hosts the DUT and the Peltier element.

The stages have a position resolution better than 1 μm so that the pointing resolution of the TCT set-up is given by the laser spot.

Cooling System

As previously mentioned the DUT can be cooled through a Peltier element placed on the back side of the mounting plate. It has a cooling power of 40 W, able to cool down to a temperature about 40°C lower than the ambient. To operate the sensors at low temperature dry air is flushed into the TCT box to ensure the dew point temperature is lower than the coldest part of the set-up. The cooling system is completed by a circulating water chiller used to cool down the warm side of the Peltier element.

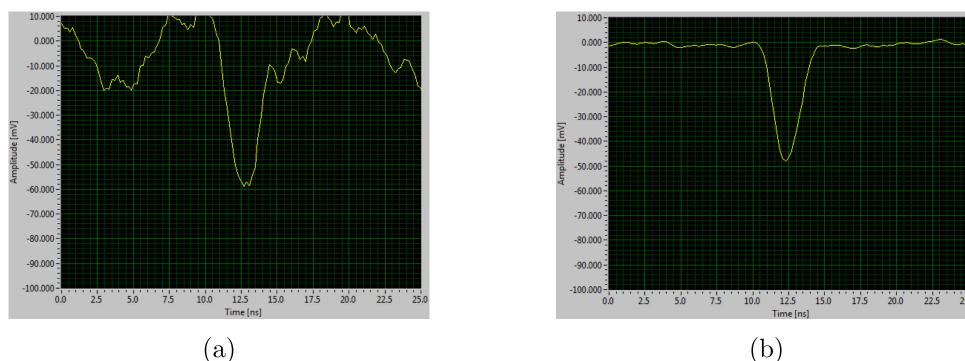
Data Acquisition System

The Particulars scanning TCT is provided of two LabView software programs that allow to control the different components of the set-up and store the digitized data.

A laser controller is dedicated to the control of the laser source, switching it on and off, and adjusting the laser properties, such as beam intensity, pulse duration and repetition rate. The DAQ software is used to control the other elements of the set-up: the three movable stages, the waveform digitizer and up to two power supplies. The only component that is not remotely controlled is the Peltier element that has to be set manually.

The DAQ system can control different models of movable stages, waveform digitizers and power supplies. In the IFAE TCT set-up these are the Standa stages and DRS4 evaluation board mentioned above and a Keithley 2100 high voltage power supply [56].

The signal over noise ratio is usually low and an average of about 100 waveforms is performed to suppress the stochastic noise and enhance the signal, see figure A.2.



(a) (b)

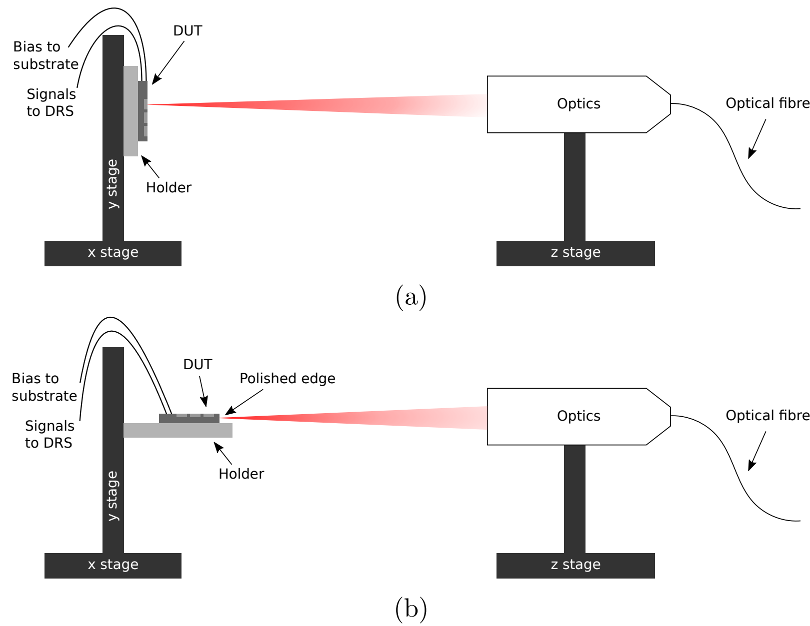
Figure A.2: TCT signal of a 50 μm thick PIN diode illuminated with infra-red laser pulses. A single waveform (a) and the average of 100 waveforms (b) are shown.

The system can be set to perform scans over any of the stages and power supplies, and also with arbitrary combinations of stages and power supplies. For each position and voltage value a waveform for each of the enabled channel of the DRS4 board is stored, additionally at each bias voltage variation the current read by the power supply is stored as well.

Scanning TCT Operation

By means of appropriate supports, the DUT can be mounted facing the beam with the top surface (Top-TCT), with the backside (Back-TCT) or with an edge (Edge-TCT). With each configuration different sensor properties can be investigated. For example, when using red light charges are generated close to the illuminated surface, so that only the charges that are collected by the electrode on the opposite side contribute to the signal, by using Top or Back-TCT it can be chosen to study the contribution of holes and electrons separately. Edge-TCT is usually used to study the evolution of

the depletion depth since shooting the laser from a lateral side of the sensor all the charges are generated at the same distance from the surface, if this is larger than the depletion depth the charges will not contribute to the signal.



(a)

(b)

Figure A.3: Sketch of the Top (a) and Edge (b) TCT set-up configurations.

In this thesis the TCT set-up at IFAE, and similar set-ups at the JSI institute in Ljubljana and at the Hamburg University, have been used for the measurement of HV-CMOS and LGAD devices. The measurement of the depletion depth of HV-CMOS devices and the study of its evolution with fluence are described in section 5.2. The study of the properties of different LGAD devices such as the gain and the inter-pixel gap is shown in sections 4.1.1 4.2.2 and 4.2.3.

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