Doctoral Programme: Electronic Engineering

Department: Electronic Engineering

MOS interface improvement based on boron treatments for high channel mobility SiC MOSFETs

Article based doctoral thesis

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Barcelona, October 2019

En memòria de

Rosalia, Ramon, Conchi, Paco, Lluch i Pepe,

una i mil vegades més.

Resum

El silici (Si) és el semiconductor utilitzat en la majoria de components comercials de potència, no obstant, les seves propietats intrínseques són insuficients per als nous requeriments de conversió energètica, fent que sigui necessari el desenvolupament de nous materials semiconductors. Les seves limitacions estan relacionades amb les pèrdues tèrmiques, la temperatura de funcionament, la resistència a la radiació o la velocitat de commutació.

Un material semiconductor més adequat és el Carbur de Silici (SiC) el qual té un alt valor de camp elèctric crític i un alt valor de la velocitat de saturació de portadors, cosa que el fa capaç de mantenir altes tensions amb menys pèrdues per conducció. A més a més, com passa amb el Si, es pot formar diòxid de silici (SiO_2) natiu sobre el SiC. Un inconvenient dels MOSFETs de SiC és la baixa fiabilitat del òxids i els baixos valors de mobilitat al canal, atribuïts a una mala qualitat de la interfície SiO_2/SiC, que conté una alta densitat de trampes a la interfície (D_{it}) i a l'òxid proper a la interfície (NIOTs). Els MOSFETs comercials de 4H-SiC són sotmesos a un procés tèrmic standard post-oxidació. Aquest consisteix en un recuit en ambient d'òxid nítric o òxid nitrós (NO, N_2O), amb el propòsit de reduir la D_{it} i els NIOTs. Tot i així, la passivació de la interfície assolida mitjançant la nitridació no és suficient i s'ha arribat al límit de millora que pot proporcionar aquest procediment.

Aquesta tesi està dirigida a resoldre un dels principals problemes de la tecnologia en 4H-SiC: trobar un procés de fabricació adequat i fiable que millori la qualitat i la fiabilitat tant de l'òxid de porta com de la interfície SiO_2/SiC, per a la seva aplicació en dispositius de potència.

Pel que fa a les prestacions elèctriques, ens centrem en dos dels principals reptes d'aquest àmbit: la millora de la mobilitat al canal d'inversió i l'estabilitat de l'òxid de porta, per tal de reduir la resistència del canal drenador-font i millorar la fiabilitat de l'òxid de porta.

Per assolir aquests reptes i millorar la tecnologia actual lligada a l'optimització de l'òxid de porta, seguim diverses estratègies: Per una banda, utilitzar una nova passivació d'interfície mitjançant mètodes d'oxinitridació combinats amb un tractament de difusió de bor (B) a través de l'òxid de la porta. Estudiant també quin és el seu impacte sobre l'estabilitat de les estructures tant a temperatura ambient com a altes temperatures. Aquest nou procés ha permès assolir valors de mobilitat del canal significativament elevats,

fins a 200 cm^2/Vs. Per altra banda hem treballat en la millora de la fiabilitat del dielèctric mitjançant una capa prima d'un material d'alta constant dielèctrica.

Paral·lelament, s'han estudiat diferents problemes de fabricació trobats durant el procés d'optimització del dielèctric. Tenint en compte les prestacions específiques dels nostres dispositius, vam adaptar els processos de caracterització elèctrica i física necessaris per a un estudi complet, tant de la qualitat de l'òxid i la interfície, com per al rendiment elèctric del MOSFET final.

Finalment, en aquest treball s'inclouen alguns estudis que proporcionen informació sobre l'impacte que té la difusió de B sobre la D_{it}, els NIOTs i, en general el comportament elèctric dels nostres dispositius. Concretament:

i) L'anisotropia en la mobilitat dels MOSFETs, tenint en compte els diferents mecanismes de dispersió implicats en la mobilitat dels portadors.
ii) L'efecte de les dimensions del canal sobre la mobilitat obtinguda.
iii) Comparació de l'efecte de passivació que té el B sobre MOSFETs fabricats en els politipus 4H-SiC i 6H-SiC.

Malgrat el procés de dopatge de bor presentat encara no està suficientment madur per ser utilitzat en dispositius comercials, ens ha permès progressar en la comprensió d'alguns dels fenòmens que tenen lloc a la interfície SiO_2/SiC, en la seva adequada caracterització i interpretació i, en definitiva, en obrir camí cap a una major millora de l'estructura MOS en SiC.

Abstract

Although silicon (Si) is used in most current commercial power semiconductor components, Si capabilities are insufficient for new energy conversion requirements. Some of its important limitations are related with power losses, operation temperature, radiation hardness and switching speed. Then, new semiconductor materials must be developed to face the future global energetic challenges, overcoming Si intrinsic limitations.

Silicon Carbide (SiC) is a proper wide bandgap (WBG) semiconductor with high critical electric field strength and a high saturation carrier's drift velocity, which makes it able to sustain higher voltages with lower conduction losses. Furthermore, in a similar way to Si, SiC native oxide (SiO_2) can be formed. However, a drawback of SiC MOSFETs is their poor oxide reliability and low channel mobility values attributed to a poor SiO_2/SiC interface quality, with high density of interface traps (D_{it}) and near interface oxide traps (NIOTs). Nitridation processes, consisting in a nitric or nitrous oxide (NO, N_2O) annealing is considered as the standard post oxidation annealing approach in 4H-SiC MOSFETs, being commonly used in commercial SiC power MOSFETs for reducing the D_{it} and NIOTs. However the nitridation interface passivation is not enough and, furthermore the limit of the improvement provided by nitridation has been reached.

This thesis is focused on 4H-SiC-based power devices, particularly, on one of the major issues in SiC technology: to find a suitable and reliable fabrication process that improves the gate oxide and SiO_2/SiC interface quality and reliability. Regarding electrical performances, we will focus on two of the major challenges of this field: the improvement of the inversion channel mobility, and the gate oxide stability, in order to further reduce the on-resistance and enhance the gate oxide reliability. Both problems are related to the defects near the SiO_2/SiC interface.

To meet these challenges and improve the current gate oxide quality state-of-the-art, several strategies were followed. We have worked on a newly interface passivation by oxynitridation methods combined with a boron diffusion treatment through the gate oxide. This novel approach allowed us to reach significantly high channel mobility values, up to 200 cm^2/Vs. We also extensively studied the impact of the boron treatment parameters on the stability performances of our test structures, revealing some stability issues, especially at high temperature operation. In parallel, we have also worked on the improvement of the dielectric reliability by using a thin layer of a high-k material.

On the other hand, equally important, we studied the different fabrication issues found during the gate dielectric optimisation process. Taking into account the specific performances of our devices, we adapted

the electrical and physical characterization processes required for a complete study of this kind of high mobility devices (for both, oxide and interface quality characterization, and final electrical MOSFET performance).

Finally, some studies which provide information about boron treatment impact on the oxide and interface traps, and about the global electrical behaviour of our devices are included in this thesis; concretely:

i) A study on MOSFET mobility anisotropy, having into account different scattering mechanisms involved in channel carrier's mobility.

ii) The effect of MOSFET channel dimensions in the obtained channel mobility.

iii) A comparison of B passivation effect on MOSFETs fabricated over 4H-SiC and 6H-SiC polytypes.

As a result, despite our new boron doping process is still not mature to be used in commercial devices, it allowed us to progress in the understanding of some of the phenomena taking place at the SiO_2/SiC interface, in the way to properly characterise and interpret them, and in the way to further improve the MOS structure on SiC.

Keywords:

Silicon Carbide (SiC)

4H-SiC

Field effect mobility (μ_{fe})

Density of interface traps (D_{it})

Near Interface Oxide Trap (NIOT)

Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

Boron diffusion

High-k dielectric

Acknowledgement

As a prelude to this thesis dissertation I would like to express all my gratitude to the people which have contributed to the work here reported, and those that always supported and believed in me.

First, I would like to express my gratitude to the members of the dissertation committee for having agreed to evaluate this work; Prof. Daniel Alquier (Université de Tours, Tours, France), Dr. Patrick Fiorenza (CNR-IMM, Catania, Italy), Dr. Enrique Maset (Universitat de Valencia, Valencia, Spain), as well as the substitute members, Dr. Jesus Urresti (Newcastle University, Newcastle, UK) and Dra. Mireia Bargalló (IMB-CNM, Barcelona, Spain).

Special thanks are expressed to all the members and coordinators of the SPEED project. Collaboration between the partners and fellow coming from different institutions, helping spirit and support, excellent scientific quality, opportunities and founding to actively participate to international congresses.

Different people from several institutions have collaborated throughout this thesis as regards specializing processing or physical characterization: Aneesha Varghese (Annealsys, Montpelier, France), Lars Knoll (ABB, Baden, Switzerland), Gabriel Ferro (Université de Lyon, Lyon, France), Anna Regouth (Imperial College London, London, UK) and Daniel Haasmann (Griffith University, Brisbane, Australia).

En segon lloc vull expressar la meva més sincera gratitud als meus directors; el Prof. Philippe Godignon i el Dr. Josep Montserrat per tots els consells, les seves idees, discussions científiques i la seva impecable feina tecnològica, que m'han permès tenir una amplia i meticulosa visió de la tecnologia que envolta el processat del SiC. Com digué Isaac Newton al 1675: "If I have seen further it is by standing on the shoulders of Giants". Però sobretot (junt amb el Prof. Francesc Guinjoan) vull agrair-los haver-me donat la oportunitat de dur a terme el treball de doctorat que aquí presento.

Tres persones que tenen un paper molt rellevant en el meu aprenentatge han estat els Drs. Matthieu Florentin, José Rebollo i Joan Marc Rafí, moltes gràcies per cada minut del vostre temps dedicat a crear, posar en dubte i forjar els meus coneixements en física de semiconductors.

El pal de paller de la meva tesi rau en el procés de fabricació i caracterització de dispositius de SiC tant a dins com a fora de Sala Blanca. En aquest cas, són moltes les persones a les que he d'agrair el seu temps, coneixement i dedicació: David, Mª Ángeles, Raquel, Miguel, Gemma, Javi, Luís, Sara, Ricard, Roser, Carles,

José, Josep, Marta, Núria, Elena, Samuel, Liber, Xevi, Albert, Oihane, Raúl, Guillaume ... Moltes gràcies per tot.

Moltes gràcies a tots els membres (i exmembres) del grup de potència per les estones, discussions i ajuda al llarg d'aquests anys: Albert, Alberto, Arnau, Bernat, David, Fede, Gemma, Jordà, Manu, Miquel, Oriol, Pepín, Perpi, Ra, Víctor i Viorel.

Companys del CNM, d'estones, de cafès, de tuppers i d'AfterWork, moltes gràcies per fer que cap dia passes de llarg sense un somriure. "Qui dia passa any empeny" i vosaltres heu fet que els darrers 5 anys passessin volant.

No seria on sóc sense el recolzament d'una família meravellosa, de la que no podria estar-ne més orgullosa, que ha demostrat amb escreix, que junts ho podem lluitar tot. Gràcies també a la família que s'escull (i que ben escollida!); mala influència, bressol, refugi i pista de ball de tots els meus estats d'ànim. Per últim, sempre agraïda als meus pares, a en Ramon i a en Pau, per tot el vostre suport, estim i confiança i per fer-nos junts cada dia més forts, més humils i més reals.

"There is a crack in everything. That's how the light gets in".

- *Leonard Cohen*

TABLE OF CONTENTS

Gate Oxide Improvement

List of Figures

List of Tables

List of Symbols

A_c	Contact area
A_G	Gate area
C_C	Corrected capacitance
C_{DEP}	Depletion layer Capacitance
C_{FB}	Flat band capacitance
C_{HF}	High frequency capacitance
C_{IT}	Interface traps capacitance
C_{LF}	Low frequency capacitance
C_m	Measured capacitance
C_{max}	Maximum capacitance (accumulation region)
C_{ox}	Oxide capacitance
C_P	Parallel capacitance
C_{QS}	Quasi-static capacitance
D	Distance between contacts (in a TLM structure)
D_{it}	Density of interface traps
E_C	Conduction Band energy level
E_F	Fermi energy level
E_g	Energy gap
E_i	Intrinsic energy level
E_V	Valence band energy level
G_C	Corrected parallel conductance
G_{it}	Parallel interface trap conductance
G_m	Measured conductance
g_m	Transconductance
G_P	Parallel capacitance
Hi-Lo	High-low
I_{cp}	Charge pumping current
I_D	Drain current
I_G	Gate current
k	Dielectric constant
k_B	Boltzmann constant ($1{,}38 \cdot 10^{23}$ $J \cdot K^{-1}$)
L	Channel length
L_T	Effective contact length
n	Electron concentration
N_a	Semiconductor doping
N_c	Effective density of states in the conduction band
N_{eff}	Effective charge in the isolator

n_i	Intrinsic carrier concentration
N_s	Free carriers density
N_T	Trapped charge density
q	Electron charge, (1,602·10e-19 C)
Q_{cp}	Charge pumping charge
Q_F	Fixed insulator charge
Q_{IT}	Interface trapped charge
Q_{ot}	Oxide trapped charge
R_C	Metal/semiconductor interface resistance
R_{ch}	Channel resistance
R_d	Drain resistance
R_{dc}	Drain contact resistance
R_m	Metallic contact resistance
R_{ON}	On channel resistance
R_s	Series resistance
R_{sc}	Source contact resistance
R_{semi}	Semiconductor resistance
R_{sh}	Sheet resistance
R_{so}	Source resistance
R_T	Total resistance
T	Temperature (K)
T_{ox}	Oxide thickness
v_d	Carriers drift velocity
V_{DS}	Drain-Source voltage
V_{FB}	Flat band voltage
V_G	Gate voltage
V_t	Thermal velocity of electrons
V_{th}	Threshold Voltage
W	Channel width
W_{DEP}	Depletion zone width
W_{max}	Maximum depletion layer width
μ_{AC}	Acoustic phonon scattering mobility limitation
μ_C	Coulomb scattering mobility limitation
μ_{eff}	Effective mobility
μ_{fe}	Field effect mobility
μ_{Hall}	Hall effect mobility
μ_n	Bulk electron mobility
μ_{OP}	Optical phonon scattering mobility limitation

μ_p	Bulk hole mobility
μ_{SR}	Roughness scattering mobility limitation
Y_m	Measured admittance
Δ	Amplitude
ε_o	Vacuum permittivity
ε_{ox}	Oxide relative permittivity
ε_r	Relative permittivity
λ_d	Debye length
ρ_c	Contact resistivity
σ_n	Capture cross section
τ_c	Capture time constant
τ_e	Emission time constant
ψ_{BI}	Build in potential
ϕ_B	Bulk potential
Φ_M	Metal work function
Φ_{MS}	Metal-Semiconductor work function
Φ_S	Semiconductor work function
χ_{SiC}	SiC electron affinity
Ψ	Phase
Ψ_S	Band bending

List of abbreviations

AC	Alternating Current
AFM	Atomic Force Microscope
B	Boron
BJT	Bipolar Junction Transistor
BSE	Backscattered Electrons
BSI	Bias Stress Instability
BTI	Bias Temperature Instability
CC	Constant Current
CMOS	Complementary Metal–Oxide–Semiconductor
CNM	Centre Nacional de Microelectrònica
CO_2	Carbon Dioxide
CP	Charge Pumping
CV	Capacitance-Voltage
CVD	Chemical Vapor Deposition
D	Drain
DC	Direct Current
DLTS	Deep-Level Transient Spectroscopy
EDX	Dispersive X-ray Spectroscopy
G	Gate
Ga_2O_3	Gallium trioxide
GaN	Gallium Nitride
GV	Conductance-Voltage
HEV	Hybrid Electric Vehicles
HF	High Frequency
HMOS	Hexamethyldisilazane
HS	High Speed
IGBT	Insulated-Gate Bipolar Transistor
JFET	Junction Field-Effect Transistor
LF	Low Frequency
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
N_2O	Nitrous Oxide
NBSI	Negative Bias Stress Instability
NIOTs	Near Interface Oxide Traps
NO	Nitric Oxide
NonRlx	Non Relaxation
PBSI	Positive Bias Stress Instability
POA	Post Oxidation Annealing
PSPD	Position Sensitive Photo Detector
PV	Photo Voltaic

QS	Quasi Static
R&D	Research and Development
RMS	Root Mean Square
RT	Room Temperature
RTO	Rapid Thermal Oxidation
S	Source
SBE	Switch Back Epitaxy
SE	Secondary Electrons
SEM	Scanning Electron Microscope
SF	Stacking Fault
Si	Silicon
SiC	Silicon Carbide
SIMS	Secondary Ion Mass Spectroscopy
SiO_2	Silicon Dioxide
TEOS	Tetraethyl Orthosilicate
TFT	Thin Film Transistor
TLM	Transfer Length Method
TOF-SIMS	Time of Flight Secondary Ion Mass Spectroscopy
UPS	Uninterrupted Power Supply
UV	Ultra Violet
WBG	Wide Band Gap

Section 1

General introduction

Chapter 1

Introduction to SiC and MOS based devices

Nowadays the main challenges to face with, in terms of energy, are: reaching an efficient energy management and the reduction of energy needs, as well as, the clean energy generation. The world consumption of electrical energy is yearly growing [1]. It is expected that the amount of the electrical energy that passes through an electronic power converter will highly increase in the next years. Hence it is necessary to improve the converters performance in order to reduce the energy losses. The milestone of reducing the CO_2 emissions could be reached by reducing the percentage of energy lost in the transportation/conversion systems.

Semiconductor microelectronics is largely based on silicon (Si) technologies, which have been developed and improved during the last 60 years. The advantages of Si are mainly to have a more favorable chemistry and physics for doping, oxidizing, etching, cleaning, as well as the high quality of the starting crystalline substrates and their low cost. However, in order to have more efficient voltage conversion we need electronic switches where no current flows when the device is off, and no voltage drop when it is on.

It is today widely recognized that new generations of power devices based on wide band gap (WBG) semiconductor materials with superior material properties are required for a higher efficiency and robust operation of power converters [2]. Power electronics based in WBG semiconductors like silicon carbide (SiC), galium nitride (GaN) or gallium oxide (Ga_2O_3) overcome the material-dependent limits of Si-based power devices, having superior properties for specific electronic applications, with the exception of the electron mobility where slightly higher values are reported on Si. They have a higher switching speed (reducing power losses), endurance to higher temperatures, higher power, higher breakdown voltage and lower on-resistance. As WBG critical field is more than one order of magnitude higher than in Si, the use of a thinner and more conductive epitaxial layer is allowed and, consequently, the on-state current losses of electronic devices are drastically reduced. The superiority of these WBG materials compared to Si can be schematically seen in Fig. 1.1 in terms of electron mobility, critical electric field, energy bandgap, electron saturation velocity, thermal conductivity and melting point values.

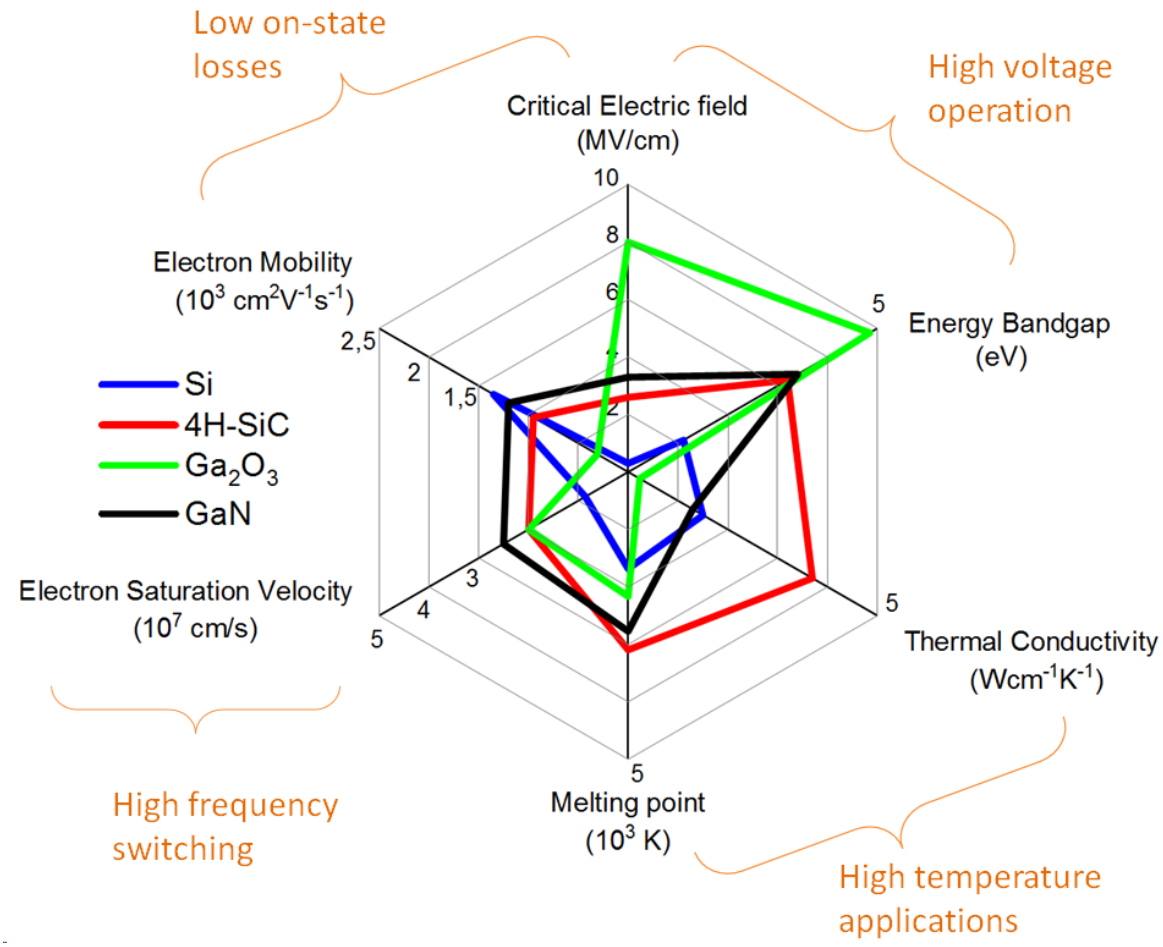

Figure 1.1 Material limits of some wide band gap semiconductors compared with Si values.

Nevertheless WBG semiconductors usually present more drawbacks, both in terms of technologies and costs. Within the WBG family, SiC is one of the most promising semiconductor materials for the fabrication of power devices, and currently several commercial devices are already offered in high volume production. In addition, SiC is foreseen for other applications like ultraviolet (UV) detectors, high temperature radiation detectors for nuclear physics applications, high temperature (>250°C) digital and analog electronics, gas sensors and biosensors.

On the other hand, MOSFET is a key element in modern microelectronics, with applications spanning from highly integrated CMOS to high power devices. It has really boosted the development of all kind of microelectronic technologies since the 70's. Regarding power electronics technologies, which was initially based on Si bipolar devices (BJTs and thyristors), MOSFETs and MOS gate-controlled devices (mainly IGBTs), completely monopolizes today's market. However, these Si-based MOS controlled devices have reached their limits imposed by the Si material properties. Among SiC-based power devices, SiC MOSFET has been

the focus of numerous investigations since its demonstration in 1993 [3]. However, the development of efficient low resistive SiC power MOSFETs has been slower than other SiC power switches, like JFETs or BJTs, due to very low inversion channel mobility values and high instability of the threshold voltage (V_{th}). These two limitations were mainly caused by a poor quality of the MOS interface, which is affected by the amount of oxide charges and the large interface trap density (D_{it}) values. Despite these issues, sufficient improvements in the MOS interface quality allowed the realization of first generations of commercial SiC MOSFETs operative up to 1.2 kV–1.7 kV. However, we are still far from the theoretical potential of the material, especially regarding channel mobilities and higher voltage devices. The current roadmap for SiC semiconductor industry tentatively predicts the introduction of 3.3 kV–6.5 kV SiC devices in the market in the medium term to compete with their Si-based counterparts [4]. SiC MOSFET is also foreseen for digital electronics able to work at temperatures higher than 200°C. The issues are similar as with power MOSFETs regarding interface quality and stability. Fig. 1.2 shows market perspective for SiC and GaN in the following years in different application fields.

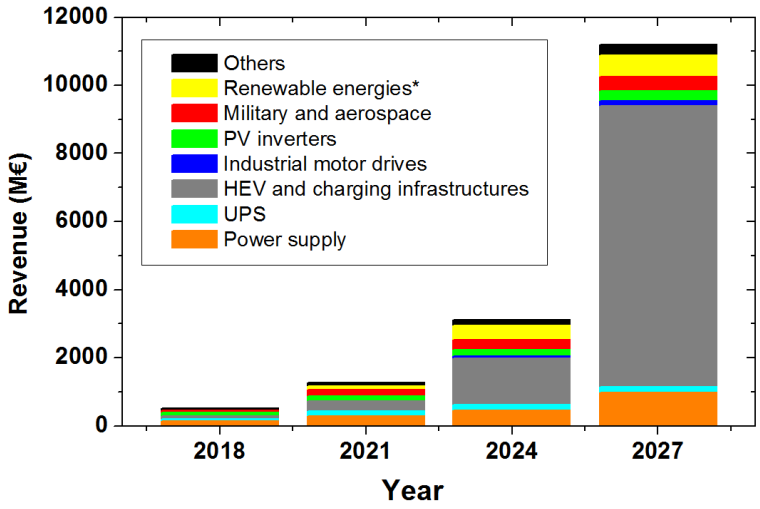

Figure 1.2 Perspectives for SiC and GaN market. PV means photovoltaic, HEV means Hibrid electric vehicles and UPS means Uninterrupted Power supply. (Source: IHS Markit [5] and Yole développement [6]).
**Data about renewable energies estimated to 2027 was not found in literature, we have chosen the plotted value following the "renewable energies growth tendency of the other time periods reported.*

Consequently, there is a large interest to further improve the MOSFET structure on SiC. This thesis is then focused on one of the main limitations of the SiC MOSFET: the gate oxide and the SiC/SiO_2 interface quality.

1.1 Outline

In order to improve the SiC MOSFET properties, we first need to familiarize ourselves with the SiC material, as well as with the different SiC polytypes, especially with the 4H-SiC polytype. 4H-SiC is the most employed polytype in the R&D and commercial devices (for several reasons detailed later in this work). We will focus on the oxidation of this semiconductor material, the different charges involved, defects, scattering phenomena and other characteristics that could imply limitations on the electrical properties of the final MOS and MOSFETs structures.

This work has been structured as follows: A general introductory section, focused in general theory and experimental methodology; a second section with the objectives, results (compendium of the main relevant publications of my work) and some discussion related with the obtained results, and finally the conclusions and recommendations for future work.

In this introductory chapter (Chapter 1) are described some properties of different SiC-polytypes as well as basic concepts related to SiC technology, oxidation, MOS and MOSFET structures. In Chapter 2, experimental methods are deeply explained, from the manufacturing steps up to the characterization of the obtained devices. Focusing in the different issues found during this work. The manufacture of the devices is detailed in the Apendix.

In Chapter 4, relevant articles published along this work can be found. The paper's main topics are:

i) A review on the different processing techniques used for 4H-SiC MOSFETs
ii) The impact (and mobility increase) in MOSFETs using a B doping process
iii) The B impact on 2 different SiC polytypes
iv) The mobility anisotropy seen in SiC MOSFETs
v) The study of high-k materials used as alternative dielectrics on 4H-SiC devices

1.2 SiC general properties

SiC is a semiconductor composed by Si and C atoms, which can adopt different crystal structures, called polytypes. These polytypes are commonly named (Ramsdell's notation) by the number of Si-C bilayers in the unit cell and the crystal system (C=cubic, H=hexagonal or R=rhombohedral). Some of the most popular polytypes structures are shown in Fig. 1.3 (a).

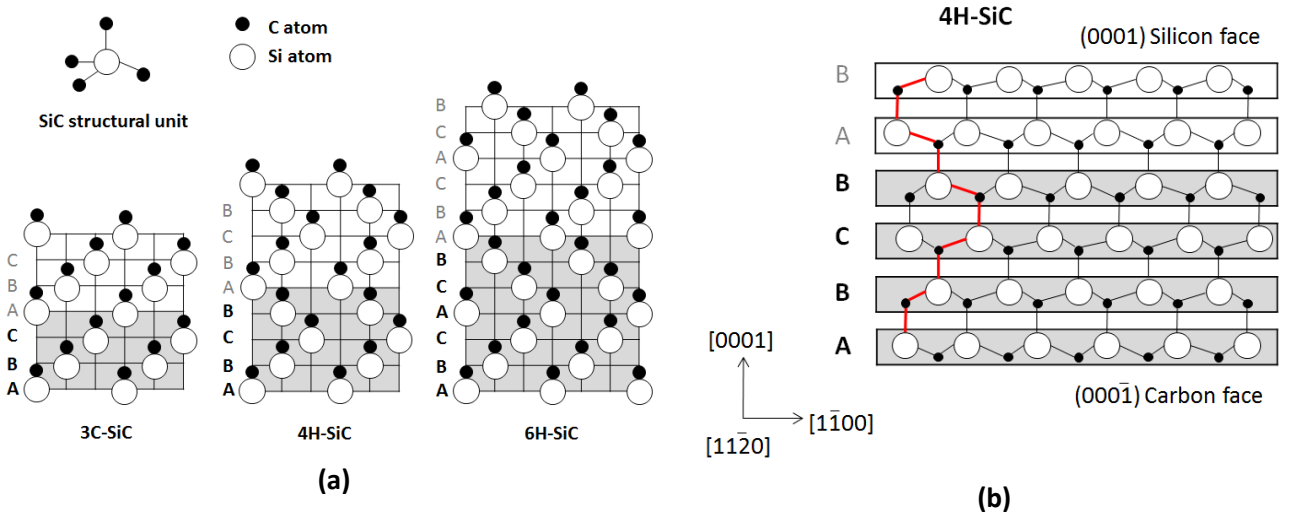

Figure 1.3 (a) Stacking sequence of bilayers of Si and C atoms of 3C-, 4H- and 6H-SiC. (b) Basic structural unit of SiC and the stacking sequence of bilayers of Si and C atoms for 4H-SiC polytype (Stacking sequence indicated by a red line).

SiC basic structural unit consists of a covalently bonded tetrahedron of four C (or Si) atoms with a Si (or C) atom in the center. Each tetrahedral unit joins to other four units at the corners to form the SiC crystals, where stacks follow distinctive bilayer arrangements for each polytype.

Table 1.1. Properties of SiC polytypes compared to Si.

Material	E_g (eV) @ 300k	μ_n ($cm^2/V{\cdot}s$)	μ_p ($cm^2/V{\cdot}s$)	μ_{fe}* ($cm^2/V{\cdot}s$)	Ratio μ_n/μ_{fe}	E_c (MV/cm)	ε_r
Si	1.11	1350	450	500	2.7	0.3	11.8
3C-SiC	2.3	750	40	150	5	1.6	9.6
6H-SiC	3.05	415	90	45	9.2	2.6	9.7
4H-SiC	3.2	950	120	7	135	2.5	9.7
15R-SiC	2.98	600	-	60	10	2.5	9.7

*Average value of inversion channel mobility for either dry or wet oxidations [7]

Each polytype exhibits unique electrical, optical, thermal and mechanical properties. Table 1.1 summarizes main fundamental electrical properties of some polytypes, together with Si characteristics for reference. In most present applications, devices are fabricated on 4H-SiC polytype, due to its superior and more isotropic bulk carrier mobility.

1.2.1. 4H-SiC

Among the available polytypes, 4H-SiC has superior material properties and availability. Its breakdown field is one order of magnitude higher than Si, leading to more favorable on resistance (R_{ON}) optimization. 4H-SiC has a wide bandgap of 3.26 eV at room temperature and can be operated at high temperatures over 300°C. 4H-SiC shows the best trade-off combining bulk mobility, breakdown voltage and epilayer resistance. In terms of substrate/crystal production, originally this polytype was found to be energetically the most favorable, followed by 6H and 8H-SiC, respectively [8]. Yet, these polytypes are actually metastable and, therefore, require non-equilibrium growth conditions. In Fig. 1.3 (b), the basic structural unit of SiC, and the stacking sequence of bilayers of Si and C atoms of 4H-SiC are shown.

C atoms are more electronegative than Si atoms, therefore SiC is a polar compound semiconductor where the valence electrons are slightly located closer to C atoms than to Si atoms. In a hexagonal (or rhombohedral) structure, the (0001) face, where one bond from a tetrahedrally-bonded Si atom is directed along the c-axis [0001], is called the "Si-face," while the $(000\bar{1})$ face, where one bond from a tetrahedrally-bonded C atom is directed along the c-axis, is called the "C-face."

Fig.1.4 (a) illustrates the definition of several major planes in a hexagonal SiC polytype. Other than the Si and C faces, there is the $(11\bar{2}0)$ face, also called the a-face, and the $(1\bar{1}00)$ face the m-face. The surface energy, chemical reactivity, and electronic properties are significantly dependent on these crystal faces. Standard SiC wafers are directed along [0001] axis with several degrees off-axis toward $[11\bar{2}0]$ axis, as shown in Fig. 1.4 (b).

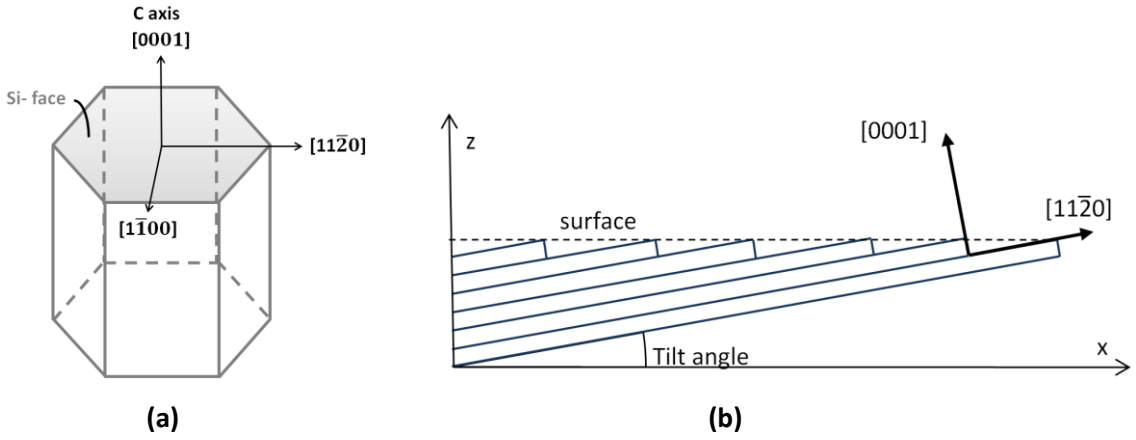

Figure 1.4 (a) Different planes in a hexagonal SiC polytype. (b) Standard off-axis SiC wafer surface.

1.2.2. 3C-SiC

Compared to 4H-SiC and 6H-SiC based MOSFETs, the few examples of 3C-SiC MOSFETs reported in the literature systematically exhibit higher field effect mobility (μ_{fe}) values. Their behavior is corroborated by their lower density of interface traps (D_{it})($7 \times 10^{10}\,cm^{-2}\,eV^{-1}$ at 0.2 eV from the conduction band (E_C)) values obtained from their experimental measurements. The fact is that as the 3C-SiC bandgap is smaller than of the hexagonal polytypes, therefore, the traps that capture electrons from the channel, which would partially cause μ_{fe} degradation, are located within the E_C and they do not participate to electron trapping and de-trapping [9]. This behavior is illustrated in Fig. 1.5.

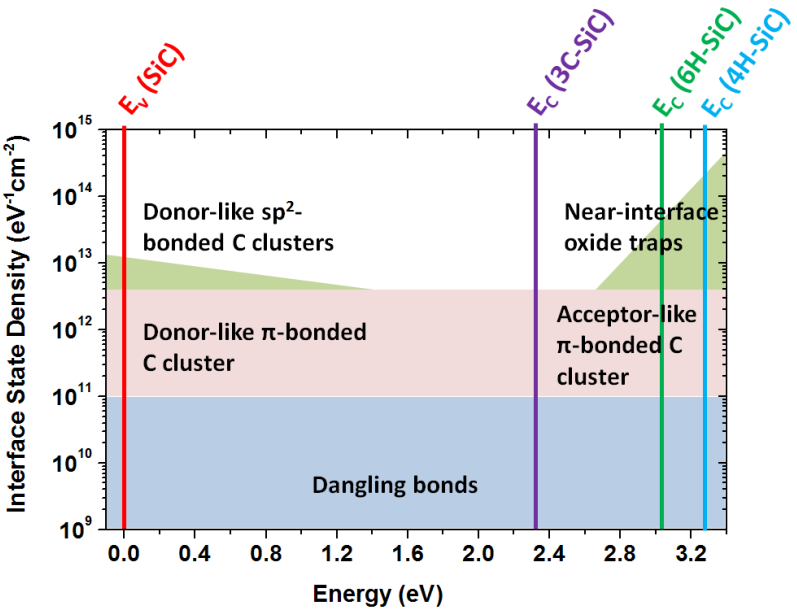

Figure 1.5 Schematic composition of the SiO_2/SiC interface state density as a function of the energy position for 3C-, 4H-, and 6H-SiC (adapted from [10]).

The lower active D_{it} values obtained in 3C-SiC have allowed the manufacture of N-MOSFETs with μ_{fe} values between 75 and 260 cm^2/Vs using a conventional dry oxide gate process [9]. This is different from the rest of SiC polytypes where extra nitridation or specific Post Oxidation Annealing (POA) treatment are required. From the point of view of channel efficiency, 3C-SiC would be the ideal polytype for the fabrication of SiC-based power MOSFETs. However, this polytype also has important limitations. Drawbacks include its lower critical field strength or lower thermal conductivity, which both limit 3C-SiC application in MOSFET high voltage applications. Moreover, the main issue is the 3C-SiC starting material quality and its processing. Since 3C-SiC polytype is a metastable crystal phase, it cannot be grown in large wafer size by the

sublimation method. Despite original growth methods have been proposed, such as Chemical Vapor Deposition (CVD) on Si substrates [9, 11] or Switch Back Epitaxy (SBE) method, a large density of defects and, especially, Si-terminated stacking faults (SF) are still largely present in the available material, which limits 3C-SiC use for real commercial devices.

It is expected that the quality of the 3C-SiC material available in the market will be greatly improved in the next few years thanks to the "*3C Challenge"*, which is a HORIZON 2020 project financed under the "Nanotechnologies, advanced Materials, Biotechnology and Production" (NMBP) work program that studies growth, processing and devices in 3C-SiC. With 15 partners from different world countries involved. More information can be found in their website; http://www.h2020challenge.eu/

1.2.3. 6H-SiC

Similar to 3C-SiC, the quality of the SiO_2/6H-SiC interface, and consequently μ_{fe} values, is inherently higher than that of the 4H-SiC polytype, which is due to its smaller bandgap. Technologically, 6H-SiC MOSFET's with μ_{fe} values up to 72 cm^2/Vs have been reported when standard dry oxidation treatment is combined with low temperature wet re-oxidation annealing, in this case, without the need of, for instance, nitridation or incorporation of other element atoms [12]. Indeed, nitridation was also proven effective in improving the interface quality of 6H-SiC MOSFET [13]. However, despite high quality 6H-SiC crystal, unlike 3C-SiC, can actually be obtained, its low bulk mobility along the c-axis, due to its large crystal anisotropy, makes this polytype unattractive for MOS gated devices fabrication [14].

1.2.4. 15R-SiC

15R-SiC polytype behaves similarly to 6H-SiC polytype, but with slightly higher μ_{fe} values due to its higher bulk mobility. However, 15R-SiC material is very difficult to synthesize, so experimental results of growth process always contain large amounts of other polytypes inclusions.

1.3 SiC oxidation

SiC is the only WBG semiconductor that grows thermal SiO_2 dielectric, either by dry or wet oxidation:

- ➔ Dry oxidation: $2SiC(s) + 3O_2(g) \rightarrow 2SiO_2(s) + 2CO(g)$
- ➔ Pyrogenic (wet) oxidation: $SiC(s) + 3H_2O(g) \rightarrow SiO_2(s) + CO(g) + 3H_2(g)$

This oxidation reaction occurs at SiC surface, so that SiO_2/SiC interface move into the SiC during the oxidation process. Since oxidation area is fixed, oxide thickness is proportional to oxide volume. As the volume of 1 mol of the SiC and SiO_2 are known, the SiC thickness being consumed can be calculated. Considering 1 mol of SiC converted into 1 mol of SiO_2, one will obtain: thickness of SiC/thickness of SiO_2 ≅ 0.46.

The oxide growth rate depends on the 4H-SiC crystallographic face. The growth ratio on the 4H-SiC Si-face is 10 times slower than that on Si. And, the 4H-SiC C-face is just 5 times slower than in Si.

Although, like in Si, SiC is oxidized into SiO_2, this process becomes more complicated in SiC. An important issue is the presence of C atoms in the reaction, and so, the presence of C at the interface, which is associated to a possible source of interface traps. As it is deeply explained later on this chapter one of the main issues of the SiC technology is related with its poor SiC/SiO_2 interface quality, and the high density of interface traps. Many theories and efforts have been dedicated to the SiO_2/SiC interface improvement, the reduction of the D_{it} and therefore, the improvement of SiC devices mobility (see Chapter 1.6. Present challenges).

1.4 MOS structure

The study of the semiconductor/oxide interface is of particular interest for the MOSFET technology. The presence of electrically active impurities at the semiconductor/oxide interface is responsible for the low channel mobility of devices in comparison to the higher theoretically expected channel mobility. The estimation of the dielectric quality and its interfacial properties is usually carried out with MOS capacitors.

In Fig. 1.6 there is a schematic explaining the physical principles on MOS structures. Fig. 1.6 shows how a MOS capacitor works and how the band diagram looks like depending on the applied gate voltage. The flat band condition on an ideal MOS capacitor (no bias applied) is the condition where the substrate energy bands (E_C and valence band (E_V)) are flat at the substrate/dielectric interface. While in an ideal MOS capacitance the work function of the gate electrode (Φ_M) and of the semiconductor (Φ_S) have the same value, in a real MOS the difference between these values (Φ_{MS}) is [15]:

$$\Phi_{MS} = \Phi_M - \Phi_S = \Phi_M - \left(\chi_{SiC} + \frac{E_G}{2q} \mp \phi_B\right) \quad (1.1)$$

where the bulk potential (ϕ_B) operation would be - ϕ_B in N-type MOS and +ϕ_B for p-type MOS structure. χ_{SiC} is the electron affinity of the semiconductor. The ϕ_B is given by:

$$\phi_B = \frac{E_F - E_i}{q} = \frac{k_B T}{q} \ln\left(\frac{N_A}{n_i}\right) \quad (1.2)$$

where N_A is the semiconductor doping and K_B the Boltzmann constant.

In Fig. 1.6 E_F is the fermi level, E_i the intrinsic energy level and Ψ_s is the band bending. If the substrate is held at ground and a voltage is applied to the gate, the MOS capacitor would go through different working regions (different band bending magnitude) depending on the applied voltage:

If a positive voltage is applied electrons (majority carriers) will start to store at the SiC surface. The surface will have a greater density of electrons than N_a, and the bands will bend downwards. This condition, where the band bending is positive ($\Psi_s > 0$) and $\phi_s > 0$, is known as surface **accumulation**. In this condition the mobile charge on both sides of the oxide can respond rapidly to changes in the applied voltage, and the device looks just like a parallel plate capacitor of thickness T_{ox}. Since it is a pure gate oxide capacitance, its value is denoted as C_{ox}. If a negative gate voltage is applied to the gate, the concentration of holes near the SiC surface will be larger than that of electrons. This condition, where $\Psi_s \leq -2\phi_B < 0$ and $\phi_s < 0$, is known as **inversion**. In inversion condition the minority carriers are supplied by thermal generation (or another source as a pn junction). Then, due to the large bandgap of SiC there is practically no thermal generation of carriers, being nearly impossible to reach the inversion condition in a SiC MOS capacitor at room temperature. When the surface potential decreases, the electrons concentration also decreases, and hence, the width of the depletion layer increases with the gate voltage in order to maintain the charge neutrality. This corresponds to the **deep depletion** condition.

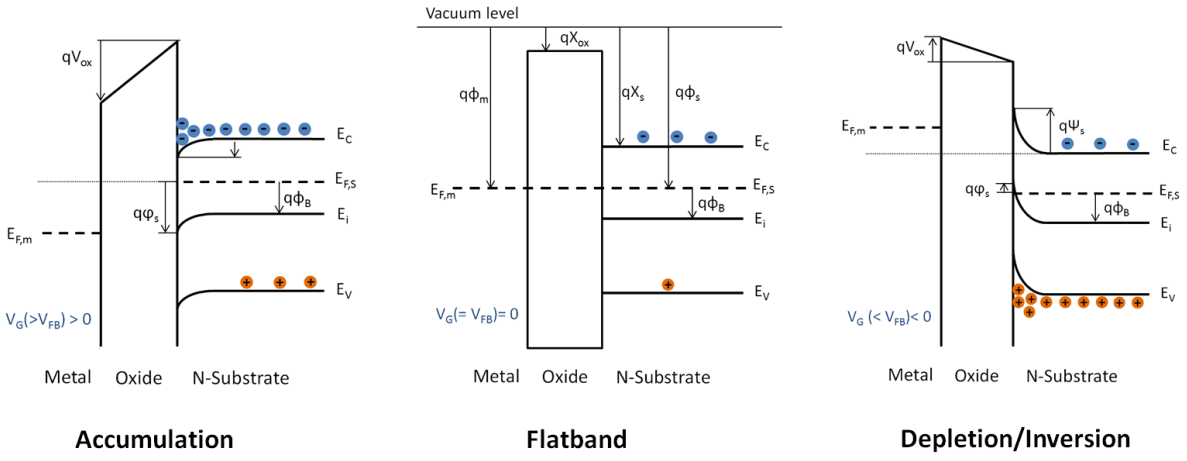

Figure 1.6 Energy band diagram for an n-substrate ideal MOS capacitor under different bias conditions: Accumulation, Flatband and Depletion/Inversion. An arrow pointing down defines a positive potential and an arrow pointing up a negative potential.

As is shown in Fig. 1.6, in a n-type ideal MOS capacitor, the resulting charges produce a band bending near the oxide/substrate interface. The bands bend upwards if $V_G<0$ and downwards when $V_G>0$. The energy levels and potentials are marked for the flatband condition ($V_{FB}=0$).

On a real MOS structure the flat band voltage (V_{FB}) will not be zero, instead it has into account the different oxide charges by [15]:

$$V_{FB} = \Phi_{MS} - \frac{Q_F}{C_{ox}} - \frac{Q_{it}(\psi_S)}{C_{ox}} - \frac{1}{C_{ox}}\int_0^{T_{ox}} \frac{x}{T_{ox}}\rho(x)dx \tag{1.3}$$

Where $\rho(x)$ is the oxide charge per unit volume, x is the position inside the oxide being x=0 in the metal/oxide interface and $x=T_{ox}$ in the oxide/semiconductor interface. $Q_{it}(\psi_s)$ is related with the interface traps, which occupancy depends on the surface potential. Q_F accounts for the fixed charge located near the SiC/SiO_2 interface, which is considered to be at the interface. The main factors affecting the V_{FB} value are the fixed and trapped charges in the oxide which are independent of the applied BIAS, the mobile charges and the near-interface states that can be charged or discharged.

The energy band diagram will be different depending on the SiC polytype (different band gap and different offsets values). Because of the wide bandgap of SiC, one can find very few contact metals with very low barrier heights. Fig. 1.7 shows the band diagram of different SiC polytypes, including the vacuum level.

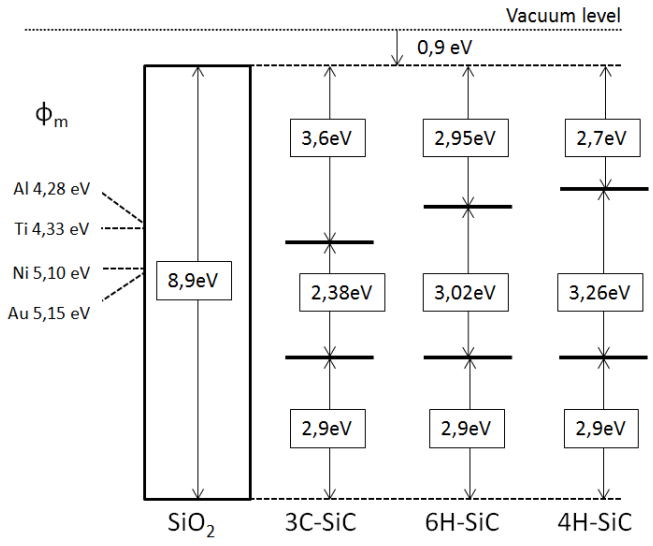

Figure 1.7 Schematic energy band diagram of 3C-SiC, 6H-SiC, 4H-SiC and SiO_2 illustrating the conduction and valence band offsets for each of these materials with respect to SiO_2. The work function of some metals commonly used is also showed.

1.5 MOSFET structure

A Metal-Oxide-Semiconductor Field-Effect transistor (MOSFET) could be described as a MOS capacitor where the inversion layer is contacted on both sides; from Source (S) and Drain (D) regions, which doping type is opposite to the main substrate. The n-MOSFET transistor is based on the injection of electrons through a highly n-doped region, the source. The electrons have then to cross a p-type region in which an inversion channel can be created by applying a given bias into the gate (G). The body (B) is the contact to the p-well (or p-epitaxy), is normally connected with the source to the ground potential. The inversion channel dimensions are a length L and a width W. The two main parameters of the current flow inside the channel are the free carrier's density (N_s), and their mobility.

Due that the current in a MOSFET is transported predominantly by carriers of only one polarity, the MOSFET is usually referred to as a unipolar or majority-carrier device. The operation of an n-MOSFET device can be easily understood from the MOS capacitor:

- When there is no voltage applied to the gate or when the gate voltage is zero, the p-type SiC surface is either in accumulation or depletion. There is not current flow between the source and the drain. The MOSFET acts like two back-to-back p-n junction diodes with only low-level leakage current present.
- When a sufficiently large positive voltage is applied to the gate, SiC surface is inverted to n-type, forming a conducting channel between the N^+ source and drain. If there is a voltage difference between them, an electron current will flow from the source to the drain.

The gate voltage at which the inversion layer is formed ($\psi_s = 2\phi_B$) can be expressed in the ideal MOSFET (e.g. without interface and oxide charges) by the following expression [16]:

$$V_{TH} = V_{FB} + 2\phi_B + \frac{\sqrt{2\varepsilon_0\varepsilon_{SiC}qN_A(2\phi_B)}}{C_{ox}} \quad (1.4)$$

Where V_{FB} is given by eq 1.3 and N_A [cm^{-3}] is the acceptor density of the p-well.
The general expression for the drain current is given by [17]:

$$I_D = \frac{W}{L}\mu_n C_{ox}\left\{\left(V_G - V_{FB} - 2\phi_B - \frac{V_{DS}}{2}\right)V_{DS} - \frac{2}{3}\frac{\sqrt{2\varepsilon_{SiC}qN_A}}{C_{ox}}\left[(V_{DS}+2\phi_B)^{3/2} - (2\phi_B)^{3/2}\right]\right\} \quad (1.5)$$

where μ_n [cm^2/Vs] is the mobility of electrons (n-MOSFET) in the inversion channel.

Eq. 1.5 predicts the different working regions of a MOSFET for a given V_G; when $V_G<V_{th}$ but V_G is high enough to drive the surface in weak inversion (sub-threshold region). Then, for $V_G>V_{th}$ and $V_{DS} << (V_{GS}-V_{TH})$, the drain current increases linearly with drain voltage (the linear region) in this region the inversion channel has a uniform thickness and behaves as a variable ohmic resistance. Gradually, as V_{DS} increases, $V_{DS} < (V_{GS}-V_{TH})$, the space charge region extends, repelling he mobile charge carriers (the nonlinear region). It will happens until reaching the pinch-off point where $V_{DS} = (V_{GS}-V_{TH})$. Finally, beyond the pinch-off point, when $V_{DS} >> (V_{GS}-V_{TH})$, the drain current saturates (the saturation region). The nMOSFET configuration and the different working regions can be seen in Figs. 1.8 (a) and (b) respectively.

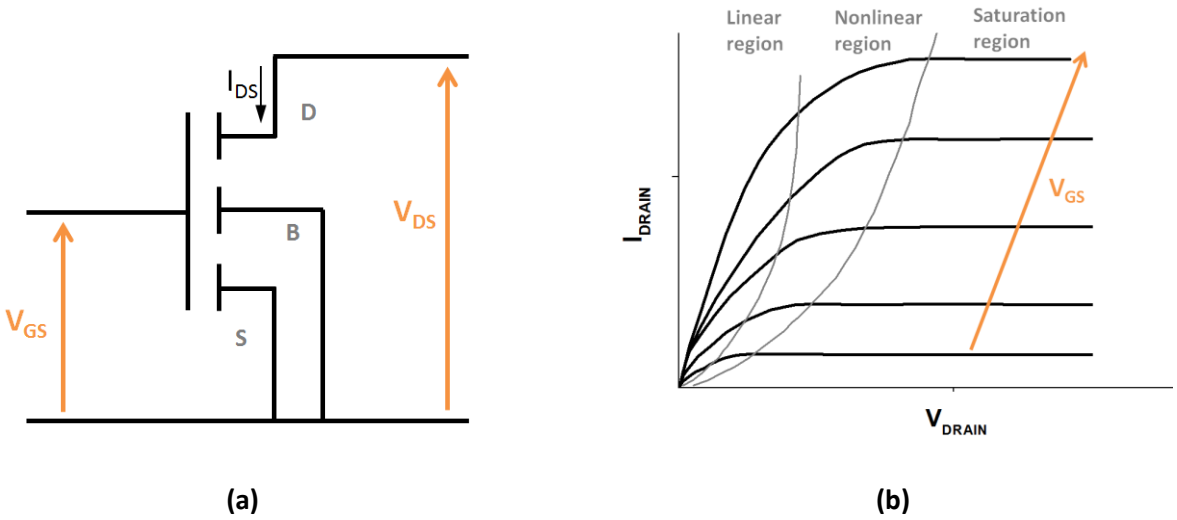

Figure 1.8 (a) n-channel MOSFET configured in the common source mode. The input voltage is V_{GS}, and the output voltage, V_{DS}. The output current is I_{DS}, and the gate current is typically negligibly, so the DC input current is assumed to be zero. (b) Output current characteristics.

The on-resistance (R_{ON}) of an n-MOSFET is determined by various contributions along the path of electrons: Source contact resistance (R_{sc}), Drain contact resistance (R_{dc}), Source resistance (R_{so}), Drain resistance (R_d) and Channel resistance (R_{ch}).

A large contribution to the R_{ON} is the R_{ch}, which value in a MOSFET inversion layer is given by:

$$R_{ch} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_G - V_{TH})} \tag{1.6}$$

where C_{ox} is the oxide capacitance, V_G is the applied gate voltage and V_{th} is the threshold voltage. The R_{ON} of a power MOS strongly depends on the channel mobility. The high D_{it} at SiO_2/SiC interface results in a low inversion channel electron mobility and thus high R_{ch}.

1.6 Present challenges

There are several technological solutions focused on the improvement of the SiC MOS interface. The main target is to increase the channel carrier mobility [18]. Specifically, regarding mobility in the MOSFET channel, two ranges of operation have to be considered, one at relatively low electric field, just above V_{th} (typically 5 V), and a second regime at higher electric field, for MOSFET gate voltages of 15–25 V. The latter is especially relevant for power electronics converters as it corresponds to the gate operation voltage of the devices.

The channel mobility values can be extracted by different methods, coming from Si technology: a) effective channel mobility (μ_{eff}) is extracted from output curves (dI_{DS}/dV_{DS}), b) field effect mobility (μ_{fe}) is extracted from transfer curves (dI_{DS}/dV_{GS}), and c) hall mobility (μ_{Hall}) is extracted under magnetic field using Hall laws. However, in SiC, the electrons in the inversion layer are trapped by the high amount of traps near and at the interface, this fact strongly affects the extraction of an accurate μ value [19]. Accordingly, the concept of apparent channel mobility would better reflect the mobility extracted from the measurements. In the literature, most of the reported mobility values for SiC MOSFET test structures are specifically μ_{fe}. But experimentally, the μ_{fe} versus gate voltage (or electric field) curve typically shows a peak maximum just after V_{th} is reached. Then, μ_{fe} decreases when increasing gate voltage (increasing vertical electric field). This behavior will be carefully discussed latter in this work, yet eventually, the μ_{fe} peak value can be much higher than the μ_{fe} values at high fields. When considering a possible technological solution for MOSFET improvement, this behavior must be also taken into account. While in Si technology μ_{eff} is usually a factor 2.5 lower than the bulk mobility, in SiC this difference is not only larger but it depends on the substrate crystallographic structure; i.e. SiC polytype.

Nowadays, the two main technological challenges for SiC MOS technology are:

1) to increase the n- inversion channel mobility

2) to reach a gate high stability and operational reliability

This thesis is mainly focused on two aspects of these SiC challenges; find optimal dielectric processes and configurations to increase the channel mobility and the V_{th} instability study.

In order to have a deep understanding about the change in the mobility values, it is very important to know the SiC/SiO_2 interface properties and the interface traps main characteristics. A proper modelling for μ also needs to account for several types of physical scattering effects and the electron trapping effect. Furthermore oxide traps are also affecting the V_{th}, producing changes in its value and stability.

Having into account all this knowledge, different strategies have been carried in order to reduce the traps inside and near the SiC/SiO_2 interface. On the one hand strategies based on nitridation processes are studied such as how different N treatments account in different interface qualities. On the other hand, very good results have also been obtained by doping the gate dielectric (and the interface) by different species as P, B or some alkaline earth elements as Ba, Sr, Cs or Rb.

In addition to the poor quality of the SiC/SiO_2 interface, a drawback of SiO_2 is its low dielectric constant, (k=3.9) which is approximately 2.5 times lower than that of SiC material (Table 1.1), obtaining a proportionally larger electric field enhancement in the dielectric medium compared to that in the semiconductor layer. For this reason, a great deal of effort is put in the study of new dielectrics with higher dielectric constant both in Si and in SiC [11, 21]. High-k gate dielectric materials reduce significantly the amount of electric field with equal gate dielectric thickness and hence the total gate current density. These strategies are deeply explained in Paper I included in Chapter 4.

1.6.1. SiC/SiO_2 interface and interface traps

Up to now, it's known that the flow of the charge carriers through the MOSFET conduction channel is reduced due to structural defects either in the dielectric layer (oxide bulk) or at the SiO_2/SiC interface. Hence the channel mobility is reduced. The active traps formation process details are not still completely understood since they can be of several types. It's pointed up that the creation of electrically active traps is due to whether O vacancies in the SiO_2, Si vacancies, interstitial C clusters, C vacancies in the SiC surface or a high strain in the SiC/SiO_2 interface. The different types of charges in a MOS structure [22] and their arrangement are schematically represented in Fig. 1.9.

In Si technology it is assumed that interface traps, located at the Si/SiO_2 interface, can easily exchange charge with majority carriers from the bottom of E_C or from the top of the semiconductor E_V. On the other hand, in addition to to this density of interface traps (D_{it}) it was suggested that near interface oxide traps (NIOTs) residing in close proximity to the Si/SiO_2 interface with the semiconductor surface can also exchange charge with the substrate [23]. Since both kind of traps (interface and near interface traps) have a

very similar behavior on modifying the MOS device characteristics they are commonly grouped and simply referred by authors as “interface traps”.

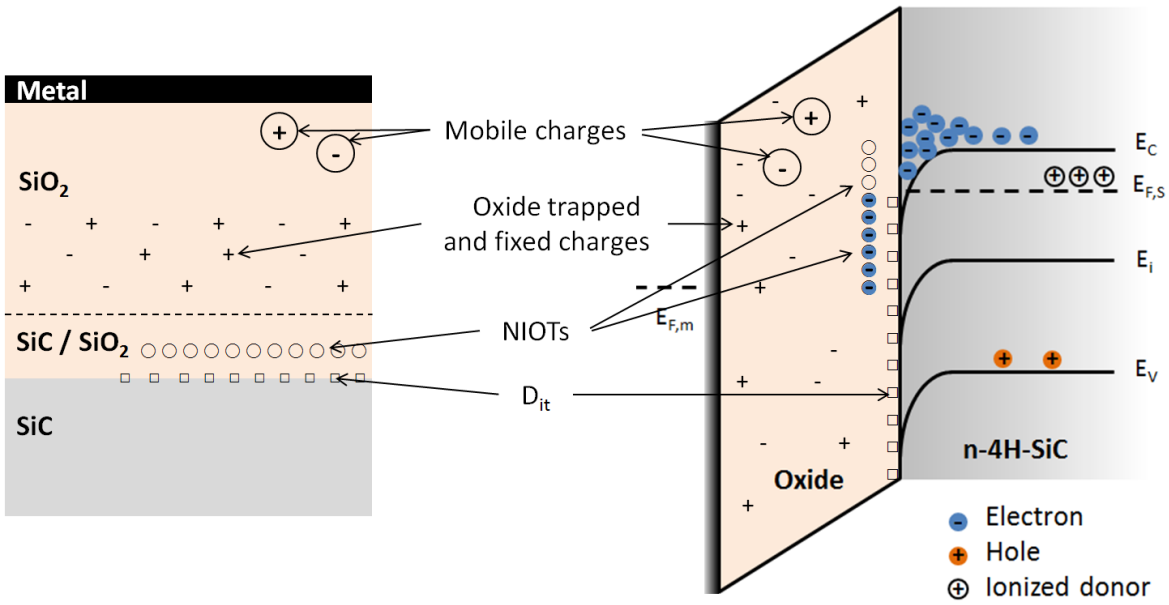

Figure 1.9 Schematic representations of the charges present in the SiC MOS interface.

1.6.2. Scattering mechanisms

The channel mobility (n-channel) in the linear region is usually estimated from the following equations [24]:

Field effect mobility μ_{fe}:

$$\mu_{fe} = \frac{L}{WC_{ox}V_D}\frac{dI_D}{dV_G} \tag{1.7}$$

Effective mobility μ_{eff}:

$$\mu_{eff} = \frac{L}{WC_{ox}(V_G - V_T)}\frac{dI_D}{dV_D} \tag{1.8}$$

Where I_D and V_D are the drain current and drain voltage, respectively. L and W are the channel length and the channel width, respectively.

Several physical scattering effects are limiting the mobility value in 4H-SiC MOSFETs. The impact is different depending on the applied gate voltage (or electric field). According to the Matthiessen’s rule [25], the total inversion layer mobility can be described by:

$$\frac{1}{\mu} \cong \sum_i \frac{1}{\mu_i} \tag{1.9}$$

Where μ_i depends on different scattering effects: commonly μ_C represents the mobility limited by the Coulomb scattering, μ_{SR} by the roughness scattering and μ_{AC} by the acoustic phonon scattering. These values are determined by:

$$\mu_C = \frac{T}{N_T}\left(1 + \frac{N_S}{N_{scr}}\right)^{\zeta_C} \tag{1.10}$$

$$\mu_{SR} = \frac{\delta}{E_{eff}^2} \tag{1.11}$$

$$\mu_{AC} = \frac{A}{E_{eff}} + \frac{B}{T \cdot E_{eff}^{1/3}} \tag{1.12}$$

where N_T is the trapped charge, T is the temperature, N_S is the surface inversion carrier concentration and N_{scr}, ζ_C, δ, A and B are empirical parameters which can be found in literature [26, 27].

The physical mechanisms involved in surface carrier scattering that accounted for the mobility behavior in Si MOSFETs, when $V_G > V_{th}$, were accepted to be at least 3 [28]:

1) Phonon scattering due to the various modes of lattice vibration including surface acoustic phonons and optical phonons [29]. This was considered negligible at low temperature values.
2) Coulomb scattering due to charged centers, including fixed oxide charge, interface-state charge, and localized charge due to ionized impurities [29, 30].
3) Surface-roughness scattering caused by the deviation of the interface from an ideal plane [31, 32].

These thoughts have been transmitted from Si to SiC MOSFETs, but there is not a complete agreement about what and when are the dominant scattering effects limiting the 4H-SiC MOSFETs mobility. In SiC MOSFETs it's commonly thought that roughness surface scattering becomes dominant at high effective electric field [19]. However, recent works [27, 33] concluded that surface roughness scattering is not limiting the inversion channel mobility in standard MOSFETs. Katsuhito et al. proposed an improved mobility model, which seems to perfectly agree with the experimental results. This model takes into account optical phonon scattering (μ_{OP}), which is defined as:

$$\mu_{OP} = \frac{C}{E_{eff}} \cdot \left[exp\left(\frac{\hbar\omega_{OP}}{kT}\right) - 1\right] \tag{1.13}$$

where C is an empirical parameter [27].

Fig. 1.10 shows the modelling of the different scattering phenomena versus the applied electric field at two different temperatures.

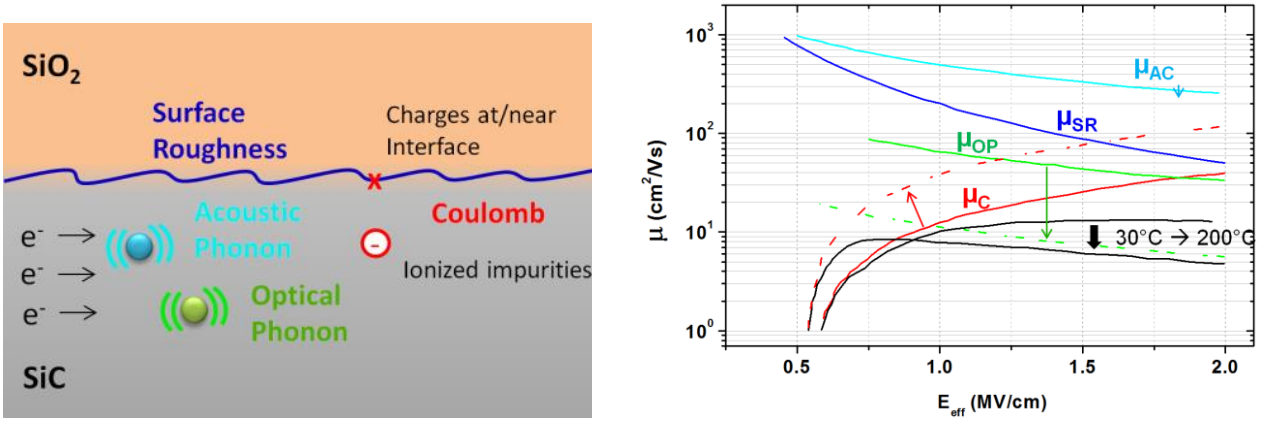

Figure 1.10 (a) Schematic on electron scattering limiting factors.(b) Calculated inversion channel mobility at 30°C and 200°C. Figure adapted from [27].

Assuming that μ_{OP} dominates mobility behavior at high electric field, it's needed to think about what is happening at low electric field values (near V_{th}). When using Eq. 1.7 and Eq. 1.8, one is assuming that all the electrons in the inversion layer are mobile, traveling in the conduction band from the source to the drain. However, it must be taken into account that, differently from Si, due to the high interface state density in SiC structures (10^{12} cm^{-2}), several electrons will be trapped at interface states, becoming immobile electrons. The amount of trapped electrons could be higher than the % of induced electrons able to travel through the channel and contribute to the drain current. By increasing temperature, more and more electrons are excited to the conduction band, and become mobile. For this reason the channel mobility of 4H-SiC (0001) MOSFETs with thermal dry or wet oxidation show a positive temperature coefficient (increases at elevated temperature). For this reason, "Coulomb scattering" is a deceptive explanation for the mobility-limiting factor at low electric field values. A more correct term would be thermally activated transport or "*electron trapping effect*" [19].

1.6.3. Increase the channel mobility

One of the technological concerns that affect the behavior of 4H-SiC MOSFETs is their low μ_{fe}. This limitation becomes particularly relevant for the development of 4H-SiC MOSFETs devices operating below 1kV, for which μ_{fe} represents the most important contribution to the total on-resistance (R_{ON}) of the device.

It is important to take into account that reported mobility and D_{it} values strongly depend on the method and on the test structure used for parameter extraction, particularly when comparing results in different papers of the literature. Furthermore, extracted μ_{fe} values decrease when 1) the channel length decreases,

2) the surface doping is increased, and 3) the p-type doping is done by implantation instead of epilayer growth.

It is known that the amount of D_{it} and NIOTs at the SiO_2/SiC interface limits μ_{fe} in 4H-SiC MOSFETs processed with dry or wet oxidation [34, 35]. Nitridation processes are the most common and widely studied technological strategies developed for reducing D_{it} and NIOTs, allowing the technology advance to commercial high performance SiC MOSFETs. Nitridation process consists in complete or partial growth of the gate oxide in the presence of a N-containing gas. The introduction of N at the SiO_2/SiC interface has been proved to reduce D_{it} below 10^{12} $cm^{-2}eV^{-1}$ near the E_C edge by using POA in NO [14] or N_2O [36] and thus increases μ_{fe}. Fig. 1.11 illustrates the three most common processes followed to build up nitrous oxides; the oxide can be directly grown in N ambient at high temperature, or alternatively, a dry thermal oxide can be submitted to a POA in an ambient with N.

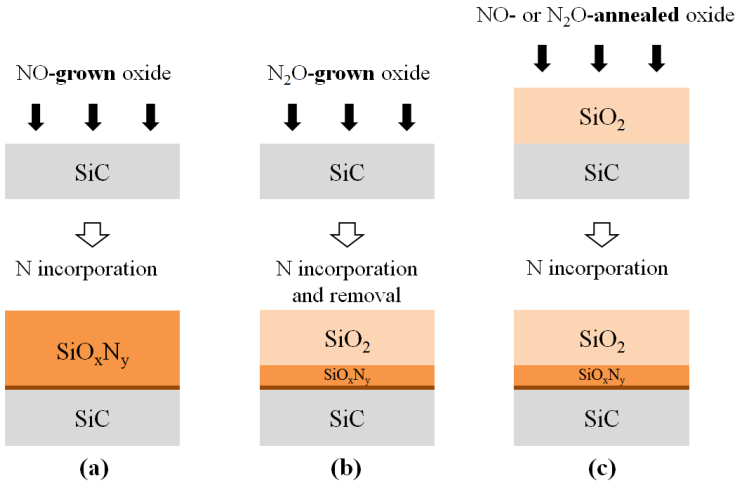

Figure 1.11 Different nitridation processes for (a) NO-grown oxide, (b) N_2O grown oxide, and (c) NO- or N_2O annealed oxide.

As for its comprehension, at high temperature, N_2O decomposes into small percentages of NO and a large percentage of N_2 and O_2. The latter (N_2 and O_2) become undesired byproducts as they lead to competing reactions which hinder the N incorporation process at the SiO_2/4H-SiC interface. In consequence, NO treatment is considered more effective than N_2O treatment. However, main drawback of NO for processing is its high toxicity. Results of NO annealing in SiO_2/SiC [35, 37] found that nitrogen is incorporated mainly at the interface, therefore being very efficient in reducing D_{it}. The higher the N concentration at the interface, the higher the channel mobility.

In order to promote the N incorporation into the oxide and avoid the saturation effect due to oxygen competition some alternative methods without oxygen have been proposed have been suggested to promote the N incorporation into the oxide. This methods consisting in POAs in N_2 environment [38-40], ammonia (NH_3) nitridation [41-43] or N-plasma nitridation [44, 45]. Their main characteristics are summarized in Table 1.2. and also explained in Paper I.

Nitridation process is commonly used in the production of commercial power MOSFETs. It must be highlighted that the most tried and accepted process in commercial devices consist of performing a POA of 1175 ° C in NO to the gate oxide. In spite of the μ_{fe} increase obtained by nitridation, the mobility values are still rather low (less than 5% of the bulk mobility) and it is thought that the maximal improvements provided by nitridation have been reached. Consequently, alternative methods for a further μ_{fe} enhancement have been addressed. Several of those approaches consist of doping the gate oxides by the introduction of different ions. Some relevant results are shown in Table 1.2.

Although Table 1.2 can be used to have a general view of the oxide process impact in 4H-SiC MOS and MOSFETs performance, the reported values are not 100% comparable each other; different methods of D_{it} extraction (with their different limitations) may therefore underestimate or overestimate the value of D_{it} reported in each case. In addition although we provide the D_{it} value near the conduction band (E_c-E = 0.2eV), not always the data of the original papers are so clear, or so specific. Likewise, the analyzed transistor dimensions vary from one work to another, which can affect in the obtained mobility values. More details either in nitridation or in doped gate oxides can be found in the attached Paper I and in [46].

In addition when choosing a dielectric it is necessary to take into account its application, because some of the techniques considered in Table 1.2, especially those that involve ion doping, often result in a reduction in the value of the breakdown voltage or the appearance of V_{th} instabilities.

Finally, it should be added that there are a large number of studies made with high-k dielectrics or compound oxides which have not been considered when doing this Table 1.2.

Table 1.2 Comparison of the impact of different oxidation processes on the electrical properties of 4H-SiC MOSFET and MOS capacitors. Including D_{it} and μ_{fe} values obtained at E-Ec=0.2eV.

Main Process	Main oxidation treatment	Post oxidation treatment	μ ($cm^2V^{-1}s^{-1}$)	D_{it} ($cm^{-2}eV^{-1}$)	Reference
Dry	O_2 1200°C Ar 950°C	-	6-8	$5x10^{11}$ - $9x10^{12}$	[47, 48]
Dry	O_2 1400°C Ar 1400°C	-	2	N/D	[49]
Dry	1500°C (7%O2, 93%Ar)	-	40	2-6 $x10^{12}$	[50]
Dry	O_2 600°C ALD Al_2O_3	-	81	10^{11}	[51]
Wet	Wet 1150°C Ar 1150°C	-	40	2 $x10^{12}$	[52]
NO	1100°C -1250°C (dry or wet)	1175 °C in NO **Used in most commercial devices**	25-40	1-5 $x10^{12}$	[53-56]
N_2O	H_2 800°C N_2O 1050°C Ar 1100°C	-	32	4 $x10^{11}$	[57, 58]
N_2O	PECVD ≈400°C	N_2O 1150°C	24-40	4-8 $x10^{11}$	[33, 59]
N_2O	O_2 1200°C Ar 950°C	N_2O 1200°C -1300°C	20-25	8 $x10^{11}$	[47]
N_2	Dry 1150°C	N_2 1350°C -1400°C	N/D	1-2$x10^{12}$	[38, 39]
N_2	Dry 900°C	N_2 1300	50	$2x10^{11}$	[40]
NH_3	Wet 1100°C	NH_3 1050°C -1175°C	N/D	10^{12} - $8x10^{11}$	[41-43]
Nitrogen plasma	Dry 1150°C	N_2 plasma 1160°C	50-60	4 $x10^{11}$	[44, 45]
P doping $POCl_3$	Dry 1100°C Dry 1200°C	$POCl_3$ 1000°C $POCl_3$ 1000°C	89 -	$9x10^{10}$ $2x10^{11}$	[60] [61]
P doping P_2O_5	Dry 1150°C	P_2O_5 1000°C	80	$3x10^{11}$	[62]
P ion implantation	P implantation Dry 1150°C	-	N/D	1 - $4x10^{12}$	[63]
P ion implantation	P implantation PECVD	N_2 1150°C	N/D	10^{11} - 10^{12}	[64]
B Doping (Dry)	Dry 1200°C	BN 950°C	102	10^{11}	[65]
B Doping (N_2O)	N_2O 1050°C	BN 1100°C	160	$2x10^{11}$	[66]
B Doping (Dry) + Sb	Sb implantation Dry 1150°C	B_2O_3 950°C	180	10^{12}	[67]
Sb doping	Sb implantation Dry 1150°C	-	80	N/D	[68]
Sb doping	Sb implantation	NO 1175°C	110	N/D	[68]

(NO)	Dry 1150°C				
Ba doping	Ba deposition	-	110	$3x10^{11}$	[69]
Sr doping	Sr deposition	O_2/N_2 > 950°C	65	N/D	[69]
La (N_2O)	La deposition ALD	N_2O 900°C	133	$2x10^{12}$	[70]
(11$\bar{2}$0) (Wet)	Wet 1150°C Ar 1150°C	-	32	1 $x10^{12}$	[71]
(11$\bar{2}$0) (Dry)	Dry 1050°C PECVD	-	156	1-4 x $x10^{11}$	[72]
(11$\bar{2}$0) (H_2)	Wet 1150°C Ar 1150°C	H_2 800°C	110	1.4 $x10^{11}$	[71]
(11$\bar{2}$0) (NO)	Dry 1150°C	NO 1175°C	85	$3x10^{11}$	[73]
(11$\bar{2}$0) P doping	Dry 1150°C	P diffusion 1000°C	125	6 $x10^{11}$	[73]
(03$\bar{3}$8) (Wet)	H_2 1000°C Wet 1150°C Ar 1150°C	-	10.6	5 $x10^{11}$	[74]
(03$\bar{3}$8) (N_2O)	N_2O 1300°C	-	11	10^{12}	[75]
(03$\bar{3}$8) (NO)	Dry (undisclosed T)	NO (undisclosed T)	80	3 $x10^{11}$	[76]

In Table 1.2 "dry" indicates that the oxidation is done in an O_2 environment, while we refer to "wet" when H is present in the oxidation process.

1.6.4. V_{th} value

As introduced before, a big issue in SiC MOS technology is related with having a gate high stability and operational reliability. Although several of the processes summarized in Table 1.2 show promising D_{it} and μ_{fe} values, many times, especially when working with doped oxides, the stability of the devices is compromised, discarding the process for a commercial use.

V_{th} instability mechanism

It is for this reason that a correct characterization of the V_{th} and its stability becomes a very important step in the characterization of a gate oxide. Either in this thesis or in any other work.

Apart from the existence of mobile ions, there are two dominant mechanisms affecting the V_{th} stability in MOSFETs [77, 78]:

1) Oxide trap activation

2) Oxide trap charging via a tunneling mechanism (charge injection)

The phenomenon of charge trapping in SiO_2 is related with the differences in electron and hole mobility in the SiO_2. If holes or electrons are generated inside the oxide or injected from the interfaces, most of the holes will be trapped within the bulk of the oxide layer while electrons will remain trapped at the SiC/SiO_2 interface. Moreover, the displacement rate of holes in the oxide is much lower than the electron's one. The mechanism is as follows. The trapped positive charge (holes in the oxide) accounts for a negative shift of V_{th}. However, this negative V_{th} shift can be compensated under positive gate biasing since electrons coming from the channel may tunnel into the oxide, i.e. forming a charge-neutral dipole. Then, if a negative gate bias is subsequently applied, electrons can tunnel back and move out from the oxide into the SiC substrate, causing again a negative V_{th} shift by the uncovered positively charged oxide traps. This sequence is repeatable and reversible at room temperature, although the V_{th} instability increases during a bias-temperature stress at temperatures above 150 °C. This further V_{th} instability increase is likely due to the activation of additional traps in the oxide, with activation energies of about 1.1 eV.

Yet, when the oxide trap activation is less important, the V_{th} shift generally exhibits a time dependence response to the bias stress since the oxide-trap charging occurs via a direct tunneling mechanism. In this case, charge trapping is mainly attributed to NIOTs which can change their charge state very quickly. Consequently, the testing time sequence, the time taken to measure the effect of a stress or a long duration of an applied bias when measuring, greatly affects the type of phenomena which is observed.

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Chapter 2

Experimental methods

MOSFETs and other test structures fabrication, which technology is shown in this chapter, was mainly carried out in the CNM clean room facilities. Similarly much of the final devices characterization was performed in the CNM laboratories. Some special oxidation processes and specific characterization methods have been outsourced, giving rise to several collaborations, which will be detailed in the corresponding sections.

In this chapter we will give a complete overview on the experimental methods used along this thesis, including the process technology involved for MOS and MOSFETs fabrication and their electrical characterization.

2.1 Fabrication

2.1.1 Mask Design

For the MOSFET transistor manufacture, we first draw a new set of photolithographic masks including different structures, geometries and designs. This mask set, named SiC039, is shown in Fig. 2.1.

The masks set [Fig. 2.1] consists of 8 photolithographic levels as follows:

1. Alignment pattern. This step is the first one, because the high temperature anneal does not allow the use of conventional reference patterns (SiO_2) required for the alignment of the following masks. However, this also permits changing the mask sequence for the manufacture of different process configurations.
2. P-well implantation mask (not used if starting material is p-type epitaxied).
3. P^+ implantation mask for the definition of bulk contact on Lateral MOSFETs
4. N^+ implantation mask for the definition of source and drain of the MOSFETs devices.
5. Gate active area definition (when field oxide is used).
6. Drain/Source contacts opening through the gate oxide.
7. Drain and Source contacts metallization pattern.

8. Gate metallization pattern.

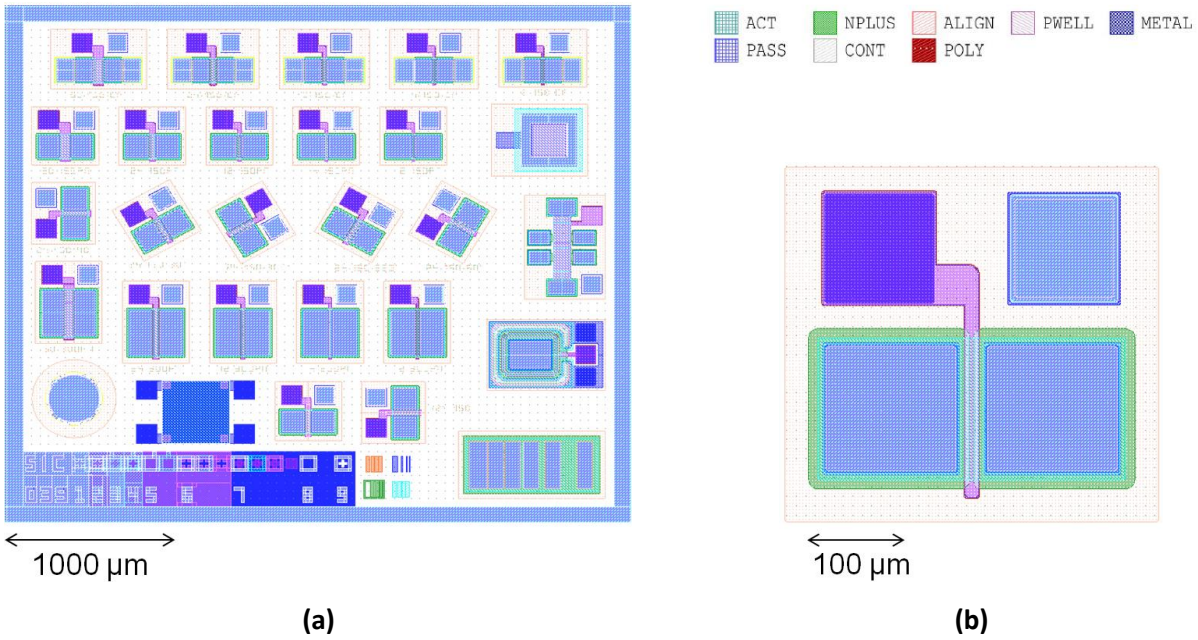


Figure 2. 1 Masks layout showing a monitor chip (a) and the layout for a single lateral MOSFET (b).

In summary, the following devices are incorporated into the layout (from top to bottom and from left to right):

- 5 MOSFETs with Charge Pumping design and L/W (µm) =50/150, 24/150, 12/150, 4/150, 2/150;
- 5 MOSFETs with L/W (µm) = 50/150 (SiC039), 24/150, 12/150, 8/150(SiC009), 4/150, 2/150;
- 1 lateral MOS capacitors on the epilayer and the P-well region, with an area of 200 × 200 μm^2;
- 5 MOSFETs with L/W (µm) = 24/150, and different twist versus main flat orientation= 90°, 30°, 300°, 330°, 60°;
- 1 Hall effect MOSFET;
- 5 MOSFETs with L/W (µm) = 50/300(SiC039), 24/300, 12/300, 8/300(SiC009), 4/300, 2/300;
- 1 rectangular MOSFET with W = 1 mm;
- 1 circular Diode,
- 1 Hall test structure;
- 2 VDMOS devices with L/W=24/150µm;
- Alignment structures;
- 1 TLM structure;

In Fig. 2.2 are shown some images from the final fabricated devices on a 4 inch 4H-SiC wafer; It can be seen a complete processed wafer (a), the microscope image of a monitor chip (b), and two SEM images of the sidewall of a cleaved sample, showing the total wafer thickness (c), and the different stacks in the MOSFET channel region (d).

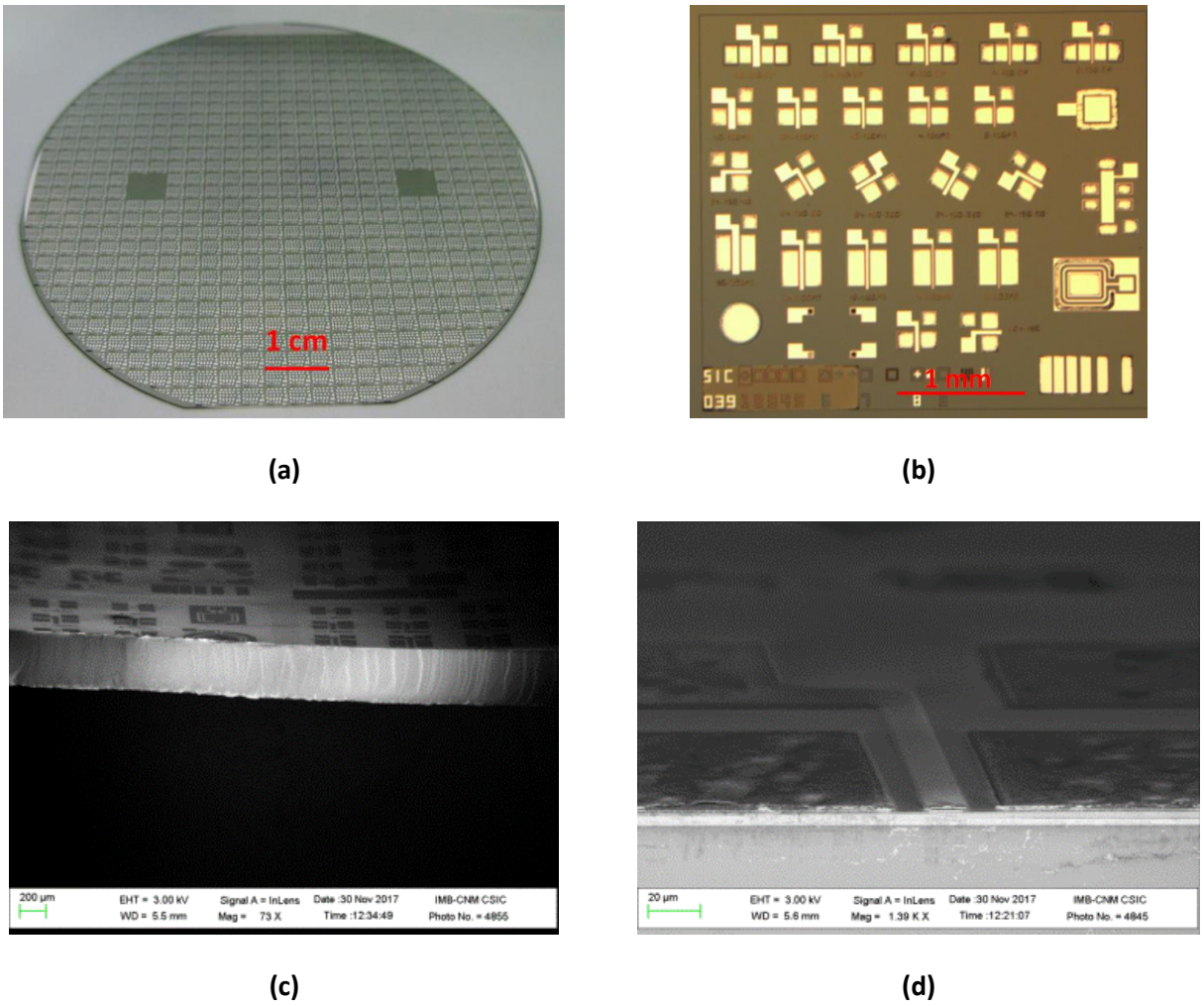


Figure 2. 2 4 inch 4H-SiC wafer processed (a), obtained image by an optic microscope (b), SEM cross section image of the wafer (c) and SEM, cross section images of a MOSFET (d).

2.1.2 Overview of process technology approach

Despite all SiC advantages mentioned in Chapter 1, two main problems remain and are dependent on each other: The low inversion channel mobility values and high threshold voltage instability. Both limitations are partially related with a poor quality of the SiC/SiO_2 interface after SiO_2 growth process. However, those

problems point out the importance of various other manufacturing steps, including bulk and epitaxy crystal growth, implantation step, surface preparation and oxidation process.

Then, a SiC MOSFET manufacture contains a certain number of key-technological steps listed below:

- SiC substrate manufacture.
- Epitaxy with the appropriate mastering of the required doping level, surface roughness and defects density.
- Implantations and post implantation annealing.
- Oxidation and interface state defect reduction.
- Photolithographic steps with a proper critical alignment.
- Metallisation and contact resistance reduction.

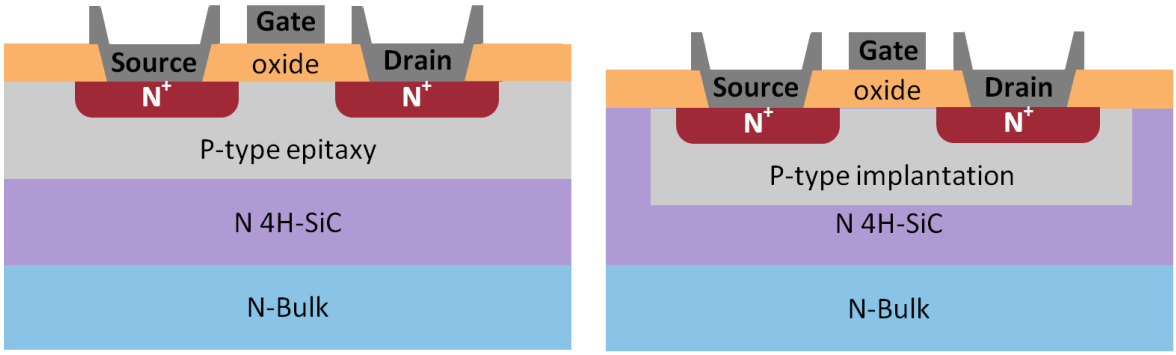


Figure 2. 3 Cross section of a lateral MOSFET structure including the key technological steps. A lateral MOSFET with P well epitaxy (a) or with P well implanted (b). Schematics not to scale.

The cross section of the MOSFET processed on P-epilayer or on implanted P-well are schematically showed in Fig. 2.3. A detailed description of the fabrication process and schematics of all the steps followed to make a MOSFET during this thesis can be found in Appendix (MOSFET fabrication process).

Despite the SiC device fabrication process sequence is pretty similar to that on Si technology, several specific process steps with particular requirements are needed, due to the unique physical and chemical properties of SiC.

Regarding doping by ion implantation, one must take into account the low diffusion coefficient of dopants in SiC, the abnormal diffusion of B atoms in p-type implantations, showing a resistive tail, and the high temperature required in post-implantation annealing for the dopants activation.

Concerning etching, the SiC is an extremely inert material against chemicals. This is a problem for etching and also for other procedures: for instance, while in Si it is quite easy to dye the N+ implanted areas to observe them by SEM looking at the MOSFET cross section, this staining is impossible to perform in 4H-SiC samples. In our case, the N^+ implantation (corresponding to drain and source) has been checked by SEM microscope images where, depending on the sample composition, the observed contrast provided by primary electrons changes (as shown in Fig. 2.2 (d)).

From the main relevant issues in a SiC MOSFET fabrication listed above, this thesis focuses on the oxidation improvement and the reduction of the interface state defects density.

Figure 2.4 shows the initial SiC oxidation process used in our research group since previous PhD thesis [1]. It consists on a rapid thermal oxidation (RTO) in N_2O nitrous oxide environment, with a surface pre-treatment cleaning by H_2 at 800°C for 120s, and a final annealing in Argon. The H_2 annealing at high temperatures is believed to reduce the D_{it} due to the passivation of C-dangling bonds [2].

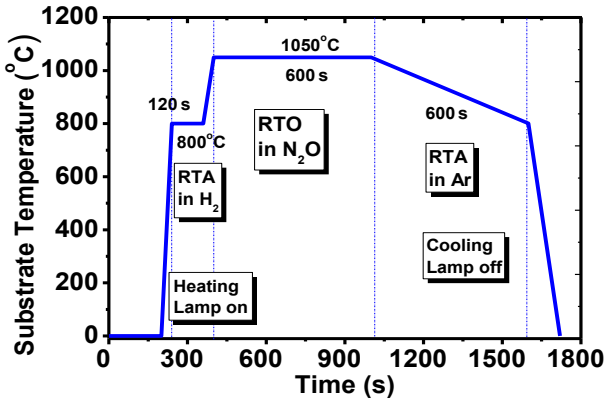


Figure 2. 4 SiC oxidation process developed previously in our research Group [1].

During this work we have also manufactured MOSFETs with oxides grown on NO environment, supplied by ABB-CRC (Switzerland) and Griffith University (Australia) laboratories.

In order to improve the interface quality (reduction of D_{it} and NIOTs and hence, increase the MOSFETs mobility value), our main proposal is to study a boron diffusion process done through the gate oxide, as schematically shown in Fig. 2.5, SiC samples with a thermally grown SiO_2 layer, are located between BN planar sources at temperatures between 1050°C and 1150°C during 30 min. In some cases, a thin TEOS oxide (50nm) is deposited on top after the boron doping process (see Appendix), in order to avoid boron out-diffusion and increase the device robustness.

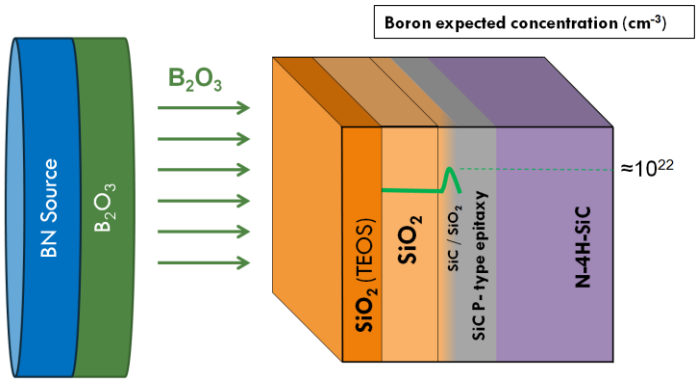


Figure 2.5 Schematics of the boron doping procedure.

2.1.3 Main issues during processing

Due to the topic of this thesis, the main challenges we faced with are related with the oxidation process, the oxides dielectric properties and the final interface characteristics. Regardless SiC is the only WBG semiconductor that as Si, thermally oxidizes to SiO_2, as explained in Chapter 1, the resulting oxide on SiC is not free of carbon, and its interface with the semiconductor is worse than that on Si. During the device fabrication one must also take into account that SiC oxidation rate strongly depends on the crystal face [3-5]. Indeed, on the most standard crystal orientation 4H-SiC (0001), the oxidation rate is the lowest, and much lower than in Si, especially under wet oxidation. Oxide thicknesses higher than 50nm require high oxidation temperatures (>1200°C) and very long oxidation times (several hours).

Another important fabrication issue we had to deal with was the metal adherence on the doped dielectrics (especially on top of the gate area). When the SiO_2 layer was highly doped with B, it becomes more hydrophilic, retaining much more water and resulting in a worse adherence with metals (also with photoresist as shown in Fig. 2.6). This poor adherence made very difficult to manufacture devices with highly doped oxides or with innovative high k dielectrics.

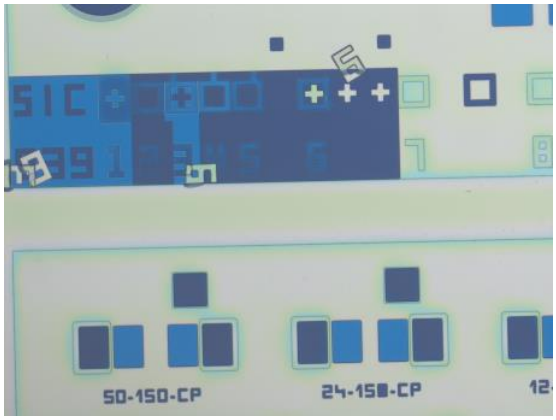


Figure 2.6 Picture showing how some photoresists structures (numbers) have taken off and moved respect their correct location.

Some of the corrective actions carried out to address these issues were:

- Very careful sample cleaning and drying (including dehydration baking steps).
- Use of adherence promoter before photoresist deposition. We use hexamethyldisilazane (HMDS), which functional groups Si-NH-Si react with the SiO_2, forming strong bonds to the surface. It is assumed that the remaining methyl will bond to photoresist.
- Leave the samples in a vacuum environment for some hours in the sputtering chamber before the Al deposition to ensure low water content.
- Reduction on gate metal thickness in order to reduce the metal surface strain.

Cutting 4H-SiC wafers by cleaving method into pieces is also quite tricky due to the hexagonal crystal structure. SiC crystals are very easy to break according to different crystallographic (or stress) planes than 0° or 90°, making difficult get regular and square/rectangular precisely cut portions, like usually obtained with Si.

Finally, as is shown in the following sections (Physical and Electrical Characterization), the SiC devices characterization methodology must be somehow different from that on Si due to the specific SiC properties. Electrical characterization must be different due to: Extremely low intrinsic carrier density and extremely low carrier generation, so no inversion layer is created in SiC MOS capacitance in reasonable test times; and the presence of very deep interface states due to its wide bandgap.

Despite all these difficulties, we have been able to process more than 80 samples properly to be characterized.

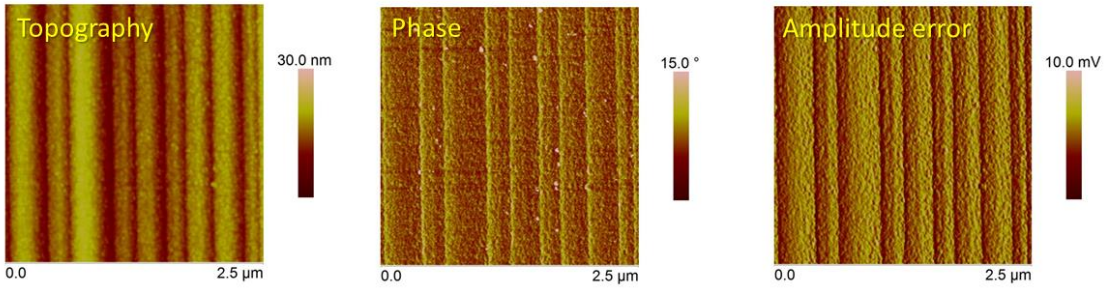
2.2 Physical characterization

In this and the following section (2.2 and 2.3) we will go through some state-of-the-art characterization techniques which have been used during this thesis. Although we have focused on 4H-SiC electrical characterization methods it must be highlighted the importance of the physical and structural characterization methods used during this thesis. I was directly involved in carrying out most of the measurements when the required equipment was available in self-service at CNM clean room facilities (AFM, perfilometer, SEM, EDX, ellipsometry), while other specific measurements have been done thanks to the project partners (XPS) or specialized companies (SIMS).

2.2.1 AFM (Nanoscope IV controller + Veeco Dimension 3100 head)

Using the CNM clean room Atomic Force Microscope (AFM), we are able to evaluate the sample surface quality. AFM allows obtaining very accurate values of the samples roughness. SiC terraces can be observed in detail. To measure high steps (> few 10nm) we have used a perfilometer instead of the AFM.
The AFM principle is based on a cantilever with a sharp tip that interacts with the sample surface and scans it. The AFM probe interacts with the substrate through a raster scanning motion. The up/down and side to side motion of the AFM tip as it scans along the surface is monitored through a laser beam reflected off the cantilever. A position sensitive photo detector (PSPD) can be used to track the probe motion. The raised and lowered features on the sample surface influence the cantilever deflection, which is monitored by the PSPD. The tip height with respect to the surface is controlled using a feedback loop which allows the AFM to generate a topographic map of the surface.

The AFM microscope allows us to measure the root mean square (RMS) roughness value of the surface as well as the SiC terraces (width and height). The amplitude, phase and topography error can be extracted. Images taken on one of our samples are shown in Fig. 2.7. Some of the RMS measurements obtained with AFM on non-processed epitaxied wafers were too high. In this case we decided to polish the wafers before processing them.



Surface roughness: R_q=3.26 nm , R_a=2.67 nm

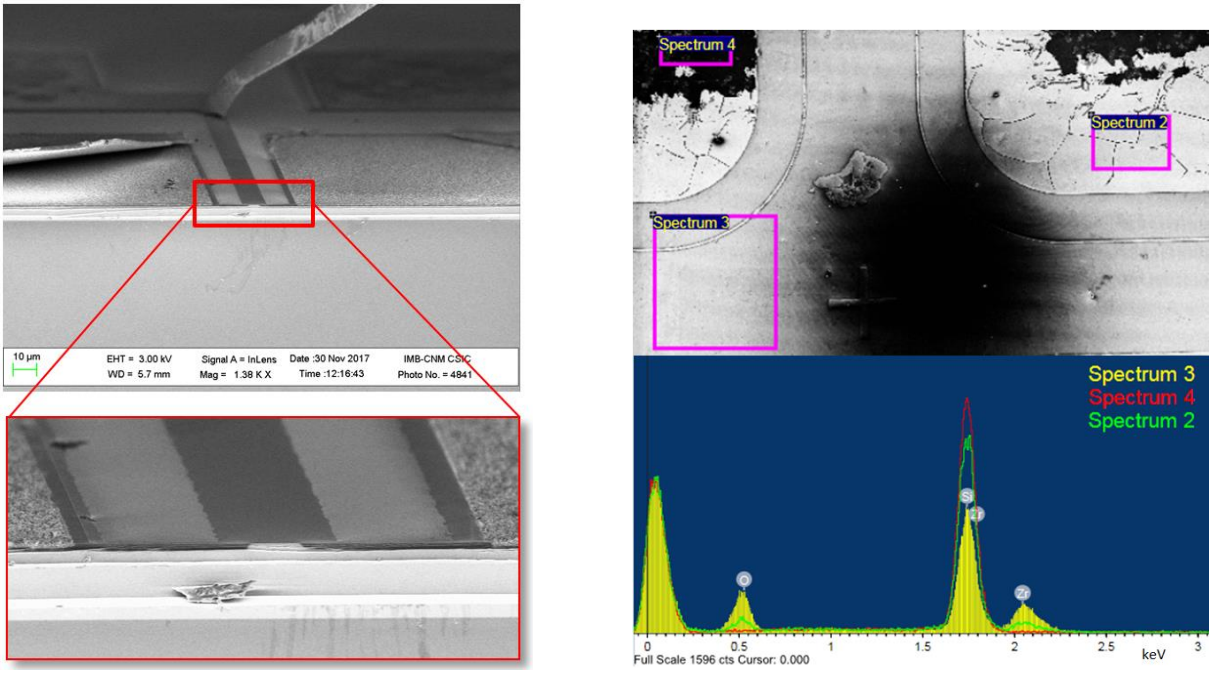
Figure 2.7 AFM image of a 4H-SiC initial wafer roughness on a 2.5µmx2.5µm area.

2.2.2 SEM/EDX (Zeiss Auriga 40/ Oxford INCA x-act)

A visual check of the devices surface at nanometers scale, at any fabrication step, can be done by Scanning Electron Microscope (SEM) available at CNM. This equipment also includes an Energy-dispersive X-ray spectroscopy (EDX) module which provides a qualitative measure of the atom species contained in the analyzed sample.

SEMs employ a focused beam of electrons in order to get data from a sample at the nanoscale. The electrons interact with atoms in the sample, producing various signals that contain information about their surface topography and composition. The main type of signals that are detected are the backscattered electrons (BSE) or commonly called primary electrons, and secondary electrons (SE), which allows generating a grayscale image of the sample at very high magnifications. However, there are many other signals which can be a product of the electron-matter interaction, and these can provide additional information about the sample. The EDX module uses the X-ray spectrum emitted by a solid sample bombarded with a focused beam of electrons to obtain a localized chemical analysis.

Using this technology we have been able to study the accuracy of device dimensions, as well as the Drain and Source implantation qualitative shape, and the composition of some of the new tested high-k dielectrics compounds.



(a) **(b)**

Figure 2.8 (a) SEM image obtained with a BSE signal of a MOSFET cross-section, where the aluminum has come off due to the cross-section polishing. (b) SEM image and EDX qualitative spectrum of several areas of the studied sample, which allows us to compare the dielectric composition on different location of the sample.

2.2.3 Spectroscopic ellipsometer (Horiba scientific Auto SE)

Spectroscopic ellipsometry is an optical method for the characterization of an interface or a film between two media. It is a non-destructive, non-contact, and non-invasive optical technique based on the change in the polarization state of light as it is reflected obliquely from a thin film sample. Spectroscopic ellipsometry measures ψ (phase) and Δ (amplitude), both of which describe the output elliptical polarization state after linearly polarized light is reflected obliquely off from a thin film sample. After collecting ψ and Δ, a model representing the thin film structure must be built in order to determine thickness and/or optical constants.

We use this technique to determine the thickness as well as the refractive index of our dielectrics used for MOS devices, at different steps of the fabrication process, for thicknesses from few nm to several microns. Measurements for most semiconductors are usually made with an incident angle around 70°-75°, but measurements on transparent materials like SiC are preferably made around 60°.

2.2.4 TOF-SIMS characterization (Ion TOF-SIMS IV, Vigo University)

Secondary Ion Mass Spectrometry (SIMS) technique is used to analyze the composition of solid surfaces and thin films. It consists in the mass analysis of charged particles (secondary ions) emitted from a surface that is bombarded by a pulsed primary ion beam of heavy particles. The main elements of a SIMS instrument are: a Primary beam source; a collecting method for the ejected secondary ions; a mass analyzer to isolate the ions of interest and an ion detection system to record the secondary ion signal magnitude.

In our case, the type of analyzer used to determine the mass of the sputtered ions was a time of flight detector (TOF-SIMS). The time of flight mass analyzer separates the ions in a field-free drift path according to their velocity. It is based on the fact that ions with the same energy but different masses travel with different velocities. Since all ions possess the same kinetic energy, the velocity and therefore the time of flight towards the detector varies according to the ion mass. It is the only analyzer type able to detect all generated secondary ions simultaneously, and is the standard analyzer for static SIMS instruments.

In this work, quantitative depth profiling of nitrogen, boron, phosphorous and carbon species in the as-grown oxide films have been investigated. The depths were quantified by measuring the craters depths by perfilometry. The measurement was performed by the nanotechnology and surface analysis service in the "Universidad de Vigo" on an IonTOF IV TOF-SIMS instrument. Its instrumentation consist of two canons, the primary is a bismuth metal liquid canon, and a secondary one, to realize the sputtering, is generating Cs^+ or O_2^+. Our TOF-SIMS measurements were performed at 25 KeV pulsed $^{208}Bi_3^+$ primary analysis Ion Gun. The flux of these primary ions is extremely low. As a result, the surface excitation by particle bombardment leads to the emission of secondary ions characteristic of the chemical composition in the upper monolayer. For each type of molecule, secondary ion emission results in a characteristic set of ionized molecular fragments with well-defined mass spectra. The time of flight from the sample to the detector was measured in a reflection mass spectrometer.

The main issue on our samples was a proper detection of the dielectric compounds. On the one hand, the proper gun for sputtering should be chosen: If we want to "track" the O, or O-rich ions, we should use the Cs+ canon; but the O_2^+ canon increases the ionization probability of electropositive species, being a better option for the B detection (while the Cs^+ increases the ionization probability in electronegative species as N, C or O). Any of the canons is a good option for detecting N and B at the same time, and then, study the B and N interaction at the SiC/SiO_2 interface.

Finally, it should be mentioned that the N detection by TOF-SIMS analysis became very difficult and not completely truthful for several reasons. In the first place, N weakly ionizes. So, we decided to try the detection of some N clusters, but there was a lot of interference / overlap with other species in the same nominal mass. For instance, the cluster $_{14}N_{30}Si$ (44 amu) coincides with $_{16}O_{28}Si$ (44 amu) or $_{28}Si_{14}N$ (42 amu) coincides with the ion $_{12}C_{30}Si$ (42 amu). In Fig. 2.9 are shown some of the species detected by TOF-SIMS analysis which can help us to understand where the B is located.

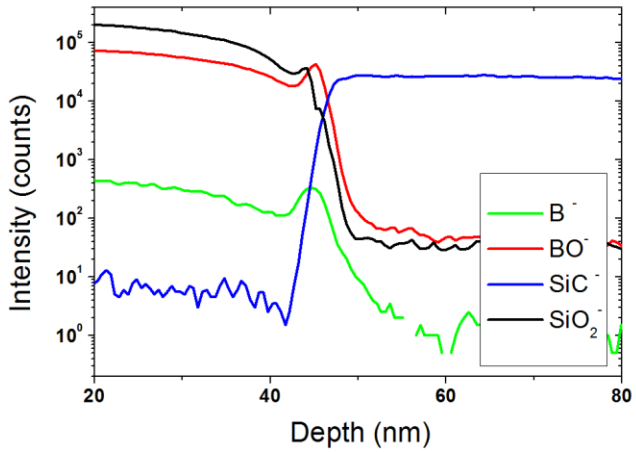


Figure 2.9 TOF-SIMS Intensity profile acquired in negative polarity vs depth for a boron doped oxide sample.

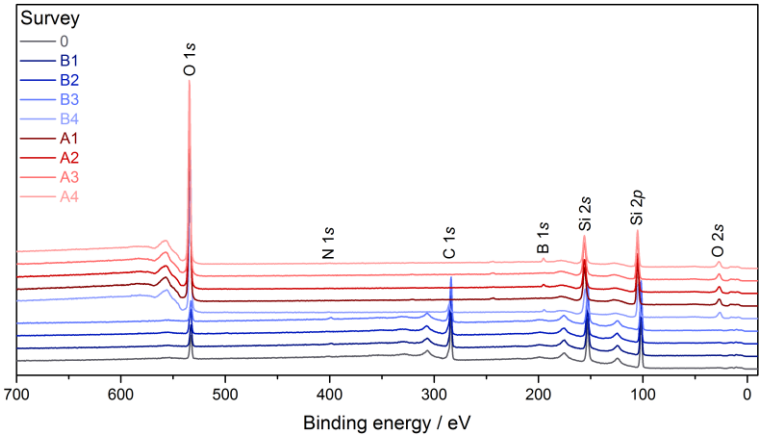
2.2.5 XPS Measurement (Scienta ESCA 300 spectrometer, Daresbury Laboratory U.K.)

Due to the difficulties reached with the TOF-SIMS analysis in identifying the Boron atoms location, and to detect Nitrogen, a broader study over samples with and without Boron doped oxides was realized by X-ray photoelectron spectroscopy (XPS) measurements. The XPS measurements were done at the Imperial College London.

XPS spectra are obtained by irradiating a material with a beam of X-rays while simultaneously measuring the kinetic energy and number of electrons that escape from several nanometers of the material being analyzed. From the binding energy and intensity of a photoelectron peak, the elemental identity, chemical state, and quantity of a detected element can be determined.

XPS reveals which chemical elements are present at the surface and the nature of the chemical bond that exists between these elements. Thanks to this technique we have been able to define the location of the atoms, used during this thesis, around the interface and the interactions between them. We have analyzed several samples with different oxide treatments implying N and B effect and also in samples where the

oxide has been removed in order to evaluate what is the scope of the B and N atoms, and to study if there is any relation between the N and B location. The B concentration is calculated based on the detection of B1s.In Fig. 2.10 some of the measurements obtained by XPS during this thesis are detailed. Taking into account that the average depth of analysis for an XPS measurement is approximately 5-10 nm, depth profiling XPS measurements must be performed to obtain more information about B location.



Sample	Definition
0	**Bare SiC**
A1	**SiC + SiO_2** (grown in NO)
B1	**SiC** (NO- SiO_2 removed)
A2	**SiC + SiO_2** (NO) + **B**
B2	**SiC** (NO-SiO_2 + B removed)
A3	**SiC + SiO_2** (grown without N)
B3	**SiC** (free N -SiO_2 removed)
A4	**SiC + SiO_2** (free N) + **B**
B4	**SiC** (free N -SiO_2 + B removed)

Figure 2.10 XPS measurement acquired in a set of samples with and without boron doped oxide, with all expected core levels visible. A table with samples details is included.

2.3 Electrical Characterization

Below are described all the electrical measurements performed in order to complete full electrical characterization of our fabricated n-type MOS capacitors and MOSFETs. Calculation methods for evaluating the main electrical parameters are detailed.

2.3.1 TLM

In order to determine the sheet resistance on our samples, the Transfer Length Method (TLM) is used [6, 7]. TLM consist on a group of metal/semiconductor contacts with a low ohmic contact resistance (R_C). The measured total resistance (R_T) of a simple semiconductor resistor (with two contacts) can be obtained by:

$$R_T = 2R_m + 2R_C + R_{semi} \tag{2.1}$$

where R_m is the resistance due to the metal layer, R_C is the resistance associated with the metal/semiconductor contact and R_{semi} is the semiconductor resistance:

$$R_{semi} = R_{Sh}\frac{d}{W} \tag{2.2}$$

where W and d correspond to the contact width and distance between contacts respectively and R_{sh} is the semiconductor sheet resistance. A single contact resistance would be R_m+R_C, where R_m can be rejected in most cases due to $R_m<<R_C$. Hence the total measured resistance is as follows:

$$R_T = R_{Sh}\frac{d}{W} + 2R_C \tag{2.3}$$

As shown in Fig. 2.11 (a), if identical resistors of different lengths are measured and plotted as function of contacts distance, several parameters such as the contact resistance (extrapolating results to L=0) or the sheet resistance (from the slope in Fig. 2.11(a)) can be extracted.

We will use the contact resistivity (ρ_C) to evaluate the doped material layers:

$$\rho_C = R_C A_C \tag{2.4}$$

being A_c the contact area.

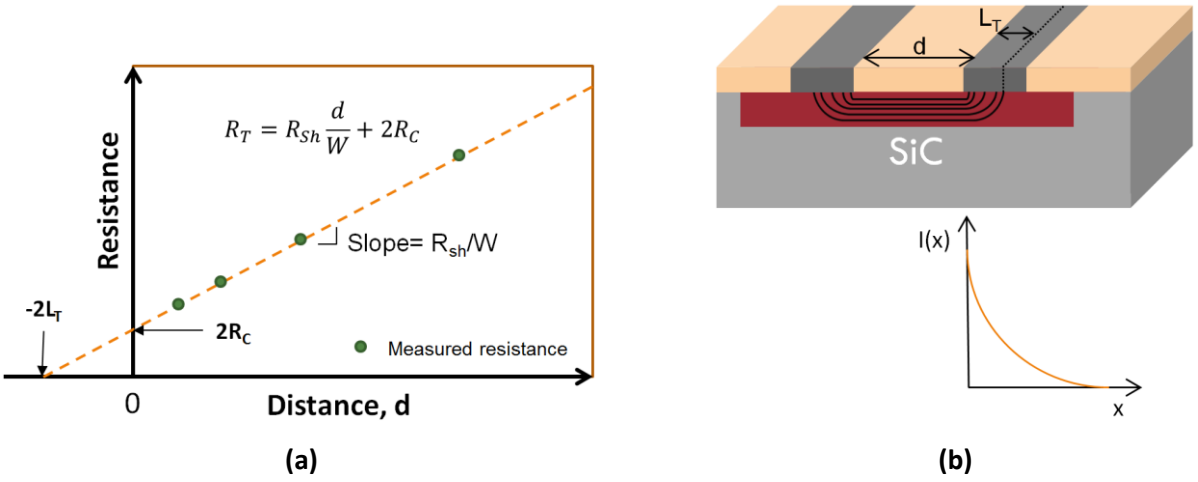


Figure 2.11 (a) Parameters obtained from the resistance versus distance measurement results. (b) Schematics of our planar geometry for measuring the sheet resistance.

Since we are working with planar geometry structures (Fig. 2.11 (b)), the contacts are located one next to the other, then the current flow is not uniform. So we shouldn't use the entire contact area for our calculations. We have to use the effective contact length (L_T), which is the average distance that an electron (or hole) travels in the semiconductor beneath the conductor before it flows up into the contact:

$$L_T = \sqrt{\frac{\rho_C}{R_{Sh}}} \tag{2.5}$$

So the contact resistance is:

$$R_C = \frac{\rho_C}{L_T W} = \frac{R_{Sh} L_T}{W} \tag{2.6}$$

By combining some of the equations above:

$$R_T = R_{semi} + 2R_C = \frac{R_{Sh}}{W}(d + 2L_T) \tag{2.7}$$

Therefore, the L_T value can be obtained from Fig. 2.11 (a), at the horizontal axis intercept.

The TLM arrangement used in this thesis is shown in Fig. 2.12. There is a rectangular region (red rectangle) with the same doping (same sheet resistance) as the device contact area. Identical contact pads with different spacing are located in this area. The spacing values are; 5, 10, 20, 40 and 100 µm, the contact dimensions L/W are 86/296 µm. By measuring the resistance between each pair of contacts, we can construct the TLM graph (Fig. 2.11 (a)) and obtain all the parameters: R_{Sh}, R_C, L_T and ρ_C. The ρ_C expected values in n-type 4H-SiC and 6H-SiC are between 10^{-4} Ωcm^2 and 10^{-6} Ωcm^2.

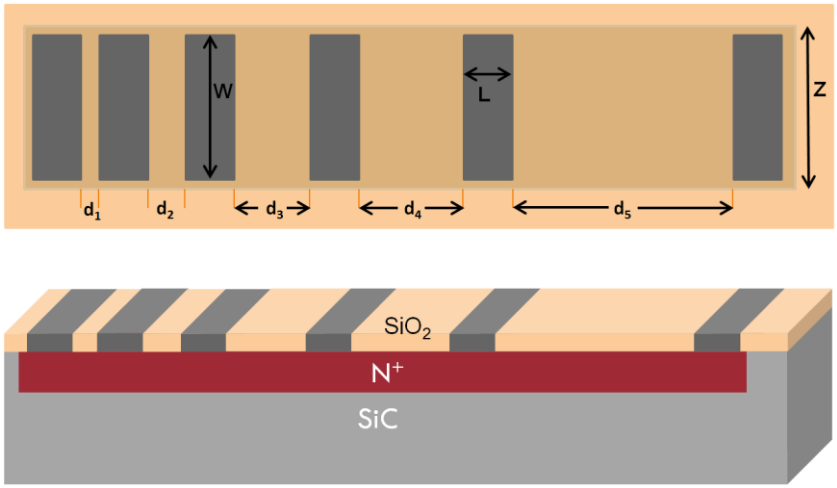


Figure 2.12 Schematics of the full TLM test structure used in this thesis.

It is important to have a high contact quality to maintain the R_C value negligible in comparison with the on-channel resistance. We have used the TLM method to verify a good performance of the ohmic contacts and to obtain the R_C value. In our devices R_C is several orders of magnitude below the experimental R_{ON} even in MOSFETs with shorter L.

2.3.2 MOS capacitance

MOS capacitors work principle has been explained in Chapter 1. Basically it consists of a three layers stack; a semiconductor, a dielectric and a metal layers. The main sources of energy loss in a MOS capacitor could be: changes in the interface trap level occupancy, changes on the bulk trap levels occupancy, leakage through the oxide and series resistance [8]. In order to avoid the error induced by series resistance, a correction to the measured impedance is applied [8].

The equivalent circuits of the MOS capacitance for the different operating regions are shown in Fig. 2.13. The schematics correspond to:

(a) MOS equivalent circuit for depletion to weak accumulation showing the oxide accumulation capacitance (C_{ox}) connected in series with the semiconductor and with the series resistance (R_s). The semiconductor consist of a parallel circuit of the semiconductor or space charge region capacitance (C_{SC}), the interface trap capacitance (C_{it}) and the interface trap conductance (G_{it});

(b) Simplified circuit where the parallel capacitance is C_P=C_{SC}+C_{it} and the parallel conductance is G_P= G_{it}.

(c) Measured circuit of the impedance analyzer with the measured admittance (Y_m) components; capacitance (C_m) and conductance (G_m). These quantities correspond to the experimentally measured quantities. Being the admittance:

$$Y_m = G_m + j\omega C_m \tag{2.8}$$

(d) Equivalent circuit of a MOS capacitor in strong accumulation, used in the C_{ox} and R_s values extraction. Since the interface states do not change their occupancy with the AC signal during accumulation C_{it} and G_{it} has no contribution in C_P and G_P. On the other hand C_{SC} can be considered infinity in accumulation. Hence, the measured impedance only contains the C_{ox} and R_s.

C_P and G_P can be obtained in terms of the measured capacitance and measured conductance by the equations [9]:

$$C_P = \frac{C_{ox}\left[{C_m}^2+\omega^2 C_{SC}(C_{SC}+C_{ox})\right]}{\omega^2(C_{SC}+C_{ox})^2+G_m} \tag{2.9}$$

$$G_P = \frac{\omega^2 G_m {C_{ox}}^2}{{G_m}^2+\omega^2(C_{ox}-C_m)^2} \tag{2.10}$$

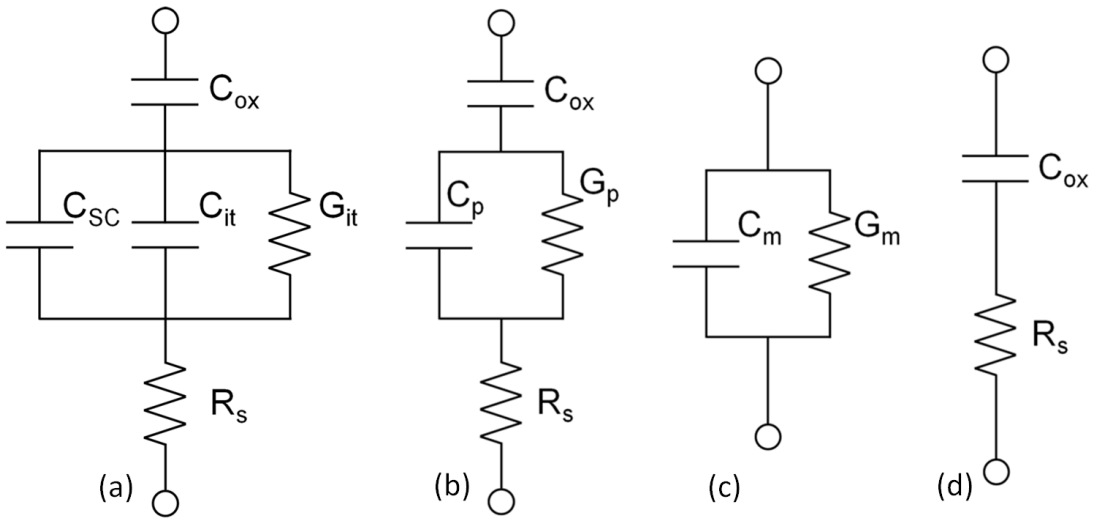


Figure 2.13. (a) Equivalent circuit of the MOS capacitor for depletion to weak accumulation, including oxide capacitance, semiconductor capacitance, interface traps capacitance, interface traps conductance, and series parasitic resistance (b) Simplified circuit with parallel capacitance and parallel conductance, (c) equivalent circuit of the impedance analyzer with measured capacitance and conductance and (d)Equivalent circuit for strong accumulation.

As shown in Fig. 2.13 (d) C_{ox} and R_s can be estimated from the admittance behavior in accumulation. The series resistance is the real part of the impedance ($Z_m=1/Y_m$), hence [8]:

$$R_s = \frac{G_{m,acc}}{G_{m,acc}^2+\omega^2 C_{m,acc}^2} \tag{2.11}$$

where “acc” indicates accumulation measurement.

Then, the C_m and G_m are compensated for R_s value at a particular frequency, being the corrected values C_C and G_C:

$$C_C = \frac{(G_m^2+\omega^2 C_m^2)C_m}{a^2+\omega^2 C_m^2} \tag{2.12}$$

$$G_C = \frac{(G_m^2+\omega^2 C_m^2)a}{a^2+\omega^2 C_m^2} \tag{2.13}$$

where $a = G_m - (G_m^2 + \omega^2 C_m^2)R_s$ and C_m and G_m are the measured capacitance and conductance respectively.

In this work, circular n-type SiC capacitors with diameter of 300 µm, used for gate dielectric evaluation, were fabricated on 8 µm n-type epitaxial layers with a doping concentration of $7\cdot10^{15}$cm^{-3}. Epilayers were grown on the Si-face of 4° off-axis cut n-type 4H-SiC substrates.

The analysis based on the capacitance-voltage (CV) measurement is effective for investigating the basic characteristics of the materials and improving the device quality. There are two kind of CV measurements: The small signal ones (high frequency), which consists on the measurement of differential C by small AC modulation (of 20mV in our case) of the applied bias voltage (DC); and the quasi-static (QS) CV measurement, where the linear ramp voltage sweeping technique is used, in which the charge current is measured instead of the capacitance. Under thermal equilibrium conditions, this ramp response is proportional to the low frequency differential capacitance. The QS capacitance is then computed from this current response [C = I/(dV/dt)]. QS-CV measurement allows capturing the slow response than cannot be measured by high-frequency (HF) CV.

For the CV electrical measurements on MOS capacitors we used a Keithley 4200 (high freq), and the Impedance Analyzer 4192A. Quasi Static measurements were done with a *Keysight B1500A*. The BIAS applied in each case depends on the dielectric thickness, to ideally apply an oxide electric field of 2-4 MV/cm.

CV study

The measurement of the gate to substrate capacitance of a MOS device is very important since it is the only way to calculate many important device parameters such as substrate impurity concentration (N_a) and flat band voltage (V_{FB}).

From the CV measurements, properly correcting the series resistance, we can obtain [8]:

1. The oxide thickness,

$$T_{ox} = \frac{\varepsilon_0 \varepsilon_{ox} S}{C_{ox}} \tag{2.14}$$

where C_{ox} is the maximum capacitance measured (it corresponds to the capacitance measured in accumulation regime), ε_0 is the free space permittivity, being $8.85 \cdot 10^{-14}$ F/cm, ε_{ox} is the dielectric constant (ε_{SiO2} =3.9) and S the capacitance surface area.

2. The substrate doping can be obtained by using Eqs. (2.15),(2.16):

$$\frac{1}{C_{min}} = \frac{1}{C_{ox}} + \frac{W_{max}}{\varepsilon_S} \tag{2.15}$$

$$W_{max} = \sqrt{\frac{2\varepsilon_S \phi_B}{qN_a}} \tag{2.16}$$

where W_{max} is the maximum depletion layer width and ϕ_B is the bulk potential defined in Chapter 1, Eq. (1.2).

3. The flatband capacitance (C_{FB}) at one Debye length (λ_d) can be obtained from Eqs. (2.17), (2.18):

$$\frac{1}{C_{FB}} = \frac{1}{C_{ox}} + \frac{1}{C_{SC}} = \frac{1}{C_{ox}} + \frac{\lambda_d}{\varepsilon_s} \tag{2.17}$$

$$\lambda_d = \sqrt{\frac{\varepsilon_s kT}{q^2 N_a}} \tag{2.18}$$

4. The total amount of charge in the isolator:

$$N_{eff} = (\Phi_{MS} - V_{FB}) \frac{C_{ox}}{qS} \tag{2.19}$$

From CV measurements, it can also be extracted the interface state density (D_{it}). In Chapter 2.4 some D_{it} extraction methods are widely explained. The CV measurement is done from depletion to accumulation regime. Several consecutive measurements are made in the same direction to stabilize the flat band voltage value. In our case, we did 5 measurements from depletion to accumulation, obtaining the V_{FB} value from the last (stable) curve. After that, we applied a biasing voltage in depletion during several minutes, in order to discharge the device. And the V_{FB} is measured again, obtaining a second V_{FB} value.

The CV in SiC exhibits special characteristics, different from those of Silicon. The main factors involved are the extremely low minority carrier generation, the recombination rate, and the activity of fast and slow single-level interface traps [10]. Some of the artifacts seen throughout this thesis that helped us to determine which oxidations treatments provided with a better SiC/SiO_2 interface, are explained below:

a) A **V_{FB} shift** indicates the presence of fixed insulator charge (Q_F). A shift to positive voltage values could indicate the presence of fixed charges or the presence of deep lying interface states with a very long response time. These states are charged during the measurement, and they are only discharged over time or by the recombination of minority carriers. A typical CV negatively shifted in P-doped samples is due to fixed oxide charges resident at the interface.

b) A **slope variation** (or distortion) indicates a high density of Interface trapped charge (Q_{IT}). **A bump** in the CV measurement (see Fig. 2.14) indicates that most of the negatively charged surface states can be discharged by hole capture. The bump position depends of the voltage sweep rate and on how long is the DC bias applied in accumulation or depletion. The bump width depends of the density of surface states negatively charged out of the equilibrium.

c) The appearance of a **ledge** with a constant capacitance value (see Fig. 2.14) indicates a delayed evacuation of minority carriers, due to the high band bending in deep depletion [11]. The length of this ledge depends on the minority carrier generation at the SiC/SiO_2 interface.

d) The appearance of **hysteresis** reflects the difference between a forward (depletion to accumulation) and a reverse (accumulation to depletion) CV curve. Hysteresis is due to the activity of slow traps that reside in the oxide covering the SiC surface. In case we do not detect hysteresis, it may be either that there is a low density of slow traps, or a high generation of minority carriers. Often mobile electric charges in the oxide and deep interface states have low emission times and cannot follow the probe frequency or the sweep rate of the voltage ramp. Therefore they fail to charge during CV measurement. Both types of defects are often not able to ionize during one period of the measurement signal, but are activated at higher gate bias. Reduction of the velocity of the voltage ramp results in a less intense hysteresis, as more time is available for the emission of charge carriers.

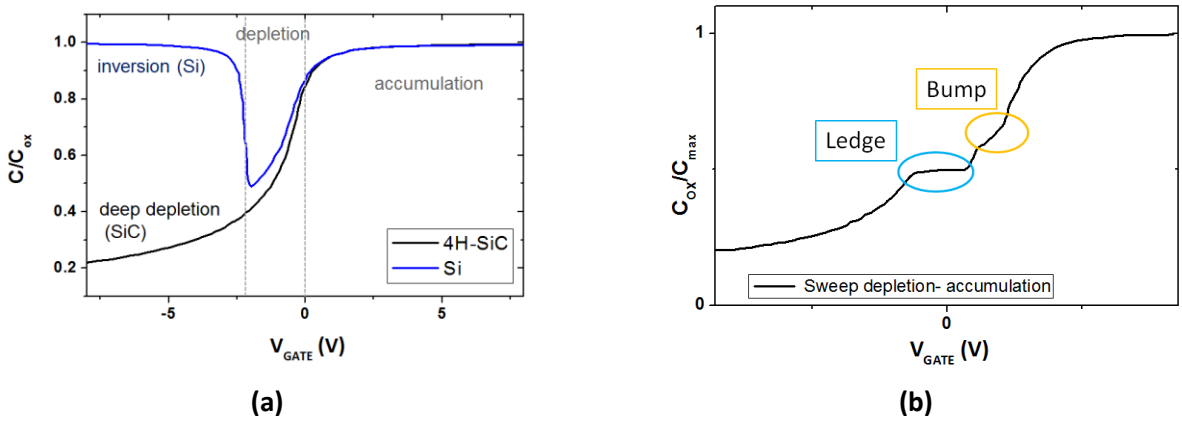


Figure 2.14 (a) Ideal capacitances normalized to C_{ox} for Si and 4H-SiC, as a function of the gate voltage (b) Slope distortions observed in a CV curve when sweeping from depletion to accumulation.

The insulator charge Q_{OT} (oxide trapped charge) is independent of the applied bias while Q_{IT} do change with the gate BIAS. Due to the capture and emission of Q_{IT}, the ideal CV stretches out along the voltage axis. Because, for a given surface potential, more charge on the gate is required to compensate Q_{IT}.

GV study

The conductance technique, based on the parallel conductance (G_p) expression, is one of the most complete methods for interface states characterization, since it allows for the extraction of the traps parameters such as their concentration and position in the bandgap, the D_{it}, the emission time, the capture cross sections and the standard deviation of the surface potential [12].

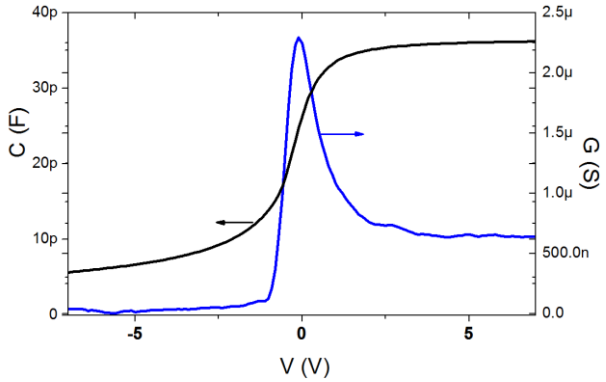


Figure 2.15 Obtained CV and GV curves for one of our boron doped samples for an applied frequency of 100kHz where the peak and the accumulation conductance can be seen. Evaluated on a circular capacitance with a diameter of 150 µm.

The conductance method measures (Fig. 2.15) are commonly used to obtain reliable average values of interface and near interface traps, referred as D_{it} in the depletion region. Furthermore this method examines the full frequency dispersion of the MOS capacitance rather than just the high- and low-frequency aspects. The D_{it} extraction is detailed in section 2.4. [13-15].

Conductance is generally measured as a function of frequency at different values of gate bias voltage. Fig. 2.16 shows an example of measured conductance during this work on two different MOS oxides. It shows 2D graphics of the obtained conductance versus voltage in MOS capacitors with and without boron. In Fig. 2.16 are plotted the G_c values corresponding to the conductance data obtained at different frequency values, swept in voltage. As can be seen, conductance peak amplitudes change with frequency, and their maximum is shifted to slightly higher voltages on boron samples.

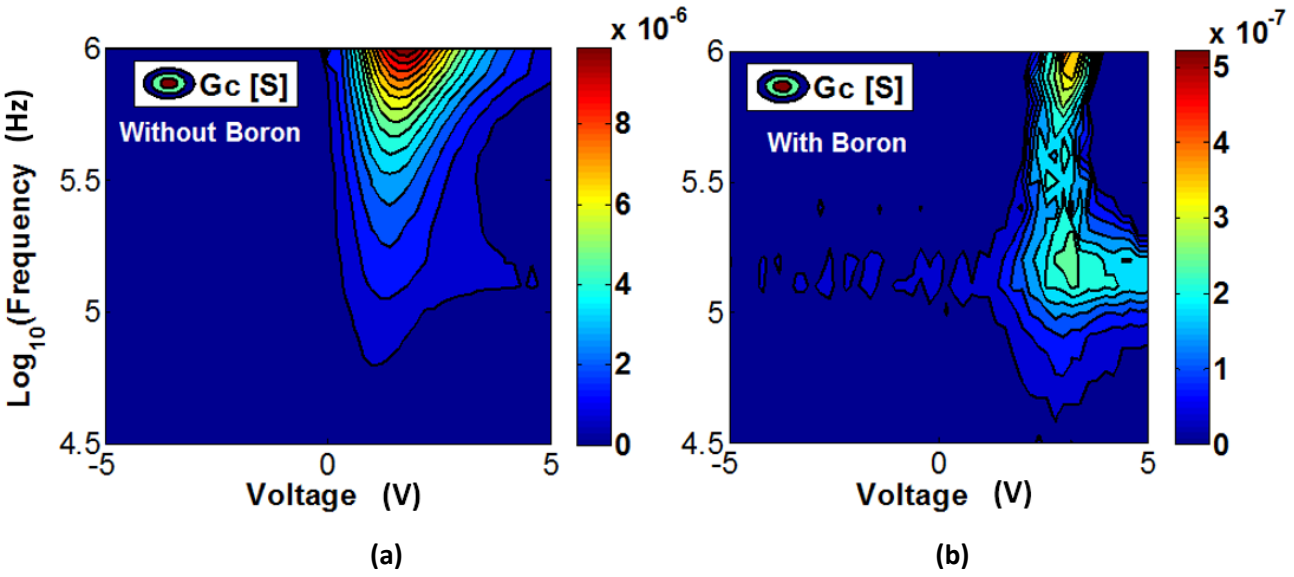


Figure 2.16 Measured conductance in function of frequency and voltage for implanted MOS samples without Boron treatment (a) and with Boron treatment (b).

The same interface trap information can be obtained by both, conductance and capacitance measures. However, conductance is a direct measure, does not require the determination of the doping density (for C_{SC} calculation), and hence provides more accurate information about interface traps. Conductance method only depends on the energy loss mechanisms associated with the capture and emission process of majority carriers in or near resonance with the time period at the measurement signal frequency.

The main advantage of using capacitance instead of conductance technique is that it requires less time to acquire and process the data. And it is easier to compare the obtained results with other authors.

2.3.3 MOSFETs

The on-state measurements of the lateral nMOSFETs were performed using a Keithley 251 IV SMU system. All the devices were tested at wafer level using a semiautomatic probe station. With the source contacts grounded, the output $I_{DS}(V_{DS})$ characteristics were obtained by applying positive voltages to the drain and gate. The transfer $I_{DS}(V_{GS})$ characteristics were measured with the source grounded and applying a constant voltage of 0.1 V or 1 V to the drain. The gate-drain leakage was first measured, and was confirmed to be of the order of 100 pA.

Field effect mobility

The field effect mobility (μ_{fe}) was extracted for each transistor from the transconductance measurement, as well as from the $I_{DS}(V_{GS})$ curve at low drain voltage. The MOSFET transconductance is defined by:

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}}\Big|_{V_{DS}=constant} \tag{2.20}$$

When this expression is solved, the field effect mobility is given by:

$$\mu_{fe} = g_m \frac{L}{WC_{ox}V_{ds}} \tag{2.21}$$

where L is the channel length [cm], W is the channel width [cm] and C_{ox} the gate oxide capacitance [$F \cdot cm^{-2}$].

At high gate voltage values, the $I_{DS}(V_{GS})$ curve reaches its maximum, and remains constant. Then, its derivative (and hence the transconductance) must be zero. Regarding the μ_{fe} equation, g_m being zero would imply a value of zero mobility (no electrons movement), which is strictly false. On account of that, when the μ_{fe} has been obtained for high V_G bias values, we used an expression which has been slightly modified to a differential equation:

$$\mu_{fe} = \frac{(I_{ds}(V_G) - I_{ds}(V_{TH}))}{V_G - V_{TH}} \frac{L}{WC_{ox}V_{ds}} \tag{2.22}$$

Threshold voltage

The threshold voltage (V_{th}) is a key parameter in the MOSFET characterization. It may be understood as the gate voltage value at which the transition between weak and strong inversion takes place in the MOSFET channel. V_{th} is usually evaluated using the constant-current (CC) method [16] which consist on taking the value of the gate voltage corresponding to a given arbitrary drain current fixed value. The drain current value chosen in our measurements is $1x10^{-8}$ A. Even though we decided to mostly use the CC method because of its simplicity, this technique is inherited from Si technology and is not always accurate in SiC technology.

In some cases, where a very precise value of V_{th} was required, a technique which extracts the proper value from the power-law exponent [17] was used. The saturation drain current in SiC MOSFETs in strong inversion is usually modeled by a power law with an exponent which can differ from 2 (the conventional value in monocrystalline Si) as it happens in amorphous and polycrystalline Si thin film transistors (TFTs) [17].

Threshold voltage instability

In any case, for a proper study of the MOSFET properties, the $I_{DS}(V_{GS})$ was measured several times before of data acquisition, to assure the V_{th} stabilization.
Regardless of all the efforts devoted to increase the channel mobility of the SiC MOSFETs, the instability of the threshold voltage remains a central problem. The commercialized devices contain nitride oxides (e.g. NO or N_2O), without additional doping processes. This is because many of the recent techniques proposed for mobility improvement (phosphorus, boron, …) introduce problems with regard to V_{th} stability, being nitride oxide devices still the most stable option for room temperature performance.

Under operation stress, a positive V_{th} shift means that the device R_{ON} increases for a given Vg. As a positive V_{th} shift increases then conduction losses, limiting power-conversion efficiency. Differently, a negative V_{th} shift may imply an increase of the leakage current at V_G=0V and, therefore, reduce the blocking-voltage and normally-off capabilities.

To evaluate the MOSFETs V_{th} shift, a time Bias Stress Instability (BSI) test is typically used. BSI technique allows observing the impact on the device electrical parameters of the amount of both NIOTs and mobile charges with time. In this way, BSI measurements (inherited from Si technology) have been classically carried out with the application of bias cycles defined according to each experiment. A typical test sequence is illustrated in Fig. 2.17. Initially, the V_{GS} is generally ramped from $-V_{GS}$ to $+V_{GS}$ applying a constant drain bias (step 1 in Fig. 2.17). Then, the positive gate bias is maintained for a certain bias-stress time while the other terminals remain grounded (step 2 in Fig. 2.17). Following this positive bias stress, the V_{GS} is ramped from $+V_{GS}$ to $-V_{GS}$ to determine the shift of the I_{DS} (V_{GS}) characteristics (step 3 in Fig. 2.17). Finally, the gate is negatively biased, defining a bias cycle. This implementation of the BSI method has been used for most of the reported SiC MOSFET optimization studies up to now. However, the accuracy of this method is limited for SiC, and does not provide all the necessary information.

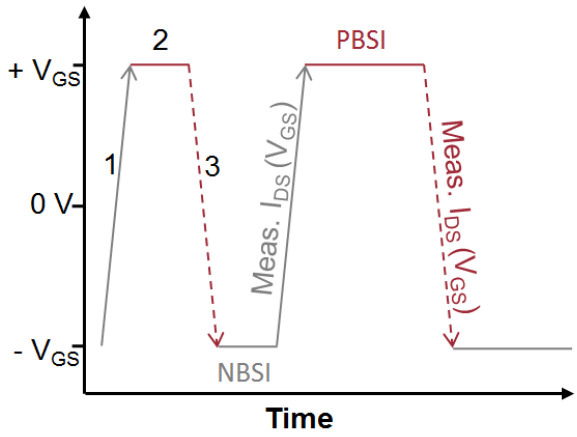


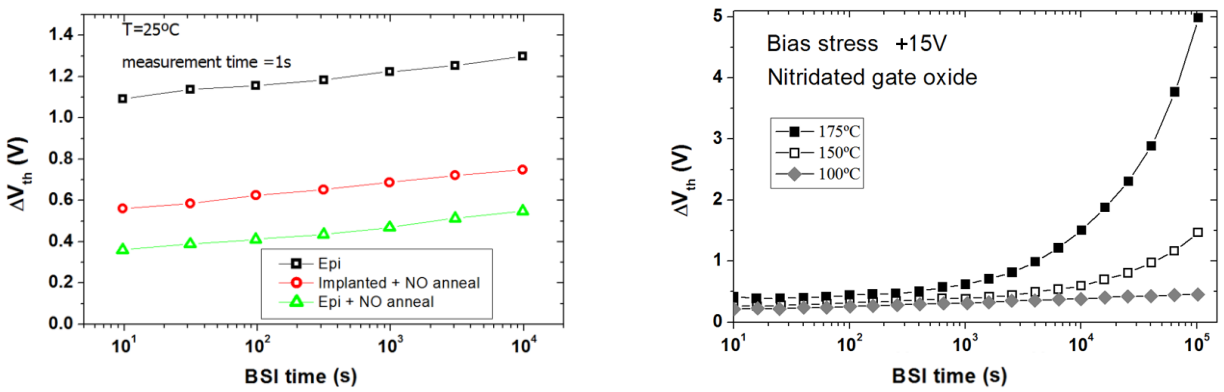
Figure 2.17 Schematic of bias-stress cycle showing the applied V_{GS} versus time during the gate bias-stress threshold instability measurements. Numbers 1, 2 and 3 correspond to the different steps defining a BSI test cycle (Adapted from [18]).

In our measurements we usually sweep the V_G between -15V and 15V, or even more if the gate oxide is thicker, to work with applied electric fields between ±3 MV cm^{-1}. At higher stress-bias new defects generation can take place, complicating the data analysis on the study of the native traps. The V_{th} is measured in the sweeps after both; negative bias stress (NBSI) and positive bias stress (PBSI) (step 1 and step 3 on Fig. 2.17), using log stress time intervals (10s, 36s, 100s, 360s, 1000s and 3600s…). The V_{th} shift (ΔV_{th}) is studied both, after a NBSI or after a PBSI measurement.

Nitridated oxides

The V_{th} drift has been broadly studied over different kind of oxides. Fig. 2.18 (a) shows the V_{th} shift of various types of 4H-SiC MOSFET devices, with and without nitridation, when stressed with a gate oxide electric field of ±3 MV cm^{-1}. The results can be explained by electron tunneling in and out of NIOTs, as reported in [18]. As can be inferred in Fig. 2.18 (a), MOSFETs with nitride gate oxides do exhibit a reduction of the instability. Additionally, the threshold voltage shift slightly increases with the increase of the applied bias voltage during the stress test, since tunneling is sensitive to the local field in the gate oxide [18].

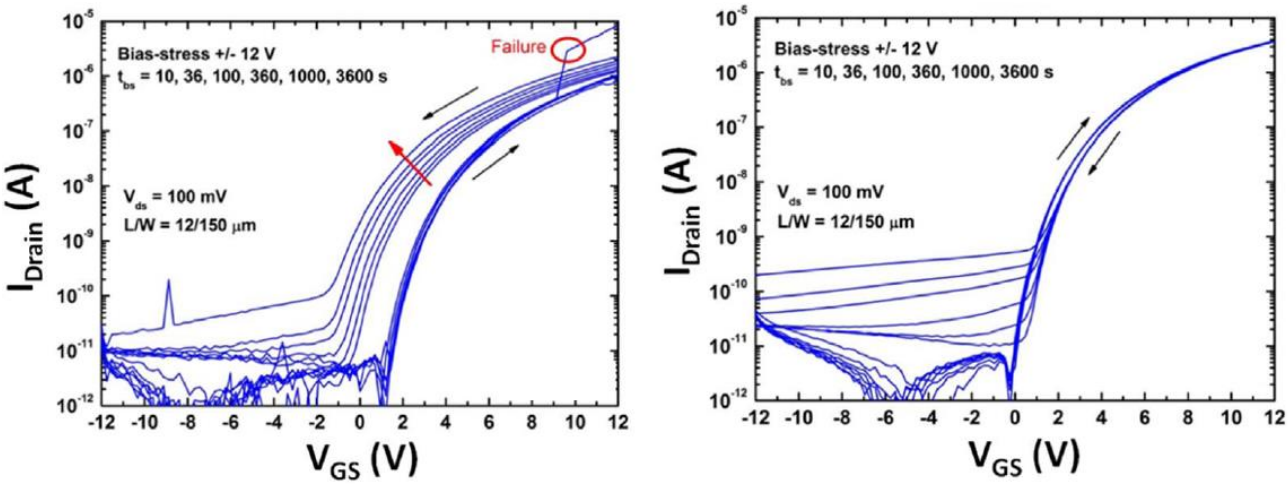
Although it has been shown that oxide nitridation contributes to a better V_{th} stability [18] at room temperature, V_{th} instability is observed after long stress time (> 1 hour) for temperatures over 150°C. This behavior may be attributed to NIOTs [19, 20], and its effect can be seen in Fig. 2.18 (b), where a strong drift is observed at 175°C when performing a PBSI.



(a) **(b)**

Figure 2.18 (a) Threshold voltage shift of 4H-SiC MOSFETs with different oxides, when stressed with an oxide field of +3 MV cm^{-1}. Epi means that the channel is built on a P-type epilayer. While Implanted means that the channel is formed on an implanted P-well. (Adapted from [18]). (b) ΔV_{th} as a function of a PBSI measurement in a 4H-SiC MOSFET with a nitride oxide at different temperatures. (Adapted from [20]).

Similarly, the evolution of transfer curves I_{DS} (V_{GS}) during a BSI test previously done in our group are shown in figure 2.19 [21].This study was done in samples with different surface preparation before a N_2O gate oxidation process is applied. Fig. 2.19 (a) shows the evolution of the transfer curve of n-MOSFETs pre-treated by O_2 plasma, while Fig. 2.19 (b) shows the results obtained when a pre-annealing under H_2 at 800°C is done. It can be clearly observed that a H_2 pre-treatment allows reducing both the threshold hysteresis and its drift.



(a) **(b)**

Figure 2.19 Evolution of the transfer curve for (a) O_2 plasma pre-treatment and (b) H_2 at 800 °C pre-treatment on N_2O grown oxide during stability BSI test. V_{GS} sweeps from – 12 V to + 12 V, and reverse, are applied for increasing step-time durations, up to 1 h [21].

It must be added that the drain leakage current in the subthreshold region increases when doing the BSI test, being proportional to the charge exchange between NIOTS and drain region (n-type SiC) of the substrate [1]. This effect can be seen in Fig. 2.19.

To conclude this section, we must emphasize that the actual mechanism causing the V_{th} instabilities in SiC devices intrinsically differs from silicon. We observe a lot of variations in V_{th} measurements depending on the interface and the dielectric properties and, importantly, the BSI test does not cause a permanent damage to the interface. V_{th} recovery phenomena results in the underestimation of the number of trapped charges during the gate bias stress, because trapped charges are released immediately once the stress is removed. Consequently, it is necessary to reduce the relaxation time in order to obtain a reliable V_{th} shift evaluation.

Novel characterization methods

Accordingly, several recent papers point out that, in order to measure V_{th} instability in SiC, dedicated characterization methodologies are needed for SiC MOSFETs, since silicon-based standards can lead to ambiguous results when directly applied. For instance, Aichinger and co-workers have recently deeply studied the V_{th} peculiarities and response to Bias Temperature Instability (BTI) test of SiC MOSFETs in comparison with Si ones [22]. It is highlighted that SiC MOSFETs exhibit a fully reversible hysteresis effect due to charging and discharging of interface traps. This effect is not seen in Si MOSFETs due to the different bandgap and its lower D_{it} value. Then, they propose a new measure-stress-measure procedure for BTI evaluation of SiC MOSFETs, which allows distinguishing between reversible V_{th} hysteresis and more permanent V_{th} drift. The new method mainly consists in a proper preconditioning, prior to the stress procedure and the resulting V_{th} readout, as shown in Fig. 2.20.

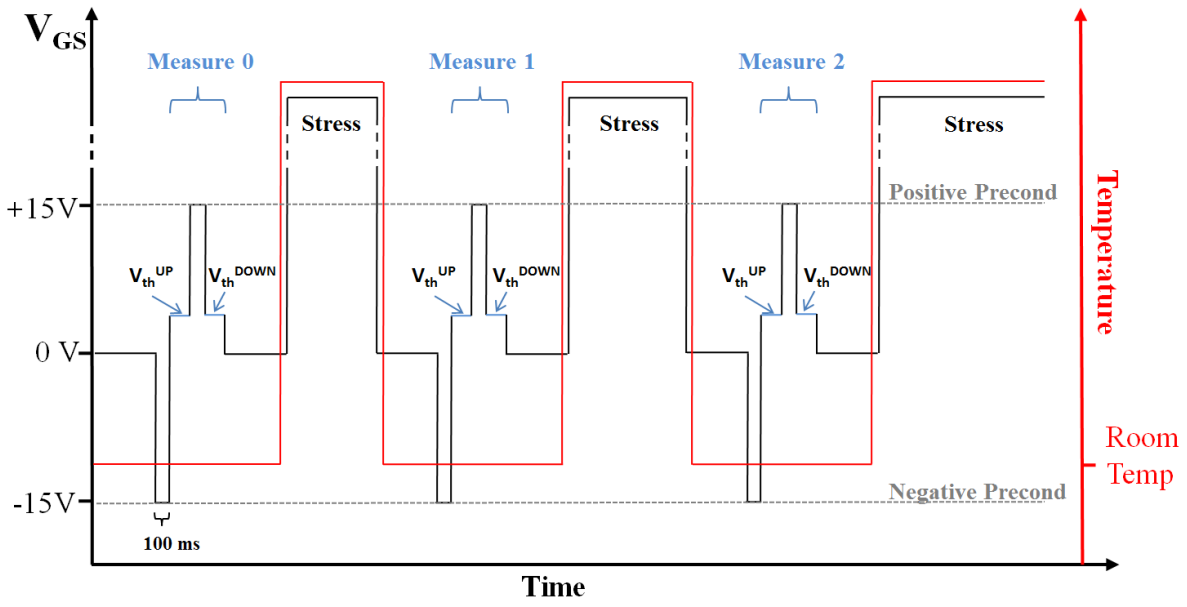


Figure 2.20 Measure-stress-measure procedures suggested in [22] to optimize BTI test for SiC MOSFETs. Drift in V_{th}^{DOWN} = BTI degradation. (Adapted from [22]).

At present, it is considered that the V_{th} shift of 4H-SiC MOSFETs has a strong dependence not only on stress time, but on the measurement time [23, 24]. Recently Okamoto *et al.* published their investigation about the V_{th} instability of 4H-SiC MOSFETs with dry, 10 min NO POA and 60 min NO POA at 1250°C gate oxides, using high-speed (HS) I-V measurement instrument [25]. DC stress measurement ranging from 10^{-6} to 10^{3}s without relaxation effect revealed that the V_{th} shift had two modes, a fast and a slow component, of which the fast component can be suppressed by NO POA. The results are shown in Fig. 2.21, where it can be seen different samples measured by the conventional slow sweep method and by non relaxation (NonRlx) method explained in [26]. In this NonRlx method, a constant V_{GS} is continuously applied as a gate stress avoiding the V_{th} relaxation. A High Speed Non relaxation method (HS NonRlx), where the sampling period is of the order of s (instead of ms) using HS IV instrumentation [25] is also used for comparison. An extremely large V_{th} shift is observed when using the HS NonRlx method compared with the other methods. This result indicates that a large number of charges were trapped in a short stress time, and that such effect cannot be observed by conventional methods.

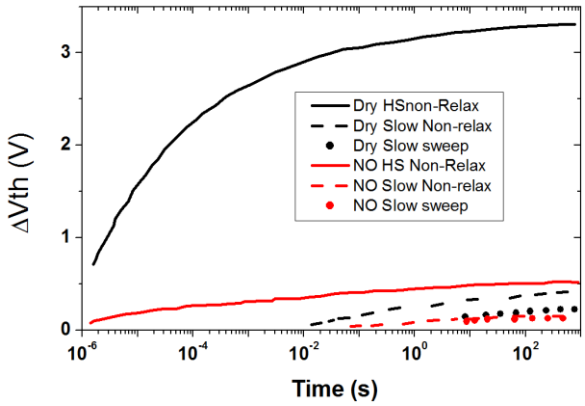


Figure 2.21. ΔV_{th} vs time for a dry sample and a 60 min NO POA at 1250°C (*NO60) sample measured by three different methods (traditional slow sweep, slow non-relaxation and high speed non-relaxation method). The DC bias is 15V. (Adapted from [25]).*

Similarly, Sometami *et al.* also propose evaluating V_{th} shift by HS NonRlx methods. The V_{th} shift of 4H-SiC MOSFETs with Ar or N_2O POA was measured by conventional sweep, three points, NonRlx methods and HS NonRlx methods [26, 27]. Although the V_{th} shift values of both samples were almost identical when measured by the sweep method, those for the Ar POA samples were larger than those for the N_2O POA samples when measured by the non-relaxation method.

Finally, it should be noted that although faster measurements (on the order of μs) will likely result in larger observed V_{th} shifts, they probably will not affect the reliability of most of the applications employing these devices since they do not lead to increased leakage in the OFF state or increased resistance in the ON state.

Currently, a committee of JEDEC experts; JC-70 Wide Bandgap Power Electronic Conversion Semiconductors [28] led by Chair Dr. Stephanie Watts Butler from Texas Instruments and composed by representatives of the most relevant industries of the field is elaborating a new international standard for SiC characterization, including the definition of a proper method for SiC MOSFET V_{th} shift evaluation.

2.4 D_{it} extraction techniques

To fully understand the magnitude of the effect that interface traps have on the MOS devices operational behavior it is important to be able to quantify the traps accurately. As shown in Table 2.1 there are several methods used for this purpose. The methods can be classified among those that use the MOS capacitor and those using the transistor (or diode) as test structure. In addition, they can be classified in 2 types depending on the direct or indirect nature of the measure, being direct measures those in which the measured signal is directly proportional to the density of interface states, and indirect measures those

based on variations caused by the interface states over an external signal. It is expected direct methods being more reliable than indirect ones.

Table 2.1 Main methods used for interface states characterization.

	Indirect methods	Direct methods
MOS Capacitor	QS, High and Low frequency CV [10, 15]	DLTS [31, 32] Conductance [14]
MOSFET	Subthreshold method noise 1/f [29, 30]	DLTS Charge Pumping [33, 34]

In this section we are defining some of the interface states characterization methods, which have been used during this thesis. The techniques that can be considered more widely studied, are those based on MOS capacitors. Of which we will discuss both capacitance measurements, as well as the conductance method. On the other hand, we will talk about measurement techniques applied to MOS transistors. Some results have been obtained through the subthreshold method (in the weak inversion zone), although there are other factors, different from interface states, that influence the transistors behavior in the subthreshold region, limiting the use of this technique. Finally, the charge pumping technique is presented. It is based on the recombination process that takes place in the SiC/SiO_2 interface, which generates a current directly related to the density of interface states.

2.4.1 High-low method, C(V)

A lot of information regarding the oxide properties can be obtained from the MOS capacitors analysis. The high-low (Hi-Lo) CV method [10, 15] is widely used to determine the interface state density (D_{it}) energy distribution in the SiC bandgap. The D_{it} is extracted from the C-V behavior in the depletion regime, where the high-frequency capacitance (C_{HF}) curve and the low-frequency (C_{LF}) (or quasi-static capacitance (C_{QS})) curve are different because of the response time of the switching states. Indeed, as the DC bias is swept from accumulation to depletion, the traps emit their charges when the Fermi level at the interface crosses the corresponding energy in the band-gap. At a given DC bias, the energy band bending at the interface should be ideally the same for C_{QS} and C_{HF}. A difference between C_{QS} and C_{HF} reveals the D_{it} value at the corresponding energy, as shown in Eqs 2.25-2.27.

It is important to notice that in silicon technology, C_{HF} does not reach inversion above frequency of typically 1 MHz, because the frequency is much faster than the generation rate. In the case of wide band-gap

semiconductors like SiC, even C_{QS} measured at low frequency does not reach inversion because of the low intrinsic-carrier concentration of SiC.

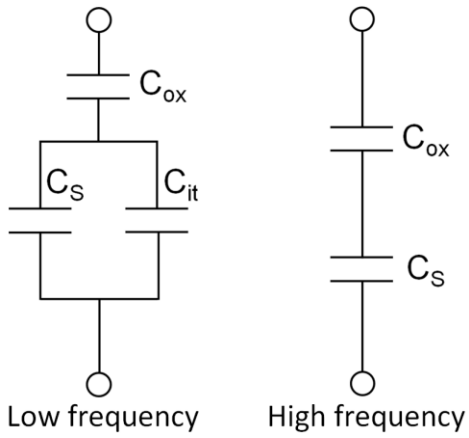


Figure 2.22 Simplified MOS capacitor equivalent circuit measured at low frequency and at high frequency, where C_{ox} is the oxide capacitance, C_s the semiconductor Capacitance and C_{it} the interface trap capacitance.

Fig. 2.22 illustrates the MOS capacitor equivalent circuit measured at low frequency and at high frequency. As it can be seen, the C_{LF} can be obtained by:

$$C_{LF} = (C_S - C_{it})\frac{C_{ox}}{C_{ox}+C_s+C_{it}} \tag{2.23}$$

And the C_{HF} is given by:

$$C_{HF} = \frac{C_s C_{ox}}{C_S+C_{ox}} \tag{2.24}$$

Therefore C_{it} can be obtained from the difference of both capacitance values, and D_{it} would be given by:

$$D_{it} = \frac{1}{qA}\left[\frac{C_{ox}\cdot C_{LF}}{C_{ox}-C_{LF}} - \frac{C_{ox}\cdot C_{HF}}{C_{ox}-C_{HF}}\right] \tag{2.25}$$

Where A is the testing area and C_{ox} comes from Eq. 2.14: $C_{ox} = \frac{\varepsilon_0 \varepsilon_{ox}}{T_{ox}}$.

Note: Theoretically, D_{it} should be expressed in $cm^{-2}J^{-1}$ and consequently a term q^2 should be used in Eq. 2.25. In order to express D_{it} in $cm^{-2}eV^{-1}$, it is usually only divided by "q".

In order to calculate the D_{it} position inside the gap, we need to know the distance to the conduction band "E_C-E" for the n-type MOS or the distance to the valence band "E-E_V" for the P-type MOS. These positions can be calculated as:

$$E_C - E = \frac{E_g}{2} - \psi_s(\mathrm{V}) + \phi_B \text{ ; for n-type} \tag{2.26}$$

$$E - E_V = \frac{E_g}{2} + \psi_s(\mathrm{V}) - \phi_B \ \text{; for p-type} \tag{2.27}$$

where E_g is the semiconductor gap and ϕ_B is the built-in potential shown in eq (1.2):

The flat band voltage (V_{FB}) value corresponds to the flat band capacitance (C_{FB}) obtained from the C_{LF} curve.

The surface potential (ψ_S) can be calculated with:

$$\psi_s(\mathrm{V}) = \int_{V_{FB}}^{V} \left(1 - \frac{C_{LF}(V)}{C_{ox}}\right) dV \tag{2.28}$$

where ψ_S (V_{FB})=0.

Experimentally we do not measure a continuous function of C_{LF} versus V, but we obtain discrete values depending on the measurement voltage step (the smaller the step, the more precision you have). The surface potential is then determined by a sum instead of an integral. For the range going from V_{FB} to "depletion region" we proceed as shown below:

$$\psi_s(V_1) = \left(1 - \frac{C_{LF}(V_1)}{C_{ox}}\right)(V_1 - V_{FB})$$

where V_1 is the next voltage step, moving to "depletion" (going to higher voltages for a P-type MOS, or to lower voltage values for N-type MOS). In general terms:

$$\psi_s(V_n) = \sum_{V_{FB}}^{V_n} \left(1 - \frac{C_{LF}(V_n)}{C_{ox}}\right)(V_n - V_{n-1}) = \left(1 - \frac{C_{LF}(V_n)}{C_{ox}}\right)(V_n - V_{n-1}) + \psi_s(V_{n-1})$$

In Fig. 2.23 some results on D_{it} with this method are shown, it can be seen how the boron process through the gate oxide reduces the D_{it} value near the conduction band.

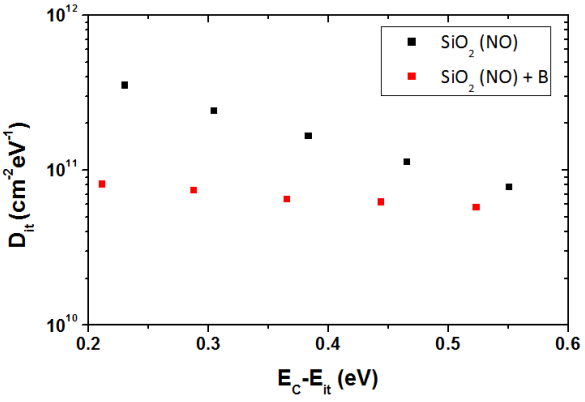


Figure 2.23 Experimental D_{it} values as a function of the energy distance to the conduction band (E_C-E_{it}) obtained in 2 MOS capacitors fabricated during this thesis with and without the boron treatment through the gate oxide.

A key process in order to understand the CV characterizations and their limitations [35], is the capture and emission of electrons between a trap state and the conduction band. The capture time constant (τ_c) corresponds to the time in which an electron from the conduction band is captured by a trap. This constant depends on the electron capture cross section (σ_n) and the thermal velocity of electrons (v_t) as follows:

$$\tau_c = \frac{1}{\sigma_n v_t n} \tag{2.29}$$

where n is the electron concentration.

On the other hand, the emission time constant (τ_e), of an electron from a trap state to the conduction band is:

$$\tau_e = \frac{1}{\sigma_n v_t N_C} exp\left(\frac{E_c - E}{kT}\right) \tag{2.30}$$

where N_c is the effective density of states in the conduction band, E_c is the conduction band edge energy and E a trap energy.

As can be seen in Eq.2.28 the interface states response time depends exponentially on the conduction band edge energy and on 1/T [13]. It should be noted that the emission time of the traps, on which the high-low method is based, also sets the limit of the technique. Indeed, in a n-type material, for energy levels very close to the conduction band, the emission time is so fast that charges can follow the high frequency signal and the two high and low frequency capacitances are therefore equal. For deep levels, the emission time is so long that the traps cannot follow the AC signal and therefore they do not empty. Subsequently, there is only a small energy window in which the method is valid (Fig. 2.24). D_{it} extracted data are valid only over the energy range where it is expected that the high-frequency capacitance does not include any trap contribution, and the low frequency capacitance includes the contribution of all traps within an energy range of a few *kT* of the Fermi level [35]. The upper limit (deep states), of the allowed energy window, is set by the voltage ramp rate and the lower limit (shallow states) is set by the frequency. At room temperature, the assumed valid window is between ~ 0.2 eV and ~ 0.6 eV from the band edges for ramp rate of 0.1 V/s and 1 MHz frequency.

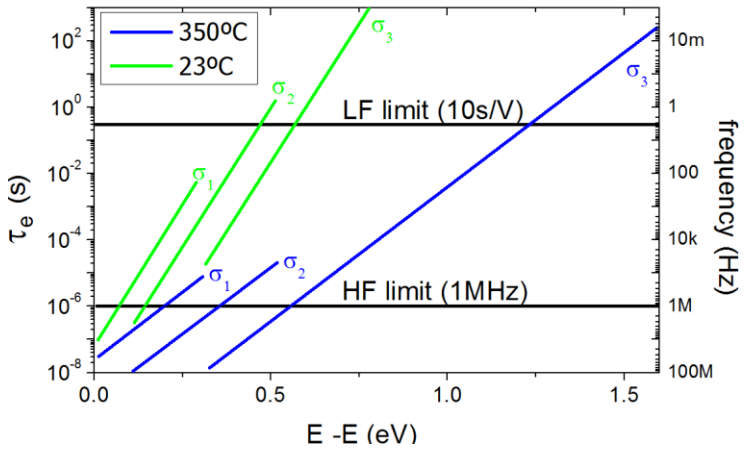


Figure 2.24. *Emission time constants at 23 °C and 350 °C of traps with different capture cross-sections (σ_1=4x10^{-20}cm^2, σ_2=7x10^{-19}cm^2 and σ_3=3x10^{-17}cm^2 from shallower to deeper states). Ec-E is the energy within the gap measured from the conduction band edge. Low-frequency (LF) and high-frequency (HF) limits of the high-low C-V techniques are indicated [15].*

2.4.2 Conductance method, G(V)

A D_{it} estimation can be obtained from the parallel conductance peak value according to the equation $D_{it} \approx \frac{2.5}{q \cdot A} \cdot \left(\frac{G_P}{2\pi f}\right)_{max}$ where A is the testing area [6, 36, 37]. In the equation, we can see the D_{it} dependence on frequency. Comparing with CV, the GV conductance method is useful over a large range of frequencies and makes no *a priori* assumptions about the frequency response of the states. For this reason, it is the preferred technique in case large time constants dispersion is present. However the inherently wide bandgap of SiC results in a broad variation of interface traps response times. Consequently, by using traditional capacitance or conductance measurements, the interface traps distribution can only be determined in a narrow energy range close to the majority carrier's band edge.

Although, by Si theory inheritance, it is accepted that in accumulation regime C_{it} and G_{it} do not contribute to measured values of capacitance and conductance, (as shown in Fig. 2.13 in chapter 2.3.2), in SiC, where there are many NIOTs near the conduction band, the measurements in accumulation could be affected by these traps.

To enable a proper conductance measurement, a small AC signal is superimposed to the DC bias. This AC signal oscillates the energy levels of the NIOTs above and below the Fermi level, which results in electron capture and release into the channel. The equivalent G_p measured in the accumulation region is a direct result of this electrons capture and release process. In addition, the accumulation conductance does not

change with temperature, which demonstrates that there is a channel-carrier communication with the NIOTs by tunneling [14].

In this work, G(V) measurements on MOS capacitors biased in accumulation were used as a direct method to detect and characterize NIOTs with energy levels aligned to the SiC conduction band (CB) edge, which is responsible for the μ_{fe} reduction [13, 14, 38, 39]. The evolution of conductance values with frequency when the device is biased in accumulation (at 15V) is shown in Fig. 2.25, for both samples with and without boron. It can be seen how the conductance value (and hence the amount of traps) is approximately one order of magnitude lower in the sample with boron at any frequency value.

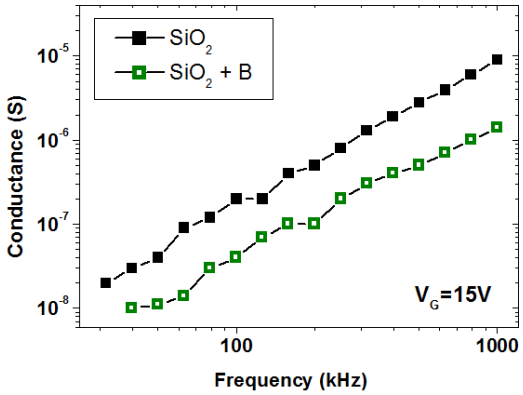


Figure 2.25 Accumulation conductance evolution with frequency for capacitors with and without B (V_G=15V).

The accumulation conductance increase at higher frequencies indicates that the density of NIOTs increases closer to the SiC/SiO_2 interface, thereby having shorter tunneling distances resulting in shorter tunneling times [14].

2.4.3 Subthreshold method

D_{it} value can also be extracted from the Id-Vg curve. It is known as the subthreshold slope method, which allows us to extract the D_{it} profile directly from a MOSFET transistor instead of a MOS capacitance. This method is very useful for performing in situ complete studies of MOSFETs. The $I_D=f(V_G)$ is typically measured at V_{DS}=0.1V and D_{it} is extracted with the formula [6, 40]:

$$\frac{dV_G}{d(\log_{10} ID)} = \frac{kT}{q} ln10 \left(1 + \frac{C_{DEP}(2\phi_B)+qD_{it}(SS)}{C_{ox}}\right) \quad (2.31)$$

Then:

$$D_{it}(SS) = \frac{1}{q}\left(\left(\left(\frac{dV_G}{d(log_{10}I_D)} \cdot \frac{q}{kT} \cdot \frac{1}{ln10}\right) C_{ox} - C_{ox}\right) - C_{DEP}(2\phi_B)\right) \quad (2.32)$$

where we are considering the D_{it} ≈C_{it}/q in $cm^{-2}eV^{-1}$ instead of the theoretical $D_{it}=C_{it}/q^2$ as explained previously. In Eq. 2.32, ϕ_B and C_{Dep} are obtained with:

$$2 \cdot \phi_B = 2\frac{kT}{q} \cdot ln\left(\frac{N_a}{n_i}\right) \quad (2.33)$$

$$C_{Dep}(2\phi_B) = \frac{\varepsilon_0 \varepsilon_{SiC}}{W_{DEP}} = \sqrt{\frac{\varepsilon_0 \varepsilon_{SiC} kqN_a}{2 \cdot 2(\phi_B \pm V)}} = \sqrt{\frac{\varepsilon_0 \varepsilon_{SiC} kqN_a}{2 \cdot 2(\phi_B)}} \quad (2.34)$$

In Eq. 2.34 we are assuming that the channel is not biased, which means that channel voltage (V_c) and bulk voltage (V_B) values are zero. The depletion layer capacitance is $C_{Dep}(2\phi_B)$ because we are considering the maximum depletion region width ($2\phi_B$), since the space-charge region cannot expand anymore.

As seen before, in both CV and subthreshold method cases, the challenge is the need for a representation of the data versus its energy position related to the conduction band (n-type) or valence band (p-type). In order to calculate the D_{it} energetic position, we use the same expressions; Eq. 2.25 and Eq. 1.2, where the surface potential used corresponds with its weak inversion value:

$$\psi_S = \frac{C_{OX}}{C_{OX} + C_{DEP}} V_{GS} \quad (2.35)$$

2.4.4 Charge Pumping

In the last decades, charge pumping current techniques (CP) have arisen as a powerful characterization tool to assess the semiconductor/dielectric interface in Si MOSFETs [33, 34], and recently they have been successfully applied on 4H-SiC MOSFETs [41-43]. Early work on this topic has been done previously in the group. In order to complete the previous studies, some special structures have been included in our new mask set. As it happens with the subthreshold method, one of the main advantages of the CP method is the availability of data on the SiC/SiO_2 interface by directly measuring a MOSFET transistor rather than measuring a MOS capacitor.

The technique of CP is based on the interaction between the interface states and the free carriers (both, in the valence and conduction bands) of the semiconductor. It is related to a recombination mechanism which obeys to Shockley-Read-Hall statistics [44] taking place in the SiC/SiO_2 interface. When several trapezoidal pulses are applied to the transistor's gate, it generates a cyclical filling and emptying of the interface states. This process is schematically shown in Fig. 2.26 for an nMOSFET; when the device is biased in inversion mode, there is an injection of electrons from the source and the drain to the channel, and some of these electrons are captured by the interface states. After that, when the device is brought to accumulation, the free electrons conforming the inversion layer will come back to source and drain regions, and the electrons trapped at the interface states will recombine with holes provided by the bulk P^{++} contact. This process causes the appearance of a current called charge pumping current (I_{cp}), directly related to the density of interface states in a bandgap energy range. The charge pumping current is related to the applied pulse frequency and the recombined charge (Q_{cp}) as follows [42]:

$$I_{cp} = f Q_{cp} = f q A_G \overline{D_{it}} \Delta E \tag{2.36}$$

Where f is the pulse frequency, Q_{CP} is the recombined charge, A_G the gate area and $\overline{D_{it}}$ is the average density of trapping states measured within the allowed energy region ΔE.

As we are directly measuring an electric current (charging and discharging interface states), this method, unlike capacitive measurements, is not affected by R_s introduced in Eq. 2.11, which value depends on frequency.

This technique has been applied in this work using the design shown in Fig 2.26, where N^+ and P^+ implantations were performed over the P-type epitaxied samples. For some reason attributed to the geometry of the structure, the results obtained did not scale properly with the channel length. It seems than

in our test structure design, the P^+ implantation (bulk contact) was too close to the N^+ source and drain contacts area. New structures are going to be fabricated.

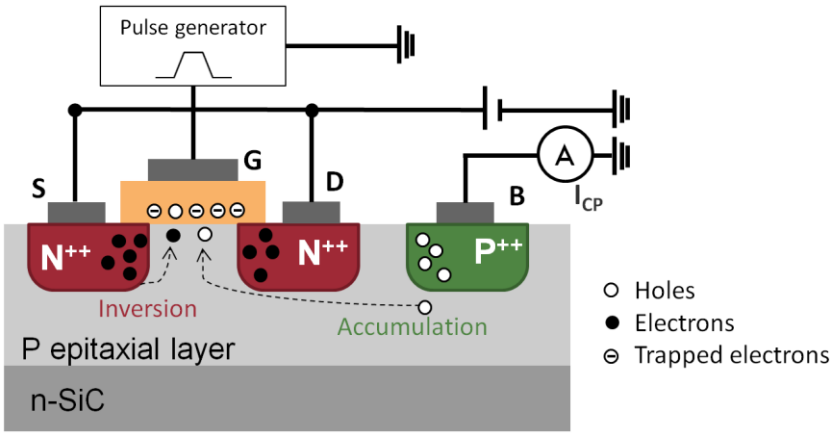


Figure 2.26 Schematic setup for charge pumping measurement on a SiC n-channel MOSFET. Where it is shown how electrons flow into the channel from Drain and Source regions when the interface is in inversion, and how holes from the p+ (or bulk) contact are trapped in the interface states in the interface accumulation condition.

2.4.5 D_{it} techniques summary

It should be clarified that, despite considering that the study of GV measurements on MOS capacitors biased in accumulation were the best direct method to detect and characterize NIOTs with energy levels aligned to the SiC conduction band, we have also used other techniques for several reasons:

1. Silicon technology has historically used the CV technique and a lot of the published research in SiC (also by our group) has been carried out with this technique. In order to be able to compare our results with previous works, we have analyzed the CV curves several times.

2. On the other hand, sometimes MOS capacitors equivalent to the studied MOSFETs were not available. For example, when working with 6H-SiC nMOSFETs. Hence, the quality of the interface was evaluated using the subthreshold method directly on MOSFETs. This way we were able to get an idea of traps reduction in 6H-SiC MOSFETs by using boron treatments.

3. As shown in Table 2.1, where the different methods for interface states characterization are classified, it would be better to use the charge pumping instead of subthreshold method since it is a direct method, but our actual designed architecture for CP is not working properly. We are currently working on the improvement of charge pumping devices.

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Section 2

Gate Oxide Improvement

Chapter 3

Objectives

The main purpose of this work is to propose a suitable and reliable fabrication process that can improve one of the major issues in SiC technology, the gate oxide (and interface) quality, by combining different fabrication techniques. With this goal, we have to improve the main electrical parameters of current SiC MOSFET structures.

We have implemented lateral nMOSFETs in 4H-SiC with improved electrical characteristics compared with the ones which can be found in literature and market nowadays: mobility values higher than 25 $cm^2V^{-1}s^{-1}$ (pursuing a goal of 300 $cm^2V^{-1}s^{-1}$ which corresponds to one third of the bulk mobility); high threshold stability and high gate breakdown voltage with a thin gate device able to work properly at high frequencies and high temperature regime. The state of the art, on different techniques carried out in the literature for this purpose, are detailed in Paper I.

On the one hand, in order to passivate the SiC/SiO_2 interface, reduce the D_{it} value and thus to increase the obtained mobility, we contemplated to start from our existing oxynitridated oxide of 42 nm thick and over it apply some process variations and additions. We specifically focused on the boron diffusion through this gate oxide. The first objective would be to obtain a device with boron diffusion coupled with a nitrogen rich interface, that improves or at least equals the good results obtained by Okamato et al (μ_{eff}=100$cm^2/V{\cdot}s$) [1]. Then, combination with a CVD TEOS oxide will be tested to increase the main thickness of the gate dielectric. The idea is to have a very thin N+B thermal oxide combined with a CVD TEOS deposited oxide forming the main thickness of the oxide. The details and results obtained through this procedure are explained in Paper II.

We would also try to improve it, with the optimal oxynitridation and annealing procedures, in order to also improve the reported MOSFET instability. Some relevant data is shown in Papers II, III and IV, where the results obtained from different B dopings, and Nitridation process (NO instead of N_2O from different providers) are detailed.

The main objective is not only to improve the μ_{fe} value, but also to understand how the processes carried out on the oxide impacts on the interface and near interface traps, as well as on the scattering phenomena involved in the carriers mobility through the channel. The scattering model that explains the reduced μ_{fe}

value in 4H-SiC MOSFETs is discussed in Paper III. The impact of nitridated boron doped oxides on NIOTs reduction is studied in Paper IV by comparing 4H and 6H-SiC polytipes MOSFETs electric behavior.

In a second phase we will study some high-k dielectrics, such as Al_2O_3 or $Zr_xSi_yO_z$ compounds, to ultimately find an optimal material and thickness to have a good device performance in terms of electric field distribution, gate leakage and reliability. Results obtained with some $Zr_xSi_yO_z$ compounds are detailed in Paper V.

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Chapter 4

Results

Paper I

Advanced processing for mobility improvement in 4H-SiC MOSFETs: A review

https://doi.org/10.1016/j.mssp.2017.10.030

https://www.sciencedirect.com/science/article/abs/pii/S1369800117318978

Paper II

Impact of boron diffusion on Oxynitrided gate oxides in 4H-SiC metal-oxide-semiconductor field-effect transistors

https://doi.org/10.1063/1.4996365

https://aip.scitation.org/doi/10.1063/1.4996365

Paper III

Evidence of channel mobility anisotropy on 4H-SiC MOSFETs with low interface trap density

https://doi.org/10.4028/www.scientific.net/MSF.963.473

https://www.scientific.net/MSF.963.473

Paper IV

Comparative study of boron doped gate oxide impact on 4H and 6H-SiC N-MOSFETs

https://doi.org/10.1016/j.mssp.2019.01.016

https://www.sciencedirect.com/science/article/abs/pii/S1369800118319309

Paper V

Analysis of $Zr_xSi_yO_z$ as high-k dielectric for 4H-SiC MOSFETs

https://doi.org/10.4028/www.scientific.net/MSF.924.939

https://www.scientific.net/MSF.924.939

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which correspond to the articles cited here,
on each publisher's website

Chapter 5

Discussion

Since the first studies on SiC MOSFETs in the early 90s, many technology developments and testing experiments have been performed to improve its initial low channel μ_{fe} values. Since 2000, Si-face off-axis cut 4H-SiC turned to be the material of choice for fabricating power devices. Most efforts on material growth have been done toward this polytype, particularly, aiming at defect reduction and increasing the wafer size. However, the poor quality of the SiO_2/SiC interface severely limits the value of the channel field-effect mobility, especially in 4H-SiC MOSFETs. Several strategies have been addressed to overcome this issue. As explained in Paper I, nitridation methods are broadly used to improve μ_{fe} values, being commonly used in the production of commercial power MOSFETs. However, mobilities obtained with nitridation are still rather low compared with bulk mobility values, reaching the limits of acceptable values. Moreover, with the availability of first pre-commercial power MOSFET devices, new issues such as V_{th} instabilities have appeared.

In recent years different strategies, alternative to nitridation, have been addressed for a further μ_{fe} enhancement. Most of these techniques can be grouped depending on if they are based on the use of doped gate oxides, high-k dielectrics or different 4H-SiC crystal orientations.

The B incorporation in the oxide allows a strong μ_{fe} increase, up to remarkable values of 160 cm^2/Vs. When combined with nitridation, devices show good stability at room temperature, but start to drift significantly above 100 °C. More efforts are needed to solve this problem, so that B doping can be eventually validated as a solution for SiC MOSFETs. Another remark is that using improvement of interface based on incorporation of foreign atoms, like N, P, B, Ba, La, it seems that the thinner the layer, the better in terms of interface passivation, stability and reliability [1]. Indeed, the optimization of N, P or B treatments shows that the higher the concentration, the better the obtained results. This means that this is not really doping which is efficient, but the formation of a new material with atoms concentration of the order of the atoms concentration of Si and C. The fact that B strongly improves the mobility also draws some attention, as it is not a n-dopant like P, As, Sb, N, and, in addition, it is a small size atom. Then, atomically, B itself is pretty different from other atoms, yet also allowing an increase of the mobility.

Then, a general tendency on 4H-SiC Si-face seems to be that a μ_{fe} increase is counter-balanced by degradation in both stability and reliability. It has been highlighted that measurement methods inherited from Si technology are not appropriate for a 4H-SiC MOSFET characterization. In recent years, much attention has been paid to the correct measurement of the V_{th} stability, proposing new non-relax or high-speed non-relax testing methods.

Technologically summarizing, the results comprehensively shown in Paper I indicate that the SiC surface oxidation must be minimised to reduce the generation of carbon based defects, and to reduce the compressive stress caused by the oxidation process.

Then, we will deepen on some of the results obtained throughout this thesis (also reported in the presented papers) that we believe are important to highlight, since they help to better understand the charges behavior in the SiC/SiO_2 interface and its effect on MOSFET devices.

5.1 MOS capacitors

It has been previously reported that N^+-ions implanted into 4H-SiC n-MOS capacitors previously to the oxidation process, to force the N presence at the interface, cause a shift of V_{FB} to negative voltages [2, 3]. This fact is due to the generation of a positive fixed charge, Q_F, which is either located in the oxide or at the SiC/SiO_2 interface. A similar behavior is obtained in our oxinitridated samples, which have a high N concentration. All samples where N was involved in the SiO_2 growth process, either in NO or N_2O ambient, show a V_{FB} shift to negative voltages. The N unwanted negative V_{FB} shift has been previously compensated by adding Al at the interface which generates negative charges [3]. Similarly to Al atoms, B is also expected to be able to diffuse through the SiO_2-Network, acting either in the bulk of SiO_2 layer or at the SiC/SiO_2 interface. The above explained V_{FB} shift can be seen in Fig. 5.1 (a) and (b). It is shown the normalized capacitance results obtained on n-MOS capacitors with different dielectric characteristics. Three different curves can be seen in Fig. 5.1 (a), corresponding to:

a) Sample with SiO_2 (grown in N_2O ambient). With a thickness of 30nm.
b) Sample (a) where a B treatment is done through the oxide. Final thickness of 60 nm.
c) Sample (b) where the SiO_2, containing N and B, has been partially removed and a PECVD TEOS oxide has been deposited on top. Final thickness of 85 nm.

On the other hand, samples shown in Fig. 5.1 (b) correspond to:

d) Sample with SiO_2 (annealed in NO ambient). With a thickness of 50nm.

e) Sample (d) with a B treatment done through the oxide. Final thickness of 70 nm.

f) Sample with SiO_2 (grown in pure NO ambient), with a higher N surface concentration. With a thickness of 20nm.

g) Sample (f) with a B treatment done through the oxide. Final thickness of 45 nm.

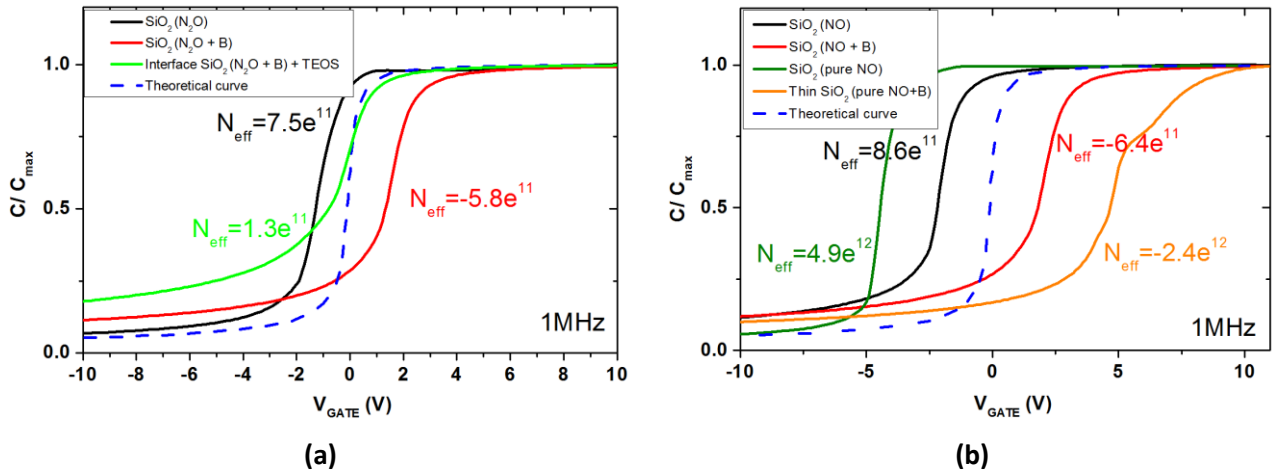

Figure 5.1 (a) CV curves obtained with different oxides based on N_2O grown SiO_2, including the N_{eff} value [cm^{-2}] obtained in each case. (b) CV curves obtained with different oxides based on NO annealed/grown SiO_2, including the N_{eff} value [cm^{-2}] obtained in each case.

As it can be seen by comparing Fig 5.1 (a) and (b), N presence implies a higher V_{FB} shift in NO than in N_2O annealed samples. This behavior had been already reported in Si technology [4, 5], concluding that NO process provides more control of the nitrogen incorporation process (an order of magnitude increase in the nitrogen concentration for the same thermal budget) as compared to that of an N_2O process.

The obtained results are in accordance with the fact that channel mobility obtained in NO annealed MOSFETs is higher (lower D_{it}) than that obtained in our N_2O annealed MOSFETs as a result of a better surface passivation. The V_{FB} shift phenomenon (and N_{eff} value) is also higher when a thin dielectric is grown in pure NO reaching a higher N concentration in the SiC/SiO_2 interface. When the B treatment is done over the samples, the negative V_{FB} shift is compensated, or also overcompensated due to the high amount of B atoms effect, showing a higher positive shift, when the amount of the expected N in the interface was higher. It can be speculated that, as in the case of Al [3], B atoms ionize, by trapping mobile electrons (acting as interface acceptors) and hence, this fixed negative charge causes a large positive V_{FB} shift. This effect can be also seen in Paper III, Fig. 4.

Actually, as can be seen in Eq. 2.19, the V_{FB} depends not only on the N_{eff} value, but also on the oxide thickness T_{ox}. Hence, due to the wide range of T_{ox} values we have used on the studied samples, it is more

reliable to compare directly the N_{eff} than the V_{FB} values. N_{eff} values have been added in Fig. 5.1. These values have been obtained for each curve, using Eq. 2.19 where usually $\Phi_{MS} = V_{FB}^{ideal}$. It can be seen that, as expected, the N_{eff} value is higher in samples annealed in NO than in N_2O, and is also higher in samples with pure NO nitridation. The obtained values have different sign depending on whether the average charge into the oxide is positive or negative.

The obtained results are in accordance with nitridation theory explained in Chapter 1. As shown in Fig. 5.2, the amount of trap density depends on the nitrogen density in the dielectric. While the amount of NIOTS and electron trapping decrease when increasing N density, the amount of h^+ trapping highly increases, when increasing the N density.

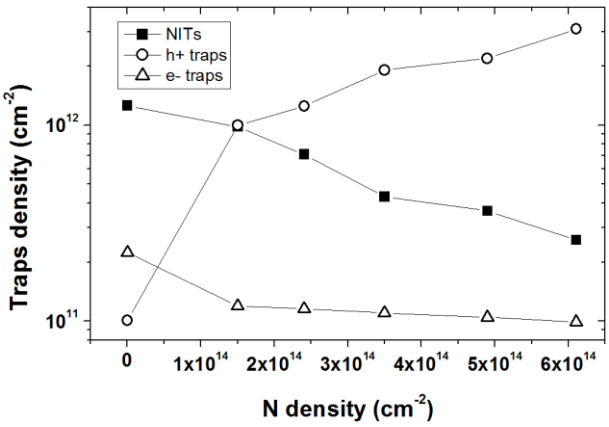

Figure 5.2 Different traps densities as a function of nitrogen density. (Adapted from [6]).

A possible explanation to the dependence of the B-related positive V_{FB} shift and the N content into the dielectric is the suppression of B diffusion via the SiO_2 nitridation. This phenomenon and its impact on the gate oxide integrity had been deeply studied in Si CMOS technology, in MOS and MOSFET devices with p^+-polysilicon (heavily doped with B) as gate material [7-11].

Then, assuming that nitridation is acting as a B diffusion barrier, the higher B effect (higher positive V_{FB} shift) when the N concentration is increased could be explained by the generation of a dipole. There is a direct relation between the amount of N and the B concentration. As higher the N barrier, higher the dipole, and hence the voltage applied in the gate is screened, producing the measured V_{FB} shift.

Although looking at SIMS analysis results (Paper II, Fig. 1) boron could seem to slightly diffuse into SiC. This is because there is some "memory effect" due to the high boron amount in SiO_2. To check this in our work the SiO_2 was removed, and a SIMS analysis was done again. No boron was detected when the oxide had

been removed. We also performed some electrical measurements on the samples were the boron treated oxide had been removed. The samples were annealed in order to activate the possible impurities and promote the B diffusion. We metalized them to form diodes. The fabricated diodes behaved as Schottky diodes, showing that there weren't any active B in the sample. So we can conclude that B is almost uniformly distributed inside the thermally grown oxide, and no active B was detected at the SiC surface. It agrees with the idea that nitrogen acts as a barrier of boron atoms into the channel.

5.2 MOSFET

5.2.1 Remarks on Mobility

Scattering effects

The MOSFETs with the boron treatment done on NO and N_2O previously grown thermal oxides had been also tested at high temperatures. The general tendency of samples without and with the boron treatment is shown in Figs. 5.3 (a) and 5.3 (b) respectively. In B doped samples the μ_{fe} decreases with temperature independently of the V_G value. This behavior differs from the features regularly seen in nitride oxides previously mentioned [12] but it is conform to the new model described by Katsuhiro et al. [13], which takes into account the optical phonon scattering effect (Eq.1.13).

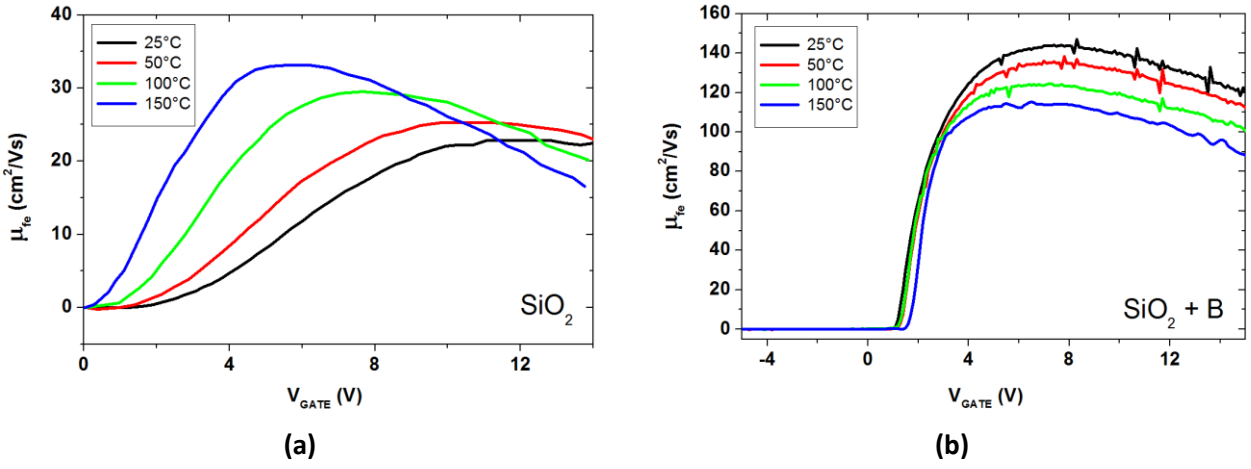

Figure 5.3 (a) Mobility obtained at different temperatures in a N_2O nitridated gate oxide. (b) Mobility obtained at different temperatures in a N_2O nitridated gate oxide with the boron diffusion process.

By comparison of the samples with and without boron, we can conclude that in both cases, a temperature increase supposes an increase in the transconductance curves verticality (subthreshold slope). However, the

mobility value varies differently in each case; in the first case mobility increases with temperature, while in samples with boron, where the electron trapping effect has been reduced, the mobility decreases with temperature. Changes on V_{th} value are discussed in section 5.2.2.

Similar behaviors have been reported and discussed in paper III for NO nitridated gate oxides, where thanks to the increase on mobility values obtained with B treatment, and different scattering effects affecting each measurement, mobility anisotropy can be systematically detected in 4H-SiC MOSFETs. Having higher mobilities in an orientation such that the current flow parallel to the 4H-SiC surface steps, in the $[1\bar{1}00]$ direction.

Due that we are working with 4°off axis samples, in a regular MOSFET with channel length L, where the current flows perpendicular to the SiC steps the effective distance traveled by an electron would be longer than L, while it would be ideally L when the current flow occurs parallel to the steps. Intermediate length values are expected for intermediate angles. This fact is shown in Fig. 5.4. The μ_{fe} anisotropy cannot be directly attributed to this fact since, as reported in Paper I, crystal orientation has a relevant impact in MOSFETs performance. For an entire understanding of anisotropy phenomena, it must be taken into account the differences reported on MOSFETs fabricated on (0001) or $(11\bar{2}0)$ surface. For instance, mobility can change in more than 1 order of magnitude depending on the SiC face. Oxidation kinetics also changes (Paper I).

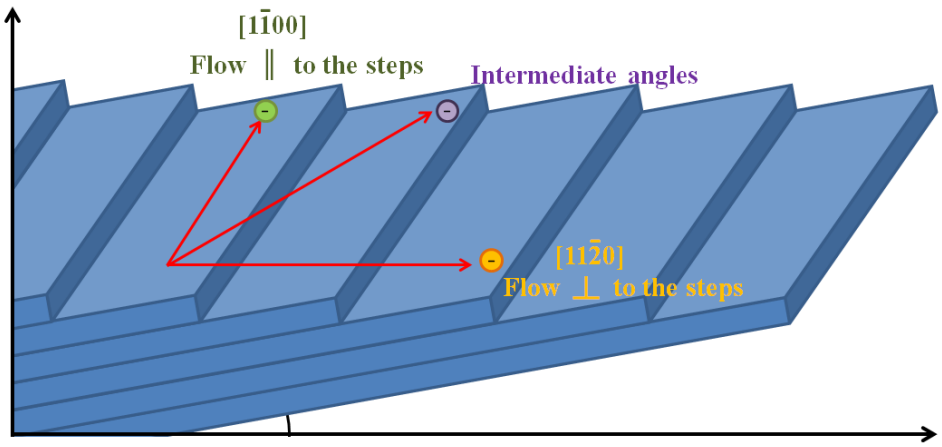

Figure 5.4 Different current flow directions through the 4°off 4H-SiC STEPS.

As it is indicated in the Paper III, anisotropy could be important for planar power MOSFETs with square or hexagonal cells configurations, where unbalanced current could appear. However, as the channel mobility also decreases when increasing temperature, current filamentation could be self-limited and the transistor

could remain stable despite having channels in different orientations. A SEM image and a schematic of this kind of MOS previously done in the group are shown below, in Fig. 5.5.

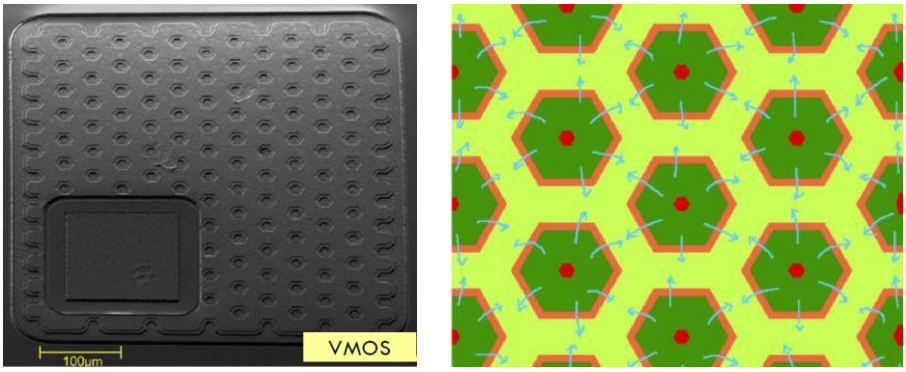

Figure 5.5 SEM image and schematics of MOSFETs with hexagonal cells configuration.

Mobility dependence on channel length

An important phenomenon observed repeatedly along this thesis is how the μ_{fe} decrease as channel length (L) decreases, as it can be seen in Paper IV, Fig. 5. This behavior has been previously reported in Si [14]. We have observed this phenomenon in several MOSFETS with different SiC/SiO_2 interface properties. μ_{fe} variation with L is shown in Fig. 5.6 for samples with a CVD deposited SiO_2, samples with a NO-ambient grown SiO_2, and samples with thermal oxide and a B treatment; as it can be seen the tendency is almost the same, being more pronounced in the B doped samples. The data in Fig. 5.6 is shown in bars of values instead of singular points in order to schematically visualize the full range of values obtained with equivalent MOSFETs from different furnaces and hence slightly different oxides.

On the other hand, we have extracted the R_{ON} versus the channel length. As it can be seen in Eq. 1.6 R_{ON}/L is proportional to μ^{-1}, hence the L impact on the R_{ON}/L value must behave oppositely to μ_{fe}, decreasing when L increases. The obtained values correspond to Fig. 5.6 inset.

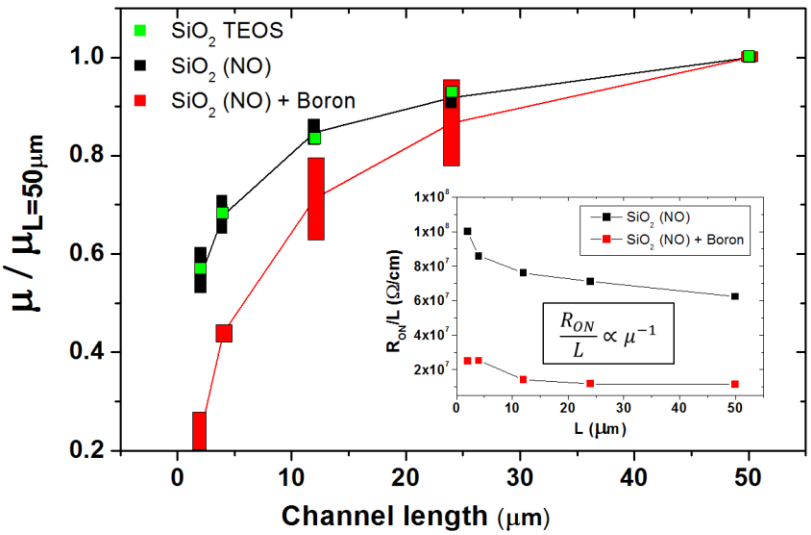

Figure 5.6. Normalized mobility value as a function of channel length L, for different kind of oxides in 4H-SiC MOSFETs. The behavior of the CVD TEOS (low interface quality, μ_{fe}≈1 and then high R_{ch}), is similar to an oxide grown in nitrogen ambient (better interface quality, μ_{fe} ≈25 and lower R_{ch}). On the other hand, with B treatment, (μ_{fe}≈100), larger mobility variation with L reduction is achieved. It is attributed to optical phonon scattering. The inset image shows R_{ON}/L evolution with L of nitridated samples with and without boron that verifies the mobility variation L.

Contrary to what is mentioned in some previous works, this tendency cannot be attributed neither to contact resistance (which is very low compared to channel resistance) nor to the oxide process because the same effect is obtained in 4H-SiC MOSFETs with extremely different channel properties. From our understanding, the μ_{fe} dependence on L should be attributed to phonon scattering effects, as proposed in [15]. For non-polar semiconductors, such as Si, carrier scattering that significantly affects the mobility is due to the presence of acoustic phonons and ionized impurities. However, in polar semiconductors, such as in SiC, other phenomena like polar-optical phonon scattering remain significant [15]. The carriers drift velocity (v_d) in a semiconductor is the product of the electric field and the low-field mobility. By reducing the channel length L, E increases and hence the electrons drift velocity v_d increases. When L is further reduced and electron kinetic energy reaches the optical phonon energy (around 104 meV for 4H-SiC) at the top of the valence band, the entire energy of electrons proceeds to produce optical phonons; thus v_d saturates [15] producing this effect on the channel mobility.

On the other hand, the mobility evolution with L differences seen between the samples with and without the boron treatment is attributed to differences in phonon scattering susceptibilities.

SiC polytype

As can be seen in Paper I, the reported μ_{fe} values in 4H-SiC and 6H-SiC devices fabricated under identical conditions are quite higher in 6H-SiC polytype despite having half the bulk electron mobility of 4H-SiC. These unexpected results highlighted the fact that more comprehensive analysis of the SiC/SiO_2 interface is required in order to deeply understand the effect of the electrically active defects responsible of SiC MOS devices performance degradation.

In Paper IV, the effect of boron treatment is studied in 4H and 6H-SiC MOSFETs identically fabricated. The differences in the μ_{fe} improvement, when doping with B, are related with a different location and density of NIOTs in both polytypes. Since B supposes a higher improvement in 4H-SiC MOSFET performance, where the amount of NIOTs close to the conduction band edge is higher, the B treatment performance is directly related with a reduction of NIOTs.

It would be interesting to repeat this procedure on 3C-SiC samples to verify if, thanks to its narrow band gap (compared to 4H and 6H-SiC), the effect of the NIOTs disappears when doing the B treatment, obtaining higher improvements in the mobility.

5.2.2 Remarks on threshold voltage

Temperature behavior

In theory, the normal trend of V_{th} is to decrease when increasing the temperature for two reasons: a) The Fermi level approached the midgap (less V_{GS} is needed to move surface potential to the inversion condition), and b) the detrapping of negative electrons at the channel interface (since trapped electrons are more easily emitted) [16]. This standard behavior have been seen in MOS samples with a N_2O process previously developed in our group [17].

However, as it can be seen in Fig. 5.7 (a) (Paper II, Fig. 7) in both samples (with and without boron) we observe a positive V_{th} shift around 125°C. This is thought to be due to an increase in the number of trapped electrons into NIOTs at elevated temperatures; at high temperatures the electrons distribution becomes wider, reaching higher energies in the band gap. Similar behaviors have been published in NO samples [16].

Furthermore, around 250°C, in boron passivated samples (where a reduction on NIOTs is expected), the number of available NIOTs decreases as most of them are filled with trapped electrons. Then, the first

mentioned effect (a) predominates again and V_{th} value decreases anew with temperature. This last V_{th} decrease was not reported previously (as far as we know) because up to now the amount of NITs was higher than the one reached thanks to the B treatment. This phenomenon is observed independently of the channel length (Fig. 5.7 (b)).

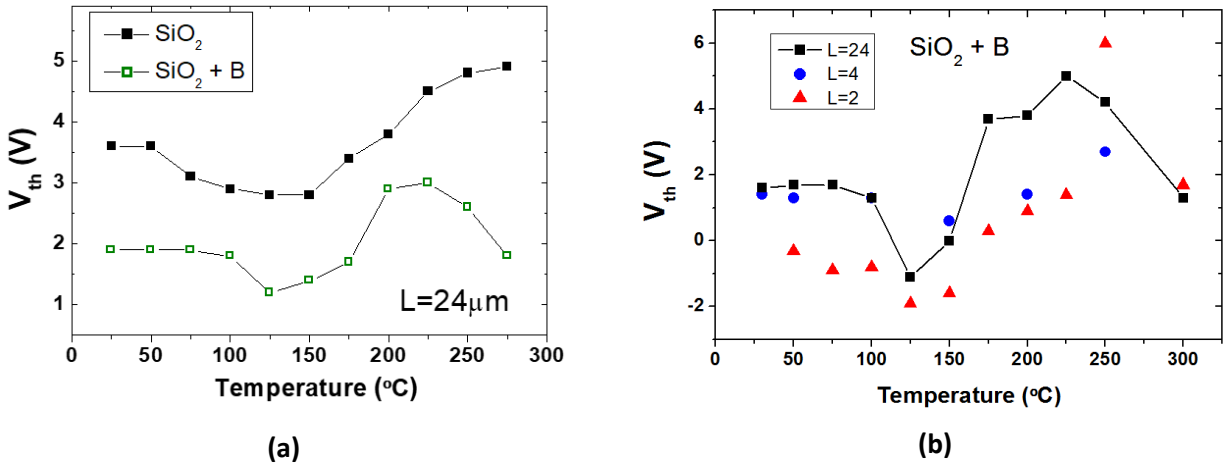

Figure 5.7 (a). V_{th} evolution with temperature of 4H-SiC MOSFETs with a regular N_2O ambient grown SiO_2 (Fig. 7 of Paper II). (b) V_{th} evolution with temperature of 4H-SiC MOSFETs with a regular N_2O ambient grown SiO_2 doped with boron at different channel lengths.

BSI Measurements

Some results obtained during this thesis with NO annealed oxides, after a PBSI and after a NBSI, are shown in Fig. 5.8. The V_{th} variation is very low, showing a slight decrease for PBSI measurement at room temperature, probably due to some charges in the oxide. When rising up in temperature, there is an activation of defects in the oxide as additional trap centers, increasing the V_{th} positive shift during PBSI. On the other hand, the V_{th} variation also increases during NBSI at high temperature. It is consistent with electrons tunneling to and from oxide traps near the SiC/SiO_2 interface [18]. Some works attribute the negative shift of V_{th} during a NBSI to the hole trapping effect [19, 20]. This is consistent with Fig. 5.8 (b) where V_{th} value saturates quickly with stress time, as expected when ΔV_{th} is caused by hole trapping.

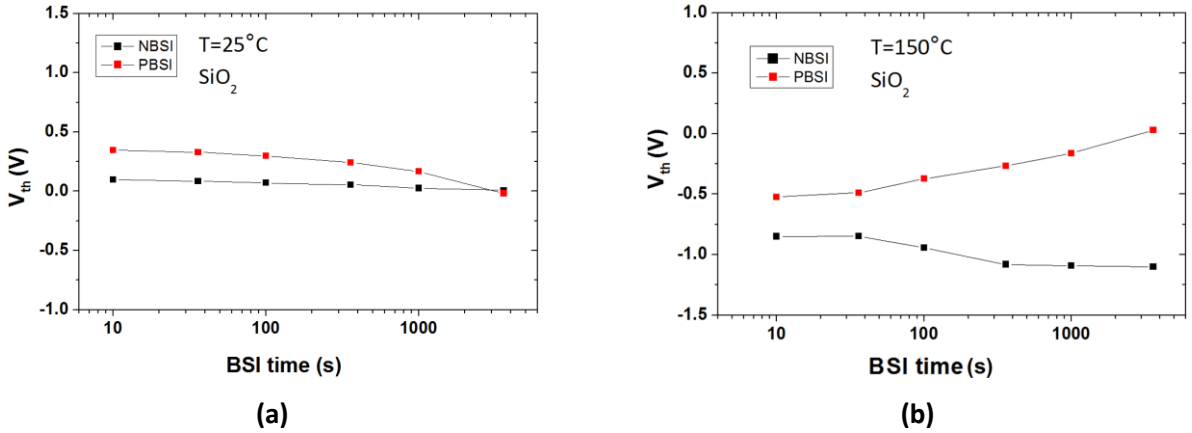

Figure 5.8 (a) V_{th} obtained for a NO annealed sample when appling a 1 hour long BSI test at room temperature. (b) V_{th} obtained for a NO annealed sample when appling a 1 hour long BSI test at 150°C.

Some of the BSI results obtained in samples were boron process has been implemented are shown in Fig. 5.9. The good V_{th} stability observed at RT (Fig 5.9(a)) is not maintained when the temperature is increased, as shown in Fig.5.9 (b). In this test the V_{th} value has been strongly modified after a stress step time of 1h. Nevertheless, the V_{th} value is recovered after the BSI test is stopped. If no mobile charges are present in the oxides, a PBSI stress must generate a positive V_{th} shift, and a NBSI will produce a negative V_{th} shift due to electrons filling or emptying interface traps and NIOTs, in response to the applied electric field. Anyhow, it has been previously reported than between 100°C and 225 °C, the results vary depending on the manufacture source and process [18], being common to obtain negative ΔV_{th} during a PBSI and positive ΔV_{th} during a NBSI. This behavior, seen in our boron samples, is due to the presence of mobile ions (B atoms in our case), which become mobile enough to move as the temperature increases.

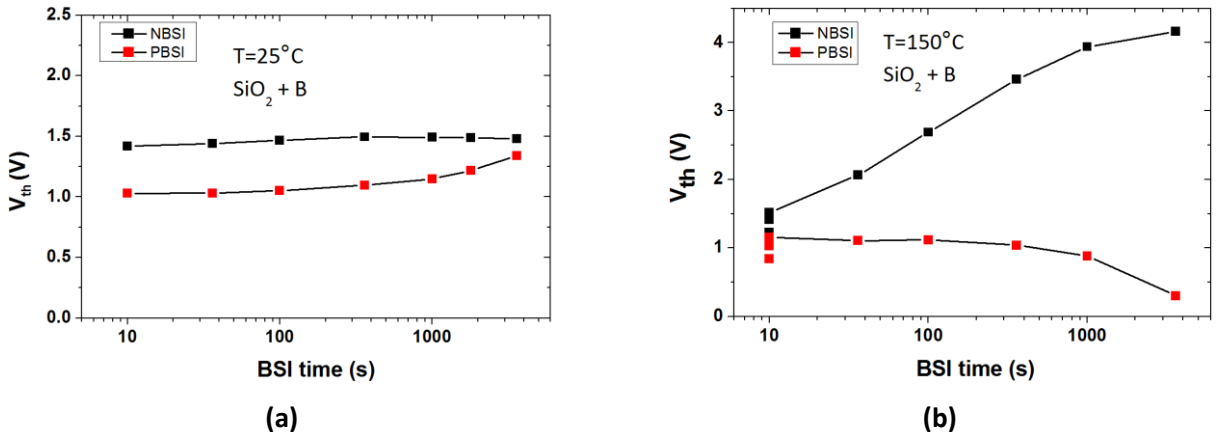

Figure 5.9 (a) V_{th} obtained for a B doped sample when appling a 20-hours long BSI test at room temperature. (b) V_{th} obtained with a B doped sample when appling 1-hours long BSI test at 150°C. V_{th} value recovers after the test.

While it's accepted that the main mechanism causing a shift in V_{th} at room temperature is the charging of NIOTs via direct tunneling mechanism [21, 22], the stress time determines which oxides traps may change charge state during the bias stress. The longer the stress, the deeper into the oxide the affected traps (deeper tunneling), resulting in larger V_{th} instabilities [21]. These traps located deeper from the SiC interface inside the oxide will not change charge state during either a positive or negative bias stress, producing a larger hysteresis in V_{th} [21].

The device stability of some devices was evaluated in Paper II with a 20-hours long BSI to be sure that a majority of oxide traps were activated and to properly evaluate the interface quality of samples without and with the boron treatment. Some results can be seen in Fig. 5.10 *(Fig. 6 of Paper II).*

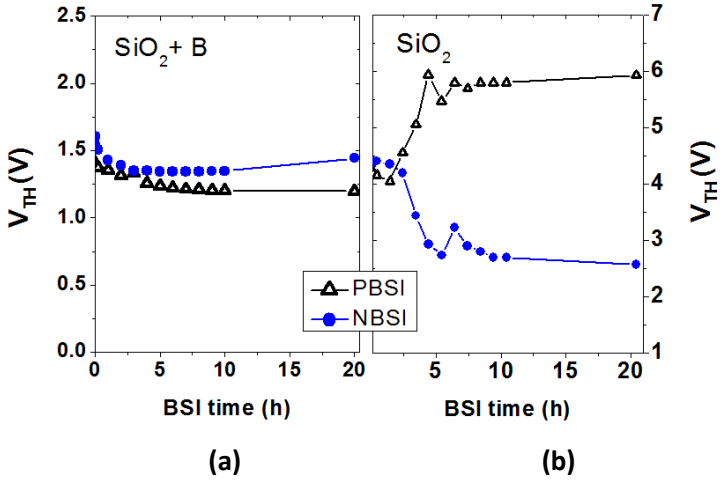

Figure 5.10 Positive and negative V_{th} variations of a MOSFET (a) with and (b) without B after a 20h BSI test *(Fig. 6 of Paper II).*

Nitridated samples without B showed a high V_{th} shift after approximately 3h of stress (not seen in standard 1h test). It's shown a PBSI increase of 2V and a NBSI decrease of 2V. In contrast, the MOSFETs fabricated with B doped gate dielectrics shown a reasonable V_{th} stability at room temperature up to 20h, indicating a possible B effect passivating nitrogen related positive charges in the oxide. This effect agrees with the results obtained in MOS capacitors where we analysed the N_{eff} variation when doping nitridated samples with B was performed (Chapter 5.1).

5.2.3 High-*k* dielectrics

As introduced in Paper I, the low SiO_2 dielectric constant (*k*=3.9) is also a big issue for SiC power MOSFETs. It's widely accepted the use of high-k gate dielectric materials in order to reduce the electric field value for a given dielectric thickness.

Some drawbacks associated to the use of high-k dielectrics are i) their re-crystalization temperature; ii) an increase in the gate leakage due to its reduced bandgap, and iii) a different alignment with the SiC bandgap. To deal with these disadvantages, it is commonly used a thin SiO_2 layer stacked between SiC and the high-k layer.

The high-*k* oxide must act as an insulator. This requires that the potential barrier at each band must be over 1 eV in order to inhibit conduction by the Schottky emission of electrons or holes into the oxide bands.

The main advantage of dielectric proposed in Paper V, $Zr_XSi_YO_Z$ is its higher recrystallization temperature, above 600°C. The $Zr_XSi_YO_Z$ is expected to have a bandgap alignment similar to that defined for $ZrSiO_4$, where the potential barrier is ≥ 1eV. Hence, we thought it would be interesting the use of an interfacial SiO_2 layer in order to increase the bandgap offset and thus reduce the leakage current characteristics Fig. 5.11. However, the effect of using a SiO_2 layer is to reduce the effective *k* of our dielectric stack up to values of 7 or 8 instead of a higher value, the reported $ZrSiO_4$ theoretical value being *k*=12.6 [23].

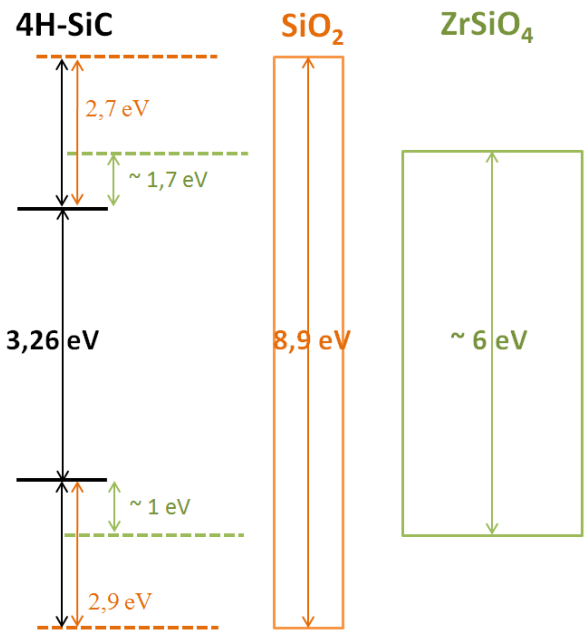

Figure 5.11 Band offset calculations for SiO_2 and $ZrSiO_4$ [24].

Some comparative measurements of breakdown voltage measured on different MOSFETs can be seen in Fig. 5.12. It seems that the B treatment is not compromising the oxide reliability, while that the oxide breakdown is earlier reached by using $Zr_xSi_yO_z$ as gate dielectric, being worse at slower Si/Zr ratios.

When we performed the study reported on Paper V, we had to discard some Si/Zr interesting tested ratios because of the low breakdown voltage values obtained in MOSFETs, after several studies, it was deduced that the main problem of such dielectrics were that there was lateral leakage through the dielectric. The premature breakdown voltage seen in Fig. 5.12 is attributed to this phenomenon. We could manage this problem by dry etching the dielectric areas that were not under the gate (using the metal gate itself as a protective mask), thus breaking the continuity of the leaky oxide between drain, source and gate.

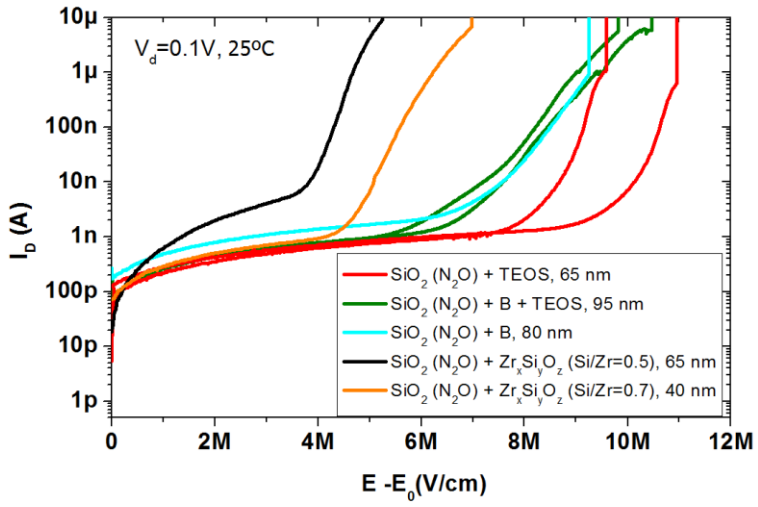

Figure 5.12 Dielectric breakdown measured in MOSFETs with different gate dielectric compositions.

5.3 Global assessment

In most cases, an improvement of the channel mobility and subthreshold slope is accompanied by a decrease of the V_{th}, typically below values required in real devices (3-5V). To compensate the V_{th} decrease, the p-doping could be increased. However, the channel mobility decreases when the doping is increased. Then, other approaches to increase V_{th} should be used.

In Fig. 5.13 (a) some of the results obtained during this thesis when using the boron treatment are shown, the results of other authors are also included in order to compare the obtained results. It can be seen a relation between mobility and V_{th} values. This effect could be worrying for the manufacture of future normally off devices with high field effect mobilities.

In Fig. 5.13 (a) NO set1 and NO set 2 correspond to NO samples provided by different sources. One of the points corresponding to Zheng et al. results [25], seems to be very out of the general tendency. It should be highlighted that it corresponds to a peak mobility value, since their reported mobility values at high voltage has a behavior very similar to ours. This effect has been previously seen in the bibliography with many other dopants [26], as it is shown in Fig. 5.13 (b), depending on the resistance of the channel.

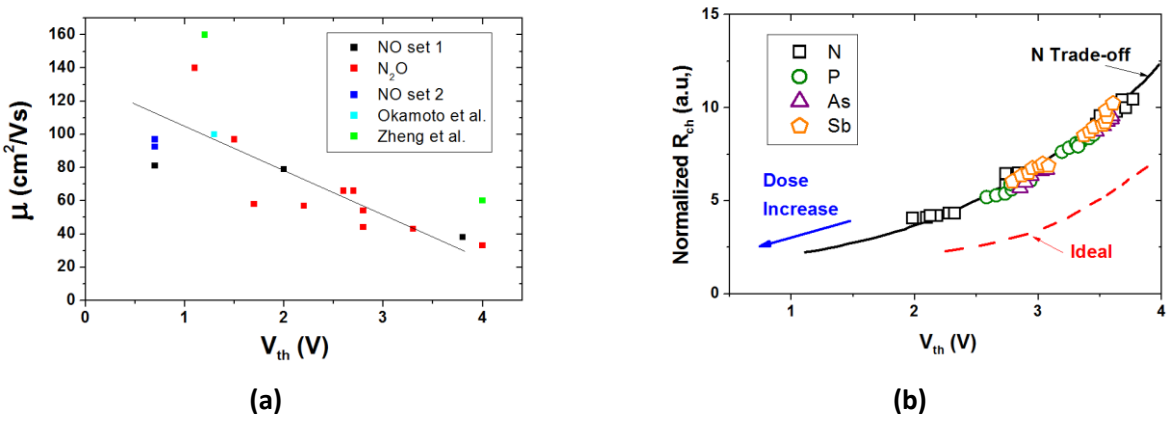

Figure 5.13 (a) Relation between mobility and V_{th} in our MOSFETs (with and without B). Other autors results are included, corresponding to Okamoto et al.[27] and Zheng et al.[25] works. (b) Relation between normalized R_{ch} and V_{th} with N, P, As or Sb doping in p-type well region [26].

During many years, the main focus to improve the mobility was toward a reduction of the interface traps. In Fig. 5.14 left side, can be seen a clear linear relationship between D_{it} decrease and a μ_{fe} increase. However, when including the recent works on B, La_2O_3, high-k, etc, it can be seen that this linear increase of mobility is broken and a kind of D_{it} saturation at a minimum value of $10^{11}cm^{-2}eV^{-1}$ is observed. The mobility can be improved despite the D_{it} is not reduced below those levels (10^{11} $cm^{-2}eV^{-1}$). A minimum D_{it} may have been reached or a lower value cannot be measured with the current test configurations. Another possibility is that interface traps (like ultra-fast D_{it}) are further reduced by the new treatments, but not detected by the usual characterization methods. However, most probably, no more efforts on D_{it} reduction are needed. On the contrary, NIOTs and strain must be improved for further increase of the channel mobility.

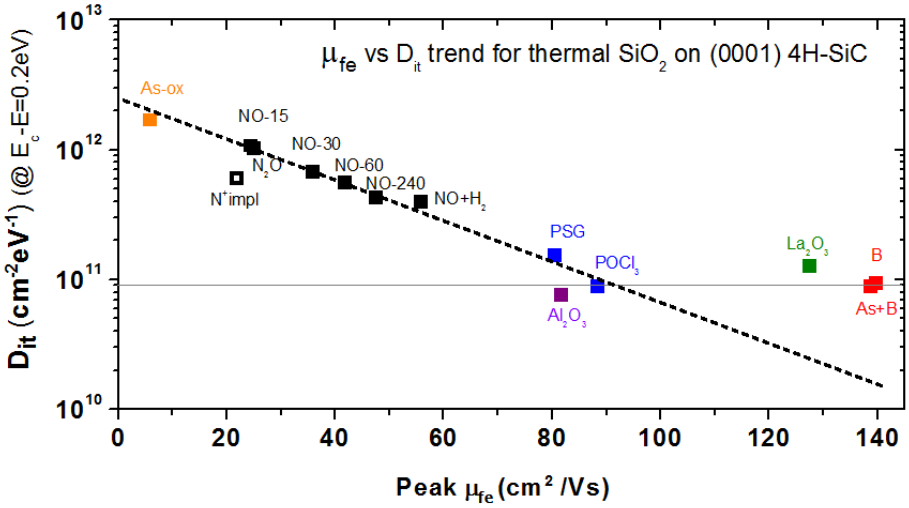

Figure 5.14 Peak field effect mobility at low field (dominated by coulomb scattering) extracted on Si-face 4H-SiC MOSFETs with different thermal oxides and POA, versus corresponding D_{it} at 0.2eV from E_C.

As stated in paper I, today, one of the most promising solutions to combine high μ_{fe} values and good stability seems to use a Ba interface layer on Si face for planar MOS channels, despite the fact the oxide breakdown voltage is low. Another approach is to use of trench or groove gates to build (only) the channel on other crystallographic orientation more favorable to high channel mobilities, like $(11\bar{2}0)$ or $(03\bar{3}8)$. Yet, novel issues appear for these architectures, such as a poor breakdown voltage capability in power devices. More recently, it has been confirmed that generation of carbon at the interface is generating a decrease of the mobility. Then, oxidation of the SiC surface must be avoided as much as possible. The chosen optimization will depend, as usual, on the final application and the specific trade-offs associated with the application.

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Chapter 6

Conclusions and Recommendations

6.1 Conclusions

Off-axis cut Si face 4H-SiC turned to be the material of choice for fabricating power devices, due to its superior and more isotropic bulk carrier mobility. Therefore low channel mobility attributed to the presence of traps either in the gate oxide or into the SiO_2/SiC interface is the main issue to be solved for next generation of power MOS devices. Advanced gate dielectric processes for 4H-SiC MOSFETs improvements are necessary.

Although nitridation process has been proved to reduce the D_{it}, the obtained mobility values are still rather low (less than 5% of the bulk mobility) and it is though that the limit of improvements provided by nitridation has been reached. Alternative strategies for further mobility enhancement have been addressed, being the use of doped oxides a promising approach.

The research findings presented in this thesis deal with the improvement of 4H-SiC MOSFETs gate oxide. An improved performance of the MOSFET gate oxide configuration obtained by a RTO in a N_2O environment (or a NO POA), B diffusion into SiO_2, and PECVD TEOS oxide deposition, has been presented. The combination of N and B in the gate oxide provides much higher channel mobility values. This work therefore contributes to the wider research effort towards improving, and understanding, the performance of SiC MOSFETs in several ways. The major findings and key conclusions that we obtained from this study are summarized below:

- A suitable and reliable fabrication and an adapted characterization process have been found to obtain 4H-SiC MOSFETs with an improved gate oxide (and interface) quality. The final gate oxide obtained by combining a nitridation process with a B diffusion through the gate oxide improves Okamoto's [1] previous results, especially in terms of stability.

- SiC surface oxidation must be minimized to reduce the generation of carbon based defects, and to reduce the compressive stress caused by the high temperature oxidation process. Additionally, when using the incorporation of foreign atoms (N, P, B, Ba …), the thinner the layer, the better in terms of interface passivation, stability and reliability.

- The GV measurements on MOS capacitors have been considered to be the best direct method for D_{it} extraction, especially the measurements in accumulation region to detect and characterize NIOTs with energy levels aligned to the SiC conduction band. However, other techniques such as high-low CV, subthreshold or charge pumping methods are widely used by the SiC community and could be very useful to obtain traps information by comparing measurements.

- The reported higher amount of N in the SiO_2/SiC interface of NO nitridated samples compared with N_2O implies a major Boron interaction at the interface. In CV measurements it can be seen how B compensates the V_{FB} negative shift caused by increasing the N concentration. The dependence of the B-related positive V_{FB} shift and the N content into the dielectric can be explained by a suppression of the B diffusion via the SiO_2 nitridation. Then, the higher B effect (higher positive V_{FB} shift) when the N concentration is increased could be explained by the generation of a dipole. Since the higher is the N barrier, the higher is the dipole, hence the voltage applied in the gate is screened, producing the measured V_{FB} shift.

- The stress at the SiO_2/SiC interface can be reduced by the incorporation of network formers such as Boron. During our diffusion process, B is distributed within the thermal gate oxide. B diffuses through the SiO_2-network acting either in the bulk of the SiO_2 layer or at the SiO_2/SiC interface, without penetrating significantly into the SiC crystal. In our experiments, higher boron concentration is associated with lower interface trap density and therefore higher channel mobility.

- In most cases, an improvement of the channel mobility and subthreshold slope is accompanied by a decrease of the V_{th}, typically below applications required values. To compensate the V_{th} decrease, the P-well doping could be increased. Moreover, an experimental channel mobility increase is generally counter-balanced by a degradation in both stability and reliability. However, the presence of N and B contributes to obtain a proper interface passivation which reduces the D_{it} and NIOTs values and, as a consequence, μ_{fe} increases without compromising the V_{th} stability. A relatively good

threshold voltage stability under both positive and negative bias stress at room temperature has been obtained.

- An improved field-effect electron mobility model taking into account the optical phonon scattering effect at high electric field values fits properly with our experimental data. Although roughness scattering is not the dominant mechanism in the inversion layer mobility, it has an appreciable effect on the mobility anisotropy in 4H-SiC MOSFETs with relatively high mobility, independently of the temperature value.

- A different NIOTs density and energy location can be seen as a possible explanation for the differences in mobility improvement behavior seen in 4H and 6H-SiC polytypes. From this different behavior seen when doing the boron treatment, it can be concluded that boron treatment is effective in NIOTs reduction.

- Typically, a μ_{fe} decrease as channel length decreases is systematically observed in our experiments, as well as in many other reported works. Unlike it is sometimes claimed, this behavior is not due to the contact resistance (which is very low compared to channel resistance) nor to the oxide process. We do attribute this μ_{fe} dependence on L to phonon scattering effects.

- High-k dielectric materials reduce significantly the amount of electric field through the oxide, with equal gate dielectric thickness. Our gate dielectrics stack consisting of a thin SiO_2 interlayer and a $Zr_xSi_yO_z$ layer with an optimal Si/Zr ratio (theoretical Si/Zr=0.7), seems a promising candidate for SiC MOS gate oxide since it has been proved to have a large *k* (double than SiO_2), thermodynamic stability on SiC, a good interface quality (checked in terms of mobility and V_{TH} stability) and process compatibility with SiC technology. The main high-k materials drawback, the leakage current through the gate, in this case can be controlled by carefully select the dielectric parameters and post processing treatments.

- At high voltage and high temperature operation regime, a high mobility value is not necessary as the on-state losses are driven by the drift layer, and not anymore by the channel. The selection of an optimal gate oxide will depend on the final application and the specific trade-offs associated with this application.

- The main focus to improve mobility was toward a reduction of interface traps. When analyzing recent works (doping gate oxide, counter doping, use of high-k dielectrics…) it can be seen a discontinuity in the linear increase of mobility with decreasing D_{it}, until a "minimum" D_{it} value around 10^{11} cm^{-2} eV^{-1}, where this linear relationship is interrupted. It is possible that a "minimum" D_{it} value is still not reached, but that very fast D_{it} are not being detected by the usual characterization methods. However, most probably, no more efforts on D_{it} reduction are needed. On the contrary, NIOTs and strain still must be improved for further increase of the channel mobility.

6.2 Suggestions for future research

- It is necessary to find better processing methods for B diffusion to ensure a B doping homogeneity and repetitiveness through the entire wafer.

- More efforts have to be employed in obtaining thin B doped gate dielectrics, to ensure a very high stability also at high temperatures.

- The B location inside the SiO_2, SiO_2/SiC interface or bulk SiC, as well as which percentage of B is activated inside SiC surface, needs to be more deeply understood. Different authors, with different B doping processes and concentrations, have reached different conclusions. Probably the B is differently located in each case, but the limited knowledge about the mechanisms driving B diffusion into SiC makes difficult to find the proper explanation in each case. In our case, some depth profiling XPS measurements could provide more accurate information about B location and distribution through the oxide, and B interaction with N.

- A new design for the Charge Pumping measurement is necessary to obtain proper D_{it} values.

- Some anisotropy simulation would be very useful to clarify some of the discussion related with Paper III.

- Future works addressed to study the B process effect in 3C-SiC polytype MOS interface are needed. A negligible impact of B treatment in 3C-SiC MOSFETs electrical properties is expected, due to the

lack of NIOTs near the 3C-SiC conduction band. Hence, it would corroborate the results obtained in paper IV.

- Other High-k dielectrics such as BaTiO3, but also more standard AlN and Al_2O_3 should be more deeply explored.

- In order to discriminate between different types of traps, its location and its effect, new standard unified fast electrical measurement procedures to properly characterize the SiC/SiO_2 interface are required.

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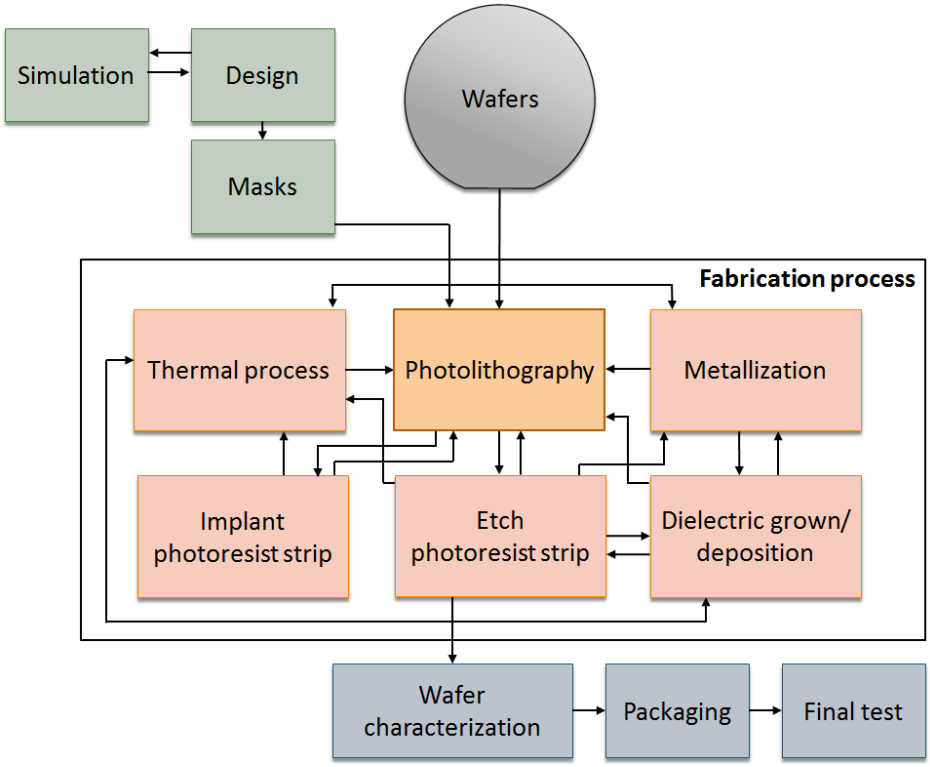
Appendix

MOSFET fabrication process

The typical process flow of a wafer is shown in the figure below. In this section the details on the fabrication process (the main rectangle in the figure) of our samples are specified step by step. The cleaning steps have not been included in the figure, but they will be detailed in each steps listed below.



The fabrication of a regular MOSFET during this thesis requires, first of all, a set of masks with a proper design and validation. The initial material we work with, are 4 inch N-type 4H-SiC wafers, with a p-type epitaxy on top. Although they are not included in the process flow, the cleaning steps are very important. An inadequate or incomplete cleaning or drying can be fatal for the final device reliability.

The first thing we will do is a photolithographic step to be able to define the scribe lines and alignment patterns (etching process). After that, a 2nd and a 3rd photolithography will be done in order to do P^+ (bulk contact) and N^+ (source and drain regions) implantations respectively. After that, the dopant activation annealing is required (thermal process).

Then, the dielectric (or dielectric stack) will be grown or deposited, with the required thermal steps in each case.

Another photolithography is required for contact opening (dielectric etching).

Finally, similar to the dielectric deposition, the contact metals are deposited, with the correspondent photolithographic and etching, or lift off, steps.

In the following pages there are specified: The initial wafer details (1), the cleaning processes details (2) and the different steps followed along the fabrication of one of our regular n-MOSFETs (3-11).

1. 4 inches 4H-SiC wafers

Supplier: Ascatron AB (Kista (Stockholm), Sweden)

Wafer	Epilayer
4H-SiC wafer **thickness= 358 µm** **Si-face (0001), tilted 4.03º** **N-type wafer** **Rho= 0.0219 Ωcm** **Diameter 99.85 mm**	Thickness= (7.0 ± 0.5)µm P-type epilayer [Al] = (5.0 ± 1.5) x10^{16} cm^{-3}

- Doping disuniformity over the wafer < 15% (standard deviation over mean values, 5mm edge exclusion)
- Thickness disuniformity over the wafer < 10% (standard deviation over mean values, 5mm edge exclusion).

2. Complete wafer cleaning:

a. Acetone
b. Isopropanol

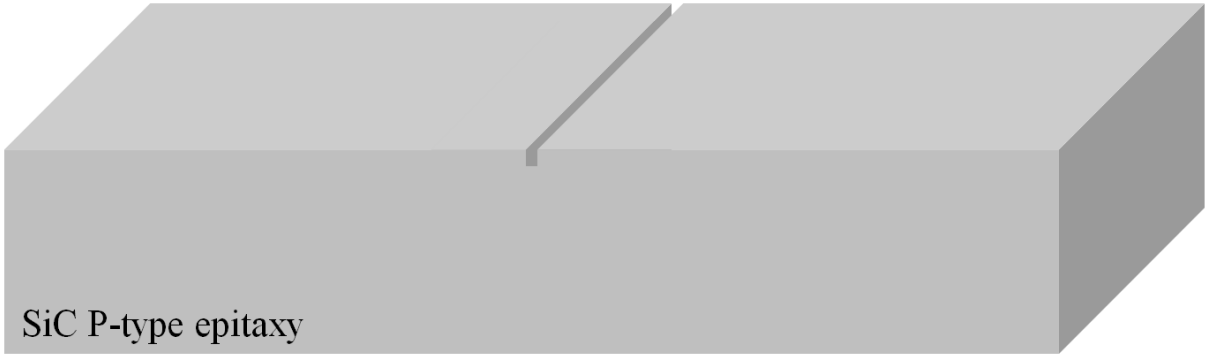
} Steps performed to the samples coming from outside the clean room, or when they can have some organic contamination

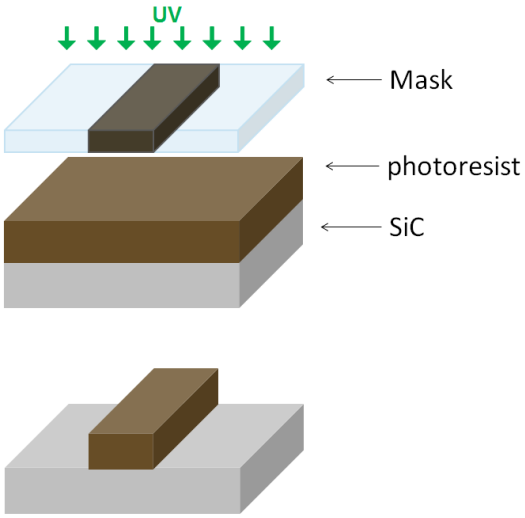
c. Deionized Water
d. Piranha (H_2SO_4 + H_2O_2)
e. Deionized Water

f. HCl / H_2O_2 / H_2O → Step done on pre-oxidation cleanings

g. Deionized Water
h. Dip in HF
i. Deionized Water
j. Dry samples

3. Alignment marks



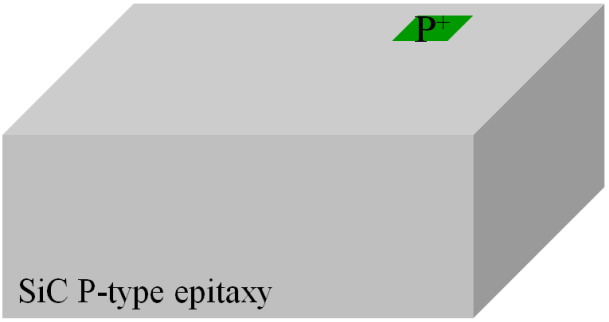


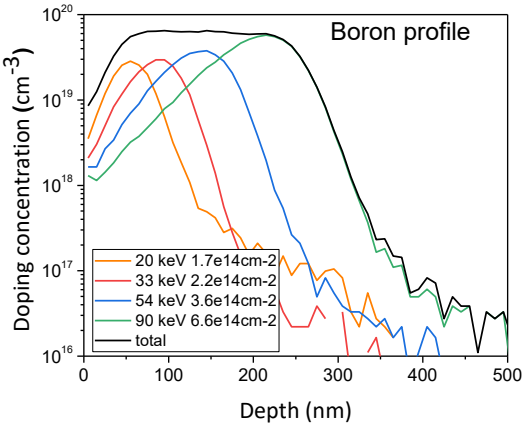
Standard Photolithography (KarlSüss MA 56)
(1st level)
Positive photoresist (Fujifilm, HiPR 6512)
Mask: SiC039-ALIGN

Reactive Ion etching (Alcatel GIR. 160)
time: 4 min
Species: SF_6 and O_2
Power: 100W
Pressure: 5 Pa

Resist removal, (Tepla 300 SA)
O_2 plasma power 1000W

4. P^+ implantation (bulk contact)



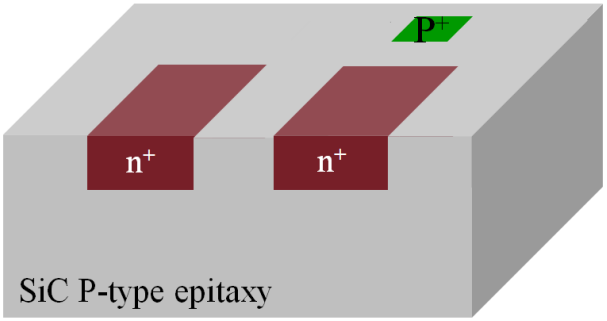


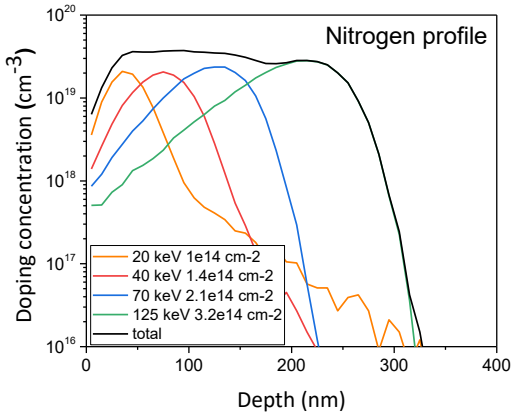
Standard Photolithography (2nd level)
Positive photoresist 6512
Mask: SiC039-PPLU

P-well implantation (Eaton NV 4206)
Boron, 7º tilted, Energies and doses:
20 keV 1.7e14 cm^{-2}
33 keV 2.2e14 cm^{-2}
54 keV 3.6e14 cm^{-2}
90 keV 6.6e14 cm^{-2}

Resist removal, (Tepla 300 SA)
O2 plasma power 1000W

5. N^+ implantation and dopants activation





Dopants activation

Temperature values must be higher than 1600ºC so that the dopant impurities are activated. Higher temperature could produce roughness problems and SiC amorphorization.

Sample cleaning

Standard Photolithography (KarlSüss MA 56)
Positive photoresist 6512
Mask: SiC039-NPLU

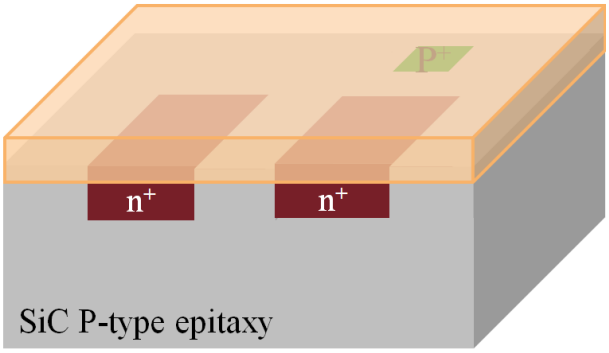
N-well Implantation (Eaton NV 4206)
Nitrogen, 7º tilted, Energies and doses:
20keV 7e13 cm^{-2}
40keV 1e14 cm^{-2}
70keV 1.5e14 cm^{-2}
125keV 2.25e14 cm^{-2}

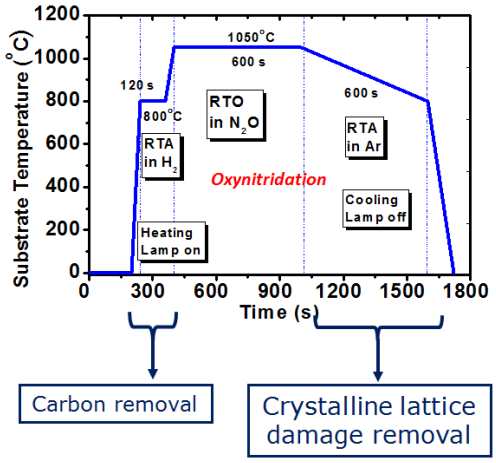
Photoresist removal, (Tepla 300 SA)
O2 plasma power 1000W

Sample cleaning (ensure total SiO_2 removal)

Activation annealing (Centrotherm)
1640°C 20 min → dopants activation

6. Oxide grown





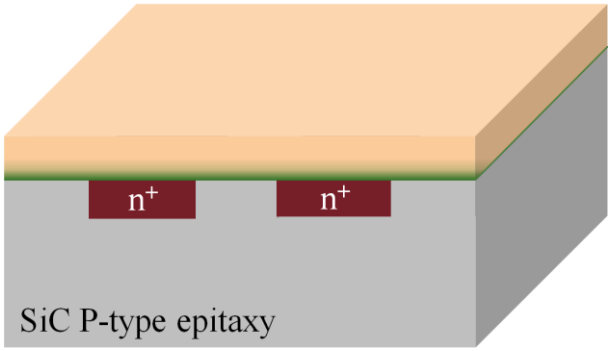
Sample cleaning

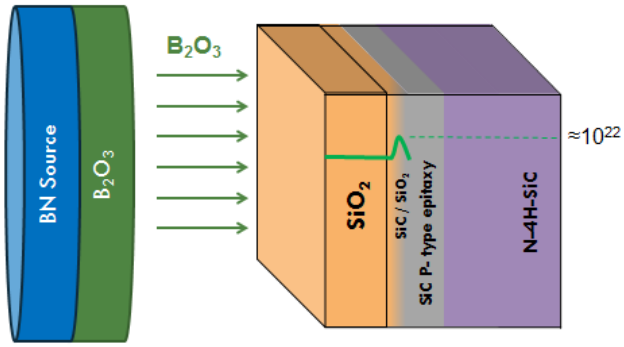
SiO_2 Growth (Jipelec)

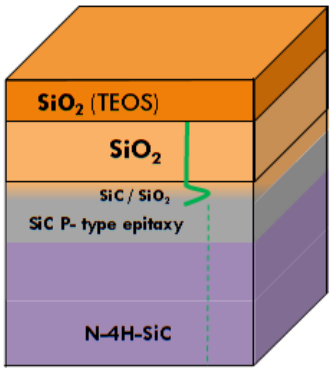
42 nm
RTA in H_2 (120s, 800ºC)
RTO in N_2O (600s, 1050ºC)
RTA in Ar (600s, 1050-800ºC)

SiC consumption ($2SiC + 3O_2 \rightarrow 2SiO_2 + 2CO$)
For each mole of SiO_2 Grown, 1 mole of SiC is consumed

7. Boron doping





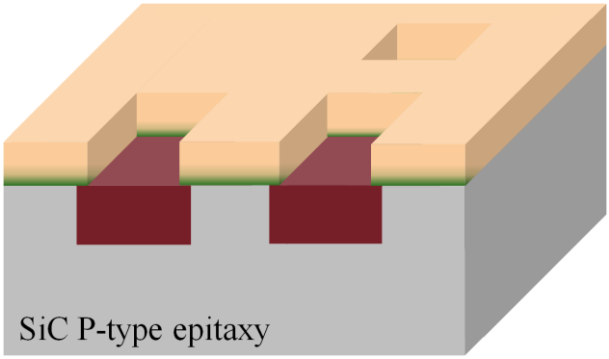


Boron doping process
Samples annealing between BN planar sources, 30 min, 1050-1150°C
boron expected peak concentration (interface) = $10^{22}cm^{-3}$

Oxide top layer deposition, PECVD TEOS 2:1 (AMI precision 5000)
Thickness, 40nm
(This step is not done in all the used/tested devices. It is for increasing the device robustness)

***Ellipsometer**, oxide thickness and optical constant measurement.*

8. Contacts opening



Standard Photolithography (KarlSüss MA 56)
Positive photoresist 6512
Mask: SiC039-cont

Wet* etching (SiO_2)
SiOetch+ Deionized water + dry
Thermal oxide is etched at a ratio of: 90nm/min, or faster when it is boron doped

Microscope optical check

*In addition to the boron doped SiO_2, other dielectric materials have been processed during this thesis (externalized deposition), which required to be **dry**- etched by Reactive Ion etching:

Inductively Coupled Plasma (ICP), (Alcatel AMS 110-DE)

- **SiN_x or SiO_2 etching**,

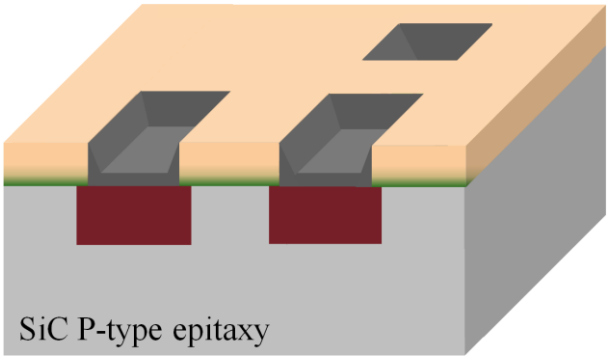
Etching rate: 200nm/min
Species: C_4F_8
Power: 1800W Source, 150W Chuck
Pressure: 1 Pa

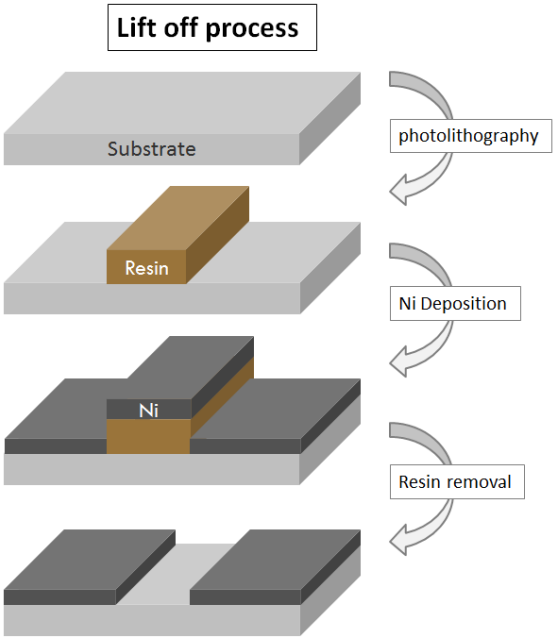
- **$Zr_xSi_yO_z$ etching**,

Etching rate: 120nm/min
Species: SF_6 and O_2
Power: 400W Source, 12W Chuck
Pressure: 1 Pa

Remaining resist is removed by Plasma with PVA Tepla.

9. Contacts metallization (Ni)





Nickel deposition (Sputtering MRC 903)
1000A

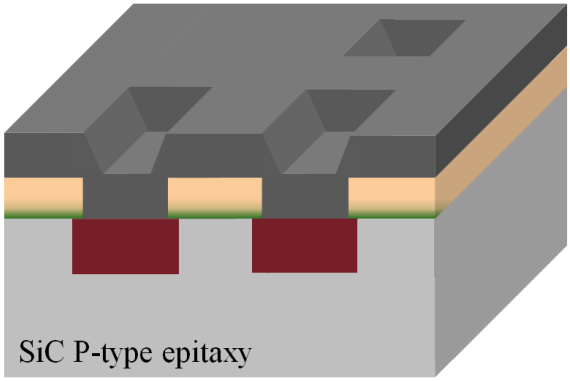
Lift-off, overnight in acetone.

All the resist is removed and the nickel just stay in the areas where Drain, Source and bulk contacts will be located.

Microscope optical check

RTA, (contact annealing)
900ºC 2 minutes in Argon ambient

10. Contacts (and gate) metallization (Al)

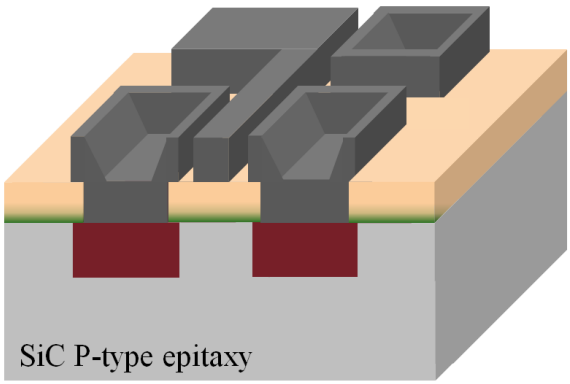


Aluminum deposition (Alcatel A610)
Between 0.5 µm and 1 µm, sputtering

Standard Photolithography (KarlSüss MA 56)
Resin 6512
Mask: SiC039-metal

Microscope optical check

11. Final device



Aluminum etching
Wet etching in Aletch at 45-50ºC in a double boiler (1 µm≈3min)

Microscope optical check

Resist removal
Acetone, Isopropanol, H_2O