STEP UP AND DOWN CONVERTER COMBINED WITH MOTOR INVERTER FOR POWERTRAIN APPLICATIONS

Ivan Ruiz Erni

UNIVERSITAT
ROVIRA i VIRGILI

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Ivan Ruiz Erni

A thesis submitted for the degree of Doctor of Philosophy

Supervised by Dr. Enric Vidal Idiarte and Dr. Francisco Javier Calvente Calvo

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FAIG CONSTAR que aquest treball, titulat "STEP UP AND DOWN CONVERTER COMBINED WITH MOTOR INVERTER FOR POWERTRAIN APPLICATIONS.", que presenta Iván Ruiz Erni per a l'obtenció del títol de Doctor, ha estat realitzat sota la meva direcció al Departament d'Enginyeria Electrònica, Elèctrica i Automàtica d'aquesta universitat.

HAGO CONSTAR que el presente trabajo, titulado "STEP UP AND DOWN CONVERTER COMBINED WITH MOTOR INVERTER FOR POWERTRAIN APPLICATIONS", que presenta Iván Ruiz Erni para la obtención del título de Doctor, ha sido realizado bajo mi dirección en el Departamento de Enginyeria Electrònica, Elèctrica i Automàticade esta universidad.

I STATE that the present study, entitled "STEP UP AND DOWN CONVERTER COMBINED WITH MOTOR INVERTER FOR POWERTRAIN APPLICATIONS", presented by Iván Ruiz Erni for the award of the degree of Doctor, has been carried out under my supervision at the Department of Enginyeria Electrònica, Elèctrica i Automàtica of this university.

Tarragona, 19 de maig de 2022

El/s director/s de la tesi doctoral
El/los director/es de la tesis doctoral
Doctoral Thesis Supervisor/s

Dr. Enric Vidal Idiarte

Dr. Francisco Javier Calvente Calvo

To all the professors - mentors who throughout my university education encouraged and nurtured my passion for power electronics and research.

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To Dr. Enric Vidal Idiarte, who always with a smile, good ideas, great work and dedication, has accompanied me throughout this thesis as director and also to Dr. Javier Calvente Calvo, co-director who collaborated in setting the roadmap of this thesis and followed its development until its end, contributing with his guidance.

To my parents, to whom I would like to dedicate this step in my academic life, of so much value to them.

Abstract

In the electric vehicle industry, the inclusion of a DC-DC converter between the battery and the inverter has shown to improve the efficiency of the propulsion system and reduce its size. Typically, a boost converter is used as DC-DC, which, although is simple to implement, has high losses, low power density and generates high-frequency electromagnetic noise. This thesis proposes a new step-up and step-down stage combined with the motor inverter that is able to increase efficiency, operate in soft switching, provide galvanic isolation and operate in a wider voltage range, optimizing the propulsion system significantly. The proposed topology is analyzed and a design method is presented to meet the main automotive requirements. Subsequently, the proposed converter is modeled in discrete time and continuous time. With these models, a control for the stage is proposed. In addition, a second control loop is added to improve the efficiency of the system. All the results obtained throughout this thesis are validated experimentally by means of two setups, agreeing previous theoretical and simulated results.

Contents

LIST OF ABBREVIATIONS

PMSM (Permanent Magnet Synchoronous Motor)

EV Electrical Vehicles

EMF Electromotive Force

FWC Field Weakening Control

NVH Noise Vibration Harshness

CCM Continious Conduction Mode

OEM Oriquinal Equipment Manufacturer

DAB Dual Active Bridge

ZVS Zero Voltage Switching

SPWM Sinusolidal Pulse Width Modulation

SVPWM Space Vector Pulse Width Modulation

EPA Enviromental Protection Agency

UDDS Urban Dynamometer Drive Schedule

NYCC New York City Cycle

HWFET Highway Fuel Economy Test

FOC Field Oriented Control

PI Proportional Integral

f_{sw} Swithcing frequency

T_{sw} Swithcing period

i_a Phase a current

i_b Phase b current

i_c Phase c current

v_b Bus voltage

v_{bat} Battery voltage

v_m Phase motor voltage

v_p Primary side voltage

v_s Secondary side voltage

N Transformer turns number

d_1 Primary side duty cycle

d_2 Secondary side duty cycle

ϕ Phase shift

P_o Output power

P_i Input power

P_{cond} Conduction losses

P_{sw} Switching losses

Chapter 1

Introduction

In the wake of climate change and scandals such as diesel gate, governments have encouraged a decrease in CO2 emissions. This includes promoting renewable energies and the use of electric cars. In the latter field, for example, the European Union has set itself the target of having at least 30 million zero-emission cars on the road by 2030 and a ban on the sale of new combustion-engine cars from 2035. As a result, vehicle manufacturers have been pushing for the rapid development of electric vehicles, while conventional propulsion has been put on the back burner. This boom in electric propulsion in the automotive sector in recent years has boosted the use of power converters in vehicles. In today's electric or hybrid vehicle architectures, 3 voltage levels may be present: the high-voltage battery, which is recharged via the electrical grid, the regenerative braking system or the combustion engine. This battery provides power to the traction system and to the 12 V low-voltage system with which most of the vehicle's electronic systems operate. In some cars there is also a 48 V voltage level responsible for systems such as start-stop, regenerative braking energy storage, suspension height adjustment, among others. Due to the large number of DC voltage levels that can coexist in the same car and the search for elimination of additional batteries, DC-DC converters have become indispensable.

The combustion engine, made up of thousands of parts and subject to compliance with a very costly environmental directive that makes its amortization period about 15 years, is replaced by an electric motor. Among the electric motors in the electric vehicle sector, the permanent magnet synchronous, induction and switched reluctance motors stand out. In [1, 2], the following comparison is made between them: The commutated reluctance motor, despite being the most economical, has a low torque density, high noise and high torque ripple, which is the reason why it is only used in very economical vehicles. The induction motor is still an economical solution without noticeable torque vibrations, but, on the other hand, it has a low efficiency rate which makes it unsuitable for a long mileage. Finally, the perma-

nent magnet synchronous motor (PMSM), although being the most expensive due to the need for rare earths, presents high efficiency, high torque density and low torque ripple making it ideal for high performance electric cars.

One of the most used powertrain systems in electrical vehicles (EVs) is the described by Figure 1.1

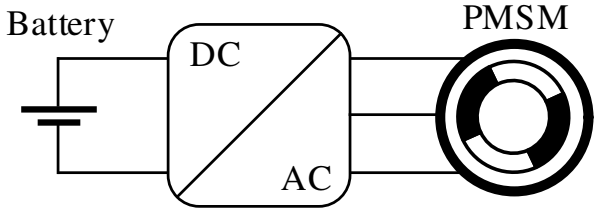


Figure 1.1: Conventional powertrain system converter.

It can be seen that the high voltage battery faces directly the motor inverter. As stated in [3], regarding the number of components the system shown in Figure 1.1 may seem more convincing. However, regarding the performance, the system of Figure 1.2 may prove to be superior.

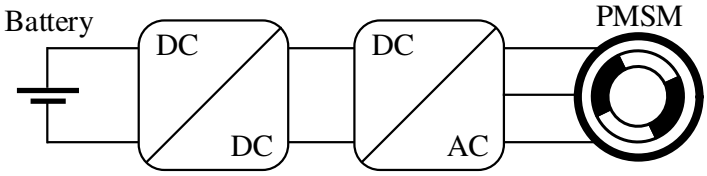


Figure 1.2: Conventional powertrain system with DC-DC converter.

In the system of Figure 1.1 the battery voltage range is very wide, so the inverter is oversized to withstand the full battery voltage and the high currents that flow when the battery is at a lower voltage due to discharge. Similar situation occurs in certain hybrid vehicles where super capacitors are used. In [4], the Toyota's Hybrid System is presented, where a DC-DC is placed between the battery and the motor. Thanks to this DC-DC inclusion, aside from reduce the power losses, by keeping the same size and weight of the engine used in the old Toyota version without DC-DC, the new engine power output is increased by approximately 1.5 times. The reasons of this improvement are explained in [5]. The motor back-electromotive force (EMF) voltage of the PMSM is proportional to the rotational speed. At high speeds, the induced voltage increases noticeable. If this voltage is higher that the one provided by the inverter, which is limited by the battery voltage level in Figure 1.1, it is impossible to control the current that flows to the engine,

specially in discharged batteries that present lower voltages than nominal. This situation in illustrated in Figure 1.3. The torque remains constant as the engine speed ω increases thanks to the inverter control. The induced voltage produced by the motor is higher than the maximum voltage that the inverter can deliver due to the limitation of the battery voltage at ω_{base}. From this point on, flux weakening control (FWC) must be used to further increase the motor speed. So the flux-weakening control of PMSM becomes a hotspot. In PMSMs, as described in [6], the main basis of the FWC is to increase the negative direct axis current and use armature reaction.

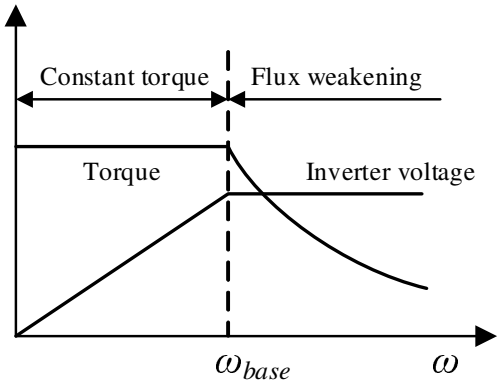


Figure 1.3: Torque versus revolutions.

Summarizing, the motor induced voltage is lowered by FWC. As a result of flux weakening, the output torque for the same current is lower, so efficiency decreases but driving at high rotations speeds is possible. In Figure 1.4, it is shown how the maximum torque region can be extended in the high-speed region if a higher voltage than the motor induced voltage is applied by the inverter.

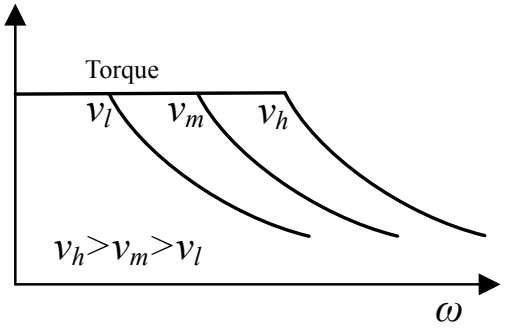


Figure 1.4: Torque versus revolutions at several bus voltages.

[7, 8] describe how varying the inverter bus voltage using a DC-DC converter

as in Figure 1.2 can improve system efficiency. The losses of the system, composed by the inverter, DC-DC converter and the motor; depend on the bus voltage. Motor losses can be lowered if the current flowing through them are minimized. The inverter and DC-DC converter losses are minimized if a lower voltage is used due to reduction of the switching losses. If FWC appears because the inverter voltage is too low, currents will increase and the system efficiency will be reduced. Therefore inverter voltage must be in the limit before FWC appears. That is, the inverter voltage must be slight above the motor induction voltage which depends on the motor conditions. Another interesting point for manufacturers is that the introduction of DC-DC converter allows to decouple the optimum design of the motor inverter and the engine from the optimum point of the battery pack. The introduction of a DC-DC converter can also help to remove the need of an expensive multi-speed transmission while reaching the optimum efficiency and Noise Vibration Harshness (NVH) of the electric powertrain.

The most common structure, used in the previous articles and also appearing in many commercial vehicles such as the Toyota Prius, [9], is shown in Figure 1.5

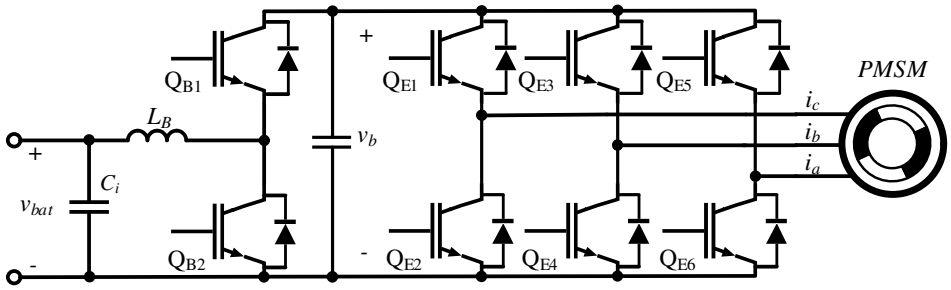


Figure 1.5: Conventional powertrain system with boost converter.

As shown in Figure 1.1, the most utilized topology as DC-DC is the boost converter operating in continuous conduction mode (CCM). The boost converter is preferred and implemented by most OEMs as it is a well-known topology and its simplicity stands out. When the converter has to operate under high duty cycles, ie: reduced v_{bat} and elevated v_b, the semiconductors starts to suffer from significant conduction losses. In addition, the switching devices operate under hard-switching, which is translated into high voltage and current spikes causing additional losses that limits the switching frequency and electrical noise. Thus, the cooling system and the differential and common mode filters needs to be of a larger size and weight. The inductor L_B that ensures CCM and withstand the motor current results also in a large component. As previously commented, the bus voltage must be proportional to the electromotive force, this being proportional to the mechanical speed of rotation of the motor. Therefore, at low speeds a low bus voltage must be used, which increases proportionally with increasing rotational

speed. That means that in certain occasions the DC-DC converter must reduce v_b to a value lower than v_{bat} instead of boosting it. In spite of increasing the DC-Link voltage can bring advantages, it is inefficient at low-speed, low torque and/or low power usage. In that case, a lower voltage would be more beneficial to increase the efficiency. This is an inconvenient of the topology presented in Figure 1.5, which cannot reduce v_b below the battery voltage.

Based on that extra degree of freedom given by the regulated v_b, the inverter variable bus voltage, in [10], a Monte Carlo analysis is performed to generate a look up table with the optimum values of the control variables for several operating points. This task of voltage variation between the battery or fuel cell and the motor inverter is performed by the DC-DC converter. Aside from adjust the output battery voltage to the optimum bus voltage depending on the motor condition, the DC-DC converter allows to use high voltage machines with lower voltage batteries. Thus, the series-connected cells stack and its balancing system can be reduced.

DC-DC converters acting as interface between the battery and the three phase inverter must present the following characteristics:

- High efficiency at maximum inverter peak power.
- Elevated power density.
- Low cost at high, medium and low power.

Based on previous requirements and seeking for an alternative to the conventional boost powertrain system, in [11, 12], several Z and Quasi-Z source inverters like the shown in Figure 1.6 are compared.

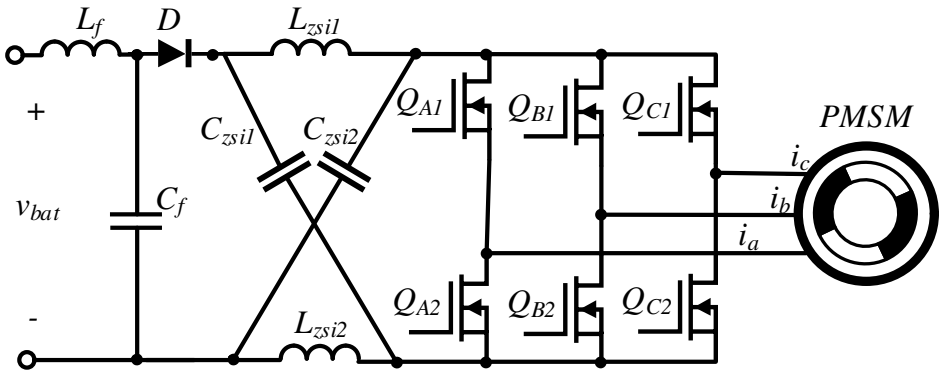


Figure 1.6: Quasi Z-Source Inverter for electric traction system.

In Z or Quasi Z voltage source proposals, low number of components, in particular semiconductors, is achieved, but the required Z-source capacitances and

inductances are relatively large and must withstand large peak voltage and currents.

Other alternative which achieves very high efficiency at all battery and inverter voltages is studied in [13]. A composite converter made of a buck converter in series with DC transformer parallelised with a boost converter is placed between the battery and the inverter. These converters are partially activated or deactivated depending on vehicle battery and motor status. Although high performance is achieved for all loads and battery levels, the size and cost represents a main drawback since several semiconductors/ converters depending on the voltage levels or loads are unused.

From security point of view, most vehicles today have a degree of reinforced insulation between the grid and the battery, mainly affecting the on-board charger. Some manufacturers, mainly french, propose to remove this degree of insulation, while others propose to add one more between the battery and the engine, since in case of impact, it has been seen that some contactors that isolate the engine from the battery fail and the inverter box or the engine casing may be damaged having high voltage levels. In previous solutions there is no galvanic insulation. Recent years, the interest of the application of the non resonant dual active bridge (DAB) for isolated DC-DC power conversion systems has been continuously growing [14, 15]. Its easy soft-switching realization, bidirectional power transfer capability, and modular and symmetrical structure made it a good candidate in automotive application [16–19], fuel-cell and battery storage systems [20, 21] and fuel-cell power-conditioning systems [22].

This dissertation proposes a topology that, in addition to achieve high powertrain system efficiency. It also provides with galvanic isolation, a reduced components number, easy control and implementation. Moreover, comparing with the conventional boost solution the electrical noise is minimized. These characteristics are obtained combining two converters: a zero voltage switching (ZVS) step up and down converter and a motor inverter, which are merged into one single topology.

This thesis is organized as follows: Chapter 2 presents the proposed topology including the description of the operation modes and the mathematical analysis of its waveforms and the study of the losses. Also, a converter design procedure is proposed with an example to match the requirements of the automotive sector and ensure the ZVS condition. The experimental verification is also presented. Further details of this chapter can be found in [23]. Chapter 3, which is based on [24, 25], presents the large-signal and small-signal modelling of the proposed converter. It is important to mention that this thesis does not focus on the motor, nor on the different modulations that the inverter can perform, as they have been extensively studied. Using the above models, Chapter 4 proposes two controllers,

one with each model, to regulate the DC bus. More information of this chapter can be found in [24, 25] An efficiency optimization method is proposed in Chapter 5, which is based on [25]. Finally, the conclusions are set out in the last chapter. The thesis contains two annexes detailing the model used for the design of the magnetic components and the basic modelling of a PMSM rotating the reference frames of AC waveforms to obtain DC levels.

Chapter 2

Combined converter

2.1 Converter introduction

As in Chapter 1 was mentioned, the converter proposed in this thesis pursues the following objectives:

- High efficiency at inverter maximum peak power.
- Elevated power density.
- Low cost at high, medium and low power.
- Isolation.
- Reduced electrical noise.
- Reduced number of components.
- Step up and down the bus voltage.
- Ability to transfer energy in both directions.

As a result of meeting the objectives, the topology shown in Figure 2.1 emerges:

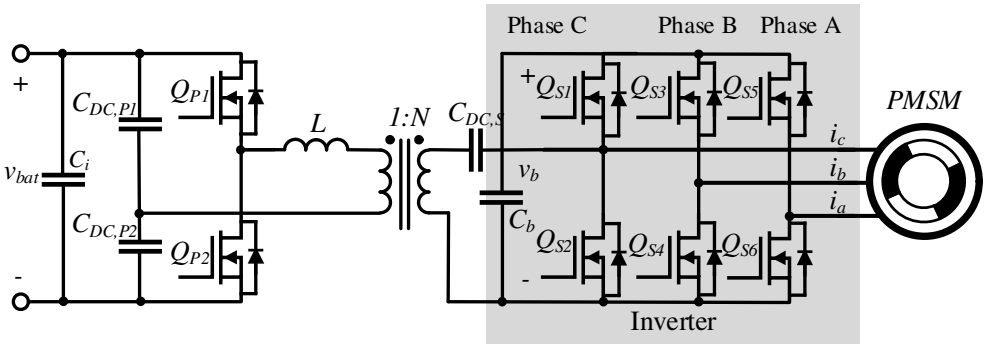


Figure 2.1: Combined step up and down converter.

The converter is composed by the three phases (A,B,C) of the conventional inverter that power the PMSM. This inverter contains six switches (Q_{S1}, Q_{S2}, Q_{S3}, Q_{S4}, Q_{S5} and Q_{S6}) and the bus capacitor C_b. To one branch of the inverter is added the part of the converter responsible for raising and lowering the bus voltage v_b. This step up and down part, joined to phase C in Figure 2.1 consists of at least two switches Q_{P1} and Q_{P2}, a small inductor L in charge of limit and regulate the current and a transformer which aside of providing galvanic insulation, provides with the nominal voltage gain N. In addition, DC blocking capacitors must be allocated to avoid transformer saturation. These capacitors can be placed in split form, as shown on the left side of the transformer $C_{DC,P1}$ and $C_{DC,P2}$, to facilitate filtering or in series, as located on the secondary side of the transformer $C_{DC,S}$. As it can be seen in this case, phase C has to withstand a higher stress than the rest of the phases, since a higher current flows through this phase, which allows the bus voltage to be raised. The simplest option, keeping the chip area of all semiconductors, could be to parallel semiconductors in the most stressed parts: phase C and the step up and down part which also carries all the power. This solution is the most commonly used. For example, in the conventional inverter with boost converter solution shown in Figure 1.5, two or three transistors are usually placed in parallel for each switch of the DC-DC and the use of a big boost inductor results mandatory. Instead, the proposed topology allows the system to be more balanced, so a step up and down stage is placed in each of the inverter phases, resulting in the stage shown in Figure 2.2. In this way, the distribution of currents is more balanced and the sizing of the system and its thermal distribution is simpler. The bus voltage capacitor C_b is keep common to the three phases, so the voltage ripple is reduced close to three times. This solution also allow the activation or deactivation of each step and down stage depending on the power level to maximize the efficiency.

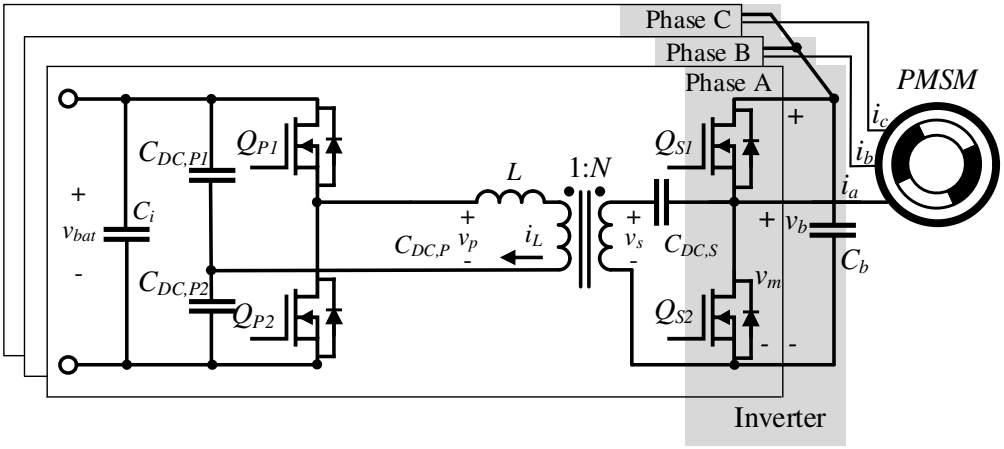


Figure 2.2: Proposed converter placing one step up and down stage at each inverter branch using half-bridge configuration.

The topology in Figure 2.1 is presented mainly to facilitate the reader's understanding. Due to the existing current stress unbalance, it is only recommended for simple low power applications where efficiency is not a major concern and cost is a priority. The nominal gain between the battery voltage v_{bat} and the bus voltage v_b of the proposed topology is given by the transformer turns ratio N, where the maximum efficiency point is located. The proposed stage can regulate around this optimum working point, either by raising or lowering the voltage. As the voltage regulation moves away from this optimum, the efficiency of the stage decreases. A higher efficiency implementation of the topology is represented in Figure 2.3.

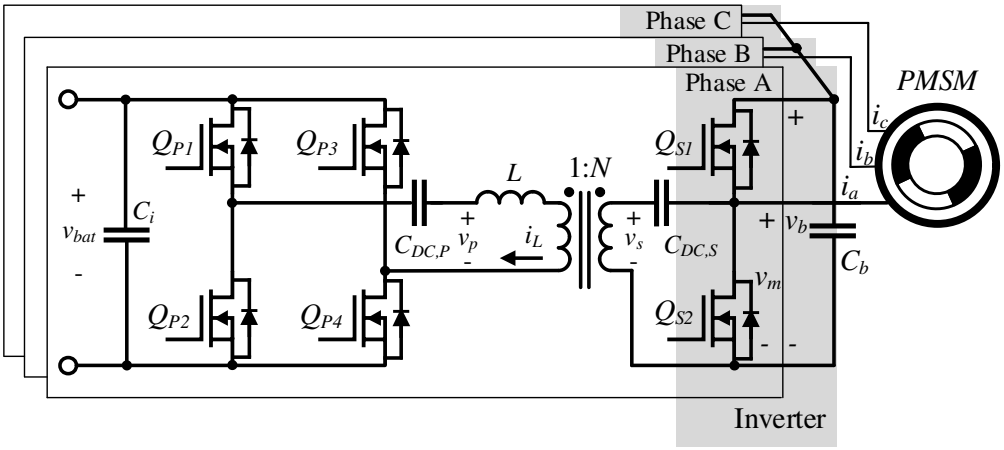


Figure 2.3: Proposed converter placing one step up and down stage at each inverter branch using full-bridge configuration.

This implementation allows operation over a wider range of input and output voltages around the optimum points. The full-bridge implementation allows operation at two optimal points. The first optimum point is $2N$, but if one of the two full-bridge branches keeps the lower switch turned on and the upper switch turned off permanently as in Figure 2.4, the stage becomes a half-bridge and is equivalent to the stage shown in Figure 2.2 with the optimal operating point N.

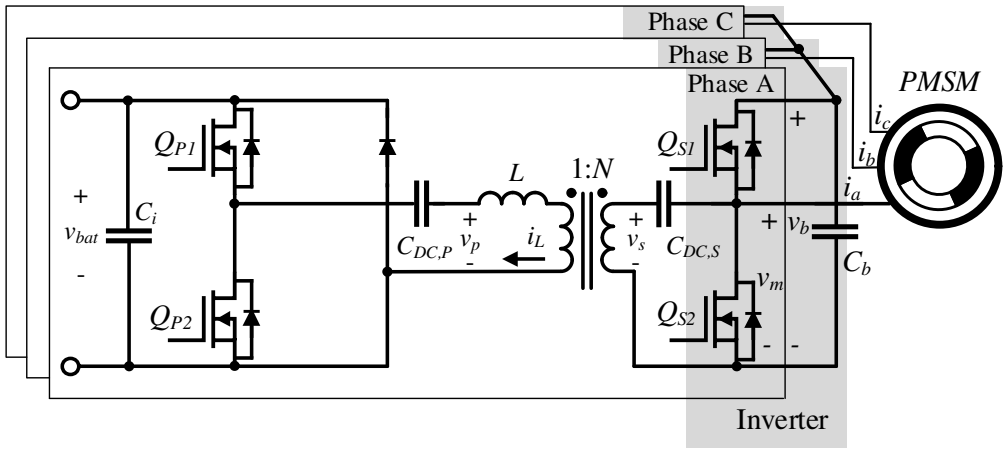


Figure 2.4: Proposed converter placing one step up and down stage at each inverter branch using full bridge implementation and operating under half bridge condition.

In other words, the topology of Figure 2.3 can turn into the topology of Figure 2.2, being allow to switch between two optimum points: $2N$ and N. In such way the main disadvantage of the boost converter when the elevation requirement is high which reduces the efficiency drastically is avoided.

RMS current in the inverter stage semiconductors is slightly smaller, about 10% lower, since part of the power is transferred directly from the primary side transistors to the motor. The other major advantage of the new proposal over the conventional boost converter is the zero voltage switching on the step up and down side. This reduces switching losses and electromagnetic noise.

2.2 Analysis

To facilitate understanding of the topology operation, only one phase, $PhaseA$, of the 3 that make up the combined converter of Figure 2.3, is analyzed below. This analysis is equivalent for each of the three phases that make up the converter. Based on the state of the switches and the direction of the current flowing to the motor, the operation of the converter can be classified into eight states, four when i_a is greater than zero and four when i_a is negative. The waveforms during one

switching period T_{sw} of the inductor current i_L, the primary side voltage v_p and the secondary side voltage v_s for the four states when i_a is positive are illustrated in Figure 2.5. The duty cycle of the primary side voltage is named as d_1, while the duty cycle of the secondary side voltage is denoted as d_2. The phase shift between v_p and v_s is marked as ϕ.

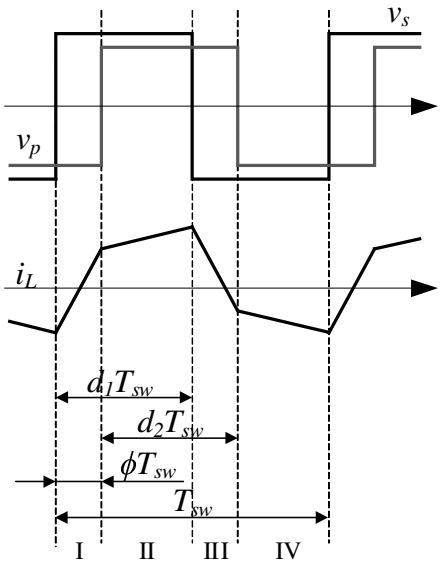


Figure 2.5: Combined converter waveforms.

In the first state, shown in Figure 2.6, Q_{P1} and Q_{P4} are activated, while Q_{P2} and Q_{P3} are deactivated. This generates a positive voltage, $+v_{bat}$, at the first terminal of inductance L, v_p. On the other hand, on the secondary side, that is the inverter side, the lower transistor Q_{S2} is activated, generating a negative voltage $-v_b/2$ on the secondary side v_s. This high voltage difference between the terminals of the inductance generates a rapid increase in the current flowing through it. At the beginning of the switching cycle, i_L is negative, so the diodes will start conducting until the channel of the MOSFET is fully on or i_L reverses polarity in case IGBT. In that state, part of the power is transferred directly from the primary to the motor wingdings.

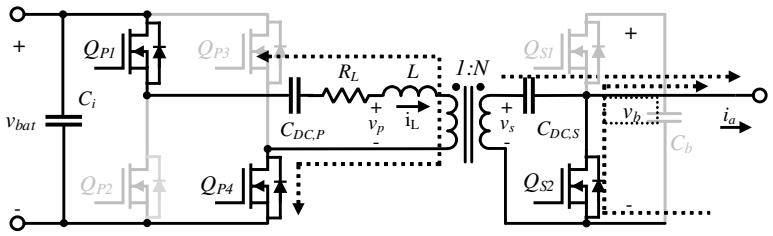


Figure 2.6: Combined converter: State I.

In State II, shown in Figure 2.7, Q_{S2} turns off and Q_{S1} switch on, generating a positive voltage $+v_b/2$ on the secondary side v_s. In that state, the voltage difference between L terminals is relatively small, thus the current hardly varies. Since Q_{S1} is activated current flows in and out of C_b.

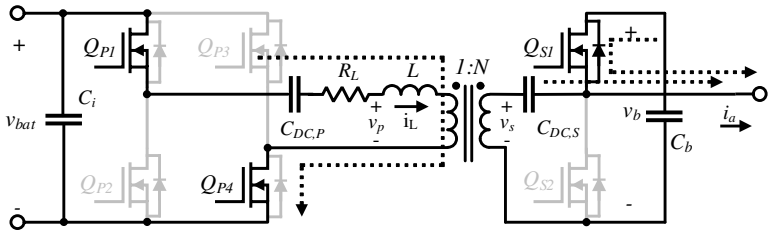


Figure 2.7: Combined converter: State II.

In Figure 2.8, Q_{P1} and Q_{P4} switch off while Q_{P2} and Q_{P3} turn on. When this occurs, the voltage in the primary is reversed to $-v_{bat}$ causing a rapid drop in i_L. Similar to State I, once the transistors Q_{P1} are turned off, current begins to flow through the anti-parallel diodes of transistors Q_{P2} and Q_{P3} before they turn on.

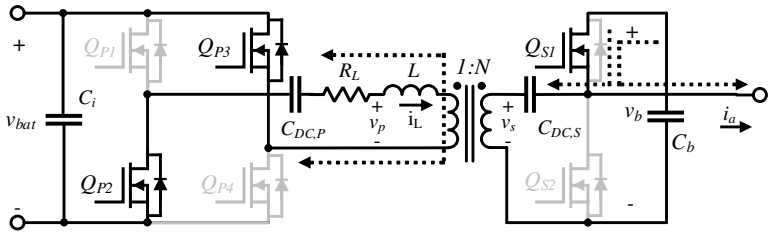


Figure 2.8: Combined converter: State III.

State IV is shown in Figure 2.9 where v_s reverses to $-v_b/2$. Due to the small voltage difference across L, the slope of i_L is low.

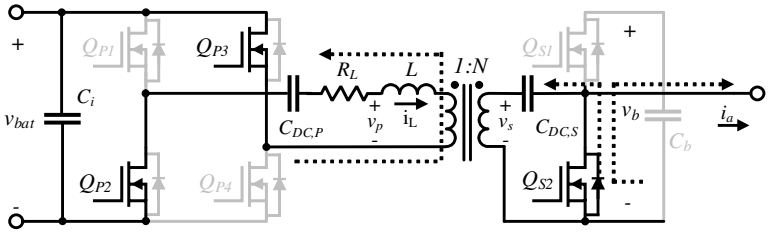


Figure 2.9: Combined converter: State IV.

During this states where $i_a > 0$, C_b is being discharged. Otherwise, when i_a becomes negative, the C_b is charged. This is illustrated in the following figures. It can be seen that now, the phase current flows into C_b.

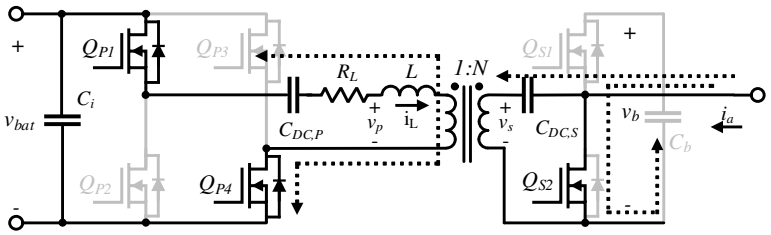


Figure 2.10: Combined converter: State V.

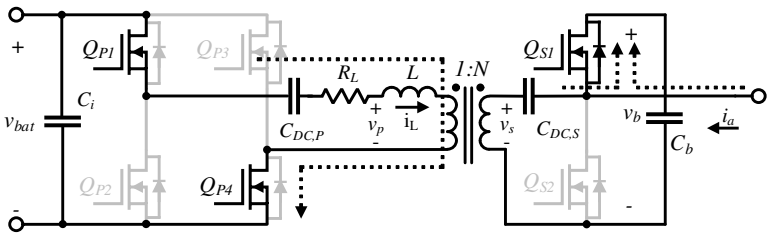


Figure 2.11: Combined converter: State VI.

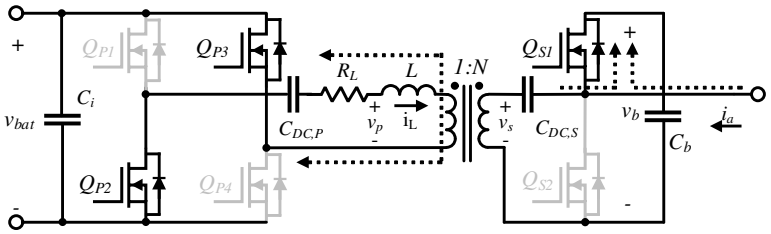


Figure 2.12: Combined converter: State VII.

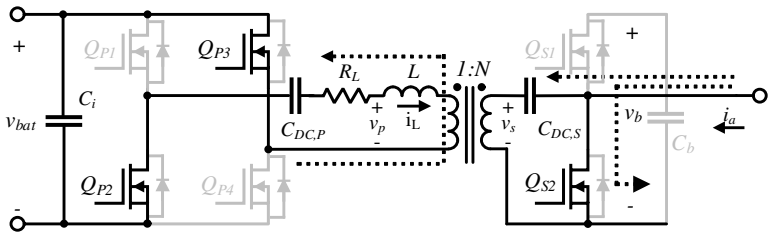


Figure 2.13: Combined converter: State VIII.

Figure 2.14 represents converter current and voltage waveforms. In PMSM control, modulations vary the duty cycles of each of the three phase inverter legs. As example, in sinusoidal and space vector pulse width modulations (SPWM and SVPWM) described in [26] the maximum duty cycle is achieved when the phase current is at its maximum value and the minimum duty cycle is when the current is minimum. This is illustrated in Figure 2.14, where the current and voltage waveforms of the main components are shown. In this picture, also are indicated the previous defined States: I-VIII. Q_{P2} waveforms are equal to Q_{P3} and Q_{P1} waveforms are equal to Q_{P4}. L_m represents the motor phase large inductance. Figure 2.14 shows 3 points: Point 1 with high duty cycle, point 2 for medium duty cycle and point 3 for low duty cycle where the current is minimal. It can be seen that primary side transistors must block the battery voltage when they are turned off and withstand the inductor current when they are turned on. It can be seen that every time, in the three points, they turn on, the current cross the zero axis. On the other hand, the secondary transistors, like conventional inverters, carry the current going to the motor i_a, but the proposed topology also adds part of the reflected current coming from the primary i_L/N, which can increase or reduce the total current flowing through them depending on the operating point. When Q_{S2} and Q_{S1} are switched off they block, as in a common inverter, the bus voltage.

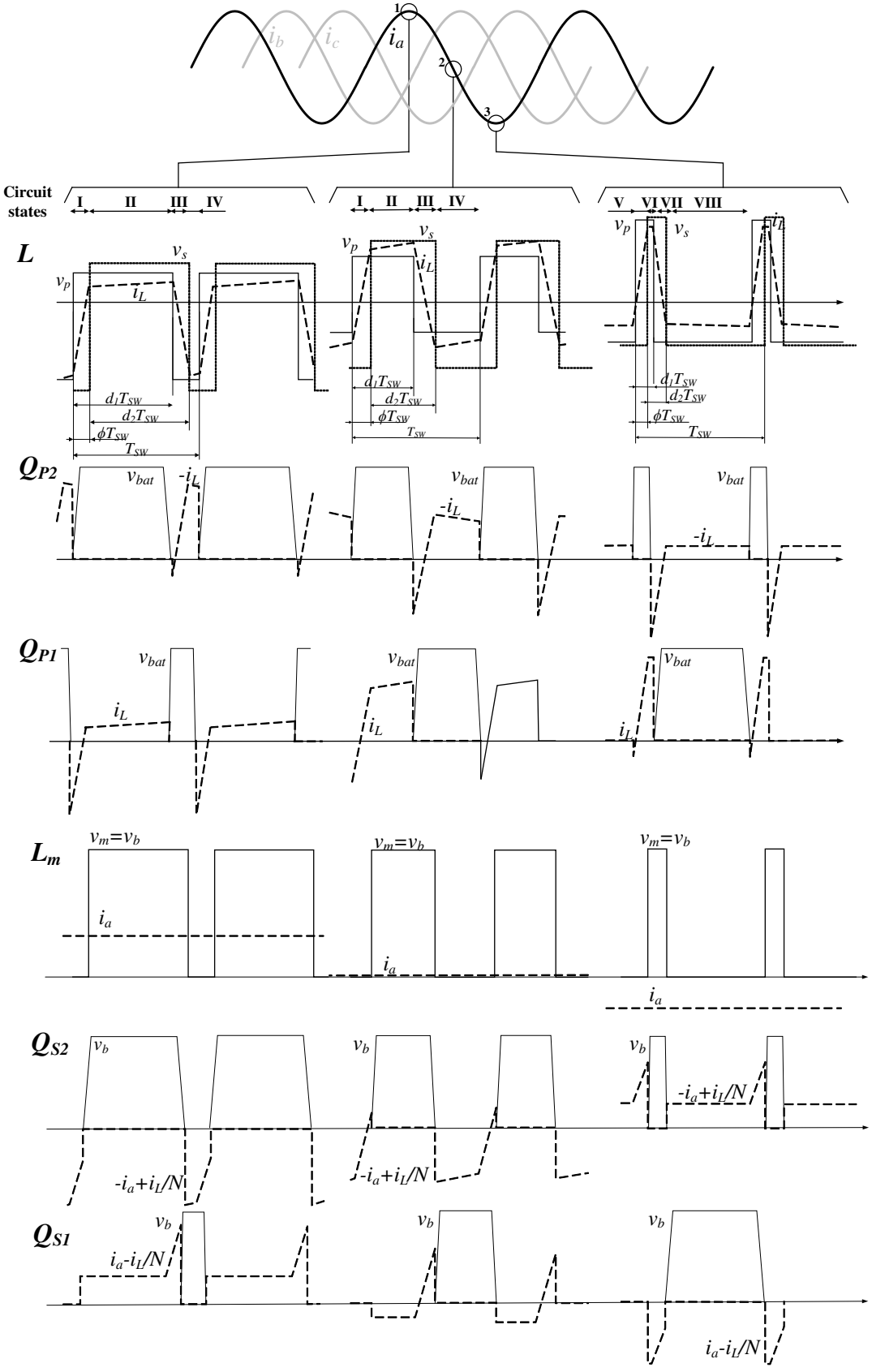


Figure 2.14: Combined converter waveforms.

2.2.1 Primary side current, i_L

In each of the four states appearing in a switching cycle, from 1 to 4 for positive phase currents, or from 5 to 10 for negative phase currents, four slopes in the i_L waveform during T_{sw} can be distinguished:

$$m_{i_L}(\tau) = \begin{cases} m_{i_L,1} & 0 < \tau \leq \phi T_{sw} \\ m_{i_L,2} & \phi T_{sw} < \tau \leq d_1 T_{sw} \\ m_{i_L,3} & d_1 T_{sw} < \tau \leq (d_2 + \phi) T_{sw} \\ m_{i_L,4} & (d_2 + \phi) T_{sw} < \tau \leq T_{sw} \end{cases} \tag{2.1}$$

where $\tau = t - nT_{sw}$. These slopes depend on the voltage difference applied to the terminals of L: $v_p - v_s/N$. First terminal voltage depends on v_p and d_1. Second terminal voltage of L depends on v_s, d_2 and N. The amplitude of v_p results $2v_{bat}$ and the maximum and minimum values depend on d_1. Similarly with v_s, where the amplitude is $v_b/2$ and the maximum and minimum values depend on d_2. It is important to note that the maximum and minimum values are determined by the duty cycle because DC blocking capacitor exists. The four slopes, assuming that ϕ is between 0 and $\min(d_1, 1 - d_2)$, and $d_1 < d_2 + \phi$ can be calculated as:

$$m_{iL,1} = \frac{d_2 v_b + (2 - 2d_1)\, N\, v_{bat}}{LN} \tag{2.2}$$

$$m_{iL,2} = \frac{(d_2 - 1)\, v_b + (2 - 2d_1)\, N\, v_{bat}}{LN} \tag{2.3}$$

$$m_{iL,3} = \frac{-(1 - d_2)\, v_b/N - 2d_1 v_{bat}}{L} \tag{2.4}$$

$$m_{iL,4} = \frac{d_2 v_b/N - 2d_1 v_{bat}}{L} \tag{2.5}$$

The instantaneous value of $i_L(t)$ can be obtained as the current at the beginning of the switching cycle $i_L(nT_{sw})$ added to the incremental term $\Delta i_L(\tau)$:

$$i_L(t) = i_L(nT_{sw}) + \Delta i_L(\tau) \tag{2.6}$$

The incremental term depends on the duration that each of the four slopes is applied:

$$\Delta i_L(\tau) = \begin{cases} \Delta i_{L,1}(\tau) & 0 < \tau \leq \phi T_{sw} \\ \Delta i_{L,2}(\tau) & \phi T_{sw} < \tau \leq d_1 T_{sw} \\ \Delta i_{L,3}(\tau) & d_1 T_{sw} < \tau \leq (d_2 + \phi) T_{sw} \\ \Delta i_{L,4}(\tau) & (d_2 + \phi) T_{sw} < \tau \leq T_{sw} \end{cases} \tag{2.7}$$

where

$$\Delta i_{L,1}(\tau) = m_{iL,1}\tau \tag{2.8}$$

$$\Delta i_{L,2}(\tau) = m_{iL,1}\phi T_{sw} + m_{iL,2}(\tau - \phi T_{sw}) \tag{2.9}$$

$$\Delta i_{L,3}(\tau) = m_{iL,1}\phi T_{sw} + m_{iL,2}(d_1 - \phi)T_{sw} + m_{iL,3}(\tau - d_1 T_{sw}) \tag{2.10}$$

$$\begin{aligned}\Delta i_{L,4}(\tau) = {} & m_{iL,1}\phi T_{sw} + m_{iL,2}(d_1 - \phi)T_{sw} + \\ & + m_{iL,3}(d_2 + \phi - d_1)T_{sw} + m_{iL,4}(\tau - (\phi + d_2)T_{sw})\end{aligned} \tag{2.11}$$

Due the blocking capacitors placed in series at primary and secondary C_{DC}, average current during one switching cycle is assumed to be zero at steady state.

In other words, to calculate $i_L(nT_{sw})$ its necessary to make the average current equal to zero along each switching period:

$$\begin{aligned}i_L(nT_{sw}) + \frac{1}{T_{sw}}\int_0^{T_{sw}} \Delta i_L(\tau)\mathrm{d}\tau = {} & i_L(nT_{sw}) + \\ & + \frac{1}{T_{sw}}\left(\int_0^{\phi T_{sw}} \Delta i_{L,1}(\tau)\mathrm{d}\tau + \int_{\phi T_{sw}}^{d_1 T_{sw}} \Delta i_{L,2}(\tau)\mathrm{d}\tau + \right. \\ & \left. + \int_{d_1 T_{sw}}^{(d_2+\phi)T_{sw}} \Delta i_{L,3}(\tau)\mathrm{d}\tau + \int_{(d_2+\phi)T_{sw}}^{T_{sw}} \Delta i_{L,4}(\tau)\mathrm{d}\tau\right) = 0\end{aligned} \tag{2.12}$$

2.2.2 Output power, P_o

Input power P_i can be calculated as the current flowing through the inductor, i_L, multiplied by the applied input voltage at the first inductor terminal v_p, in such way the absorbed energy from the battery is obtained.

$$\langle P_i \rangle_{T_{sw}} = \frac{1}{T_{sw}}\int_0^{T_{sw}} v_p(t) i_L(t)\ \mathrm{d}t = \frac{1}{T_{sw}}\left(E_1 + E_2 + E_3 + E_4\right) \tag{2.13}$$

where

$$E_1 = \int_0^{\phi T_{sw}} 2v_{bat}(1 - d_1) i_L(\tau))\ \mathrm{d}\tau \tag{2.14}$$

$$E_2 = \int_{\phi T_{sw}}^{d_1 T_{sw}} 2v_{bat}(1 - d_1) i_L(\tau)\ \mathrm{d}\tau \tag{2.15}$$

$$E_3 = \int_{d_1 T_{sw}}^{d_2 + \phi T_{sw}} -2v_{bat} d_1 i_L(\tau)\ \mathrm{d}\tau \tag{2.16}$$

$$E_4 = \int_{d_2+\phi T_{sw}}^{T_{sw}} -2v_{bat}d_1 i_L(\tau)\ \mathrm{d}\tau \tag{2.17}$$

Assuming high efficiency, it is possible to establish:

$$P_o = P_i \tag{2.18}$$

Substituting (2.13) in (2.18), it is obtained:

$$\langle P_o \rangle_{T_{sw}} = \frac{\left(\phi^2 - (2d_1d_2 + 2d_1)\,\phi - d_1{d_2}^2\right) v_{bat}v_b}{L\,f_{sw}N} + \\ + \frac{\left(\left({d_1}^2 + d_1\right) d_2 - {d_1}^2\right) v_{bat}v_b}{L\,f_{sw}N} \tag{2.19}$$

(2.19) is the general way to obtain the output power of one phase, but in this application, to simplify the control, it is assumed that $d_1 = d_2 = d$. Therefore, (2.19) can be shortened:

$$\langle P_o \rangle_{T_{sw}} = \frac{\left(-\phi^2 + (-2d^2 + 2d)\,\phi\right) v_{bat}v_b}{L\,f_{sw}N} \tag{2.20}$$

If previous equation is normalized to the maximum output power, P_{nom} can be defined as:

$$P_{nom} = \frac{P_o}{P_{o,max}} \tag{2.21}$$

Plotting (2.21), Figure 2.15 is obtained. It can be observed that maximum output power is achieved with $d = 0.5$. As long as duty cycle deviates from its central value, output power decreases. Lower ϕ values implies lower output power. If ϕ goes further than half the duty cycle, power transfer starts to decrease. Symmetrical graph is obtained when ϕ takes negative values. If ϕ is negative, power transfer direction reverses and power energy flows from the output bus to the battery. It is important to note that P_o refers to the power transferred through the transformer to the output.

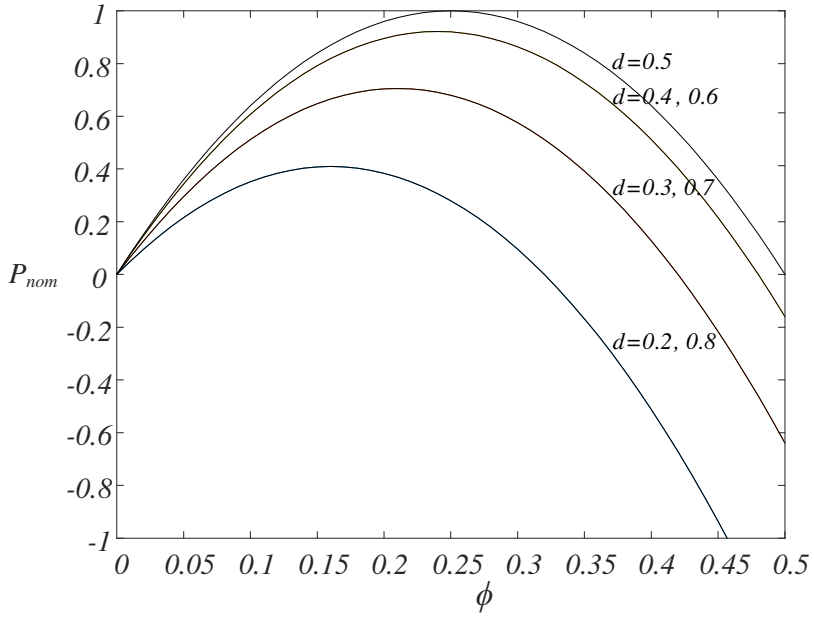


Figure 2.15: Normalized output power. Valid for $0 < \phi < min(d, 1-d)$.

2.2.3 Efficiency

This section evaluates the power losses P_{loss} to estimate the efficiency, which can be written as:

$$\eta = \frac{P_o}{P_i} = \frac{P_i - P_{loss}}{P_i} \tag{2.22}$$

The main elements that reduce the converter efficiency and are considered in this analysis are:

- Primary side switching devices.
- Secondary side switching devices.
- Series inductor.
- Transformer.
- Blocking capacitors.

2.2.4 Switching devices

The switching devices Q_{P1}, Q_{P2}, Q_{P3}, Q_{P4}, Q_{S1} and Q_{S2} contain two main sources of losses: Conduction P_{cond} and switching losses P_{sw}.

2.2.4.1 Conduction losses

Conduction losses of the primary side are only dominated by i_L. i_L flows through $Q_{p,1}$ and $Q_{p,3}$ when they are turned on, that is from $\tau = 0$ to $\tau = d_1 T_{sw}$. In case of MOSFETS, to calculate the conduction losses the RMS current is required:

$$I_{p,rms,0\_d_1} = \left(\frac{1}{T_{sw}} \int_0^{d1T_{sw}} i_L(\tau)^2 \, \mathrm{d}\tau \right)^{1/2} \tag{2.23}$$

By contrast, if IGBTs are employed the current average value must be calculated:

$$I_{p,avg,0\_d_1} = \frac{1}{T_{sw}} \int_0^{d1T_{sw}} i_L(\tau) \, \mathrm{d}\tau \tag{2.24}$$

Similary occurs to the other diagonal of the primary side switches that depends solely on i_L. The RMS current that flows through Q_{p_2} and $Q_{p,4}$, when they are conducting, from $d_1 T_{sw}$ to T_{sw} is:

$$I_{p,rms,d_1\_T} = \left(\frac{1}{T_{sw}} \int_{d1T_{sw}}^{T_{sw}} i_L(\tau)^2 \, \mathrm{d}\tau \right)^{1/2} \tag{2.25}$$

The average current can be calculated as:

$$I_{p,rms,d_1\_T} = \frac{1}{T_{sw}} \int_{d1T_{sw}}^{T_{sw}} i_L(\tau) \, \mathrm{d}\tau \tag{2.26}$$

On the other hand, the secondary transistors carry the primary current and the current to the motor. For the transistor Q_{S1} the RMS current can be calculated from ϕT_{sw} to $(d_2 + \phi)T_{sw}$ as:

$$I_{s,rms,\phi\_d_2\phi} = \frac{1}{T_{sw}} \left(\int_{\phi T_{sw}}^{(d_2+\phi)T_{sw}} (-\frac{i_L(\tau)}{N} + i_a)^2 \, \mathrm{d}\tau \right)^{1/2} \tag{2.27}$$

The average current can be estimated as:

$$I_{s,rms,\phi\_d_2\phi} = \frac{1}{T_{sw}} \int_{\phi T_{sw}}^{(d_2+\phi)T_{sw}} (-\frac{i_L(\tau)}{N} + i_a) \, \mathrm{d}\tau \tag{2.28}$$

Q_{S2} conducts from $(d_2 + \phi)T_{sw}$ till ϕT_{sw}. The RMS current for that period results:

$$I_{s,rms,d_2\phi\_\phi} = \left[\frac{1}{T_{sw}} \left(\int_{(d_2+\phi)T_{sw}}^{T_{sw}} (\frac{i_L(\tau)}{N} - i_a)^2 \, \mathrm{d}\tau + \right. \right. \\ \left. \left. + \int_0^{\phi T_{sw}} (\frac{i_L(\tau)}{N} - i_a)^2 \, \mathrm{d}\tau \right) \right]^{1/2} \tag{2.29}$$

And the average current is:

$$I_{s,avg,d_2\phi\_\phi} = \frac{1}{T_{sw}}\left(\int_{(d_2+\phi)T_{sw}}^{T_{sw}} (\frac{i_L(\tau)}{N} - i_a)\ \mathrm{d}\tau + \int_0^{\phi T_{sw}} (\frac{i_L(\tau)}{N} - i_a)\ \mathrm{d}\tau\right) \quad (2.30)$$

Finally, each MOSFET conduction losses P_{cond} can be obtained multiplying the squared RMS current by the MOSFET channel resistance $R_{ds,on}$. In case IGBTs the average current must be multiplied by the device saturation voltage $v_{ce,sat}$.

2.2.4.2 Switching losses

Due to the existence of switching at high voltages and currents at a reasonably high frequency, these losses have to be considered. Primary side transistors Q_{P1} and Q_{P2} are designed to work under ZVS conditions at switch on, but hard switching will appear at turn off. Due to that, turn on switching losses are considered negligible. Since this work is focused on MOSFETs, the estimation of turn off losses will be strongly conditioned by the MOSFET output capacitance C_{oss}.

At the end of the switch off event, the voltage across C_{oss}, $v_{sw,Coss}$ will rise till:

$$v_{sw,Coss}(t_f) = \int_0^{t_f} \frac{I_{ini}t}{C_{oss}t_f}\mathrm{d}t = \frac{I_{ini}t_f}{2C_{oss}} \quad (2.31)$$

Where I_{ini} is the current value that circulates through the semiconductor at the switch off moment and t_f is the MOSFET current falling time that can be found in the manufacturer datasheet. During switch off, the MOSFET current, $i_{SW,C_{oss}}$, goes down:

$$i_{SW,C_{oss}} = I_{ini}\left(1 - \frac{t}{t_f}\right) \quad (2.32)$$

If a linear charging/ discharging process is considered, the switching losses at turn off caused by $t_f > 0$ are:

$$P_{SW,C_{oss}}(I_{ini}) = \frac{1}{T_{sw}}\int_0^{t_f} v_{SW,C_{oss}} i_{SW,C_{oss}}\mathrm{d}t = \frac{{I_{ini}}^2 f_{sw} {t_f}^2}{24C_{oss}} \quad (2.33)$$

Since C_{oss} is voltage dependent, non linear charge equivalent capacitance $C_{oss,eq}$ during voltage transition form 0 V to v_{bat} can be used and it is defined as:

$$C_{oss,eq}(v_{bat}) = \frac{\int_0^{v_{bat}} C_{oss}(v)\ \mathrm{d}v}{v_{bat}} \quad (2.34)$$

According to (2.33), a higher value of C_{oss} will reduce the losses. As C_{oss} increases, the voltage slope falls-down, causing a decrease in the losses. On the

negative side, the higher the capacitance is, the more dead time or current I_{ini} is required to charge or discharge the capacities. In other words, more energy is needed to ensure the capacity charge/discharge. If this is not available during switching, the ZVS condition may be lost.

Q_{P1} and Q_{P4} switch off at $t = d_1 T_{sw}$:

$$P_{SW,C_{oss},1} = P_{SW,C_{oss}}(I_{ini} = i_L(d_1 T_{sw})) \tag{2.35}$$

The other transistor pair, Q_{P1} and Q_{P4}, switch off at $t = T_{sw}$:

$$P_{SW,C_{oss},2} = P_{SW,C_{oss}}(I_{ini} = i_L(T_{sw})) \tag{2.36}$$

The inverter side semiconductors Q_{S1} and Q_{S2} work in hard switching conditions. Each time one inverter branch commutes its voltage one transistor switch on while the other one switch off.

$$P_{SW,Hard}(I_{ini}) = \frac{1}{2} v_b I_{ini}(t_{ri} + t_{fv}) f_{sw} + \frac{1}{2} v_b I_{ini}(t_{rv} + t_{fi}) f_{sw} \tag{2.37}$$

Parameters t_{ri}, $t_{f,v}$, t_{rv}, t_{fi} refer to current rise time, voltage fall time, voltage rise time and current fall time respectively. Two hard switching events occurs along T_{sw}, substituting I_{ini} in equation (2.37) results:

$$P_{SW,Hard,1} = P_{SW,Hard}(I_{ini} = \frac{i_L(\phi T_{sw})}{N} - i_a) \tag{2.38}$$

$$P_{SW,Hard,2} = P_{SW,Hard}(I_{ini} = \frac{i_L((d_2 + \phi) T_{sw})}{N} - i_a) \tag{2.39}$$

2.3 Capacitors

Assuming that DC blocking capacitors $C_{DC,P1}$, $C_{DC,P2}$ and $C_{DC,S}$ The capacitor losses P_c can be calculated as:

$$P_c = R_{C_{DC,P}} I_{p,rms}^2 + R_{C_{DC,S}} I_{s,rms}^2 = R_{C_{DC,P}} I_{p,rms}^2 + R_{C_{DC,S}} \left(\frac{I_{p,rms}}{N} \right)^2 \tag{2.40}$$

where I_p can be calculated as:

$$I_{p,rms} = \left(\frac{1}{T_{sw}} \int_0^{T_{sw}} i_L(\tau)^2 \, \mathrm{d}\tau \right)^{1/2} \tag{2.41}$$

Parameters $R_{C_{DC,P}}$ and $R_{C_{DC,S}}$ can be extracted from capacitor manufacturers datasheets

2.4 Magnetics

Tight design of the magnetic components is necessary to obtain the desired power density and efficiency ratio. Equation (2.19) shows the inversely proportional relationship between the switching frequency and the inductance value required for the same output power. A higher switching frequency will require a lower inductance value and viceversa. For the same frequency / inductance ratio, it is possible to choose a high inductance volume to lower inductance losses, or a smaller inductance size which reduces efficiency but increases power density. The main losses that exist in the magnetic components are core losses and winding losses.

Regarding the core losses, the most known method is the Steinmetz model [27]. This method is based on empirical constants, which depend on the switching frequency:

$$P_{core} = k f^{\alpha} B^{\beta} \tag{2.42}$$

Constants k, α and β are obtained experimentally applying small sinusoidal signals at multiple frequencies. Since the current waveforms that flow through L are more similar to a trapezoidal shape and the waveform flowing through the magnetizing inductance of the transformer is triangular, the Improved Generalized Steinmetz Equation detailed in [28] allows to accurate predict the ferrite core loss with non-sinusoidal waveforms using Steinmetz parameters.

$$P_{core} = \frac{1}{T_{sw}} \int_0^{T_{sw}} k_1 \left| \frac{\mathrm{d}B}{\mathrm{d}t} \right| B(t)^{\beta-\alpha} \mathrm{d}t \; v \tag{2.43}$$

being

$$k_1 = \frac{k}{2\pi^{\alpha-1} \int_0^{2\pi} |\cos\theta|^{\alpha} |\sin\theta|^{\beta-\alpha} \mathrm{d}\theta} \tag{2.44}$$

B represents the magnetic flux density and v is the volume of the core. Constants k, α and β are the Steinmetz parameters which can be obtained from core material manufacturers. Flux density across L, B_L, is proportional to i_L:

$$B_L(t) = \frac{L i_L(t)}{n A_e} \tag{2.45}$$

being A_e is the effective core area and n is the inductor number of turns. The transformer flux B_T depends on the voltage applied to the magnetizing inductance $L_m ag$:

$$B_T(t) = \frac{1}{n_p A_e} \int \frac{v_b(t)}{N} \mathrm{d}t \tag{2.46}$$

being n_p the number of turns at the primary. Since the voltage applied to L_{mag} is v_s, which is a square waveform, according to (2.46), B_T becomes a triangular shape.

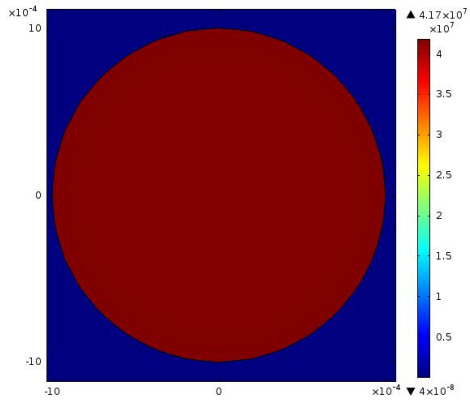
Winding losses can be separated in two types, low and high frequency losses, according to Pouillet law [29], low frequency losses can be modeled by the resistance R_{dc}:

$$R_{dc} = \rho \frac{N_w M}{\left(\frac{d_s}{2}\right)^2 \pi n_s} \tag{2.47}$$

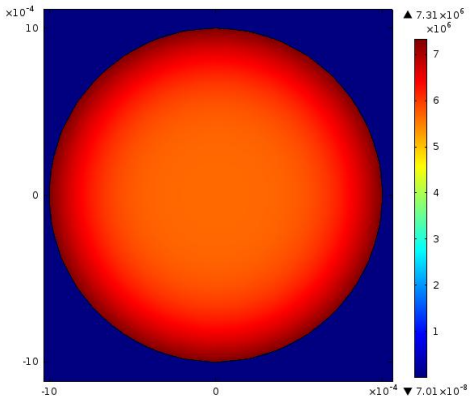
where M is the mean coil length of a turn around the used core. Resistance R_{ac} is used to characterize the high frequency losses caused in the windings. Two main effects occur, the skin effect and the proximity effect. In the skin effect, the current flowing through the conductor induces eddy currents in the wire itself. This results in a decrease in the current flowing through the center of the conductor. As a result, the current is distributed on the outside, decreasing the effective area of the conductor. The effect is emphasised with increasing frequency. In [30] the penetration depth δ is described as:

$$\delta = \sqrt{\frac{\rho}{\pi f_{sw} \mu_0}} \tag{2.48}$$

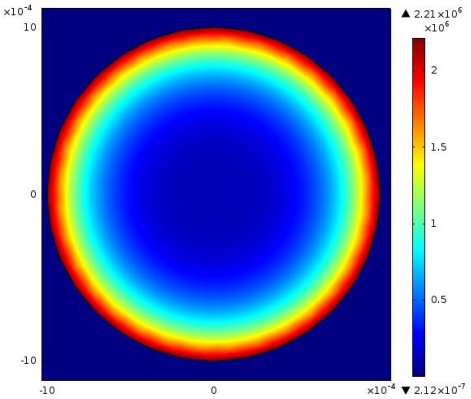
This parameter indicates the depth measured from the surface of the conductor through which current flows. Figure 2.16 shows how the increase in frequency causes a decrease in the penetration depth for a conductor with diameter d.



(a) $f = 0.1$kHz.



(b) $f = 1$kHz.



(c) $f = 10$kHz.

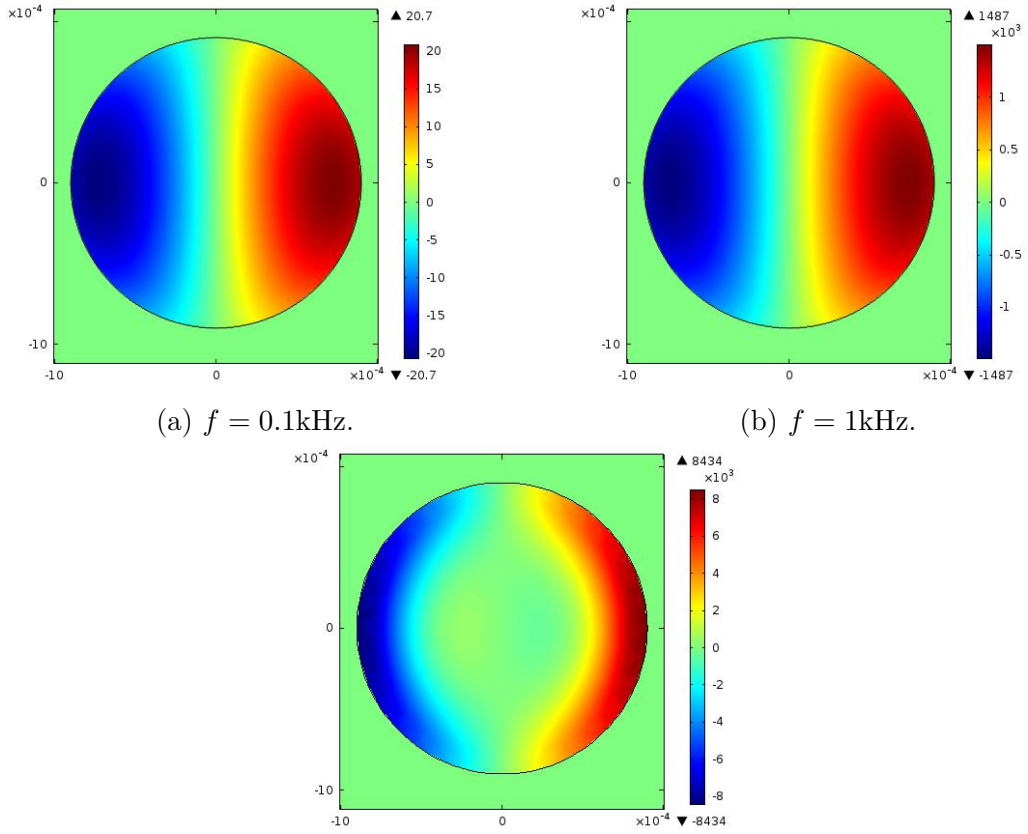
Figure 2.16: Skin effect: $J\left[\frac{\mathrm{A}}{\mathrm{M}}\right] \rightarrow d = 1$mm.

For this reason, in order to ensure that the entire cable conducts current, it is recommended to use conductors that satisfy at least:

$$d < 2\delta \tag{2.49}$$

Consequently, at high frequencies where d has to be small and a large cable cross-section is required, it is necessary to use multi-stranded conductors.

The proximity effect, like the skin effect, is caused by high-frequency alternating current. In this effect, unlike the previous one, Eddy currents are induced by other conductors instead of being the conductor itself the generator of these currents. The existence of an external field from a nearby conductor acts as a source of energy that is dissipated in the cable. It induces a current whose net value is zero, but generates losses. Figure 2.17 illustrates the increase of this phenomenon due to the rise of the excitation frequency of the external field.



(a) $f = 0.1$kHz. (b) $f = 1$kHz.

(c) $f = 10$kHz.

Figure 2.17: Proximity effect: $J\left[\frac{\text{A}}{\text{M}}\right] \rightarrow d = 1$mm.

In [31], an analytical expression of R_{ac} based on Dowell's method that considers skin and proximity effects is presented:

$$R_{ac} = R_{dc}\left(1 + \frac{(\pi n_s N_w)^2 d_s^6}{192\delta^4 b^2}\right) \tag{2.50}$$

being b the windings window height, n_s the strands number and N_w the winding turns number. Constant μ_0 is the free space permeability and constant ρ is the conductor resistivity.

Finally, winding losses can be obtained as:

$$P_{winding,h} = I_{L,rms,h}^2 R_{ac,h} \tag{2.51}$$

Sub-index h makes reference to the harmonic. If the current signal contains several relevant high order harmonics, they must be taken into account. Also, if several windings appear on the same magnetic component, as in a transformer, losses in

each winding needs to be included. Both magnetic components, L and transformer, must be considered in the magnetic losses:

$$P_{mag} = P_{core,L} + P_{windings,L} + P_{core,T} + P_{windings,T} \tag{2.52}$$

2.5 Zero voltage switching

Primary side semiconductors must operate under ZVS condition to avoid extra losses and EMI issues. In order to guarantee that condition, switches must be turned on during anti-parallel diodes conduction time. Moreover, external MOSFETs parallel capacities C_{oss} must be charge-discharged before current changes direction. As described in [32], to achieve ZVS in primary side full-bridge, stored energy in inductor L must be large enough to discharge / charge the four parallel capacities $C_{oss,eq}$. Figure 2.18 shows the three ZVS transition steps for the primary side bridge.

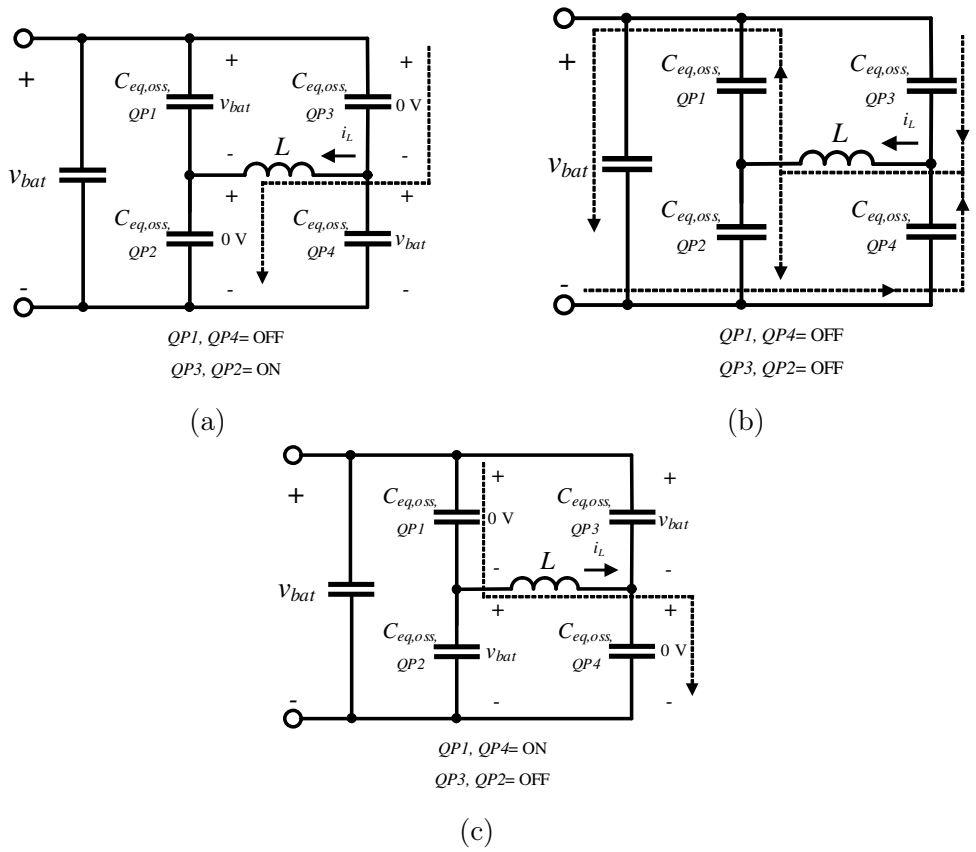


Figure 2.18: Parallel output MOSFET equivalent capacitance charge during ZVS transition event. (2.18a) before transition occurs. (2.18b) during ZVS transition. (2.18c) ZVS transition is completed.

Figure 2.18a shows the first state, in the instant when switching event starts. Current flows through MOSFETs Q_{P2} and Q_{P3} maintaining its external capacities discharged. Stored energy is at the inductor L and at the capacities of the two

turned off MOSFETs, $C_{oss,eq,QP1}$ and $C_{oss,eq,QP4}$ which are charged at v_{bat}. Initial instant transition energy, just before all transistors are switched off, can be written as:

$$E_{initial} = \frac{1}{2}Li_{L,sw}^2 + \frac{1}{2}(C_{oss,eq,QP1} + C_{oss,eq,QP4})v_{bat}^2 \tag{2.53}$$

where $i_{L,sw}$ represents the current through L and conducting MOSFETs at the switching instant. When all transistors are turned off during dead time t_{dead}, situation depicted in Figure 2.18b arises. MOSFETs are turned off and i_L starts to flow through Q_{P1} and Q_{P3} intrinsic body diodes discharging $C_{oss,eq,QP1}$ and $C_{oss,eq,QP4}$. At same time, $C_{oss,eq,QP2}$ and $C_{oss,eq,QP3}$ are being charged till they reach v_{bat}. During this process, $C_{oss,eq,QP1}$ and $C_{oss,eq,QP4}$ stored energy is transferred to the source or load.

$$E_{delivered} = \frac{1}{2}(C_{oss,eq,QP1} + C_{oss,eq,QP2} + C_{oss,eq,QP3} + C_{oss,eq,QP4})v_{bat}^2 \tag{2.54}$$

Transition is completed when Q_{P1} and Q_{P3} are activated, as shown in Figure 2.18c. If ZVS transition is successfully completed, Q_{P1} and Q_{P3} parallel capacitances are discharged when respective MOSFETs gates are activated. In order to ensure ZVS, MOSFETs must be turned on before current cross zero, so final energy is:

$$E_{final} = \frac{1}{2}(C_{oss,eq,QP2} + C_{oss,eq,QP3})v_{bat}^2 \tag{2.55}$$

Given previous states ZVS boundary condition results:

$$E_{initial} > E_{delivered} + E_{final} \tag{2.56}$$

Substituting equations (2.53),(2.54) and (2.55) into equation (2.56), assuming are MOSFETs capacities are equal and solving for $i_{L,sw}$ results:

$$|i_{L,sw}| > \sqrt{\frac{4C_{oss,eq}v_{bat}^2}{L}} \tag{2.57}$$

As it can be seen in Figure 2.19, two switching events exists during T_{sw} at primary side. The switching event must be completed while the diodes conducts, that is during $t_{a,1}$ and $t_{a,2}$.

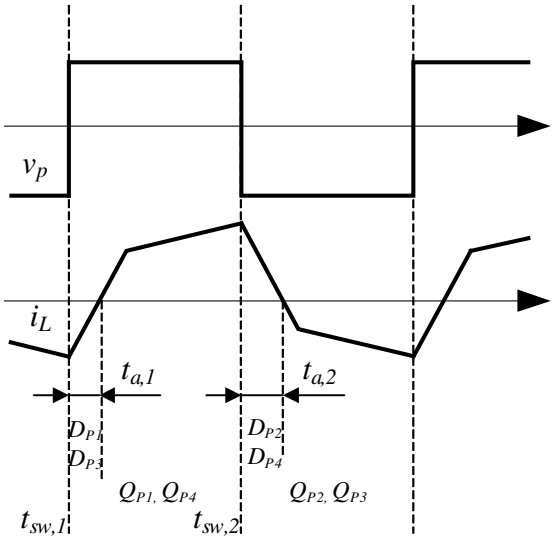


Figure 2.19: ZVS switching instants for primary side devices and ZVS available time.

According to the current sign of i_L in Figure 2.19 and the condition of (2.57), the two ZVS limits can be obtained:

$$i_{L,sw1} = i_L(\tau = 0) < -\sqrt{\frac{4C_{oss,eq}v_{bat}^2}{L}} \tag{2.58}$$

$$i_{L,sw2} = i_L(\tau = d_1 Tsw) > \sqrt{\frac{4C_{oss,eq}v_{bat}^2}{L}} \tag{2.59}$$

Rewriting previous equations in terms of ϕ the ZVS conditions for the two diagonals of the full bridge are obtained:

$$\phi > -\frac{\sqrt{L}\,\left(\left(d^2-d\right)v_b + \left(2d-2d^2\right)N\,v_{bat}\right) - 4\sqrt{C_{oss,eq}}L\,f_{sw}N\,v_{bat}}{2d\sqrt{L}\,v_b} \tag{2.60}$$

$$\phi > \frac{\sqrt{L}\,\left(\left(d^2-d\right)v_b + \left(2d-2d^2\right)N\,v_{bat}\right) - 4\sqrt{C_{oss,eq}}L\,f_{sw}N\,v_{bat}}{\left(4d-4\right)\sqrt{L}N\,v_{bat}} \tag{2.61}$$

C_{oss} value must be considered when selecting primary side semiconductors. Higher C_{oss} values reduces turn off losses but requires more discharging/ charging time to achieve ZVS. Primary side semiconductors switching instants are shown in Figure 2.19. When first instant named as $t_{sw,1}$ occurs, Q_{P2} and Q_{P3} are turned off and body diodes from Q_{P1} and Q_{P4} start to conduct. Transistors must be switched on when anti-parallel diodes are conducting, which means before current crosses zero, so equations (2.58) and (2.59) must be satisfied. This available time to turn

on transistors is defined in Figure 2.19 as $t_{a,1}$. That implies that required dead time t_d must be less than $t_{a,1}$ Equivalent situation occurs for $t_{sw,2}$. In addition, condition described in equation (2.57), where $i_{L,sw}$ needs to be large enough to discharge capacities, must be satisfied. Minimum required ideal dead time with no stray capacitance considered can be obtained:

$$t_{dead} > \frac{4C_{oss,eq}v_{bat}}{i_{L,sw}} \tag{2.62}$$

The inverter or secondary side semiconductors Q_{S1} and Q_{S2} are designed to work under hard switching events, so there is no ZVS boundary requirement.

2.6 Design procedure

2.6.1 Introduction

The chassis dynamo-meter driving schedules and shift schedules used by the Environmental Protection Agency (EPA) for vehicle emissions and fuel economy testing can be found in [33]. To meet efficiently the EPA's driving schedules a design methodology is presented in this section. Three different drive schedules are defined by EPA: Urban Dynamometer Drive Schedule (UDDS) and New York City Cycle (NYCC), shown in Figure 2.20, that features low speed stop-and-go traffic environment, the Highway Fuel Economy Test (HWFET), shown in Figure 2.21, represents highway driving conditions and the US06 cycle, shown in Figure 2.22, based on high acceleration aggressive driving schedule that is often identified as the "Supplemental FTP" driving schedule.

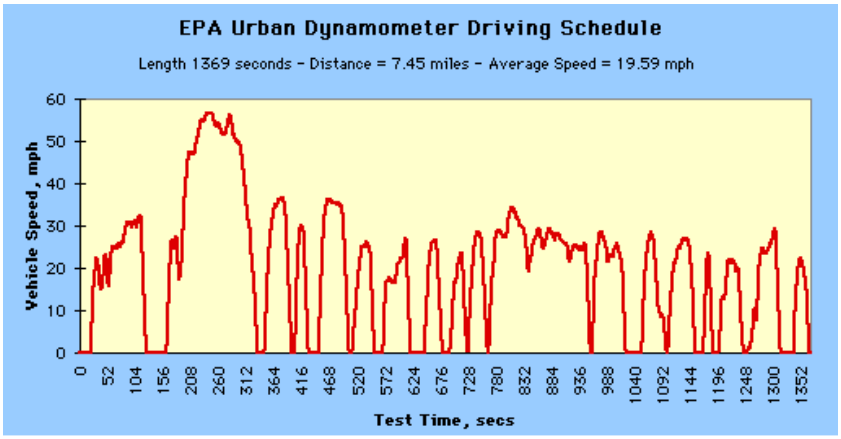


Figure 2.20: Dynamometer Drive Schedules: UDDS.

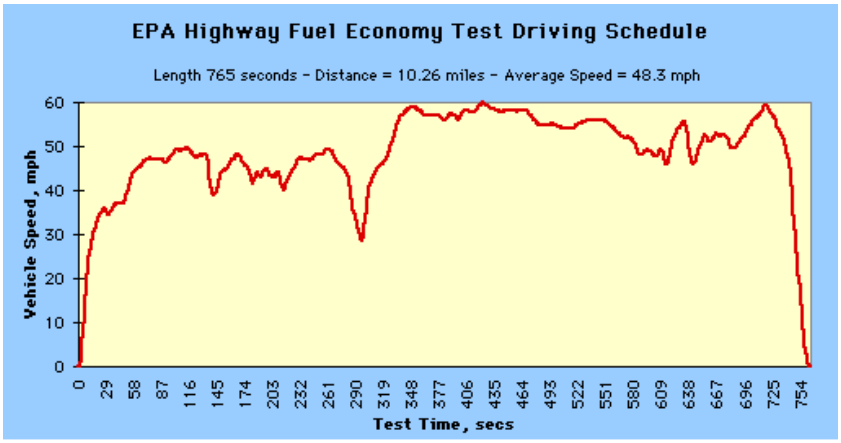


Figure 2.21: Dynamometer Drive Schedules: HWFET.

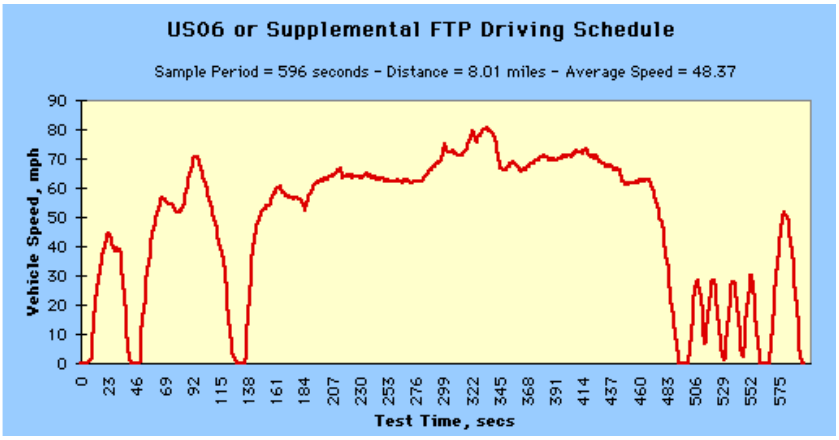


Figure 2.22: Dynamometer Drive Schedules: US06.

According to [34], the urban cycle is characterized by low speeds. So low ω_s, which implies the use of low dc bus voltages. Although moderated torque may be required, since the speed is relatively small, low power must be provided by the inverter. The highway driving style is distinguished by high motor speeds and normal torque due to the constant speed. This is translated into a high bus voltage and medium power. The aggressive driving style is known for its abrupt accelerations, including at high speeds. These accelerations at high or moderate speeds can also occur in situations of overtaking or merging onto a highway. In order to meet these situations the inverter has to deliver its peak power at high voltages. Summarizing, maximum output power occurs at higher bus voltages and low output power exists at lower bus voltages.

2.6.2 Operating modes

To meet all the voltage range efficiently, the full-bridge configuration shown in Figure 2.3 can be implemented for high output voltages and switch to half-bridge configuration when low output voltages are required. As shown in Figure 2.4, toggling between full-bridge and half-bridge configurations with the same hardware can be done by maintaining enabled Q_{P4} and Q_{P3} disabled. As named previously at the beginning of this section, the maximum converter efficiency is achieved when it operates close to its nominal voltage gain provided by the transformer turns ratio N for half-bridge or $2N$ for full-bridge. Half-bridge and full-bridge operation modes are defined in Figure 2.23 and converter may switch into one mode or the other depending on the desired bus voltage and the existing battery voltage. As it is illustrated, for high bus voltages full bridge mode is preferred while for low bus voltages the half bridge mode is selected.

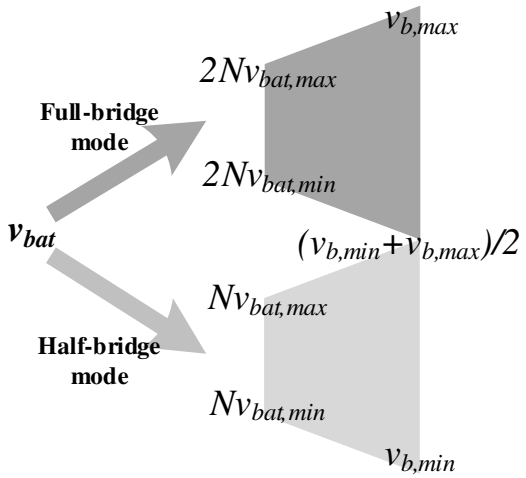


Figure 2.23: Operation modes.

The transitions between bridge and half-bridge mode can give rise to small over-currents in the primary side. In a vehicle, these transitions with the vehicle running would occur very rarely, since it rely mainly on the state of the battery and the driving behavior depending on the type of road. The soft transition switching pattern shown in Figure 2.24 can be implemented.

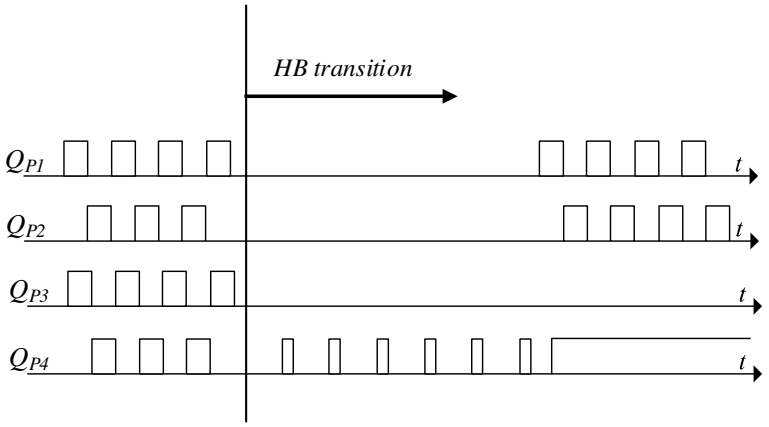


Figure 2.24: Transition pattern from full bridge to half bridge.

When the command to convert from FB to HB is received, the primary transistors stop switching. Transistor Q4 continues to switch with small pulses that allow the series capacitor to charge in a controlled manner to the new blocking voltage avoiding current spikes. After a series of pulses on Q4, it remains permanently activated. Is important to underline that this type of transitions, which are not the objective of this thesis, have been studied in previous works such as, [35], to make them smoothly and avoid oscillations.

2.6.3 Procedure

Proposed design procedure is collected by Figure 2.25. To cover the range defined Figure 2.23 in an efficient way, the converter natural gain N must be placed in the middle of the isosceles trapezoid and can be calculated as:

$$N = \frac{(v_{b,min} + v_{b,max})/2 + v_{b,min}}{v_{bat,min} + v_{bat,max}} \tag{2.63}$$

Once N is obtained, if the step up and down stage is to be added to an existing or independently designed inverter, the same switching frequency selected for the inverter-motor unit must be used. The inverter can operate with a modulation index from 0 to 1, which may involve extremal duty cycles. As shown in Figure 2.15, instantaneous minimum output power by the step and down part is delivered at d_{min} or d_{max} duty cycles values. This means that when one phase of the inverter is operating at duty cycles lower or higher than d_{min} or d_{max} respectively, the step up and down stage of that phase will not be able to deliver the instantaneous power needed to maintain the bus voltage. When this occurs, the other two phases operate around d=0.5 and can supply the power needed, allowing the use of a small value capacitor. As a design criteria, d_{min} and d_{max} define the range of duty

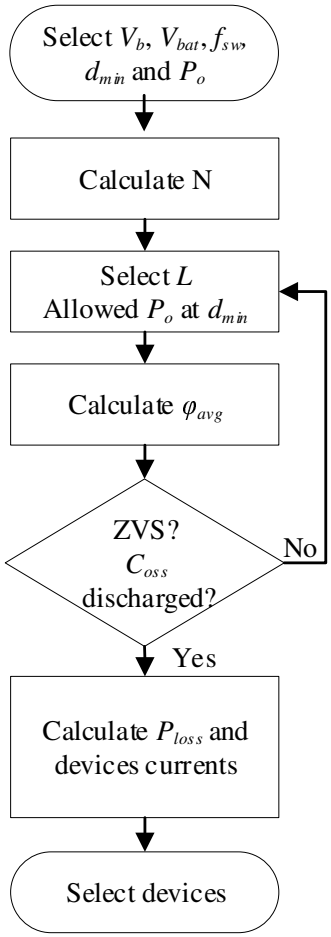


Figure 2.25: Design procedure diagram.

cycles where a maximum power can be supplied by one individual phase. It is important to remark that for values closer to d=0.5, the stage would instantly be able to deliver more instantaneous power than nominal power and maintain v_b. Selecting maximum and minimum cycles close to 0.5 (i.e., d_{max}=0.6, d_{min} =0.4) will increase v_b ripple, while very extreme values will increase losses (i.e., d_{max} =0.9, d_{min} =0.1). It is therefore recommended to use an intermediate term: d_{max}=0.8, d_{min}=0.2. Variables d_{max}, d_{min} are used to adjust the value of L, not to limit the inverter duty cycle. Consequently, inductance L must be selected to provide required maximum power at critical condition: minimum duty cycle and minimum battery level. It can be calculated rewriting equation (2.20) and substituting ϕ by

$d_{min}(1-d_{min})$, where according to (2.20), the maximum output power is given:

$$L = \frac{\left(d_{min}^4 - 2d_{min}^3 + d_{min}^2\right) v_{bat,min} v_{b,min}}{\langle P_o \rangle_{T_{sw}} f_{sw} N} \tag{2.64}$$

The DC blocking capacitors $C_{DC,P}$ and $C_{DC,S}$, as in typical DC-DC converters, should be chosen appropriately so they are not too small to cause a large voltage drop across the voltage square waveforms, v_p and v_s, under steady-state operating condition and not to large to avoid affecting transient behavior. For full-bridge implementation, the minimum value of $C_{DC,P}$ and $C_{DC,S}$ can be obtained by:

$$C_{DC,P} = \frac{P_o d_{max}}{v_{bat,min} f_{sw} v_{drop}} \tag{2.65}$$

$$C_{DC,S} = \frac{P_o d_{max}}{v_{bat,min} f_{sw} v_{drop} N} \tag{2.66}$$

where v_{drop} represents the allowed voltage drop of the square waveforms. It is recommended to be between 5 and 10% of v_{bat} or v_b. In case half-bridge is implemented, obtained capacitors values using (2.65) and (2.66) must be multiplied by 2.

Averaged phase angle, which is the control signal, during one motor sinusoidal current cycle $\langle \phi \rangle_{T_m}$ must be calculated to obtain, in simply and relatively accurate way, the averaged losses. $\langle \phi \rangle_{T_m}$ is obtained from equation (2.20):

$$\langle \phi \rangle_{T_m} = \left(d_{avg} - {d_{avg}}^2\right) + \\ + \frac{\sqrt{\left({d_{avg}}^4 - 2{d_{avg}}^3 + {d_{avg}}^2\right) v_{bat} v_b - L \langle P_o \rangle_{T_{sw}} f_{sw} N}}{\sqrt{v_{bat}} \sqrt{v_b}} \tag{2.67}$$

where d_{avg} is the average duty cycle value over a quarter of a motor phase current sinusoidal cycle. Then, P_{loss} and currents are calculated substituting d_{avg} and $\langle \phi \rangle_{T_m}$ in equations given in subsection 2.2.3. ZVS conditions in equations (2.58) and (2.59) must be checked. If they are not satisfied, lower L value should be selected or $\langle P_o \rangle_{T_{sw}}$ must be limited when duty cycle is at extreme values. Given that situation, at least one stage per inverter branch is required. When one phase is at extreme duty cycle, another phase will be close to $d = 0.5$ and will be able to provide more power and compensate the phase which provides less power. Another way to increment delivered power and maintain ZVS is slightly reduce f_{sw} for a fixed L. If motor control allows, several procedure iterations varying f_{sw} can be done, which permits an optimization between power density and losses. This can be done using the diagram of Figure 2.26. It is similar to the previous procedure but with an additional loop that goes forward an array with different f_{sw} values.

If a Pareto diagram to find an optimum power density, the volume model of the passive components and heat-sink should be included.

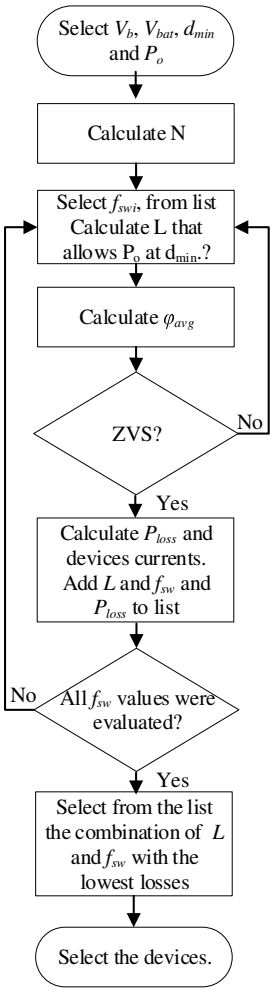


Figure 2.26: Design procedure diagram with f_{sw} optimization.

2.6.4 Simulation and experimental results

Considering typical automotive industry voltage levels and following the proposed design methodology, the converter parameters listed in Table 2.1 are obtained.

Table 2.1: System design parameters.

Parameter	**Value**
Battery voltage range, V_{bat}	290-420 V
Motor bus voltage range, V_b	200-800 V
Maximum phase output power, $P_{o,max}$	3.3 kW
Turns ratio, N	1
Inductor, L	59 μH
Blocking capacitors, $C_{DC,P}$ and $C_{DC,S}$	10 μF
Switching frequency, f_{sw}	50 kHz

Each of the three phases has one converter which is designed to withstand 3.3 kW, making possible to supply a motor of 10 kW. To evaluate the feasibility of the proposal and the performance of the whole system, different tests of the designed converter supplying a 10 kW PMSM are done by simulation using MATLAB-Simulink. Focusing on the behavior of a single phase operating at 3.3 kW, Figure 2.27 shows the simulation results of different situations or critical points that the designed converter must deal with during a switching cycle. Figure 2.27b shows the waveforms of the converter when the bus voltage is boosted to its maximum, 800 V, with the minimum duty condition. Figure 2.27c demonstrates that 800 V can be also obtained with the maximum duty cycle.

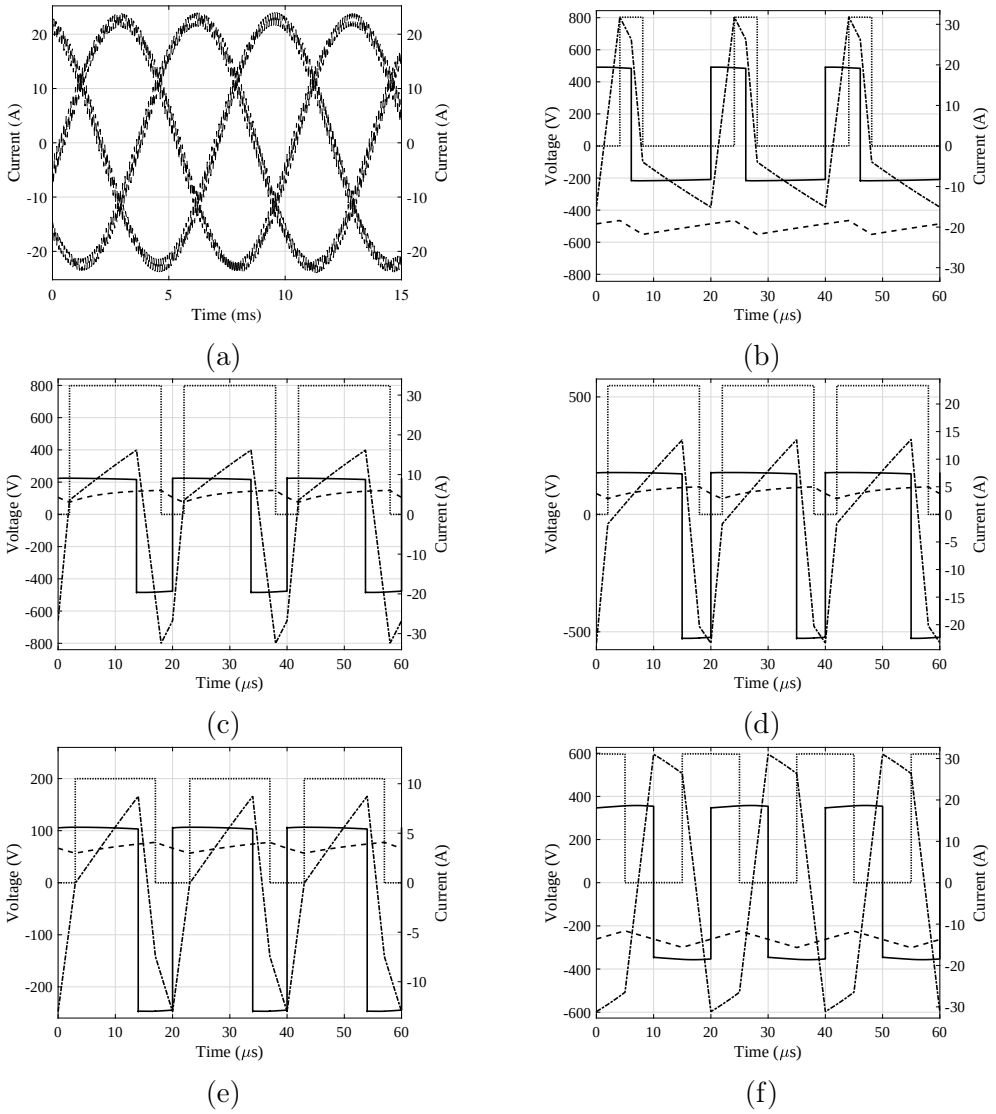


Figure 2.27: Proposed design simulations results operating at 3.3 kW per phase in different conditions. Solid trace v_p, dotted trace v_m, dash-dot trace i_p and dash trace i_a. (a) Phase currents: i_a, i_b and i_c. (b) d_2=0.2, v_b=800 v_{bat}=350 V. (c) d_2=0.8, v_b=800 v_{bat}=350 V. (d) d_2=0.8, v_b=550 v_{bat}=350 V. (e) Half-bridge operation: d_2=0.8, v_b=200 v_{bat}=350 V.(d) Reverse operation: d_2=0.5, v_b=600 v_{bat}=350 V.

According with the operation modes described in Figure 2.23; when the converter works in full-bridge mode, the minimum bus voltage before changing to half-bridge mode must be guaranteed. This bus voltage is 550 V and the converter operation is depicted by Figure 2.27d. Figure 2.27e shows the feasibility to reach

the minimum bus voltage, 200 V with a high battery voltage level thanks to the half-bridge mode. In all cases, ZVS is accomplished in the primary side at turn on, since (2.58) and (2.59) are satisfied, ensuring the MOSFET body diode conducts before the channel activation. Regenerative braking or reverse operation is illustrated in Figure 2.27f. It can be distinguished from normal application because phase ϕ is negative. ZVS situation is now achieved at the secondary side. Additionally, in Figure 2.27a, the three phase converters are operated simultaneously at 3.3 kW each during multiple switching cycles generating the motor phases currents.

From the motor control point of view, the proposed converter acts as a typical inverter. It is able to generate the slow phase currents varying the duty cycle. The operation of the PMSM with the properties contained in Table 2.2 is simulated.

Table 2.2: PMSM specifications.

Parameter	**Value**
Pole pairs	4
Rated torque, $T_{m,nom}$	50 Nm
Rated speed, $w_{m,nom}$	200 rad/s
Rated power, $P_{m,nom}$	10 kW
Armature inductance, L_m	3 mH
Stator resistance, R_m	1.5 Ω
Torque constant, K_T	1.8 Nm/A

Figure 2.28a depicts the simulation results of the start-up transient of the motor with a speed reference of 200 rad/s. At the beginning, the motor currents increase until the reference is reached. Then, a perturbation is introduced at 0.015 s, the mechanical torque grows from 37.5 Nm to the rated value, 50 Nm. Thus, the speed control increments the amplitude values of the phase currents to maintain the speed reference. Figure 2.28b shows the phase currents flowing through the motor and the converter under the maximum bus voltage gain: $v_{b,max}$ and $v_{bat,min}$. In the opposite way, Figure 2.28c shows the motor phase currents with the maximum bus voltage reduction: $v_{b,min}$ and $v_{bat,max}$.

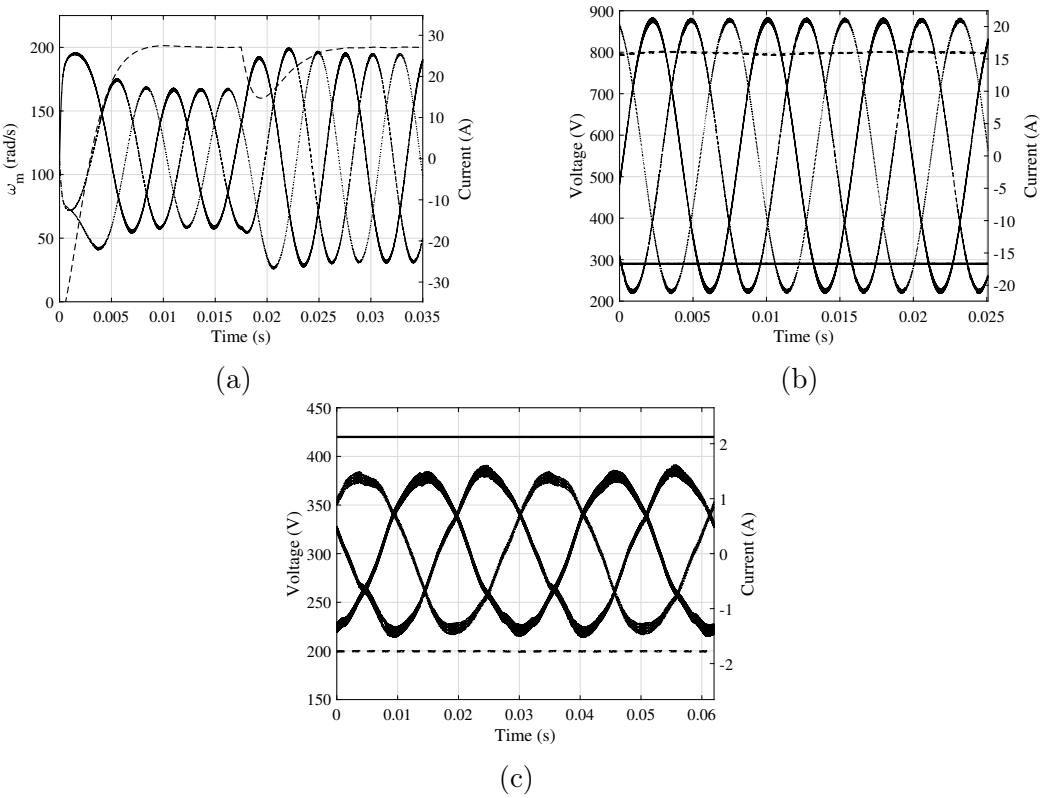


Figure 2.28: Inverter stage simulations. Solid lines: Phase motor currents: i_a, i_b and i_c (a) $w_{m,ref} = 200$ rad/s. At 0.015 s, T_m is increased by 25%. Dashed line: ω_m. (b) Minimum battery voltage to provide maximum output voltage: $v_{bat} = 290$ V, $v_b = 800$ V. (c) Maximum battery voltage to provide minimum output voltage: $v_{bat} = 420$ V, $v_b = 200$ V.

Two experimental prototypes have been built. The aim of the first one is to validate the feasibility of the converter itself: high-voltage operation and step up and down DC voltage capabilities while the secondary side transistors are also able to generate a DC square waveform with a peak voltage value of v_b and a constant output current i_a, like a common inverter. To do that, one phase of the converter using the parameters of Table I is connected to an inductive load, L_a, of 700 μH. The schematic and hardware implementation of the experimental set are represented in Figure 2.29.

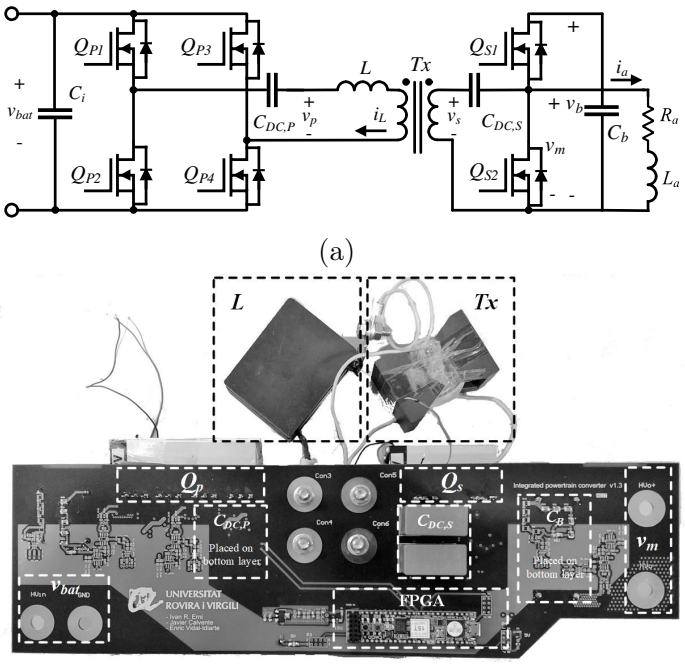


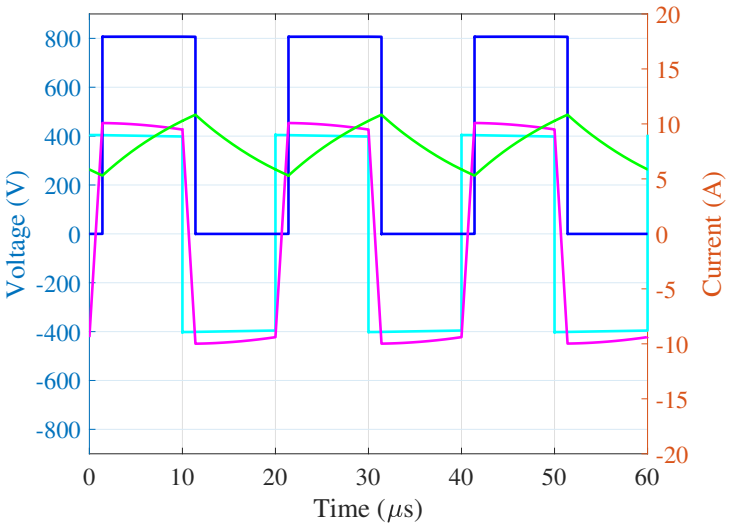
Figure 2.29: 3.3 kW experimental set. (a) Proposed solution schematic. (b) Experimental.

Converter prototype was implemented according to the design procedure in previous section with the parameters described in Table 2.1. Selected semiconductors characteristics are collected by Table 2.3. Selected semiconductors are STW70N60DM2 for primary side and C3M0065100K for secondary side. It is important to remark that primary side switches operate under ZVS turn-on condition, so higher C_{oss} decreases turn-off losses but also increases required deadtime to discharge/ charge external MOSFET capacities. In contrast, secondary side switches operate under hard-switching condition at high voltages, thus fast switching semiconductors are needed.

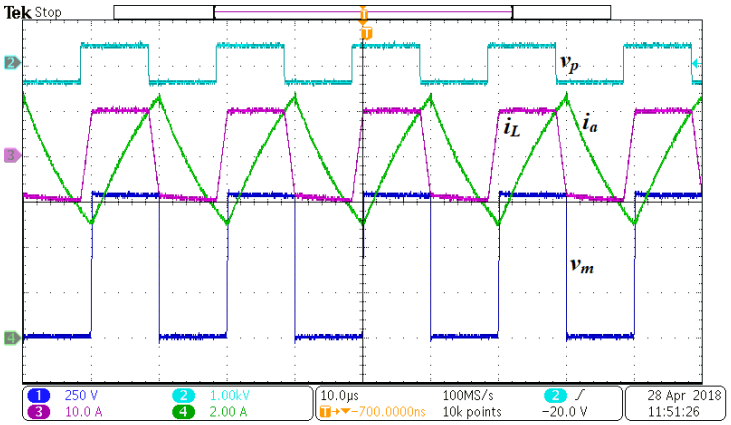
Table 2.3: Prototype semiconductors characteristics summary.

Device	**Characteristic**	**Value**
Q_P	Drain-source breakdown voltage	600 V
STW70N60DM2	Static drain-source on resistance	0.037 Ω
	Output capacitance	241 pF
Q_S	Drain-source breakdown voltage	1000 V
C3M0065100K	Static drain-source on resistance	0.065 Ω
	Output capacitance	60 pF

Digital PI control strategy using a FPGA was implemented. Bus voltage v_b is measured and compared with desired bus voltage v_{ref}. The control signal ϕ is used to regulate v_b. Figure 2.30 shows main waveforms at $P_o = 3.3$ kW. Input battery voltage v_{bat} is placed at 400 V and bus voltage v_b is set at 800 V. It can be demonstrated that output motor phase current is decoupled from the primary side current i_L and that high voltage elevation ratio is achieved. Measured efficiency of the system, including boost and inverter, is higher than 97 %.



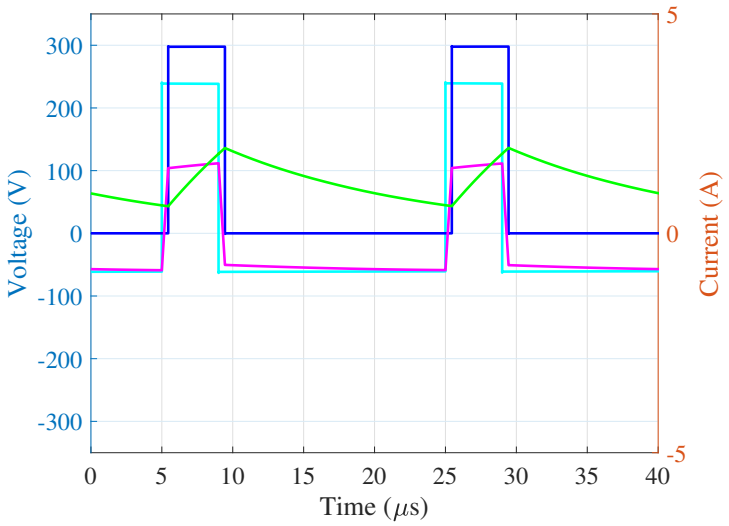
(a)



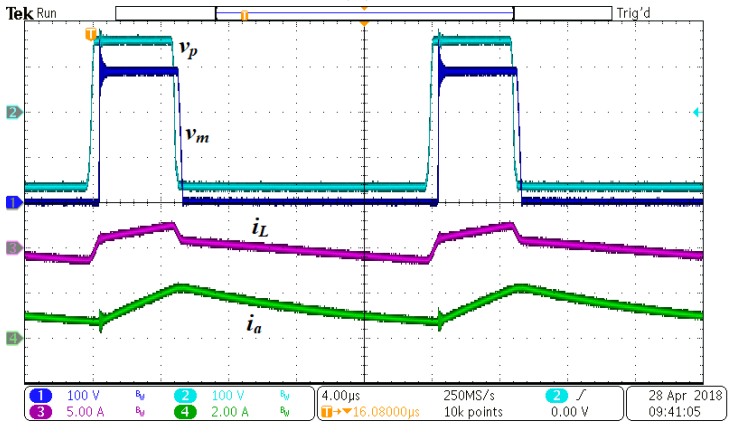
(b)

Figure 2.30: Measured converter main waveforms supplying 3.3 kW to the load, d=0.5, v_{bat}=400 V, v_b=800 V. Primary side voltage v_p (1 kV/div), inductor current i_L (10 A/div), inverter output voltage v_m (250 V/div), current flowing to the inductive load i_a (5 A/div). (a) Simulated. (b) Experimental.

Figure 2.31 corroborates that ZVS condition is maintained in the step up and down part for critical operating points: low load, low battery and extreme duty cycle values.



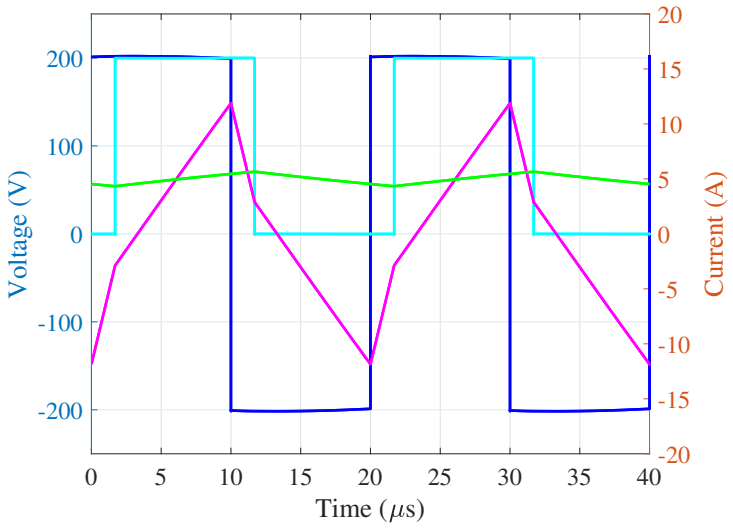
(a)



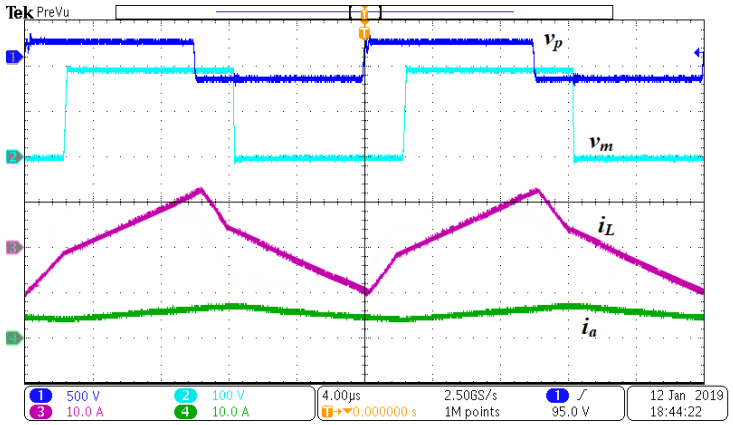
(b)

Figure 2.31: Measured converter main waveforms supplying 300 W to the load, d=0.2, v_{bat}=150 V, v_b=300 V. Primary side voltage v_p (100 V/div), inverter output voltage v_m (100 V/div), inductor current i_L (5 A/div), current flowing to the inductive load i_a (2 A/div). (a) Simulated. (b) Experimental.

Figure 2.32 shows the converter operating in half-bridge mode. An input battery of 400 V steps down to 200 V at the converter output. The half-bridge configuration is used, so the nominal converter gain changes from $2Nv_{bat}$ to Nv_{bat}.



(a)



(b)

Figure 2.32: Measured converter main waveforms supplying 1000 W to the load, d=0.5, v_{bat}= 400 V, v_b =200 V. From top to bottom: Primary side voltage v_p (500 V/div), inverter output voltage v_m (100 V/div), inductor current i_L (10 A/div), current flowing to the inductive load i_a (10 A/div). (a) Simulated. (b) Experimental.

Efficiency measurements are done using Yokogawa WT3000 power analyzer. Measured and calculated efficiency values are plotted in Figure 2.33, where a peak efficiency of 97.6% is achieved at nominal output power and v_{bat}=350 V.

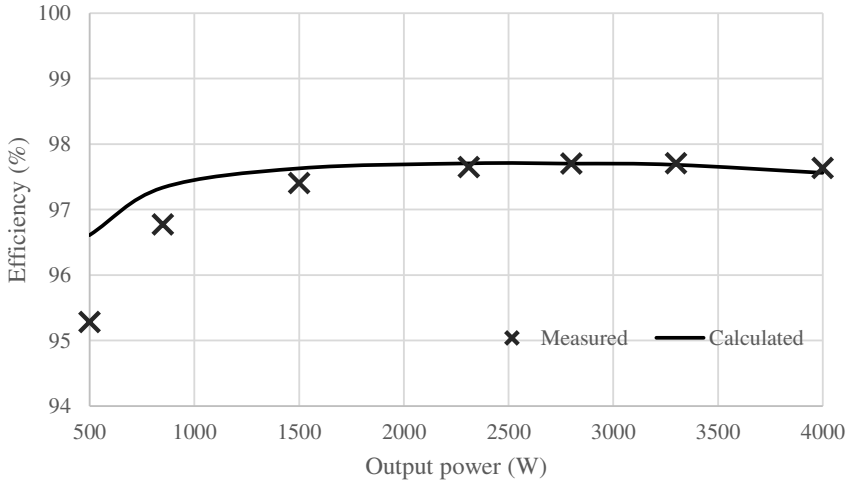


Figure 2.33: Calculated versus measured efficiency results of the proposed converter.

The estimated distribution losses in this operating point are represented in Figure 2.34.

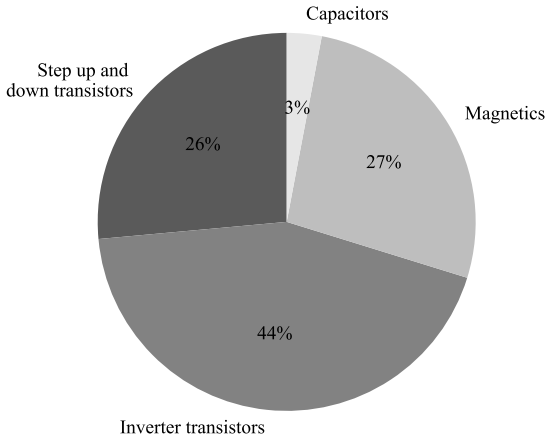


Figure 2.34: Estimated distribution losses.

The prototype of Figure 2.29 is reconfigured to be equivalent to a phase of Figure 1.1, obtaining the schematic of Figure 2.35. In this way, the same semiconductors and the same volume are used. It is important to note that the transformer

disappears, but the inductor required by the boost stage is of much higher value, 280 μH, so the size of the resulting magnetic components is similar. In the boost topology of the conventional solution, several transistors are usually placed in parallel in order to handle the current levels. Therefore, the system is implemented with 2 transistors in parallel.

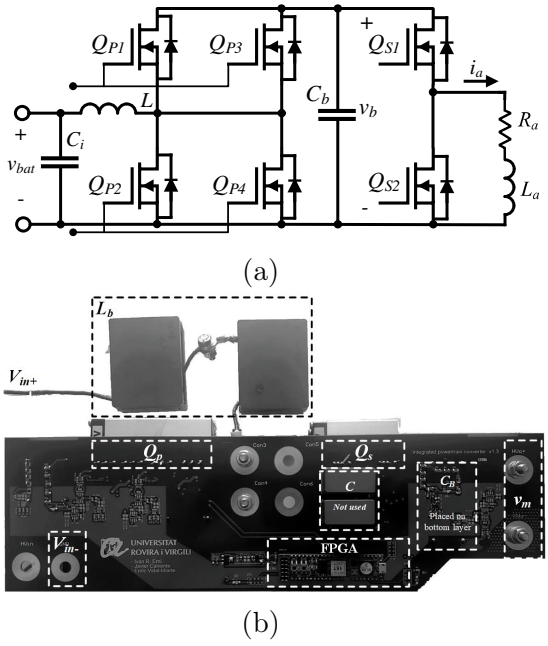


Figure 2.35: 3.3 kW boost based conventional solution. (a) Schematic. (b) Experimental.

Comparing both solutions at several bus voltages, 3.3 kW and v_{bat}=350 V, the obtained efficiency results are shown in Figure 2.36. It can be seen that at higher voltages the efficiency of the proposed converter results higher where maximum efficiency point occurs at $v_b = 2Nv_{bat}$.

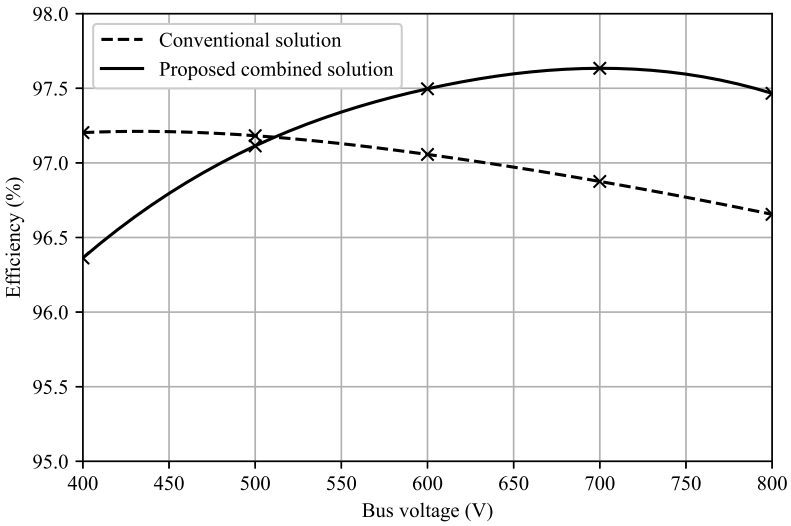


Figure 2.36: Comparison of efficiencies between the conventional solution and the combined stage at 3.3 kW and v_{bat}=350 V.

The rapid efficiency drop of the proposed converter at low voltages is due to the loss of ZVS, since the design of previous section is intended to maintain ZVS up to 550 V. Below 550 V, where lower power is required by the PMSM, it is recommended to change the operating mode to half-bridge, which varies the new point of maximum efficiency. Figure 2.36 shows how for lower power and lower bus voltages, the proposed half-bridge stage is again more efficient than the conventional solution. In addition, the proposed converter allows to step down v_b with regards to v_{bat}.

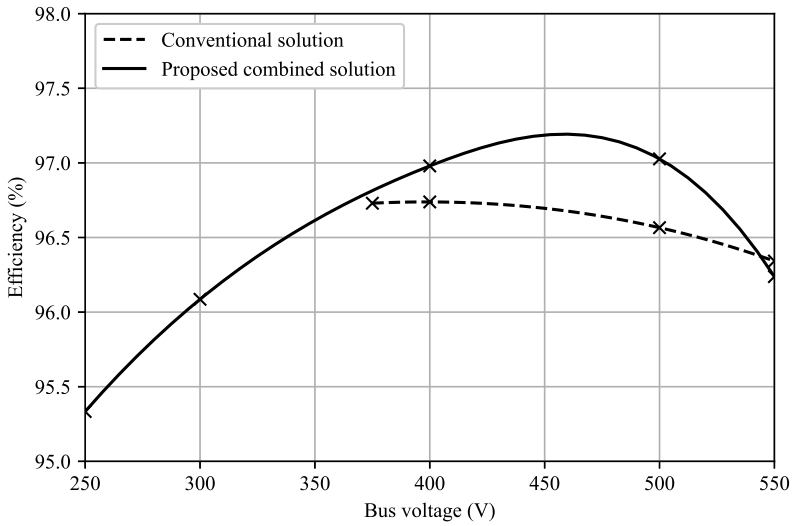


Figure 2.37: Comparison of efficiencies between the conventional solution and the combined stage at 1150 W and v_{bat}=350 V.

A second prototype has been built to validate the performance of the whole system presented in this paper, merging the motor inverter and a step up and down stage into a single converter to operate a PMSM. This low power system, depicted in Figure 2.38 with the parameters of Table 2.4, is based on Figure 2.3, placing one step up and down stage at each inverter leg and using half bridge configuration.

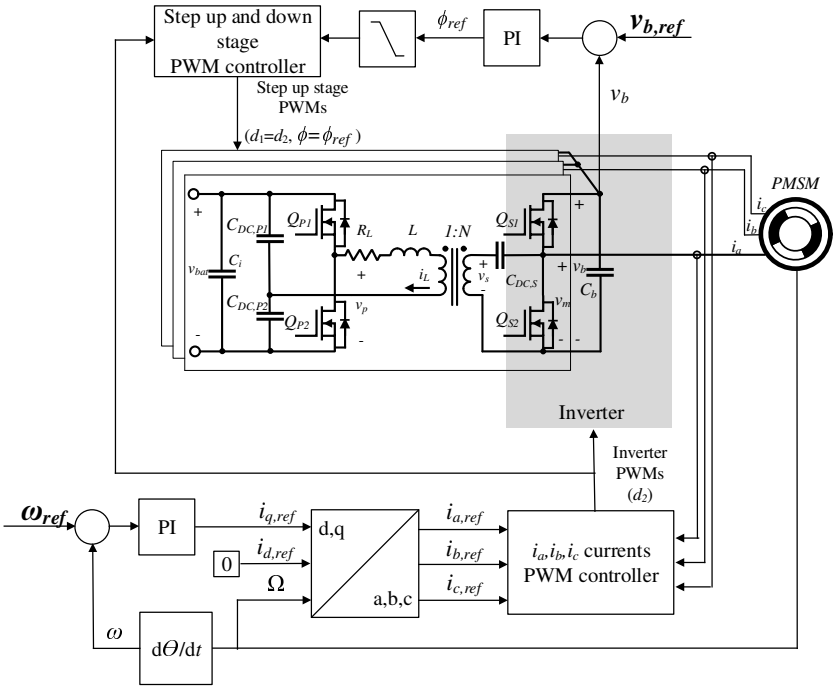
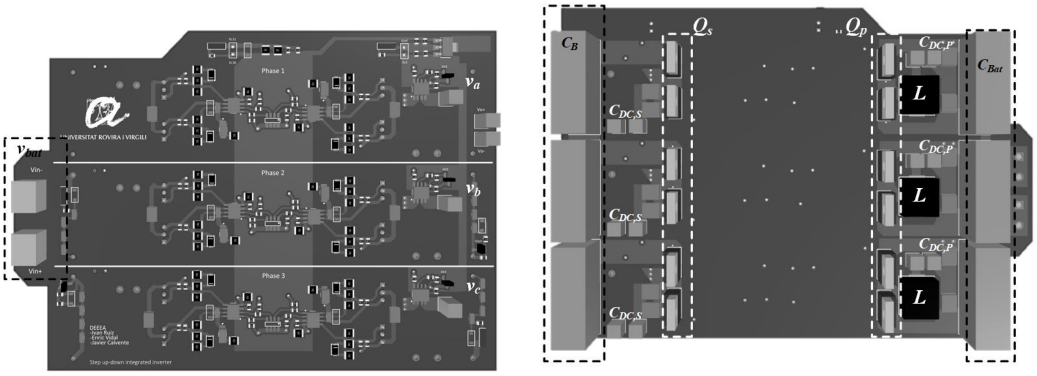


Figure 2.38: Full system experimental set with PMSM as load and Phase Shift DC bus control.

Table 2.4: Low power system design parameters.

Parameter	**Value**
Battery voltage, V_{bat}	100 V
Motor bus voltage range, V_b	200 V
Maximum phase output power, $P_{o,max}$	300 W
Turns ratio, N	2
Inductor, L	45 μH
Primary side blocking capacitor $C_{DC,P}$	4.4 μF
Secondary side blocking capacitor $C_{DC,S}$	2.2 μF
Switching frequency, f_{sw}	60 kHz
SPWM amplitude modulation index, M	0.6

The implemented converter with no heatsinks is shown in Figure 2.39.



(a) (b)

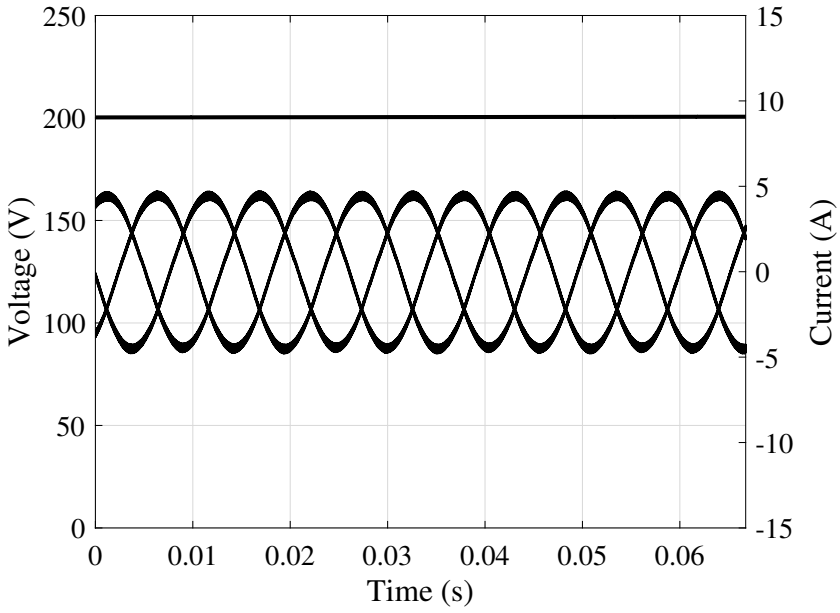
Figure 2.39: (a) Top side. (b) Bottom side. Heatsinks and transformers were not included.

The PMSM described in Table 2.5 is connected as load.

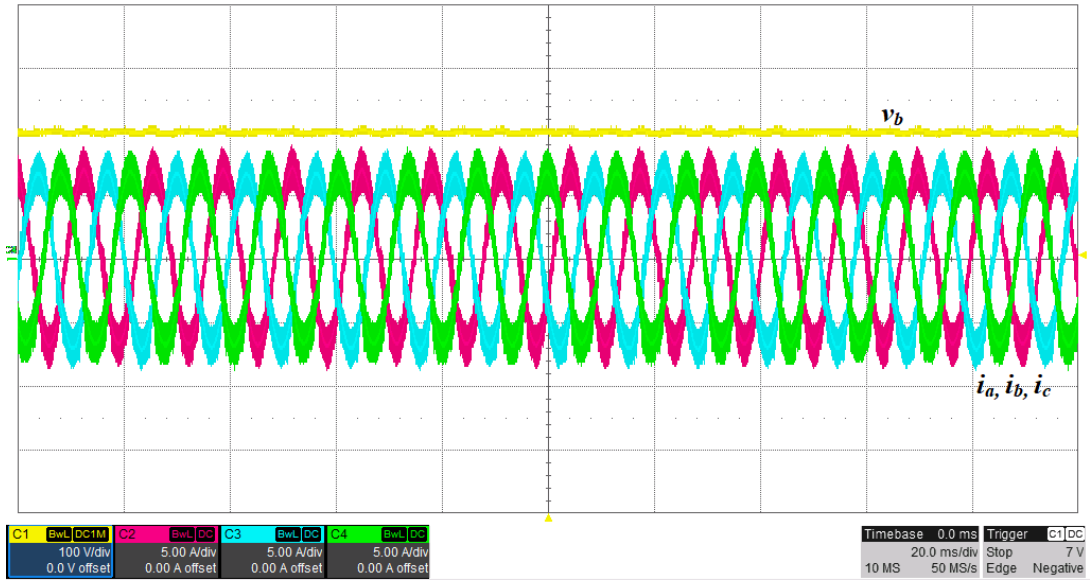
Table 2.5: Low power PMSM specifications.

Parameter	**Value**
Pole pairs	4
Rated torque, $T_{m,nom}$	1.27 Nm
Rated speed, $w_{m,nom}$	100 rad/s
Rated power, $P_{m,nom}$	300 W
Armature inductance, L_m	1 mH
Stator resistance, R_m	2.25 Ω
Torque constant, K_T	0.564 Nm/A

The semiconductors used in the step up and down stage, operating in ZVS and in the inverter are the same: STP11N60DM2. A field oriented control (FOC) to regulate the motor speed and a bus voltage control is implemented in a TMS320F280049C C2000 DSP. The FOC inverter modulation generates the inverter duty cycle. The step up and down part uses the same duty cycle as the inverter and employs the phase shift ϕ signal to regulate the bus voltage v_b. Magnetic components are made of N87 ferrite. Figure 2.40 shows the experimental results of the converter operating with v_b at 200 V and v_{bat} at 100 V when the PMSM is absorbing 300 W at 1000 rpm.



(a)

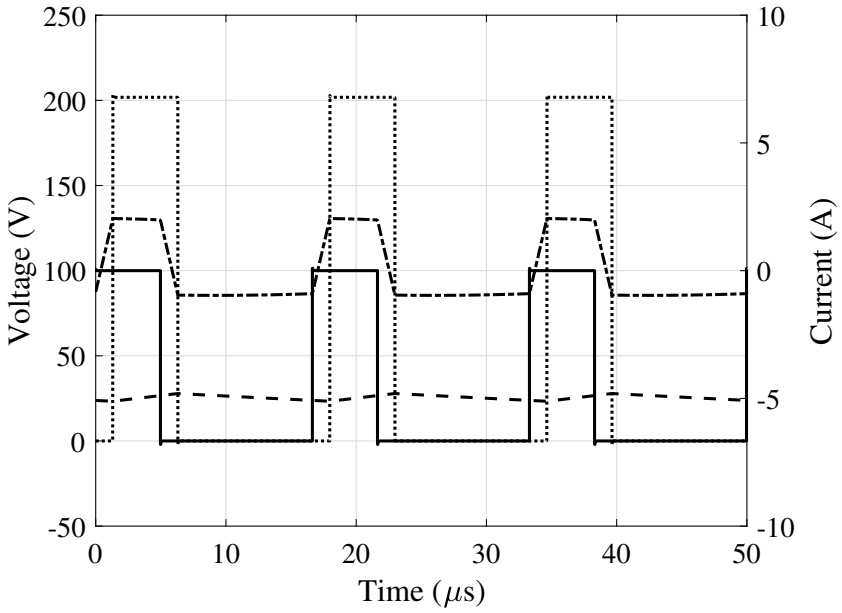


(b)

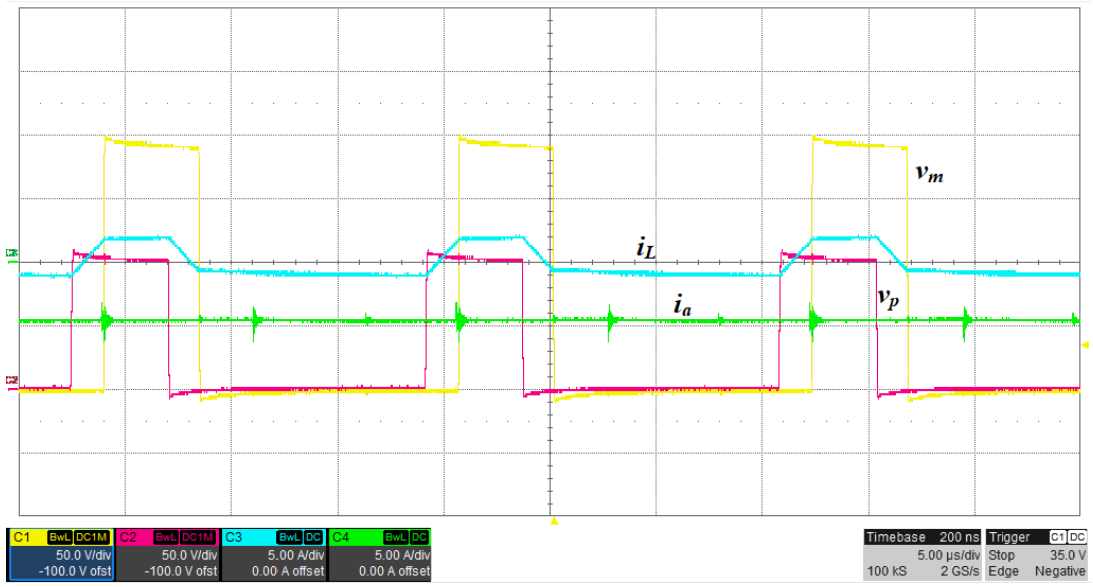
Figure 2.40: Measured converter main waveforms when the PMSM operates at 1000 rpm, absorbs 300 W and v_{bat}=100 V. Bus voltage v_b (100 V/div) and the phase currents flowing to the motor: i_a, i_b and i_c (5 A/div). (a) Simulated. (b) Experimental.

Looking in more detail one phase at the operation point shown in Figure 2.40,

Figure 2.41 and Figure 2.42 are obtained. In Figure 2.41, phase current is negative, close to its minimum peak value, which corresponds to duty cycles lower than 0.5. In contrast, in Figure 2.42 the current flows to the motor, close to its maximum peak value, which implies duty cycles greater than 0.5.

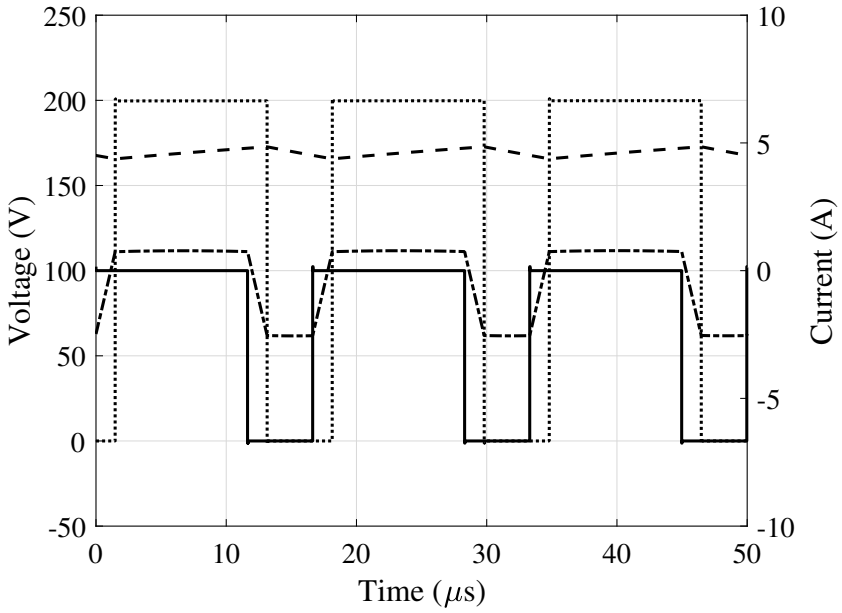


(a)

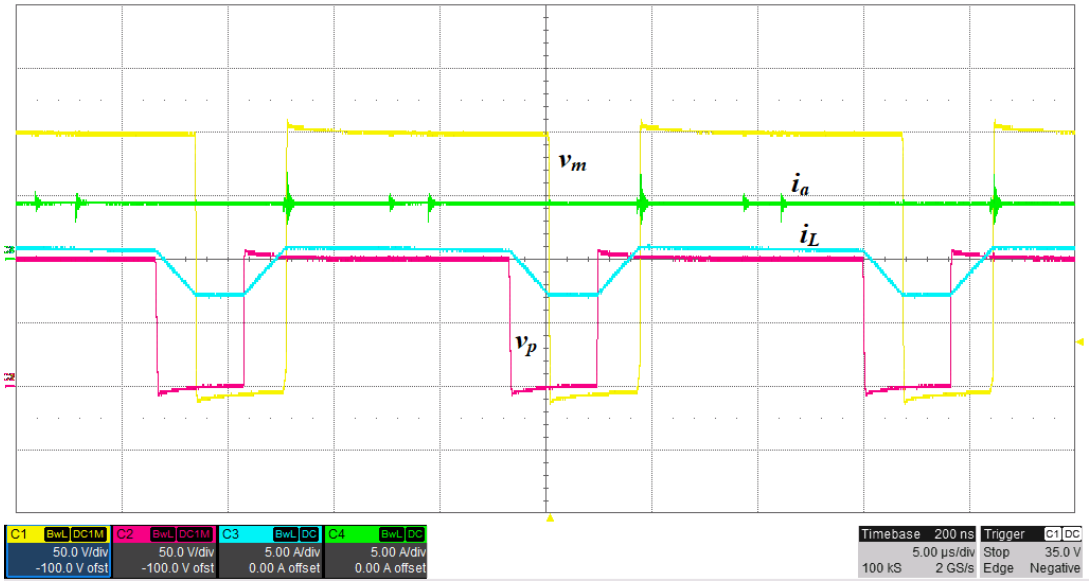


(b)

Figure 2.41: Measured converter phase waveforms when PMSM phase current is negative and v_{bat}=100 V. Inverter output voltage v_m (50 V/div), inductor current i_L (5 A/div), primary side voltage v_p (50 V/div), current flowing to the PMSM i_a (5 A/div). (a) Simulated. (b) Experimental.



(a)



(b)

Figure 2.42: Measured converter phase waveforms when PMSM phase current is positive and v_{bat}=100 V. Inverter output voltage v_m (50 V/div), inductor current i_L (5 A/div), primary side voltage v_p (50 V/div), current flowing to the PMSM i_a (5 A/div). (a) Simulated. (b) Experimental.

The experimental results in Figure 2.40, Figure 2.41 and Figure 2.42 agree

with respective results obtained by simulation. These simulated and experimental results validate the feasibility of the converter to perform both tasks with a single stage converter: Generate the low frequency AC currents to drive a PMSM and regulate the bus voltage.

2.7 Conclusions

This chapter presents the converter that combines a wide range step-up and step-down stage, and an inverter for electrical vehicle powertrain system. Analytical waveforms and loss model are developed. Based on this analysis, converter design procedure to meet main automotive requirements is proposed. From common high voltage automotive battery values, entire inverter voltage operating range is covered. ZVS is maintained in the step up and down stage. Moreover, since part of current generated at primary side flows directly to motor, inverter transistors RMS current results lower than in typical used solutions. Simulated and experimental results with two prototypes are used to validate the converter proof of concept. In summary, a compact solution that merges the inverter and the step up and down stage with less components, and wide voltage range is achieved for electrical vehicles powertrain system.

Chapter 3

Converter model

This section proposes two different models of the presented combined converter. The large signal model and the small-signal model to be able to implement different kinds of control strategies.

3.1 Non-linear discrete time model

3.1.1 Large signal analysis

The variables used in this model are shown in Figure 3.1

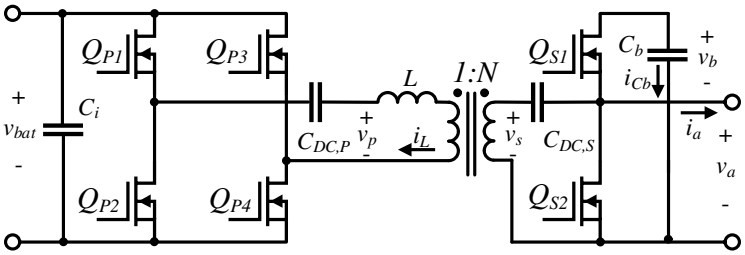


Figure 3.1: One phase of the step up and down combined converter.

The inductor current is represented by i_L, the phase current that flows to the motor by i_a and the capacitor current by i_{C_b}. The bus capacitor voltage is named as v_b, while the motor phase voltage is v_a.

The non-linear discrete time waveforms of the converter phase A current are illustrated in Figure 3.2.

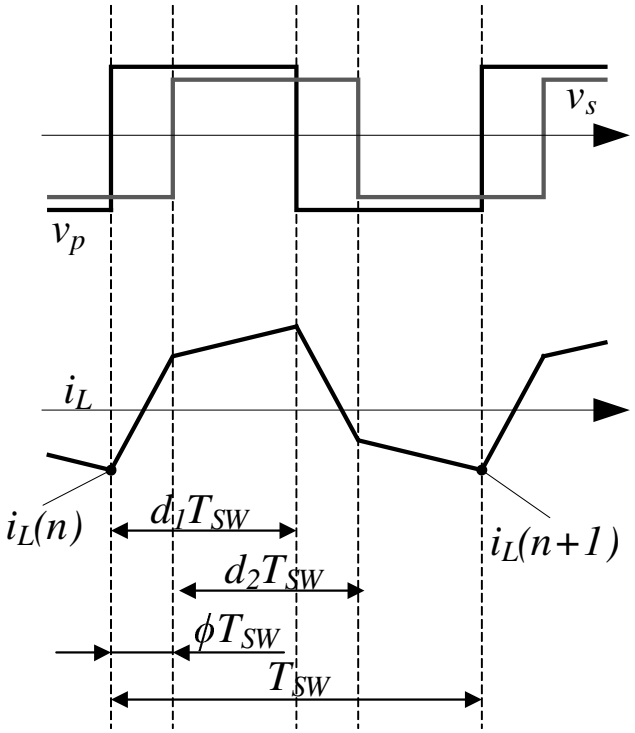


Figure 3.2: Integrated boost converter main waveforms.

In Figure 3.2, d_1 and d_2 represent v_p and v_s duty cycles respectively and ϕ is the phase difference between v_p and v_s. The inductor current at the beginning of the switching period T_{SW} is named as $i_L(n)$. Four inductor current i_L slopes are distinguished in L depending on the voltage difference between v_p and v_s/N along T_{SW}. Current i_L can be modeled from Chapter 2 using (2.6). The result of solving (2.12) is $i_L(n)$:

$$i_L(n) = \frac{(2D\phi + D^2 - D)\ v_b + (2D - 2D^2)\, N\, v_{bat}}{2LNf_{sw}} \tag{3.1}$$

In Figure 3.1, C_b is charged/ discharged by i_L and i_a when the secondary side upper transistor Q_{S1} is switched on:

$$i_{Cb}(\tau) = \begin{cases} 0 & T_{sw} < \tau \leq \phi T_{sw} \\ i_L(\tau)/N - i_a & \phi T_{sw} < \tau \leq d_1 T_{sw} \\ i_L(\tau)/N - i_a & d_1 T_{sw} < \tau \leq (d_2 + \phi) T_{sw} \\ 0 & (d_2 + \phi) T_{sw} < \tau \leq T_{sw} \end{cases} \tag{3.2}$$

The voltage capacitor evolution at the end of the switching cycle can be calculated

as:

$$v_b(n+1) = v_b(n) + \frac{1}{C_b}\int_0^{T_{sw}} i_{Cb}\mathrm{d}\tau \tag{3.3}$$

Substituting (3.2) in (3.3) results in:

$$v_b(n+1) = v_b(n) - \\ - \frac{\left(\phi^2 + \left(2d^2 - 2d\right)\phi\right)\, v_{bat} + dLN\, f_{sw} i_a \phi}{C_b LN\, {f_{sw}}^2} \tag{3.4}$$

The previous analysis has only been carried out for one phase, phase A. The control variable can be controlled independently in each phase, A ,B and C; but it is also possible to use the same control variable in common for all phases. The voltage variation across C_b changes if the rest of the phases that form the three-phase system, phases B and C, are considered. If the three phases are equal and

$$i_a = i_m \cos(\omega t) \tag{3.5a}$$
$$i_b = i_m \cos(\omega t + 2\pi/3) \tag{3.5b}$$
$$i_c = i_m \cos(\omega t - 2\pi/3) \tag{3.5c}$$

where i_m is the peak phase current flowing to the motor, then the duty cycles of each phase will also be different and related to the current carried by each phase at that moment. It is important to remember that in a PMSM motor the power factor is close to unity. A simplification for better understanding is to assume a sinusoidal modulation which gives rise to the following duty cycles:

$$d_a = \frac{M}{2}\left(1 + \cos(\omega t)\right) \tag{3.6a}$$
$$d_b = \frac{M}{2}\left(1 + \cos(\omega t + 2\pi/3)\right) \tag{3.6b}$$
$$d_c = \frac{M}{2}\left(1 + \cos(\omega t - 2\pi/3)\right) \tag{3.6c}$$

Using the same control value of ϕ, defining the incremental term of (3.4) as a function of the duty cycle d and the instantaneous current i:

$$f(d,i) = \frac{\left(\phi^2 + \left(2d^2 - 2d\right)\phi\right)\, v_{bat} + dLN\, f_{sw} i \phi}{C_b LN\, {f_{sw}}^2} \tag{3.7}$$

and combining with (3.6) and (3.5); (3.4) can be rewritten for three phases as:

$$v_b(n+1) = v_b(n) - \left(f(d_a, i_a) + f(d_b, i_b) + f(d_c, i_c)\right) \tag{3.8}$$

which solving, results in:

$$v_b(n+1) = v_b(n) - \frac{\left(12\phi^2 - 3\phi\right)\, v_{bat} + 3LN\, f_{sw} i_m}{4 C_b LN\, {f_{sw}}^2} \tag{3.9}$$

3.1.2 Discrete time small-signal model

Using previous previous discrete large signal analysis it is feasible to obtain a discrete-time small-signal analysis.

3.1.2.1 Phase to bus voltage transfer function

Equation (3.4) can be linearized around equilibrium points.

$$\hat{v_b}(n+1) = \frac{\mathrm{d}v_b(n+1)}{\mathrm{d}v_b(n)}\hat{v_b}(n) + \frac{\mathrm{d}v_b(n+1)}{\mathrm{d}\phi(n)}\hat{\phi}(n) \tag{3.10}$$

Converting into z domain and grouping terms of (3.10)

$$\frac{C_b R_a, f_{sw} z + (D - C_b R_a f_{sw})}{C_b R_a\, f_{sw} z}\hat{v_b} = -\frac{(2\Phi + 2D^2 - 2D)\; V_{bat}}{C_b L N\, {f_{sw}}^2 z}\hat{\phi} \tag{3.11}$$

and solving for $\hat{v_b}$, the phase to bus voltage discrete-time small-signal model representation of the converter is obtained:

$$G_{v\phi}(z) = \frac{\hat{v_b}}{\hat{\phi}} = -\frac{(2R\Phi + (2D^2 - 2D)\, R_a)\, V_{bat}}{C_b L N R_a, {f_{sw}}^2 z - C_b L N R_a, {f_{sw}}^2 + D L N f_{sw}} \tag{3.12}$$

where

$$R_a = \frac{V_a}{i_a} D^2 \tag{3.13}$$

and capitalized variables represents their stationary point value.

3.1.2.2 Switching frequency to bus voltage transfer function

Similar to the previous section, but linearizing for f_{sw} we obtain:

$$\hat{v_b}(n+1) = \frac{\mathrm{d}v_b(n+1)}{\mathrm{d}v_b(n)}\hat{v_b}(n) + \frac{\mathrm{d}v_b(n+1)}{\mathrm{d}f_{sw}(n)}\hat{f_{sw}}(n) \tag{3.14}$$

Applying z transform and grouping terms of (3.14)

$$\frac{C_b R_a f_{sw} z + (D - C_b R_a f_{sw})}{C_b R_a f_{sw} z}\hat{v_b} = \frac{(2R_a\Phi^2 + (4D^2 - 4D)\, R_a\Phi)\, v_i + D L N\, f_{sw} V_o}{C_b L\, N R_a {f_{sw}}^3 z}\hat{f_{sw}} \tag{3.15}$$

and solving for $\hat{v_b}$:

$$G_{vf_{sw}}(z) = \frac{\hat{v_b}}{\hat{f_{sw}}} = \frac{(2R_a\Phi^2 + (4D^2 - 4D)\, R_a\Phi)\, v_i + D L N\, f_{sw} V_b}{C_b L N R_a {f_{sw}}^3 z - C_b L N R_a {f_{sw}}^3 + D L N\, {f_{sw}}^2} \tag{3.16}$$

the switching frequency to bus voltage discrete-time small-signal model representation of the converter dynamics is attained.

3.2 Continuous-time model

The most commonly used method for modeling PWM converters is based on the averaged state-space, [36]. The application of the averaged state-space model is used in converters such as the boost or buck converter where the state variables, voltages and currents, have high DC levels and higher order harmonics are neglected. In the case of the proposed converter, this situation does not occur. The current flowing through the inductance does not contain DC level, only AC current. The model presented in this chapter is based on the generalized state-space model, explained in [37] and [38], where higher order harmonics are considered.

3.2.1 Mathematical fundamentals of the GSSAM

In this section, the mathematical basis of the generalized state-space average model is explained in depth to facilitate the understanding of the model. Fourier series allow any periodic and continuous signal in time, $f(t)$ to be decomposed into an infinite sum of sinusoidal or cosine functions called harmonics, n:

$$f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty}(a_n \cos(\frac{2\pi n}{T_{sw}}t)) + b_n \sin(\frac{2\pi n}{T_{sw}}t)) \tag{3.17}$$

where the period T_{sw} is the inverse of the switching frequency f_{sw}. The coefficient of the Fourier series a_0 refers to the 0 harmonic, $n = 0$, or DC level of the signal:

$$a_0 = \frac{2}{T_{sw}} \int_0^{T_{sw}} f(t)\mathrm{d}t \tag{3.18}$$

The remaining coefficients, a_n and b_n, represent the frequency content of the signal:

$$a_n = \frac{2}{T_{sw}} \int_0^{T_{sw}} f(t) \cos(\frac{2\pi n}{T_{sw}}t)\mathrm{d}t \tag{3.19}$$

$$b_n = \frac{2}{T_{sw}} \int_0^{T_{sw}} f(t) \sin(\frac{2\pi n}{T_{sw}}t)\mathrm{d}t \tag{3.20}$$

According to Euler's formulas:

$$\cos(nt) = \frac{e^{jnt} + e^{-jnt}}{2} \tag{3.21}$$

$$\sin(nt) = -j\frac{e^{jnt} - e^{-jnt}}{2} \tag{3.22}$$

Then, it is possible to rewrite (3.17) as:

$$f(t) = c_0 + \sum_{n=1}^{\infty}(c_n e^{jnt} + c_{-n}e^{-jnt}) = \sum_{n=-\infty}^{\infty} c_n e^{jnt} \tag{3.23}$$

where c_n can be calculated as:

$$c_n = \frac{1}{T_{sw}}\int_0^{T_{sw}} f(t)e^{-j\omega_{sw}nt}\mathrm{d}t = \langle f\rangle_n \tag{3.24}$$

or separating the real and imaginary part:

$$\Re(c_n) = \frac{1}{T_{sw}}\int_0^{T_{sw}} f(t)cos(\frac{2\pi n}{T_{sw}}t) = \langle f\rangle_n^{\Re} \tag{3.25}$$

and

$$\Im(c_n) = \frac{1}{T_{sw}}\int_0^{T_{sw}} f(t)sin(\frac{2\pi n}{T_{sw}}t) = \langle f\rangle_n^{\Im} \tag{3.26}$$

The time derivative of the coefficient $\langle f\rangle_n$ is obtained by applying Leibniz's law:

$$\begin{aligned}\frac{\mathrm{d}\langle f\rangle_n}{\mathrm{d}t} &= \frac{1}{T_{sw}}\int_0^{T_{sw}} \frac{\partial}{\partial t}(f(t)e^{jn\omega_{sw}t})\mathrm{d}t = \\ &= \frac{1}{T_{sw}}\int_0^{T_{sw}} \left(\frac{d}{dt}f(t)\right) e^{-jn\omega_{sw}t} - jn\omega_{sw}f(t)e^{-jn\omega_{sw}t}\mathrm{d}t\end{aligned} \tag{3.27}$$

Substituting equation (3.24) into (3.27), it is finally reached:

$$\frac{\mathrm{d}\langle f\rangle_n}{\mathrm{d}t} = \langle\frac{\mathrm{d}f}{\mathrm{d}t}\rangle_n - jn\omega_{sw}\langle f\rangle_n \tag{3.28}$$

Let there be two Fourier coefficients, $\langle f\rangle_n$ and $\langle h\rangle_n$, the product of these is realized by discrete convolution:

$$\langle f\rangle_n * \langle h\rangle_n = \sum_{i=-\infty}^{\infty}\langle f\rangle_i\langle h\rangle_{n-i} \tag{3.29}$$

Solving (3.29) for the continuous level, $n = 0$, and the first-order terms, $n = \pm 1$, which are part of the first harmonic, it is obtained:

$$\langle f\rangle_0 * \langle h\rangle_0 = \langle f\rangle_{-1}\langle h\rangle_1 + \langle f\rangle_0\langle h\rangle_0 + \langle f\rangle_1\langle h\rangle_{-1} \tag{3.30a}$$

$$\langle f\rangle_{-1} * \langle h\rangle_{-1} = \langle f\rangle_{-1}\langle h\rangle_0 + \langle f\rangle_0\langle h\rangle_{-1} \tag{3.30b}$$

$$\langle f\rangle_1 * \langle h\rangle_1 = \langle f\rangle_0\langle h\rangle_1 + \langle f\rangle_1\langle h\rangle_0 \tag{3.30c}$$

Assuming $\langle f\rangle_n$ must be a complex number, it is satisfied that its complementary is:

$$\langle f\rangle_n = \langle f\rangle^*_{-n} \tag{3.31}$$

Substituting (3.31) into (3.30), it is obtained:

$$\langle f\rangle_0 * \langle h\rangle_0 = \langle f\rangle_0\langle h\rangle_0 + 2\langle f\rangle_1^{\Re}\langle h\rangle_1^{\Re} + 2\langle f\rangle_1^{\Im}\langle h\rangle_1^{\Im} \tag{3.32a}$$

$$\langle f\rangle_1^{\Im} * \langle h\rangle_1^{\Im} = \langle f\rangle_1^{\Im}\langle h\rangle_0 + \langle f\rangle_0\langle h\rangle_1^{\Im} \tag{3.32b}$$

$$\langle f\rangle_1^{\Re} * \langle h\rangle_1^{\Re} = \langle f\rangle_0\langle h\rangle_1^{\Re} + \langle f\rangle_1^{\Re}\langle h\rangle_0 \tag{3.32c}$$

3.2.2 Application of the method to single phase

The equations developed in Subsection 3.2.1 are applied to the converter phase shown in Figure 3.3.

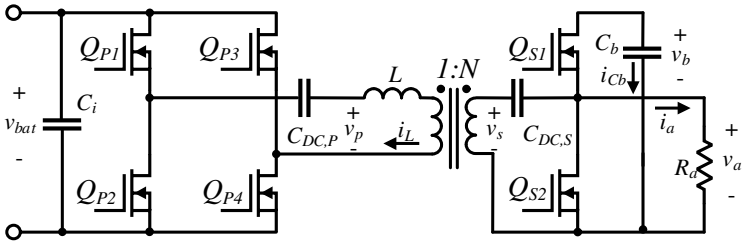


Figure 3.3: One phase of the step up and down combined converter with R_a.

Figure 3.1 differs from Figure 3.3 in that instead of modeling the output with a current, a resistor equivalent to the power absorbed by the motor is placed.

The square voltage waveforms of the primary v_p and secondary v_s bridges are proportional to the signals $u_1(t)$ and $u_2(t)$, being:

$$u_1(t) = \begin{cases} 1 & 0 < t \leq d_1 T_{sw} \\ -1 & d_1 T_{sw} < t \leq T_{sw} \end{cases} \tag{3.33}$$

and

$$u_2(t) = \begin{cases} 1 & \phi T_{sw} < t \leq (\phi + d_2) T_{sw} \\ -1 & (\phi + d_2) T_{sw} < t \leq T_{sw}(1 + \phi) \end{cases} \tag{3.34}$$

On the other hand, in the secondary side, the energy is transferred from the inductance L to the capacitor C when the signal $u_2(t)$ is positive, giving place to $u_3(t)$:

$$u_3(t) = \begin{cases} 1 & \phi T_{sw} < t \leq (\phi + d_2) T_{sw} \\ 0 & (\phi + d_2) T_{sw} < t \leq T_{sw}(1 + \phi) \end{cases} \tag{3.35}$$

Choosing as state variables the current in the inductance L, $\langle i_L(t)\rangle$ and the voltage on the output capacitor C_b, $\langle v_b(t)\rangle$, the differential equations of the stage shown in Figure 3.1 result in:

$$\frac{\mathrm{d}i_L(t)}{\mathrm{d}t} = -\frac{R_L}{L}i_L(t) + \frac{u_1(t)}{L}v_{bat}(t) - \frac{u_2(t)}{2NL}v_b(t) \tag{3.36}$$

$$\frac{\mathrm{d}v_b(t)}{\mathrm{d}t} = -\frac{u_3(t)}{C_b R_a}v_b(t) + \frac{u_3(t)}{NC_b}i_L(t) \tag{3.37}$$

It is important to remark that the current i_L does not contain a continuous level, so it is necessary to calculate at least the first harmonic $n = 1$ to obtain a valid model. The signal $v_{bat}(t)$ is considered as constant, with no ripple, so:

$$\langle v_{bat}\rangle_1^{\Re} = \langle v_{bat}\rangle_1^{\Im} = 0 \tag{3.38}$$

Applying (3.32) in (3.36) and (3.37), gives the corresponding Fourier coefficients:

$$\frac{\mathrm{d}\langle i_L\rangle_n}{\mathrm{d}t} = -\frac{R_L}{L}\langle i_L\rangle_n + \frac{\langle u_1\rangle_n * \langle v_{bat}\rangle_n}{L} - \frac{\langle u_2\rangle_n * \langle v_b\rangle_n}{2NL} \tag{3.39}$$

$$\frac{\mathrm{d}\langle v_b\rangle_n}{\mathrm{d}t} = -\frac{\langle u_3\rangle_n * \langle v_b\rangle_n}{C_b R_a} + \frac{\langle u_3\rangle_n * \langle i_L\rangle_n}{NC_b} \tag{3.40}$$

Representing (3.39) and (3.40) up to the first harmonic (n = 0,-1,1) and applying (3.32) results in :

$$\begin{aligned}\frac{\langle \mathrm{d}i_L\rangle_1^{\Re}}{\mathrm{d}t} = &-\frac{R_L}{L}\langle i_L\rangle_1^{\Re} + \frac{\langle u_1\rangle_0\langle v_{bat}\rangle_1^{\Re} + \langle u_1\rangle_1^{\Re}\langle v_{bat}\rangle_0}{L} - \\ &- \frac{\langle u_2\rangle_0\langle v_b\rangle_1^{\Re} + \langle u_2\rangle_1^{\Re}\langle v_b\rangle_0}{2NL} + \omega_{sw}\langle i_L\rangle_1^{\Im}\end{aligned} \tag{3.41}$$

$$\begin{aligned}\frac{\langle \mathrm{d}i_L\rangle_1^{\Im}}{\mathrm{d}t} = &-\frac{R_L}{L}\langle i_L\rangle_1^{\Im} + \frac{\langle u_1\rangle_0\langle v_{bat}\rangle_1^{\Im} + \langle u_1\rangle_1^{\Im}\langle v_{bat}\rangle_0}{L} - \\ &- \frac{\langle u_2\rangle_0\langle v_b\rangle_1^{\Im} + \langle u_2\rangle_1^{\Im}\langle v_b\rangle_0}{2NL} - \omega_{sw}\langle i_L\rangle_1^{\Re}\end{aligned} \tag{3.42}$$

$$\begin{aligned}\frac{\langle \mathrm{d}v_b\rangle_0}{\mathrm{d}t} = &-\frac{\langle v_b\rangle_0\langle u_3\rangle_0}{C_b R_a} - \frac{2(\langle u_3\rangle_1^{\Re}\langle v_b\rangle_1^{\Re} + \langle u_3\rangle_1^{\Im}\langle v_b\rangle_1^{\Im})}{C_b R_a} + \\ &+ \frac{2(\langle u_3\rangle_1^{\Re}\langle i_L\rangle_1^{\Re} + \langle u_3\rangle_1^{\Im}\langle i_L\rangle_1^{\Im})}{NC_b}\end{aligned} \tag{3.43}$$

$$\frac{\langle \mathrm{d}v_b\rangle_1^{\Re}}{\mathrm{d}t} = -\frac{\langle v_b\rangle_1^{\Re}\langle u_3\rangle_0}{C_b R_a} - \frac{\langle v_b\rangle_0\langle u_3\rangle_1^{\Re}}{C_b R_a} + \frac{\langle u_3\rangle_0\langle i_L\rangle_1^{\Re}}{NC_b} + \omega_{sw}\langle v_b\rangle_1^{\Im} \tag{3.44}$$

$$\frac{\langle \mathrm{d}v_b\rangle_1^{\Im}}{\mathrm{d}t} = -\frac{\langle v_b\rangle_1^{\Im}\langle u_3\rangle_0}{C_bR_a} - \frac{\langle v_b\rangle_0\langle u_3\rangle_1^{\Im}}{C_bR_a} + \frac{\langle u_3\rangle_0\langle i_L\rangle_1^{\Im}}{NC_b} - \omega_{sw}\langle v_b\rangle_1^{\Re} \tag{3.45}$$

where $w_{sw} = 2\pi f_{sw}$.

Defining the state vector $\boldsymbol{x}$ as:

$$\boldsymbol{x} = [\langle i_L\rangle_1^{\Re}\ \langle i_L\rangle_1^{\Im}\ \langle v_b\rangle_0\ \langle v_b\rangle_1^{\Re}\ \langle v_b\rangle_1^{\Im}]' \tag{3.46}$$

and the input vector $\boldsymbol{u}$:

$$\boldsymbol{u} = [\langle v_{bat}\rangle_0] \tag{3.47}$$

equations (3.41)-(3.45) can be represented in matrix form, obtaining the state-space model:

$$\dot{\boldsymbol{x}} = \boldsymbol{A}\boldsymbol{x} + \boldsymbol{B}\boldsymbol{u} \tag{3.48}$$

Being$\boldsymbol{A}$:

$$\boldsymbol{A} = \begin{bmatrix} -\frac{R_L}{L} & \omega_{sw} & -\frac{\langle u_2\rangle_1^{\Re}}{2NL} & -\frac{\langle u_2\rangle_0}{2NL} & 0 \\ -\omega_{sw} & -\frac{R_L}{L} & -\frac{\langle u_2\rangle_1^{\Im}}{2NL} & 0 & -\frac{\langle u_2\rangle_0}{2NL} \\ \frac{2\langle u_3\rangle_1^{\Re}}{NC_b} & \frac{2\langle u_3\rangle_1^{\Im}}{NC_b} & -\frac{\langle u_3\rangle_1}{C_bR_a} & \frac{2\langle u_3\rangle_1^{\Re}}{C_bR_a} & \frac{2\langle u_3\rangle_1^{\Im}}{C_bR_a} \\ \frac{\langle u_3\rangle_0}{NC_b} & 0 & -\frac{\langle u_3\rangle_1^{\Re}}{C_bR_a} & -\frac{\langle u_3\rangle_0}{C_bR_a} & \omega_{sw} \\ 0 & \frac{\langle u_3\rangle_0}{NC_b} & -\frac{\langle u_3\rangle_1^{\Im}}{C_bR_a} & -\omega_{sw} & -\frac{\langle u_3\rangle_0}{C_bR_a} \end{bmatrix} \tag{3.49}$$

and $\boldsymbol{B}$:

$$\boldsymbol{B} = \begin{bmatrix} \frac{\langle u_1\rangle_1^{\Re}}{L} \\ \frac{\langle u_1\rangle_1^{\Im}}{L} \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{3.50}$$

The continuous and first-order Fourier coefficients of the signals $u_1(t)$, $u_2(t)$ and $u_3(t)$ are obtained from developing the Fourier series of the signals (3.33), (3.34) and (3.35) by means of (3.17), (3.25) and (3.26). In this way, it is obtained for $u_1(t)$:

$$\langle u_1\rangle_0 = 2d_1 - 1 \tag{3.51a}$$

$$\langle u_1\rangle_1^{\Re} = \frac{\sin(2\pi d_1)}{\pi} \tag{3.51b}$$

$$\langle u_1\rangle_1^{\Im} = \frac{\cos(2\pi d_1) - 1}{\pi} \tag{3.51c}$$

for $u_2(t)$:

$$\langle u_2\rangle_0 = 2d_2 - 1 \tag{3.52a}$$

$$\langle u_2\rangle_1^{\Re} = \frac{\sin(2\pi\phi + 2\pi d_2) - \sin(2\pi\phi)}{\pi} \tag{3.52b}$$

$$\langle u_2 \rangle_1^{\Im} = \frac{\cos(2\pi\phi + 2\pi d_2) - \cos(2\pi\phi)}{\pi} \tag{3.52c}$$

and for $u_3(t)$

$$\langle u_3 \rangle_0 = d_2 \tag{3.53a}$$

$$\langle u_3 \rangle_1^{\Re} = \frac{\sin(2\pi\phi + 2\pi d_2) - \sin(2\pi\phi)}{\pi} \tag{3.53b}$$

$$\langle u_3 \rangle_1^{\Im} = \frac{\cos(2\pi\phi + 2\pi d_2) - \cos(2\pi\phi)}{\pi} \tag{3.53c}$$

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3.2.3 Small-signal model

The system represented in (3.48) contains non-linear terms. For this reason, to design the control loop, it is necessary to linearize the system around an equilibrium point $\boldsymbol{x_{eq}}$, where there are no significant variations.

The equilibrium point $\boldsymbol{x_{eq}}$ is obtained from eliminating the derivative in (3.48), $\dot{\boldsymbol{x}} = 0$, and solving:

$$\boldsymbol{x_{eq}} = -\boldsymbol{A}^{-1}\boldsymbol{B}\boldsymbol{u} \tag{3.54}$$

By introducing a small perturbation in the control variables, in this case: $\hat{\phi}$, $\hat{d}_1$, $\hat{d}_2$ or $\hat{\omega}_{sw}$, the state variables will vary with respect to the equilibrium point. Perturbing the system around the equilibrium point yields the small-signal model. Linear approximation of the system is obtained thorough the first order term of the Taylor Series representation. Let $f(x)$ be continuous and differentiable, x_{eq} the equilibrium point and $\hat{x}$ a small perturbation, it is satisfied:

$$\hat{x} = x - x_{eq} \tag{3.55}$$

and

$$f(x) = \hat{\dot{x}} \approx f(x_{eq}) + f'(x_{eq})(x - x_{eq}) = 0 + f'(x_{eq})\hat{x} \tag{3.56}$$

The first order derivative $f'(x_{eq})$ at the equilibrium point is calculated by the Jacobian of the system. Being:

$$f(\boldsymbol{x}, \phi, d_1, d_2, \omega_{sw}) = (\boldsymbol{A}\boldsymbol{x} + \boldsymbol{B}\boldsymbol{u}) \tag{3.57}$$

Applying the Jacobian matrix in (3.57)

$$\frac{\mathrm{d}\langle\hat{\boldsymbol{x}}\rangle}{\mathrm{d}t} = \nabla f(\boldsymbol{x}, \phi, d_1, d_2, \omega_{sw}) \tag{3.58}$$

it is obtained the small-signal representation of the system:

$$\hat{\dot{\boldsymbol{x}}} = \hat{\boldsymbol{A}}\hat{\boldsymbol{x}} + \hat{\boldsymbol{B}}\hat{\boldsymbol{u}} + \hat{\boldsymbol{E}}\hat{\boldsymbol{\phi}} + \hat{\boldsymbol{E}}_{\boldsymbol{1}}\hat{\boldsymbol{d}}_{\boldsymbol{1}} + \hat{\boldsymbol{E}}_{\boldsymbol{2}}\hat{\boldsymbol{d}}_{\boldsymbol{2}} + \hat{\boldsymbol{E}}_{\boldsymbol{3}}\hat{\boldsymbol{\omega}}_{\boldsymbol{sw}} \tag{3.59}$$

where:

$$\hat{\boldsymbol{A}} = \begin{bmatrix} -\frac{R_L}{L} & \omega_{sw} & -\frac{\langle U_2\rangle_1^{\Re}}{2NL} & -\frac{\langle U_2\rangle_0}{2NL} & 0 \\ -\omega_{sw} & -\frac{R_L}{L} & -\frac{\langle U_2\rangle_1^{\Im}}{2NL} & 0 & -\frac{\langle U_2\rangle_0}{2NL} \\ \frac{2\langle U_3\rangle_1^{\Re}}{NC_b} & \frac{2\langle U_3\rangle_1^{\Im}}{NC_b} & -\frac{1}{CR} & 0 & 0 \\ \frac{N\langle U_3\rangle_0}{C_b} & 0 & 0 & -\frac{1}{C_bR_a} & \omega_{sw} \\ 0 & \frac{\langle U_3\rangle_0}{NC_b} & 0 & -\omega_{sw} & -\frac{1}{C_bR_a} \end{bmatrix} \tag{3.60}$$

$$\hat{\boldsymbol{x}} = [\langle \hat{i}_L\rangle_1^{\Re}\ \langle \hat{i}_L\rangle_1^{\Im}\ \langle \hat{v}_b\rangle_0\ \langle \hat{v}_b\rangle_1^{\Re}\ \langle \hat{v}_b\rangle_1^{\Im}]' \tag{3.61}$$

$$\hat{\boldsymbol{B}} = \begin{bmatrix} \frac{\langle U_1\rangle_1^{\Re}}{L} \\ \frac{\langle U_1\rangle_1^{\Im}}{L} \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{3.62}$$

$$\hat{\boldsymbol{E}} = \begin{pmatrix} -\frac{(\cos(2\pi\Phi+2\pi D_2)-\cos(2\pi\Phi))\langle \hat{V}_b\rangle_0}{LN} \\ \frac{(\sin(2\pi\Phi+2\pi D_2)-\sin(2\pi\Phi))\langle \hat{V}_b\rangle_0}{LN} \\ \frac{\alpha_1}{CR}+\frac{\alpha_2}{CN} \\ -\frac{(2\cos(2\pi\Phi+2\pi D_1)-2\cos(2\pi\Phi))\langle \hat{V}_b\rangle_0}{CR} \\ \frac{(2\sin(2\pi\Phi+2\pi D_1)-2\sin(2\pi\Phi))\langle \hat{V}_b\rangle_0}{CR} \end{pmatrix} \tag{3.63}$$

where

$$\alpha_1 = -4\cos(2\pi\Phi+2\pi D)\langle \hat{V}_b\rangle_0^{\Re} + 4\cos(2\pi\Phi)\langle \hat{V}_b\rangle_0^{\Re} + 4\sin(2\pi\Phi+2\pi D)\langle \hat{V}_b\rangle_0^{\Im} \tag{3.64}$$

and

$$\begin{aligned}\alpha_2 = -4\langle \hat{I}_L\rangle_1^{\Im}\sin(2\pi\Phi+2\pi D) + 4\langle \hat{I}_L\rangle_1^{\Re}\cos(2\pi\Phi+2\pi D)CN+ \\ +4\langle \hat{I}_L\rangle_1^{\Im}\sin(2\pi\Phi) - 4\langle \hat{I}_L\rangle_1^{\Re}\cos(2\pi\Phi)\end{aligned} \tag{3.65}$$

$$\hat{\boldsymbol{E}}_{\boldsymbol{3}} = \begin{bmatrix} \langle I_L\rangle_1^{\Im} \\ -\langle I_L\rangle_1^{\Re} \\ 0 \\ \langle V_b\rangle_1^{\Im} \\ -\langle V_b\rangle_1^{\Re} \end{bmatrix} \tag{3.66}$$

Capitalized letters in the above equations represent the variables at their equilibrium point. These variables result in the equation (3.54). $\hat{\boldsymbol{E}}$ is illustrated since it would be used to calculate the transfer function using ϕ as a control variable. Another option is to use $\hat{\boldsymbol{E}}_{\boldsymbol{3}}$ to employ ω_{sw} as control variable. $\hat{\boldsymbol{E}}_{\boldsymbol{1}}$ and $\hat{\boldsymbol{E}}_{\boldsymbol{2}}$ are not represented due to the lack of interest from the control point of view.

3.2.3.1 Phase to bus voltage transfer function

The state variable to be usually regulated in this topology is the DC bus voltage v_b. The most simple way to control it, is using ϕ. Therefore, using (3.59), (3.60), (3.61) and (3.63) the small-signal representation required to design the controller become:

$$\frac{\mathrm{d}\hat{\boldsymbol{x}}}{\mathrm{d}t} = \hat{\boldsymbol{A}}\hat{\boldsymbol{x}} + \hat{\boldsymbol{E}}\hat{\phi} \tag{3.67}$$

The control signal to bus voltage transfer function is denoted as:

$$G_{v\phi}(s) = \boldsymbol{C}(s\boldsymbol{I} - \hat{\boldsymbol{A}})\hat{\boldsymbol{E}} \tag{3.68}$$

where $\boldsymbol{C}$ is:

$$\boldsymbol{C} = [0\ 0\ 1\ 0\ 0] \tag{3.69}$$

If the three phases are considered due to the use of R_a in the model, gain must be multiplied by 3 and the average value of D along one sinusoidal cycle must be considered.

3.2.3.2 Frequency to bus voltage transfer function

Another option is to use the switching frequency f_{sw} to control v_b. Using previous section analysis is easy to obtain it:

$$\frac{\mathrm{d}\hat{\boldsymbol{x}}}{\mathrm{d}t} = \hat{\boldsymbol{A}}\hat{\boldsymbol{x}} + \hat{\boldsymbol{E}}_{\boldsymbol{3}}\hat{\omega} \tag{3.70}$$

The control signal to bus voltage transfer function is denoted as:

$$G_{vf_{sw}}(s) = 2\pi\boldsymbol{C}(s\boldsymbol{I} - \hat{\boldsymbol{A}})\hat{\boldsymbol{E}}_{\boldsymbol{3}} \tag{3.71}$$

3.3 Model comparison

In order to analyze the obtained continuous-time and discrete-time small-signal models of the combined converter, both of them will be compared in the frequency domain with the model obtained through the switched circuit model using MATLAB-Simulink. The following converter parameters are used:

Table 3.1: Equilibrium point parameters.

Parameter	Value
V_{in}	400 V
V_o	800 V
ϕ	0.071
D_1	0.5
D_2	0.5
f_{sw}	50 kHz
N	1
L	59 μH
R_L	50 mΩ
C_b	60 μF
R_a	97 Ω

3.3.1 Bode plots

3.3.1.1 Phase to bus voltage transfer function

Substituting Table 3.1 parameters in (3.68) results in the following discrete transfer function:

$$G_{v\phi}(z) = \frac{6144000}{377600z - 376951} \tag{3.72}$$

where just one pole is appreciated. If Table 3.1 parameters are substituted in the transfer function obtained with the continuous model (3.12), a much more complex transfer function is obtained:

$$G_{v\phi}(s) = \\ -66442\frac{(s+1.101\times10^6)(s-1.101\times10^6)(s^2-0.0001773s+9.86\times10^{10})}{(s+85.94)(s^2+0.793s+9.86\times10^{10})(s^2+172.8s+9.865\times10^{10})} \tag{3.73}$$

Both transfer functions are represented in the Bode diagram of Figure 3.4.

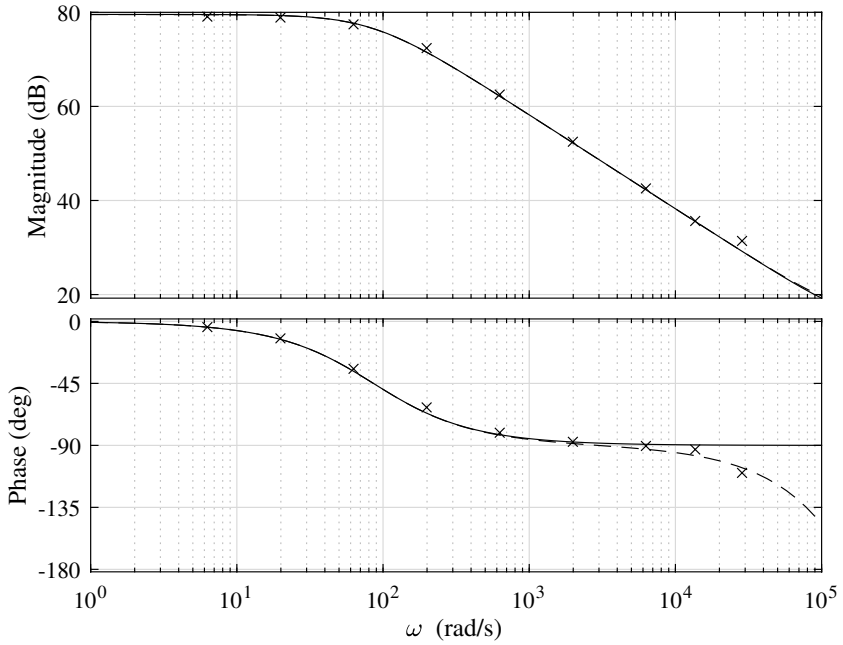


Figure 3.4: Frequency response of $G_{v\phi}$. Solid line: Continuous. Dashed line: Discrete. Crosses: Points obtained with Matlab/Simulink.

It can be seen that although looks like different models, in the useful frequencies their behaviours are similar, dominated by one single pole. In Figure 3.4, it is also possible to observe an agreement between the frequency representation of the obtained model and that obtained by simulation with Matlab/Simulink.

3.3.1.2 Frequency to bus voltage transfer function

Equation (3.74) is the transfer function (3.16) after substituting the values of Table 3.1.

$$G_{vf_{sw}}(z) = -\frac{162646}{5900000000z - 5889859375} \tag{3.74}$$

In the same way, the numerical representation of (3.71) is:

$$G_{vf_{sw}}(s) = \frac{66476(s - 1.96 \times 10^6)(s^2 - 0.000131s + 9.86 \times 10^{10})}{(s + 85.94)(s^2 + 0.793s + 9.86 \times 10^{10})(s^2 + 172.8s + 9.865 \times 10^{10})} \tag{3.75}$$

The representation of previous transfer functions is shown by Figure 3.5 where an agreement between both models and the data obtained by means of simulation are similar.

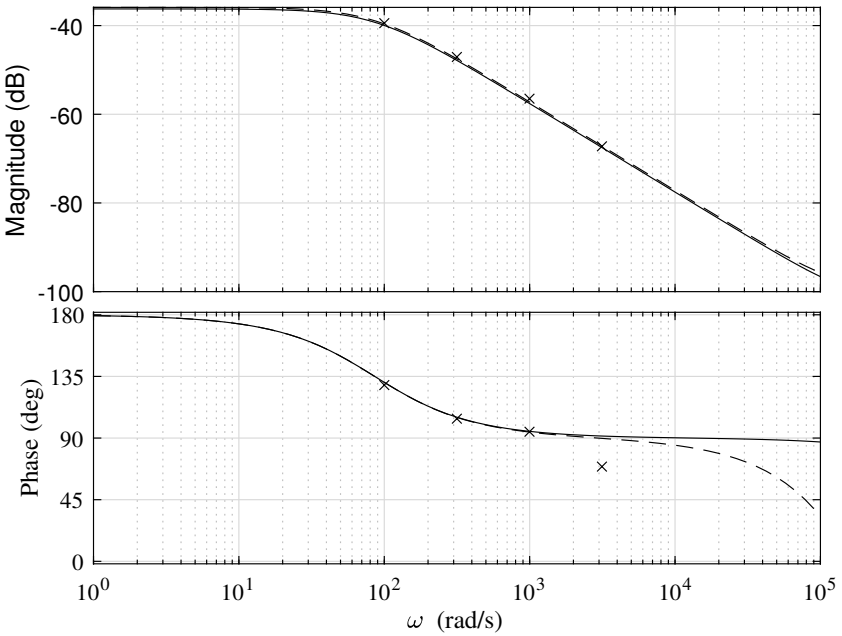


Figure 3.5: Frequency response of $G_{vf_{sw}}$. Solid line: Continuous. Dashed line: Discrete. Crosses: Points obtained with Matlab/Simulink.

It is important to remark that, due the calculation of the First Fourier harmonic for obtaining the model, (3.72) and (3.75) present high-frequency modeling effects in form of resonance and non minimum phase dynamics. The high frequency resonance is placed at the switching frequency and the right half plane zero represents the delay in power output transmission, which is related to $d_2 T_{sw}$ plus ϕ. However, these high frequency effects are far away of the useful frequency range of a small-signal model, which is below half of the switching frequency, and usually are not taken into account for control design purposes.

3.4 Conclusions

Two different models, one obtained from the discrete time equations and the other based on continuous time, have been developed in this chapter. For both models, the transfer functions from the control signals, phase and frequency, to the voltage to be regulated are developed. The transfer functions obtained with both models and those obtained with Matlab/Simulink show very similar results. Although they are practically identical, the transfer functions obtained with the discrete model are easier to operate and where parameters conditioning the frequency response are easily identifiable.

Chapter 4

Bus voltage regulation

In this chapter, the previous continuous-time and discrete time models, obtained in chapter 3 are used to design respectively linear and non-linear discrete-time controllers for bus voltage regulation.

4.1 Non linear control

Due to specifications, converters must support critical conditions where the converter output regulation and robustness result crucial. Since converters are being recently used in mass production, lots of errors and unexpected behaviours arises during the first years of the product. Any HW change results fateful due to the product recall and manual substitution of the parts. Given previous circumstances, digital control results a mandatory condition in the requirements of the product making them easy to update. Another issues of mass production are the large tolerance of the converter components and the unexpected line and load disturbances along the multiple situations.

Among the non-linear controllers the main advantages of the sliding controllers are the low sensitivity to the plant parameter variations and disturbances which eliminates the necessity of exact modeling, [39] and [40]. Discrete-time sliding control allows designing and analyzing direct digital controllers for power converter, [41, 42], using a discrete-time converter model achieving similar dynamics behavior than the continuous sliding mode. However, the controller depends on plant parameters.

To guarantee proper operation, this chapter presents a digital proportional control based on discrete-time sliding of the converter bus voltage [43]. In this type of controls usually, as detailed in [41, 42, 44], inductor current is controlled with a fast control loop via sliding based regulation, while bus voltage is controlled by a slower proportional integral control loop which sets the inductor current reference.

Also, it allows to implement digital loss free resistors for PFC applications [45]. Inductor current sensing at high speeds results in an extra noticeable cost that, if it is possible, must be avoided. Thus, bus voltage value is controlled directly. In this section, discrete-time approach of the sliding-mode control theory is applied and accurate description of the converter dynamics are obtained. Thanks to that, a sliding based control for the converter is proposed and the closed loop stability is proved analytically.

4.1.1 Discrete-time sliding-mode voltage control

Sliding mode control is a variable frequency control that is usually applied in variable structured systems [46, 47]. The structure variation forces the controlled variable trajectory to evolve towards a particular surface. When the surface is reached, the controlled variable trajectory slides on the neighbourhood of this surface. This is why it is called sliding surface. Figure 4.1 describes this situation, where the selected surface is $s = x + \dot{x} = \sigma$. Depending on σ value condition, the control structure varies to make $\sigma = 0$.

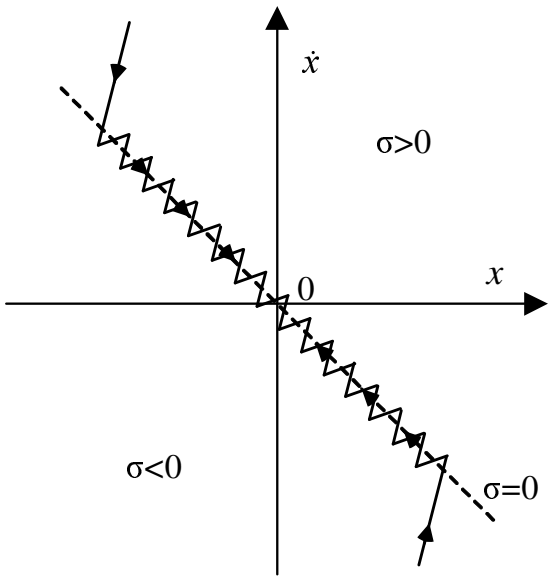


Figure 4.1: Sliding surface.

In case the presented converter, for bus voltage regulator a classical sliding control surface could be the following:

$$s(t) = v_b^* - v_b(t) \tag{4.1}$$

In a pure sliding mode regulator, the control action $\phi(n)$ would have the following action:

$$\phi(n) = \begin{cases} \frac{D}{2}, & \text{if } s \geq 1 \\ 0, & \text{otherwise} \end{cases} \tag{4.2}$$

The control will change its structure between two points, in that case: the first point where the converter delivers the maximum power $D/2$ and the point where it delivers the minimum power 0. When the sliding surface is reached, continuous switching between these two points will cause excessive ripple in the output, known as chattering, making it impractical.

A discrete switching surface $s(n)$ that provides asymptotic behavior when the converter dynamics are forced to evolve over it, must be selected. The converter dynamics should move towards the surface. In order to reach the desired output capacitor voltage reference v_b^*, the following discrete time manifold is selected:

$$s(n) = v_b^* - v_b(n) \tag{4.3}$$

where n represents the nth sampling period, in this case the beginning of the nth switching, as represented in Figure 3.2. The surface defined in (4.3) must converge so the system must evolve to make v_b equal to v_b^* in the next sampling period:

$$s(n+1) = 0 = v_b^* - v_b(n+1) \tag{4.4}$$

For a single phase of the converter, which is shown in Figure 3.1, substituting (3.4) into (4.4) yields:

$$v_b^* - v_b(n) + \frac{\left(\phi^2 + \left(2D^2 - 2D\right)\phi\right) v_{bat} + DLN\, f_{sw} i_a}{C_b LN\, {f_{sw}}^2} = 0 \tag{4.5}$$

The control action that equals the reference at next switching cycle $(n+1)$ can be derived from (4.5). As illustrated in Figure 4.2, a smooth control action ϕ_{eq}, which is equivalent to the variation of ϕ between $D/2$ and 0 over time, is used. This is an extension of the equivalent control notion in continuous-time systems to a discrete-time context [43, 48].

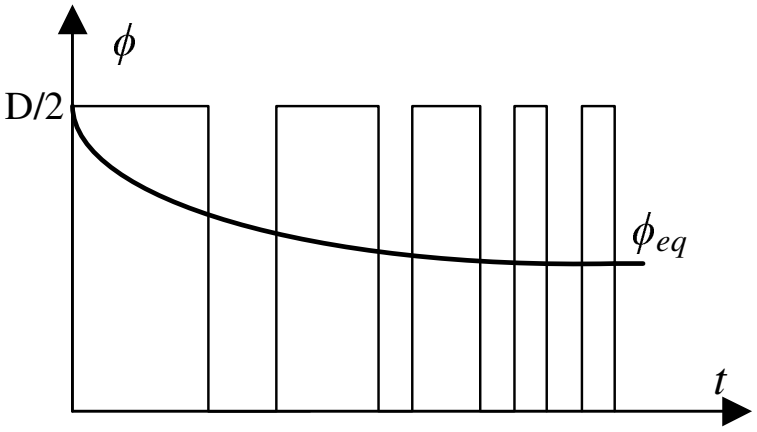


Figure 4.2: Equivalent control action.

It is assumed that v_b^* is constant during several cycles, therefore the average value can be used V_b^*. The same occurs for $v_{bat}(n)$ that is assumed constant, where V_{bat} is the averaged value. Equivalent control action signal ϕ_{eq} is obtained from (4.5) solving for ϕ:

$$\phi_{eq} = D\,(1-D) - \frac{\sqrt{\left(\left(D^4 - 2D^3 + D^2\right)\,V_{bat} + C_b LN\,{f_{sw}}^2 e(n) - DLN\,f_{sw} i_a\right) V_{bat}}}{V_{bat}} \tag{4.6}$$

where the error $e(n)$ is defined as:

$$e(n) = V_b^* - v_b(n) \tag{4.7}$$

It is worth of noting the control action is not a pure sliding mode control one, which would imply the application of a bivalent ($\{\phi_{min}, \phi_{min}\}$) discontinuous control action. In this case, the control action is a discrete-time continuous multivalent ($[\phi_{min}, \phi_{min}]$) control action.

It must be noted that the equivalent control action is not a pure sliding mode regulator, being a control based on a continuous action signal.

Equivalent control action value must be limited according to minimum and maximum power delivering capacities of the converter, described by (2.20) in Chapter 2:

$$0 \leq \phi_{eq}(n) \leq D_{crit} \tag{4.8}$$

where D_{crit}

$$D_{crit} = \begin{cases} D/2, & D \leq 0.5 \\ (1-D)/2, & D > 0.5 \end{cases} \tag{4.9}$$

In case ϕ_{eq} overpass the restrictions of (4.8), the control action must be saturated:

$$\phi(n) = \begin{cases} 0, & \phi_{eq}(n) < 0 \\ \phi_{eq}(n) & 0 \leq \phi_{eq}(n) \leq D_{crit} \\ D_{crit} & \phi_{eq}(n) > D_{crit} \end{cases} \tag{4.10}$$

It must be noted that the lower limit of $\phi(n)$ is set to 0 to avoid absorbing energy. If regenerative braking is desired, which implies transferring energy from the motor to the battery, $-D_{crit}$ should be placed instead 0.

When $\phi(n)$ is saturated at the upper or lower limit, (4.4) is not satisfied. To ensure the existence of discrete-time sliding motion in further cycles, the convergence to the surface defined in (4.3) must be proved.

4.1.2 Reachability condition

The desired discrete-time sliding mode dynamics must be attained and maintained. To reach the discrete time sliding behaviour, the following condition which ensures that $s(n+1)$ decreases must be guaranteed:

$$||s(n+1)|| < ||s(n)|| \tag{4.11}$$

which is equivalent to:

$$s(n+1)\Delta s < 0 \tag{4.12}$$

where

$$\Delta s = s(n+1) - s(n) \tag{4.13}$$

Substituting (4.3) and (4.4) into (4.13), it results:

$$\Delta s = \frac{\left(\phi^2 + \left(2D^2 - 2D\right)\phi\right)\, v_{bat} + DLN\, f_{sw} i_a}{C_b L N\, {f_{sw}}^2} \tag{4.14}$$

According to (4.10), two reachability cases, shown in Figure 4.3 appear depending on the saturation condition.

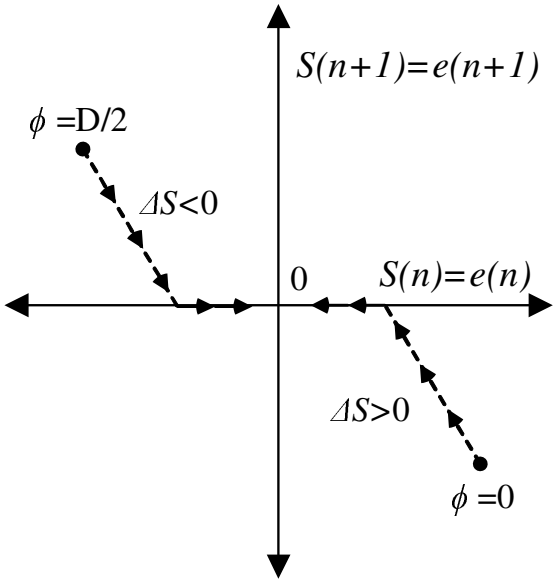


Figure 4.3: Reachability conditions.

In (4.14) and Figure 4.3, if ϕ is saturated to the lower limit $\phi = 0$, it implies that $s(n+1) < 0$ so, Δs must be positive to satisfy (4.12). After substituting $\phi = 0$ in (4.14) and simplifying, it results:

$$\Delta s = D i_a > 0 \tag{4.15}$$

which means that the system will move towards the surface if a load is connected. It must be noted that ϕ was limited to positive values where no regenerative braking exists.

In contrast, when ϕ is saturated to the higher limit $\phi = D/2$, it yields to $s(n+1) > 0$. To meet (4.12), Δs must be negative. After substituting $\phi = D/2$ in (4.14) and shortening, it results:

$$\Delta s = \left(4D^2 - 3D\right)\, v_b + 4LN\, f_{sw} i_a < 0 \tag{4.16}$$

Above equation establish the maximum power that can be delivered due to hardware design restrictions and the limit established by D as shown in Chapter 2. If (4.16) is not fulfilled, L or f_{sw} should be reconsidered and D limited. If the above equations are satisfied, (4.15) and (4.16), the system will move towards the sliding mode condition: $s = 0$.

4.1.3 Ideal sliding mode dynamics in discrete-time

Once sliding surface is reached, the control action obtained in (4.6) can be substituted in (3.4) and (3.1) obtaining:

$$v_b = v_b(n+1) = v_b^* \tag{4.17}$$

which means that the surface is attained. Due to 3.1, the converter model is of first order and therefore the remaining sliding mode dynamics does not exist.

4.1.4 Chattering effect reduction

In analog sliding mode, even under steady state operation, control signal ϕ commutes at certain frequency between its maximum and minimum value. This phenomenon creates small oscillations in the sliding regulated variable which is known as chattering. Chattering, aside from electrical noise, increases electrical and mechanical component stresses. In order to solve the above problem in continuous time sliding mode, the discontinuous control function which switches between its maximum and minimum value, is replaced by a continuous smooth approximation. Detailed explanation can be found in [49]. In discrete-time, although an equivalent control action ϕ_{eq} is calculated, which should not generate chattering, it appears due to small tolerances and uncertainties in the system. Figure 4.4 illustrates this situation, where a small variation in ϕ results in excessive ripple in the bus voltage. This situation makes very difficult to reach a smooth equilibrium point.

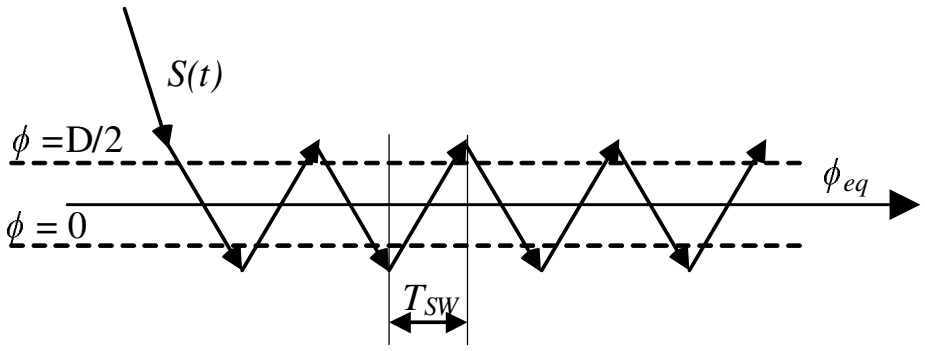


Figure 4.4: Chattering caused by high gain.

In discrete time, a smoothed control signal can be obtained by solving (3.4) for a certain moment k instead $s(n+1) = 0$. Solving for $s(n+k) = 0$.

$$\phi_{eq} = D\,(1-D) - \sqrt{(D^4 - 2D^3 + D^2) + \frac{C_b L N\, {f_{sw}}^2}{k V_{bat}} e(n) - \frac{D L N f_{sw} i_a}{V_{bat}}} \tag{4.18}$$

4.1.5 Model and control strategy validation

In this section the proposed analytical model, the circuit simulation and the experimental results are contrasted to validate the discrete-time representation and the proposed discrete-time sliding mode control for one single phase. The prototype shown in Figure 2.29 was used to obtain the experimental results. The same parameters, described in Table 4.1, were used for the analysis, simulation and experimental results.

Table 4.1: Parameters.

Parameter	Value
Switching frequency	50 kHz
Inductor	58 μH
Output capacitor	60 μF
Nominal input voltage	100 V
Nominal bus voltage	200 V
Nominal output current	1.85 A

After implementing the discrete-time sliding mode control strategy into a FPGA, the converter waveforms shown in Figure 4.5 were measured.

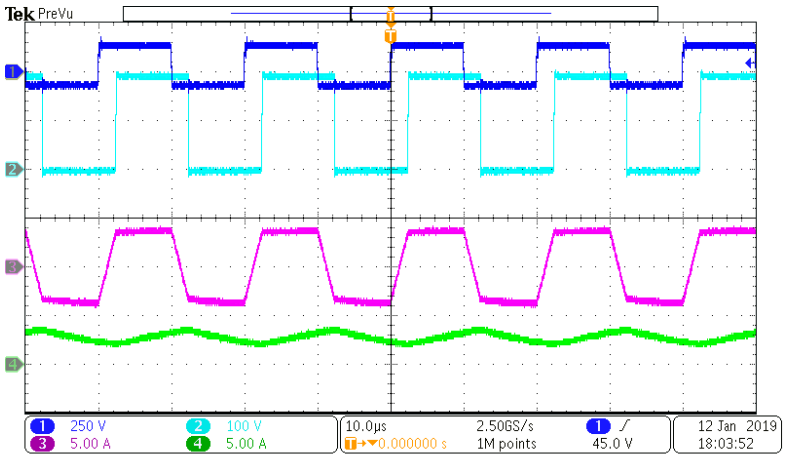
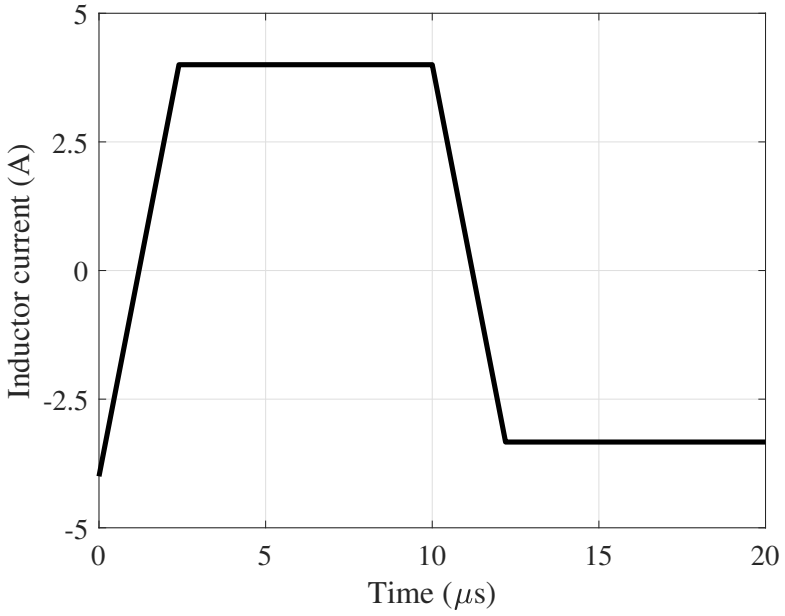


Figure 4.5: Key experimental waveforms of the combined converter. From top to bottom: Primary voltage v_p, bus voltage v_b, inductor current i_L, load current i_o.

For same operation point, inductor current waveforms acquired in (2.7) from Section 2 and simulation are plotted in Figure 4.6.



(a)

Figure 4.6: Analytically calculated inductor current i_L.

Both, analytical and simulated results match the experimental current waveform shown in Figure 4.5, where 4 A as peak current value can be observed.

Figure 4.7 represents, from (4.18), the maximum allowed voltage error at v_b before the control action saturates to its maximum $\phi = 0.25$.

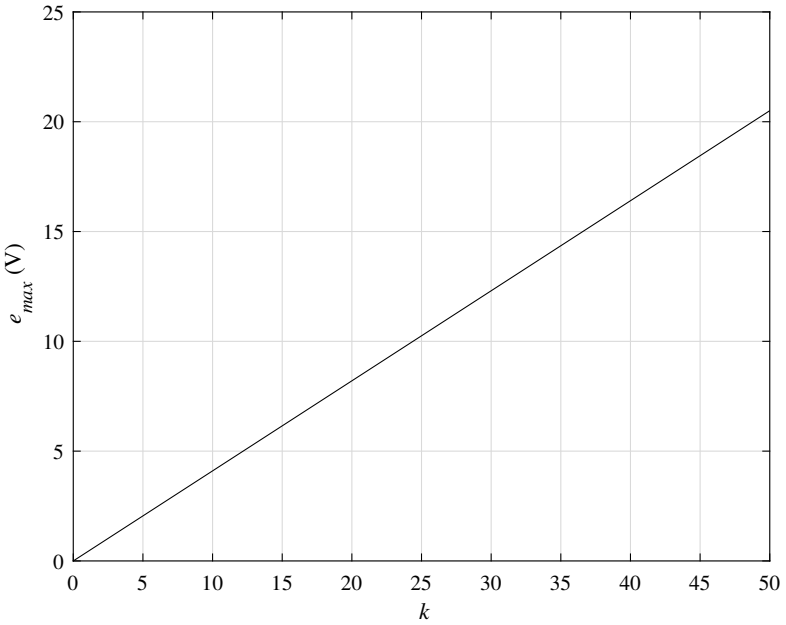


Figure 4.7: Maximum voltage error before control action saturates.

Making $k = 20$, the maximum allowed voltage error before the control saturates is around 8V, which is a reasonable value. Control action ϕ is contrasted solving for smoothed $s(n + 20) = 0$ and sharp $s(n + 1) = 0$ values. Figure 4.8 represents the comparative of the control action from 0 to 200 V and from 200 to 250 V.

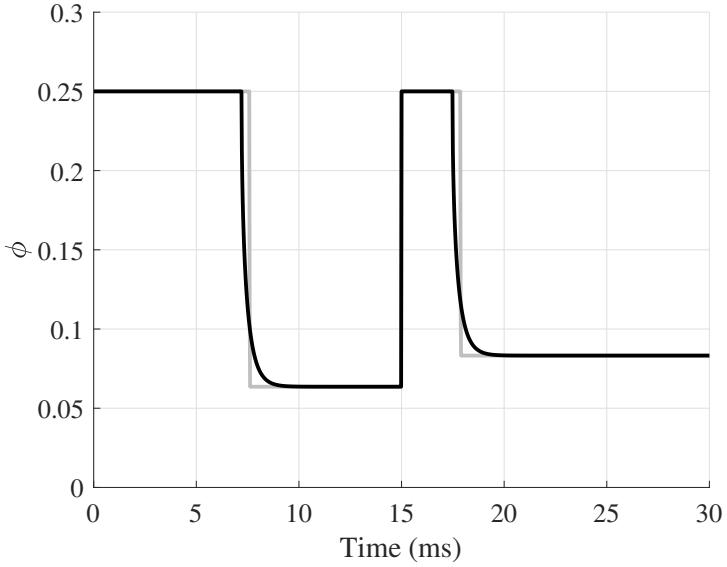
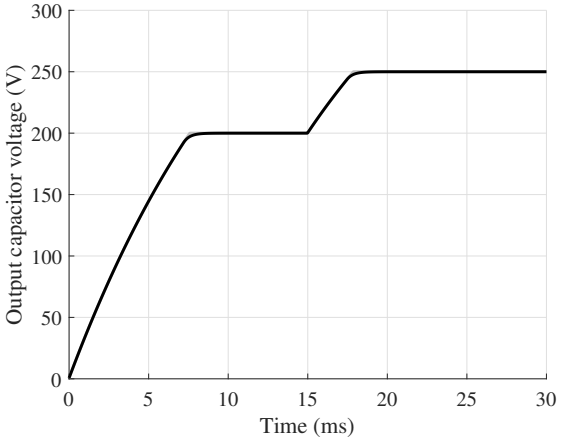
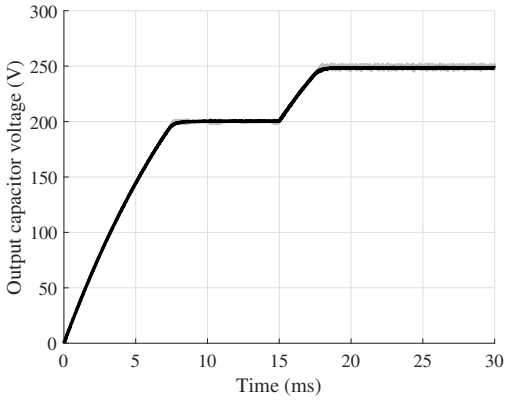


Figure 4.8: Variation of control signal ϕ for 0 to 200 and 200 to 250 voltage reference change. Black trace: Smoothed sliding regulation.

In Figure 4.8, soft transitions occur from one step to the other preventing chattering if small tolerances or uncertainties appear. The voltage evolution described by (3.4) is contrasted for previous action with simulation results in Figure 4.9. Same results are obtained, but it must be highlighted the chattering which appears in the simulation results for non smoothed action.



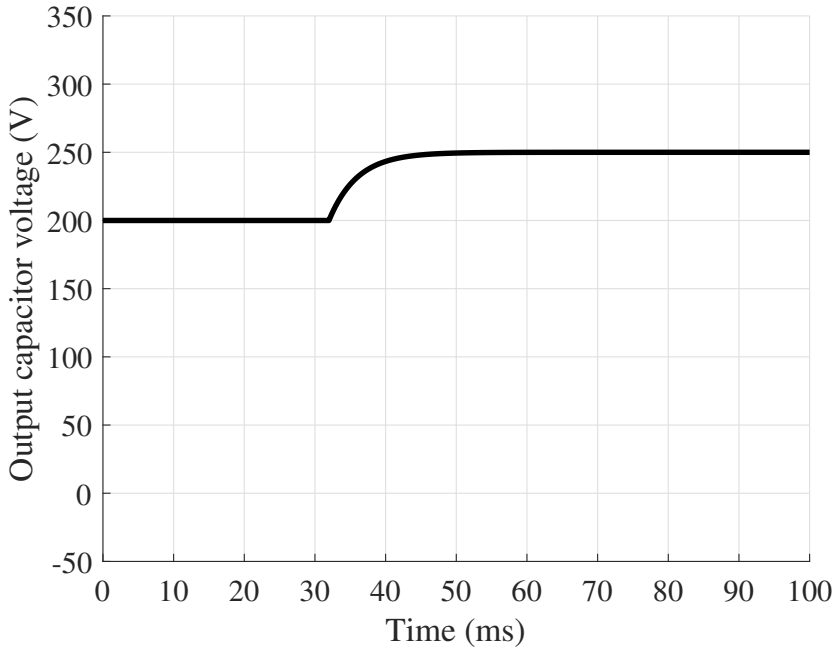
(a)



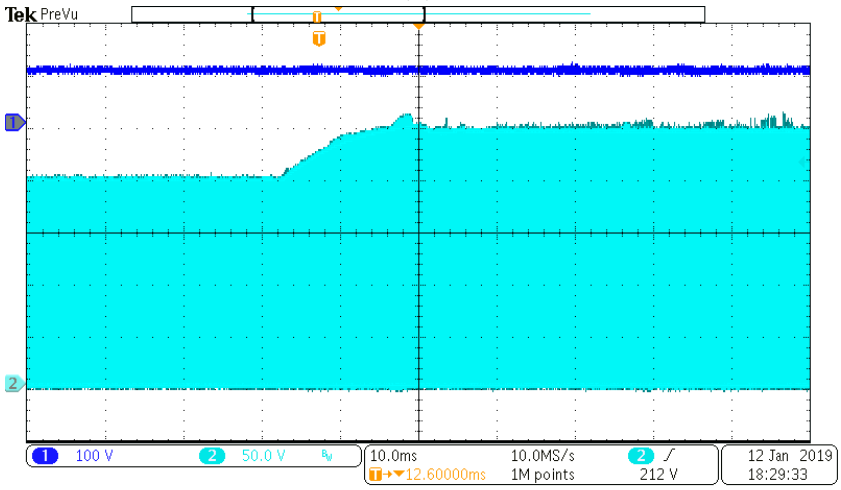
(b)

Figure 4.9: Voltage reference change. Black trace: Smoothed sliding regulation. Grey trace: common sliding regulation. (a) Analytical. (b) Simulated.

As it is shown, between $s(n+1) = 0$ and $s(n+20) = 0$ smoothed control signal has little effect on the setting time. Solving for much slower dynamics, $s(n+200) = 0$, as depicted in Figure 4.10, the control signal and the settling time are softened. In this picture, it is important to remark that the analytical model presents similar results than the experimental model.



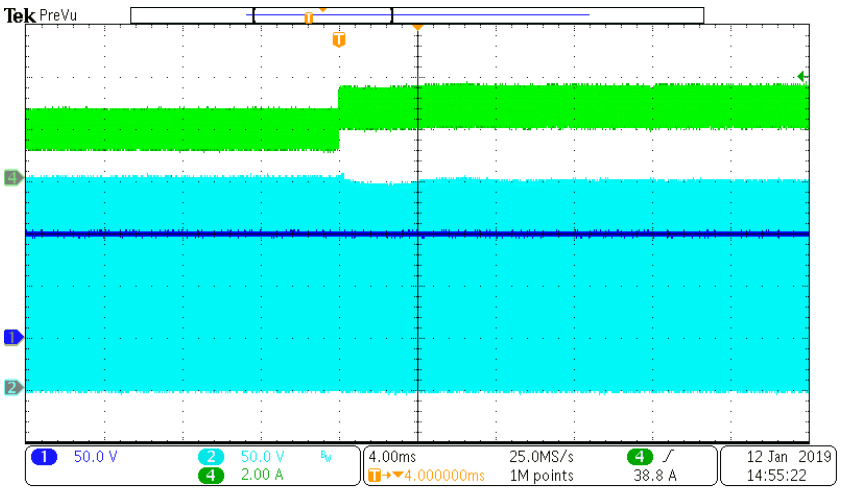
(a)



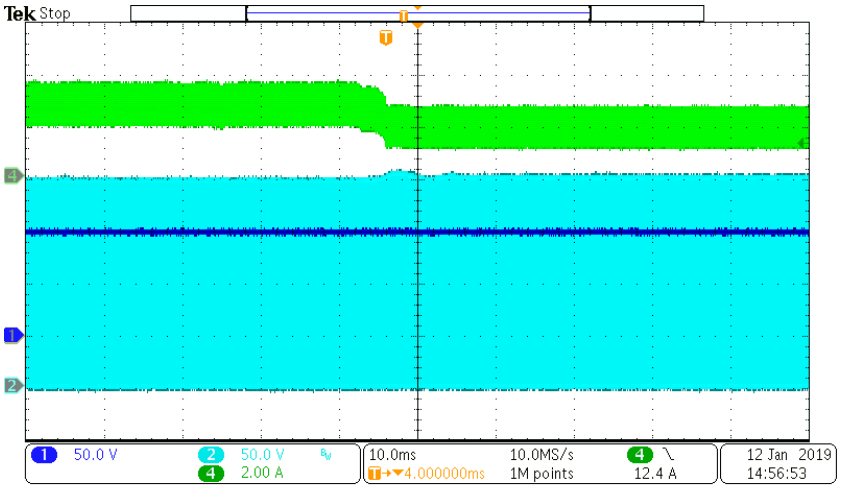
(b)

Figure 4.10: Smoothed 50 V reference change (a) Analytical. (b) Experimental. Waveforms from top to bottom: Input voltage v_i, motor voltage v_m.

Regarding the control stability when perturbations appear, Figure 4.11 depicts a load increase of 33% and decrease, turning back to its nominal conditions. Control, which is able to minimize the disturbance, shows a stable operation in both cases with little effect in bus voltage.



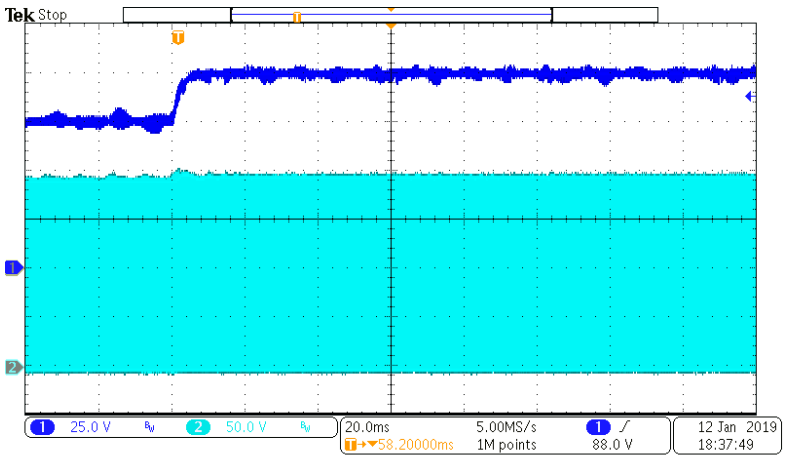
(a)



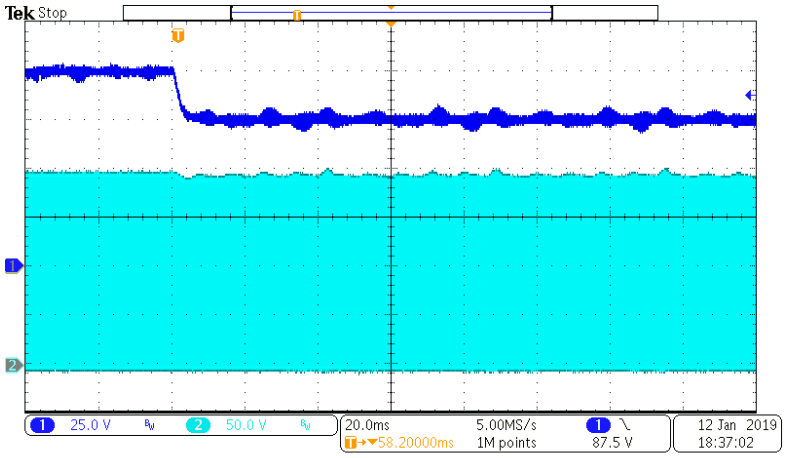
(b)

Figure 4.11: Experimental phase A motor voltage response to load variations. Waveforms from top to bottom: Output current i_o, bus voltage v_b. (a) Load increases 33%. (b) Load reduces 33%.

The reference is also maintained after applying a 25% of input voltage variation, as can be observed in Figure 4.12.



(a)



(b)

Figure 4.12: Experimental phase A motor response to input voltage variations. Waveforms from top to bottom: Input voltage v_i, bus voltage v_b. (a) Input voltage increases 25%. (b) Input voltage reduces 25%.

Looking in greater detail Figure 4.10, Figure 4.11 and Figure 4.12, it can be seen that v_b does not reach with precision v_b^* which is 200 V. This is because the implemented control, even if based on a sliding surface, employs a discrete equivalent control action making it a non-linear proportional control.

4.1.6 Parametric steady-state error elimination

It has been shown that the proportional control is able to react fastly against perturbations but it is not able to reach the reference accurately due to parametric

uncertainties. In this section, an additional integrator control loop is added to the proportional control obtained based on the equivalent control action from sliding. To do that, the phase to bus voltage small signal model of the converter at the equilibrium point is used. The control diagram is shown in Figure 4.13.

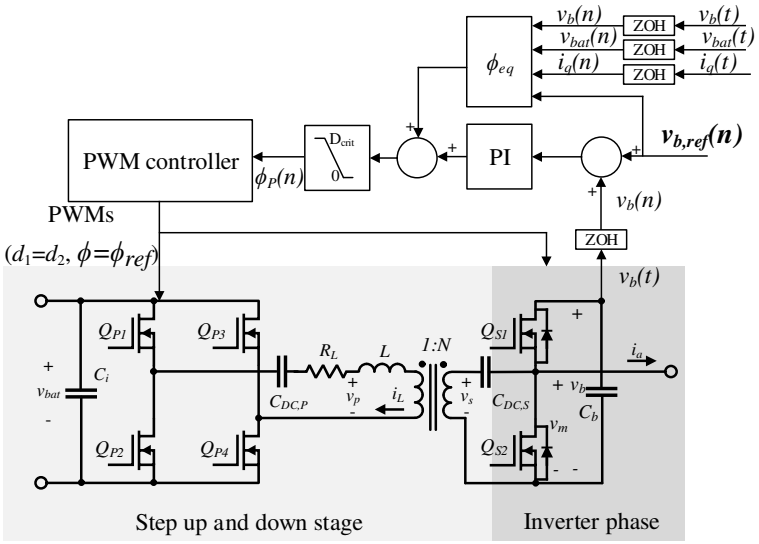


Figure 4.13: Control diagram for converter using the proportional control based on sliding and an integrator.

The PI transfer function of Figure 4.13 that must be added to the proportional action has the following form:

$$G_i(s) = \frac{1}{|G_{v\phi}(j\omega_o)|}\left(\frac{s+\omega_I}{s}\right) \tag{4.19}$$

where ω_I represents the frequency at which the integrator begins to act, 100 rad/s in that case. $|G_{v\phi}(j\omega_o)|$ is the magnitude gain of $G_{v\phi}(s)$ at crossover frequency ω_o, selected at 100 rad/s.

The PI frequency response is shown in Figure 4.14.

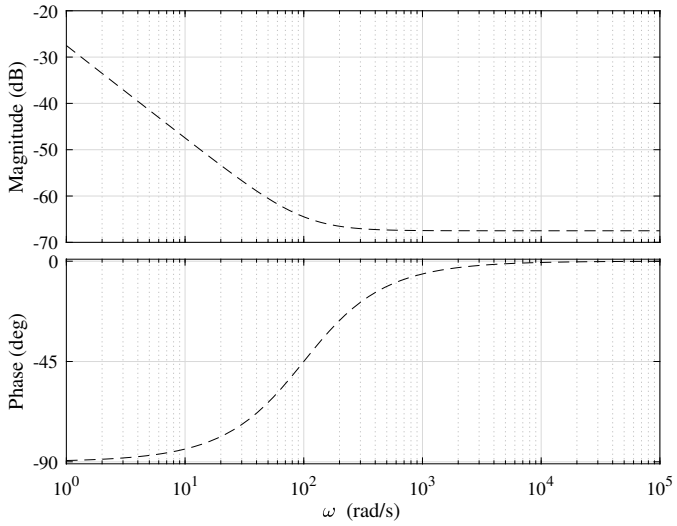


Figure 4.14: Frequency response of $G_i(s)$. Solid line: Continuous. Dashed line: Discrete.

Once the $G_i(s)$ is obtained, it is discretized using the bilinear transform which maps the left half of the complex s-plane to the unit circle in the z-plane:

$$G_i(z) = G_i(s)|_{s=\frac{2}{T_s}\frac{z-1}{z+1}} \tag{4.20}$$

where T_s is the sampling period, in that case agrees with $1/f_{sw}$.

Figure 4.15 shows how the converter is able to achieve the reference with no stationary error thanks to the inclusion of the integrator.

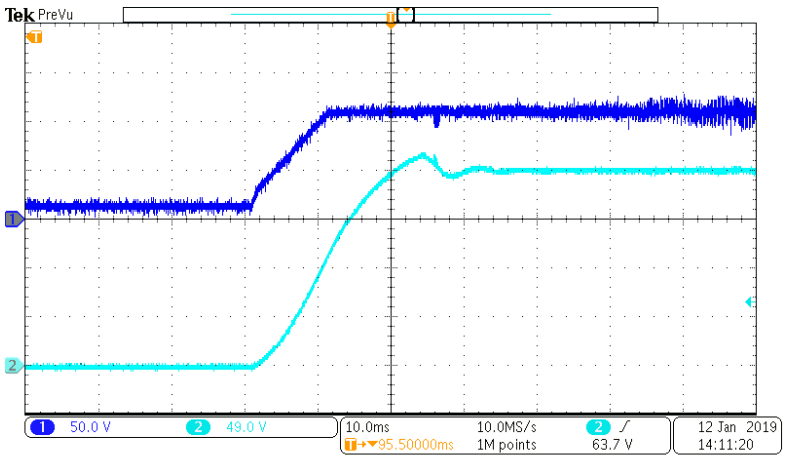


Figure 4.15: Experimental phase A motor response to input voltage variations with integrator. Waveforms from top to bottom: Input voltage v_i, bus voltage v_b.

4.2 Three phase control

For the three phase converter of Figure 2.1, as described in subsection 4.1.1 each phase can have its own control action signal operating individually:

$$\phi_P(n) = \begin{cases} 0, & \phi_{eq,P}(n) < 0 \\ \phi_{eq,P}(n) & 0 \leq \phi_{eq}(n) \leq D_{crit,P}/2 \\ D_{crit,P}/2 & \phi_{eq,P}(n) > D_{crit,P}/2 \end{cases} \tag{4.21}$$

where subindex P represents each phase. $\phi_{eq,P}(n)$ can be obtained from (4.6). In that case, one phase will be always operating close to its maximum power delivery point, $D = 0.5$ while the others will be in worse points.

Another interesting option to simplify calculations is to use an equivalent control action signal common to all phases:

$$\phi(n) = \begin{cases} 0, & \phi_{eq,P}(n) < 0 \\ \phi_{eq}(n) & 0 \leq \phi_{eq}(n) \leq D_{crit,P}/2 \\ D_{crit,P}/2 & \phi_{eq,P}(n) > D_{crit,P}/2 \end{cases} \tag{4.22}$$

It must be denoted that the saturation of each phase must be done individually to take advantage of the maximum power that each one can provide.

Following the process described in Section 4.1.1, the equivalent control action common to all phases can be calculated. Using (3.9) instead (3.4), the three phase common equivalent control action can be obtained:

$$\phi_{eq,3ph} = -\frac{\sqrt{3}\sqrt{v_{bat}}\sqrt{3v_{bat} - 64C_oLN\,{f_{sw}}^2 e(n) - 48LN\,f_{sw} i_m} - 3v_{bat}}{48v_{bat}} \tag{4.23}$$

The control loop of Figure 4.16 is implemented in the microcontroller of the low power prototype shown in Figure 2.39.

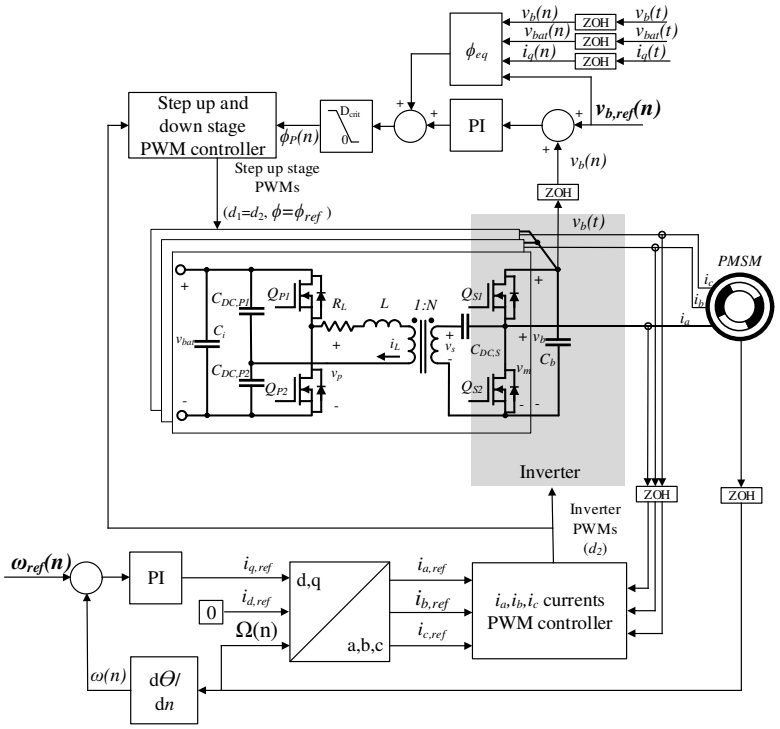


Figure 4.16: Control diagram of combined converter and PMSM using the proportional control based on sliding and an integrator.

The control loop is implemented in a C2000 microcontroller and incorporates a proportional gain using the discrete time approach and a conventional integrator to remove the error at steady state. Figure 4.17 shows the voltage variation with a sudden change in current due to an increase in torque. Despite the 33% rise of the torque, the sliding-based proportional control acts quickly while maintaining the bus voltage while the added PI control action contributes to eliminate the stationary error.

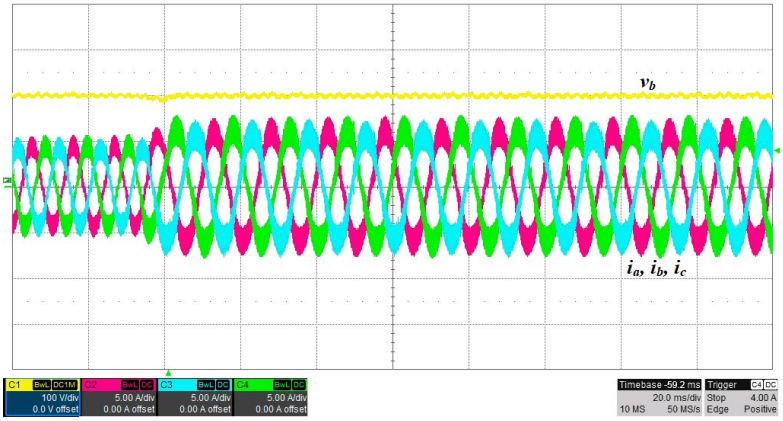


Figure 4.17: Measured combined converter and PMSM main voltage and current waveforms after a torque perturbation of 33 %. The PMSM operates at 1000 rpm, absorbing 300 W and v_{bat}=100 V. Bus voltage v_b (100 V/div) and the phase currents flowing to the motor: i_a, i_b and i_c (5 A/div).

4.3 Conclusions

This Chapter presents bus voltage regulation of the converter detailed in Chapter 2 by varying the phase. A direct digital proportional control has been realized using the discrete time model of Chapter 3 and employing sliding design procedures. To cope with the stationary error, a slow digital PI loop is added and tuned using the redisign approach strategy. Both controls were validated experimentally showing a good rejection against disturbances at input battery and loads changes.

Chapter 5

Efficiency optimization

In Chapter 4, variable ϕ is used to control the bus voltage, but as shown in (2.20) other variables can regulate the output power and hence v_b. In this Chapter, f_{sw} regulates the output voltage and a second slower control loop which varies ϕ is added to find the point of maximum efficiency. Since this chapter presents an optimization, the proposal has not been proved using a three phase converter with a PMSM as load. Instead, it has been validated with a dual active bridge converter, shown in Figure 5.1 and re-configuring the prototype in Figure 2.35. The main difference is that the energy required by the load is absorbed directly from the bus capacitor and not from the mid point of the inverter.

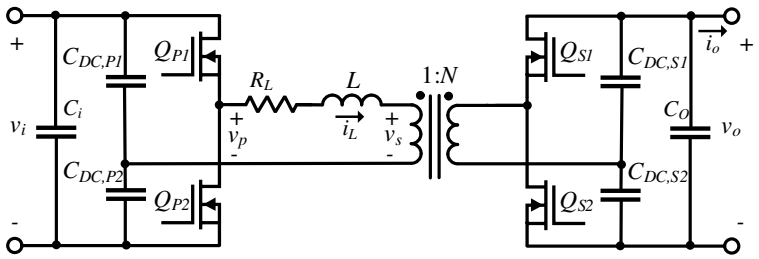


Figure 5.1: Dual active bridge schematic.

5.1 Digital controller design and experimental verification

This section develops a digital control based on the transfer function obtained from the procedure of Chapter 4. Substituting the parameters of Table 5.1 in (3.71) and dividing the gain by two due to the difference between full-bridge and half-bridge, the following transfer function is obtained:

Table 5.1: DAB Equilibrium point parameters.

Parameter	Value
v_{in}	200 V
v_o	200 V
ϕ	0.1
d_1	0.5
d_2	0.5
f_{sw}	45 kHz
N	1
L	20 μH
R_L	240 mΩ
C_o	150 μF
R_{load}	40 Ω

$$G_{vf_{sw}}(s) = \frac{72015(s - 8.069 \times 10^5)}{(s + 166.5)(s^2 + 5.136s + 8.171 \times 10^{10})} \tag{5.1}$$

It is important to remark that, due the calculation of the First Fourier harmonic for obtaining the DAB model, equation (5.1) presents high-frequency modelling effects in form of resonance and non minimum phase dynamics. The high frequency resonance is placed at the switching frequency and the right half plane zero represents the delay in power output transmission, which is related to d_2T_{sw} plus ϕ. However, these high frequency effects are far away of the useful frequency range of a small-signal model, which is below a half of the switching frequency, and usually are not taken into account for control purposes. The obtained transfer function is represented in the Bode diagram of Figure 5.2. In this Figure, it is also possible to observe a perfect agreement between the frequency representation of the obtained analytical model and the obtained by simulation using Matlab/Simulink.

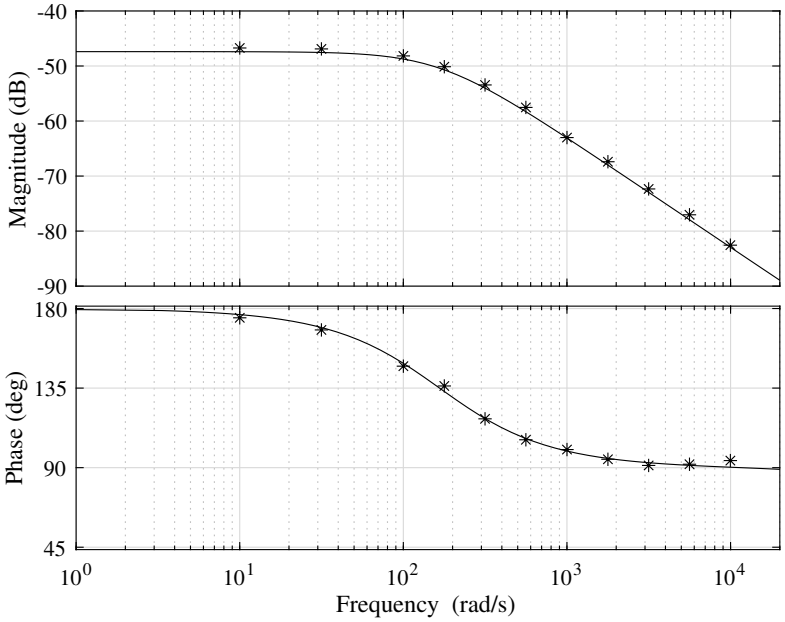


Figure 5.2: Frequency response of $G_{vf_{sw}}(s)$. Solid line: Analytical model results. Asterisks: Simulation.

5.1.1 Controller design

A design based on digital redesign is proposed, where a continuous controller is initially designed and then discretized. Since the controller is discrete-time, a delay t_d occurs between the sampling instant and the update of the control action. This delay is represented by the transfer function:

$$G_{del}(s) = e^{-t_d s} \tag{5.2}$$

So, the new continuous plant with the included delay results in:

$$G_{vf_{sw},del}(s) = G_{vf_{sw}}(s)G_{del}(s) \tag{5.3}$$

A PI controller to ensure output voltage regulation and zero steady-state error is proposed as follows:

$$Gc(s) = \frac{-1}{|G_{vf_{sw},del}(j\omega_o)|}(\frac{s+\omega_I}{s}) \tag{5.4}$$

A simple design process of this PI is done choosing the crossover frequency ω_o regarding the desired Phase Margin, setting ω_I one decade below ω_o and adding the gain needed to ensure loop gain 0 dB crossing at ω_o. This is done dividing by $|G_{vf_{sw},del}(j\omega_o)|$ that represents the magnitude gain of (5.3) at ω_o. Once the $G_c(s)$

is obtained, it can be discretized using the bilinear transform which maps the left half of the complex s-plane to the unit circle in the z-plane:

$$Gc(z) = Gc(s)|_{s=\frac{2}{T_s}\frac{z-1}{z+1}} \tag{5.5}$$

where T_s is the sampling period.

5.1.2 Simulation and experimental results

In order to show the model utility, a digital PI controller is designed following the procedure described in Section 5.1.1. A loop gain crossover frequency of 1000 rad/s its sufficiently below of the minimum switching frequency and gives a conservative Phase Margin value around 90°. As explained in Section 5.1.1, the zero of the PI is placed one decade below the crossover frequency, i.e. ω_I= 100 rad/s. The gain of the controller is adjusted to achieve 0 dB loop gain crossing at ω_o= 1000 rad/s, thus giving $1/|G_{vf_{sw},del}(j\omega_o)|$=63 dB, as can be seen in Figure 5.3.

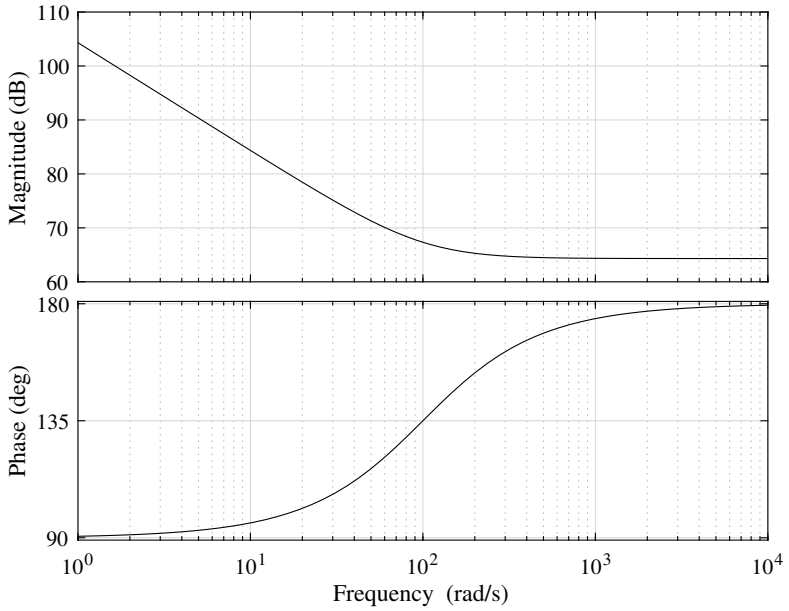


Figure 5.3: Frequency response of $G_c(s)$.

Table 5.2: Controller parameters.

Parameter	Value
ω_c	1000
ω_I	100
t_d	33.33μs
T_s	6.67μs

The open loop gain, $G_{ol}(s)$ of the system, defined as

$$G_{ol}(s) = G_c(s)G_{v,f_{sw}}(s)G_{del}(s) \tag{5.6}$$

is represented in Figure 5.4 using the parameters of Table 5.2.

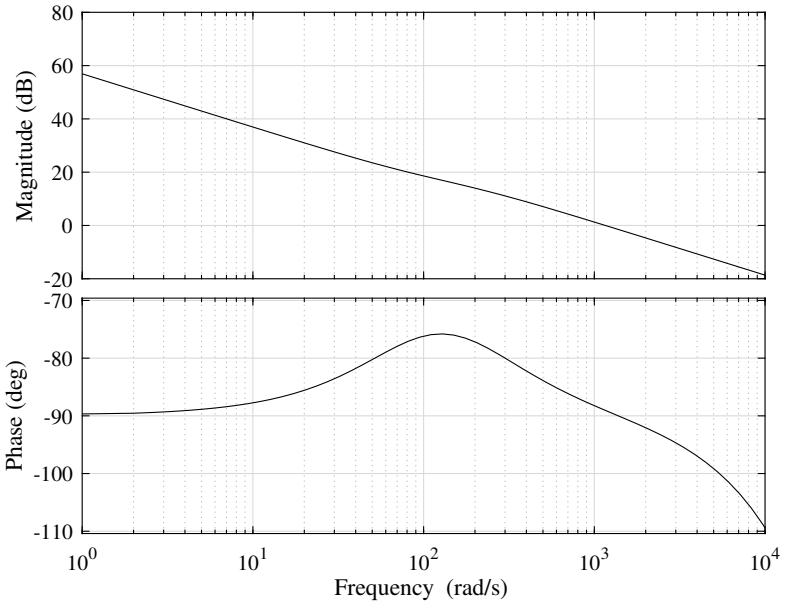


Figure 5.4: Frequency response of converter gain loop.

From Figure 5.4, it can be seen than the phase margin is around 90° ensuring the stability of the system.

The continuous controller is discretized using the Bilinear transformation with a sample time T_s, that ensures that all the poles are located inside the unit circle of the z-plane. The discretized controller, $G_c(z)$ is implemented in the prototype shown in Figure 5.5, which is based on Table 3.1 and is based on the reconfiguration of the prototype of Chapter 2. Selected semiconductors are STW70N60DM2 and

the magnetic components are made of ferrite N87. The control is implemented in a FPGA from the Artix-7 family.

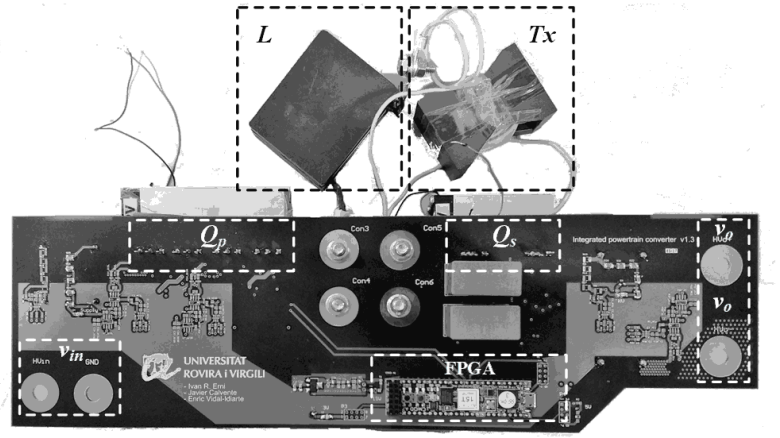
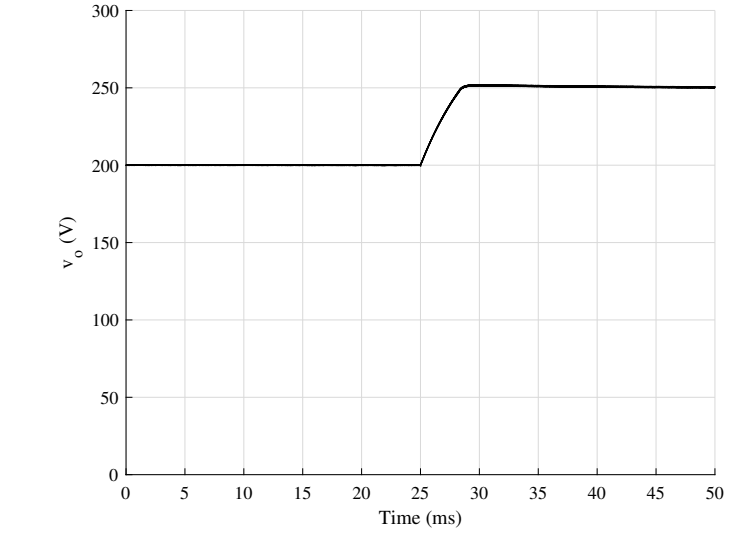
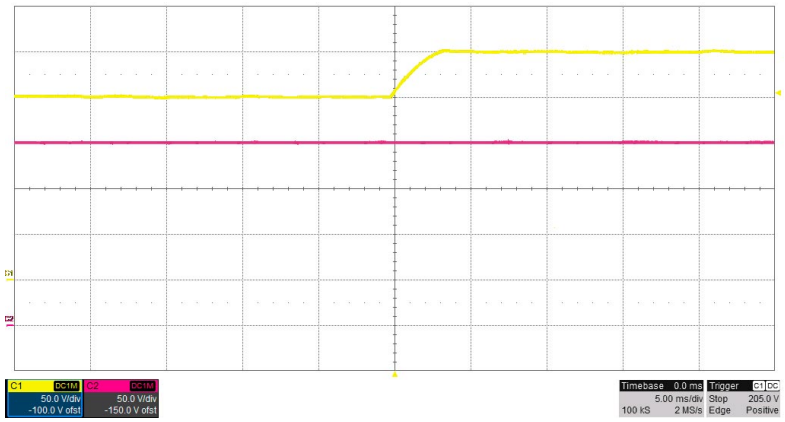


Figure 5.5: Converter prototype.

Figure 5.6 compares the response obtained by simulation with the experimental response to a 25% increase in the output voltage reference. Experimental and simulation transient behaviors agree and show the system is able to reach the new set point with zero stationary error.



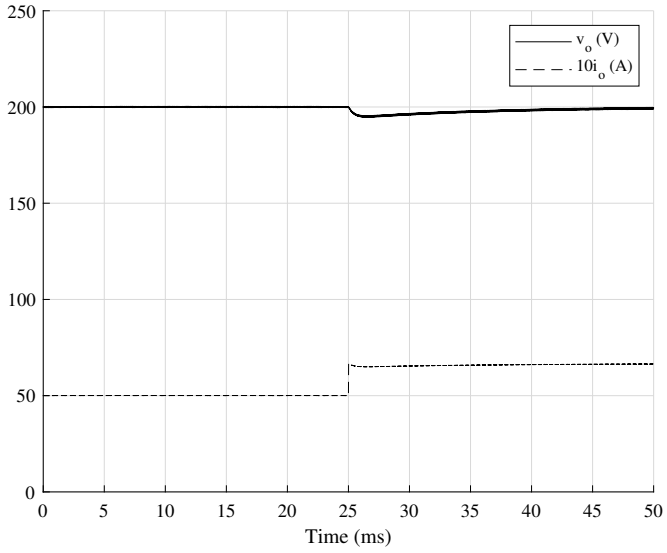
(a)



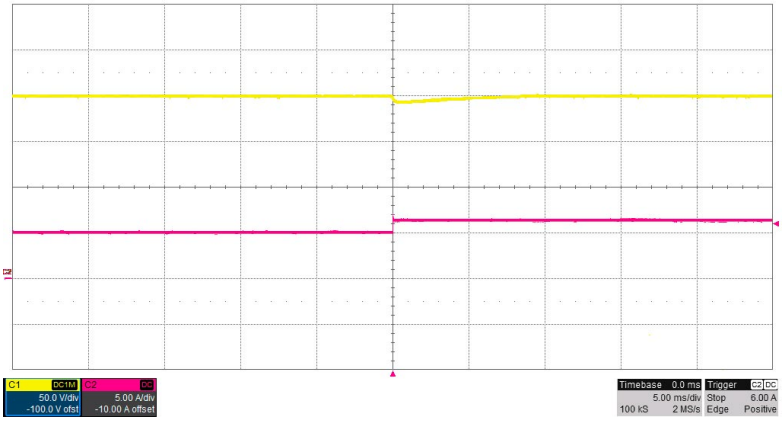
(b)

Figure 5.6: Voltage reference variation. (a) Simulated. (b)Experimental. From top to bottom: Output voltage v_o (50 V/div) and input voltage v_i (50 V/div). Timescale (5 ms/div).

Experimental and simulated time responses for 25% of load perturbation are presented respectively in Figure 5.7. Both experimental and simulation transient behavior agree again, showing the system is able to recover again its zero output voltage error stationary state, validating the theoretical predictions and the feasibility of the controller.



(a)



(b)

Figure 5.7: Output voltage response to load perturbation of 25%. (a) Simulated- (b) Experimental. From top to bottom: Output voltage v_o (50 V/div) and output current i_o (5 A/div). Timescale (5 ms/div).

Similarly, Figure 5.8 shows how the regulator presented in the previous subsection is able to maintain the output voltage in the presence of a 25 % variation in the converter input voltage.

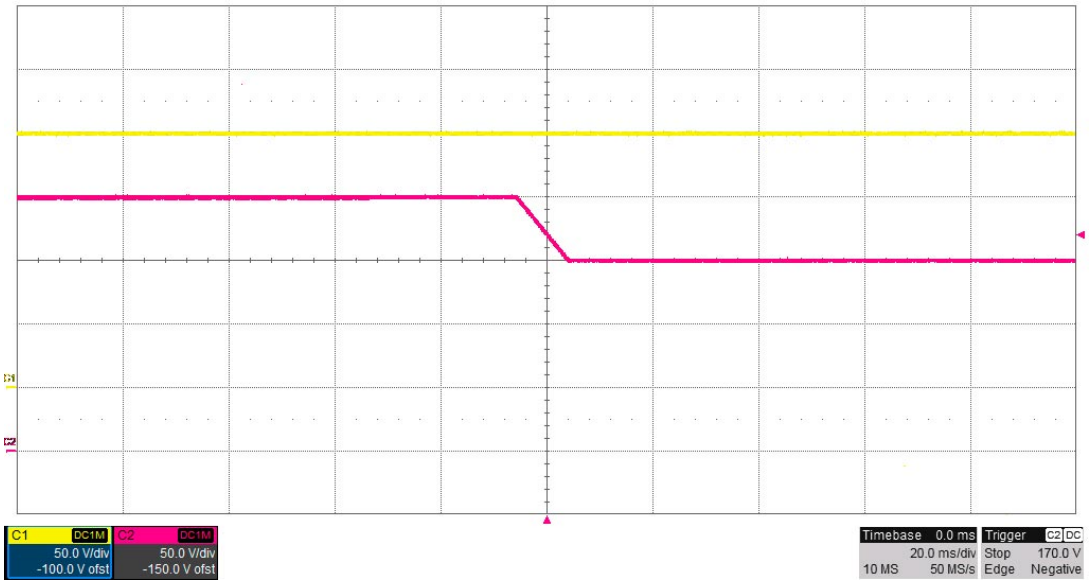


Figure 5.8: Output voltage response to iput voltage perturbation of 25%. From top to bottom: Output voltage v_o (50 V/div) and input voltage v_i (50 V/div). Timescale (20 ms/div).

5.2 Maximum efficiency point tracking

As it has been seen, when varying the switching frequency using the controller designed in previous section, it is possible to regulate the output variable relatively quickly in front of load disturbances and reference changes. This leaves free the control variable most commonly used in this topology, the phase shift ϕ. This variable could be left fixed at a value that guarantees the full range of operation, but taking advantage of this additional degree of freedom, the aim is to improve the efficiency of the converter.

5.2.1 Converter losses and control motivation

Previous works [50, 51] describe how the conduction loss is dominant in the total power loss, which implies that the overall system efficiency can be improved reducing the RMS value of $i_L(t)$ or the input current $i_{in}(t)$. Thus, the minimization of $I_{in,rms}$ can be adopted as the optimization objective. Consequently, the reactive input current is reduced. It is important to note, that switching looses are less dominant since ZVS exists during turn on, while at turn off, they are compensated by a lower switching current. The inductor current analysis of Chapter 2 is valid

if (2.2), (2.3),(2.4) and (2.5) are substituted by:

$$m_{iL,1} = \frac{d_2 v_o + (1-d_1)\, N\, v_i}{LN} \tag{5.7}$$

$$m_{iL,2} = \frac{(d_2-1)\, v_o + (1-1d_1)\, N\, v_i}{LN} \tag{5.8}$$

$$m_{iL,3} = \frac{-(1-d_2)\, v_o/N - d_1 v_i}{L} \tag{5.9}$$

$$m_{iL,4} = \frac{d_2 v_o/N - d_1 v_i}{L} \tag{5.10}$$

In such way, the voltage gain is now adapted to a half-bridge.

Once inductor current slope is obtained, instant inductor current $i_L(t)$ can be determined as the initial current $i_L(nT_{sw})$ plus the increment $\Delta i_L(\tau)$:

$$i_L(t) = i_L(nT_{sw}) + \Delta i_L(\tau) \tag{5.11}$$

$$\Delta i_L(\tau) = \begin{cases} \Delta i_{L,1}(\tau) & 0 < \tau \leq \phi T_{sw} \\ \Delta i_{L,2}(\tau) & \phi T_{sw} < \tau \leq d_1 T_{sw} \\ \Delta i_{L,3}(\tau) & d_1 T_{sw} < \tau \leq (d_2+\phi) T_{sw} \\ \Delta i_{L,4}(\tau) & (d_2+\phi) T_{sw} < \tau \leq T_{sw} \end{cases} \tag{5.12}$$

where

$$\Delta i_{L,1}(\tau) = m_{iL,1}\tau \tag{5.13}$$

$$\Delta i_{L,2}(\tau) = m_{iL,1}\phi T_{sw} + m_{iL,2}(\tau - \phi T_{sw}) \tag{5.14}$$

$$\Delta i_{L,3}(\tau) = m_{iL,1}\phi T_{sw} + m_{iL,2}(d_1-\phi)T_{sw} + \\ + m_{iL,3}(\tau - d_1 T_{sw}) \tag{5.15}$$

$$\Delta i_{L,4}(\tau) = m_{iL,1}\phi T_{sw} + m_{iL,2}(d_1-\phi)T_{sw} + \\ + m_{iL,3}(d_2+\phi-d_1)T_{sw} + m_{iL,4}(\tau - (\phi+d_2)T_{sw}) \tag{5.16}$$

As , the value that makes the average current equal to zero corresponds to $i_L(nT_{sw})$ during each switching period: With $i_L(t)$ calculated, the input effective current can be obtained as:

$$I_{in,rms} = \left(\frac{1}{T_{sw}} \int_{d1T_{sw}}^{T_{sw}} i_L(\tau)^2 \, \mathrm{d}\tau \right)^{1/2} \tag{5.17}$$

which by solving the equation and substituting d_1 and d_2 by 0.5, results in:

$$I_{in,rms} = \frac{\sqrt{{v_o}^2 + \left(-64n\,\phi^3 + 48N\,\phi^2 - 2n\right)\,v_b v_o + N^2\,{v_i}^2}}{8\sqrt{6}L\;|f_{sw}|\,|n|} \tag{5.18}$$

Input power P_i can be calculated as the current flowing through the inductor multiplied by the applied input voltage at the first inductor terminal:

$$\langle P_i \rangle_{T_{sw}} = \frac{1}{T_{sw}} \int_0^{T_{sw}} v_p(t) i_L(t)\;\mathrm{d}t = \frac{1}{T_{sw}}\left(E_1 + E_2 + E_3 + E_4\right) \tag{5.19}$$

where

$$E_1 = \int_0^{\phi T_{sw}} v_i(1-d_1) i_L(\tau))\;\mathrm{d}\tau \tag{5.20}$$

$$E_2 = \int_{\phi T_{sw}}^{d_1 T_{sw}} v_i(1-d_1) i_L(\tau)\;\mathrm{d}\tau \tag{5.21}$$

$$E_3 = \int_{d_1 T_{sw}}^{d_2+\phi T_{sw}} -v_i d_1 i_L(\tau)\;\mathrm{d}\tau \tag{5.22}$$

$$E_4 = \int_{d_2+\phi T_{sw}}^{T_{sw}} -v_i d_1 i_L(\tau)\;\mathrm{d}\tau \tag{5.23}$$

Assuming high efficiency, the output power P_o equals P_i and equating d_1 to d_2:

$$\langle P_o \rangle_{T_{sw}} = \frac{\left(-\phi^2 + \left(-2d^2 + 2d\right)\phi\right)\,v_i v_o}{L\,f_{sw} N} \tag{5.24}$$

By solving for the variable f_{sw} in the previous function and substituting in (5.18), $I_{in,rms}$ can be rewritten as:

$$I_{in,rms} = \frac{|P_o|\;\sqrt{{v_o}^2 + \left(-64\phi^3 + 48\phi^2 - 2\right)\,v_i v_o + {v_i}^2}}{2\sqrt{6}\;|2\phi^2 - \phi|\;v_i v_o} \tag{5.25}$$

Using the parameters of Table 3.1 in equation (5.25), Figure 5.9 is obtained.

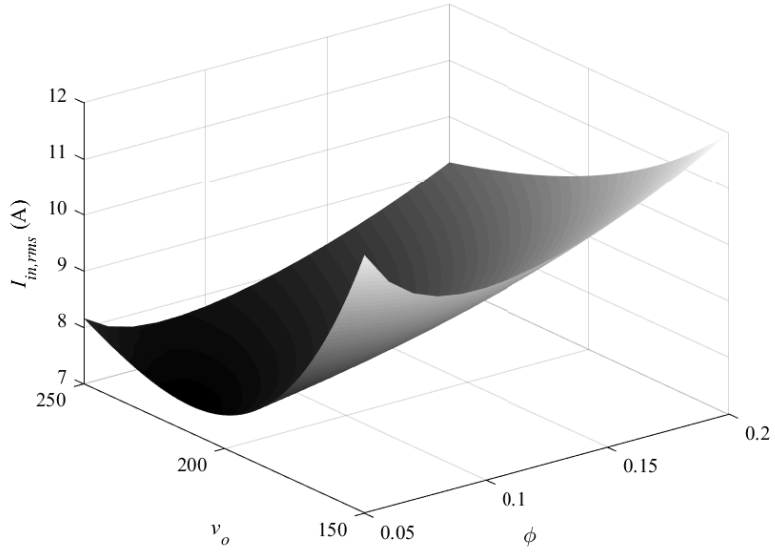


Figure 5.9: $I_{in,rms}$ variation depending on v_o and ϕ.

It can be seen that for the same P_o, the effective input-current can increased or reduced depending on v_o and ϕ. While v_o is tightly regulated to achieve the voltage reference setting, ϕ can be modified to reduce the effective input current.

By making three cuts at different voltages in Figure 5.9, Figure 5.10 is obtained, where the existence of an optimum ϕ value for each voltage that reduces the effective current in the system can be seen in more detail.

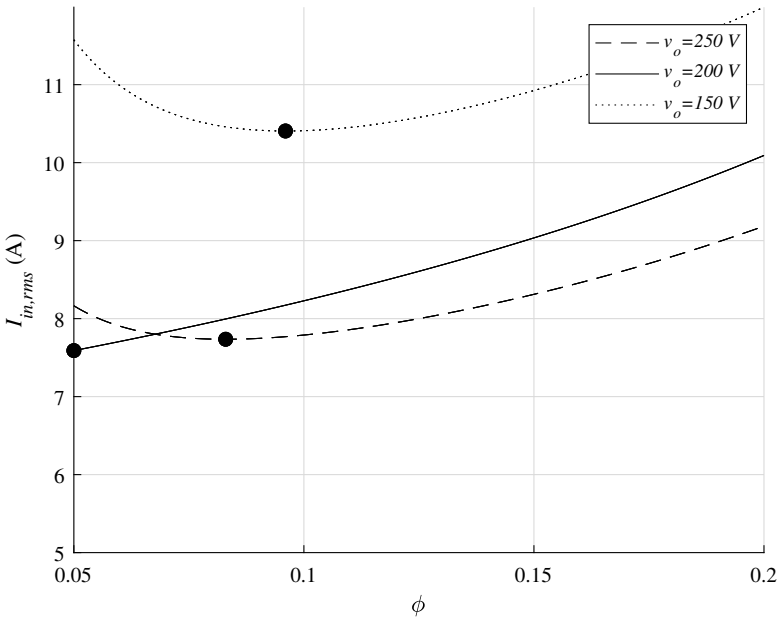


Figure 5.10: Detail of $I_{in,rms}$ variation.

It is important to note that when $v_i = Nv_o$, the optimum ϕ value would be almost zero and switching frequency to maintain P_o results too low. This would imply the use of large volume magnetic components and the loss of ZVS. For this reason, a minimum switching frequency, $f_{sw,min}$ must always be considered, which is also translated into a minimum phase shift, preventing the magnets from saturating due to excess current and ensuring ZVS.

5.2.2 Maximum efficiency point tracking strategy control loop

As demonstrated in previous subsection, the efficiency of the topology can be improved reducing $I_{in,rms}$ by varying ϕ. Finding the optimal ϕ value would involve solving the derivative of ϕ and equating to 0 in equation (5.25), which results in an equation that is difficult to implement. A possible solution would be to use a look up table, but due to component tolerances, switching losses and variations caused by thermal effects, the actual instantaneous optimum point would not be reached. To simplify and ease the computational cost and hardware required to perform the measurement, taking into account the analysis of Section 5.2.1 and the relationship:

$$I_{in} = \frac{P_o + I_{in,rms}^2 R_{loss}}{V_i} \tag{5.26}$$

where capital letters represent the average values and R_{loss} the overall loss resistor, the following method is proposed. The maximum efficiency point tracking (MEPT) intends to establish a secondary control loop that slowly varies ϕ to find the optimum operating point of the converter by reducing the averaged current consumed at the input I_{in} and ensure ZVS while maintaining the power delivered at the output. In other words, modify ϕ to minimize equations (5.25) and (5.26). For this aim, it is proposed to use the Perturb and Observe method, a widely known technique that has proven its effectiveness in the solar energy sector and improved in [52, 53]. In this technique, a small perturbation is applied to provoke the input power variation. With a given period, the phase shift is modified and the evolution of the current at the input is observed. At the end of the cycle, if the filtered input current I_{in} is lower, ϕ is varied again in the same direction. Conversely, if I_{in} is higher than in the previous cycle, ϕ is varied in the opposite direction in this cycle. Consequently, the RMS current will evolve to the corresponding minimum current point, marked with a black point Figure 5.10. It is important to note that when there is a change in ϕ, f_{sw} varies to maintain regulation at the output. A large ϕ step is a large perturbation that the regulator must correct varying ϕ which may create oscillations in v_o. Therefore, the increase or decrease in the phase shift step should not be too high to maintain v_o without ripple. By solving for f_{sw} and linearising (5.24), the variation of f_{sw} as a function of ϕ is obtained:

$$\hat{f}_{sw} = \frac{\left(D_1 - {D_1}^2 - \theta\right) V_b V_o}{L\, P_o N} \hat{\phi} \tag{5.27}$$

Using (5.27), it is possible to know how much f_{sw} will vary with a small change ϕ. In addition, this control is in charge of maintaining the ZVS operation and ensure that the operation point is able to deliver the required output power, so ϕ should never be less than a certain value, ϕ_{min}. It is important to maintain the ZVS condition to prevent switching losses from increasing significantly. To guarantee ZVS in all semiconductors, the anti-parallel diode must conduct and discharge the MOSFET capacities before it turns on:

$$i(t = T_{sw}) < -I_{min} \tag{5.28a}$$

$$i(t = (\phi + d_2)T_{sw}) < -I_{min} \tag{5.28b}$$

$$i(t = d_1 T_{sw}) > I_{min} \tag{5.28c}$$

$$i(t = \phi T_{sw}) > I_{min} \tag{5.28d}$$

I_{min} represents the minimum required current to discharge the parallel capacitance of the switching devices. Detailed information about ZVS capacitances discharge

can be found in [32]. Rewriting (5.28) and substituting (5.24), it is obtained:

$$\phi_{min} > \begin{cases} -\frac{Nv_{in}-v_o+8I_{min}LNf_{sw}}{4v_o} \\ \frac{Nv_{in}-v_o-8I_{min}LNf_{sw}}{4Nv_{in}} \\ -\frac{Nv_{in}-v_o-8I_{min}LNf_{sw}}{4v_o} \\ \frac{Nv_{in}-v_o+8I_{min}LNf_{sw}}{4Nv_{in}} \\ \frac{\sqrt{v_i}\sqrt{v_o}\sqrt{v_iv_o-32L\,P_o\,f_{sw,min}n}+v_iv_o}{4v_iv_o} \end{cases} \tag{5.29}$$

where $f_{sw,min}$ is the minimum allowed switching frequency of the converter. The maximum value of ϕ from equation (5.29) must be selected as the low saturation limit, ϕ_{min} to ensure ZVS in all transistors. The control steps described above are summarized in the flow diagram in Figure 5.11.

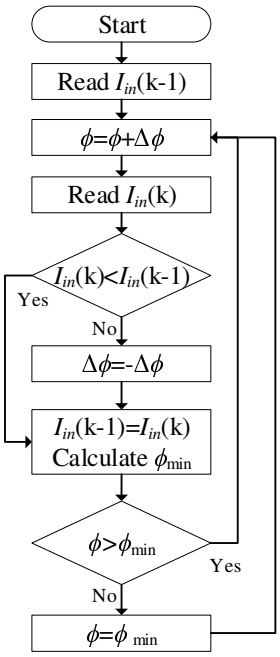


Figure 5.11: Maximum efficiency point tracking control flowchart.

5.2.3 Experimental MEPT validation

Figure 5.12 shows how once the equilibrium point is reached, the phase control starts to act and reduces the input current by about 15%.

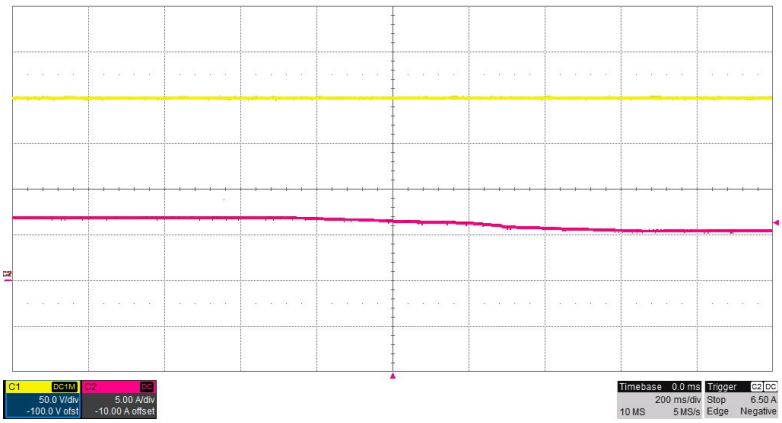


Figure 5.12: Effect of maximum efficiency point tracking control on i_i.From top to bottom: Output voltage v_o (50 V/div) and input current i_i (5 A/div). Timescale (200 ms/div).

Once the optimum point in Figure 5.12 has been reached, the converter waveforms can be seen in more detail in Figure5.13. In it, it can be observed that the stage operates in ZVS fulfilling equation (5.28). It is also important to note that the final phase shift match the expected value in Figure 5.10, since ϕ is at the minimum allowed value given by (5.29), 0.056 for $f_{sw,min}$=25 kHz. Similarly occurs when v_o=250 V as shown in Figure5.14. Equation (5.28) is also fulfilled, ensuring ZVS and ϕ results 0.085, matching with the optimum value obtained in Figure 5.10.

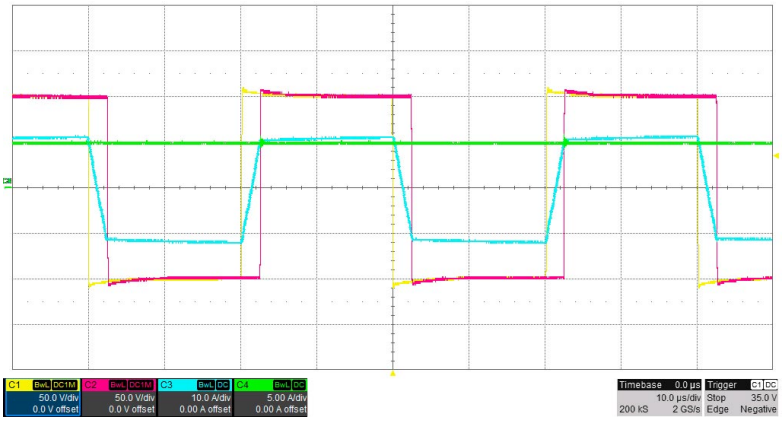


Figure 5.13: Measured converter main waveforms: P_o=1 kW, v_i=200 V, v_o=200 V. Yellow trace: Primary side voltage v_p (50 V/div). Magenta trace: Secondary side voltage v_s (50 V/div). Blue trace: Inductor current i_L (10 A/div). Green trace: Output current i_o (5 A/div). Timescale (10 μs/div).

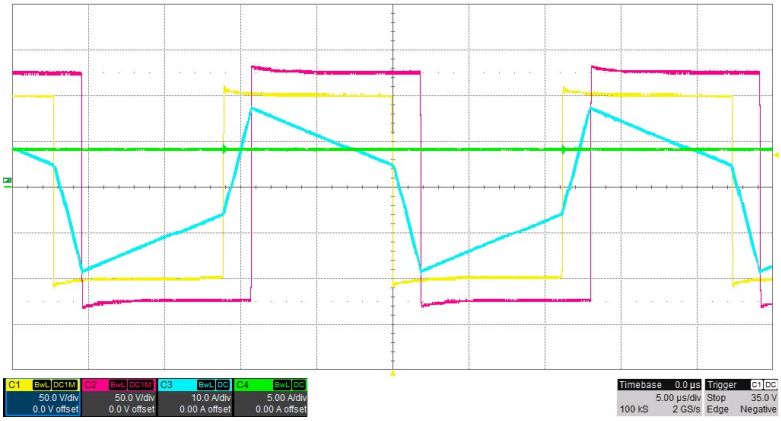


Figure 5.14: Measured converter main waveforms: P_o=1 kW, v_i=200 V, v_o=250 V. Yellow trace: Primary side voltage v_p (50 V/div). Magenta trace: Secondary side voltage v_s (50 V/div). Blue trace: Inductor current i_L (10 A/div). Green trace: Output current i_o (5 A/div). Timescale (5 μs/div).

Figure 5.15 compares the efficiency between the conventional phase shift method and the proposed one at different input voltage levels. The improvement in efficiency is most noticeable as the stage moves away from its optimum operating point, for example an output voltage of 200 V. At the optimum voltage ratio, the proposed control presents a significant improvement over the conventional one at high currents.

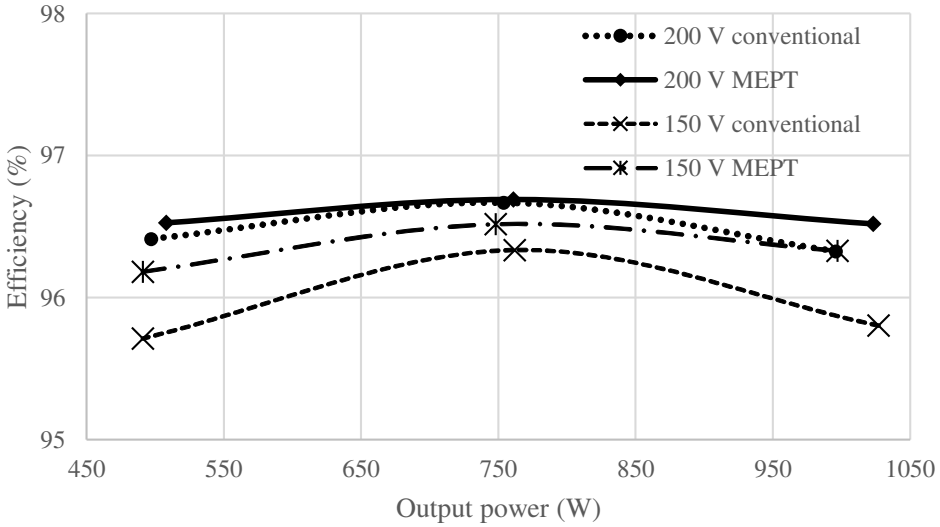


Figure 5.15: Efficiency comparative of the conventional ϕ control and the proposed MEPT control.

5.3 Conclusions

Chapter 5 presents the regulation of bus voltage using the phase shift as control variable. In this chapter, the bus voltage is regulated varying the switching frequency. Additionally, using the phase shift, a second slower control loop is added to find the point of maximum efficiency. By experimental verification the proposal was corroborated and an improvement around 0.5% efficiency was achieved at critical operating points.

Conclusions

This thesis is based on the improvement of the electric vehicle powertrain system thanks to the introduction of a DC-DC converter between the battery and the inverter of the permanent magnet synchronous motor. This converter regulates the bus voltage of the inverter, increasing the battery voltage and improving the efficiency of the system thanks to the reduction of the current for a given torque. The most commonly used topology is the boost converter. Although this is an easy to implement stage, it has high losses, especially switching losses. These losses increase notably as the difference between the battery voltage and the bus voltage increases, limiting the operating range of the converter. On the other hand, it does not allow the bus voltage to be reduced below the battery voltage. The thesis presents a novel converter that combines a step up and down stage together with an inverter. The step up and down stage operates under soft switching reducing the switching losses, in addition to reducing the RMS currents flowing through the inverter switches by 10%. It is an isolated stage that thanks to a transformer and the design process proposed in the thesis, allows to choose the optimal gain of the system depending on the battery voltage and the bus voltages levels, being able to operate in a wide range of voltages. Through experimental verification, an improvement of up to 0.75% is observed with the proposed stage compared to the conventional boost converter. In addition to the analysis of the proposed stage, two models are included: one in discrete time and the other in continuous time. From these models, transfer functions are extracted to control the bus voltage from two control variables, phase shift and switching frequency. The transfer functions obtained with either model and with Matlab Simulink are equivalent, with the transfers functions calculated from the discrete model being the simplest to operate and understand. From these models, a proportional control based on discrete control techniques that allows a fast response to disturbances and reference changes, and an integrator using conventional continuous control techniques are elaborated. Finally, an alternative control based on switching frequency variation to regulate the output voltage and phase shift variation to minimize the input current, allowing to improve the efficiency of the stage is elaborated.

List of Figures

List of Tables

Bibliography

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