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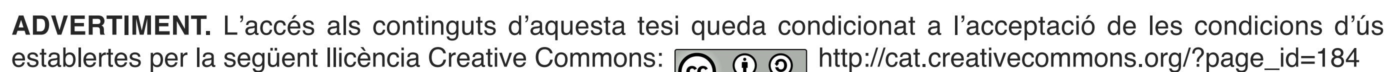

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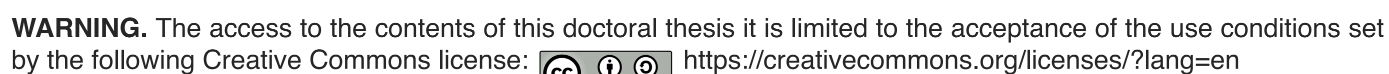

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INTEGRATION OF CERAMIC THIN FILMS IN SILICON TECHNOLOGY FOR ENERGY CONVERSION AND OXYGEN SENSING

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El Prof. Albert Tarancón Rubio y Dr. Nerea Alayo Bueno, investigadors de l'Institut de Recerca de l'Energia de Catalunya (IREC), certifiquen:

Que la memòria titulada "Integration of ceramic thin films in silicon technology for energy conversión and oxygen sensing" presentada per Marco Bianchini per optar al grau de Doctor en el Programa de Ciència de Materials de la Universitat Autònoma de Barcelona ha estat realizada sota la seva direcció a l'Institut de Recerca de l'Energia de Catalunya (IREC).

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Abstract

Entering a new era of sustainable energy generation and consumption, with *Internet of Things* (IoT) dominance in the industry sector and the need of powering more and more devices every year, research is nowadays focusing on alternative power sources as well as on low consumption devices.

Miniaturization of devices has greatly advanced from the beginning of the century, and together with the recent progresses on materials engineering at the nanoscale, new families of devices have come to light. This is the case of Solid Oxide Fuel Cells (SOFCs) and electrochemical oxygen sensors, where their miniaturization was achieved by integration of ceramic thin films in silicon technology and through mainstream microfabrication processes from the microelectronics world. Nevertheless, building devices that operate at temperatures above 500 ºC has proven challenging throughout the years due to the quest of compatible materials that can maintain long-term stability. Furthermore, cost reduction is necessary to scale-up the fabrication of thin-film micro-devices, especially regarding the proposed deposition techniques.

The present thesis focuses on the integration of functional thin films on 4-inches silicon substrates, with the objective of batch-fabricating electrochemical devices such as micro-SOFCs and potentiometric oxygen sensors. To this end, four main areas of study can be identified: (i) optimization of physical/chemical vapor deposition methods to cover large-area substrates with advanced ceramic materials, ranging from selective depositions of crystalline films by *Pulsed Laser Deposition* (PLD), to the conformal coating of high aspect ratio structures by *Atomic Layer Deposition* (ALD), and the development of a faster (and cheaper) counterpart than the latter, i.e., *Spatial Atomic Layer Deposition* (SALD); (ii) Design and fabrication of miniaturized SOFC units based on ceramic suspended membranes on silicon substrates, focusing on obtaining pinhole-free ceramic membranes and on increasing the active area per micro-SOFC unit; (iii) Design and fabrication of a miniaturized electrochemical oxygen sensor for high-temperature applications in IoT; and (iv) Design and microfabrication of other micro-SOFC components, i.e., the gas processing unit necessary to feed the fuel to the electrochemical cell starting from dimethyl ether (DME), and the interconnects to complete a micro-SOFC stack assembly.

The ALD fabrication of a metastable $ZrO_{2-\delta}$ layer showing good ionic conductivity allowed for reliable and pinhole-free electrolyte bilayers, representing the core of these ionic devices. This, together with the control on the residual stresses in the films, improved the yield of fabrication 4-folds. The micro-SOFC technology hereby proposed showed a power output of 40 mW/cm^2 at 600 ºC, while an innovative design based on doped-silicon slabs increased the active area by two orders of magnitude compared to state-of-the-art devices.

The absence of pinholes in a ceramic membrane enabled the creation of a stable reference atmosphere for a potentiometric gas sensor. A reference chamber was obtained by encapsulating the micro-machined sensing platform with a glass lid, due to a glass-ceramic sealing compatible with silicon for operation up to 600 ºC. The sensor showed stable and reproducible response in the range 0.01-100% of oxygen content and comparable performances to bulk commercial sensors operating at higher temperature and based on noble metals.

Finally, the silicon-based micro-reactor technology developed showed great potential for converting DME into synthetic fuel by partial oxidation (POX) reaction. The micro-reformer

included an embedded heater for efficient reaction start-up (<500 J of energy consumption), making it an ideal candidate for integration in micro-SOFCs.

Resumen

Entrando en una nueva era de generación y consumo de energía sostenible, con el dominio del *internet de las cosas* (IoT, por sus siglas en inglés) en el sector industrial y la necesidad de alimentar cada vez más dispositivos, hoy en día es importante desarrollar fuentes de energía alternativas, así como dispositivos de bajo consumo.

La miniaturización de dispositivos ha avanzado mucho desde principios de este siglo, y junto con los avances en la ingeniería de materiales en la nano escala, han emergido nuevas familias de dispositivos. Es el caso de las celdas de combustible de estado sólido (SOFCs, siglas en inglés) y de los sensores electroquímicos de oxígeno, se ha avanzado mucho en su miniaturización gracias a la utilización de procesos convencionales de microfabricación. Sin embargo, la realización de dispositivos funcionantes a altas temperaturas ha demostrado ser un desafío a lo largo de los años por la baja estabilidad termo-mecánica de los materiales a esa temperatura. Además, es necesaria una reducción de los costes asociados a su fabricación y escalado para ser competitivos en el mercado. La presente tesis se enfoca en la integración de capas finas funcionales sobre sustratos de silicio de 4 pulgadas, con el objetivo de fabricar dispositivos electroquímicos a gran escala como micro-SOFC y sensores de oxígeno potenciométricos. Aquí se pueden identificar cuatro áreas principales de estudio: (i) optimización de métodos de deposición físicos/químicos de vapor para cubrir grandes sustratos con materiales cerámicos avanzados, pasando por las deposiciones selectivas de capas cristalinas con *Pulsed Laser Deposition* (PLD), al revestimiento uniforme de microestructuras complejas con Atomic Layer Deposition (ALD), hasta el desarrollo de una versión más rápida (y económica) de esta última, *Spatial Atomic Layer Deposition* (SALD); (ii) Diseño y fabricación de unidades micro-SOFC basadas en membranas cerámicas suspendidas sobre sustratos de silicio, enfocándose en la fabricación de electrolitos densos y cristalinos (así evitando cortocircuitos) y en el aumento del área activa disponible en cada celda; (iii) Diseño y fabricación de un microsensor de oxígeno electroquímico para aplicaciones de alta temperatura en IoT; (iv) Diseño y microfabricación de otros componentes del sistema micro-SOFC, como la unidad de procesamiento de combustible necesaria para alimentar la celda electroquímica a partir de dimetil éter (DME), y las interconexiones para completar el apilamiento de celdas.

La fabricación por ALD de una capa de $ZrO_{2-\delta}$ con buena conductividad iónica permitió obtener electrolitos densos y sin poros, que representan una parte fundamental de estos dispositivos iónicos. Esto, junto con el control de las tensiones residuales en las capas, cuadruplicó el rendimiento de fabricación. Esta tecnología micro-SOFC mostró una potencia de 40 mW/cm^2 a 600 ºC, mientras el diseño innovador con nervios de silicio dopado permitió aumentar el área activa en dos órdenes de magnitud en comparación con los dispositivos tradicionales.

Además, este electrolito sin poros permitió la creación de una atmósfera de referencia estable necesaria para un sensor de gas potenciométrico. Asimismo, se obtuvo una cámara de referencia encapsulando la plataforma de detección con una tapa de vidrio micromecanizada, gracias a un sellado a base de vidrio compatible con silicio para aplicaciones hasta 600 ºC. El sensor mostró

una respuesta estable y reproducible en el rango de 0,01-100 % de oxígeno y rendimiento comparable a sensores comerciales que funcionan a temperaturas más altas y están basados en metales nobles.

Por último, el microreactor desarrollado mostró un gran potencial para convertir DME en combustible sintético mediante una reacción de oxidación parcial (POX). El microreformador incluye un calentador incorporado para un inicio de reacción eficiente (<500 J de consumo de energía), convirtiéndolo en un candidato ideal para la integración en sistemas micro-SOFC.

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CHAPTER 1

INTRODUCTION

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1.1 Introduction on portable power sources

1.1.1 State-of-the-Art power generators for portable devices

Ever since the development and commercialization of Li-ion batteries in the 1980's, the number of portable electronic devices and power tools has drastically increased. While the first commercial devices featuring these innovative power-sources were considered luxury goods, it has been estimated that nowadays the number of portable devices exceed the world population [1]. Years of efforts on research and development of rechargeable batteries, also called secondary batteries, succeeded in the improvement of the batteries' performances and led to the cost reduction of the materials and manufacturing processes.

Whereas primary batteries (non-rechargeable) are still commonly used for low power applications (1-100 mW) together with energy harvesters (EH), secondary batteries represent the main choice for the devices forming the so-called 4 Cs, i.e. cellular phones (smartphones), portable computers, camcorders and cordless power tools [2]. Figure 1.1 shows a classification of the most common portable energy sources as a function of their operating power needs [3].

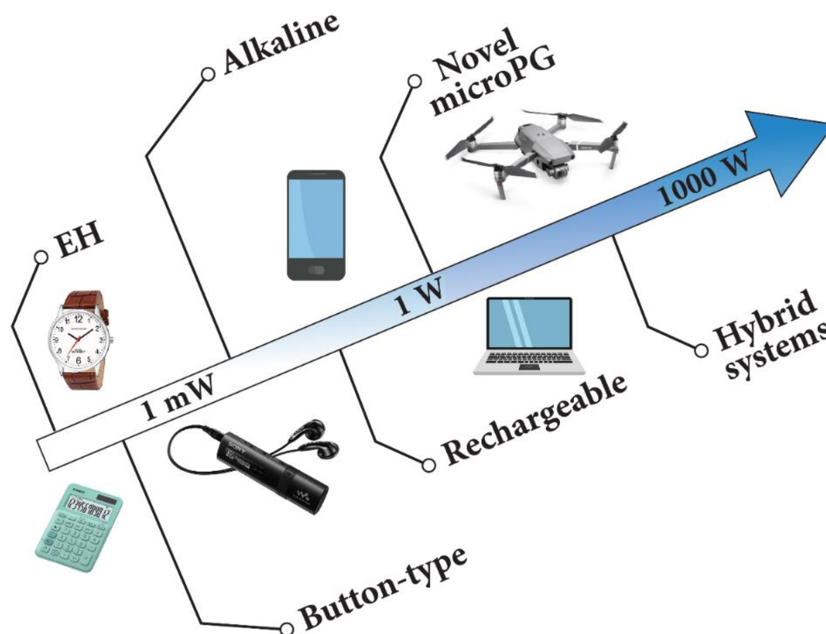


Figure 1.1. Illustration of portable devices and typical power sources depending on the power requirements.

Apart from the specific power needed for a certain application (W/kg), the most important parameters to describe a power source are energy density (Wh/L) and specific energy (Wh/kg), usually expressed as a volume or weight fraction of the active materials. In the particular case of batteries, these latter only count for about 50% of the total weight of the device as there are other components besides electrodes and electrolyte. Moreover, the actual energy density of a battery is about 25-35% of its theoretical value [4].

Table 1.1 below reports the most typical commercial batteries for portable applications [5,6]:

Technology	Gravimetric energy density (Wh/kg)	Volumetric energy density (Wh/L)	Voltage (V)	Specific power (W/kg)
Ni-Cd	40-70	50-150	1,2	150
NiMH	60-120	140-300	1,2	250-1000
Lead acid	30-50	60-110	2,1	180
Alkaline	85-190	250-430	1,5	50
Zn-air (primary)	442	970-1500	1,5	100
Li-ion (polymer)	100-300	250-700	3,7	200-1200

Table 1.1. Comparison between traditional power sources for portable applications

Li-ion batteries have become predominant for most applications as they provide good energy density and specific power, but especially for their rechargeable characteristics that would allow long lifetime and cycling capability. Therefore, these power sources are currently preferred for most portable applications in the power range 1-1000 W.

1.1.2 Limitation of Li-ion batteries

Li-ion batteries have been the main power source candidates for portable application due to their high energy density (250-700 Wh/L) and specific energy (100-300 Wh/Kg) that make them ideal for a wide range of applications. Nevertheless, at the current state this technology features major drawbacks when one considers the future trends for mobile electronic devices, where high energy density as well as low weight and volume are of major concern. Indeed, while the specific power achieved with commercial LiPO batteries is attractive for many applications, major concerns arise from the low specific capacity (Ah/Kg) that strongly limit the time of operation of a device and the long recharge time needed (typically 1-2 hours). From a practical point of view, these issues limit the application of Li-ion batteries for continuous operation. For instance, if we look up to applications in drones, the average specific capacity of a Li-ion battery integrated in commercial products is about 14 mAh/g and the average flight time for commercial drones is estimated to be around 20-40 min [7]. Indeed, it is evident the need of novel power sources to extend these devices' operation time and the overall energy density in portable devices.

This concept is illustrated in Figure 1.2, where the gap between capacity requirement and the energy density provided by Li-ion batteries increases with the addition of new functionalities of the devices for the specific case of smartphones and tablets.

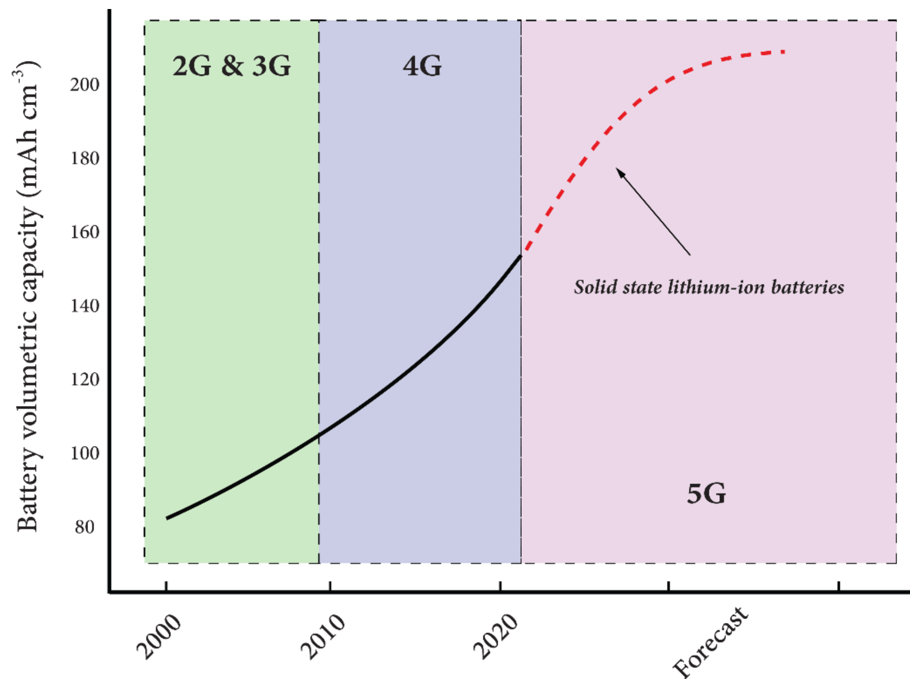


Figure 1.2. Evolution of the volumetric capacity of Li-ion batteries over time.

Other big issues related to battery technology are cost and lifetime. Whereas in recent years the cost has experienced a significant reduction in the whole value chain, lifetime is much harder to improve due to technological limitations such as aging, secondary phases formation at the interfaces and polarization effects. This results in a lifetime estimation of 1500 to 2000 cycles with a capacity retention above 80% in the best-case scenario [6].

Finally, sustainability issues are arising around Li-ion batteries as the raw critical materials involved in their fabrication are non-abundant, require a great deal of resources for their extraction (such as water) and their uneven localization causes geopolitical issues around the globe [8].

1.1.3 Alternative technologies for portable power generation. Micro-fuel cells

Research on Li-ion batteries has collected more than half-billion Euros funding in the H2020 framework programme and it accounts for a growing trend of investments especially due to the advent of the electric mobility era. Most efforts in research and development are nowadays focused on finding a way to overcome the main issues related to Li-ion batteries (as mentioned in the previous section) or to find new portable and rechargeable power sources relying on different technologies, especially for those portable applications where high gravimetric and specific energy densities are needed.

Different types of promising technologies have been proposed to undertake this challenge, among other, solid-state Li-ion batteries (SSLIB), micro-fuel cells (FC), metal-air batteries and micro-harvesters (for low-energy applications), or hybrid systems taking advantage of multiple technologies combined. The main selection criteria for a certain application are power requirement and size (or weight) of the power source, since many last-generation portable devices require miniaturization of all components (e.g., smartphones, laptops, power banks,

drones and robots for rescue or military applications). Here, safety and recharge time also play an important role for continuous operation in practical applications.

Table 1.2 below reports some of the main features of the abovementioned technologies [4,9–13]:

Technology	Recharge	Gravimetric energy density (Wh/Kg)	Volumetric energy density (Wh/L)	Power density single cell (mW/cm^2)
SSLIB (Li metal)	~20 min	440	1000	*NA*
Micro-PEMFC	Refill	250-800	500-1000	20-40
Micro-SOFC	Refill	1000	1000	10-500
Metal-air	*NA*	1000-12000	2000-10000	1-100
Redox flow	Refill	10-50	10-200	1000-1500

Table 1.2. Comparison between novel miniaturized power sources

Micro-fuel cells are the most promising technology to take over applications where the heavy weight of batteries is particularly limiting. Indeed, the maximum capacity in Li-ion batteries is limited by the amount of active material in the battery, thus higher energy density is associated to heavier batteries. while in fuel cells by the amount of available fuel. Conversely, the main advantage of fuel cells technology is that they rely on a fuel supply that increases the energy density provided by one single charge depending on the size of the tank. Therefore, recharge time is equal to the time needed to refill the tank (e.g., less than a minute). The two main fuel cell technologies, namely proton exchange membrane fuel cells (PEMFC) and solid oxide fuel cells (SOFC) and further described in section 1.2.2, show different advantages in a miniaturized system: while PEMFC are easier to integrate and to scale-up to different power requirements, they show relatively low energy density and lower efficiency; SOFC instead provide outstanding energy densities but they work at intermediate or high temperatures (usually above 500 ºC), making their integration in portable systems challenging [14].

Here, hydrogen is usually the fuel of choice in many applications. Nevertheless, when considering energy vectors for mobility and portable applications, hydrogen is not considered the best candidate because of its difficult distribution and storage. Physical storage is the most mature and frequently used approach and it consists in the cooling (down to cryogenic temperature, ~ -253 ºC) and/or compression of H_2. In the mobility sector, standard pressures for gaseous H_2 storage are 350 bar and 700 bar, leading to gravimetric energy density values of 2.9 and 4.8 MJ/L respectively [15]. These alternatives can be technologically non-trivial in miniaturized systems.

Hydrocarbon-based fuels represent a possible solution for a safer and easier feeding of portable devices. They possess high energy density, are easy to store and the infrastructure for their distribution is already existing in most cases [15]. Reforming of these fuels usually lead to a H_2-rich syngas production, containing about 70-80% of H_2 in the case of steam reforming and about 35-40% for partial oxidation reactions.

Here, the choice on the type of fuel for a certain application should be made based on its reforming temperature, which shall be as low as possible to reduce the size of water-shift reactors. Table 1.3 proposes a comparison between hydrogen and hydrocarbon-based fuels where ethanol and dimethyl ether show the highest volumetric energy and H_2 density and, first and foremost in portable applications, are non-toxic (e.g., conversely to methanol).

Fuel	Mole mass (g/mole)	Density (kg/m^3)	H_2-content (mole H_2/mole)	H_2-density (kg H_2/m^3)	HHV (MJ/kg)	Energy per volume (MJ/m^3)
Methanol (CH_3OH)	32	792	0.125	99	22.7	$1.78x10^3$
Ethanol (C_2H_5OH)	46	789	0.130	103	29.7	$2.34x10^3$
Dimethylether (CH_3OCH_3)	46	666	0.130	87	31.7	$2.11x10^3$
Propane (C_3H_8)	44	1.88[(1)]	0.182	0.34	50.2	94.38
Natural gas (CH_4, alkanes, CO_2)	19	0.90[(2)]	0.211	0.19	52.23	47.00
Methane (CH_4)	16	0.72[(2)]	0.250	0.23	55.5	39.96
Hydrogen[(3)] (H_2)	2	70	1.000	70	141.9	9.93

[(1)] NTP - Normal Temperature and Pressure - is defined as air at 20°C and 1 atm
[(2)] STP - Standard Temperature and Pressure - is defined as air at 0°C and 1 atm
[(3)] For comparison

Table 1.3. Physical properties of different hydrocarbon fuels compared to pure hydrogen, from ref [16].

Among these fuels, DME is a non-petroleum based alternative fuel that could have a great impact on society due to its low environmental impact and physio-chemical properties that would lead to technological advantages compared to other fuels. Indeed, previous studies [17] demonstrated higher well-to-wheel efficiency and lower greenhouse gases emissions together with the lowest start-up energies correlating to higher overall efficiencies for on-board automotive fuel processors. Finally, DME storage and transport infrastructures are the same as LPG or natural gas, making it cheaper to integrate than compared to hydrogen. On the other hand, from a technological point of view, DME would be easier to integrate in micro-fuel cells for its reforming temperature is reported to be lower than for ethanol for instance, allowing for an easier thermal management of the device [18].

1.2 Introduction to fuel cells

Fuel Cells (FC) are electrochemical devices able to convert chemically bound energy directly into electrical energy. Invented by Sir William Grove in the middle of the 19th century, their development has been much slower than for the well-known steam engine or internal combustion engine. The reason for this was reduced to economic factors and lack of adequate materials. A new drive for the development of this technology came one century later, when a power generator that could also provide heat and potable water arouse interest for airspace applications[19].

In fuel cells, the energy contained in the fuel is converted into electrical and heat energy. In this process, 286 kilojoules of energy are released per mol of hydrogen. The conversion of this energy (reaction enthalpy) into electrical energy determines the maximum efficiency of a fuel cell that, in theory, can reach over 80% efficiency depending on the technology. The high efficiency, high gravimetric energy density and low emissions (only water is produced if H_2 is used as a fuel) are the main features driving the development of these devices [20].

Nowadays, fuel cells find worldwide application mostly for stationary and backup power and combined heat and power generation. More than 800 MW of installed capacity from large stationary fuel cell systems were installed prior to 2018, 95% of which is located in the US and South Korea [21]. On the other hand, figures show that since 2016 the main fuel cells application for installed capacity is transportation, whereas a small percentage is dedicated to portable applications [22].

1.2.1 Fuel cells working principles

The basic structure of fuel cell consists of an ion-conducting electrolyte which separates the electrodes, namely cathode and anode on each side. Redox reactions take place when a fuel and an oxidant are flowed through the anode and cathode respectively, generating electricity from the fuel oxidation and oxidant reduction. The electrolyte is designed to transport one of the ionic species generated by these reactions (either H^+ or O^{2-}, depending on the type of FC) from one electrode to the other, while remaining electrically insulator. In this way, ions flow through the cell and electrons through an external circuit, closing the redox reaction and creating the desired electronic output.

A schematic representation of the FC working principle is depicted in Figure 1.3 where a distinction is made between anion-conducting and proton-conducting electrolytes, where oxygen and hydrogen are used as oxidant and fuel, respectively. The redox reactions occurring at the electrodes interface are oxygen reduction reaction (ORR), at the cathode side, and hydrogen oxidation reaction (HOR) at the anode side.

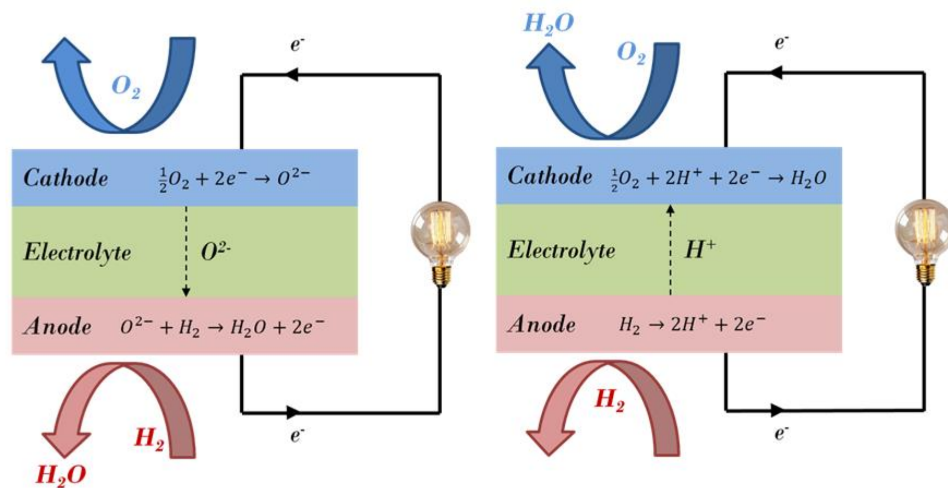


Figure 1.3. Schematic illustration of the fuel cell's working principle with anion conducting or proton conducting electrolytes.

The electrochemical potential of the fuel cell is a measure of the energy per unit charge arising from the redox sub-reactions to drive the fuel cell overall reaction, written as

$$H_2 + \frac{1}{2}O_2 \rightarrow H_2O \qquad (1)$$

The fuel cell potential strongly depends on the chemical species fed to the cell and is given by Nernst equation as follows

$$\Delta E = E_{FC} - E_{FC}^{0} = -\frac{RT}{nF}\ln Q = -\frac{RT}{nF}\ln\frac{a_{ox}}{a_{red}} \tag{2}$$

where R is the universal gas constant, T is the temperature, n the number of charges involved in the cell reaction, F the Faraday constant and Q the reaction quotient, related to the chemical activity of the selected chemical species (a_{ox} and a_{red}). The potential gradient ΔE is indeed the difference between the potential of the cell measured in operating conditions and the ideal standard potential measured at 25 °C and (i) concentration of 1M, (ii) partial pressure of 1 atm or (iii) metals in their pure state.

The fuel cell potential E_{FC} can also be calculated from the redox sub-reactions potentials, which define the capacity of the oxidant to gain electrons in respect to the counter reduction reactions (in this case, $H_2 \leftrightarrow 2H^+ + 2e^-$). The reduction reaction potential E_{red} is arbitrarily set to +0.00, thus the fuel cell potential can be written as

$$E_{FC} = E_{ox} + E_{red} \tag{3}$$

where the E_{ox} related to oxygen reduction has a value of +1.229. According to equation (3), the fuel cell potential related to the overall reaction (1) is E_{FC}=+1.229 V for liquid water product, or E_{FC}=+1.18 V for vapor water product.

It is important to notice that this equation describes a fuel cell system under equilibrium, i.e., without current flowing through the device (open circuit voltage, OCV). In practice, the real voltage measured across the cell is lower than the standard cell potential due to irreversible losses associated to different physio-chemical factors occurring under operation.

Three main causes has been identified to be responsible for these losses: (i) activation losses, when low current is flowing through the cell due to the activation of the electrochemical reactions, especially relevant in low-temperature fuel cells (LT-FC); (ii) ohmic losses, increasing linearly with the current due to the ionic and electronic conduction and (iii) concentration losses, when the flowing current is high and the limitation comes from mass transport and fuel delivery to the electrodes. According to the processes described above, the actual voltage under load is determined by

$$V = E_{FC} - \eta_{act} - \eta_{ohm} - \eta_{con} \tag{4}$$

where $\eta_{act}, \eta_{ohm}, \eta_{con}$ represent the abovementioned voltage losses.

Figure 1.4 shows that three regions can be indeed distinguished in a measured I-V curve (current measured upon small voltage variations) linked to the three losses phenomena. The minimization of these losses is thus critical to any fuel cells manufacturers as they directly correlate with the power output of the cell P = V•I. Finally, the cell operating voltage is usually found in the gas diffusion losses region, where the power output is the highest.

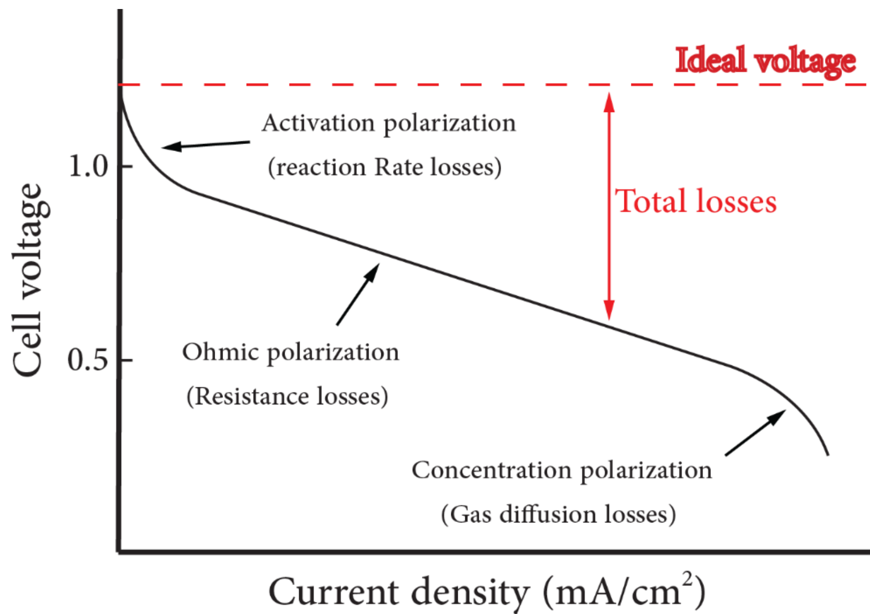


Figure 1.4. Typical voltage-current curve for fuel cells and contributions to the overall voltage losses.

1.2.2 Fuel cells types

There are five major types of fuel cells and they can be categorized on the basis of their electrolyte:

1. Alkaline fuel cell (AFC)
2. Polymer electrolyte membrane fuel cell (PEMFC)
3. Phosphoric acid fuel cell (PAFC)
4. Molten carbonate fuel cell (MCFC)
5. Solid-oxide fuel cell (SOFC)

Table 1.4 summarizes the properties of the abovementioned technologies in terms of materials, fuels, performances and applications while Figure 1.5 shows the basic working principle of each type of fuel cell.

Fuel cell type	Temperature range (°C)	Electrolyte	Power range	Fuel	Oxidant	Efficiency (%)	Investment cost (USD/kW)	Applications
AFC	60-90	Potassium hydroxide	Up to 250 kW	H2	O2 (pure)	50-60	700	Space, submarines
PEMFC	50-180	Polymer membrane	500 W to 400 kW	H2 gas, syngas,biogas, hydrocarbons (external reforming)	O2	30-60	500 (mobile)-4000 (stationary)	Transportation, space, micro CHP, backup power
PAFC	160-220	Phosphoric acid	Up to several 10 MW	H2 gas, syngas,biogas, hydrocarbons (external reforming)	O2	30-40	5000	Decentralized power generation, CHP
MCFC	600-700	Carbonate melt	100 kW to MW	H2 gas, syngas,biogas, hydrocarbons (internal reforming)	O2	55-60	6000	Power plants, CHP
SOFC	700-1000	Solid ceramic electrolyte	kW to MW	H2 gas, syngas,biogas, hydrocarbons (internal reforming)	O2	50-70	4000	Power plants, (micro-)CHP

Table 1.4. Comparison of different fuel cells technologies and properties [20].

Among these, SOFC and PEMFC are the most promising technologies for miniaturization due to their high energy density and efficiency, as mentioned in section 1.1.2. Here, the goal of researchers is to enable such technologies to deliver 0.1 to 20 W from a miniaturized and compact integrated power source for portable applications.

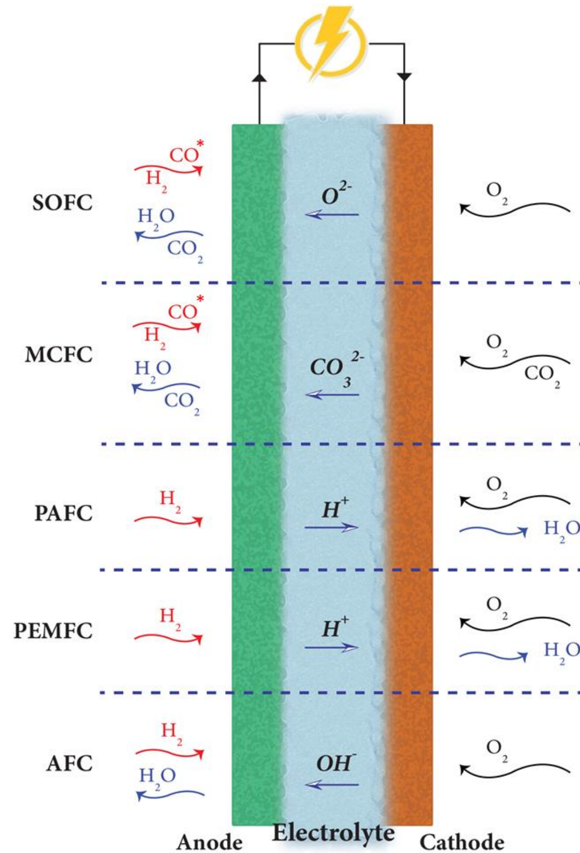


*Figure 1.5. Schematic illustration of the working principle of different fuel cell technologies. The mobile ionic species are represented (regardless the stoichiometry of reaction) in the electrolyte. *Indicates optative species.*

1.2.3 SOFC

SOFCs are considered to be a promising technology for a carbon-free energy transition due to the high efficiency provided together with low capex and high-power range.

Nowadays, SOFC technology has demonstrated to be sufficiently mature for applications in large, high-power applications such as full-scale industrial stations and power plants. A SOFC system usually utilizes a solid ceramic as the electrolyte and operates at high temperatures (700–1000°C). This high operating temperature allows internal reforming, promotes rapid electrocatalysis with non-precious metals, and produces high quality byproduct heat for co-generation (CHP). Efficiencies for this type of fuel cell can reach up to 70% with an additional 20% as heat recovery. Nevertheless, bulk SOFC systems are usually limited to provision of power in utility applications due to the significant time required to reach operating temperatures.

These modular power generators are usually designed by stacking multiple fuel cell units that can be fabricated either in planar (Figure 1.6-a) or tubular configurations (Figure 1.6-b). Depending on the chosen configuration, different interconnect geometries can be applied to electrically connect multiple fuel cells together in series or parallel, also providing gas diffusion paths (especially in the case of planar flat-plate stacks). Stainless steel is the reference material for interconnects, although better-performing alloys and coatings have been under research for many years [23].

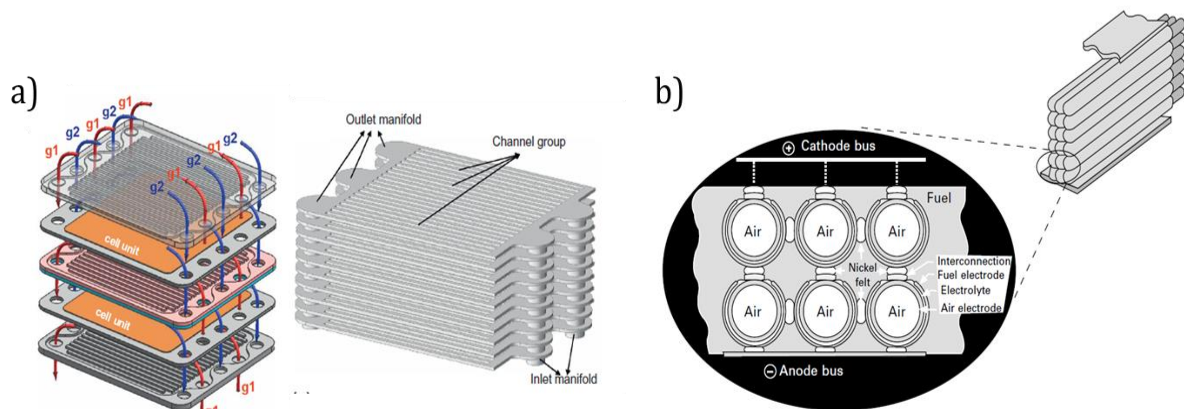


Figure 1.6. Typical (a) planar and (b) tubular SOFC stack configurations, adapted from [23,24].

1.2.3.1 Electrolyte materials

In either case, a fuel cell unit comprises a dense ceramic oxide **electrolyte** that separates two porous electrodes, namely cathode and anode, which catalyze the ORR and HOR, respectively. The main requirements for an electrolyte to work efficiently are [19,25,26]:

i. Oxide ion conductivity must be sufficiently high (~0.1 S/cm at operating temperature).
ii. Low electronic transference number (< 10^{-3}).
iii. Thermodynamic and chemical stability over wide range of temperatures (from room temperature to 1000 °C) at variable activities of oxygen (1 - 10^{-22} atm)
iv. Negligible volatilization.

v. Chemically inertness toward electrode materials both during processing and service.
vi. Compatibility of CTE with adjoining cell components.
vii. Possessing reliable mechanical properties (such as fracture strength > 400 MPa).

Zirconia is among the most common materials used in SOFC technology. It is known to be stable at low temperature in the monoclinic form which does not show good ionic conductivity. This material is therefore stabilized in the tetragonal or cubic phase (known as the high-temperature phases) by adding a trivalent dopant (Y, Sc), which simultaneously increases the ionic conductivity of the electrolyte [27]. Indeed, the creation of more oxygen vacancies in the system can be expressed according to the Kroger-Vink notation with the following equation:

$$Y_2O_3 \rightarrow 2Y_{Zr}^{`} + V_O^{\cdot\cdot} + 3O_O^x \quad (5)$$

Yttria-stabilized zirconia (YSZ) is a state-of-the-art electrolyte material and the most common commercially available composition is 8 mol.% Y_2O_3-ZrO_2 showing the highest ionic conductivity among YSZs of ~$1x10^{-2}$ S/cm at 600 ºC with no electrical contribution up to 1500 ºC [28].

YSZ has been the best candidate for integration in micro-SOFC as it satisfies the thermo-mechanical and electrical requirements for such application and for its compatibility with other SOFC components. Nevertheless, zirconium oxide tends to react in contact with the electrode's materials forming undesired secondary phases (see section 1.3.2), cerium oxide is inert, providing a unique advantage over ZrO_2 that finds further applications in SOFC technology such as barrier layers [29] between the electrolyte and the electrodes. Other families of electrolyte materials include Bi-based oxides (e.g., stabilized BiO_2 or BiMeVOX, where Me is a transition metal), doped brownmillerite structures such as $Ba_2In_2O_5$ or lanthanum gallate $(La_{1-x}Sr_x)(Ga_{1-y}Mn_y)O_3$ [25,26].

Ceria (CeO_2) is a widely investigated ceramic material, especially attractive for SOFC industry due to its thermal and chemical stability, together with good mechanical and electrical properties. CeO_2 mixed ionic and electronic conduction is indeed what allows its integration in SOFC as anode [30] or barrier layer [29]. Electrical conductivity is expressed as a function of p_{O2} according to equation 6

$$\sigma = \sigma_i + \sigma_e^{\circ} p_{O_2}^{-r} \quad (6)$$

where σ_i and σ_e stand for ionic and electronic conductivity, respectively. It is worth noting that whereas electronic contribution depends on the oxygen partial pressure p_{O2} (r=-¼ extrinsic, -1/6 intrinsic), ionic conductivity does not, and it appears as a plateau in a σ vs. log p_{O2} plot. Here, structural stability is maintained upon oxygen loss thanks to the ability of cerium cations to be reduced from Ce^{4+} to Ce^{3+}, written according to Kroger-Vink notation as in equation 7:

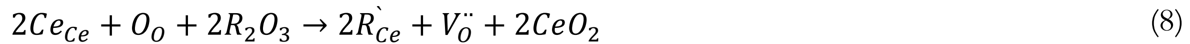
$$2Ce_{Ce} + O_O \rightarrow 2Ce_{Ce}^{`} + \frac{1}{2}O_2(gas) + V_O^{\cdot\cdot} \quad (7)$$

Nevertheless, ceria reduction causes its volume expansion that could lead to mechanical instability and peeling off the electrolyte [31].

Despite the ionic contribution to the total conductivity is usually less than 3% [32] for pure CeO_2, many studies found that higher ionic conductivity values are obtained for doped-ceria

with formula $Ce_{1-x}R_xO_2$ where *x* represents the stoichiometric doping concentration and R the dopant, usually a rare-earth element (Gd, Y, Yb, La, Sc, Sa) [33].

Doping ceria with a trivalent atom results in the formation of more oxygen vacancies in the system expressed by equation 8:



$$2Ce_{Ce} + O_O + 2R_2O_3 \rightarrow 2R_{Ce}^{`} + V_O^{\cdot\cdot} + 2CeO_2 \quad (8)$$

thus leading to higher ionic conductivity.

1.2.3.2 Electrode materials

SOFC **electrodes** are made of materials with high catalytic activity towards the redox half-reaction involved. Nevertheless, the gas species reaching the electrode undergo redox reactions only in specific spots where the electrolyte, gas and catalyst electrical connection coexist, called *triple phase boundaries* (TPB), as shown in Figure 1.7.

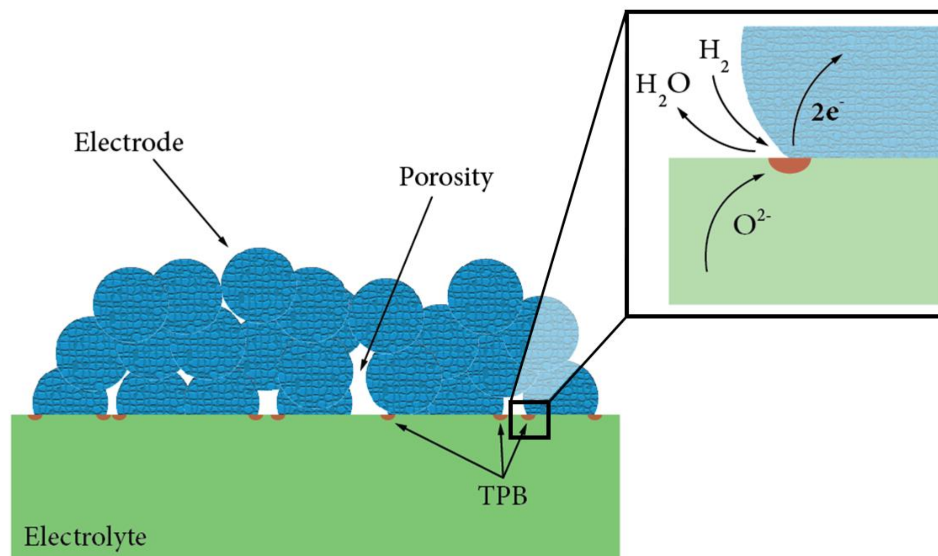


Figure 1.7. Schematic illustration of the triple phase boundaries (TPB) at the interface between electrode, electrolyte and gas. A typical catalytic reaction occurring at the anode side is represented in the inlet.

In order to maximize the extent of TPB region, porous and nanostructured materials are usually employed as fuel cell anodes or cathodes. Typical requirements for a SOFC electrode include [34]:

i. High electronic conductivity (preferably more than 100 S/cm in an oxidizing/reducing atmosphere);
ii. Minimum or no mismatch between the CTE values of the electrode and other components of the cell, such as, electrolyte, interconnect materials, etc.;
iii. Good chemical compatibility with the electrolyte and interconnect materials;
iv. Sufficient porosity to allow fast diffusion of oxidant/reducing gas from electrode to electrode-electrolyte interface or to increase the active area;
v. Good chemical, structural and mechanical stability in the corresponding atmosphere;
vi. High catalytic activity during oxygen reduction reaction or fuel oxidation reaction;
vii. Cost effective.

The most common **anode** materials are based on nickel, a well-known catalyst for hydrogen oxidation, where some examples are reported in Figure 1.8. Despite being an optimal catalyst, Ni metal shows a CTE mismatch with other common SOFC materials such as YSZ and tend to aggregate under operation conditions. For these reasons, ceramic-metallic composites (cermets) were proposed and fabricated by co-sintering or infiltration processes [26]. These Ni-based composite materials were able to satisfy most requirements for a SOFC anode, although showing severe poisoning from fuel contaminants (coking, Sulphur contamination etc.) and mechanical instability upon metal re-oxidation (e.g., from Ni to NiO) when employing hydrocarbon-based fuels [34].

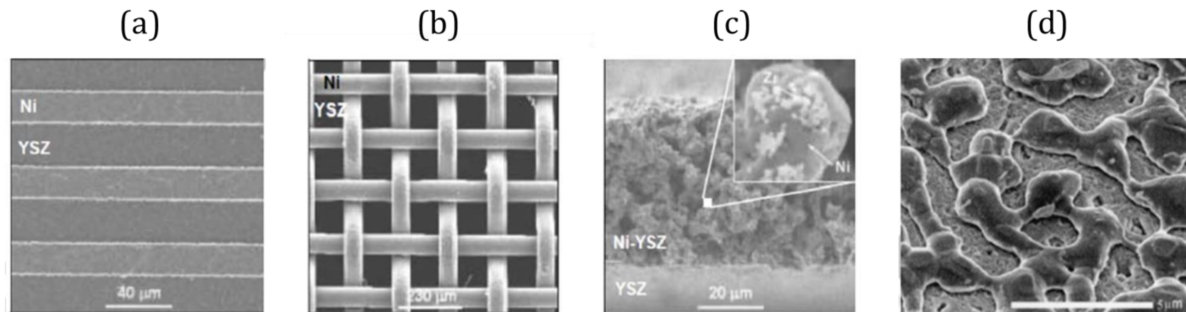
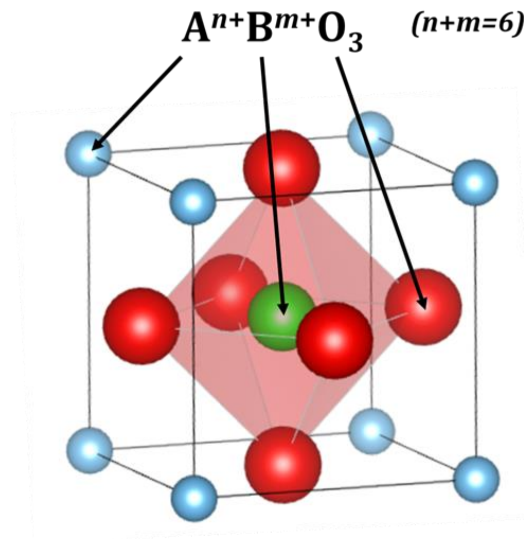


Figure 1.8. Examples of micro and nano-structured anodes based on nickel, readapted from ref [34]. *(a) Patterned thick film, (b) Woven structure (gauze), (c) porous cermet paste and (d) micro-structured metallic nickel.*

Especially driven by the need to find suitable full-ceramic anodes that could improve tolerance to contaminant and show better fuel flexibility (i.e., that are able to oxidize H_2, CO, natural gas, methanol etc.), a great interest arose from perovskite materials that, furthermore, possess mixed ionic-electronic conductivity (MIEC) properties that allow to extend the TPB length to the whole electrode's surface area, increasing it by few orders of magnitude than compared to porous electrodes showing only electronic conductivity. Among these, some materials developed for this purpose are $La_{1-x}Sr_xTiO_3$, $La_{1-x}Sr_xVO_3$ and $La_{1-x}Sr_xCr_{1-y}Mn_yO_3$, showing good electrochemical performances and improved resistance to contaminants [23,34]. The typical perovskite oxide cubic lattice (Pm3m, s.g. 221) is shown in Figure 1.9-a.

Similarly, perovskite oxides have found application as **cathodes** for SOFCs, replacing platinum that was the first demonstrated catalyst for oxygen reduction. Here, three main pathways for the cathodic reaction exist [35] and summarized in Figure 1.9-b, although in all cases the limiting step is considered to be oxygen oxidation rather than charge or mass transport. Each of these steps is predominant depending on the type of cathode's electronic properties: the electrode surface path mainly occurs in electronic materials (e.g., LSM), the bulk path is typical for MIECs (e.g., LSCF), while the electrolyte surface path was observed in composites (e.g., LSM-YSZ).



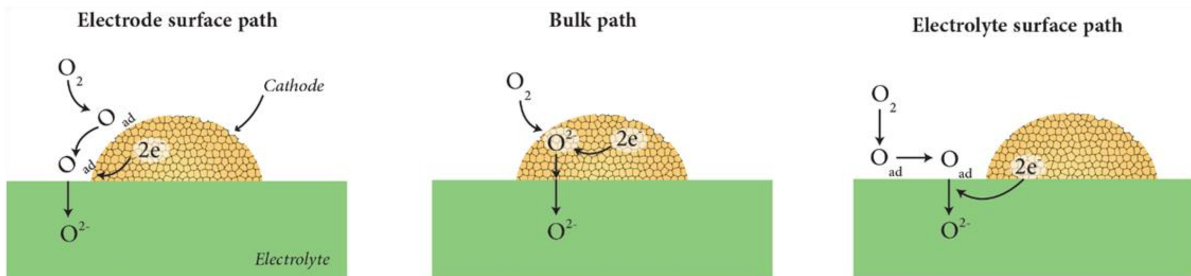


Figure 1.9. (a) Typical unit cell of a cubic perovskite structure; (b) Proposed mechanisms of oxygen reduction and diffusion depending on the type of electrode.

In the next sections, the existing approaches for integration of the abovementioned materials in micro-SOFC technology are proposed.

1.3 State-of-the-art on micro-SOFC-based power generators

As previously mentioned in chapter 1.1.2, micro-SOFCs have been considered as one of the most promising technologies for portable applications as they provide high theoretical energy density and are compatible to MEMS fabrication processes. This approach allows for easy miniaturization by means of well-established and reliable substrate micromachining techniques in combination with thin film technology.

Indeed, whereas standard SOFC employs thick (mm- to tens of µm-thick) ceramic oxygen-ion conductors as electrolytes which require high operating temperature (> 800 ºC) to obtain acceptable ionic conductivity and long start-up times, micro-SOFC components are fabricated in form of thin films (< 1 µm), thus reducing the electrolyte-associated resistance (by three orders of magnitude) and allowing these devices to operate at reduced temperatures (400 - 800 ºC) [36]. Moreover, the fabrication of low thermal mass structures based on silicon allows for fast start-up and low power consumption of the device, allowing this sort of devices to be employed in portable applications. The compatibility of micro-SOFC components with the

microelectronic industry will also has the advantage to enable scaling-up more easily and cheaply the fabrication of these portable power generators.

The schematic design of a micro-SOFC is depicted in Figure 1.10. This approach is based on the vertical stacking of multiple fuel cell units and interconnects that should be sized depending on the application requirements (e.g., with a modular approach), a fuel processing unit needed to vaporize and /or reform the hydrocarbon-based fuel, a fuel post-combustor to ensure that no toxic gases are present at the outlet of the system and, finally, a thermally insulating packaging comprising the fuel tank and gas inlet/outlet lines [37].

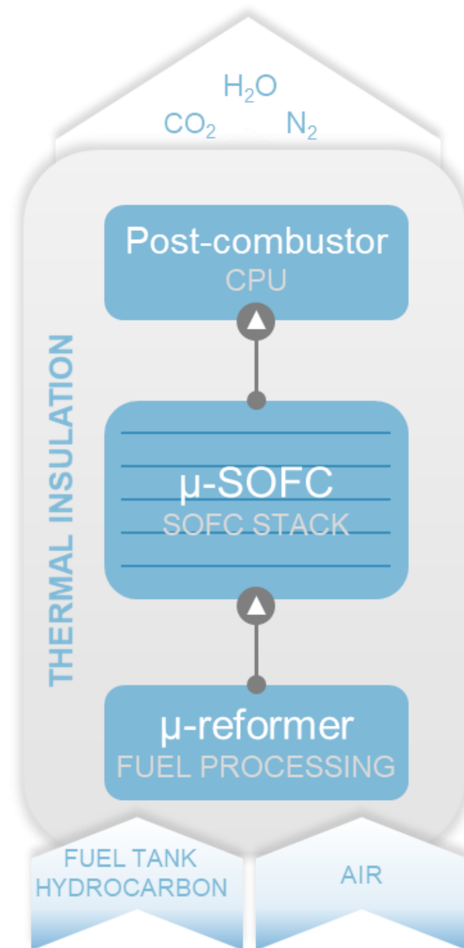


Figure 1.10. Schematic view of the components of a portable power generator based on micro-SOFC.

When designing a micro-SOFC, several requirements must be fulfilled. First, (i) the compatibility of the chosen materials (both support and active materials) with the SOFC operating temperature range and their chemical stability upon operation. Second, (ii) the choice of the substrate must ensure the possibility of bulk micromachining of complex shapes or structural arrays with high precision. Finally, (iii) controlled fuel feed and (iv) optimal thermal management of the system also represent a big challenge for micro-SOFC miniaturization.

In the following sections, a literature review on the previously mentioned micro-SOFC components and systems is proposed.

1.3.1 Micro-SOFC stack

In this section, two main architectures proposed for the fabrication of a micro-SOFC stack and related substrate materials are discussed. Both designs are based on the so-called PEN membrane, where PEN stands for "Positive electrode-Electrolyte-Negative electrode".

On one hand, it is possible to fabricate free-standing PEN membranes on a micromachined substrate through MEMS fabrication processes. In this case, a thin film trilayer structure is usually deposited on a bulk substrate (silicon single crystal or Foturan® glass wafers) that is subsequently micromachined by wet or dry etching methods. Once the substrate material is selectively removed, a free-standing ceramic membrane is obtained constituting the core structure of the micro-SOFC unit. A few examples of microfabricated SOFC membranes are included in Figure 1.11.

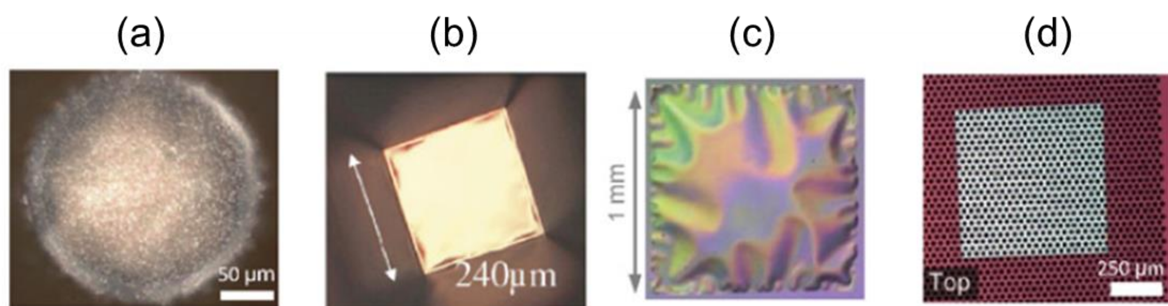


Figure 1.11. Optical images of different suspended membranes, readapted from [12]*. (a) Circular membrane on Foturan, (b-c) squared membranes on silicon, and (d) micro-patterned, corrugated, squared membrane*

Silicon is indeed the most employed substrate material because of its availability, chemical inertness and high temperature range, while the technology to process it is already well-known. Nevertheless, one should consider that when a silicon substrate is used, a dielectric thin layer (e.g., Si_3N_4, SiO_2) is usually added between the silicon and the PEN to avoid electric losses or short-circuits.

On the other hand, another fabrication method involves the deposition of the PEN structure directly onto a porous substrate, i.e., anodic alumina or metals such as nickel plates or stainless steel, allowing access of the fuel to the PEN structure without the need of substrate etching.

Some examples of works existing in literature are summarized in Table 1.5.

Reference		Group	Publication year	Membrane design	Substrate material	PEN membrane thickness (nm)
[38]	Nanoscale membrane electrolyte array for solid oxide fuel cells	Stanford University	2012	Free-standing	Silicon (pre-patterned)	300
[39]	Solid oxide fuel cell membranes supported by nickel grid anode	EPFL	2008	Free-standing	Silicon	700-900
[36]	Full ceramic micro solid oxide fuel cells: towards more reliable MEMS power generators operating at high temperatures	IREC	2014	Free-standing	Silicon (pre-patterned)	750
[40]	Integration of Spin-Coated Nanoparticulate-Based La0.6Sr0.4CoO3 –d Cathodes into Micro-Solid Oxide Fuel Cell Membranes	ETH, KIT	2013	Free-standing	Silicon	650
[41]	Scalable nanostructured membranes for solid-oxide fuel cells	Harvard University	2011	Free-standing	Silicon	220
[42]	Micro Solid Oxide Fuel Cells on Glass Ceramic Substrates	ETH	2008	Free-standing	Foturan	900
[43]	Simple fabrication of micro-solid oxide fuel cell supported on metal substrate	Pohang/ Postech	2008	Anode supported	Ni plate/porous film	4 μm (+22 Ni)
[44]	Micro solid oxide fuel cell fabricated on porous stainless steel: a new strategy for enhanced thermal cycling ability	Pohang /Postech	2016	Anode supported	Porous stainless steel	3.3 μm

[45]	All-Sputtered, Superior Power Density Thin-Film Solid Oxide Fuel Cells with a Novel Nanofibrous Ceramic Cathode	San Diego University	2020	Anode supported	AAO	3 µm
[46]	Micro-solid oxide fuel cell supported on a porous metallic Ni/stainless-steel bi-layer	Postech/ Rist	2014	Anode supported	Porous stainless steel + Ni	1,9 µm (+270 Ni/steel)

*Table 1.5. Micro-SOFC units presented in literature and comparison of substrates and scalability of the active area. *based on reported cathode area.*

In recent years, research trends in the field mostly targeted increasing the power density, improving long-term stability of the materials upon operation, and eventually lowering the operating temperature range to simplify the system requirements.

Among the highest power density values reported, researchers at University of California [45] obtained ~1.7 W/cm^2 at 600 °C with an anode-supported all-sputtered SOFC using dense YSZ and CGO as electrolyte, and co-sputtered porous Ni-YSZ and LSCF-YSZ for the anode and cathode, respectively.

On the other hand, long-term stability of the PEN element upon operation is nowadays a focus issue for researchers, as micro-SOFCs in the past were tested for only a few hours. More recently, Noh *et al.* [47] were able to obtain about 1.1 W/cm^2 power density at 600 °C with only a 17% increase in polarization resistance after 100 hours on an anode (Ni-YSZ pellet)-supported multi-scale architecture. While the anode-supported approach focuses on matching the Coefficient of Thermal Expansion (CTE) [44], graded porosity in the electrolyte is necessary to eventually obtain a fully dense structure, creating a barrier for reproducibility of the fabrication techniques. Additionally, other strategies for long-term stabilization of SOFC electrodes include the addition of a functional conformal coating deposited by ALD [48].

Finally, the real-life operation of a durable and self-sustained micro-SOFC stack is yet to be achieved, although the a few works focusing on the system requirements and designs are also included in Chapter 1.3.3.

1.3.1.1 Thin film electrolytes

Regarding the ceramic electrolyte of micro-SOFC, the most important parameters are:

- The **ionic conductivity** (σ_{el}) related to O^{2-} transport, which is also referred as the Area Specific Resistance of the electrolyte (ASR_{el}). For pure ionic conductors, these properties can be represented by the following equations:

$$\sigma_{el} = k\, e^{-\frac{E_a}{RT}} \tag{9}$$

$$ASR_{el} = \frac{t}{\sigma_{el}} \tag{10}$$

where k is a constant, E_a is the activation energy for ionic transport, R is the universal gas constant, T the temperature and t the electrolyte thickness. It should be noted that an ASR_{el} of 0.25 Ω cm^2 should not be exceeded if a power output of 1 W/cm^2 is targeted at 500 °C. As evidenced by equation 10 the ASR can be drastically reduced by reducing the electrolyte thickness. On the other hand, the electrolyte must remain electronically insulating to avoid power losses.

- **High density and homogeneity** of the film. Regardless the fabrication technique used to deposit thin film electrolytes, it is critical for the final device performance to deposit high-quality dense and homogeneous film. In fact, any macro-defect such as porosity, cracks or pinholes (see Chapter 3.2) could lead to (i) short-circuit, caused by contact between the electrodes or (ii) gas leakages, eventually leading to lower OCV across the electrolyte and thermal stress-driven rupture due to the formation of hot-spots [49].

Nowadays, while different electrolyte materials are known for SOFC applications, only a few have been downscaled to nanometric size and integrated in micro-SOFC. Among those, the most relevant are CeO_2- and ZrO_2-based electrolytes, as discussed in section 1.2.3. The most effective techniques to fabricate high-quality thin film-film electrolytes are ALD, PLD and magnetron sputtering as they provide high homogeneity of the films deposited on large-area substrates, thus showing potential for industrial scale-up. Here, electrolyte thicknesses from tens of nm to few µm have been demonstrated [36,45,50]. Moreover, these techniques are compatible to clean-room processing, eventually enabling cheap mass-scale device fabrication.

1.3.1.2 Electrodes and current collectors

As for its bulk counterparts, the first electrodes used in micro-SOFC were based on sputtered platinum [51]. Whereas the use of Pt as electrode is a good strategy for short-term testing at laboratory-scale, it presents drawbacks for real technology scale-up related to cost and long-term chemical and structural stability. Indeed, it is well-known that noble metal films evolve with temperature by coarsening (or de-wetting) causing the loss of in-plane electrical percolation and thus hindering electrons collection, and degradation both at the cathode and anode side can lead to power density losses of about 50% [52].

For this reason, Garbayo *et al.* [36] proposed for the first time a full-ceramic self-sustained membrane for applications is micro-SOFCs, fabricating by PLD a PEN trilayer made with $Gd_{0.2}Ce_{0.8}O_2$ anode, $Y_{0.08}Zr_{0.92}O_2$ electrolyte and $La_{0.6}Sr_{0.4}CoO_3$ cathode. The full-ceramic approach indeed allows for the integration of cheaper and highly performing catalysts in micro-devices, providing higher stability in time upon operation.

Nevertheless, researchers are still focused on understanding the mechanisms for oxygen transport, kinetics of reaction and especially the influence of factors such as temperature, polarization etc. over the electrode's stability in time. Here, the formation of secondary phases either at the electrode's surface or at the interface with the electrolyte is a well-known problem for perovskites containing Sr, among which we find some of the best-performing materials for SOFCs. Indeed, strontium tends to react with zirconium-based electrolytes forming $SrZrO_3$

secondary phases while SrO forms at the surface exposed to an oxidizing atmosphere, both causing an increase of the ASR of the cell [53]. On the other hand, as previously mentioned in section 1.2.3., contamination from Sulphur and coke formation is another serious problem affecting the stability of the electrodes over time. It is thereby important to find some mitigation strategies allowing for longer retention of the conversion capabilities of a device.

Another important step towards the fabrication of reliable conversion micro-devices at high temperature regards current collection. Despite many ceramic electrode materials already possess electronic conductivity in the order of 100 S/cm, the use of noble metals for current collection is still the preferred approach to improve the in-plane conductivity, especially relevant in thin films devices [54]. Here, sputtered porous films or patterned microgrids are typically used to optimize current collection [55] and improve the mechanical stability of the PEN structure, allowing for the fabrication of large-area self-sustained ceramic membranes [41]. Nevertheless, it is necessary to reduce the amount of noble metal in these devices to drastically reduce the costs of production, thus preventing the use of noble metals only as electrodes.

1.3.2 Fuel processing unit: micro-reformer and post-combustor.

Recalling what was mentioned in section 1.2.3, the use of catalytic micro-reactors for on-board hydrogen production is an established alternative to direct hydrogen storage, since hydrocarbon-based fuels provide high energy density, low cost, safety, and easy transportation [15]. The compatibility of the catalytic reformer with a micro-SOFC power generator requires a system with low thermal mass, fast start-up times with low power consumption and able to produce enough H_2 in the SOFC operating temperature range.

Micro-reactors present many advantages compared to their macro-scale counterparts: higher surface-to-volume ratio and shorter travel distance in the reactor favor the overall reaction kinetics as heat and mass transfer are greatly enhanced. Moreover, a lower amount of reactants together with faster and more efficient mixing allow for safer operating conditions, especially suitable for strong exothermic reactions at harsh conditions [56–58].

MEMS-based micro-reactors, first demonstrated between 1987 and 1994 by DuPont scientists, can be classified into three main types: i) packed bed, ii) wall coated and iii) micro-structured reactors. Each of this reactor design [56,59–61] presents some advantages and drawbacks depending on the chosen application. Nevertheless, certain requirements must be considered for continuous operation at the high temperature regime employed during hydrocarbons conversion reactions. For instance, packed-bed micro-reactors and long in-plane micro-channels reactors usually require large area and show poor heat transfer capabilities due to the insufficient radial mixing of the fuel [62]. Moreover, high-pressure drops can occur along the reaction pathways at the typical low flow rates employed at the micro-scale [63] and the catalyst stability is often compromised. A few examples of MEMS-based micro-reactors are reported in Figure 1.12.

Among other reported micro-reactors, it is remarkable a new design based on silicon monolith embedding an array of micro-channels at multiple size scales, which was developed by Llorca and coworkers [64,65] for the conversion of different hydrocarbons to syngas [66]. In addition, it was previously demonstrated the fabrication of a MEMS-based micro-reformer consisting of

an array of vertical micro-channels (50 µm diameter) defined into a silicon substrate and a serpentine-shaped heater by means of mainstream microelectronics fabrication processes. This innovative approach would allow for optimized thermal management features leading to fast start-up time (less than a minute with vacuum insulation) and low energy consumption below 60 J [37]. The device was tested for ethanol steam reforming by coating the micro-channels with a CeO_2 active support film and Pd/Rh nanoparticles grafted on top. Despite showing promising results, the functionalization of such microreactors with high aspect-ratio structures with stable and uniform catalyst coatings is technologically non-trivial. Indeed, the most typical coating technique, i.e., dip coating (or washcoating) from a liquid suspension or sol mixture, suffers from non-uniform surface tension of the micro-reactor's walls and the resulting coating tends to collect at the corners of the reactor [56]. Therefore, is it necessary to implement scalable and more reliable coating techniques for this type of micro-reactors.

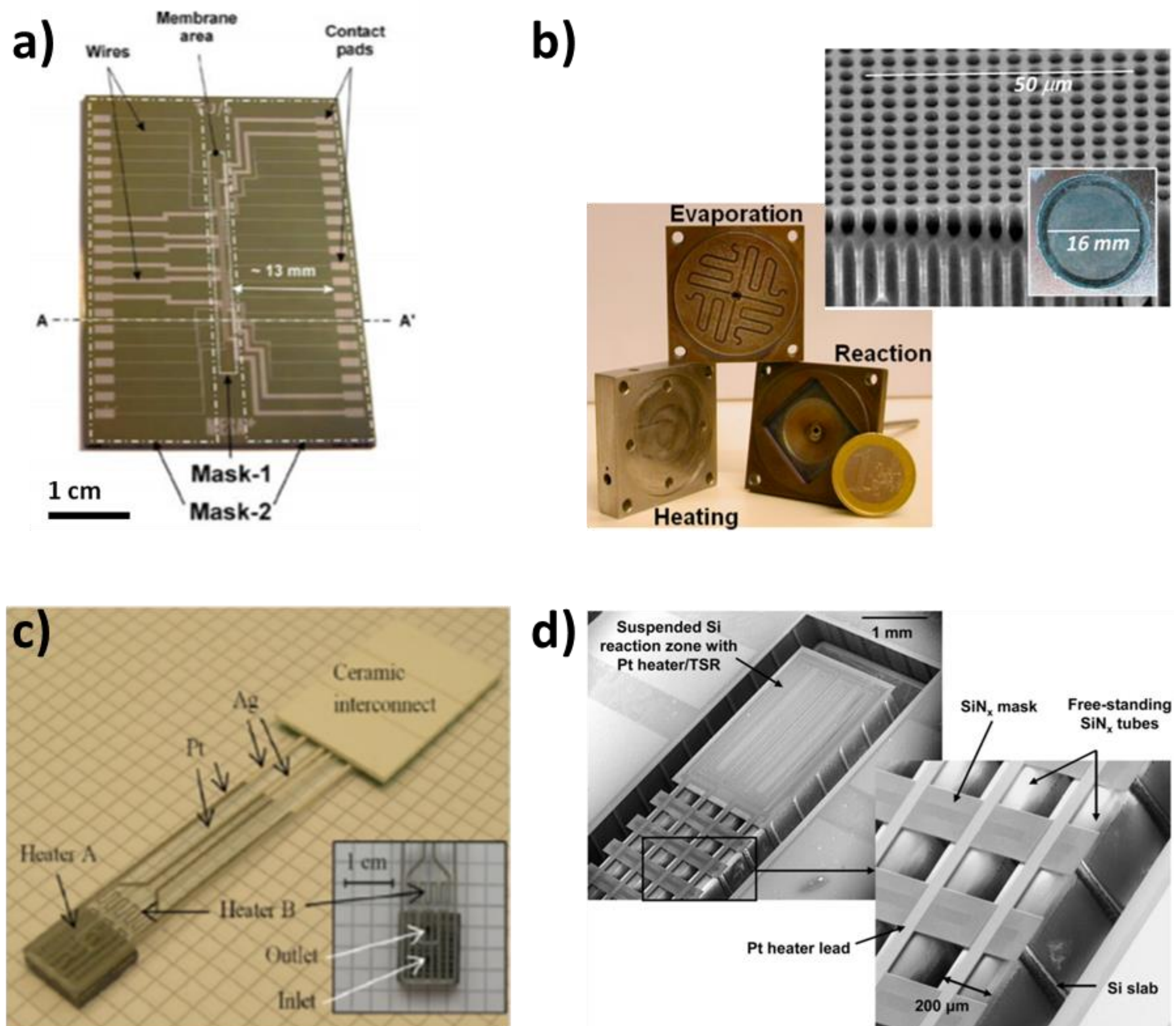


Figure 1.12. Examples of micro-reactor technology applied to portable syngas production. (a) Membrane based microreformer [59]*; (b) monolithic silicon-based micro-reformer with micro-channels* [65]*; (c) packed bed micro-reactor* [60] *and (d) suspended SiNx tubes micro-reactor* [67].

1.3.3 Integrated devices

Since the first demonstrations of miniaturized SOFCs based on thin films, many groups have been focused on the understanding and optimization of materials and processes for the PEN structure. Conversely, very few works have been published on a micro-SOFC device and integration of multiple components due to the fabrication complexity, as summarized in Figure 1.13.

In 2005, Shao et al. published the first thermally self-sustained SOFC stack based on a single chamber configuration. Here, the catalytic oxidation of propane maintained the stack at 500-600 °C and yielded 350 mW power output on a total cathode area of 1.42 cm^2 [68]. Electrical connection in series of two anode-supported micro-SOFC units was thus demonstrated together with the feasibility of a self-sustained thermal regime.

Only a few years later, a fabrication method based on Foturan substrates and a new design of the micro-SOFC power generator were presented [42]. The proposed ONEBAT system [69] consisted of a number of PEN elements in the fuel cell stack, a gas processing unit composed of fuel reformer and exhaust gas post-combustor, a thermal system composed of a fuel and an air pre-heating unit, heat exchanger and insulation.

Here, a modular approach (2.5 W each module) allows the power generator to adapt to different power needs. The same group could demonstrate the efficient hybrid start-up of a micro-power plant where a PEN cell is fed with the syngas produced by propane reforming, and the heat generated by the exothermic reaction (POX) helps reducing the energy consumption during start-up and allows for operation in self-sustained regime (T = 550 °C).

Another system patented by Lilliputian system Inc was instead based on planar stacks with little number of interconnects and where a full system would deliver 3.2 W/cm^3 [3]. Here, most components are fabricated using silicon substrates and the sealings made with a glass sealant.

Pla *et al.* published a study in 2015 [37] regarding the feasibility of designing a 1W micro-SOFC device completely based on silicon substrates and on the vertical stacking of device component previously mentioned. Here, it is shown that the design of a proper insulation (material with low thermal conductivity $k = 5\ mW\ m^{-1}\ K^{-1}$ and thickness of 1 cm) allows for optimal thermal management and thus self-sustained regime of a micro-power source relying again on hybrid electric-catalytic start-up with low energy consumption. The electric heating is provided by embedding a thin film heater onto the micro-reforming MEMS-based platform, allowing for fast start-up of ethanol steam reforming reaction at temperatures of 750 °C [70].

Lately in 2017, another work from Takahara *et al.* [71] was published in which the integration of vacuum insulation (thermal resistivity over 200 kW^{-1} at 300 °C) in a micro-SOFC packaging was demonstrated. Here, a system comprising a micro-SOFC, a fuel processor and thermal insulation was tested, providing more insights on possible system designs.

Whereas different system designs and fabrication methods have been presented, this technology still presents challenges to the full scale-up of an integrated micro-power source operated at high temperatures.

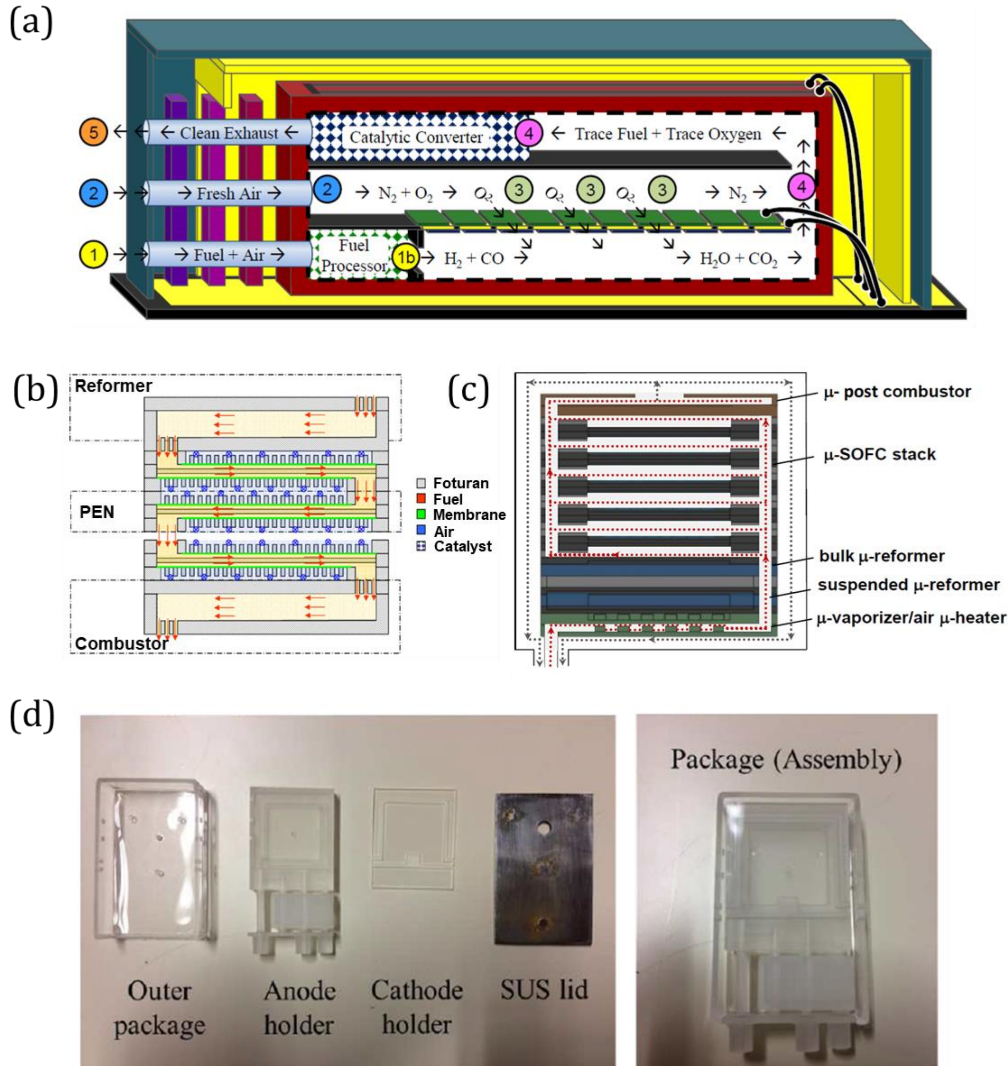


Figure 1.13. Examples of integrated devices design based on micro-SOFC. (a) Lilliputian system based on planar stack [3]*, (b) ONEBAT system and vertical stacking of Foturan-based components* [72]*, ULTRASOFC design based on vertical stacking of silicon components* [37] *and (d) packaging design including vacuum insulation* [71]*.*

1.4 Thin-film electrochemical oxygen sensors

Oxygen is a crucial gas and the precise control of its concentration in an atmosphere is of special relevance in many fields. Indeed, many processes in the chemical industry or combustion-based reaction require good control on the oxygen concentration or oxygen/fuel ratio to either reduce the fuel consumption (and related emissions) or to increase the power output. On the other hand, oxygen sensors can also find applications in the medical sector, where recovering patients can be exposed to a controlled amount of oxygen, or in diving, where the oxygen concentration fed to the diver depends on the time and depth of the activity.

Nowadays, together with an increasing presence of the Internet of Things (IoT) in our society, it is important to develop cheaper and reliable technologies for gas sensing that could be used in

applications before inaccessible and in larger number, enabling a precise and automated control on oxygen concentration for different processes.

Thereby, the next sections focus on the integration of ceramic thin films on silicon platforms for sensing applications.

1.4.1 Oxygen sensors state-of-the-art

The electrochemical oxygen sensors were the first technology developed and adopted in combustion engines since 1976, and it takes advantage of chemical reactions to sense the oxygen concentration in a target atmosphere. The first commercial product developed by Bosch was based on a ceramic solid electrolyte (i.e., YSZ) that requires high temperatures to work properly. Nevertheless, the high cost, low accuracy and high response time of those sensors was a major issue for large-scale adoption [73].

Electrochemical sensors can be divided in two main categories depending on the sensing principle:

- **Potentiometric sensors**: the output signal is the electrical voltage between the two electrodes in the presence of a target gas separated from a reference atmosphere. Then, the oxygen partial pressure of the target gas can be calculated from Nernst equation:

$$E(V) = \frac{RT}{4F}\, ln \frac{P^0_{O2_{ref}}}{P^0_{O2_{meas}}} \qquad \text{(X)}$$

  Here, a solid phase or multi-phase mixtures that establish constant activity of the electrochemically active species are used as reference electrodes. It is particularly important to ensure gas-tightness of the electrolyte to keep the reference electrode isolated from the target gas. Another type of potentiometric sensors instead consists of two electrodes with different catalytic activity exposed to the same atmosphere, generating a potential difference due to kinetics effects.
- **Amperometric sensor**: the output signal is the limiting current due to mass transport or reaction kinetics. Here, rate-limiting elements (gas diffusion barriers) are used, e.g., small holes or porous coatings. The application of an external bias can be used to tune the chemical selectivity of the electrode reaction.

The most typical design for such sensors comprises a membrane electrolyte separating the two electrodes and the two atmospheres. The main advantage of using a solid electrolyte is therefore the possibility of miniaturization by implementing thin film technology, broadening the spectrum of possible applications for such devices. This approach would allow overcoming the main limitation of YSZ-based technology, i.e., high response time, maintaining the features that make it competitive among all sensing technologies, e.g., low cost and high sensitivity.

1.4.2 Miniaturized sensing devices

The miniaturization of electrochemical gas sensors does not simply allow to fabricate a small version of its macroscopic counterpart. Indeed, being the sensing mechanism based on electrode kinetics, the use of thin film micro-structured electrodes would improve the sensing performances and reproducibility compared to thick-film and porous electrolyte. Besides, the reduction of the electrolyte thickness enables sensing at a lower temperature range [74].

In the past, the most popular approach to miniaturize oxygen sensors included a solid-state reference electrode instead of a reference gas, thus enabling a planar electrodes configuration and a simpler fabrication process. Figure 1.14-a shows different patented designs from Croset and collaborators [75] based on planar configuration that take advantage of the low ionic resistance across the electrolyte. Based on the same configuration, Radhakrishnan et al [76] fabricated a series-connected array of potentiometric sensing units, increasing the voltage output by 8-fold compared to the output of a single unit.

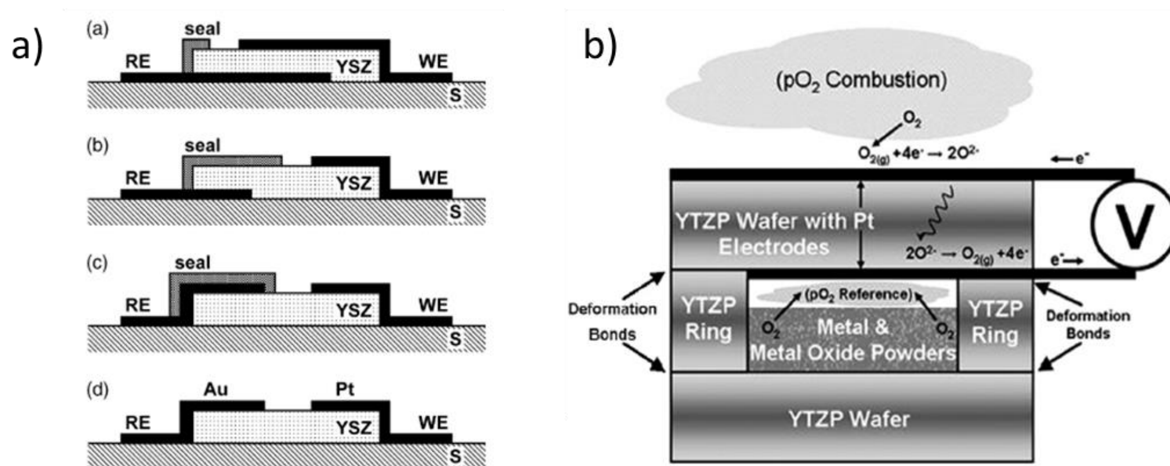


Figure 1.14. Potentiometric oxygen sensor designs: (a) planar configurations with different sensing approaches [75] *and (b) out-of-plane configuration with internal reference electrode and hermetic sealings* [77].

On the other hand, a different approach (Figure 1.14-b) enables the fabrication of a membrane-based electrochemical oxygen sensor that resembles the original bulk sensor design, but without the need of a reference gas. Here, the main challenge is to obtain a gas-tight sealed cavity comprising an internal reference electrode that would buffer any changes in the oxygen concentration in the cavity [78,79]. Morata *et al.* [80] patented in 2013 a silicon-based sensing platform for the miniaturization of solid-state oxygen sensors that perfectly matches with the concept above.

One thing all these sensor designs have in common is the choice on the electrode materials. Noble metals have always been the preferred electrode for oxygen sensing applications especially for their high catalytic activity, although their high cost and poor long-term stability (when in form of thin film) are the main drawbacks. Here, as for SOFC technology, replacing noble metals with MIEC materials wound drastically reduce the costs of production and moreover, the sensing area would be extended to the whole electrode's surface and not just to the TPBs (see Section 1.2.3.2). Here, high superficial area and porosity, together with the tuning of the electrode's microstructure are important to ensure fast and reliable sensor response.

Acceptor-doped perovskites with the formula $ATiO_3$ (A=Sr, Ca, Ba) has been first studied and pointed out for applications to sensing devices [81], demonstrating good oxygen exchange and conduction properties as well as flexibility towards other oxidizing species by carefully tuning the stoichiometry. Later, Shuk *et al.* [82] demonstrated the integration of $B_xCa_{1-x}MnO_3$ (B=La, Y) electrodes onto YSZ solid electrolytes and the quick response time, excellent stability and reproducibility. Nevertheless, to the best of our knowledge, the integration of semiconducting perovskite materials into thin-film electrochemical oxygen sensors has not been accomplished yet.

1.5 Objectives of this thesis

This thesis is devoted to the investigation, design, and exploration of potential strategies of industrial scale-up of thin film electrochemical devices for applications in micro-SOFC and oxygen sensing. The work is encompassed on the ULTRASOFC project (H2020-ERC-CG, grant agreement n. 681146), which aims to break the low temperature operating limits of micro-SOFCs, and translates the knowledge acquired to the fabrication of micro-SOFC components and miniaturized oxygen sensors.

The thesis is organized as follows:

- **Chapter 2** introduces the experimental techniques and methods adopted throughout the thesis. Among these, microfabrication mainstream processes used to fabricate the micro-devices are described in detail, while advanced thin film deposition like PLD and ALD are extensively discussed for their potential integration into scalable industrial processes.
- **Chapter 3** firstly investigates the layer-by-layer fabrication by conventional ALD of undoped $ZrO_{2-\delta}$ and the structural, morphological, and electrical properties of 20 nm-thick films. Suspended ceramic membranes were then fabricated combining the layer above with a YSZ-based electrolyte grown by PLD. Here, their out-of-plane resistance was characterized by impedance spectroscopy to assess their potential integration in micro-SOFC and electrochemical oxygen micro-sensors. Finally, a novel technique called Spatial ALD (SALD) was optimized to deposit, for the first time, pure CeO_2 thin films with potential applications in catalysis and energy conversion, drastically reducing the fabrication time and cost.
- **Chapter 4** illustrates an optimized route for high-throughput fabrication of micro-SOFC units based on large-area deposition techniques. Moreover, a new strategy to increase the active area per unit cell is presented, that is based on the growth of doped-Si slabs and circular membrane arrays. As for the materials selection, $La_{0.8}Sr_{0.2}CoO_3$ was chosen as cathode, YSZ and ALD-grown ZrO_2 as electrolyte, and $Ce_{0.8}Gd_{0.2}O_2$ as anode, with the addition of Au or Pt current collection thin films at the cathode side and anode side, respectively. A demonstration of the fuel cell performance was also included.
- **Chapter 5** aims at translating the knowledge obtained on materials and microfabrication processes to a different application, i.e., miniaturization of potentiometric oxygen sensors. Here, a new design and fabrication flow are presented, leading to the fabrication of Si-based platforms with doped-Si slabs that include ceramic membranes for sensing. An encapsulation method for stable high-temperature operation is also developed and applied to the fabrication of a fully integrated thin-film electrochemical oxygen sensor

by creating a reference chamber. The device is finally tested in real operating conditions and compared to a commercial sensor device based on bulk YSZ and noble metals (Pt).

- **Chapter 6** is devoted to the microfabrication of a complementary component of a micro-SOFC unit in the final power generator, namely a gas micro-reforming unit. After optimization of the wafer-level fabrication of the micro-reactor comprising more than 8000 microchannels, functionalization of the above was obtained by ALD, depositing Al_2O_3/Pt catalyst within high-aspect-ratio structures. The temperature effects on both DME steam reforming and partial oxidation were investigated, where eventually the micro-reformer was tested in real-life operating conditions for integration in a micro-power generator by efficient hybrid start-up of the reforming reaction.

As **Annex** of this thesis, the full design of a micro-SOFC based power generator is presented, including a fundamental component for stacking multiple cells, i.e., micro-interconnects, providing an easy method for microfluidic and electrical connections. Ceramic insulation holders were then 3D-printed by ceramic stereolithography for the functional characterization of a micro-SOFC stack, although some technological barriers were eventually found, and their full characterization was not possible.

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CHAPTER 2

EXPERIMENTAL METHODS

Experimental methods

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2.1 Introduction

In this thesis, technological challenges arise especially from the integration of different materials in form of thin films in a device operating at relatively high temperature. A combination of mainstream microfabrication processes with chemical and physical vapor deposition techniques is chosen for an easy and more reliable integration in the production line.

This chapter is dedicated to the description of the most relevant experimental techniques for fabrication and characterization of thin films and silicon-based devices adopted throughout this work. The first section of this chapter is dedicated to a detailed description of microfabrication methods, process parameters and thin film deposition of key materials used in this thesis. Afterwards, an entire section is dedicated to the encapsulation of microfabricated devices using 3D printing technologies. The third section introduces the main analytical techniques used to characterize deposited thin films including structural, chemical and morphological analyses. Finally, the functional characterization of the fabricated device is described.

2.2 Microfabrication processes

Microfabrication is commonly referred to those processes developed for micro-electromechanical systems (MEMS) fabrication [1]. In particular, MEMS are miniaturized devices including mechanical elements – cantilevers, membranes, cavities or channels – and/or electrical elements – semiconductors, dielectrics or metals – for a wide variety of applications such as in microelectronics and sensors industries [2].

Such fabrication represents one of the most promising approaches for the miniaturization of micro-SOFC power generators [3]. On one hand, the use of clean-room facilities leads to the standardization of the processes thus improving the reliability and reproducibility of samples fabrication. On the other hand, mainstream processes allow for a cheap large-scale mass production and easy integration in existent semiconductor industrial facilities.

Here, the miniaturization and the multiplicity of devices is achieved by performing processes on thin and large-area substrates. The most common substrate, silicon single crystal (100) wafers, is commercially available with thickness usually varying between 50 μm and 1 mm and the diameter between 2´´ (5 mm) and 6´´(15 mm). Indeed, silicon has been widely used since the 60's as a building block in the electronics industry because of its semiconducting properties, its chemical inertness and abundance on earth.

2.2.1 Clean-room processes

In this section, the main microfabrication processes carried out at IMB-CNM[1] clean-room facilities will be briefly described, as well as their main application to the fabrication approach

[1] Institute of Microelectronics of Barcelona is one of the three Microelectronic National Centers belonging to the Spanish National Research Council (CSIC). www.imb-cnm.csic.es

herein discussed. The fabrication approach for substrates micromachining is divided into three main techniques, namely (i) photolithography, (ii) etching and (iii) additive techniques.

Photolithography (i) is one of the main lithography methods applied to transfer a pattern from an optical mask to the photoresist *via* exposure to UV light. Typical steps of photolithography include spin coating of the photoresist on the substrate down to controlled thickness, optical exposure to UV light masking specific regions and development of the resist. The chemical properties of the resist change when it is exposed to radiation, and consequently its solubility to a proper solvent (developer): the irradiated regions become soluble if the photoresist is positive or *viceversa* if negative. Subsequent photolithographic steps with mask alignment leads to the so-called multi-step lithography for fabrication of silicon monoliths with complex structures. The size of the minimum feature that is possible to obtain in a device, called *critical dimension*, depends on the process applied and it is in the order of 1 μm in the case of the traditional optical lithography. Nevertheless, it is feasible to obtain nano-scale features by implementing nanofabrication techniques such as electron-beam lithography or atomic force microscopy lithography [4].

Following the photolithographic step, one may proceed by **etching (ii)**, hence physical or chemical removal of bulk material from the exposed regions. The main etching techniques are referred as wet or dry etching, depending on if the reaction occurs in aqueous solution or instead involves reactant gases in low pressure plasma. These two categories are then divided into *isotropical* or *anisotropical*, depending on the resulting profile in the etched region. Figure 2.1-a shows the four categories of etching methods abovementioned.

Nowadays, wet etching is mostly used for bulk micromachining of the substrate where precise control of the etch rates is desirable. Isotropic wet etching techniques are widely addressed to metal etching and the features obtained are strongly dependent on the thickness of the material to be etched. In fact, under-etching and under-cutting of materials typically occur for thicker structures.

On the other hand, anisotropic wet etching is a common process especially for bulk silicon micromachining. Potassium hydroxide (KOH) or tetramethylammonium hydroxide (TMAH) are typically used as etchant and silicon nitride as masking layer. In particular, KOH shows a faster etch rate and a higher anisotropy. The etch rate for silicon of a 30% KOH solution at 70 ºC in (1 0 0) directions is 0.8 μm/min, which is more than 150 times higher than in (1 1 1) directions. Besides, this technique creates features with a defined angle between (1 0 0) and (1 1 1) planes which is 54.7º. When KOH etching is employed, a silicon nitride masking layer is necessary to avoid dissolution of the mask [5].

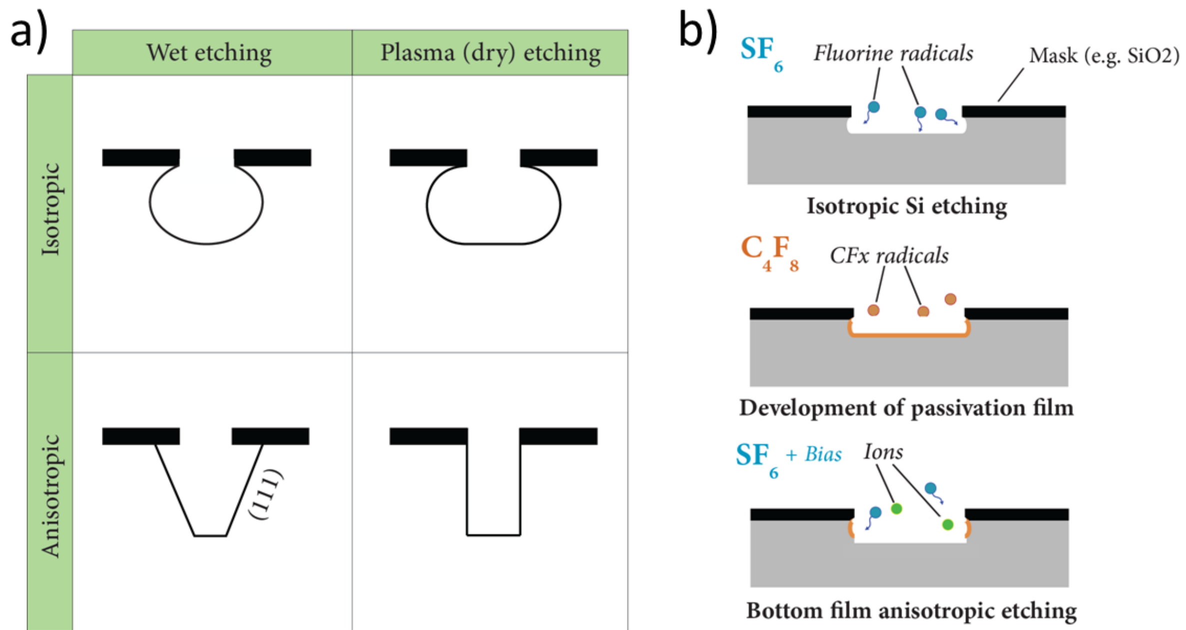

Figure 2.1. a) Visual representation of the effects of etching on a Si(100) substrate; b) Schematic view of the steps involved in the Bosch process (DRIE)

On the other hand, dry etching has evolved as an indispensable technique for miniaturization in the late 1990s and it may be divided into physical etching by ion bombardment, chemical through introducing reactive species at the surface or a mix of both.

The initial limits of this approach – for instance slow etch rates and inability to maintain the aspect-ratio after few tenths of microns – were overcome by the introduction of high-density ($10^{11}/cm^3$) plasma sources. It was thus possible to reach high etch rates while operating at low pressure (1 to 20 mTorr), increasing the ion directionality and reducing the microloading, i.e. the strong dependance of etch rates to the aspect-ratio of the feature to be etched.

Deep reactive-ion etching (DRIE) and more specifically the so-called Bosch process [6], is typically able to process up to 30:1 aspect-ratio structures where an etch rate of ~3 μm/min for Si is standard. In this process, sequential anisotropical etching (*80 sccm SF6, 6 s, 8W platen, 600 W coil, 33 mTorr*) and passivation (*85 sccm C4F8, 8 s, 0 W platen, 600 W coil, 16 mTorr*) steps are alternated, leading to the fabrication of high-quality structures such as micro-trenches, through-silicon-vias and micro-pillars, for instance [1]. The process is schematically depicted in Figure 2.1-b.

Besides wet or dry etching, typical post-lithography processes are those defined as **additive techniques (iii)**, usually consisting in the selective deposition of materials in determined regions. This group of techniques mainly includes thin-films deposition by physical or chemical methods and silicon doping by diffusion or ion implantation.

- In this work, a stress-free multilayer structure consisting of 100 nm of thermally grown SiO_2 and 300 nm of PECVD-deposited Si_3N_4 was fabricated on both sides of a silicon (1 0 0)-oriented single crystal wafer of 4'' diameter. This dielectric bilayer was used as a mask for most etching processes and the patterns were transferred to the substrate via photolithography (*Karl Süss MA6*). To this aim, optical glass/chromium masks were used and exposition to UV light of a photoresist HiPR 6512 from Fuji Film for about 30 seconds (photoresist thickness of 1.2 μm). Anisotropic KOH wet etching was

performed for bulk micromachining with a 40% solution and at 80 °C while RIE was performed in a AMS 100 equipment from Alcatel.

Typical characterization for the results of such processes performed at CNM clean-room facility includes profilometry, spectroscopic ellipsometry, optical interferometry and microscopy techniques, i.e., optical microscopy (OM), scanning electron microscopy (SEM) and atomic force microscopy (AFM). Further microfabrication processes performed outside the clean-room facility are described in the following sections.

2.2.2 Thin-film deposition of functional materials

2.2.2.1. Pulsed Laser Deposition

Pulsed laser deposition (PLD) is a versatile technique for thin-film deposition that can be easily integrated in silicon technology. It is based on laser ablation of a target material, usually in ultra-high vacuum (UHV) conditions, and its subsequent deposition on a substrate.

Figure 2.2 shows the PLD5000 system from PVD Products® installed at IREC, Barcelona and employed throughout this thesis for the fabrication of the functional oxides applied to the micro-SOFC system. Thus, PLD is a very important technique for the development of this thesis and its working principles are hereby briefly described.

Figure 2.2. a) Picture of the PLD equipment installed at IREC and b) detail of the vacuum chamber (number 3 in Figure 2.2-a)

The system, as shown in Figure 2.2, comprises a (**1**) KrF-based excimer laser (Lambda Physik COMPex PRO 205) which provides power ranging from 6 W to 248 W at a wavelength of 248 nm. The laser is focused by a set of optical components (**2**) including a focal lens and highly reflecting mirrors which redirect the beam to the target placed within the (**3**) UHV chamber. In spite the chamber is usually maintained at UHV conditions (~10^{-7} mTorr), during deposition a controlled atmosphere can be applied to the substrate region by flowing O_2 or Ar in the chamber. The motors (**4**) allow for an automated motion of the substrate Z position and rotation, as well as heater furnace motion. Finally, a loadlock chamber (**5**) is used to insert or extract the sample holder without breaking the UHV chamber vacuum [7].

Inside the chamber, the focused laser beam hits the target (**6**) and ablates a small amount of material creating a plasma plume which is thereby ejected perpendicular to the target surface and directed to the substrate (**7**) placed above it (at a controlled distance from the target), leading to its deposition by condensation [8].

One of the great advantages of PLD stands in the possibility of depositing crystalline thin films at a lower temperature than usually required by most oxide materials (above 1000 °C for solid-state reactions). For such reason and thus the possibility to avoid subsequent thermal treatments, the PLD system is especially suited for the fabrication of micro-SOFCs [9].

i. Main deposition parameters for thin film growth by PLD

The first relevant parameter for ceramic films growth by PLD is the temperature of the substrate, as temperature-dependent bulk diffusion phenomena are responsible for the resulting microstructure. Very low temperature setpoint leads to extensive porosity as the low surface diffusion favors random grain orientation. When the temperature setpoint T_S approaches $T_s = 0.5\ T_m$, where T_m is the melting temperature of the target, polycrystalline, smooth and dense films are obtained. Finally, for higher temperature setpoint the bulk diffusion leads to denser and crystalline films.

Moreover, the thin-film growth of complex oxides is performed under controlled atmosphere by introducing a gas flow while pumping – usually oxygen when growing oxides, which reduces the kinetic energy of the species in the plasma that would otherwise reach values of hundreds of eV and lead to the formation of the desired phase by providing O^{2-} anions for the film growth [7].

- In this work, the pressure in the chamber was varied between 1 and 200 mTorr with an inlet O_2 flow of 5-10 sccm in order to change the microstructure of the film. Lower pressure levels were set in combination with high temperatures (above 500 °C) to deposit dense and crystalline films, whereas higher pressure and lower temperatures (100 °C in this work) led to the growth of porous and amorphous films undergoing further post-deposition processing (annealing to temperature $T \geq T_{operation}$)

Further important parameters for PLD depositions are:

- target-to-substrate distance, usually proportional to the plume size and in this work fixed to 90 mm;
- Spot size, i.e., the area of the target hit by the laser, and laser fluence, i.e. the laser energy per area unit, which define the growth rate for a given material, in this work varied between 0.2 - 0.4 J/cm^2. The laser pulsing frequency was fixed at 10 Hz.

ii. Large-area deposition by PLD

The PLD5000 system described above is specifically designed for large-area depositions (100 mm in diameter), a fundamental feature for the integration in MEMS process flows. With this aim, the optical transmission system is designed to change the relative positions of its components in a way that allows focusing the beam at different spots of the target while maintaining the same spot size and laser fluence. This raster movement of the mirror is usually coupled with the

absolute motion and/or rotation of the target, as discussed below. The relative motion between the plume along one axis and the rotation of the substrate eventually allow for a film deposition on a large-area substrate. A schematic representation of the mirror rastering for large area deposition is included in Figure 2.3.

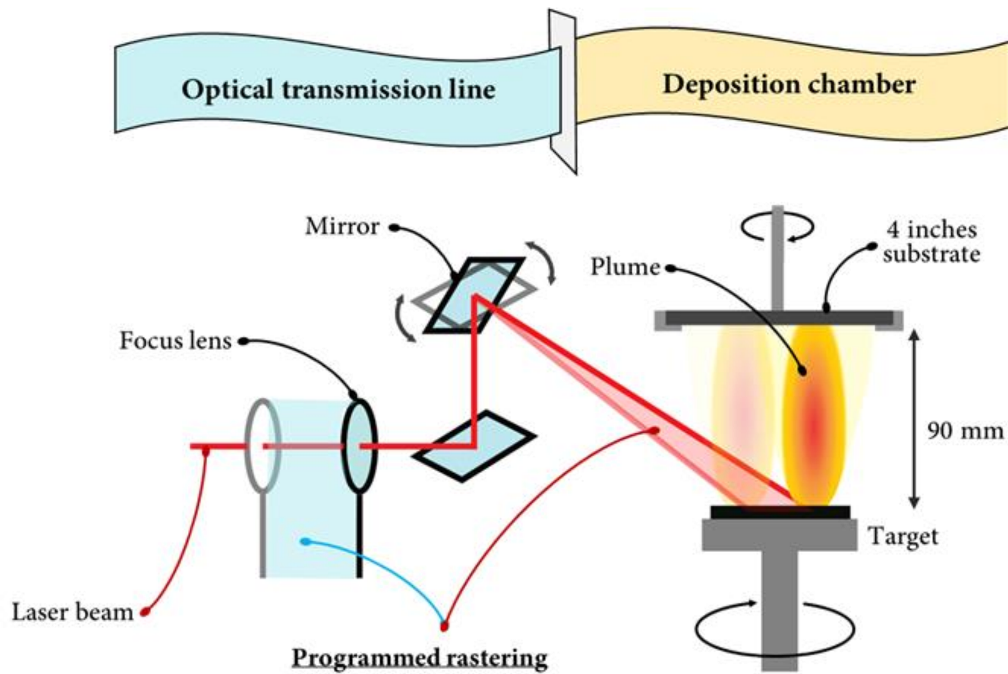

Figure 2.3. Schematic view of the PLD transmission line and chamber for large-area depositions

During large-area depositions, the rastering parameters were carefully optimized to avoid or reduce the number of defects that may appear on a target upon ablation. In general, non-optimal target ablation may affect the target by gross deformation, cones formation on the surface, exfoliation or even stress-induced target breakdown. For such reason, a rotation was always applied to the target and the scan rate of the laser over the target surface was maintained high. These conditions together with careful target polishing led to a better quality of the films by reducing the number of particles ejected upon ablation, which would eventually lead to cracks and pinholes formation in the thin film.

- In this work, the deposition of functional ceramic films for application in micro-SOFCs has been performed by PLD at 4 inches wafer level. A proper mirror rastering has been proposed where the scanning velocity at positions corresponding to the center of the wafer where about three orders of magnitude higher than for the ones corresponding to the side. Every target was polished and pre-ablated before deposition for at least 3000 laser pulses. The substrate rotation was fixed at 8 rpm while the target rotation to 15 rpm.
- On the other hand, target rotation and rastering with constant mirror position were applied for deposition of electrodes thin films on single 10 x 10 mm^2 chips of YSZ (100) single crystal substrates (up to 8 at the same time using a homemade substrate holder) for their electrochemical characterization on symmetric cells.

iii. Residual stress analysis of deposited films

The fabrication of mechanical structures at the micro-scale is not free of challenges. In the case of suspended membranes, it is necessary to tune and thoroughly characterize the residual stress in the deposited films as it is an important parameter for the successful fabrication of thermos-mechanically stable membranes.

The residual stress in a film deposited by PLD is directly correlated to the kinetic energy of the ionic species in the plasma that eventually condense into a film [10]. In the case of YSZ, a compressive residual stress was observed when the kinetic energy of the plasma species was high enough to cause atomic impingement on the substrate's surface. On the other hand, tensile residual stress was found when the chamber pressure was not sufficiently low or the laser fluence was not high enough and it inevitably led to a breakage during the release of the free-standing membranes by dry etching process.

- In this work, the characterization of the residual stress on the large-area thin-films was performed by wafer curvature measurements with a Confocal Scanning Optical Microscope (CSOM) 3D PLu Neox Optical from Sensofar. The wafer is measured before and after PLD deposition and the resulting profile is then fitted to obtain the radius of curvature at the center of the wafer. The latter is the input to the Stoney equation reported below for the calculation of thin-film residual stress on wafers, a method presented by Janssen et al. [11]

$$\sigma_f t_f = \frac{h^2}{6(s_{11} + s_{12})R}$$

where σ_f is the in-plane stress component in the film, t_f the thickness of the film, h the wafer thickness and $R = (1/R_f - 1/R_{sub})$ being R_f and R_{sub} the curvature radii of the substrate after and before deposition, respectively. Whereas s_{ij} are elements of the compliance tensor of silicon, the numerical value for $1/(s_{11}+s_{12})$ is 1.803(1)×1011 Nm^{-2} based on the stiffness values found in literature.

2.2.2.2 Atomic Layer Deposition

Atomic layer deposition (ALD) has emerged as an important deposition technique for the semiconductor industry and is nowadays employed in many processes where uniform coating and controlled thickness are critical requirements.
In particular, ALD is a special chemical vapor deposition technique where atomic layers are deposited through self-limiting surface reactions. Here, a metal-organic precursor is pulsed into the chamber through a carrier gas – usually N_2 – and reacts with the substrate's surface through a chemisorption saturation process. A second precursor (oxidant) is then pulsed into the chamber and reacts with the first one through surface chemical reaction, leading to the formation of the desired phase. Purging steps with an inert gas are always alternated to a precursor pulsing step to eliminate the molecules in excess that have not reacted with the exposed surface. The sequence of the four steps described above is called ALD cycle, and the case model for Al_2O_3 is schematically depicted in Figure 2.4.

Nowadays, ALD has been employed for the thin film deposition of many different compounds including oxides, nitrides, sulfides, phosphates and carbonates for a wide variety of applications [12]. Its unique properties of self-limiting reactions allow for a precise atomic control of the thickness and a very homogeneous deposition over large areas, which is an attractive feature for the deposition of electrolyte materials for instance or for uniform coating of high-aspect-ratio structures [13–16]

- In this work, ALD has been used to fabricate pure ZrO_2 thin films (called Oxygen Vacancies-Stabilized Zirconia - OVSZ) for application in micro-SOFCs and electrochemical oxygen sensors. The details of the fabrication processes are described in the following section. Moreover, it has also been employed to deposit a Al_2O_3/Pt -based catalyst as a uniform coating within high-aspect-ratio micro-channels for application in micro-reactor technology.

i. Chemistry of precursors

A clear understanding of the chemistry of the precursors is critical for ALD processes, as a successful self-limiting reaction may be obtained when complete saturation of the reactive sites at the substrate's surface is achieved.

Organo-metallic precursors are usually monomers or dimers, containing one or two atoms of a metal (M) and one or more ligands (L), written as ML_n or M_2L_n where n = 1,2,3,4,5,6. The most typical families of organo-metallic precursors are summarized in Figure 2.4, also comprising a schematic illustration of the ALD cycle for the deposition of alumina, extensively studied in literature and considered a model reaction [17].
The deposition parameters strongly depend on the precursor selected, since the presented compounds have different reactivity and are considered stable within different temperature windows. A suitable ALD window include a range of temperature from which the precursor is more volatile (starts evaporating or sublimating) until the temperature at which it degrades. Finally, the growth mechanism can vary depending on the chemistry of the chosen metal precursor (reactivity, steric hindrance etc.) and the properties of the adsorbent surface (especially the presence of hydroxyl groups).

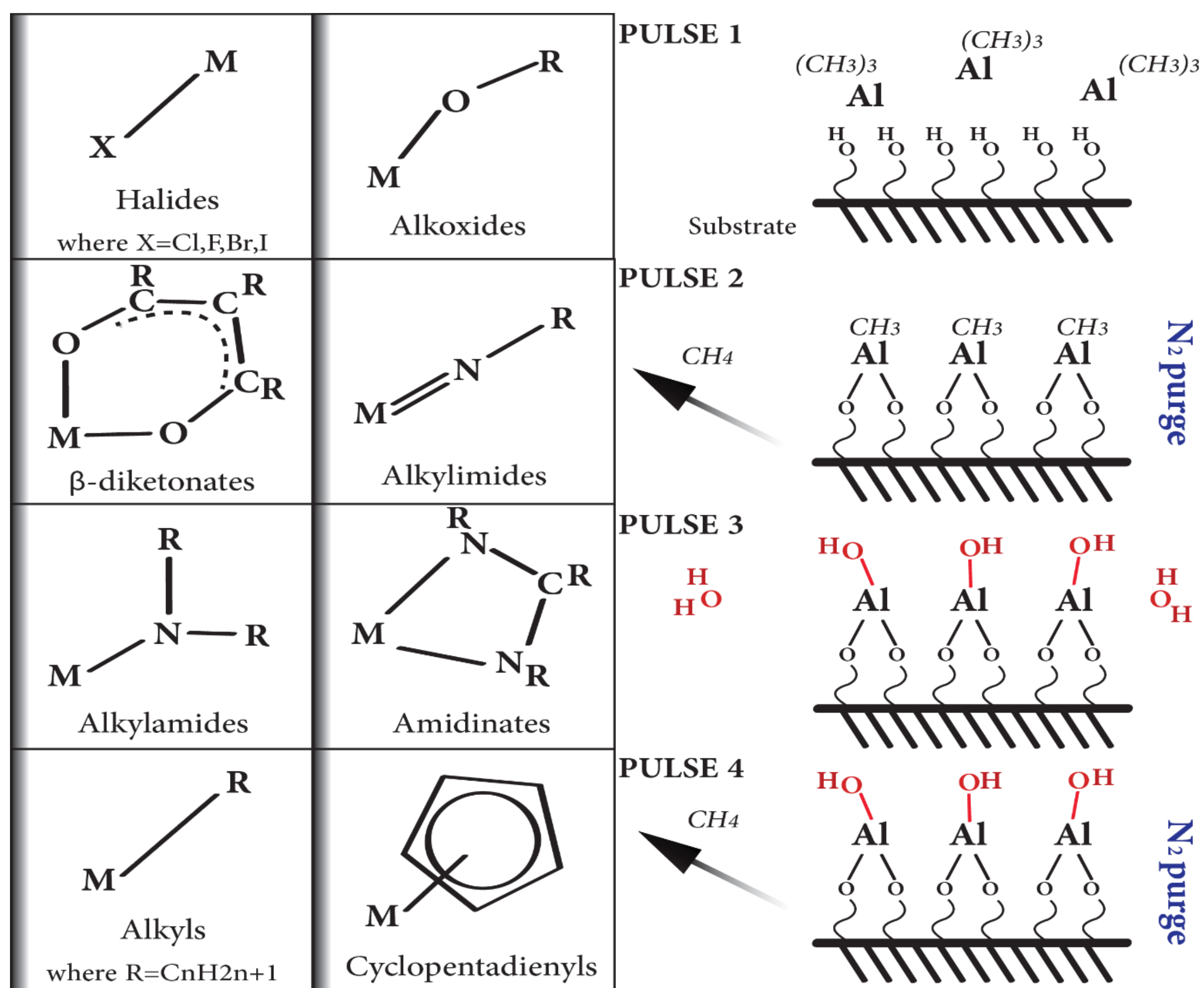

Figure 2.4. Types of metal-organic precursors for ALD and schematic view of the self-limiting reaction model for Al_2O_3 deposition

- <u>In this work</u>, the aluminum precursor chosen for Al_2O_3 deposition was the metal alkyl trimethylaluminium (TMA), 97% of purity and purchased by Sigma-Aldrich. No external heating was applied to the cylinder containing the precursor as it is very volatile at room temperature. The chosen co-reactant was H_2O.
- The platinum precursor chosen in this study was the metal cyclopentadienyl (Trimethyl)methylcyclopentadienyl platinum(IV), 99% pure and purchased from Strem Chemicals. Here, O_2 was used as co-reactant. The precursor cylinder was maintained at 80 °C to ensure partial sublimation of the white powder.
- OVSZ was deposited alternating pulses of the metal amide precursor Tetrakis(methylethylamino)zirconium(IV), or TEMAZ, 99% pure and purchased from Strem Chemicals, and H_2O. The precursor cylinder was kept at 135 °C to ensure partial evaporation of the light-yellow liquid.

ii. ALD deposition conditions for large-area substrates

A homogeneous coating on large-area substrates or on high-aspect-ratio structures is ensured by ALD as long as the reactor design allows for uniform thermalization of the substrate and the

sources of precursors are well separated. It is the case for the industrial ALD system used in this study, i.e., a R-200 Standard system from PicoSUN®. Figure 2.5 reports the optical image of the system with its components and a detailed view of the main reactor chamber.

Figure 2.5. Optical image of a) industrial ALD system from PicoSun used in this work, b) the wafer holder and reactor chamber and c) cylinders and gas lines for the precursors.

- In this work, the deposition of the alumina and platinum coatings was performed on Si (100) with a native SiO_2 surface for the sake of characterization. On the other hand, the micro-machined wafers containing more than 50 micro-reformer units were directly placed in the ALD reactor chamber on top of another silicon wafer, aiming at shielding the two sides in contact with each other from coating (see chapter 6). The reactor chamber was kept at 300 °C for both processes.

  For alumina, each ALD cycle consisted of a 0.1 sec pulse of TMA, 6 sec purge step with N_2, 0.1 sec pulse of H_2O and again 6 sec purge step. After initial calibration of the Growth per Cycle (GPC) rate, 1200 ALD cycles were repeated to obtain a thickness of about 100 nm.

  Calibration of the GPC was not performed for platinum since an island-like growth was observed within the micro-channels of the MEMS micro-reactor. A single ALD cycle consisted of 0.8 sec pulse of platinum precursor alternated to 1 sec pulse of O_2 and with 12 sec of N_2 purge in between. 80 ALD cycles were eventually carried out to obtain an array of nanoparticles grafted onto the alumina support and resulting in 1%wt metal loading with respect to the active support.

  Finally, OVSZ thin films were deposited onto silicon wafer substrates already embedding on both sides a dielectric bilayer consisting of 100 nm of SiO_2 and 300 nm of Si_3N_4. The reactor chamber was kept at 250 °C and an ALD cycle consisted of 2 sec pulses of TEMAZ, followed by 12 sec of N_2 purge, 0.2 sec pulse of H_2O and 12 sec of N_2 purge. 220 ALD cycles resulted in coatings of about 20 nm.

Most oxide materials deposited by ALD at low temperature are found to be amorphous, often finding applications such as gas diffusion barriers, while depositions at higher temperature can result in crystalline film deposition. In the case of Al_2O_3, all films grown by ALD below 500 °C are amorphous and a thermal annealing is required to obtain a crystalline structure [18].

Rapid Thermal Processing (RTP) is a suitable thermal processing method for microelectronics, allowing fast annealing (and subsequent lower activation energy for crystallization or sintering) of a MEMS device without affecting thermo-mechanically the embedded features in the device, or maintaining a smaller particle size because of the reduced diffusion [19]. The process consists of the fast heating of a specimen through infra-red radiation by applying a certain power to IR lamps.

- In this work, a RTP As-One from Annealsys was used for the thermal treatment of amorphous alumina films deposited by ALD. Here, the samples placed in a susceptor tungsten holder and heated to 500 °C with a 50% power setpoint and dwelled for 15 seconds. Subsequently, a ramp rate of 15 °C/sec was applied up to the temperature setpoint chosen (800 to 1000 °C in this study) and the dwelling fixed to 90 seconds. Cooling is obtained by slowly reducing the power of the IR lamps during about 3 minutes. Inert gas (N_2) was flowed through the chamber during the process.

2.2.2.3 Spatial Atomic Layer Deposition

In the last decade, there has been an increasing interest in ALD processes due to the high quality and unique properties of the film obtained with this technique, described in the previous section. Despite this success, the conventional ALD presents two main drawbacks that limit its application for large-scale industrial processes: first, the growth rate is usually very low – about two orders of magnitude lower than CVD – and second, the process is usually carried out under vacuum conditions, making it more expensive to scale-up [20].

The concept that was proposed to overcome these issues is the so-called *Spatial* ALD, that is very promising due to its simplicity and high deposition rates achieved. The working principle of spatial ALD (SALD), also known as Atmospheric ALD (AALD), is the same as for the conventional approach but instead of the temporal separation of precursors through alternate pulses, the precursors are continuously fed to the substrate in between inert gas regions. A thin film is thus grown alternatively exposing the substrate to the different inlet regions *via* its oscillatory motion, as shown in Figure 2.6 [21].

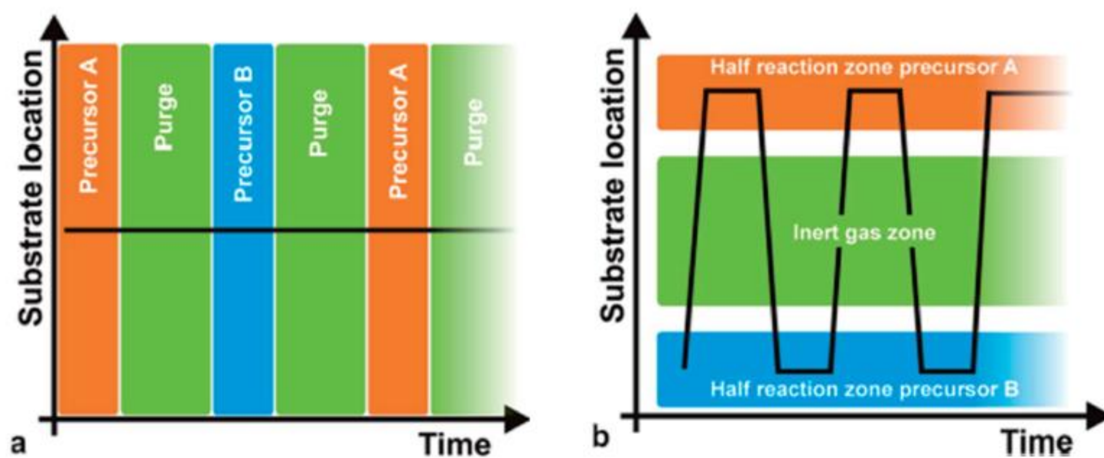

Figure 2.6. Comparison of pulsing steps and substrate location in time between a) ALD process and b) SALD process. Image from ref. [21]

In spite some issues may arise from ambient pressure deposition techniques, such as the presence of impurities, SALD has been proved as an effective technique to fabricate high-quality conformal thin films with precise control of the thickness and increased deposition rates compared to other approaches. So far, this technique has been employed for the fabrication of semiconducting materials for solar cells applications – for instance Al_2O_3, TiO_2, ZnO, Ga-doped ZnO, Cu_2O – while the plasma-enhanced PE-SALD has been recently demonstrated [22] for the fabrication of ZrO_2.

- In this work, SALD experiments were conducted at Laboratorie des Materiaux et du Genie Physique (LMGP) facility in Grenoble INP, France, during an external mobility stay. Home-made SALD II system consisted of a hot plate reaching temperatures as high as 350 °C and capable of performing an oscillating motion with tunable velocity and acceleration. Six mass flow controllers are used to feed N_2 either to the precursor cylinders or to the gas dilution lines in a range between 10 to 3000 sccm. A 3D-printed head nozzle containing microfluidic channels was used to spatially separate the precursors lines and to directing the gas flows to the substrate. The Ce precursor cylinder (bubbler) was designed and fabricated in stainless steel to provide uniform heating and hermeticity (see Figure 2.7-a). The whole system is placed inside an enclosed hood for safety reasons and showed in Figure 2.7-b.

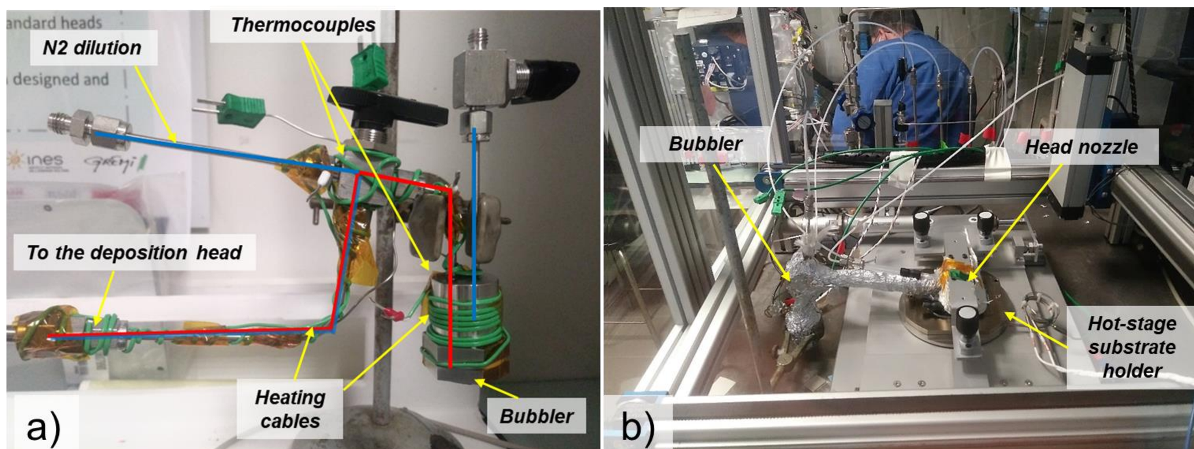

Figure 2.7. (a) Optical image of the cerium precursor cylinder (bubbler) and heating setup; (b) optical image of the SALD chamber and main components.

In the next sections, the experimental approach for the development of CeO_2 thin films by SALD is presented.

i. Deposition conditions for pure CeO_2

The deposition of CeO_2 thin films by SALD requires a non-toxic metal-organic precursor since the process is performed in open air conditions. Tetrakis(2,2,6,6-tetramethyl-3,5-heptanedionato)cerium(IV) also known as $Ce(thd)_4$ was chosen for this reason.

Nevertheless, a TGA study found in literature [23] reported the sublimation temperature of such precursor around 200 °C or above when maintained at atmospheric pressure, as shown in Figure 2.8. Uniform heating of the cylinder (containing the precursor) and of the rest of the fluidic

system was thus required to avoid condensation in the gas lines, making the whole process non-trivial.

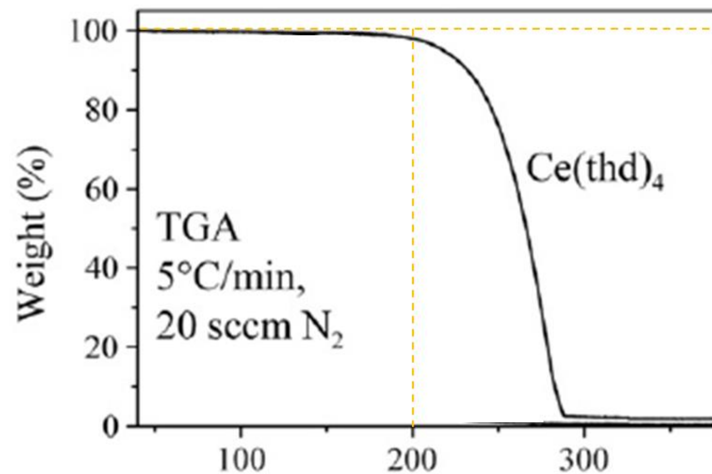

Figure 2.8. TGA analysis of cerium β-diketonate precursor, extracted from [23]

A compact and functional stainless-steel cylinder was fabricated (Figure 2.7-a) and the length of the metallic tubing reduced at the minimum necessary to avoid cold spots. Dilution of the precursor gas flow was necessary to achieve typical SALD flow rates.

- In this work, 0.3 g of $Ce(thd)_4$ powder precursor from Strem Chemicals is placed inside the customized cylinder and sealed with a PTFE flat gasket. The flow rate of N_2 in the precursor line was fixed to 120 sccm and ratio with the set to 3:2, while the overall flow rates for each line was fixed to 200 sccm. H_2O was employed as co-reactant and the ratio of N2 in water and dilution was fixed to 1:1. An external power source was connected to a heating wire that was used to maintain the bubbler and the gas line to a temperature of 220 °C and 200 °C, respectively. Finally, the substrate temperature was kept at 350 °C in order to heat up the deposition head as well, kept at 150 µm distance from the substrate.

2.3 Encapsulation of high-temperature micro-devices

For micro-devices, encapsulation is an important step as it allows the functional unit to be employed in real operating conditions, especially by providing a more mechanically stable structure as well as important features such as electrical and gas connections and gas-tight sealings. Encapsulation methods usually include wafer bonding (e.g., fusion, eutectic or anodic bonding, glass frits etc.), multichip alignment and stacking (e.g., flip chip technique) and eventually the packaging (integration in the final hardware comprising the housing and related functional features)[24].

- In this work, these processes were performed at chip-level after separating the functional units from the wafer using a DISCO DAD322 automatic dicing saw machine. The chips size is 1x1 cm2 and the further encapsulation processes are explained in the next sections.

2.3.1 Robocasting for glass frit bonding

In microfabrication, many bonding methods have been developed throughout the years and each one of them find a specific application as they present advantages and drawbacks. In this work, the fabrication limits imposed by the chosen materials are (i) temperature treatments lower than 800 °C, limit at which extended metal de-wetting would occur or the mechanically stability of the micro-structures would collapse, and (ii) low mechanical pressure.

The bonding technique that was selected for this application is called low-temperature melting glass bonding, also known as glass frit bonding, and it typically consists of the deposition of a glass-ceramic-based paste between two surfaces and the subsequent thermal process, called firing, to obtain the seal. This technique adapts well to different substrates and even rough surfaces, forming a strong sealing that is stable in different atmosphere (e.g., corrosive environment) and, more importantly, that is gas-tight.

- In this work, driven by the selection criteria discussed above the lead-free G018-197 passivation glass powder was purchased from SCHOTT®. The composition of the powder is reported in Table 2.1. The glass powder was mechanically mixed with the R008//311006 binder (97% terpineol and 3% Elvacite®) purchased from Fuel Cells Materials using a Thinky ARE-250 mixing and degassing machine. The powder to binder ratio was fixed to 4:1, that was the highest powder load still resulting in a homogeneous slurry extrudable by robocasting. The rheological behavior of the paste was characterized at IREC with a Visco 88 viscosimeter from Bohlin.

Chemical composition	
Compound	Amount (wt.%)
B_2O_3	10-50
Bi_2O_3	1-10
CeO_2	0.1-1
Sb_2O_3	0.1-1
SiO_2	1-10
ZnO	>50

Table 2.1. Chemical composition of the glass frit powder purchased from SCHOTT.

Among suitable methods to deposit pastes or slurries thick films with optimal control on thickness and width, screen-printing and robocasting are certainly the preferred approaches. The latter was chosen for the scope of this thesis as it allows for precise deposition without affecting or damaging any features present on the substrate, adapting the deposition path to any desired shape.

- <u>In this work</u>, a V-one PCB printer from VOLTERA (Figure 2.9) installed at IREC was used to deposit the glass frit paste by syringe extrusion through nozzles with diameter size of 300 µm. The substrate was then placed on a hot-plate at 80 °C for 5 minutes to evaporate the organic solvent and the joint was obtained by stacking two chips that were then placed in a furnace with a weight (about 0.2 Kg/cm^2) on top.

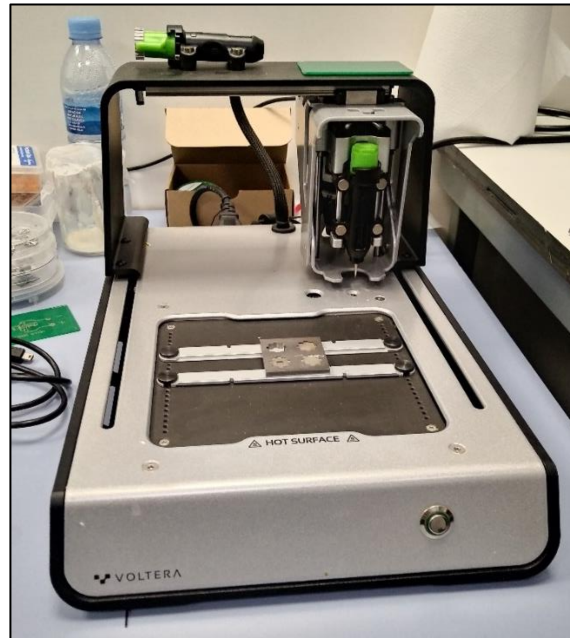

Figure 2.9. Optical image of the V-one PCB printer located at IREC and used to deposit the glass frit sealing

Finally, a thorough characterization of the glass powder and formulated paste was necessary to find a proper temperature profile for the thermal treatment upon encapsulation. The thermal treatment can indeed affect the quality and properties of the sealing such as its Thermal Expansion Coefficient (TEC). A proper characterization of the hermeticity and mechanical stability of the sealing was thus needed as well.

- In this work, Differential Scanning Calorimetry (DSC) measurements were performed with a TG-DSC Sensys Evo system from Setaram, measuring the heat exchange of a 15 mg glass powder sample from RT to 800 °C temperature range. In-situ thermal X-ray diffraction (see section 2.3.2) was used characterize the evolution of the crystallinity of the glass frit upon annealing. Hot-stage microscopy (HSM), EDX and dilatometry were performed at Politecnico di Torino facilites. Finally, the quality of the joint is visually controlled by SEM at IREC and X-ray inspection using a Nordson Quadra inspection machine located at IFAE (Institut de Fisica d'Altes Energies), Barcelona.
-

2.3.2 3D printing of high-aspect ratio ceramic parts

In the last decade additive manufacturing (AM) has strongly modified the industrial production in those sectors where complex shapes were not achievable otherwise. It consists in the addition of material layer-by-layer – from which its name – following a computer-aided design (CAD) model.

3D printing of polymers is the most common additive manufacturing technique and different methods have been developed worldwide and many equipment commercialized. Among these, fused deposition modeling (FDM) and stereolithography (SLA) are now mainstream technologies [26]. The former consists in the extrusion of a thermal plastic filament through a nozzle that reaches the fusion temperature of the given polymer, and its subsequent deposition according to a specific pattern (Figure 2.10-a). The latter instead uses a laser to trigger

photochemical processes that eventually lead to the cross-linking of monomers and oligomers to form polymers. Therefore, scanning of the laser in a layer-by-layer fashion allows to create 3D objects (Figure 2.10-b)

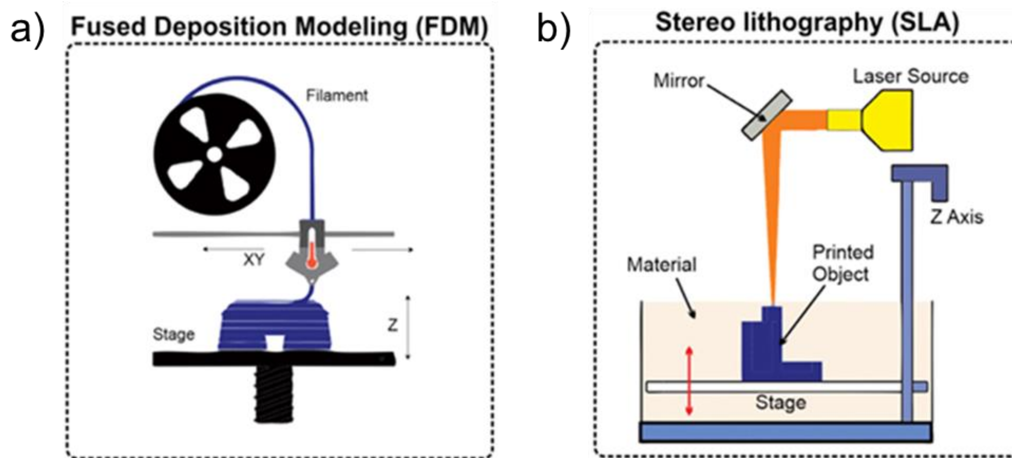

Figure 2.10. Schematic view of different polymer 3D printing techniques, extracted from [27]*: (a) Fused deposition modeling and (b) Stereolithography.*

Moreover, SLA has recently emerged as an effective technique to manufacture metal, glass and ceramic-based materials besides polymers. In the case of ceramics, photosensitive polymers are mixed with ceramic fine powders aiming to a rheological behavior compatible with tape casting techniques. Once the first layer of the paste is casted with two blades of controlled thickness on a platform, a laser is selectively polymerizing the slurry and the successive layer is then tape casted on top of the first, printing the object layer by layer by repeating the cycle. The object is finally cleaned from residual paste with a special solvent and thermally treated to remove the binder and sinter the ceramic particles, obtaining a dense and robust structure. This process already finds application in energy-related fields [28,29] and it is schematically depicted in Figure 2.11.

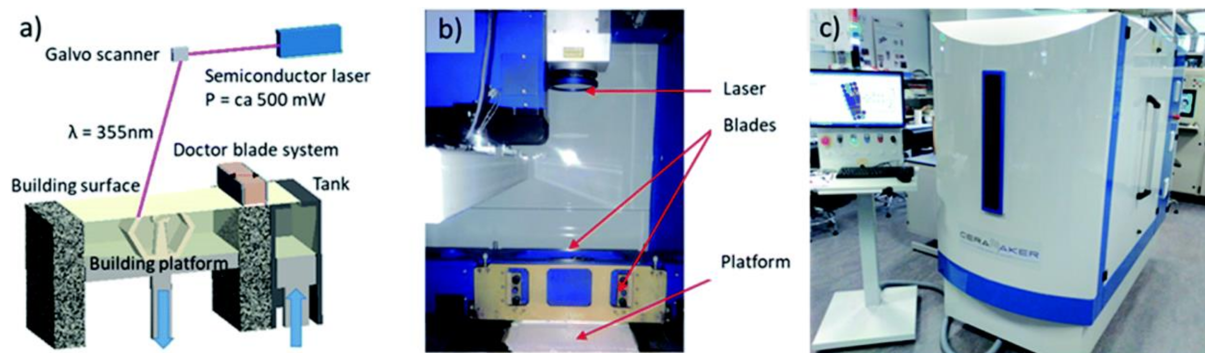

Figure 2.11. Ceramaker setup adapted from ref. [29]. *a) Schematic view of the 3D printer building platform, b) optical image of the main components of the printer and c) optical image of the Ceramaker located at IREC.*

- <u>In this work</u>, a CERAMAKER 3D printer from 3DCERAM was used to fabricate reactors and holders for the micro-SOFC device testing and packaging. Computer Assisted Design (CAD) software was employed to sketch substrates holders and housings for the high-temperature experimental set-ups. STL files were automatically created by using DMC software to slice the design and control the 3D printer. A solvent-free UV-

photocurable slurry composed by Al_2O_3 ceramic powder, acrylate UV curable monomer, photoinitiator and dispersant was employed. After deposition of the photocurable slurry, a UV semiconductor laser (power around 500 mW) focused on the building platform reproduces, slice by slice, the pattern designed by CAD using mirror rastering with a speed of 5000 mm/s. This process (lowering the platform, supplying the slurry and cure by laser rastering) is repeated as many times as layers of 50 μm (blade height) are required to generate the desired three-dimensional structure. At the end of the printing process, the uncured paste was removed from the platform for extracting the consolidated pieces. Clean parts were thermally treated for about 6 h in inert atmosphere up to 1250 ºC to eliminate the organics without crack formation within the green bodies. Subsequently, sintering of the pieces at 1550 °C for 3 h (heating and cooling rate of 2 ºC/min) in oxidizing atmosphere generating a dense ceramic piece of alumina.

2.4 Thin-film characterization techniques

In this section, the main thin film characterization techniques applied throughout the thesis are described. These techniques provide tools for the structural, morphological, optical and electronic characterization of the thin films aiming to extensively understand their behavior under operating conditions.

2.4.1 Ellipsometry

Spectroscopic ellipsometry is an optical spectroscopy technique often used in thin films as it provides a non-destructive way to characterize structural and optical properties such as the film's thickness and the refractive index for instance. Here, the variation of polarization of a white and linearly polarized light beam that is reflected by the thin-film surface is measured by placing a monochromator before the detector. The results so obtained are then fitted and compared to a model to extrapolate the physical properties. A schematic representation of this working principle is included in Figure 2.12.

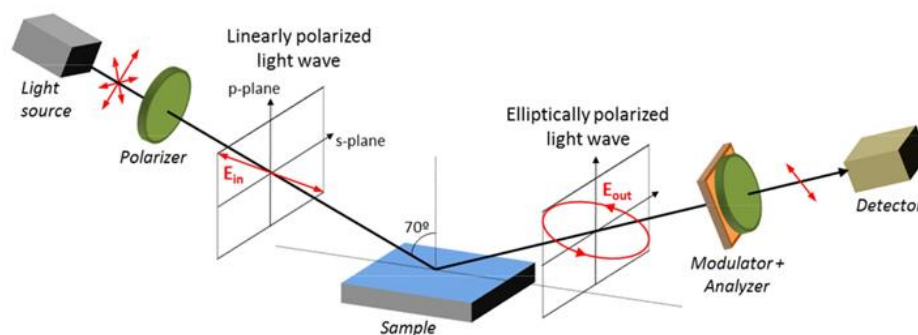

Figure 2.12. Typical scheme of the ellipsometry setup and operation principle, from [30]

- In this work, ellipsometry measurements were performed on thin-film structures after deposition in order to characterize their thickness, or after thermal treatments to observe

any changes of optical properties. A UVISEL plus equipment from Horiba scientific was used, with a spectral range 0.6 - 5.6 eV. The light incidence angle was fixed at 70°, while modulator and analyser were fixed at 0° and 45° respectively. The system was calibrated prior measurement with a Si (100) thermally oxidized substrate. Modelling was performed with a DeltaPsi2 software from Horiba.

2.4.2 X-Ray Diffraction

X-ray diffraction is the most common structural characterization technique used to define the crystal lattice and thus the corresponding phase of a material either in the form of powder, pellet or thin films. The technique is non-destructive since it consists of shining an X-ray beam on the material and analyzing the diffraction pattern generated by the elastic scattering of the X-rays with its lattice planes. Indeed, the resulting pattern presents a unique combination of reflections and their intensities that is unique for each crystalline phase of any material, therefore enabling compositional analyses, phase identifications, crystallite size and more.

- <u>In this work</u>, a BRUKER D8 ADVANCED with a Cu source (lambda = 1.5406 Å) and located at IREC, Barcelona (Figure 2.13-a) was used to perform $\theta/2\theta$ measurements with a Bragg-Brentano geometry or imposing a 1.5° θ-offset to reduce the contribution of the single crystal substrates. Most of the characterization was carried out at ambient temperature but in certain cases a temperature-controlled stage was mounted to perform in-situ measurements up to 800 °C. Grazing Incident angle XRD (GIXRD) was performed with a X'Pert Pro MRD-Panalytical with a Cu source (lambda) and located at CCiTUB, University of Barcelona (Figure 2.13-b). The incident angle was optimized for each sample to values of ω = 0.3°-0.4°.

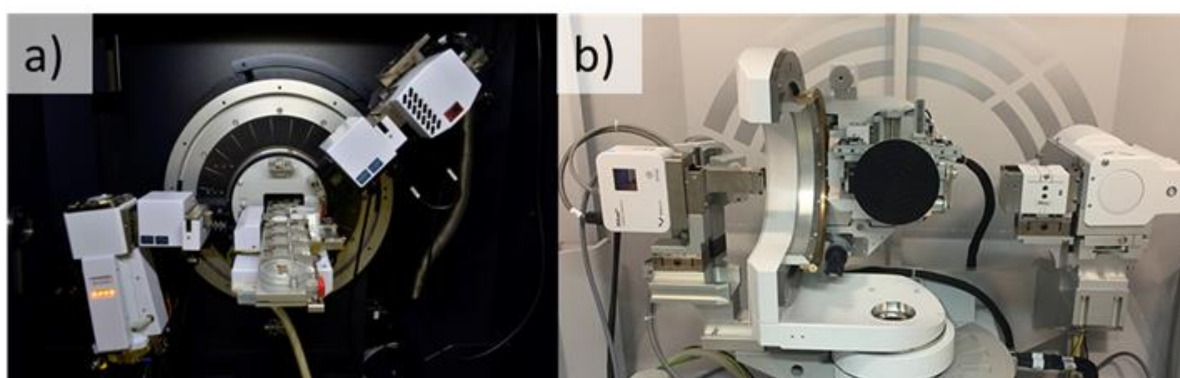

Figure 2.13. Optical images of the X-ray diffraction equipment used throughout the thesis. a) Bruker D8 located at IREC, used for theta/2theta and offset measurements, and b) X'Pert Pro MRD at Universidad de Barcelona, used for GIXRD measurements

2.4.3 Atomic Force Microscopy

Atomic force microscopy is used to characterize the topology of a surface by scanning a sharp probe (i.e., cantilever) on the samples surface and measuring the Z displacement of the tip with

a nano-scale resolution. To preserve the integrity of the sample, usually the characterization is performed in tapping mode [31]. Here, the operating principle is based on Van der Waals interaction between the tip and the sample's surface that makes the tip vibrate at a specific resonance frequency. This frequency changes depending on the distance between the tip and the surface. Then, a feedback control sends signals to the piezoelectric stage to adjust the samples Z position to maintain it fixed. Finally, a laser reflected on the tip hits a photoelectrode detector that catches these variations and generates an image of the scanned surface.

- In this work, AFM (XE15-AFM from Park Systems, located at IREC) was used in tapping mode to analyze the grain size distribution and roughness of OVSZ thin films as-deposited by ALD and after annealing at 700 °C for 6 hours.

2.4.4 Scanning Electron Microscopy and Energy Dispersive X-ray Spectrometry

Scanning Electron Microscopy (SEM) is the most common technique for microstructural characterization. It provides high resolution images of either samples surface or cross-section of the samples analyzed under vacuum conditions (10^{-4} to 10^{-5} mbar).

Here, an electron beam is generated by accelerating the electrons emitted from a tungsten cathode towards an anode and the beam is then focused by condenser lenses into a spot of 1-5 nm size, which is scanned over the surface of the sample to create an image. The signal analyzed by the detectors can provide morphological information when secondary electrons are collected, i.e., the products of inelastic scattering interaction emitted with low energy, meaning the signal is usually coming from the surface. On the other hand, backscattered electrons detection offers compositional information as they are the products of the elastic scattering interaction, emitted with higher energy than secondary electrons but dependent on the atomic composition of the specimen. Finally, images generated with a mixture of the abovementioned signals can be also generated using an InLens detector.

On the other hand, many electron microscopies comprise detectors for Energy Dispersive X-ray Analysis (EDX or EDS) used for both quantitative and qualitative analysis. Such detectors measure the x-rays emitted by a material when irradiated by an electron beam, whose photon energy depends on the orbital electron transitions and are thus characteristic for a specific element.

- In this work, a ZEISS Auriga microscope located wither at IREC (Figure 2.14) and at IMB-CNM facilities were used to characterize the results of the microfabrication processes performed as well as the microstructure of the thin films deposited by PLD at IREC. Secondary electrons, backscattering electrons and InLens detectors were usually employed in these measurements. Here, voltages values between 3 and 20 kV were applied. EDX measurements were taken after calibration on Si or Cu metals.

Figure 2.14. Scanning Electron Microscope AURIGA from Zeiss, located at IREC

2.4.5 X-ray Photoelectron Spectroscopy

X-ray photoelectron spectroscopy (XPS) is a surface analysis technique used for compositional characterization. Here, a sample's surface is irradiated with x-rays and the photoelectrons generated from this interaction are collected by a detector. In particular, the kinetic energy of these photoelectrons is measured from which the binding energy is calculated – a parameter strongly related to the chemical composition of the sample. This technique is usually performed under UHV conditions (about 10^{-9} mbar) to increase the mean free path of the photoelectrons emitted by the sample.

- In this work, a SAGE-HR SPECS XPS equipment located at Universidad de Barcelona was used by Dr. Lorenzo Calvo to perform measurements on OVSZ samples fabricated by ALD before and after annealing in different atmospheres. A general spectrum was first recorded and subsequently the high-resolution spectra of C^{1s}, O^{1s} and Zr^{3d} were measured.
- Moreover, XPS analysis on CeO_2 thin films fabricated at LMGP laboratory (INP Grenoble) was performed on samples as-deposited and after 10 seconds of Ar sputtering, recording the Ce^{3d}, C^{1s} and O^{1s} spectra.

2.4.6 Electrical characterization techniques

In this work, the electrical properties of the thin films deposited were characterized either by (i) electrochemical impedance spectroscopy (EIS) or (ii) in-plane DC measurements. The former was mostly used in this work to model the contribution of the different component of a complex system to the total resistance. These measurements were performed both in-plane and out-of-plane configurations. On the other hand, in-plane DC measurements were used to measure the total conductivity of a film or bulk systems in some cases.

2.4.6.1 Electrochemical Impedance Spectroscopy (EIS)

Electrochemical impedance spectroscopy (EIS) or AC impedance, is a technique often applied to the characterization of electrodes processes and complex interfaces. In particular, this technique analyzes the system time-response to the application of a periodic small-amplitude ac signal. This technique thus provides a powerful tool for the separation of the contribution of each component to the total resistance of the system.

The impedance as a function of the frequency applied Z(w) can be written as the ratio between voltage applied and current measured, both variable in time. The current function usually presents a phase shift θ compared to the voltage input function. Expressing this term as a sum of real and imaginary part, it is possible to obtain the following formula:

$$Z(\omega) = \frac{E(t)}{\mathrm{I(t)}} = |Z|e^{(-i\theta)} = Z'(\omega) - iZ''(\omega)$$

Representing the real part versus the imaginary part is the most common way to present the measurements, on the so-called Nyquist plots. Here, different semicircles usually appear for each process occurring in the system, e.g., electronic or ionic conduction, charge transfer or mass transport. Each of these processes are characterized by a specific time constant $\tau = 1/RC$. The most common way to study these data is thus fitting these semicircles with RC circuits, either in series or in parallel with each other, each representative of a different reaction occurring in the sample [32].

- In this work, thin film-based fuel cells or its single components (electrodes, electrolytes or barrier layers) where electrically characterized by EIS at IREC laboratory. A Novocontrol Alpha-A High performance frequency analyzer was used for EIS measurements applying a voltage amplitude range between 10 and 50 mV and scanning frequencies ranging from 10^6 to 0.1 Hz. Fitting of the EIS data was carried out with ZView software. Two configurations were adopted throughout this thesis (Figure 2.15)
- (1) in-plane measurements were carried out in a Linkam probe station (THMS600, Figure 2.17-a), consisting of a hot-stage (temperature up to 600 ºC), a chamber with controlled atmosphere and four conductive tips for electrical contact. Here, OVSZ thin films (20 nm) deposited by ALD on sapphire (0001) substrates were tested by EIS with patterning of thin-films microelectrodes in both oxidizing and reducing atmosphere.
- (2) out-of-plane measurements were performed in a Probostat cell (Figure 2.17-b), providing electrical connections and controlled atmospheres in separate chambers made of ceramic tubes placed in a high-temperature furnace. The electrodes tested in the Probostat cell were deposited on both sides of YSZ (001) single crystal substrates in a symmetric configuration (and symmetric atmosphere, either synthetic air or 5%-H_2/Ar).

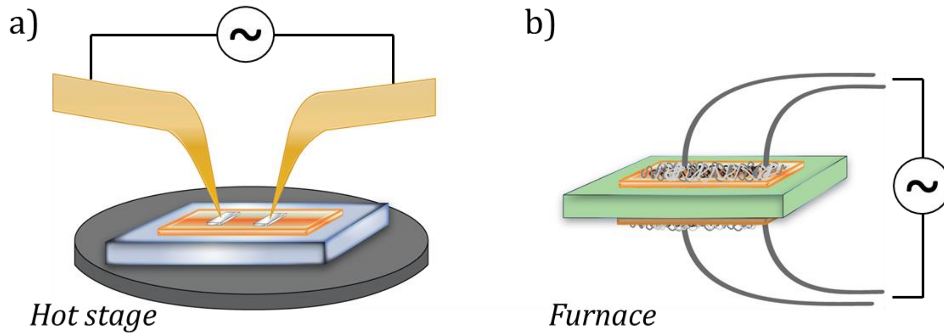

Figure 2.15. Common experimental configurations for EIS measurements. a) in-plane measurement of thin films on insulating substrates; b) out-of-plane measurement on electrochemical cells (YSZ 001 single crystal substrate) with symmetric electrodes and current collecting gold (or platinum) grids

2.4.6.2 In-plane DC measurements

DC measurements are common tool for the direct measurement of the total conductivity of a material without distinction among the electrochemical processes occurring in the system. Van Der Pauw configuration was adopted in this work, allowing to measure electrodes regardless the shape, if some conditions are fulfilled – namely: (i) the film must be homogeneous in thickness and composition; (ii) the electrical contacts must be at least one order of magnitude smaller than the sample, and (iii) the thickness of the film must be far smaller than the lateral size.

The geometry applied in this work is shown in Figure 2.16, where four contact electrodes are placed at the corners of the samples. When a current is applied between A and B contacts (I_{AB}), a certain voltage is measured between C and D (V_{CD}). The resistance R_0 can be defined as the ratio between the values V_{CD}/I_{AB}, whereas a second resistance R_v can be calculated by repeating the measurement changing the polarity and contact side.

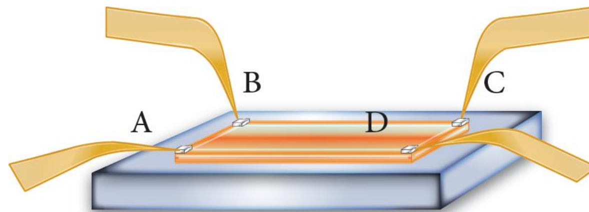

Figure 2.16. Schematic illustration of the electric measurement setup according to the Van Der Pauw method

According to the Van Der Pauw method modified taking into account the difference between R_0 and R_v caused by sample heterogeneities (considering a dimensionless factor f depending on the ratio R_0/R_v), the resistivity of a film can be calculated as follows [33]:

$$\rho = \frac{\pi d}{ln2}\frac{(R_0 + R_v)}{2} f(\frac{Rv}{R0})$$

where d is the film thickness and f the abovementioned dimensionless factor.

- In this work, Van Der Pauw method was applied to assess the resistivity of current collecting films based on evaporated platinum and gold on top of ceramic electrodes. 1x1 cm^2 silicon chips with a SiO_2/Si_3N_4 dielectric bilayer were used as a substrate and a YSZ/LSC or YSZ/CGO bilayers deposited by PLD on top. Finally, 100 nm-thick current collector films (Au and Pt for cathode and anode, respectively) are evaporated on top, and their resistivity measured over time and increasing temperature in oxidizing /reducing atmosphere to assess their integration in micro-SOFC devices.

2.5 Functional characterization of devices

In this section, the functional characterization techniques for multilayer structures and devices under operating conditions are presented. In particular, the experimental methods applied for the characterization of the micro-SOFC components and the electrochemical oxygen sensors are described.

2.5.1 Micro-SOFC and O_2 sensor electrical characterization

As already mentioned in chapter 1, the overall performance of a fuel cells is usually tested by measuring the IV curve, i.e. measuring the current flow (I) between two electrodes when different voltage values (V) are applied (potentiostatic measurement) or viceversa (galvanostatic measurement), from which it is possible to extrapolate the power output of the cell as P = V • I (W) or the specific power density (W/cm^2) as a function of the operating temperature. Similarly, by forcing the current flow to be negligible (up to a few nA) it is possible to measure the open circuit voltage (OCV) of the cell when H_2 and O_2 atmospheres were directed to the cell's anode and cathode, respectively.

- In this work, potentiostatic measurements were carried out on a Probostat cell within which micro-fuel cells (LSC/YSZ/OVSZ/CGO) are mounted, and the two chambers were hermetically sealed using Ceramabond paste from Aremco. A Parstat (2273 Advanced Electrochemical System) was used to perform such experiments, recording either IV or EIS curves (see section 2.3.6.*i*). Humidified (3% H_2O) Ar/5%-H_2 gas was used as a feed to the anode side and synthetic air to the cathode side, where the gas flows were controlled by mass flow controllers (Bronkhorst).

The oxygen sensor was tested in a similar way but controlling the oxygen partial pressure in one chamber while setting a reference atmosphere (inert gas) in the other one. The voltage response of the sensor can be described by Nernst equation:

$$\Delta E = \frac{RT}{4F} ln \frac{P^0_{O2,ref}}{P^0_{O2,meas}}$$

- In this work, solid-state electrochemical gas sensors (LSC/YSZ/OVSZ/LSC) were tested in a MicroXact CPS- HT station to simulate operation in a real environment.

The oxygen partial pressure was controlled with a SGM5EL elektrolysis device from Zirox GmbH both at the inlet and the outlet of the chamber. Voltage and time responses were measured with a Keithley 2520 multimeter by setting a negligible current between the two electrodes and measuring the OCV response to changing atmosphere.

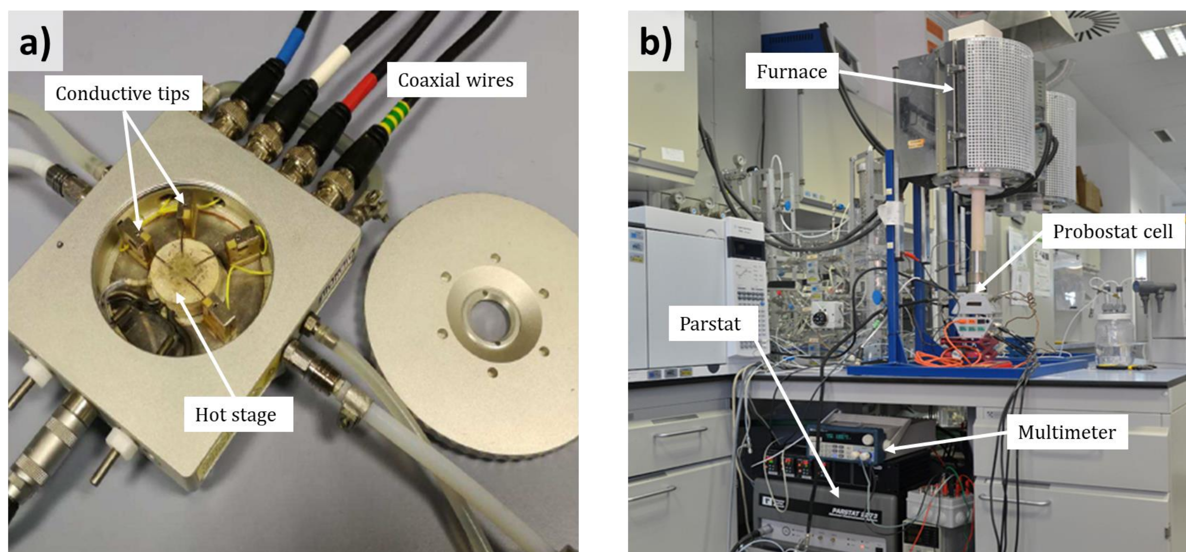

Figure 2.17. Equipment for electric measurements: a) Linkam THMS600 for in-plane measurements and b) Probostat cell for cross-plane measurements of functional thin films, fuel cells and sensors

2.5.2 Gas Chromatography

The characterization of chemical reactions where gaseous species are involved is usually carried out via gas chromatography. In this technique, a carrier inert gas is used to drive a gas mixture to the chromatograph where it is injected in the capillary columns. These components are coated with a stationary phase that interacts with the gas species retaining it for a specific time. This output is called retention time and is used for qualitative analysis. On the other hand, the detector response can be used for quantitative analysis by integrating the area of the peaks in the GC spectrum, where the detector response (usually reads μV) is plotted versus the retention time.

- In this work, a μ-GC 3000A equipment from Agilens Technologies located at INTE-UPC was used to characterize the dimethyl ether reforming reactions through the micro-reformer device. The chromatographer was equipped with PLOT U, Stabilwax and 5 Å Molsieve columns for a complete analysis of the products contained either in the effluent of the reactor or stored in special gas sampling bags for 24h, that was eventually injected in the chromatographer. The gas flows were regulated by a mass flow controller, while the amount of steam needed for steam reforming reactions was obtained by letting an inert gas (Ar) flow through a bubbler kept at 50 °C and the water vapor pressure calculated with the Riedel equation [34]. A cold trap was placed at the reactor's outlet to prevent water condensation in the capillary columns. A minimum gas flow of 15 ml/min was set to enable such measurements.

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CHAPTER 3

THIN CERAMIC FUNCTIONAL LAYERS FOR ENERGY CONVERSION AND SENSING

Thin ceramic functional layers for energy conversion and sensing

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3.1. Introduction

This chapter is devoted to the description and characterization of functional ceramic thin films deposited using different techniques, aiming at their integration in miniaturized devices for energy conversion and gas sensing. A unique combination of advanced techniques for thin films deposition is hereby presented, with the objective of defining scalable routes for the integration of ceramic films in microfabricated devices.

On one hand, state-of-the-art materials were selected and their large-area deposition by Pulsed Laser Deposition (PLD) was optimized starting from commercial targets (pellets) and adjusting the deposition parameters to obtain uniform films with a controlled morphology and electrical properties (see Chapter 2.2.2.1.2). On the other hand, the large-area deposition of functional thin films with reduced number of macro-defects was addressed by advanced chemical vapor deposition methods such as Atomic Layer Deposition (ALD) and Spatial Atomic Layer Deposition (SALD).

The results hereby presented are the building blocks necessary for the fabrication of highly performing micro-devices for power generation and sensing, allowing for the integration of ceramic thin films on micro-machined silicon platforms.

3.2. Large area deposition of thin ceramic functional layers by PLD

In this section, the large-area PLD deposition of ceramic materials onto 4-inches substrates was applied to the fabrication of high-quality electrodes and electrolytes for applications in micro-SOCs and gas sensors. One of the greatest advantages of PLD stands in its flexibility towards the fabrication of thin films with different morphologies, either dense or amorphous, and showing crystalline or amorphous structures depending on the deposition conditions chosen.

For instance, dense and crystalline electrolytes based on YSZ were typically obtained by PLD and showed promising performances for application in thin films devices [1–4]. Moreover, many studies can be found in literature about the PLD deposition of Mixed Ionic-Electronic Conductors (MIEC) materials such as $La_xSr_{1-x}MO_3$ (where M=Co, Mn, Fe etc.) for efficient Oxygen Reduction Reaction (ORR) [5–8], or fuel electrodes and catalysts based on doped-CeO_2 for Hydrogen Oxidation Reaction (HOR) [2,9].

In the following, commercial targets were purchased and the PLD deposition conditions were optimized to obtain homogeneous films on large substrates suitable for operation at high temperatures.

3.2.1 Electrolyte

The electrolyte material chosen for this application is $(Y_2O_3)_{0.03}(ZrO_2)_{0.97}O_{2-\delta}$ (3YSZ) as a high temperature anionic electrolyte well-known in literature. This target material was chosen over the 8YSZ counterpart due to reduced number of particles ejected during deposition [10] (see Figure 3.). Moreover, it was found that the compressive stress resulting from 3YSZ films was

found to be about twice higher than the one measured for 8YSZ films (1.58 GPa vs. 0.87 GPa), improving the buckling of the membranes and reducing the probability of rupture upon RIE. Further characterization of the residual stress is presented in Chapter 4.3.2.

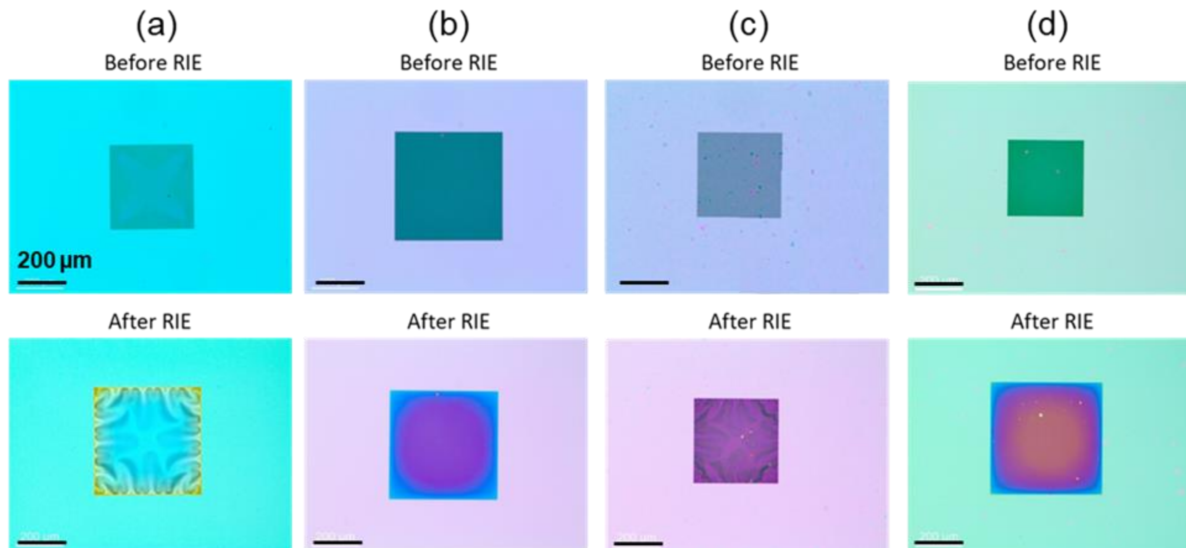

Figure 3.1. Optical images of (a) compressive and (b) tensile 3YSZ, and (c) compressive and (b) tensile 8YSZ-based membranes before and after RIE.

Optimization of the mirror rastering parameters at the PLD equipment was necessary to obtain a uniform film across the whole wafer surface. Figure 3.2 below represents the thickness of the film obtained through 125.000 laser pulses and measured by ellipsometry. The average calculated thickness was 132(±3.5) nm, resulting in a growth rate of about 0.63 nm/min on a 4-inches silicon wafer.

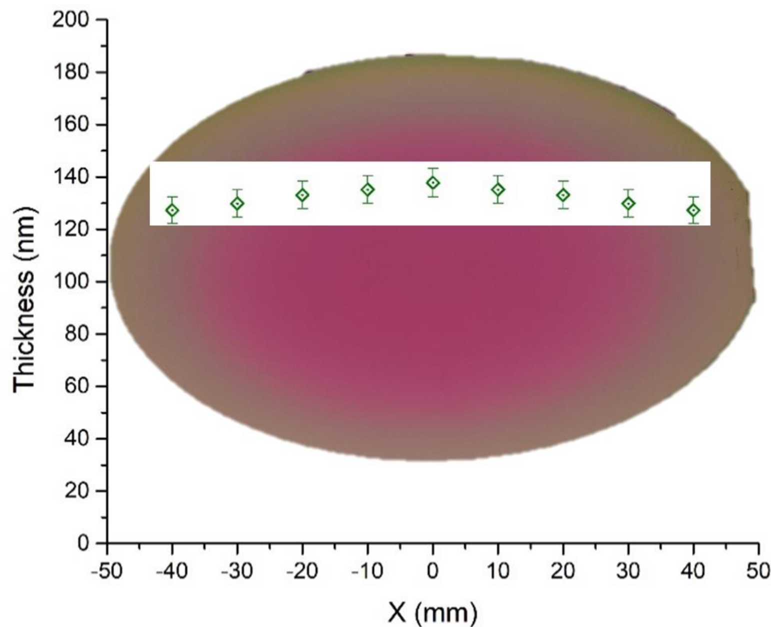

Figure 3.2. Ellipsometry measurement along the wafer diameter of the thickness of the 3YSZ film deposited by PLD

XRD measurements were performed on samples after deposition and the resulting pattern is included in Figure 3.3, showing the polycrystalline nature of the film with no preferential

orientation. Indeed, YSZ films grown by PLD on silicon or amorphous substrates are known to be polycrystalline with a columnar microstructure [4]. The peaks are indexed matching the cubic phase of YSZ (JCPDS 27-0997).

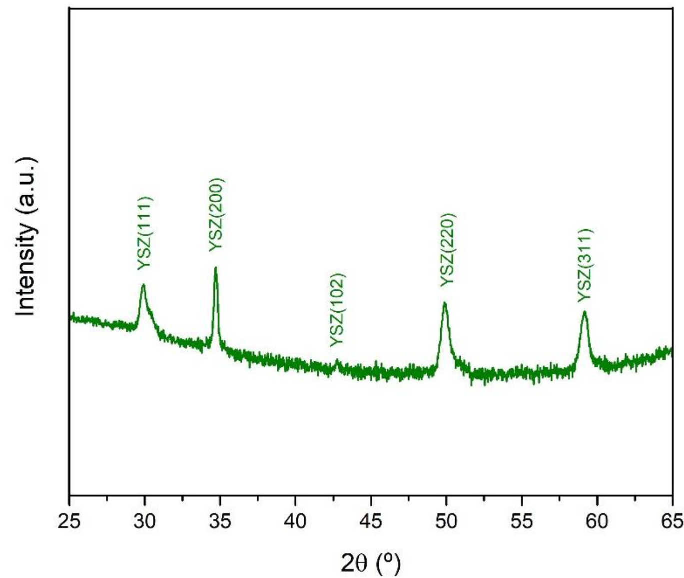

Figure 3.3. XRD pattern of the 3YSZ film as-deposited at 500 °C by PLD

Because of the presence of pinholes originating from the PLD deposition, the addition of an auxiliary thin layer deposited by ALD was necessary to obtain a more reliable electrolyte and its electrochemical characterization is reported in Chapter 3.3.1.b.

3.2.2. Electrodes

3.2.2.1 Air electrode

The air electrode chosen hereby for application in micro-SOFCs and gas sensing is based on $La_{0.8}Sr_{0.2}CoO_{3-\delta}$ (LSC) perovskite oxide that is meant to be deposited onto the YSZ electrolyte. In this section, the main goal was the optimization of the deposition conditions for large area substrates to obtain a homogeneous coating of an air electrode for oxygen reduction reaction (ORR), while two different morphologies are targeted: porous and dense LSC electrode. Indeed, porous electrodes are usually preferred in SOFC as they provide better access of the gas to the TPBs, but they can suffer from poor in-plane electrical conductivity [11]. Dense MIEC thin film can otherwise solve this problem also extending the TPBs to the whole surface area of the film. Nevertheless, CTE mismatch and residual stresses can be causes of cracks and delamination [12].

First, calibration of the growth rate and homogeneity of the film thickness were checked using ellipsometry in-plane mapping. Figure 3.4 shows the film thickness for the porous and dense LSC electrodes obtained using similar mirror rastering parameters. Considering the average film thickness along the wafer diameter, the growth rate calculated for the porous electrode was

found to be around 1.07x10^{-3} nm/pulse, i.e., 0.6 nm/min across the whole wafer's surface area. Conversely, the growth rate for the dense electrode was found to be about 4 times higher, i.e., around 2.52 nm/min. Finally, a rastering cycle to cover entirely the wafer takes about 270 seconds that results in an average of 2.7 nm or 11.3 nm-thick films for the porous and dense layers, respectively.

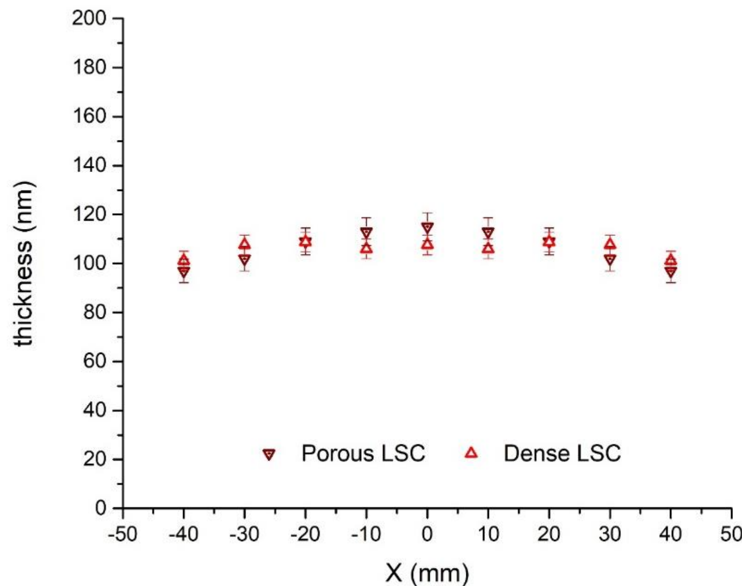

Figure 3.4. Ellipsometry measurement along the wafer diameter of the thickness of the LSC film (dense or porous) deposited by PLD

While the as-deposited film was found to be amorphous due to the low temperature setpoint chosen, annealing of the same at 700 °C for 3 hours was subsequently performed to obtain a crystalline phase. The annealed film is found polycrystalline with the (100) and (110) preferential orientations when deposited either on silicon or YSZ (001) substrates.

On the other hand, the high-temperature deposition of the dense LSC electrode yielded a crystalline film with need for further thermal treatments. The XRD pattern shown in Figure 3.5 indeed reports the (110) and (200) peaks of the cubic perovskite phase associated to LSC (JCPDS 48-0121) deposited on the YSZ thin film electrolyte during the fabrication of a micro-SOFC. Secondary peaks appearing in the pattern belong to undesired reflections from the Si(100) substrate.

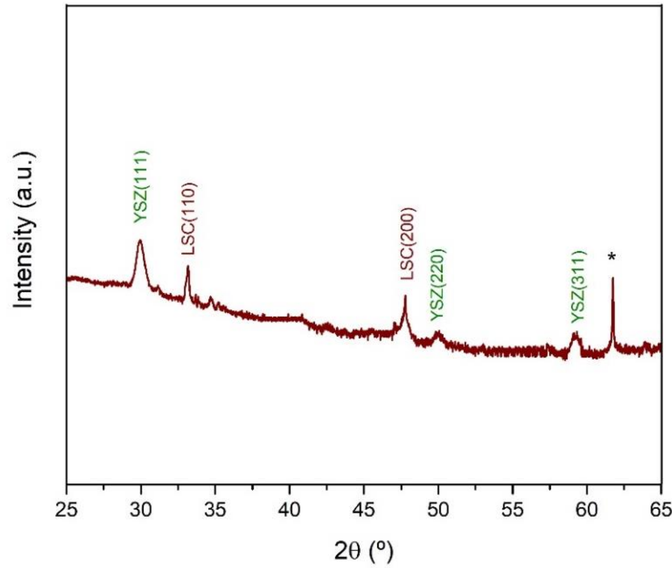

*Figure 3.5. XRD pattern of the LSC thin film deposited onto a YSZ film. *Si secondary reflections*

In order to characterize the electrochemical response of the two electrodes, symmetrical cells of LSC/YSZ/LSC were fabricated. In this regard, a 100 nm-thick LSC film is deposited on both sides of a YSZ (001) single crystal substrate, and the symmetric cell tested in oxygen atmosphere with gold paste current collector. Figure 3.6 reports the Arrhenius plot obtained by EIS including the polarization measurements for dense LSC, porous LSC and CGO_{BL}/LSC bilayer deposited at different conditions. In this latter, the CGO plays the role of a barrier layer meant to separate the Sr-rich cathode with the YSZ-based electrolyte with a ultra-thin (about 5 nm) layer of $Ce_{0.8}Gd_{0.2}O_2$, preventing the formation of deleterious strontium and lanthanum zirconates [13].

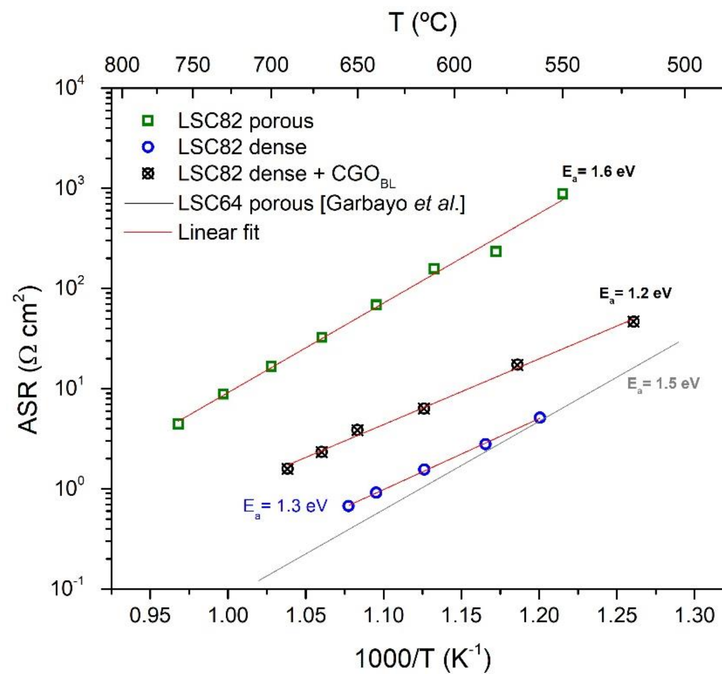

Figure 3.6. Arrhenius plot including the ASR (left Y-axis) and conductivity (right Y-axis) measured as a function of the temperature for 100 nm-thick films. LSC64 reference value was extracted from [7].

Figure 3.6 compiles the electrochemical performance of the different symmetrical cells fabricated. In particular, Figure 3.6 is an Arrhenius plot of the area specific resistance of the electrode and electrode-electrolyte interface as obtained from equivalent circuit fitting of the EIS data, included in Figure3.7. Here, the equivalent circuit model used for fitting includes a serial resistance (Rs) and two RC circuits, accounting for the contribution of the polarization (pol) and interfacial (if) charge-transfer phenomena.

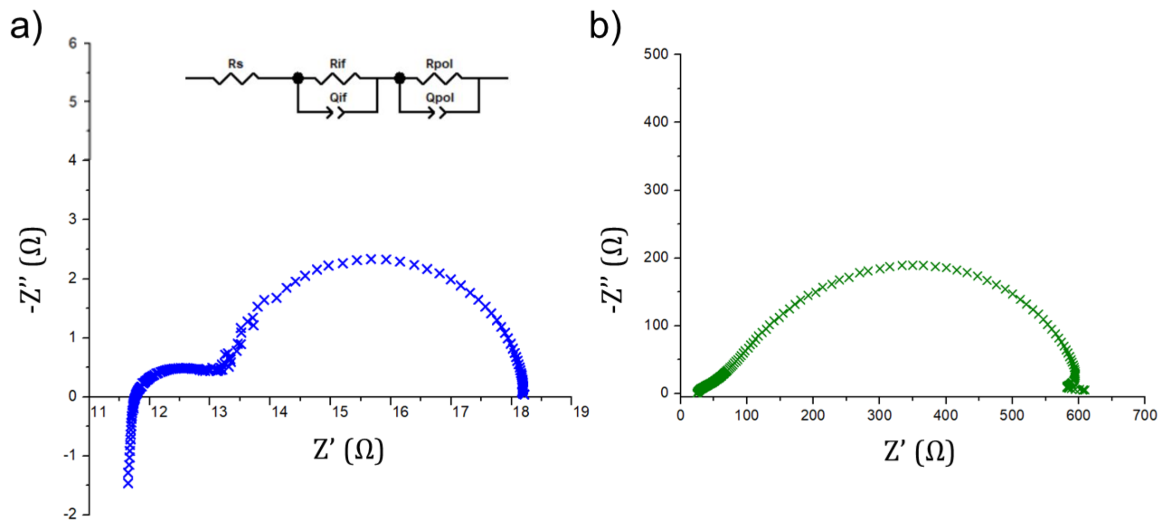

Figure 3.7. Nyquist plots obtained from the EIS measurements on (a) dense and (b) porous LSC electrodes at T = 620 ºC, including the equivalent circuit for fitting

Comparing the activation energies for the ORR reported in the graph, it is noticeable that porous materials show higher values of about 1.5-1.6 eV compared to the activation energy of the dense samples, that was found in the range of 1.2-1.3 eV. These results and the analysis of the impedance spectra obtained seem to suggest that the porous LSC layer is dominated by the oxygen surface exchange and shows higher electronic resistance, while the dense electrode is partially dominated by oxygen diffusion but shows higher in-plane electrical conductivity. Therefore, dense LSC films (≤100 nm) will be used to fabricate a micro-SOFC unit on large-area substrates.

Finally, the addition of the CGO barrier layer did not show any improvement compared to the bare LSC electrode, although it could be beneficial for long-term stability upon operation [14]. Therefore, this thin CGO layer was not included in the full cell to simplify its electrochemical characterization, as the long-term stability was not included in the scope of this thesis.

3.2.2.2 Fuel electrode

The fuel electrode of choice is based on Gd-doped ceria ($Gd_{0.2}Ce_{0.8}O_{2-\delta}$) since this material becomes a MIEC under reducing conditions and has proved remarkable performance in SOFC mode [15]. The deposition of this material by PLD showed high growth rates of about 6 nm/min on a 4-inches silicon wafer, and the thickness obtained through 25.000 laser pulses (T = 100 ºC, f = 10 Hz, P = 100 mTorr, Fluence = 0.35 J/cm^2) was measured by ellipsometry and reported in Figure 3.8 below. As illustrated, there is a homogeneous deposition with a variation

along the wafer of ±6 nm, which makes this deposition method suitable for building up scalable technology.

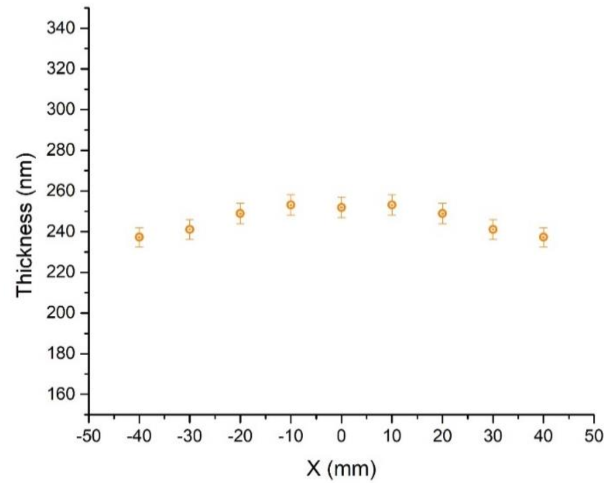

Figure 3.8. Ellipsometry measurement along the wafer diameter of the thickness of the CGO film deposited by PLD

Here, the PLD parameters were optimized to obtain a porous microstructure in order to increase the access of the fuel to the TPBs and to avoid any undesired stress from such a thick film compared to the rest of the PEN structure. Figure 3.9 shows the microstructure of the anode thin film after annealing at 700 °C and after evaporation of the platinum film (about 100 nm-thick), obtaining in-plane percolation but still access of the gas to the anode and TPBs. Here, a Pt-based current collecting layer is necessary because the CGO shows too low electronic conductivity for in-plane current collection [2].

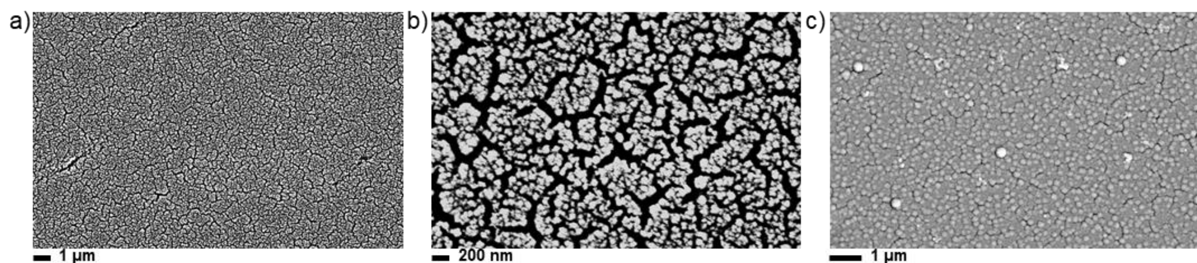

Figure 3.9. Top-view SEM images of (a,b) porous CGO thin film as-deposited at two different magnifications and (c) after Pt evaporation

XRD characterization was also performed right after deposition, showing a polycrystalline film and peaks assigned to the cubic fluorite-type lattice (JCPDS 34-0394) that was maintained even after thermal post-processing up to 700 °C, as shown in Figure 3.10.

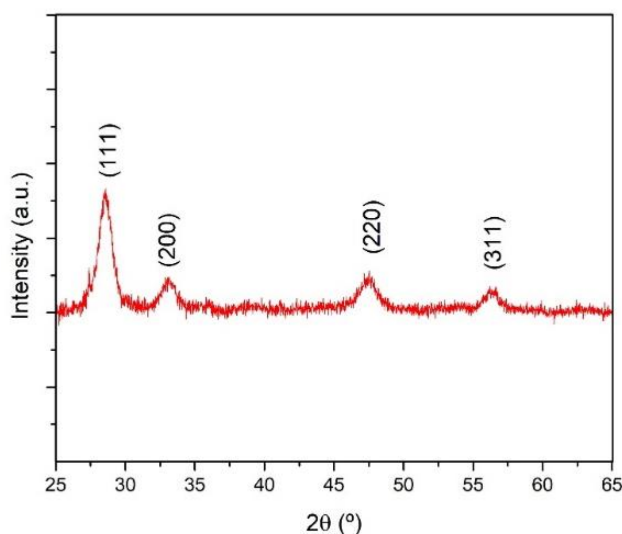

Figure 3.10. XRD pattern of porous CGO film as-deposited by PLD at T=100 ºC

Finally, symmetric cells with CGO/Pt electrodes were prepared on YSZ(001) single crystals and their electrochemical characterization was carried out by EIS in 5%-H_2 atmosphere within a range of T from 500 to 650 ºC. The results are related to two different electrode's morphologies that were analyzed - dense and porous - to study the general behavior of such material under SOFC conditions and are presented in Figure 3.11183.11.

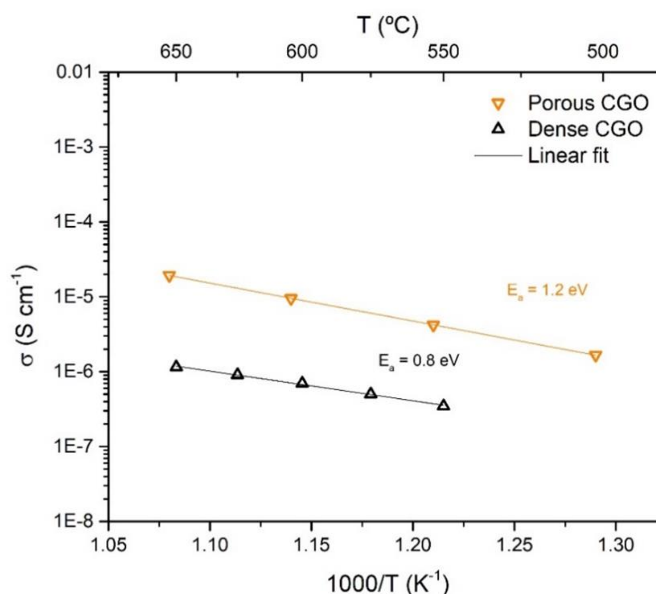

Figure 3.1118. Arrhenius plot obtained from impedance measurements in 5% H2 atmosphere of symmetric Pt/CGO/YSZ/CGO/Pt cells

In the first case, the activation energy of about 0.8 eV and high ASR values were obtained, suggesting that the contribution to the total conductivity was dominated by the ionic diffusion [16]. A different behavior is observed for the porous electrode, where an activation energy of 1.2 eV was calculated, likely indicating an oxygen surface exchange dominating behavior. Indeed, these (and higher) values of activation energy are typically observed for CGO and MIEC working electrodes [9,17,18]. Moreover, reasonable values of ASR ~1 Ωcm^2 were obtained at T>650ºC.

Overall, porous CGO thin films combined with Pt current collectors showed the potential for integration in micro-SOFC operating above 650 °C and were therefore employed in the fabrication of a fully ceramic micro-SOFC PEN nanostructure on large-area silicon substrates.

3.3. High-quality ultrathin ceramic films by Atomic Layer Deposition

Nanocrystalline zirconia (ZrO_2) and ceria (CeO_2)-based thin films find great importance for many technological applications, especially because of their enhanced electrical properties and chemical stability compared to their microcrystalline counterparts. Indeed, the increased interfacial area and size-dependent defects of nanocrystalline thin films make them ideal for applications related to gas sensors, ionic membranes, and fuel cells [19]. Nevertheless, more attention has lately been addressed to new deposition techniques able to yield very high quality and homogeneous films.

Atomic Layer Deposition (ALD) has the advantage of producing highly conformal and homogeneous films on larger substrates, but it suffers from very low growth rates and deposition conditions that increase the cost and prevent wide adoption in the industry. For instance, the 80 nm-thick YSZ-based suspended membranes for micro-SOFC applications reported by Prinz and coworkers [20] took more than 16 hours the be fabricated. Moreover, a few studies in literature reported that the deposition of yttria by ALD results in a high carbon contamination and proton incorporation in the film that would be highly detrimental for an ionic electrolyte [21].

In this section, the fabrication of ultrathin pure zirconia ionic conductor films by ALD in combination with a large-area PLD deposition is presented as a unique solution to produce high-quality and pinholes-free electrolytes for micro-SOFCs and sensing applications.

This section also aims at introducing a new promising method for the deposition of ceramic electrolytes with great control on thickness and quality of the film despite the reduced time and cost requirements of the process. Here, Spatial-ALD (SALD), also known as Atmospheric Pressure ALD (AP-ALD), is chosen to demonstrate its potential application in ceramic thin-films deposition at industrial scale (see Chapter 2.2.2.3). In this regard, Mione *et al.* [22] demonstrated the successful application of SALD for the fabrication of ZrO_2 thin films with a growth per cycle (GPC) as high as 0.14 nm/cycle, i.e., >10 times faster than a conventional ALD deposition and showing a very low number of contaminants, thus addressing two major issues typically linked to the ALD process.

Here, for the first time, the fully scalable spatial atomic layer deposition of ceria thin films for future applications in catalysis and electrochemical devices is presented.

3.3.1. Pure ZrO_2 thin films with ionic conductivity deposited by ALD

Zirconia-based ionic electrolytes present the metastable cubic or tetragonal lattice, also known as high-temperature phases, when extrinsic defects such as trivalent cations (e.g., Y^{3+}) are added to the lattice due to a charge compensation mechanism, as described in chapter 1.2.3. The presence of oxygen vacancies within the lattice makes of this material an excellent ionic

conductor, often employed as electrolyte in high-temperature solid oxide cells (SOCs) and oxygen sensors. Moreover, the metastability showed across a wide range of temperatures and atmosphere, together with presence of both surface basic and acid sites, makes it an important candidate for heterogeneous catalysis and photo-catalysis.

In recent years different charge compensation mechanisms have been proposed that do not require extrinsic doping to stabilize the cubic and tetragonal phases of zirconia at low temperature, thus preventing any possible contaminants or undesired defects coming from the yttria organo-metallic precursor [21,23]. Fabris and co-workers [24] hypothesized, for example, that the high-temperature cubic and tetragonal phases of ZrO_2 could be stabilized at room temperature by oxygen vacancies only. This concept according to which the stabilization mechanism for pure ZrO_2 is solely dominated by the lattice distortion caused by oxygen vacancies, found further support from theoretical calculations and simulations on the metastability of such material. Here, it was found that the oxygen vacancies take the form of F centers, typically observed for non-reducible oxides, where the excessive charge stays localized on the vacancy site [25,26]. A different explanation could contemplate the presence of localized Zr^{3+} already observed for materials undergoing drastic post-synthetic treatments, although not expected for non-reducible oxides at mild conditions [25]. All in all, evidence in literature suggests that the population of intrinsic defects which are the main responsible for the metastability of this high-temperature phases, is strongly affected by the synthesis method and subsequent treatments on the material. A tetragonally-cubic stabilized phase of ZrO_2 without any extrinsic doping is denoted as Oxygen Vacancies Stabilized Zirconia (OVSZ).

3.3.1.1 Structural and electrical properties

ALD layers of ZrO2 were fabricated according to the specifications detailed in Chapter 2.2.2.2. Characterization of the ZrO_2 film thickness by ellipsometry was the first step to prove its homogeneity on the substrate's surface. Figure 3.12 shows the calculated film thickness for 220 ALD cycles, confirming the suitability of a self-limiting reaction for the fabrication of highly conformal and homogeneous films. The obtained thickness remained in 20.7(±0.2) nm, i.e., with a tolerance below 1% over the whole 4-inch wafer.

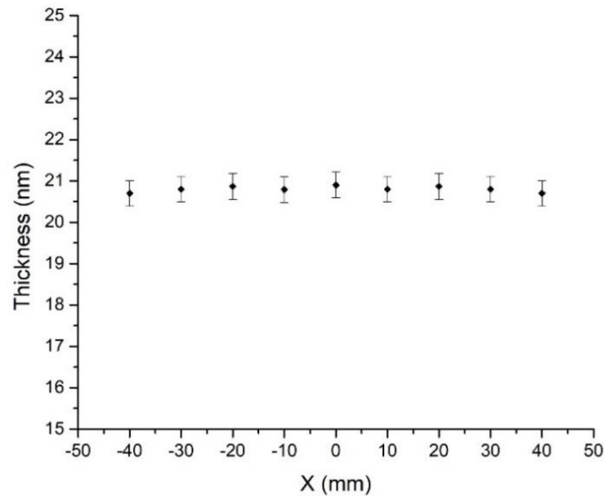

Figure 3.12. Ellipsometry measurement and results of the modeling of the film thickness along the 4-inches silicon wafer

Figure 3.13 reports the GIXRD pattern of the 20 nm-thick ZrO_2 film deposited on different substrates (silicon(001), sapphire(0001) and Si_3N_4 thin film on Si(001)) and the comparison with a 100 nm-thick film on Si(100) obtained with the same fabrication method. As-deposited 20 nm-thick samples show the tetragonal phase (JCPDS 17-0923) or a mixture of the above and cubic phase (JCPDS 27-0997), with the highest crystallinity obtained for samples deposited on amorphous Si_3N_4 substrate and a slight preferred orientation to the (111) crystal plane.

Further GIXRD patterns were registered on the same sample after annealing ex-situ at 700 ºC for 3 hours to ensure there would not be any structural change upon operation of the fuel cell. Results showed that the crystal structure was maintained without any significant change, confirming the metastable nature of nano-zirconia presented in literature [27].

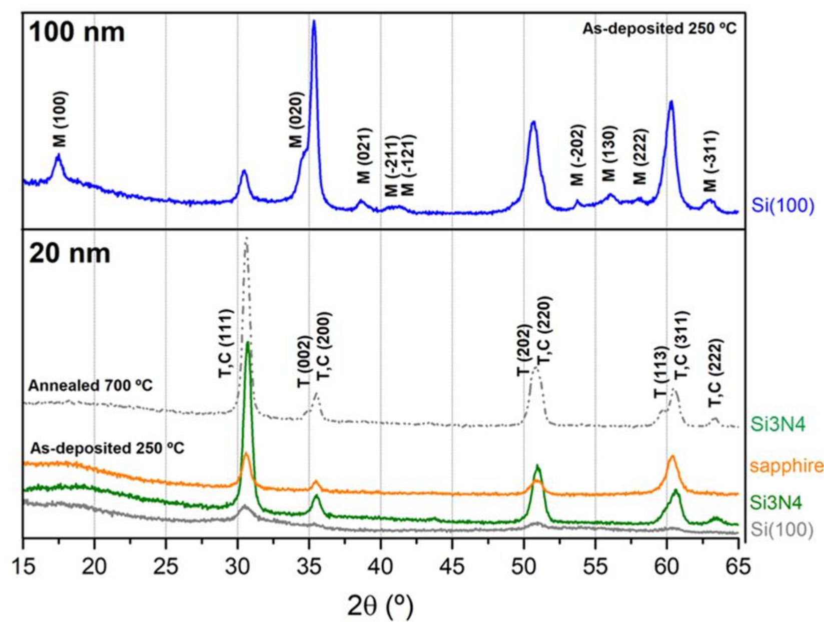

Figure 3.13. GIXRD pattern of ZrO_2 films as-deposited by ALD, with different thickness (100 nm top, 20 nm bottom) and onto different substrates. A measurement of a sample annealed at 700 ºC is also included.

On the other hand, the GIXRD pattern of the 100 nm-thick sample as-deposited showed many peaks related to the monoclinic phase of ZrO_2 (JCPDS 37-1484). This result alone suggests the influence of the crystallite size in the stabilization of the cubic and tetragonal phases of zirconia [28].

The grain size of the polycrystalline 20 nm-thick samples was examined by Atomic Force Microscopy (see Figure 3.14). The average grain size was found to be 32.6(±1.2) nm, showing almost no changes upon annealing at 700 ºC where the measured average grain size was 33.1(±1.6) nm, as expected after the results presented in [27]. The calculated roughness for both samples was found to be $R_q \sim 1$ nm.

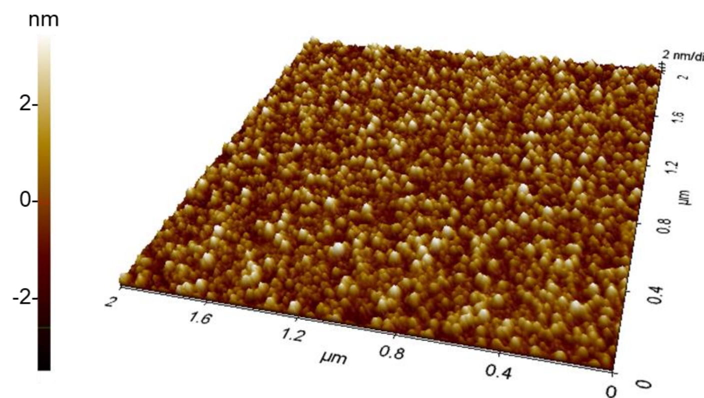

Figure 3.14. AFM measurement of the film morphology and roughness.

Finally, XPS analysis was carried out for samples deposited on Si(100) to reduce charge accumulation and thus background noise during the measurement. XPS spectra recorded for Zr^{3d}, O^{1s} and C^{1s} core level transitions are shown in Figure 3.15 for the sample as-deposited (black line) and samples annealed in oxidizing (red line), inert (blue line) or reducing (purple line) atmosphere.

XPS spectrum of the Zr(3d,5/2) transition reported in Figure 3.15-a confirmed the 4+ oxidation state of zirconium atoms on all samples (binding energy BE = 182.5 ± 0.3 eV), although showing that the thermal treatment has some effects on the binding energy of such atoms: a blue shift was observed for the samples treated in air, while red shift was observed for those treated in H_2 or N_2 atmosphere. This result suggests local Zr surroundings more or less oxidized depending on the atmosphere conditions upon thermal treatment.

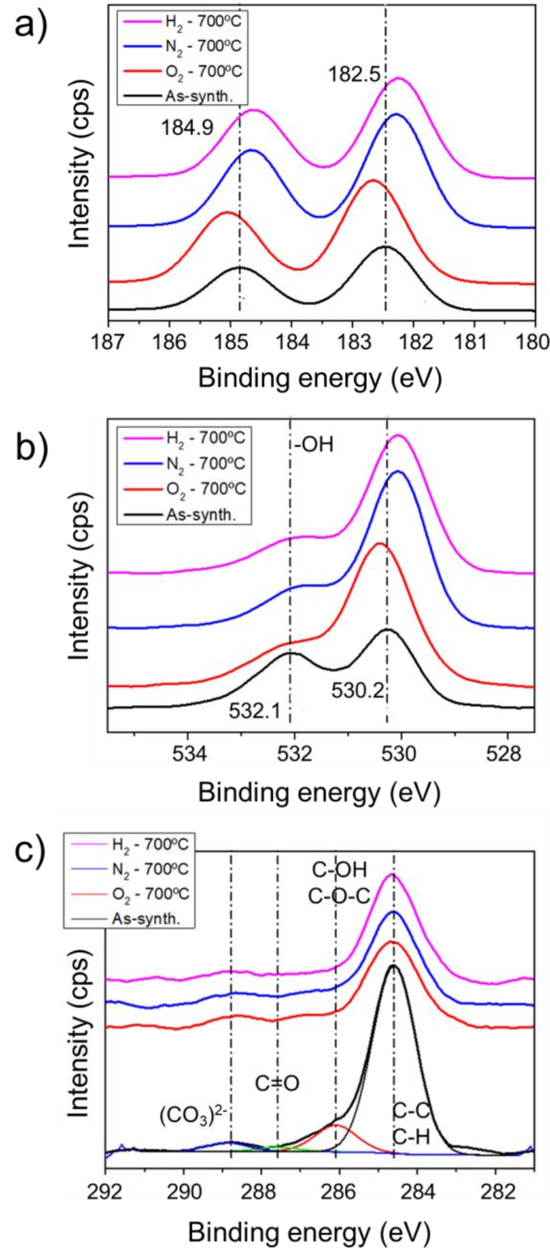

Figure 3.15. XPS spectra recorded for ZrO2 samples (20 nm in thickness) as-deposited (black line) and after annealing in O_2 (red line), N_2 (blue line) and H_2 (purple line). The spectrum is recorded for (a) Zr3d, (b) O1s and (c) C1s core level transitions.

Figure 3.15-b shows the peaks related to O^{1s} transitions where the contributions of Zr-OH and ZrO_2 can be distinguished. Here, the peak related to Zr-OH (BE = 532.1 eV) is maintained constant or slightly reducing upon annealing, while the peak at BE = 530.2 eV increases.

Finally, summing up the concentration of oxygen species and subtracting those related to carbonaceous species reported in Figure 3.15-c (i.e., impurities from ALD process and exposure to the atmosphere), it was possible to approximately calculate the non-stoichiometry of oxygen from Zr/O ratio reported in Table 3.1.

Samples	O_{tot}/Zr	C/Zr	O/Zr
A	2.73	2.74	**2.09**
O	2.44	0.76	**2.15**
N	2.27	0.74	**2.00**
H	2.28	1.02	**1.97**

Table 3.1. Calculated O/Zr and C/Zr ratios for all samples from XPS analysis.

Although the obtained absolute values should be taken cautiously, the trend of the results is meaningful. The results showed higher oxygen content for as-deposited samples and those annealed under oxygen while lower O/Zr ratio for the samples annealed in nitrogen and reducing conditions (consistent with the locally reduced Zr atoms).

To evaluate the electrical properties of the 20 nm-thick films on sapphire (0001) single crystal substrates, interdigitated electrodes were fabricated on top of the as-deposited films to measure the in-plane conductivity by EIS. These electrodes had a total length of 1.76 cm, fingers width and spacing in between of 100 μm.

The Nyquist plots obtained from the EIS measurements are reported in Figure 3.16-a and the associated resistance fitted with RC circuits for both high-frequency and low-frequency components. These spectra are fully compatible with having ZrO_2 layers with ionic conductivity. To evaluate this possibility, Figure 3.16-b reports the Arrhenius plot of the resistance values. The activation energy observed in the Arrhenius plot for these samples matches with the values previously reported for bulk YSZ [1], suggesting that the same mechanism of oxygen diffusion is occurring, although the conductivity value is two orders of magnitude lower. This difference is easily explained by the larger number of oxygen vacancies induced by yttria substitution in the 8% Y: 92% ZrO_2. Despite this, the potential ionic conductivity of our ALD deposited layers is high enough to become relevant in certain applications, e.g., as barrier layer or protective coating.

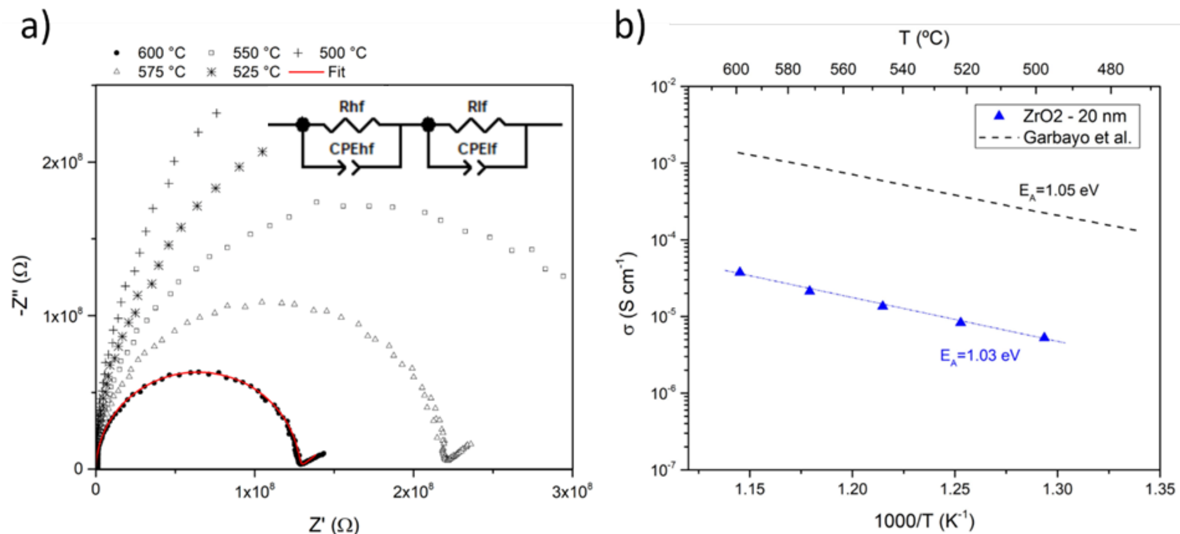

Figure 3.16. In-plane electrochemical analysis on ZrO_2 films by interdigitated micro-electrodes. (a) Nyquist plot at different temperatures and fitting, (b) Arrhenius plot and comparison with YSZ electrolyte with columnar microstructure from [1]. Measurements are performed in oxidizing atmosphere.

To confirm the origin of the reported conductivity for pure zirconia (either electronic or ionic), further impedance measurements were performed at different atmospheres. Indeed, from the Frenkel point defects theory it is well known that the electronic conductivity is strongly influenced by the oxygen content in the atmosphere while ionic conductivity does not change regardless the oxygen content in the atmosphere [29]. To prove so, Figure 3.17 shows the impedance measurements at T = 500 °C and the calculated in-plane conductivity at the same temperature as function of the oxygen partial pressure in the atmosphere.

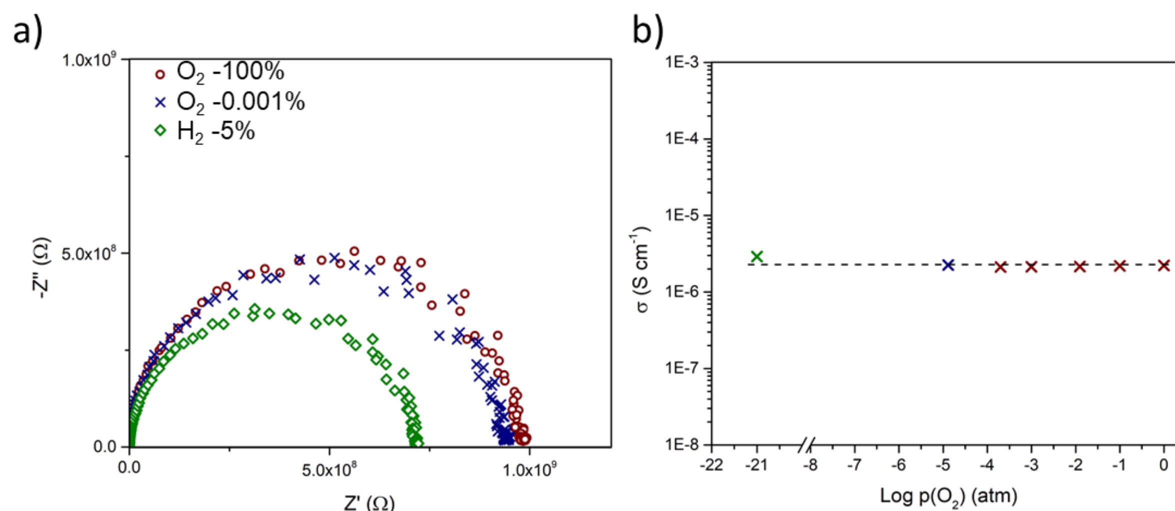

Figure 3.17. In-plane electrochemical measurements as a function of pO_2, measured at 500 ºC. (a) Nyquist plot and (b) Brouwer-like plot of film conductivity at different pO_2.

Whereas it is possible to observe small changes in the resistance associated to the thin film electrolyte, the overall conductivity is maintained throughout a wide range of oxygen partial pressure, confirming the ALD-ZrO_2 film as a mainly ionic conductor.

These results together with the absence of Zr atoms with oxidation state +3 (as determined by XPS) reveal this nanocrystalline ZrO_2 as a mainly ionic conductor, with a conductivity value of $\sigma = 4x10^{-5}$ S/cm and $3x10^{-6}$ S/cm at T = 600 °C and 500 °C respectively.

The origin of this ionic conductivity is attributed to the same oxygen vacancies that stabilize the cubic/tetragonal phase in nanocrystalline zirconia that was mentioned in section 3.3.1.a. Hence, it is reasonable to expect a lower ionic conductivity of pure zirconia than compared to yttrium-doped zirconia, since the amount of oxygen vacancies is greatly increased by doping with trivalent atoms [30]. Nevertheless, the simplicity of this approach to fabricate highly uniform and conformal ionic conductors can find indeed many interesting applications in electrochemical micro-devices. In this work, 20 nm-thick films of pure zirconia are embedded in the electrolyte component of a micro-SOFC to prevent the formation of pinholes and subsequent short circuits that eventually lead to power losses and failure of the device. The effects of the addition of this layer in the fabrication flow are presented in the following section together with the characterization of the electrolyte comprising YSZ by EIS.

3.3.1.2 Pinholes-free ceramic suspended membranes (based on ALD+PLD bilayers)

This section aims at understanding the effect of adding a 20 nm-thick film of pure zirconia to the fabrication flow for micro-SOFCs to be presented in Chapter 4, both from mechanical and electrical perspectives. As previously mentioned, the main goal of using this bi-layer is overcoming currently existing problems of pinhole formation during the fabrication of self-supported electrolyte membranes.

For this purpose, 4-inches silicon wafers with dielectric bilayers are masked prior ALD deposition so that half wafer was not covered by OVSZ. Subsequently, 20 nm of pure zirconia are deposited by ALD on half of the wafer only, and a 130 nm-thick 3YSZ layer is deposited by PLD on top of the substrate covering the whole surface. Squared membranes of 300 to 800 μm in width are eventually obtained after performing wet and dry etching on the substrate. Finally, diced 1x1 cm^2 devices are sputtered with platinum electrodes of 100 nm in thickness on both sides of the membranes for electrical characterization. Here, the resistance across the electrolyte at room temperature was checked to assess if any short circuit had occurred after Pt sputtering as a consequence of the presence of a pinhole in the electrolyte.

Since the main target is to scale the fabrication process, statistics over complete wafers were carried out. Table 3.2 summarizes the survival rate of the membranes with bi-layers compared to bare YSZ membranes.

Electrolyte	**3YSZ (130 nm)**	**3YSZ (130 nm) + ALD-ZrO_2 (20 nm)**
	%	**%**
Rupture	40	10
Short circuit [1-1000 kΩ]	25	8
Severe short circuit [1-1000 Ω]	15	3
Survival rate	20	79

Table 3.2. Comparison of success rates in the fabrication of cells with two different electrolyte configurations.

Just comparing the survival rate for these samples, it is quite evident that the yield of fabrication of the suspended membranes comprising the OVSZ layer increased 4-fold. The embedded ALD layer seems to reduce both short circuits across the electrolyte and rupture of the membrane, regardless the size of the membrane, this latter probably a consequence of the stress compatibility between ZrO_2 and YSZ (both compressive) and of the reduction in number of macro-defects such as pinholes.

In this study, the short circuits were categorized according to the resistance measured across the electrolyte. While severe short circuits were associated to a resistance range from 1 to 1000 Ω, other samples showed a higher associated resistance in the range between 1 to 1000 kΩ. These latter were ultimately linked either to nano-pinholes or small platinum contact area, often non-detectable by solely checking the OCV across the electrolyte but that inevitably cause current leakages and power losses [31].

An example of pinhole causing severe short circuit (associated resistance R ~124 kΩ) is reported in Figure 3.18-a, where the hole left by an ejected particle is covered by platinum electrodes therefore causing the short circuit. Unfortunately, no correlation between pinholes size and cross-plane resistances could be found, since the causes for the creation of a pinhole can be

different and the resistance ultimately depends on the contact area of the platinum electrodes, that was indeed impossible to estimate.

On the other hand, the fabrication entirely performed by PLD leads to a very low survival rate of the membranes and a great amount of defects. PLD is typically ejecting droplets of material that, if taking place at the beginning of the deposition process, end up into pinholes. Figure 3-18-(b,c) below shows the effects of operating conditions on a micro-SOFC membrane with a pinhole. The area where the two atmospheres are in contact – the pinhole – grew bigger upon operation and led to the formation of a hot spot, eventually melting the materials surrounding that area.

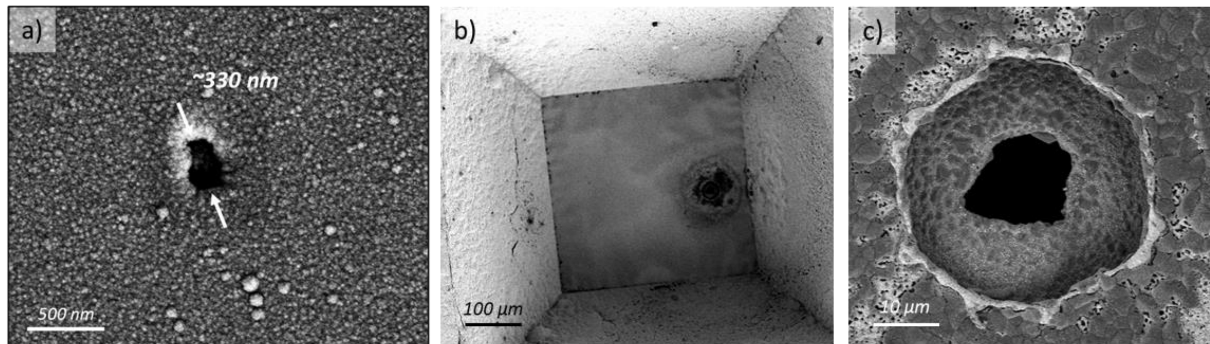

Figure 3.18. Representation of pinholes on suspended membranes. (a) SEM top image of a pinhole causing severe short circuit; (b) SEM image of a pinhole after operation at 600 ºC; and (c) SEM image of the pinhole's detailed morphology after operation

Finally, the out-of-plane impedance measurements of typical suspended membranes including such functional layer were performed by sputtering Pt electrodes (~100 nm-thick) on both sides of the electrolyte. Figure 3.19 shows the Nyquist plots obtained at low temperature in order to evidence the contribution of the electrolyte to the total resistance that would not be possible at high temperatures, where the electroylte resistance is usually modelled with a serial resistance observed at high frequency (in the MHz range). The equivalent circuit model used to fit these curves is also included, where the serial resistance is related to the wiring and current collection and two RQ components (a resistance R in parallel with a constant phase element Q) are used to model the electrolyte and electrodes contributions, respectively .

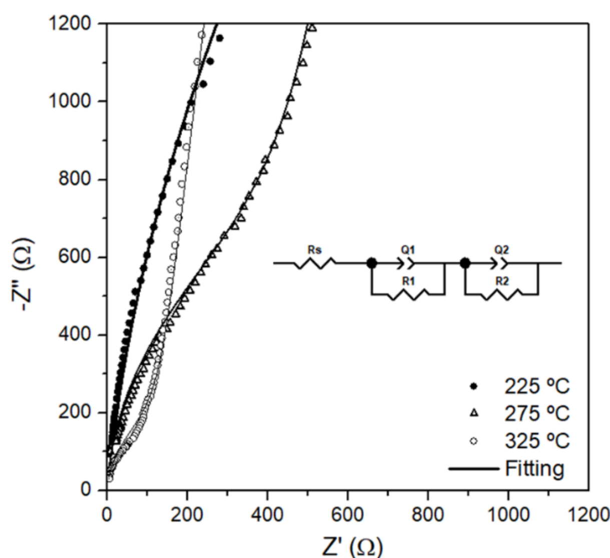

Figure 3.19. Nyquist plot from the EIS analysis on symmetric Pt/YSZ-OVSZ/Pt cells at low temperature, where the contribution of the electrolyte is fitted with Q1 and R1.

Deconvoluting arcs obtained at different temperatures allow to determine the temperature behavior of the bi-layer membranes. Figure 3.20 represents the Arrhenius plot of the total out-of-plane conductivity of the electrolyte fabricated in this work as a function of temperature. The dots representing the conductivity values from 225 °C to 325 °C were calculated from the measurements previously shown in Figure 3.19. On the other hand, the other values were obtained for higher temperatures by fitting a serial resistance that considered both electrolyte-associated resistance and wiring. The value of the conductivity of a 250 nm-thick electrolyte based on 8YSZ deposited by PLD [2] is also included for comparison. From Figure 3.20 it is noticeable that the activation energy E_a=0.95 eV associated to the ionic conductivity across the electrolyte is consistent with the reported values for bulk YSZ at low temperature. The 0.1 eV difference between the values reported in the plot above can be attributed to different defects association in the two systems, likely originating from the addition of a new interface [32].

Nevertheless, the ability to fabricate thinner electrolytes with a reduced number of defects leads to a decrease in Area Specific Resistance (ASR). Considering a value of ASR = 0.15 Ω cm^2 for application of electrolytes in SOFC technology [33], in this work we propose a 150 nm-thick electrolyte based on zirconia that can operate at temperatures as low as 350 °C.

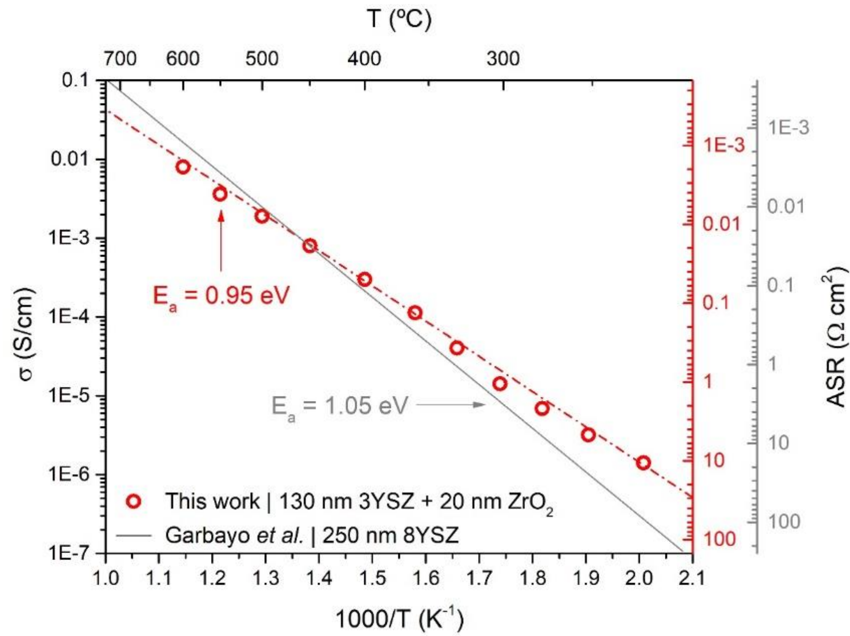

Figure 3.20. Arrhenius plot related to the out-of-plane EIS measurements of symmetric Pt/YSZ-OVSZ/Pt. Conductivity values are reported on the left Y-axis and ASR on the right Y-axis. Literature values from [2] *are reported for comparison.*

3.3.2. Spatial Atomic Layer Deposition of Ceria thin films

The development of nanocrystalline ceria films finds nowadays a wide number of applications [34]. It is indeed one of the most common supports for heterogeneous catalysis [35], it is used for electrochemical biosensing and for its antioxidant properties [36] and especially, for its excellent surface exchange properties, as a fuel electrode in SOFCs [37,38] when doped with trivalent atoms such as Yttrium, Gadolinum or Samarium. Moreover, ceria-based films are often used in SOFC technology as a barrier layer in between Zr-based electrolytes and perovskite cathodes containing strontium to prevent the formation of detrimental secondary phases upon operation [14,39]. More details can be found in Chapter 1.2.3.

There is an increasing interest in literature to fabricate high-quality CeO_2-based thin films by ALD, due to the numerous unique properties of such deposition method. Nevertheless, most results reported so far very low growth rates for such oxide films, as its precursors are usually non-volatile and with a limited ALD window where degradation of the precursors does not occur [40]. Moreover, in most cases a successful deposition was achieved only with O_3 oxidant precursor for its superior reactivity, adding even more complexity and cost to the process.

The present section aims at developing a route for CeO_2 thin films fabrication with reduced cost and time of the process compared to state-of-the-art fabrication processes. Spatial Atomic Layer Deposition (SALD), an innovative approach to layer-by-layer depositions previosuly described in Chapter 2.2.2.3, is hereby employed for the first time to achieve this goal. This technique is indeed very promising and allows for easier fabrication of nanostructured and nanocomposite materials in a wide range of applications [41]. In this work, home-made SALD equipment still under development at Grenoble INP was employed. Modification of the first version of the

system, preliminary optimization deposition conditions and characteritzation of first deposited layers of CeO_2 were carried out in the frame of this thesis (and a 4-months research stay).

3.3.2.1 Preliminary optimization of the SALD equipment and deposition parameters

The experimental setup adopted for the deposition of CeO_2 by SALD was described in Chapter 2.2.2.3, where it has been already mentioned about the low volatily of typical metal-organic Cerium precursors. In particular, previous TGA analysis found in literature [42] showed that temperatures above 200 ºC are required to ensure sufficient volatility at ambient pressure, while usually ALD systems operating in mild vacuum need the precursor to be heated at lower temperature, about 140-150 ºC [43]. Practically, such relatively high temperature make the uniform heating of the cylinder containing the cerium precursor and the gas lines non-trivial, either causing the formation of cold-spots and subsequent condensation of the precursor wihin the line, or differences in thermal expansion of the metallic lines and, therefore, gas leakages.

To avoid this, different designs of the precursor cylinder were tested in this work (Figure 3.21). The cylinder in Figure 3.21-a, which is an assembly of swagelok unions and fittings (stainless steel), indeed presented many leakages upon heating. A smaller and more compact brass-casted cylinder was therefore tested to allow for a more uniform heating (Figure 3.21-b), succeding in sublimating the precursor and transporting it to the deposition head. Nevertheless, the plastic lid used to seal the cylinder allowed for some air and humidity to enter in contact with the precursor, causing its degradation. Finally, the cylinder shown in Figure 3.21-c was designed and fabricated to replicate the compact design of the previous cylinder, but including a threaded joint and a PTFE gasket, providing hermetic sealing throughout repeated heating-cooling cycles.

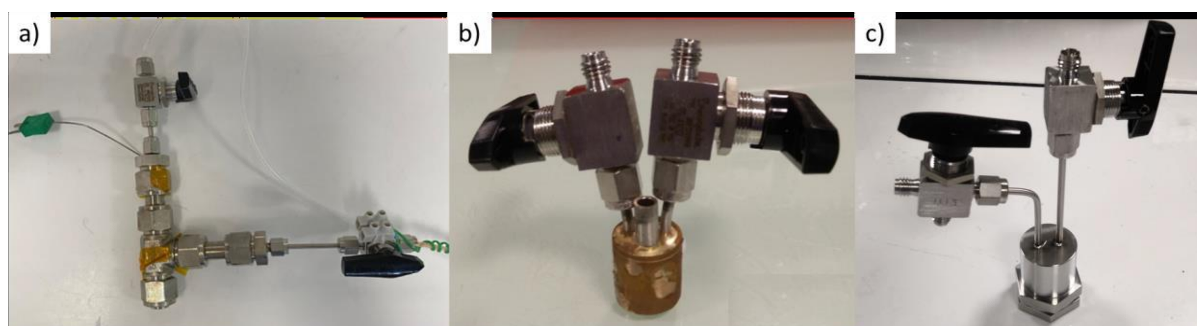

Figure 3.21. Optical images of the customized cylinders containing the $Ce(thd)_4$ precursor (thd = 2,2,6,6-tetramethyl-3,5-heptanedione). (a) Swagelok assembly, (b) brass-based wielded cylinder and (c) stainless steel customized threaded cylinder.

Once the whole system was properly assembled with heating cables and insulation, the N_2 gas flow for precursor and dilution lines were optimized to avoid dragging any solid powder from the precursor to the line, but still ensuring sufficient feed to the deposition head to reach state-of-the-art growth rates of a CeO_2 film.

After a trial and error optimization of the deposition parameters - temperature and gas flows, the film deposition started through an oscillatory motion of the substrate below the deposition head, placed at a distance of 150 μm. The deposition head was fed with a precursor line, a

humidified (2.7% H_2O) N_2 line as oxidant and N_2 as purge line. Oscillation parameters were set in a way that every substrate full motion would take 2.5 seconds.

Figure 3.22 shows the resulting film deposited after 500 oscillation cycles, i.e., about 20 min only. While some adjustments of the setup and especially the SALD head design are needed to achieve a more uniform film deposition, a dark-brownish film was obtained, suggesting either the presence of degradated organic species or Ce^{3+} within the film.

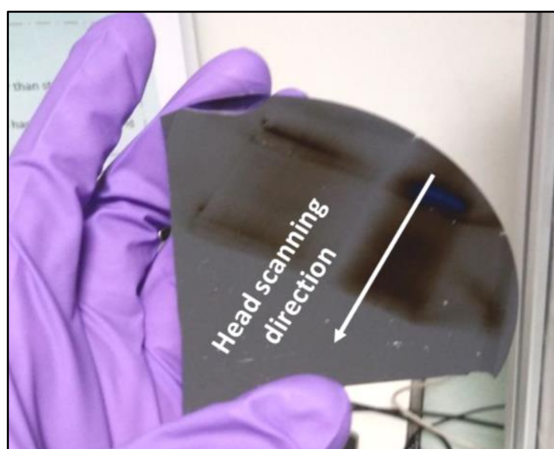

Figure 3.22. Optical image of first CeO_2 thin films deposited on a Si(100) wafer through 500 SALD cycles

Further optimization is clearly needed to obtain uniform distribution of the reacting species to the substrate. A new design of the deposition head will therefore be needed to achieve even temperature distribution. In the next section, a structural and morphological characterization of the film is presented to establish the initial quality of the films.

3.3.2.2 Structural characterization

To assess the properties of the films deposited by SALD with $Ce(thd)_4$ precursor (thd = 2,2,6,6-tetramethyl-3,5-heptanedione) and H_2O as oxidant, the morphology of the film was checked by SEM, its structural properties by XRD and its electronic structure by XPS.

Figure 3.23-(a,b) shows the top-view and cross-sectional SEM images of a 70 ± 10 nm-thick $CeO_{2-\delta}$ film grown on Si substrate by SALD. The images were taken in the area where the film thickness was found more uniform. Figure 3.23-a indicated a small amount of porosity on the surface of the films, therefore a calcination treatment at 500 °C for 2 h in air was performed to densify the film and remove any carbonaceous species left from the deposition process. The result of this temperature annealing led to a substantial increase in grain size of the film showing this time a dense microstructure, as it can be seen in Figure 3.23-c.

From this result, it is possible to roughly estimate a GPC for CeO_2 of 3 nm/min calculated on a deposition specimen of about 4 cm^2. Despite the GPC in SALD largely varies depending on the surface area to be coated, the growth rate hereby presented is remarkably higher than

expected from conventional ALD of CeO_2, reported in literature as a very slow process requiring about 2500 cycles for the same thickness, i.e. about 14 hours [43].

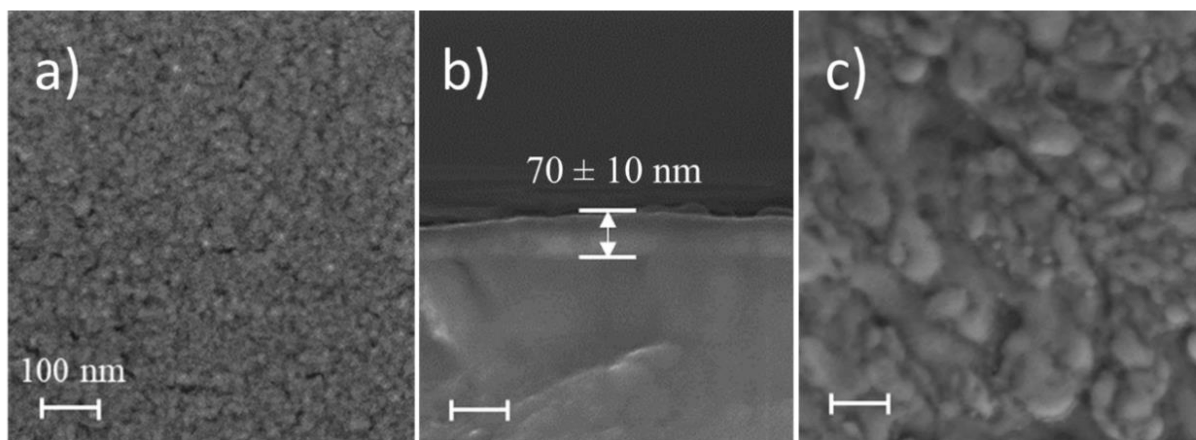

Figure 3.23. SEM images of the CeO_2 layer deposited by SALD. (a) Top-view of the as-deposited porous film; (b) cross-section view of the same; and (c) top-view of the film after calcination at 500 °C.

Interestingly, the XRD pattern recorded on the film as-deposited and reported in Figure 3.24 show all the peaks related to cubic CeO_2 (JCPDS 34-0394) with a lattice parameter a = 5.41 Å, without any evident secondary phases. Moreover, the wide peaks observed confirm the nanocrystalline nature of the film.

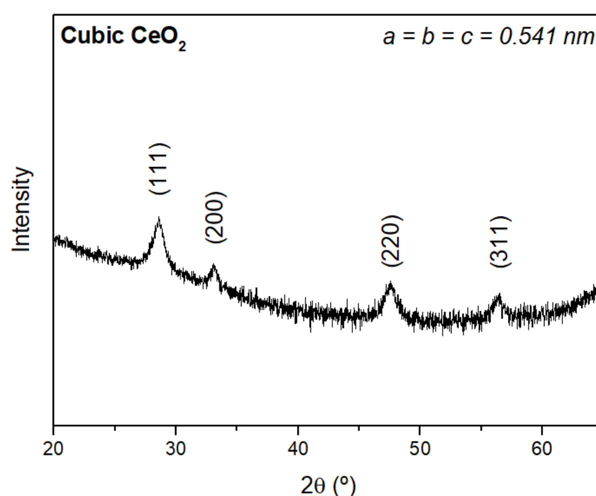

Figure 3.24. XRD pattern of the as-deposited CeO_2 by SALD

In the following, the electronic structure and chemical composition of the film were analysed by XPS. Figure 3.25-(a,c) shows the fittings of XPS core-level spectra of C^{1s}, O^{1s} and Ce^{3d} in the as-deposited film. O^{1s} and C^{1s} spectra showed different levels of adventitious carbon (284.8 eV) and other weakly adsorbed surface species OH− and H_2O (around 531.5 eV). O^{1s} core-level peaks show two peaks at around 531 and 528.6 eV. The peak at the higher binding energy of ~531.5 eV may be assigned to weakly adsorbed species at the surface (OH−, H_2O, C−O, C=O etc.), while the peak at the lower binding energy ~529 eV is characteristic of metal−oxygen bonding in the crystal network [44]. After 10 s etching with an Ar sputter gun, the surface-adsorbed species are significantly reduced (Figure 3.25-d,f). This demonstrates that the precursor was not trapped in the film, indicating a good film quality. In particular, Ce^{3d}:C^{1s} ratio was 66.9 : 33.1 in the as-deposited samples surface, while after etching, this ratio changed to 94.0 : 6.0.

The most common oxidation states of cerium is +3 and +4. The Ce^{3d} core level spectrum has been fitted with six main peaks between 875 eV and 920 eV. The peak designations are shown as blue peaks for the Ce^{3+} and red peaks for the Ce^{4+} and have been well discussed in the literature [45]. These results clearly demonstrate that there is a deviation from the stoichiometric CeO_2. The Ce^{3+} concentration at the surface of the sample is calculated as 59.2 % in the as-deposited film and 64.1 % after etching. From these values, the stoichiometry of the film can be estimated as $CeO_{1.70}$ and $CeO_{1.68}$ (after etching), respectively. If required, this substantial oxygen hypostoichiometry could be easily compensated by post-deposition annealing in oxidizing conditions.

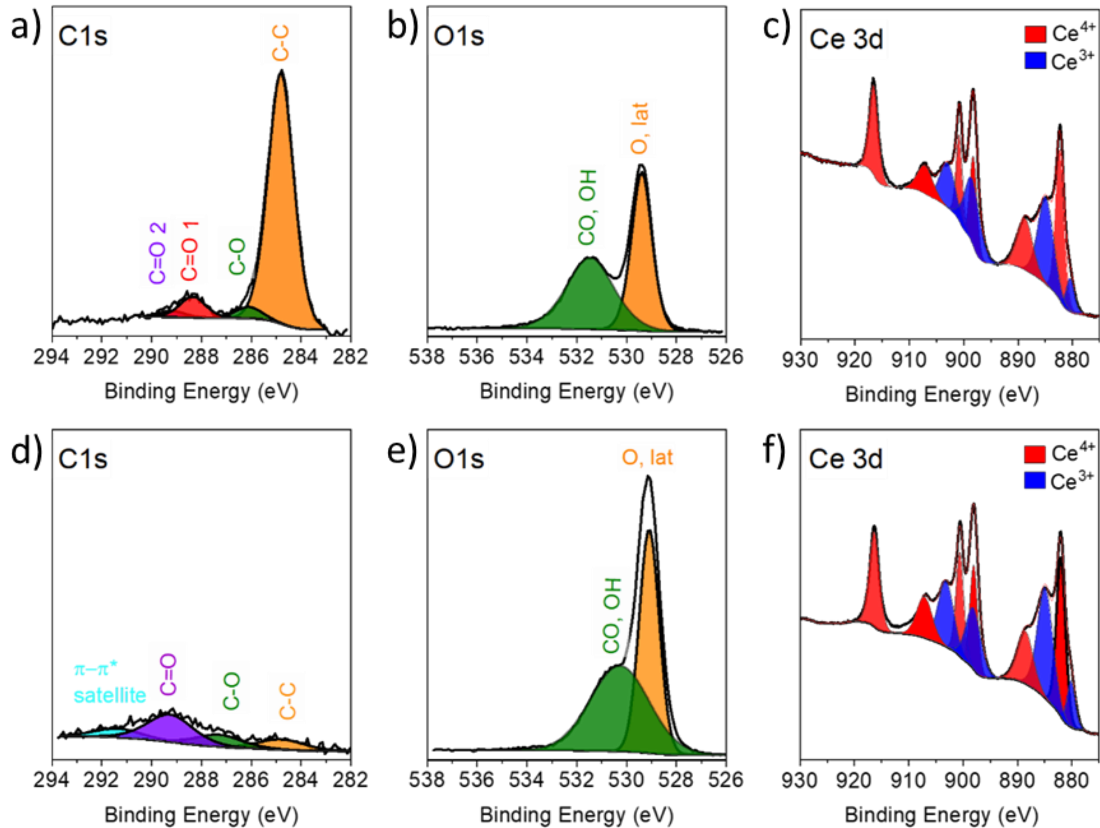

Figure 3.25. XPS analysis on the sample as-deposited (a-c) and after 10s Ar sputtering (d-f). C^{1s} (a,d), O^{1s} (b,e) and Ce^{3d} (c,f) core level transitions and fitting of the peaks are included in the analysis.

Afer the preliminary optimization carried out in this thesis, the use of SALD to fabricate CeO_2 thin film can be considered succesful since single phase crytalline layers were grown at high deposition rates. However, further optimization is required to gain lateral homogeneity that will open the way to employ SALD to scale up the fabrication of critical layers and devices.

3.4 Conclusions and future perspectives

In this chapter, the thin film deposition of advanced electrochemical materials was successfully undertaken using both physical and chemical deposition methods. The techniques hereby presented provided an effective way of integrating ceramic thin films in silicon-based micro-devices at large scale, therefore allowing cheap mass-scale production of the latter.

State-of-the-art mixed ionic electronic conductors materials such as LSC and CGO were deposited by large-area PLD on 4-inches silicon substrates and characterized both structurally and electrochemically for use as high-temperature air and fuel electrode, respectively. On the other hand, dense YSZ electrolyte thin films were deposited with the same method, but showed relatively high tendency to electrical short circuits and rupture when applied to ceramic membranes, mosly due to particle and droplet ejection during the PLD deposition process.

For this reason, ALD was chosen to deposit highly dense and ultra-thin layers (~20 nm) of pure zirconia, which was finally stabilized in the tetragonal form by solely oxygen vacancies, labelled OVSZ. The OVSZ thin layer alone demonstrated ionic conduction behaviour with negligible electronic conduction thoughout a wide range of oxygen partial pressure. The combination of PLD-deposited YSZ and ALD-grown OVSZ films resulted in high-quality and homogeneous bi-layer electrolytes with enhanced mechanical properties and high production yields. These bi-layers are proposed as robust suspended electrolytes for micro-SOFC and miniaturized oxygen sensors applications working at intermediate temperatures.

Finally, a much faster and less costly ALD counterpart - namely SALD - was applied for the first time to the fabrication of CeO_2 thin films. Taking advantage of the self-limiting reactions between a non-toxic cerium precursor and H_2O, it was possible to obtain dense $CeO_{2-\delta}$ thin films at atmospheric pressure and low temperature conditions, showing growth rates 15 times higher than for conventional ALD. These results open new horizons towards the scaling up of thin films micro-devices based on high quality ceramics, especially for application in micro-SOCs and catalysis. Indeed, SALD proven a very highly customizable technique and would certainly allow for direct doping of CeO_2 with with elements such as copper, eventually improving its oxygen exchange properties and electrical conductivity [46,47].

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CHAPTER 4

MICROFABRICATION OF THE MICRO-SOFC UNIT

4. Microfabrication of the micro-SOFC unit

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4.1 Introduction

This chapter is devoted to the design, fabrication, and proof-of-concept of a micro-SOFC unit built-up on a silicon substrate and whose electrochemically active materials are based on ceramic thin films.

As mentioned in the introduction of this thesis, technologies beyond Li-ion are receiving increasing attention, among which the development of micro solid oxide fuel cells (micro-SOFC) stands out. The dream of downscaling one of the most efficient known generators, i.e., a fuel cell, has been unsuccessfully pursued for years until recent advances in the miniaturization of micro-SOFC. Integration of micro-SOFC into mainstream silicon technology converted this disruptive technology into a serious candidate to power next generations of portable devices.

The compatibility of the clean-room processes with the ceramic thin film deposition ensures reproducibility and scalability of this technology, eventually leading to cheaper mass-scale production. Indeed, the unfair advantage of using silicon as a substrate material stands in its low cost, abundancy, and standard manufacturing processes already in use for microelectronics (see Chapter 2.2). Therefore, this chapter explores the combination of novel thin film deposition techniques, and by taking advantage of the latest advances in state-of-the-art electrochemically active materials, focus on improving the quality and fabrication yield of the suspended membranes.

In addition, it is important to fabricate thermally and mechanically stable membranes with the largest active area as possible, therefore improving the scalability of the process and the specific power per area unit of the fuel cell. A novel approach for enlarging the area of the membranes by using a mesh of doped silicon slabs as supporting structure is therefore presented. This way, the active area of the membrane has been enlarged by a factor of 10^3 compared to standard squared or circular membranes presented in the past [1–4].

4.2 Micro-SOFC basic configuration and design

In the most common micro-SOFC design found in literature, a silicon-based micro-platform supports a free-standing membrane that contains the active elements of the fuel cell, i.e., electrode/electrolyte/electrode tri-layer or usually known as PEN (positive/electrolyte/negative), see Figure 4.1. The design and geometry of the system have been optimized for minimizing heat losses, taking advantage of the low thermal mass of the silicon substrate (especially compared to a typical bulk SOFC system). Indeed, such substrates allow for reducing the time associated to the heating and start-up of the system from typical 5-10 min of bulk systems to less than a minute [5], hence enabling these micro-systems for portable applications.

The suspended membrane is formed by a tri-layer of ceramic thin films, presenting two mixed ionic-electronic conductor (MIEC) electrodes at the sides of an anionic electrolyte. Here, the redox half reactions described in Chapter 1.2.1 (Figure 1.3) occur upon operation of the micro-SOFC exposed to reducing and oxidizing atmospheres at the anode and cathode sides, respectively. Nevertheless, while research is pushing for better performing electroactive

materials, current state-of-the-art MIEC materials hardly show sufficient electronic conductivity for applications at intermediate temperatures (very high lateral resistance in thin film form). Therefore, the application of noble metals as current collectors is still the preferred pathway for minimizing power losses and was thus included in the membrane design hereby presented.

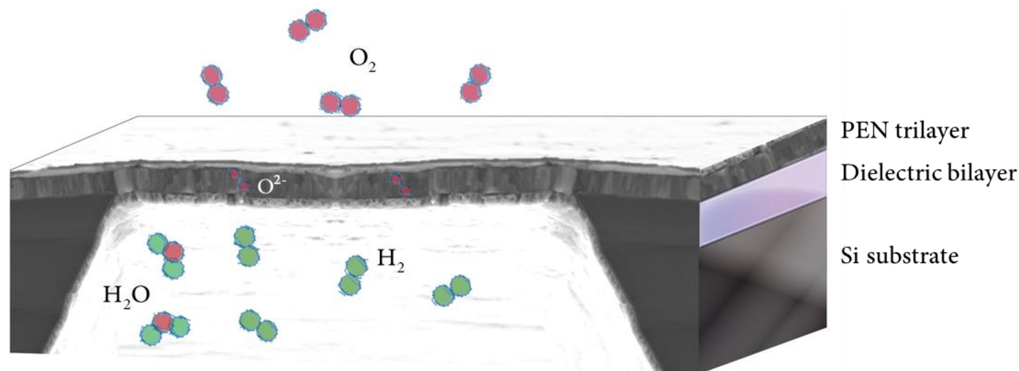

Figure 4.1. Schematic cross-section view of a UltraSOFC suspended membrane, obtained by editing SEM picture of the PEN element

Another important component of the micro-SOFC device is the dielectric layer formed of thin film silicon oxide and nitride that are deposited between the silicon wafer and the PEN components, preventing electrical effects or short-circuits due to the direct contact of the electrolyte or the electrodes with silicon. Moreover, it plays a fundamental role in the microfabrication flow, as later explained in Section 4.3.1.

4.3 Microfabrication of the micro-SOFC devices

In the following, the process performed to obtain silicon-based micro-SOFC units as in Figure 4.1 is presented, as well as the optimization of some key aspects needed to the thermomechanical stability of the ceramic membranes. Finally, the results of the microfabrication at 4-inches wafer scale will be shown.

Multiple microfabrication processes were performed for micromachining the substrate in collaboration with the IMB-CNM clean-room facilities, ensuring the fabrication of reproducible and standard platforms, subsequently integrating the ceramic thin films deposition carried out at IREC (see sections below). Regarding the deposition methods, Pulsed Laser Deposition (PLD) and Atomic Layer Deposition (ALD) were employed (as detailed in Chapter 3).

PLD is a deposition technique that has been widely investigated for deposition of thin functional ceramic layers. The technique shows good control on the stoichiometry transfer from target to substrate and it enables the growth of dense and crystalline films, as well as porous and amorphous [6]. Although it is usually a technique applied to coating of small areas of the size of a plasma plume, the Nanoionics and Fuel cells group at IREC pioneered the depositions of thin films by PLD on large-area substrates up to 4 inches wafers. Nevertheless, particles ejection from the target is a critical issue eventually leading to the formation of pinholes and short circuits across the membranes [7,8].

Atomic layer deposition (ALD) was chosen as a very promising technique to achieve large-area depositions with high degree of homogeneity and conformality. Electrolyte and electrodes materials deposited by ALD have been studied and shown good performances [9,10]. Nevertheless, the full fabrication of a micro-SOFC unit by ALD alone would require long time, and the cost (related to the equipment and precursors) would be prohibitive for mass-scale production [11].

Therefore, the microfabrication routes hereby presented explored the combination of the two techniques mentioned above to fabricate reliable and thermomechanically stable ceramic membranes for micro-SOFCs.

4.3.1 Microfabrication flow

The microfabrication flow related to the abovementioned micro-SOFC design is hereby described. These processes and the order at which they are performed were chosen to minimize manipulation of the wafer as much as possible to reduce contamination. Despite the main steps of the microfabrication were maintained throughout this thesis, two different routes were undertaken either targeting the fabrication of small, squared membranes or large-area membranes consisting of an array of small circular membranes supported by doped-silicon slabs. These two routes are hereafter described.

4.3.1.1 Small membranes fabrication

The fabrication of small, squared membranes, Figure 4.2, consists of few first steps devoted to the substrate preparation (1-3) performed at the IMB-CNM clean-room facility. Starting off a 4-inches silicon wafer, 300 μm-thick and (001)-oriented, the dielectric bilayer consisting of SiO_2 and Si_3N_4 was grown on both sides of the wafer (see Chapter 2.2.1). Subsequently, the wafer was transferred to the ALD chamber where a 20-nm thick ZrO_2 layer, namely OVSZ (see Chapter 3.3.1), was deposited on the top side (4). The substrate wafers resulting from these processes exhibit very smooth surfaces (on both sides) and the films deposited are homogeneous across the whole area of the wafer. Subsequently, the wafer is transferred inside the PLD vacuum chamber where the YSZ electrolyte and the air electrode (5) are deposited by adjusting the deposition conditions depending on the target material and desired morphology and microstructure of the films. A dense YSZ film was obtained by performing the deposition at 500 °C and at 1 mTorr of oxygen pressure in the chamber, while to obtain a dense LSC layer the temperature was raised to 600 °C and the oxygen pressure to 5 mTorr.

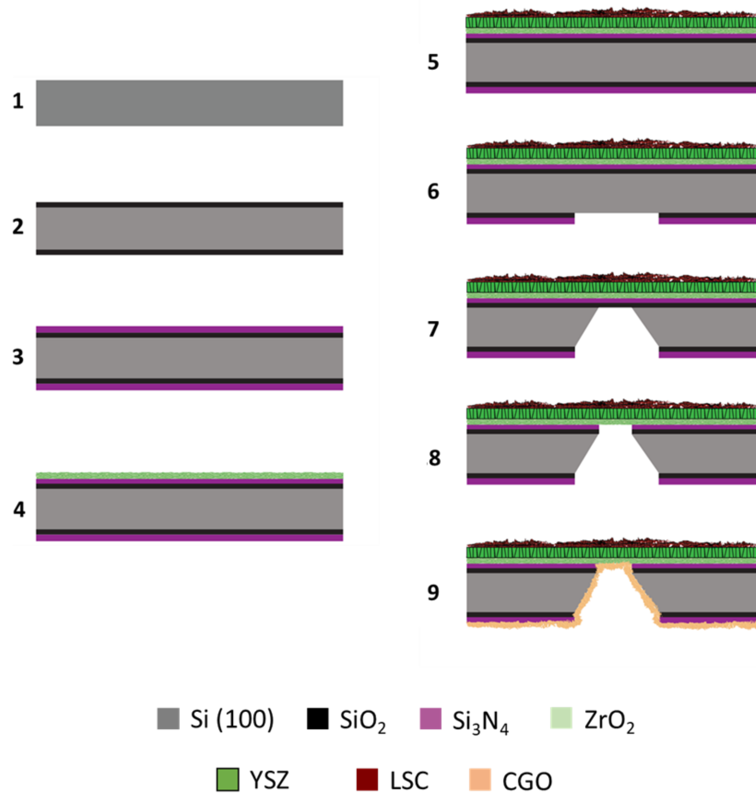

Figure 4.2. Microfabrication Flow of standard small, squared membranes

Once these two layers were deposited on top of the substrate, the wafer was transferred to the CNM clean-room and did undergo a cleaning process in water to eliminate the impurities coming from the atmosphere. At this point, the photolithographic step was performed on the back side of the wafer to define squared windows in the dielectric layer by RIE etching (6). The photolithographic mask used for patterning is shown in Figure 4.3.

Once these windows were exposing the bulk silicon from the substrate, the wafers were loaded on a customized PTFE holder that exposed only the back side of the wafer to a 40% KOH bath kept at 80 ºC. Etching of the bulk silicon (7) was finally carried out until reaching a selective layer (SiO_2) on the top side of the wafer. Subsequently, the back side of the wafer was exposed again to the RIE etching, removing the silicon dioxide and nitride left below the electrolyte (8) and resulting in the buckling of the membrane due to the residual stresses in the films. Uniform thermalization during the RIE process is especially crucial to avoid over-exposition and over-etching of the membranes located at the center of the wafer compared to those at the far side. The membranes obtained following this procedure ranged from 0.04 mm^2 to 0.64 mm^2, although the final active area depended on the porosity obtained through the metallic current collectors.

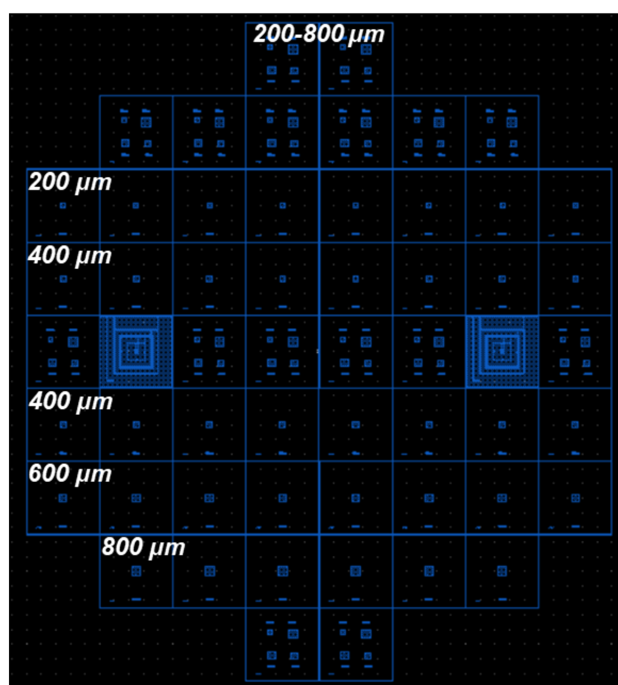

Figure 4.3. Design of the photolithographic mask used to fabricate suspended squared membranes with edge size ranging from 200 µm to 800 µm

Finally, the chosen fuel electrode (CGO) described in Chapter 3.2.2 was deposited on the back side by PLD to obtain the complete PEN element of the micro-SOFC device (9). To this end, the wafer was kept in the PLD chamber at 100 °C and 200 mTorr of oxygen pressure to obtain a highly porous electrode with low residual stress in order not to affect the mechanical stability of the membrane. By this step, the fabrication of the suspended ceramic membrane made of fully ceramic PEN tri-layer was completed and the results are reported in Chapter 4.3.3.

Nevertheless, a last fabrication step is devoted to the deposition of a current collector, used to compensate the limited electrical conductivity typical of CGO or thin films as a more general consideration. For standard squared membranes, Au and Pt thin films were evaporated directly onto the cathode and anode, respectively, targeting a thickness of 100 nm. The results of the deposition of current collectors are presented in Chapter 4.4.1.

4.3.1.2 Large-area membranes fabrication

The aspect ratio obtained on the squared membranes described above, thus using a basic micro-SOFC design, is commonly limited to less than 500x500 µm^2. Free-standing membranes with higher areas suffer cracks, which provoke leakages between both sides of the electrolyte and shortcuts the anode and the cathode of the cell. Eventually, cracks would lead to the rupture of the membrane upon thermal cycling. This limitation on the maximum area achievable imposes a limitation on the maximum power that can be obtained with single device. In this chapter an approach for enlarging the size of the membranes by using a mesh of doped silicon slabs as supporting structure is presented.

Figure 4.4 below shows a schematic top-view representation of the design adopted for the large-area membranes fabrication. It consists of an array of circular membranes, 200 µm in diameter,

separated by doped-silicon slabs used as mechanical support of the same. If overviewed from the top, a platinum current collecting grid can be observed, overlapping the same doped-silicon region in order to collect electrons from the edges of the membrane and thus maximize the active area of the cell exposed to the atmosphere.

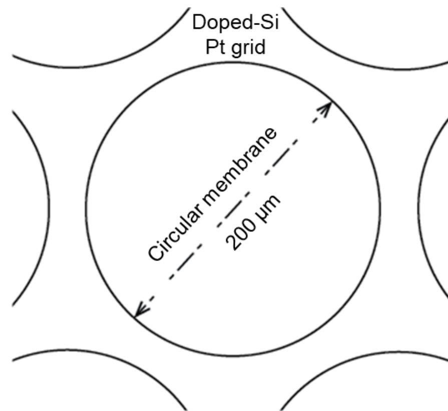

Figure 4.4. schematic representation of the pattern used to define an array of circular membranes in a large-area micro-SOFC unit

The microfabrication flow designed for this specific fabrication is depicted in Figure 4.5. Here, the fabrication steps related to the substrate preparation were different from those described for the standard membranes, since the selective doping of the silicon substrate occurred in the very first steps (1-5). Indeed, thermally grown SiO_2 micro-machined by subsequent photolithography and RIE was used as a hard mask for the selective doping obtained by boron thermal diffusion (4) [12]. After this step, the microfabrication resembled the one previously described for the small, squared membranes, despite using different masks for the etching on the back side of the wafer (7-11). Also, the Pt grid used for current collection was fabricated by consecutive photolithography and lift-off processes (7), overlapping the doped-Si grid previously defined.

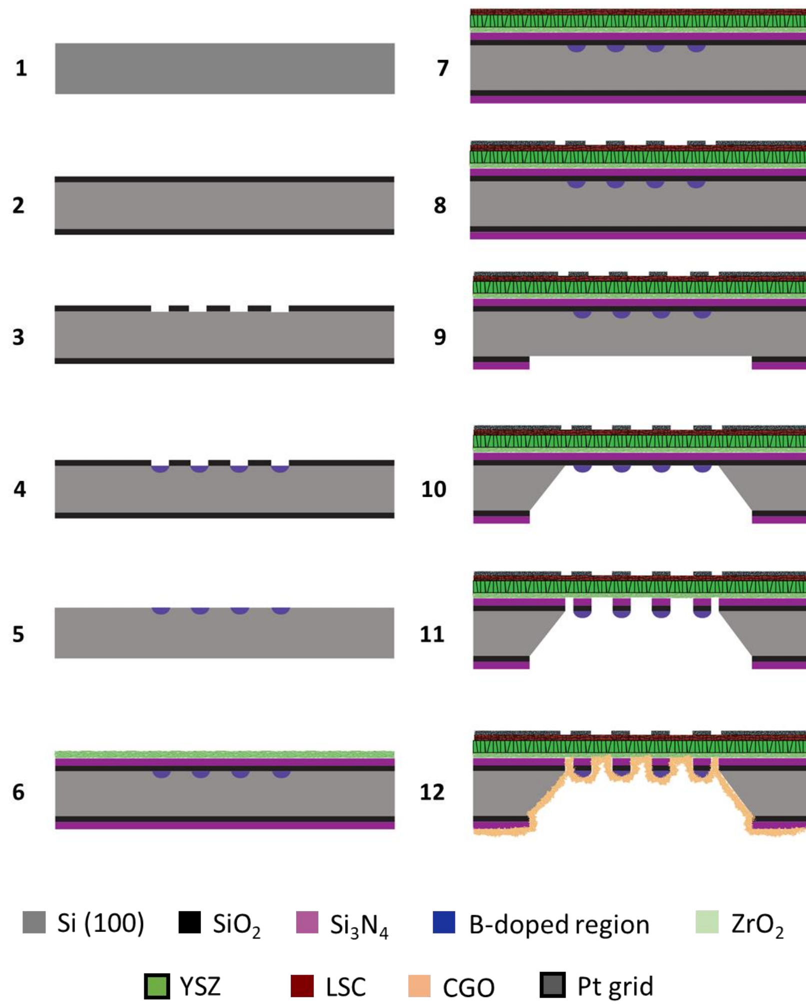

Figure 4.5. Microfabrication flow designed to fabricate large-area membranes

The microfabrication flow hereby presented allowed for obtaining large-area membranes ranging from 1 to 82 mm^2 active area (100% area utilization) within the same wafer, resulting in a 125-fold increase compared to the standard squared membranes presented in the previous section. Figure 4.6 below shows the lithographic mask used for the silicon doping and the platinum grid (Figure 4.6-a) and the one used for the RIE etching of the dielectric layer on the back side to define the final suspended region (Figure 4.6-b). It can be observed that within the same wafer, membranes of different size could be obtained, demonstrating the optimal thermalization of the wafer during RIE. The results of the fabrication of large-area membranes are presented in Section 4.3.3.

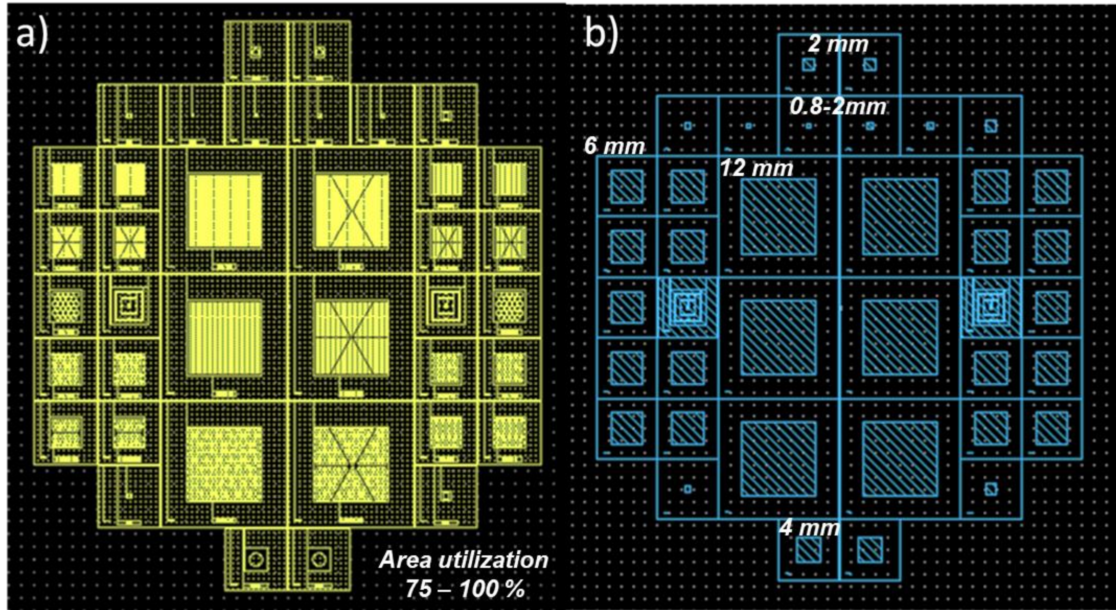

Figure 4.6. Design of the photolithographic mask used to fabricate arrays of circular membranes supported by doped-silicon slabs

4.3.2 Characterization and balance of residual stresses for deposited layers

Before showing the membranes resulting from the microfabrication processes, it is worth mentioning the important step of stress balancing typical of multi-layer devices. Such a characterization and optimization of residual stresses resulting from multiple film deposition is necessary to ensure the thermo-mechanical stability of the membrane during fabrication (to avoid the membrane rupture) and during operation.

The residual stress of each deposited film was analyzed by measuring the curvature of a silicon wafer before and after deposition, precisely knowing the thickness of the layer deposited. The resulting stress was calculated using the modified Stoney equation (see chapter 2.2.2.1) [13]:

$$\sigma_f t_f = \frac{h^2}{6(s_{11} + s_{12})R}$$

where σ_f is the in-plane stress component in the film, t_f the thickness of the film, h the wafer thickness and R = $(1/R_f - 1/R_{sub})$ being R_f and R_{sub} the curvature radii of the substrate after and before deposition, respectively. Whereas s_{ij} are elements of the compliance tensor of silicon, the numerical value for $1/(s_{11}+s_{12})$ is 1.803(1)×1011 Nm^{-2} based on the stiffness values found in literature.

According to the microfabrication flow, the most relevant materials for which the residual stress must be optimized are the electrolyte (YSZ by PLD and pure-ZrO_2 by ALD) and the air electrode. These materials and their residual stress will indeed be responsible for the buckling of the membrane after etching the substrate [14]. Assuming the uniform deposition of such materials on the whole wafer area, the deposition parameters affecting the residual stress are:

- Deposition temperature (at the substrate)

- Deposition chamber pressure
- Laser fluence (for PLD)

In this work, the laser fluence is fixed depending on the target material and previously optimized by our group in order not to damage the target and reduce particles ejection. On the other hand, previous studies [15,16] showed how the deposition temperature affected the residual stress resulting from YSZ deposition by PLD. From buckling and XRD analysis, the deposition temperature leading to the highest compressive stress was found to be around 400 ºC and progressively decreasing when the temperature was increased up to 700 ºC.

An intermediate temperature (T = 600 ºC) was chosen as a starting point, which is expected to give compressive stress and a crystalline film, together with a chamber pressure of 5 mTorr for ensuring a dense film deposition. Figure 4.7 shows the curvature of the substrate wafer (including the dielectric bilayer, subtracting the reference measurement) after deposition of the YSZ electrolyte with different deposition parameters.

The preliminary deposition conditions chosen for 3YSZ led to a dense film with residual tensile stress, as shown in Figure 4.7-a. In order to increase the impingement effect of ionic species onto the substrate upon deposition, eventually leading to the compressive residual stress in the deposited film, the deposition temperature was reduced from 600 ºC to 500 ºC (Figure 4.7-b) and the laser fluence taken to its maximum power (Figure 4.7-c). Despite changing these parameters would affect the residual stress resulting in a mild tensile stress, the oxygen pressure (pO_2) was found to be the ultimate parameter affecting the residual stress of the film. Indeed, Figure 4.7-d shows that reducing the pO_2 from 5 mTorr to 1 mTorr in the deposition chamber results in a greater change on the residual stress, finally obtaining the compressive stress necessary to the buckling of the membranes. Hence, one can deduce that the kinetic energy of the ionic species is strongly affected by the pO_2 in the chamber, causing a greater impingement of the atoms and leading to a compressive residual stress in the film [17].

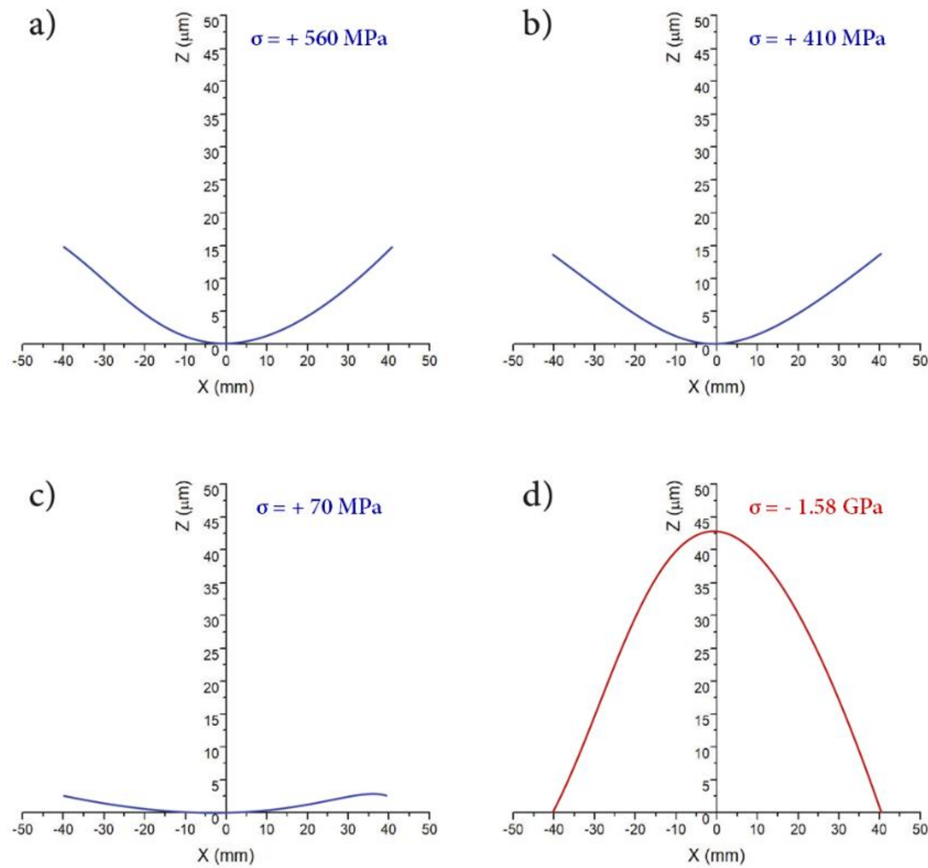

Figure 4.7. Optical microscopy wafer profile measurements to assess the residual stress in 3YSZ thin films. (a) T_{dep} = 600 ºC, P = 5 mTorr, Fluence F = 0.35 J/cm^2; (b) T_{dep} = 500 ºC, P = 5 mTorr, Fluence F = 0.35 J/cm^2; (c) T_{dep} = 500 ºC, P = 5 mTorr, Fluence F = 0.4 J/cm^2; (d) T_{dep} = 500 ºC, P = 1 mTorr, Fluence F = 0.4 J/cm^2;

The stress analysis was then performed on all films deposited on the top face of the substrate and affecting the buckling of the membrane after etching, when the films finally undergo relaxation caused by the substrate removal. Figure 4.8 shows the analysis performed on the electrolyte bilayer (OVSZ by ALD + 3YSZ by PLD), the LSC air electrode and finally the thermal stress relaxation upon annealing at 700 ºC. This final step is performed to determine the thermal stress relaxation to decide if the annealing should be performed prior substrate etching, which is not the case.

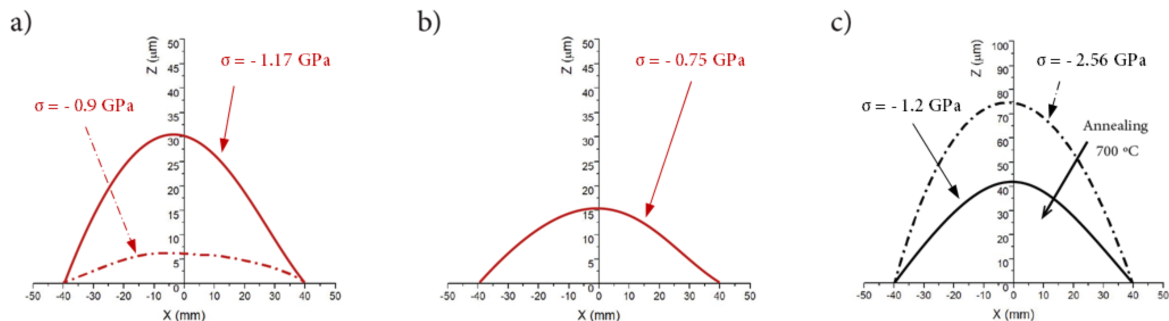

Figure 4.8. Stress analysis on different ceramic layers. (a) Stress measured after OVSZ deposition and subsequent addition of the 3YSZ layer; (b) Stress measured after deposition of the cathode; and (c) Stress reduction after thermal post-processing at 700 ºC.

This analysis was performed on every batch of samples fabricated throughout this thesis, ensuring compressive residual stress, and eventually enabling the more reliable fabrication of corrugated self-standing membranes with a higher yield.

4.3.3 Microfabrication results

The optimization of the microfabrication flow using large substrates (4-inches silicon wafers), together with a thorough control over the residual stress of the thin films after deposition, resulted in a very solid and high-throughput method for fabricating suspended ceramic membranes. Indeed, up to fifty-two 1x1 cm^2 devices could be fitted in one single wafer. Figure 4.9 below shows the optical image of the wafer resulting from the fabrication before evaporation of the current collector. Here, ununiform thicknesses of the active layers can result in change of colors of the membranes, that can be observed for both standard (Figure 4.9-a) and large-area membranes (Figure 4.9-b) fabrication. Nevertheless, it was observed that as long as the thickness of each layer was maintained within a 10% standard deviation, thermomechanical stability of the membranes was maintained. The only circular membranes that did not survive a thermal cycle up to 650 ºC were those with a diameter between 1 and 2 mm without doped-silicon grid support, therefore remarking the capability of such structure to increase the active region per unit cell.

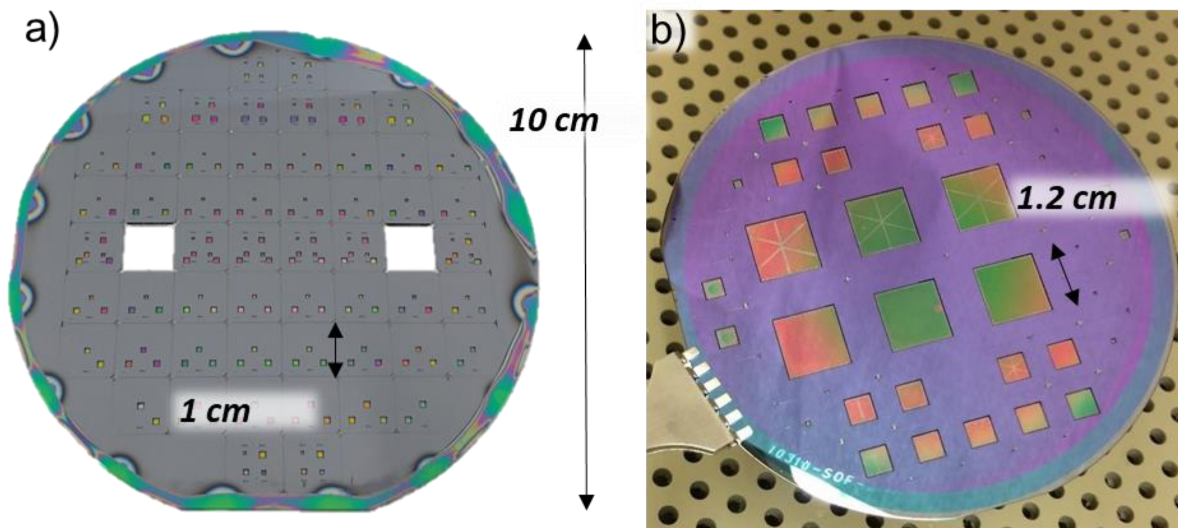

Figure 4.9. Optical images of the 4-inches wafer comprising of (a) small, squared membranes, (b) large-area membranes

The optical image of standard squared membranes (size ranging from 200 to 800 μm) is included in Figure 4.10-a, whereas the arrays of circular membranes (200 μm in diameter) supported by doped silicon slabs is shown in Figure 4.10-b. The observed buckling profiles are consistent with studies in literature and previous analyses of our group [15,18,19].

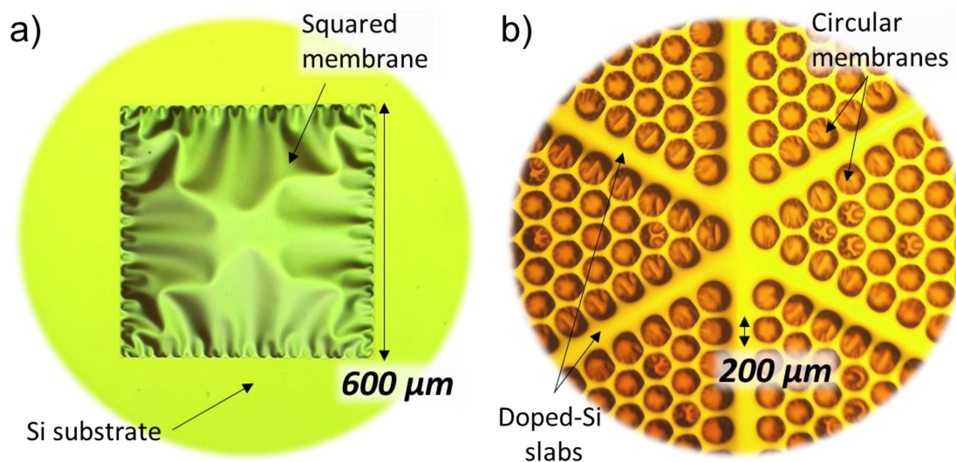

Figure 4.10. Optical microscopic image of (a) small, squared membrane and (b) array of small circular membranes supported by doped-silicon slabs

The most innovative component of the large-area membranes, i.e., the doped-silicon slab, is shown in Figure 4.11-a. The penetration depth of the boron atoms during the doping process was directly dependent on the temperature of the furnace that in this case was optimized to 1250 °C. At this temperature, the resulting doped-Si slab measured 5 µm in depth and, according to the design previously presented, about 20 µm in width. This grid-like suspended structure was able to provide great robustness to support the ceramic membranes and was designed to fit the highest density of membranes possible. Indeed, Figure 4.11-b shows the geometry obtained for the membranes array, where the ratio between the silicon-slab width (20 µm wide) and the diameter of the circular membrane (200 µm) lead to an overall 75% area utilization calculated with simple trigonometry.

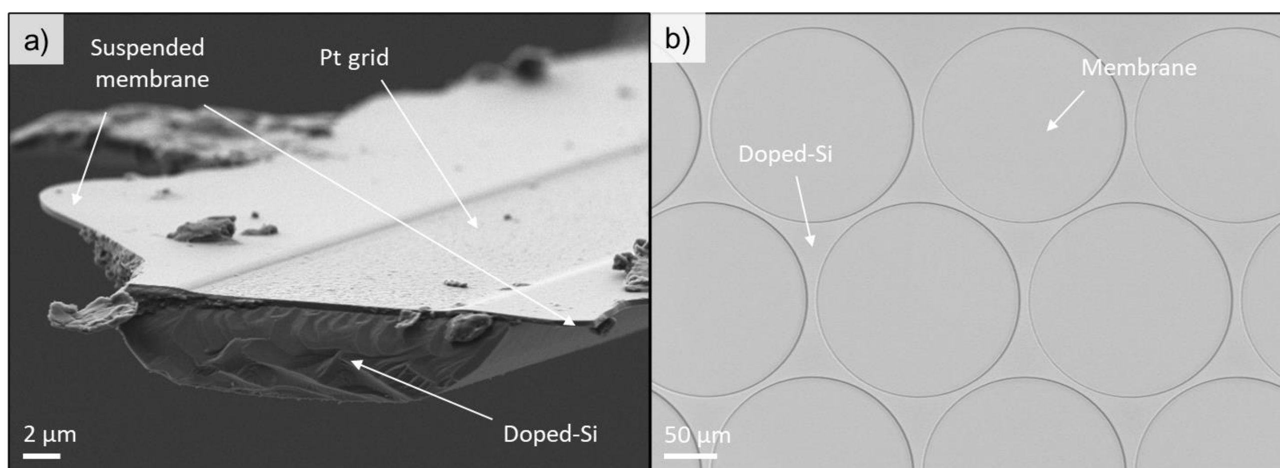

Figure 4.11. (a) Cross-section SEM image of a doped-Si slab after RIE and (b) top-view optical microscopy image of the supported membranes array

The membranes presented the same PEN structure (see Figure 4.12) but differentiate from the current collecting layer at the cathode side, which is fabricated through a photolithographic step following the doped silicon features, thus not covering the membranes but collecting current from the sides (as described in Section 4.3.1.b). This way, the actual superficial area where the electrochemical reaction occurs is maximized, providing a framework for the fabrication of robust, large-area and efficient power generators.

Specifically, in Figure 4.12-a on the left one can notice that the PEN element of the membrane is approximately 500 nm-thick, halving the thickness of a previous micro-SOFC presented by IREC group [12]. On the other hand, Figure 4.12-b on the right shows the PEN element at the edge of the circular membrane, where a doped silicon slab is present underneath the CGO anode and where the current collecting film is precisely defined by lift-off.

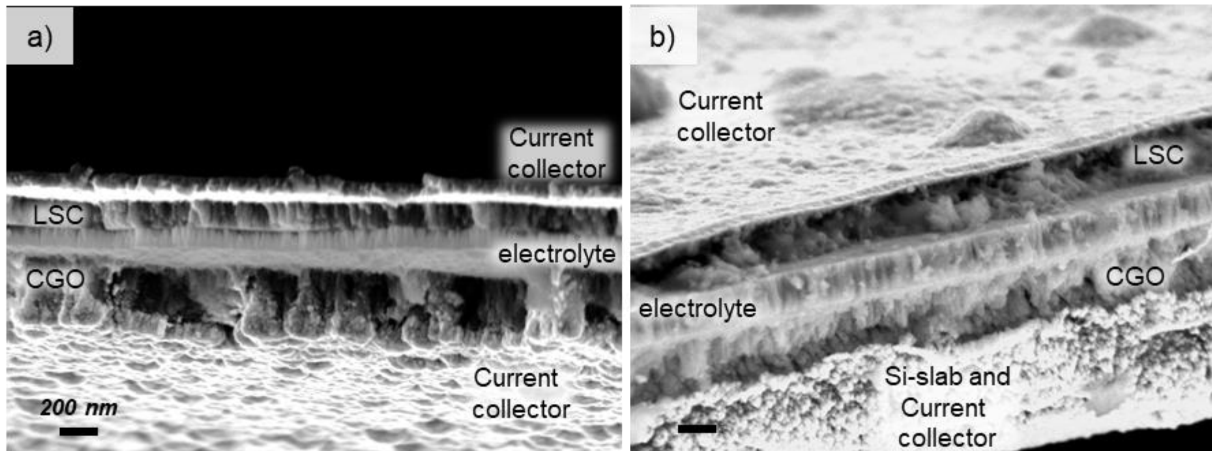

Figure 4.12. Cross-section SEM images of the PEN structure of a (a) squared membrane and a (b) circular membrane comprising of a doped-Si slab and micropatterned current collector

Finally, a size comparison of different membranes designs with a 10 Eurocents coin is presented in Figure 4.13. It is evident that the microfabrication approach adopted in this chapter succeeded on improving the reliability and yield of the process, and to scale-up the size of the active area for eventually increasing the power output of a single micro-SOFC unit.

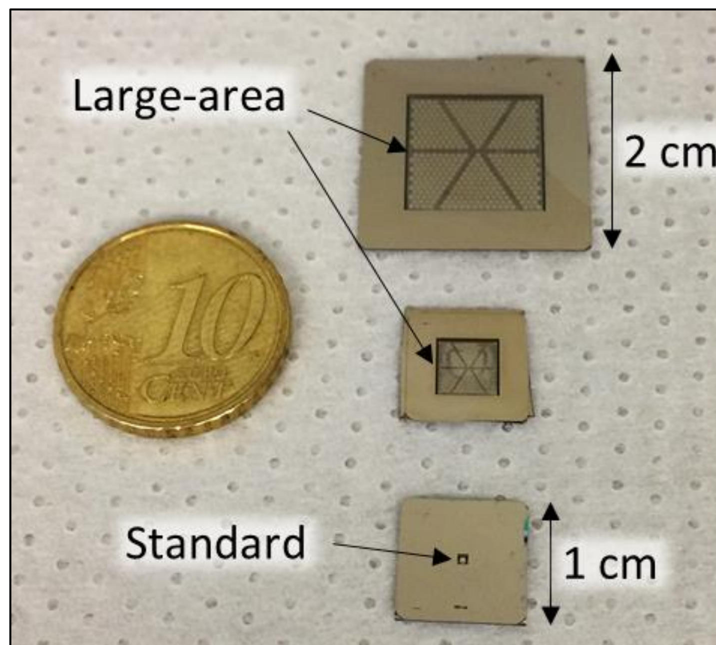

Figure 4.13. Optical image of three micro-SOFC units with suspended membranes of different size and comparison with a 10 Eurocents coin.

4.4 Micro-SOFC characterization

In the following, the electrical characterization of the active materials constituting the micro-SOFC unit is presented. Prior electrochemical testing of the micro-power generator, the optimization of the metallic current collector was performed to ensure compatibility of the materials and avoid the loss of electrical contact, a common phenomenon occurring when operating at high temperature (see Chapter 1.3.1.2).

4.4.1 Current collectors

At this stage of the technology development, metallic current collector (Au, Pt, Ag, Ni etc.) are still necessary to ensure sufficient electronic conductivity and reduce power losses related to the low in-plane conductivity of thin-film perovskite materials, especially when presenting porous morphology.

The first approach tackled in this thesis was the evaporation of a 100 nm-thick Pt layer on both electrodes of the micro-SOFC and the subsequent thermal treatment to obtain a controlled Pt de-wetting. Nevertheless, an unexpected phenomenon occurred at the cathode side when the cell was undergoing thermal post-treatment. Indeed, no de-wetting was observed even when the temperature was as high as 900 °C. As shown in Figure 4.14, the Pt layer did not present any evident porosity and was maintained dense. Such a dense layer prevented the gas to reach the electrode and thus any subsequent electrochemical reaction at the cathode's surface.

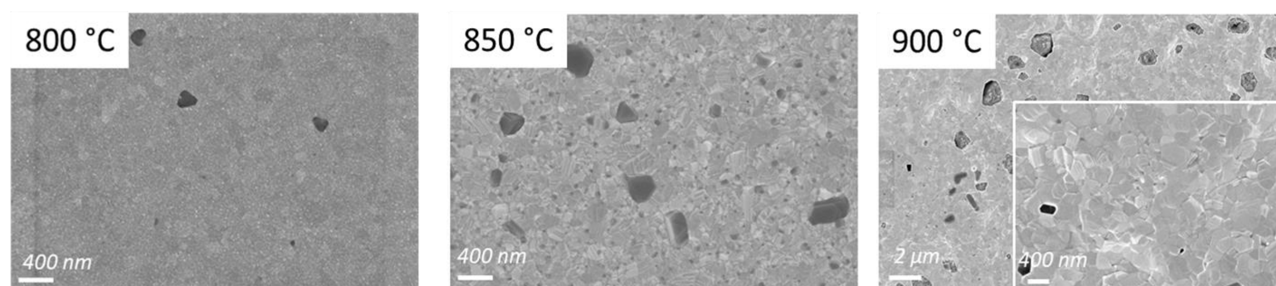

Figure 4.14. Top-view SEM images of a 100 nm-thick Pt film evaporated on top of the LSC cathode film after annealing at different temperatures

Although XRD analysis was carried to check for the formation of secondary phases or Pt-Co alloys, it was not possible to understand the striking adhesion of the Pt layer to the LSC layer.

Since it was not possible to create a porous current collector with a conventional approach based on dewetting of noble metals, a second strategy was followed where the evaporation of Au replaced the Pt at the cathode side. Figure 4.15 shows that the Au current collector does not behave as previously observed for Pt, and a clear coarsening phenomenon can be observed when increasing the temperature of annealing. While a temperature setpoint of 800 °C would cause a complete loss of the electrical network (Figure 4.15-a), it is possible to observe from Figure 4.15-(b,c) that the optimal temperature range for operation of such system can be found between 600 and 700 °C, temperature at which the loss of connectivity was starting to occur.

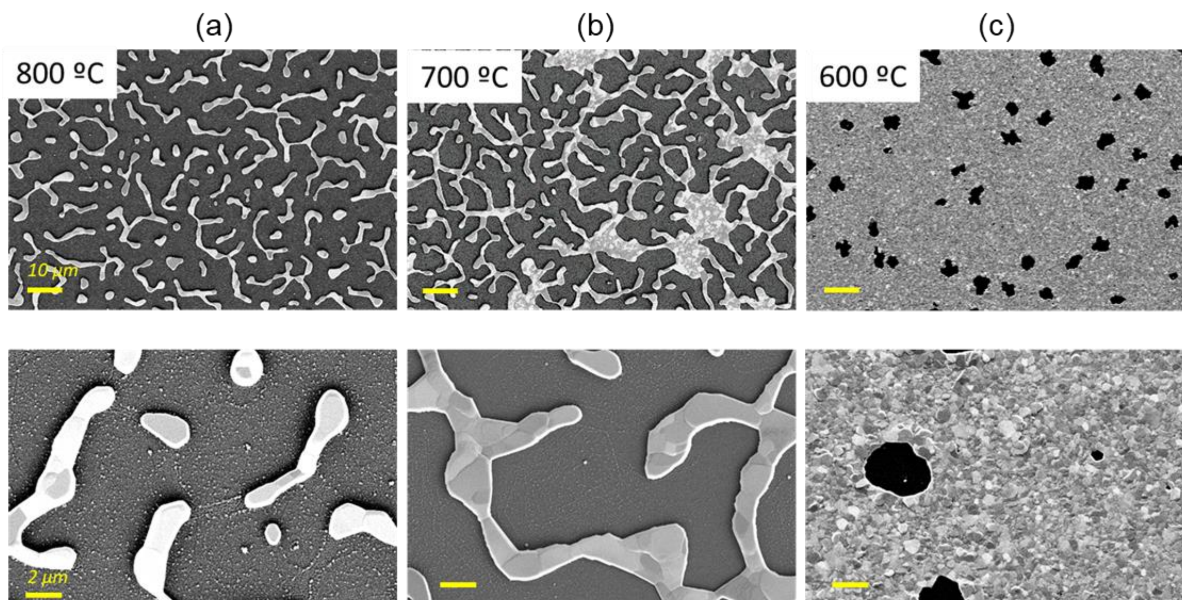

Figure 4.15. Top-view SEM images at different magnification of a 100 nm-thick Au film evaporated on top of the dense LSC cathode film and annealed at (a) 800 ºC, (b) 700 ºC and (c) 600 ºC for 3h.

To confirm if the in-plane conductivity of the so-fabricated Au current collector was maintained upon operation, 4-point Van der Pauw electrical measurements were performed while heating the substrate from room temperature up to 650 ºC. The results are reported in Figure 4.16, showing an increasing sheet resistance with temperature up to a temperature of 650 ºC and with a slight deviation from the reference values reported for these metals mostly due to the porosity. After 6 hours measurement at 650 ºC (maximum temperature of the Linkam hot-plate) the connectivity was still maintained, allowing for higher area utilization than compared to Figure 4.15-c.

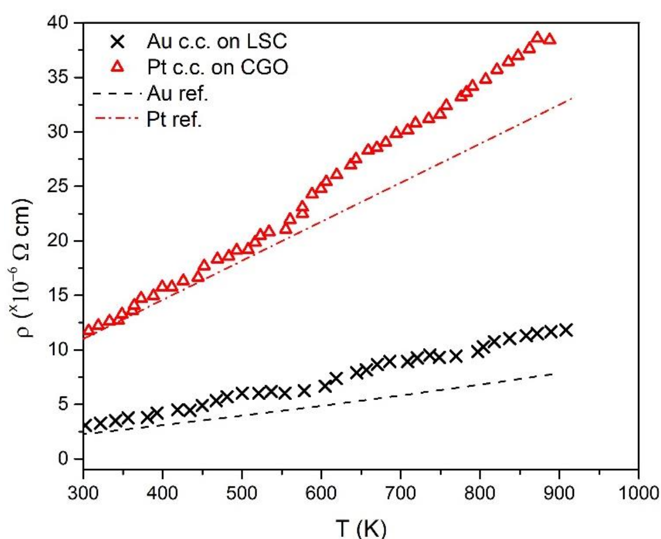

Figure 4.16. Resistivity vs. Temperature for both gold and platinum-based current collectors (thickness 100 nm) obtained from Van Der Pauw measurements.

Therefore, a thermal treatment at 650 ºC for 3h was performed prior any micro-SOFC measurement, as presented in the next chapter. The area utilization resulting from this thermal process was calculated from the top-view SEM image at the cathode side, included in Figure

4.17, and accounted for about 32% of the overall membrane area. This value was included in the calculations presented in the following section about the micro-SOFC performance.

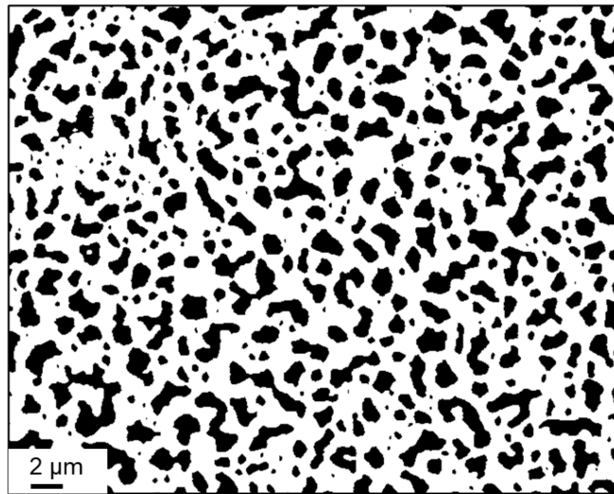

Figure 4.17. High-contrast top-view SEM image of the gold current collector (in white) on top of the cathode (in black) after thermal processing at 650 °C for three hours and at 600 °C for six hours.

It is important to mention here that the approach presented in this thesis is currently under revision in our research group since the current collectors obtained by dewetting did not provide fully satisfactory results neither in terms of performance nor in terms of stability. Currently, ongoing approaches pursue buried current collection or, alternatively, micro-patterned fully dense metallic areas with promising results, especially regarding the stability.

4.4.2 Micro-SOFC characterization

This section is dedicated to the electrochemical characterization of a micro-SOFC unit fabricated according to the processes and materials described in this chapter. Figure 4.18 below shows the details of a cross-section of the fabricated cell comprising of the novel OVSZ layer.

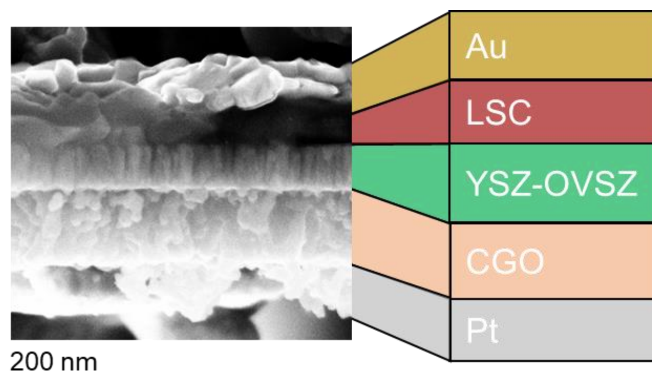

Figure 4.18. Cross-section SEM image of the ceramic PEN tri-layer and current collectors measured in the Probostat cell.

The micro-SOFC hereby presented was mounted in a Probostat cell and treated at 650 °C for 3h in inert atmosphere prior measurement, to allow some porosity through the gold current collector. The electrochemical characterization of the micro-SOFC was performed by

galvanostatic measurements and reported in Figure 4.19. Once the gases were fed to the micro-SOFC, an OCV of 0.8V could be obtained, far from the ideal value of 1.0-1.1 V expected at this temperature. Most likely, the poor OCV performance is due to hydrogen leakages from the fuel to the air chamber. This issue was observed in other measurements carried out during this thesis and it is attributable to the complexity of the measurement setup, especially regarding the sealing, since silicon's TEC (Thermal Expansion Coefficient) barely matches with the high-temperature ceramic materials used in this work, causing cracking or porosities to appear. Indeed, this mismatch resulted in dramatic failure and break of the samples in multiple occasions.

Despite this fundamental issue, specific power higher than 40 mW/cm^2 could be achieved at T = 600 °C with the present PEN design, which can be considered a proof of concept for the micro-SOFCs fabricated in this thesis.

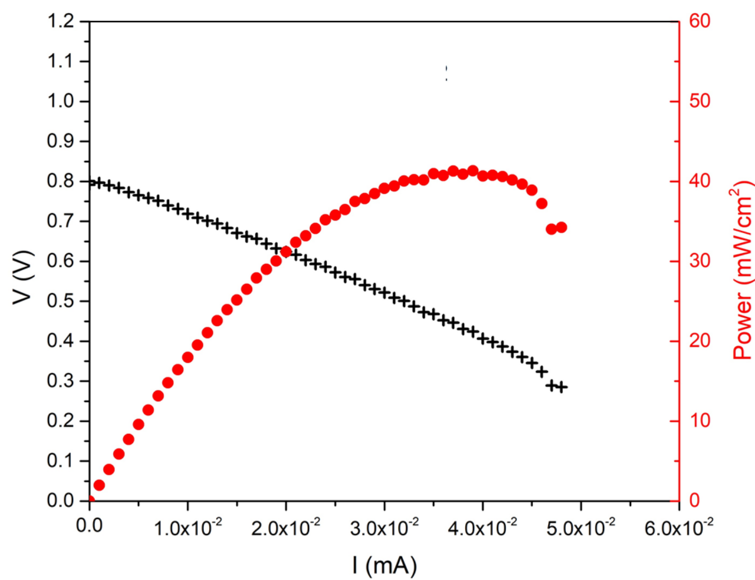

Figure 4.19. IV curve and area-specific power output of a micro-SOFC membrane measured at 600 °C

Although lower than expected, the power output obtained by a single squared membrane indeed reaches the one reported for state-of-the-art devices [12] and opens-up new possibilities to implement advanced MIEC materials and cutting-edge nano-composite materials [20,21] on a robust and pinhole-free electrolyte using a high-throughput fabrication route for industrial scale-up.

To better understand the different contributions to the total resistance of the micro-SOFC device, EIS analysis was performed after the 5%-H_2 and air gas flows were fed to the anode and cathode chambers, respectively. Figure 4.20 below reports the Nyquist plot from the impedance spectrum recorded at 650 °C at OCV. The spectrum could be fitted according to the equivalent circuit model presenting a resistance (Rs) in serie with two RC circuits (R_i, Q_i) as previously explained in Chapter 3.2.2.

The serial resistance Rs was attributed to the sum of contributions of YSZ ionic conductivity (R_{YSZ}), cabling (R_{cables}) and current collection (R_{CC}) and its values was ~8 Ω, as shown in the inlet, corresponding to an ASR of ~0.03 Ω cm^2. On the other hand, the high-frequency arc is associated to non-charge transfer phenomena at the anode side, where a contribution from the ionic conductivity of CGO can also be expected [16]. Finally, the high capacitance (C ~ 10^{-3}-10^{-4} F cm^{-2}) observed for the low frequency arc is consistent with the concept of chemical

capacitance observed for MIEC materials [22,23] and was attributed to the cathode. Therefore, the air and fuel electrodes presented an ASR of about 5 and 7.8 Ωcm^2, i.e., more than one order of magnitude higher than the expected contribution of the electrodes of a working device, expected to be below 0.15 Ωcm^2 [24].

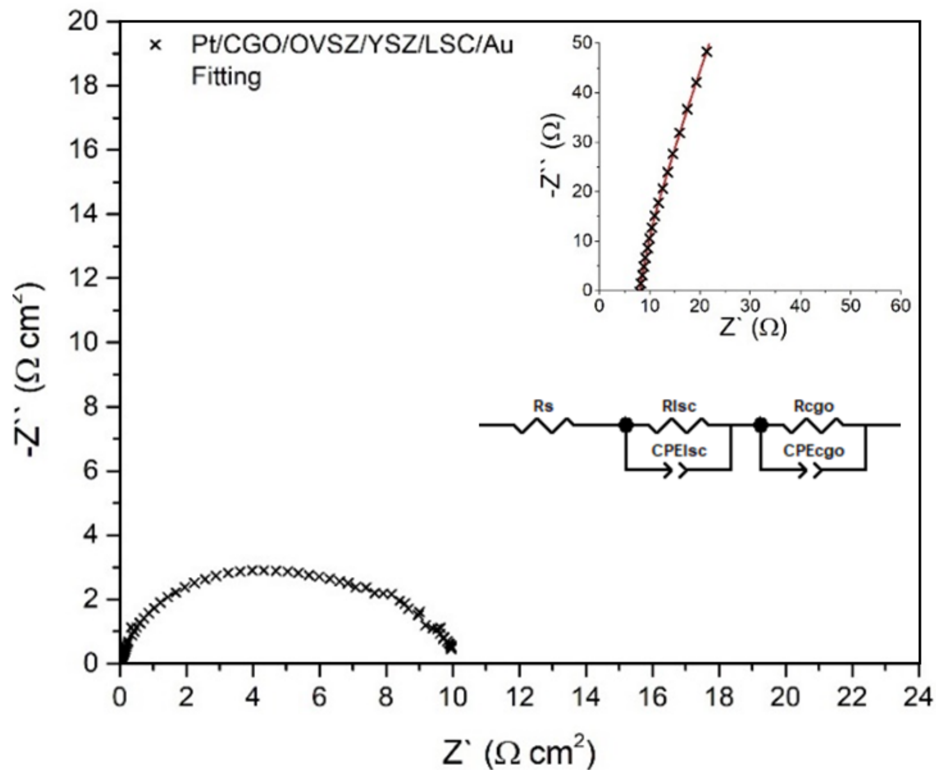

Figure 4.20. Nyquist plot from impedance measurements of a fully ceramic micro-SOFC at 650 ºC. 5% H_2 in Ar is fed to the anode side, while synthetic air was used as oxidizing. The inlet represents a magnification of the high-frequency part of the spectrum. The equivalent circuit used for fitting is also included

Opposite to squared membranes that provided reasonable performance, measurements on large-area membranes resulted in very low power outputs (< 1 mW/cm^2 at 600 ºC) as shown in Figure 4.21. Although it was not possible to clearly establish the main reason of the poor performance of our large-area membranes, it is interesting to notice that an OCV of about 1.1 V was obtained, highlighting the potential of the electrolyte bilayer for producing pinhole-free ceramic membranes.

The under-performing character of perovskites thin films exposed under UV light was suggested by previous studies [25]. According to these studies, the effect of photolithography on a perovskite film's surface could cause strong degradation with an ASR increase by a factor of 10-100.

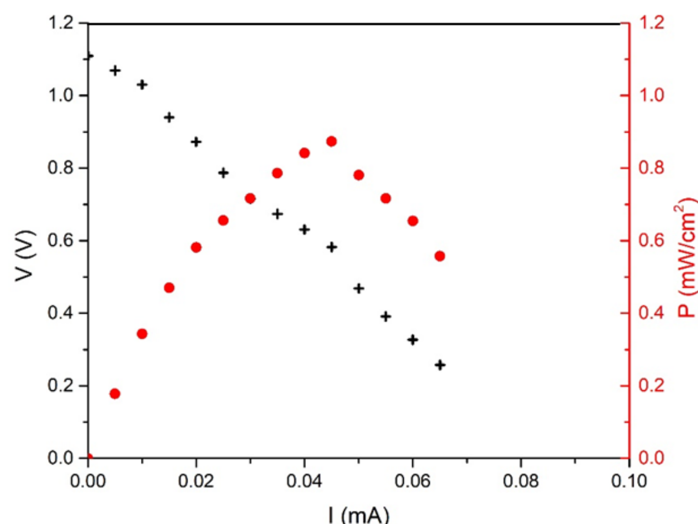

Figure 4.21. IV curve and area-specific power output of a micro-SOFC large-area membrane (3 mm^2) measured at 600 ºC

To overcome this, a new current-collecting embedded microgrid for applications in thin-film devices was implemented, to avoid exposure of the electrode to photolithographic steps. Especially in the case of the large-area membranes fabrication, a 10 nm Ti + 100 nm Au microgrid will be first defined onto the YSZ electrolyte by lift-off process, and only afterwards a porous LSC air electrode is deposited on top thus avoiding exposure to UV light. This work is out of the scope of the current thesis and the preliminary results are not included here.

4.5 Conclusions and perspectives

In this chapter, a new reliable microfabrication route for micro-SOFCs was presented, where a suspended ceramic electrolyte membrane based on zirconia was fabricated by ALD and PLD (see chapter 3) allowed for pinhole-free membranes fabrication. State-of-the-art MIEC conductors such as $La_{0.8}Sr_{0.2}CoO_3$ and $Ce_{0.8}Gd_{0.2}O_2$ were used as air and fuel electrodes, respectively, according to the selection criteria mentioned in Chapter 1 and 3.

Thorough characterization of the residual stresses in the films resulting from the chosen deposition techniques was performed to ensure the thermomechanical stability of the suspended ceramic multi-layer membranes. To this end, the curvature profile of the 4-inches wafer was measured and the stress calculated using the modified Stoney equation [13].

The results of the wafer-level microfabrication were presented, with a focus on the modification of the fabrication flow to increase the active area per cell while maintaining a stable and robust structure. Indeed, doping the silicon substrate with boron allowed for the creation of a doped-silicon grid further used as a support for an array of small, circular membranes. This way, the active area of the micro-SOFC unit was increased by 125 times.

Finally, optimization of the current collection at the cathode side was necessary to ensure compatibility of the materials and specially to allow access of the gases to the electrodes while maximizing the active area for the redox reactions to occur. The final results obtained for the

current collection strategy based on dewetting of metals was not fully satisfactory and further work is in progress to develop highly performing and long-term stable collectors.

A single squared membrane unit was characterized by EIS and galvanostatic measurements and resulted in a power output of 40 mW/cm^2 at 600 °C, similar to previous state-of-the-art performances reported in literature [26] and accounting with a fully ceramic PEN structure with improved thermal stability compared to pure metallic electrodes [16] at the expenses of a lower hydrogen oxidation reaction (HOR) performance of the anode. Several issues employing conventional sealing led to multiple dramatic failures and low OCV values. Alternative approaches based on mainstream encapsulation processes are highly recommend (see Chapter 5.4)

All in all, this chapter described a novel and scalable fabrication method for robust ceramic membranes with high-throughput and potential to increase the power output per single micro-SOFC unit by two orders of magnitude compared to previous methods. To reach this goal, currently existing issues regarding current collection and sealing should be faced and fixed.

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CHAPTER 5

ELECTROCHEMICAL OXYGEN MICRO-SENSOR BASED ON CERAMIC THIN FILMS

Electrochemical oxygen micro-sensor based on ceramic thin films

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5.1 Introduction

In recent years, the digital revolution, and the impact of Internet-of-Things (IoT) on the industry seek the possibility to integrate sensors at large scales for real-time monitoring of the industrial processes. To do so, oxygen sensors should be placed in high-temperature regions and should take advantage of the heat of the process, therefore lowering the energy consumption needed to heat up the sensing unit [1].

On one hand, the fabrication of electrochemical oxygen sensors usually results challenging especially regarding the choice of materials for the encapsulation and the hardware that is quite limiting. Indeed, typical lambda sensors comprise an internal heater to make the sensing possible at lower temperature, thus allowing for use of common materials for the hardware [2]. An interesting approach for miniaturization of sensing devices presented in the past included the micromachining of a suspended hotplate used for local heating of the sensing unit only, while maintaining the rest of the hardware at lower temperature [3]. Nevertheless, the fabrication of a fully integrated device for high-temperature applications (e.g., water boilers or industrial power-plants) is still limited by the choice of materials for encapsulation.

In this regard, silicon-integrated electrochemical cells based on YSZ electrolytes are an appealing approach due to their miniaturization and mass manufacturing potential at low cost. Indeed, the integration of ceramic thin films on silicon substrates for oxygen sensing had already been explored in the past [4,5].

In this chapter, a new design for miniaturized oxygen sensors based on MEMS technology is presented. The concepts previously illustrated for silicon-based micro-SOFC are hereby reproduced aiming at the fabrication of a ceramic-based sensing platform, and a new encapsulation strategy based on glass-ceramic materials is developed, taking inspiration from state-of-the-art miniaturized sensors [6,7] and aiming at extending the temperature range of application for electrochemical oxygen sensors. Indeed, glass-ceramic sealings have shown great potential to provide great hermeticity and stability upon operation in harsh environment, as in the case of SOFC technology [8–10].

5.2 Miniaturized electrochemical oxygen sensor

In the following, an innovative design for a miniaturized potentiometric oxygen sensor based on silicon and ceramic active materials is presented. A scalable microfabrication approach based on large (4-inches) substrates was implemented and the results of the fabrication of the different components of the sensors are included.

5.2.1 Design

In this section, the design of a miniaturized and fully integrated potentiometric oxygen sensor is presented. Like for micro-SOFCs in Chapter 4, the sensing unit of the device is based on a small circular suspended membrane including a PEN tri-layer, current collectors, a dielectric

bilayer and a doped-Si region both for electrical contact and thermalization of the specimen. Moreover, a reference chamber was achieved by the encapsulation of the bottom part of the sensor using a HOYA glass cover and adding a metal/metal-oxide powder mixture as a buffer (the role of this buffer material is explained below). A high-temperature glass-ceramic sealing was used to ensure a gas tightness in the reference chamber. In Figure 5.1 below it is possible to appreciate both cross-section and top-view schematic representation of the integrated device proposed for this thesis.

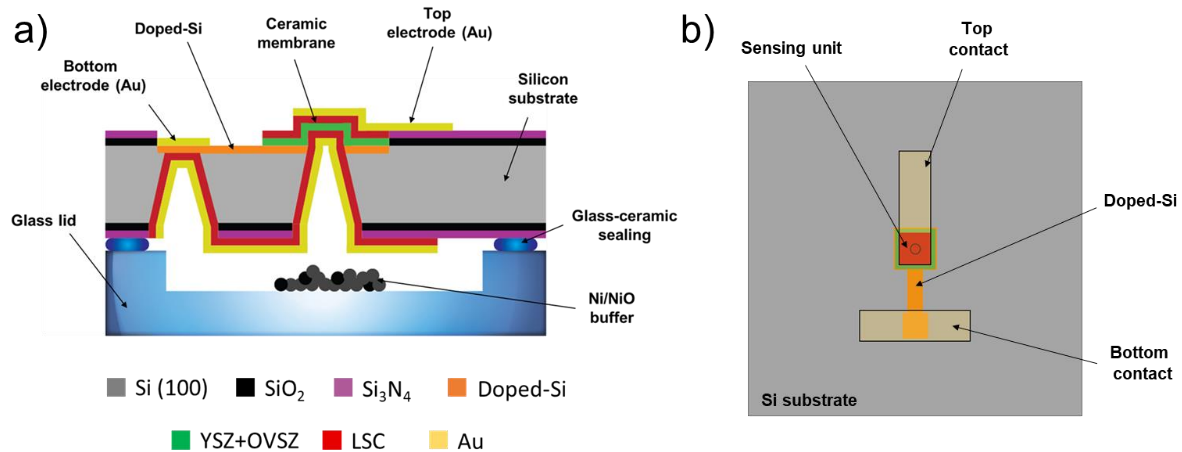

Figure 5.1. Schematic representation of the (a) cross-section and (b) top-view of the miniaturized oxygen sensor with embedded reference atmosphere.

The innovative sensing platform hereby presented aimed at simplifying the current collection through an enclosed chamber by creating a through-silicon-via (TSV) by selective doping of silicon. The B-doped regions were about 5 μm-thick (see Chapter 4.3.3) and were designed to extract the bottom contact from the embedded reference chamber up to top of the device. Although doping of the region surrounding the membrane could involve a certain reduction of the thermal conductivity, a highly uniform thermalization of the sensing region is still expected [11]. Doping levels of about ~10^{19} atoms/cm^3 were the estimated outcome of this thermal diffusion processes [12], which is expected to result in a thermal conductivity high enough (in the order of 125 W/mK).

A metal/metal-oxide powder mixture (Ni/NiO with ratio 1:4) was also included within the reference chamber as a buffer, in order to maintain a constant reference atmosphere that could be affected by long-term measurements causing drift [13,14]. Finally, the glass-ceramic sealing was proven to perform well at temperatures up to 600 °C and to match the CTE of silicon and HOYA glass (sensor lid), thus preventing for cracks and leakages upon operation. Further details are presented in Chapter 5.3. The commercial HOYA glass wafer used for the encapsulation was also micro-machined by using *ad hoc* optimized HF etching to create a reference chamber where the metal/metal-oxide mixture could be accommodated.

Interestingly for further developments, the design hereby presented is highly flexible to include multiple sensing membranes onto a single device that can be electrically connected in serial configuration, hence amplifying the output voltage signal for a more precise sensing by eliminating the need of amplification systems [4,15].

5.2.2 Fabrication flow

This section provides the microfabrication flow used to obtain the miniaturized oxygen sensing platforms and its subsequent encapsulation, as shown in Figure 5.2.

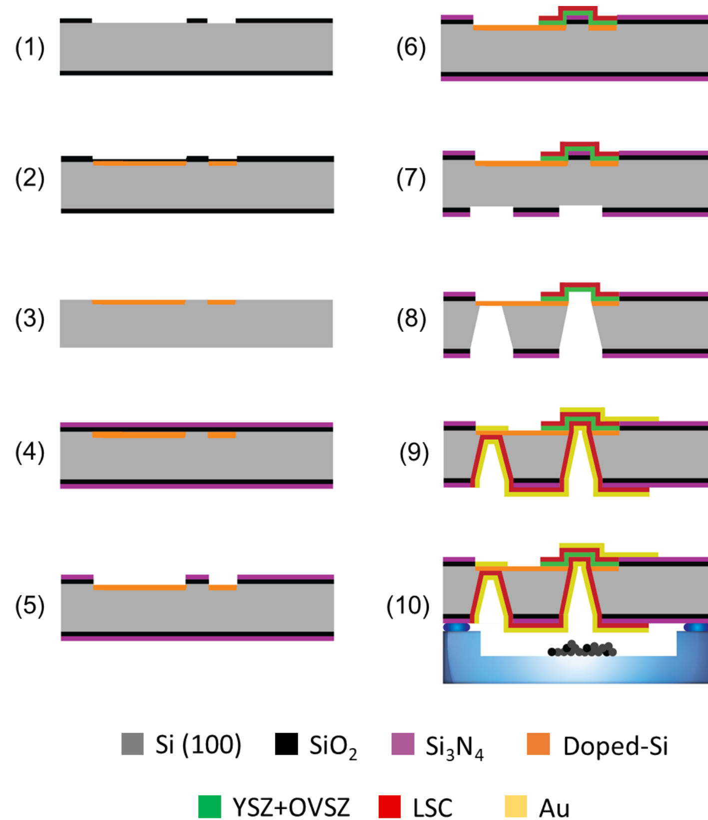

Figure 5.2. Microfabrication flow of a fully integrated miniaturized oxygen sensor with internal reference atmosphere

First, (1) a thermal SiO_2 (1 μm-thick) dielectric layer was grown on both sides of the silicon wafer and used as a mask for (2) the selective doping of silicon to create the TSV-like conductive paths and thermalization pools. Subsequently, (3) wet etching was performed to remove all the oxide from the wafer surface, since a thin oxidation layer was present on top of the doped region. Next, (4) a typical SiO_2/Si_3N_4 bilayer was grown on both sides of the wafer and (5) selectively etched by RIE on top of the doped region following a photolithographic step. Hence, (6) the electrolyte and top electrode were selectively deposited using a silicon wafer hard mask (see Figure 5.4-a).

Then, the back side of the wafer went through a photolithographic step to define the (7) etching regions that eventually constituted the doped-Si contact and the sensing membrane, (8) first by etching in KOH and later by RIE (as in Chapter 4.3.1). Finally, (9) the reference ceramic electrode was deposited by PLD on the back side in a symmetric way to the one deposited on the top of the wafer. Current collectors are then evaporated on both sides using a hard mask to prevent electrical short circuits. The last step (10) to obtain a fully integrated oxygen sensor was the encapsulation. Further details on the processes described above can be found in Chapter 2.2.1.

The silicon-based hard mask was fabricated using 500 μm-thick silicon wafer and by etching in KOH the bulk silicon, masking the surface with Si_3N_4. During the photolithography step, alignment of the mask with the sensor's wafer was necessary to ensure high precision of this multi-level process. Squared openings were eventually obtained and overlapped onto the sensor's wafer with very good tolerances (displacement < 100 μm). Very little amount of Ag paste was placed between the sensor wafer and the hard mask to function as a "glue" during the PLD process, to avoid any rotation of the hard mask with respect to the substrate, that could eventually be rinsed quickly with isopropanol.

Once the sensing platform was fabricated and tested for absence of pinholes, the encapsulation was performed depositing the sealing slurry by robocasting onto a sensor lid (see Chapter 2.3.1). Here, the slurry prepared according to the procedure described in Chapter 2.3.1 was added to a syringe equipped with a 0.36 mm nozzle to obtain a fine line. Multiple layers were deposited on top of each other until obtaining a line thickness required for optimal sealing (see Section 5.3)

The sensor lid was obtained starting from a commercial HOYA wafer, 1 mm in thickness, where amorphous silicon (750 nm-thick) was deposited by PECVD to use as an etching mask. Subsequently, the squared features were defined in the silicon film by photolithography and RIE etching, and finally the glass substrate was etched in a HF 50% solution for about 20 min [16], aiming at creating a 150 μm deep pool that would contain the reference gas for the sensor.

Both processes described above are depicted in Figure 5.3.

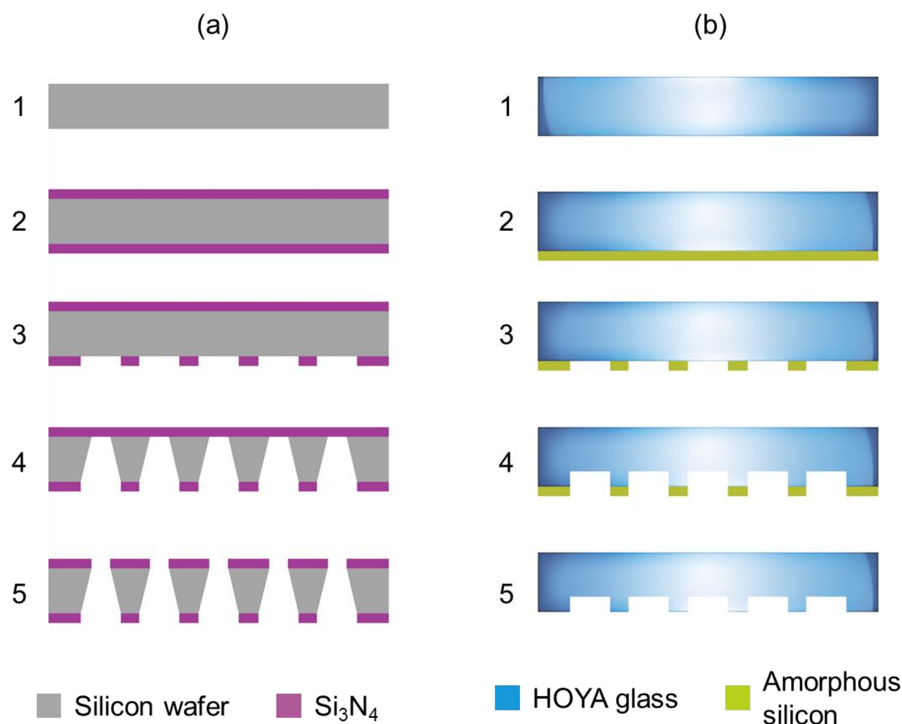

Figure 5.3. Microfabrication flow dedicated to the creation of (a) silicon-based hard mask for PLD depositions and metal evaporation, and (b) a sensor lid based on HOYA glass.

The metal/metal-oxide mixture was placed into the lid and finally the sealing was placed by robocasting controlling the line width and thickness. The joint with the sensing platform was

therefore performed and thermally treated. The details about the encapsulation are included in Chapters 2.3.1 and 5.3.

5.2.3 Fabrication results

The selective deposition of functional thin films in different regions of the wafer was the first challenge to be solved. As mentioned in the previous section, the fabrication of a silicon-based hard mask was necessary to this aim. Figure 5.4-a shows the optical image of the wafer after deposition of the electrolyte and electrode, where the hard mask (dark color) is aligned and overlapped to the wafer to enable the selective deposition in the ALD and PLD. Especially for the case of ALD, masking is non-trivial due to the conformal character of the technique. For this reason, the sensor features were designed considering a shading effect of about 1 mm underneath the mask. The result of the selective deposition can be appreciated in Figure 5.4-b.

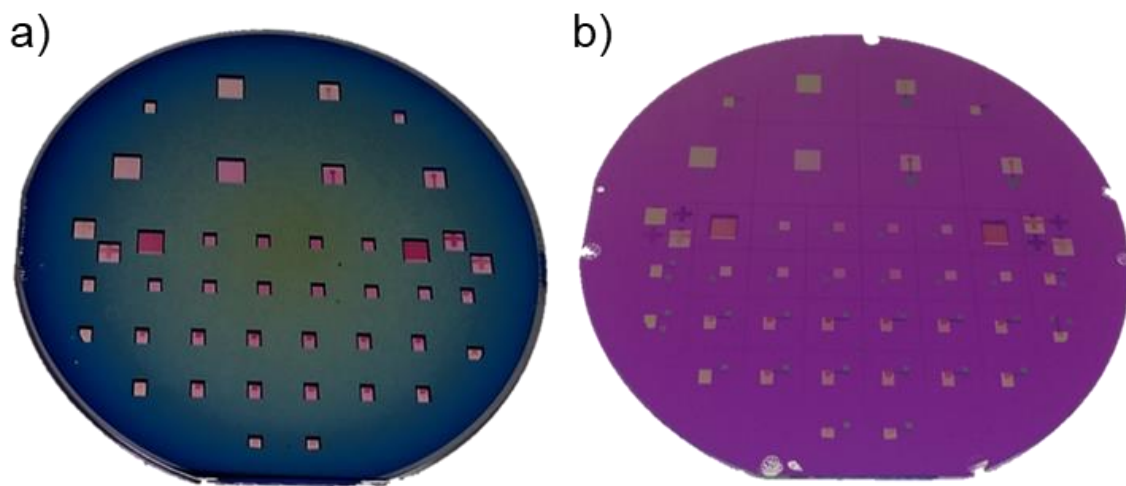

Figure 5.4. Optical image of the micromachined wafer (a) with a silicon hard mask on top for selective thin-film deposition and (b) after its removal

Within the same wafer, devices of 2x2 cm^2 and 1x1 cm^2 were obtained as shown in Figure 5.5-a, where the final configuration comprising of the current collector can be observed. The top-view optical image of the suspended circular membrane and the surrounding doped-Si pool for thermalization is included in Figure 5.5-b.

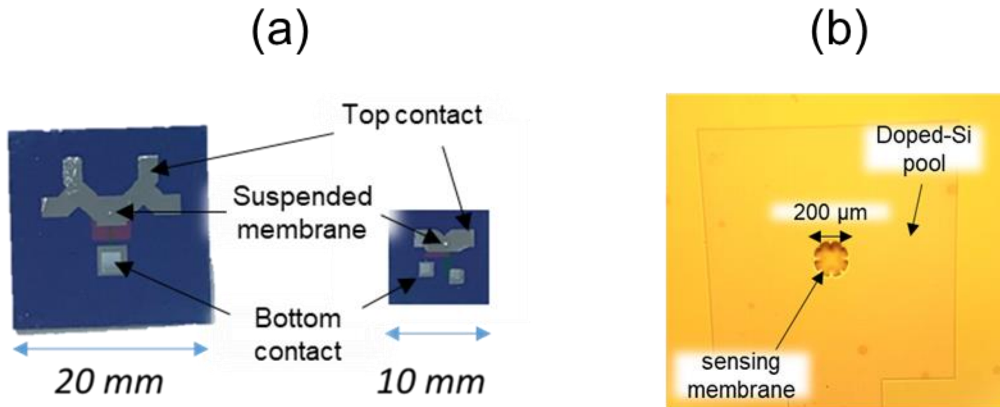

Figure 5.5. (a) Top-view optical image of the miniaturized sensors and (b) optical microscopy image of the membrane and the surrounding doped-Si pool

The cross-section SEM images of the suspended membrane are represented in Figure 5.6. Here, a fully dense self-standing 150 nm-thick YSZ electrolyte (see Chapter 3.2.2) is separating two symmetric electrodes (same material in both sides). The electrodes are made of LSC perovskite thin films of about 40-50 nm in thickness that were therefore deposited by PLD on both sides of the YSZ electrolyte. In Figure 5.6-a one can appreciate that the back electrode covered homogeneously the edges of the membrane, which was a typical issue and a challenge in similar micro-SOFC devices. Indeed, the optimized RIE process eliminated the issues related to over-etching of the dielectric layer. On the other hand, Figure 5.6-b shows a detail of the sensing membrane where the columnar structure typical of the YSZ electrolyte [17] is clearly visible.

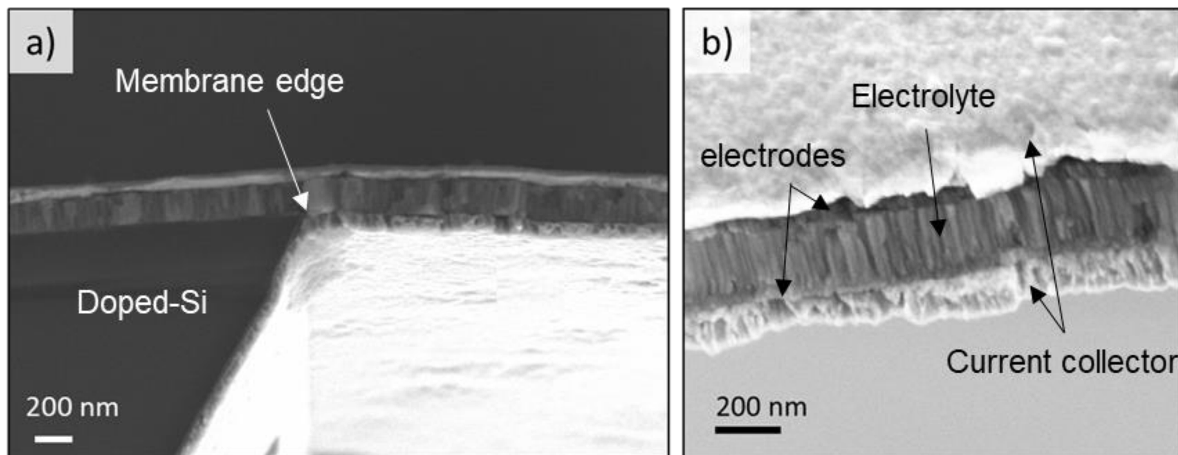

Figure 5.6. Cross-section SEM images of the sensing unit as fabricated. (a) Detail of the edge of the membrane, and (b) higher magnification on the YSZ electrolyte with two symmetric LSC electrodes and Au current collectors

Finally, the HOYA glass wafer employed as lid for encapsulating the devices is shown in Figure 5.7 after micro-machining. Pools of different sizes were obtained within the same wafers following the wafer-level design of the sensor for future direct encapsulation between two wafers. After etching in HF solution, the glass wafer showed rough surface due to re-deposition of glass particles onto the surface, but mostly limited to the region within the reference chamber.

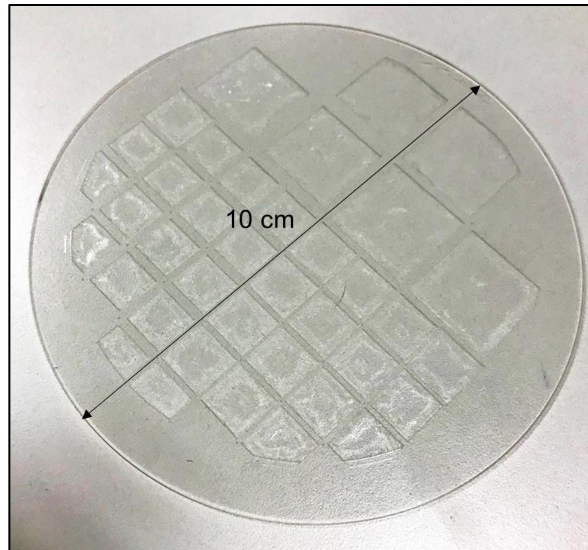

Figure 5.7. Optical image of the micro-machined glass lid at wafer-level

5.3 Encapsulation by high-temperature gas-tight sealing

The encapsulation and gas tight sealing is highly important for a gas sensor because it allows for the creation of a gas-tight chamber with a controlled reference atmosphere, i.e., a fundamental component of the sensor design presented in this study.

After the evaluation of several options for the sealing of the sensor (see section 2.3.1), the glass frit was considered the best solution as the parts to be joined are not perfectly flat and do not present smooth surfaces (required for other bonding techniques, e.g., anodic bonding [18]). The glass frit approach consists on a glass powder-based slurry placed between two surfaces and fired in air following a specific thermal treatment that depends on the glass composition. The deposition of the paste was performed using a robocasting machine that allowed great geometrical flexibility and precise control on the thickness and width of the extruded line. More details about this technique are described in Chapter 2.3.1. Among a wide variety of glass-frit materials available in the market, the G018-197 commercial powder from SCHOTT was selected due to its high substrate wettability together with a relatively low firing temperature, that for this type of sealants can reach maximum temperatures above 1000 ºC.

The paste deposition technique chosen in this work is called robocasting, i.e., a CAD-driven printing process usually employed for printed circuit boards (PCB) and very similar to the common liquid deposition modeling (LDM) 3D printing technique described in Chapter 2.3.2. The advantage of such technique compared to other suitable methods (e.g., screen-printing) stands in its versatility towards different geometries. The robocasting machine uses thin nozzles to extrude the glass-frit paste and deposit it with accuracy on the substrate. Therefore, an extrudability tests was essential for evaluating the correct extrusion of the paste through the nozzle. Different powder loadings were tested aiming at finding a homogeneous composition with the highest loading that was possible to extrude through a nozzle (360 μm in diameter). The 80-20 (%wt.) powder-to-binder ratio was thereby characterized to assess the feasibility of integration in a silicon-based high-temperature system.

The rheological behavior of the paste to be employed was thus characterized with a viscosimeter and reported in Figure 5.8. In particular, Figure 5.8-a reports the measurement of viscosity vs. time for different shear rates, confirming the required thixotropic behavior of the paste, while Figure 5.8-b reports the typical viscosity vs. shear rate plot (left Y-axis) and the flow curve (right Y-axis) that confirm an adequate shear thinning properties of the paste for a proper deposition with robocasting. According to the power law formula reported below

$$\eta = m|\dot{\gamma}|^{n-1}$$

where η is the viscosity, m a constant, $\dot{\gamma}$ the shear rate and *n* the dimensionless flow behavior index, a shear thinning behavior corresponding to a value of n<1 (n = 0.51) is observed.

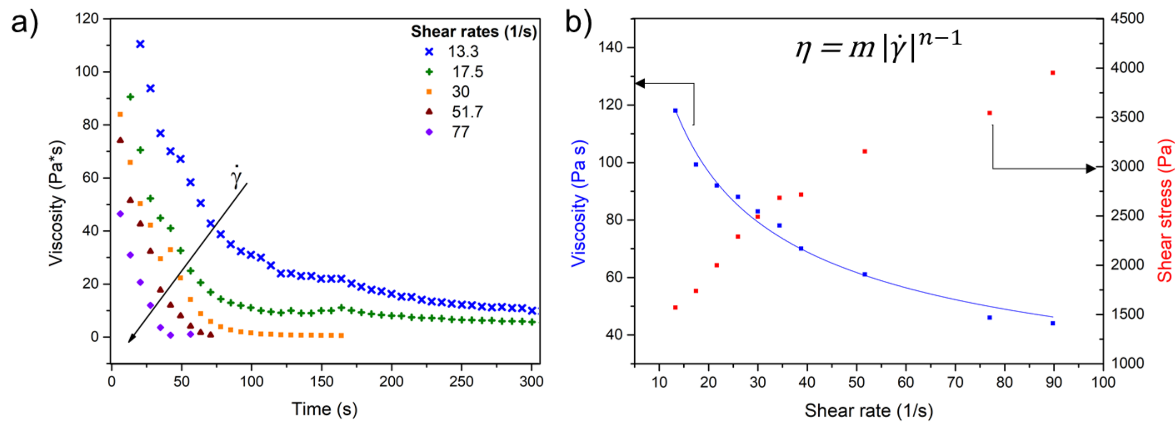

Figure 5.8. Rheological properties of the slurry. (a) viscosity vs. time at different shear rates and (b) viscosity vs. shear rate (left Y-axis) and flow curve (right Y-axis).

In second place, the thermal joint profile necessary to perform the sealing had to be studied and well controlled to ensure compatibility of the sealing with the silicon's CTE. Given glass-transition temperature of the chosen glass frit powder (T = 557 °C) according to specifications, we designed and characterized two different joint profiles, both including a temperature hold at 350 °C for de-binding but with different maximum temperature setpoints, i.e., 650 °C and 700 °C (Figure 5.9).

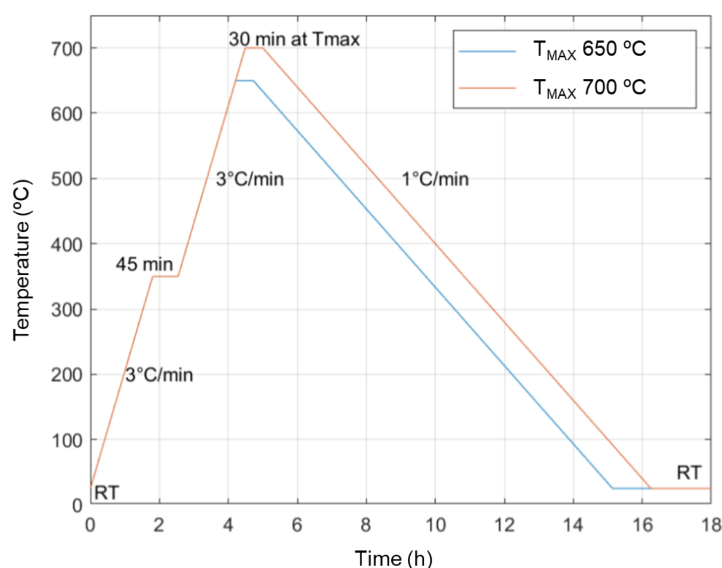

Figure 5.9. Experimental joint profiles studied in this work

The combination of DSC, in-situ thermal XRD, EDX, HSM (hot-stage microscopy) and dilatometry techniques allowed for a careful characterization of this high-temperature sealant for micro-SOFCs.

Differential scanning calorimetry (Figure 5.10-a) clearly showed the glass-transition temperature at 557 °C, as well as few more endothermic peaks at higher temperature associated to additional exothermic processes. These peaks are observed at 660 °C and around 690 °C, while further crystallization processes are expected to occur at firing temperatures above 750 °C.

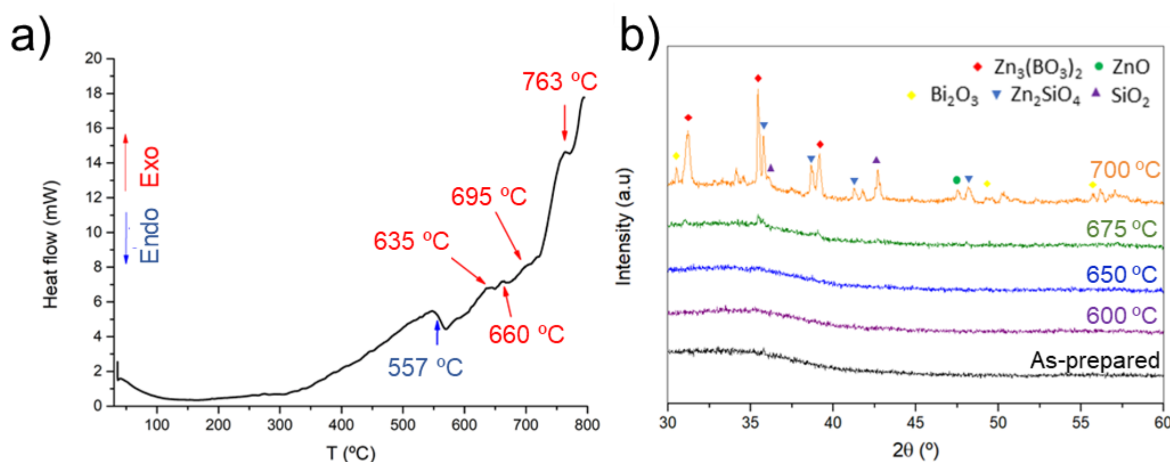

Figure 5.10. Characterization of the crystallization temperature by (a) DSC and (b) in-situ thermal XRD.

In parallel, in-situ thermal XRD analysis (Figure 5.10-b) was performed on a 500 μm-thick sealing paste layer deposited by conventional doctor blade technique onto a silicon chip. The first peaks in the pattern are observed at 675 °C and belong to the $Zn_3(BO_3)_2$ and Zn_2SiO_4 phases, while at higher temperature the degree of crystallization increases and crystalline phases belonging to ZnO, SiO_2 and Bi_2O_3 appear.

Finally, the morphology and chemical compositions obtained so far were confirmed by cross-section SEM and EDX analyses. Figure 5.11-a shows the joint fired at 650 °C, where no

crystallites are observed conversely to the joint fired at 700 °C included in Figure 5.11-b. Nevertheless, in both cases it is possible to observe some porosity and voids left by the binder that during the firing process are filled with the glassy material. In order to establish the composition either in the bulk joint or in these voids, EDX analysis was performed and included in Table 5.1.

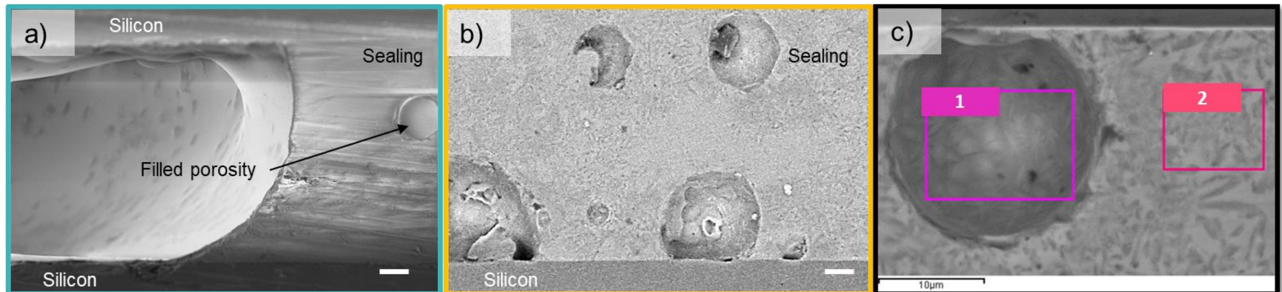

Figure 5.11. SEM images of the glass joint between silicon chips upon different thermal treatments, i.e., (a) firing at 650 °C or (b) 700 °C. (c) EDX analysis of the crystalline glass-ceramic phases after firing at 700 °C. The scale is 10 μm in all cases.

According to the results reported in Table 5.1, the bulk material is likely attributable to $Zn_3(BO_3)_2$, B_2SiO_5 or B_2O_3, while ZnO and Zn_2SiO_4 are those phases likely segregating into the voids. Further analysis should be done for a proper characterization of the sealant (out of the scope of this thesis).

Spectrum 1			Spectrum 2		
Element	Weight %	Atomic %	Element	Weight %	Atomic %
B	10.24	22.65	B	46.39	60.36
O	29.54	44.15	O	21.08	18.66
Si	2.75	2.34	Si	1.48	0.7
Zn	50.23	18.38	Zn	16.26	3.52
Sb	0.25	0.05	Sb	0.09	0.01
Ce	0.23	0.04	Ce	0.15	0.02
Bi	0.58	0.07	Bi	0.5	0.03

Table 5.1. Chemical composition of two different regions of the crystalline sealing treated at 700 °C, analyzed by EDX.

Regarding the compatibility of such sealant with silicon substrates and their vertical stacking, hot-stage microscopy (HTM)[2] was performed on a pellet to observe the volumetric evolution during the firing process. Figure 5.12 below reports the changes in volume observed upon firing up to 800 °C, where it can be seen a first shrinkage at 600 °C leading to 25% reduction in height of the pellet (1) and corresponding to the beginning of the sintering process (2). Above 650 °C we observed the so-called sphere temperature (3), used to assess at what temperature the softening of the glass occurs. Eventually, the final height of the pellet fired at 700 °C is 60% of the initial value (4). This result is technologically relevant to assess the thickness of sealing paste to be deposited on the interconnects and to obtain a controlled sealing.

[2] Measurements performed at Politecnico di Torino

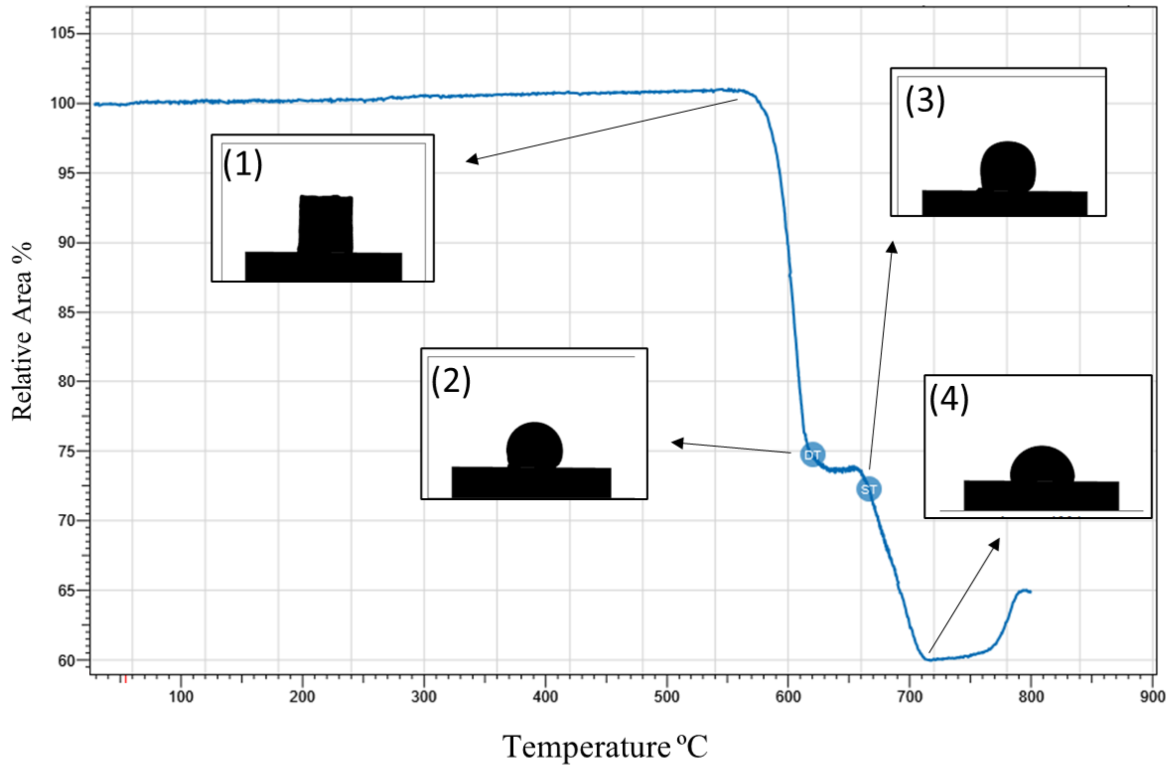

Figure 5.12. HSM of a glass pellet from room temperature to 800 °C. Micrographs report the (1) glass-transition temperature, (2) deformation temperature, (3) sphere temperature and (4) final deformation above 700 °C.

Finally, dilatometry tests were eventually performed to assess the CTE of the sealant resulting from the two different joint profiles. As it can be observed from Figure 5.13, the CTE closer to silicon's is obtained with the joint profile reaching 700 °C because of the crystallization process occurring above 650 °C. Indeed, the first joint profile firing at 650 °C shows a CTE of ~$5 \cdot 10^{-6}$ K^{-1} up to 300 °C and ~$6 \cdot 10^{-6}$ K^{-1} from 300 °C to 500 °C, while the second joint profile firing at 700 °C shows a CTE of ~$3.65 \cdot 10^{-6}$ K^{-1} up to 300 °C and then ~$5.2 \cdot 10^{-6}$ K^{-1} from 300 °C to 500 °C.

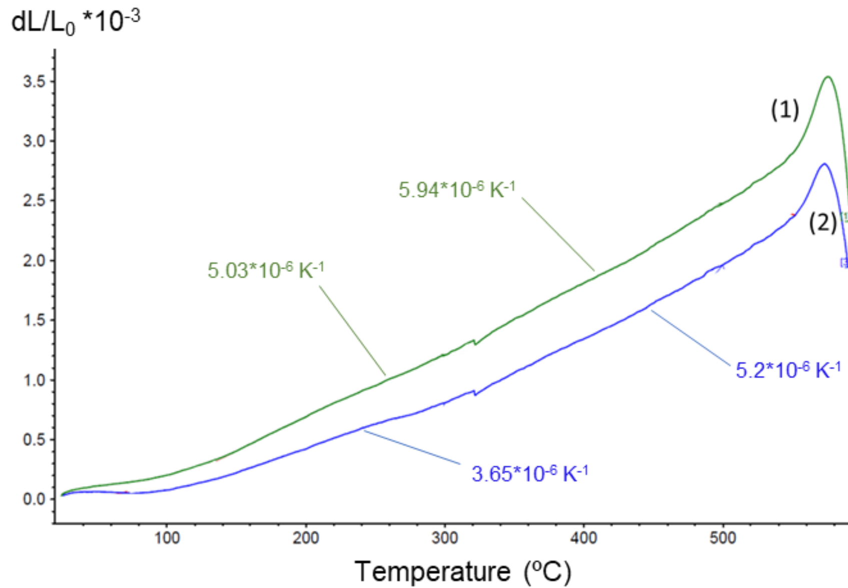

Figure 5.13. Dilatometry tests performed on samples fired at (1) 650 ºC and (2) 700 ºC.

Allowing for a better compatibility with silicon's thermal expansion [19], the chosen joint profile for the firing process of the glass-ceramic sealing follow the second route with the maximum temperature setpoint of 700 ºC upon firing.

Finally, to achieve the best quality of the sealing, the following points had to be fulfilled:

- A drying step (at 70 ºC, 5 min) was performed between the paste deposition and the assembly
- A 200 g weight is placed on the stacked parts upon thermal treatment
- Dispensed paste thickness was about 33% higher than the interconnect step (150 μm-deep), to compensate for the volumetric shrinkage of the sealing upon firing.

The so-obtained sealing demonstrated great hermetic properties up to 600 ºC, when reaching the softening point of the glass would cause leakages across the sealing. Nevertheless, once the temperature was lowered below 600 ºC, the reference atmosphere was re-established to its previous value thanks to the metal/metal-oxide mixture placed in the reference chamber. Further characterization of the sealing by X-ray inspection can be found in the Annex.

5.4 Sensor characterization and performance tests

In this section, the characterization of encapsulated miniaturized sensors is presented, starting from the current collection to the symmetric sensing ceramic membrane and eventually, to the performances of the integrated device. To this end, EIS characterization of the symmetric sensing membrane and OCV tracking upon changing the oxygen partial pressure by galvanostatic measurements were performed to assess the sensor time-response and reproducibility.

5.4.1 Experimental setup

The experimental setup is shown in Figure 5.14, including an optical image of the silicon-based micro-sensor joint with a HOYA glass (1x1 cm^2) through the glass-ceramic sealing placed around the sensing membrane.

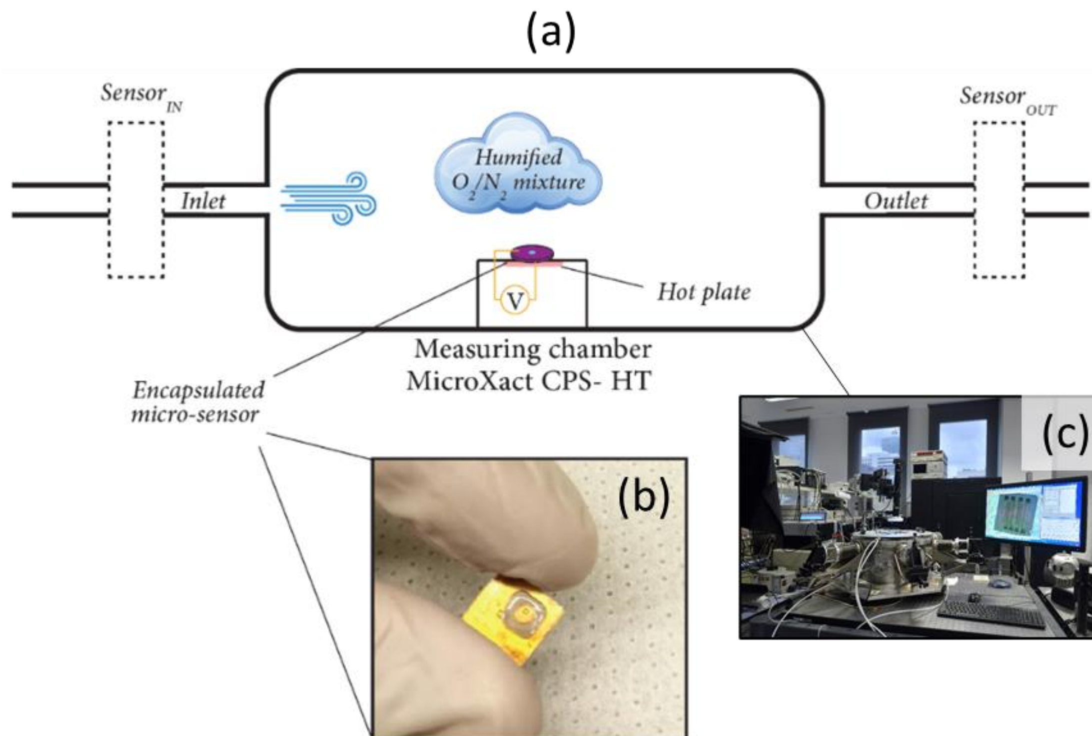

Figure 5.14. (a) Experimental setup for the sensor performance measurements, (b) optical image of the encapsulated device and (c) optical image of the MicroXact CPS-HT chamber

The miniaturized electrochemical oxygen sensor was placed onto a hot-plate inside a MicroXact CPS -HT chamber and electrical contact was established between the conducting tips and the thin-film metallic current collectors fabricated on top of the device. Nevertheless, the formation of silicon dioxide at the interface between the doped-Si contact and the gold collecting layer prevented any signal to be collected. For this reason, further optimization of the microfabrication flow is necessary to ensure the absence of dielectric layer on top of the electrical contacts. Indeed, the same problem was observed in the interconnect devices presented in the Annex of this thesis and solved by performing the metallization right after treatment in HF-based solution, quickly moving the wafer from the etching bath to the evaporator. The sensor hereby presented was therefore tested by collecting the current from the reference electrode with a gold wire.

Two SGM5EL elektrolysis devices from Zirox GmbH (commercial oxygen sensor) were placed at the inlet and outlet of the chamber to control the exact oxygen partial pressure at the inlet and to measure the signal time offset at the outlet due to the time needed to reach equilibrium inside the chamber.

5.4.2 Electrochemical characterization

The Area Specific Resistance (ASR) of the symmetric sensing membrane with thin dense electrodes was characterized by impedance spectroscopy and tested at temperatures below 550 °C, temperature at which the gas-tightness of the glass frit was found stable. The Nyquist and Arrhenius plots recorded at different temperatures (300-550°C) are included in Figure 5.15.

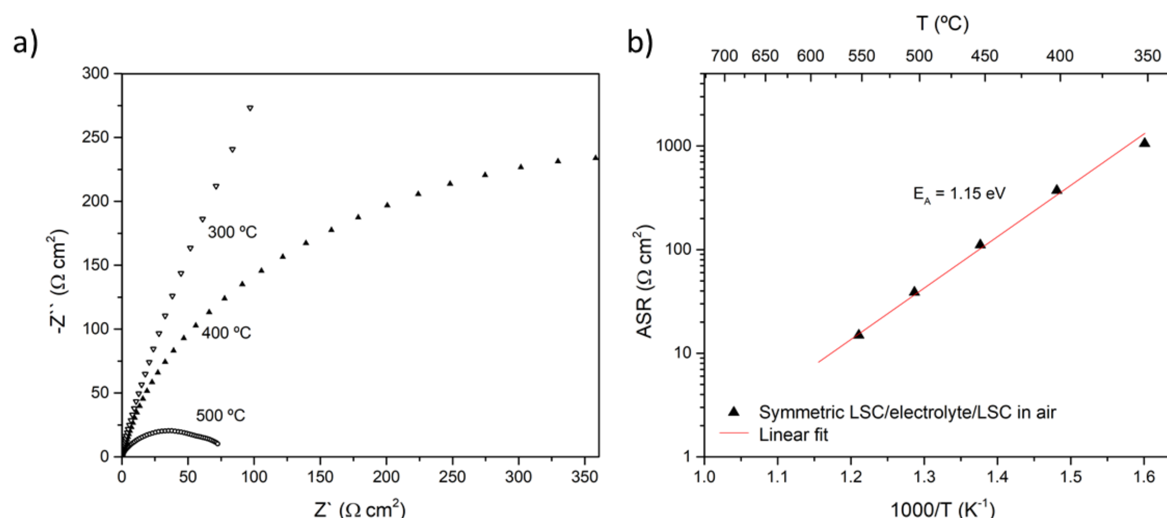

Figure 5.15. EIS characterization of the cross-plane polarization resistance of the LSC/YSZ/OVSZ/LSC sensing unit performed at different temperatures. (a) Nyquist plot and (b) Arrhenius plot are shown.

First of all, consistent results with those previously shown in Chapter 4.4.2 for YSZ single crystals with symmetric LSC electrodes were observed. The ASR of this working electrode is about 14 Ω cm^2 at 550 °C, which is too high for applications in power generation devices operating at such temperature [20]. Nevertheless, the experiments performed hereafter aim at presenting a proof-of-concept for the application of the electrolytic bilayer as well as for the utilization of MIEC ceramic electrodes for gas sensing purposes, which is an application requiring stable and reproducible voltage signals but a high output power density (needed in power generation applications).

In the following, the potentiometric oxygen micro-sensor presented above was characterized by measuring variations in OCV across the sensing membrane when the oxygen content in the measuring chamber was varied. Here, this response was qualitatively compared to the commercial oxygen sensor based on bulk YSZ and placed at the chamber outlet (SGM5EL, ZIROX). It is also important to mention here that a previous calibration of the experimental setup showed a significant delay of the time response of the commercial sensor due to the time needed to fill the measuring chamber, making the quantification of measurements in such setup non-straightforward.

Because of the use of LSC-based electrodes with limited catalytic activity at intermediate temperatures, the surface exchange kinetics of the sensors was strongly influenced by the temperature. Indeed, almost no voltage signal variation was measured at temperature below 400 °C while a slow response was instead observed in the range between 400 and 500 °C. The measurement presented in Figure 5.16 corresponds the temperature at which the sensor response was matching with the commercial sensor response, i.e., around 518 °C. Here, the electromotive

force (E.M.F.) was measured upon variations of the oxygen partial pressure and compared to the input and output signals from the commercial sensors (Figure 5.16-b).

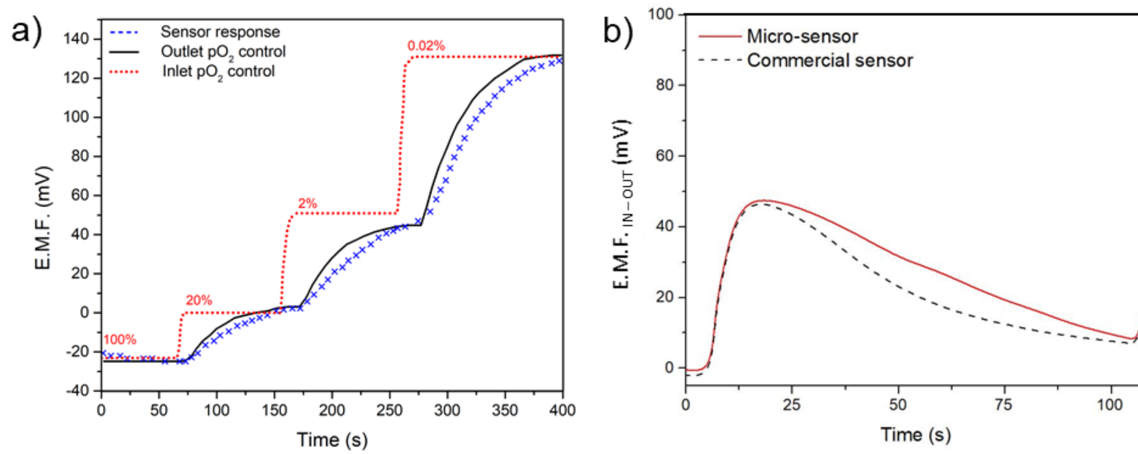

Figure 5.16. (a) Galvanostatic measurement of the potentiometric oxygen micro-sensor at different pO_2 steps between 100% and 0.02%, and (b) differential curve with respect to the inlet sensor response

From these measurements, it can be noticed that the first response of the micro-sensor matches perfectly the one from the commercial sensor placed at the outlet, thanks to the high flow of gases fed to the chamber. Nevertheless, a small difference can be observed regarding the time response, i.e., the time at which the 95% of the final value was reached, that in the case of the micro-sensor was an 6% slower than for the commercial bulk sensor. This represents an excellent performance comparable to the one provided by commercial sensors (based on bulky ceramic YSZ probes with Pt electrodes) operating at much higher temperature (700-800°C) and with much longer warming-up times (15-30 minutes). Nevertheless, the use of more performing MIEC air electrodes will be needed to implement such technology in commercial applications to achieve faster time-response.

Finally, it was possible to extrapolate a calibration curve for the miniaturized oxygen sensor, included in Figure 5.17. According to this measurement, a E.M.F. value close to zero was obtained from an O_2-N_2 mixture of 1:4, suggesting that the same atmosphere present during the sealing joint profile was also obtained inside the reference chamber. Therefore, it was possible to calculate the expected voltage response at different temperatures from the following Niquist equation:

$$\Delta E = \frac{RT}{4F} ln \frac{P^0_{O2,ref}}{P^0_{O2,meas}}$$

The calibration curve presented below shows a good match between the experimental data and theoretical calculation in the range between 0.01 and 100% oxygen. A sensitivity of about 0.001% was observed in this range, where a variation in the order of about 100 ppm was detected once the measuring chamber reached the equilibrium.

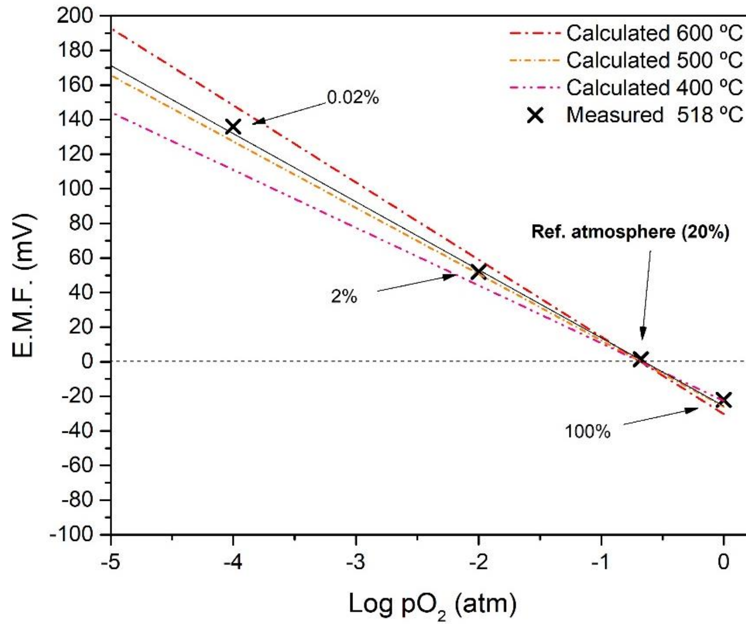

Figure 5.17. Calibration curve of the sensor voltage response at different oxygen partial pressure, including of the calculated theoretical values at different temperatures

Furthermore, the dynamic response of the sensor was tested and reported in Figure 5.18, where the atmosphere was alternatively switched from 20% to 2% oxygen content. Here, one can observe that the sensor is able to provide a consistent and stable E.M.F. response with an experimental error of 4%, although accounting for non-negligible temperature fluctuations around the sensing unit. Indeed, the gas flows fed to the chamber were the main responsible for a temperature fluctuation on the sensor surface up to 6% of the setpoint temperature (T=485-518 ºC). For this reason, at times the E.M.F. response was lower than the theoretical value.

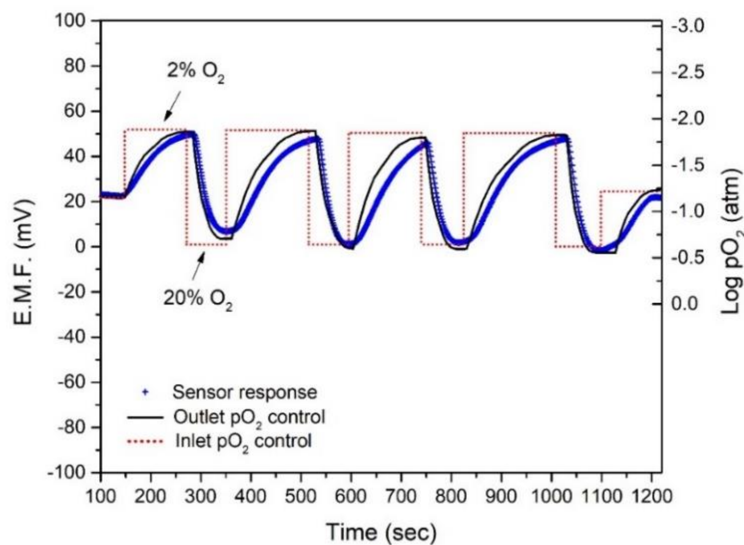

Figure 5.18. Sensor dynamic response upon switching the external atmosphere from 20% to 2% O_2 content. The response of two reference commercial sensors and the miniaturized device are included for comparison. The measurement was performed at 518 ºC.

Finally, the gas mixture in the measuring chamber was switched to a fully reducing atmosphere, comprising of 5%-H_2 in Argon, and the time response measured accordingly and shown in

Figure 5.19. Even if the sensor had been measured at a relatively low temperature, a sensor response of about 38 mV/s was observed until reaching 95% of the final E.M.F., which was 0.93 V.

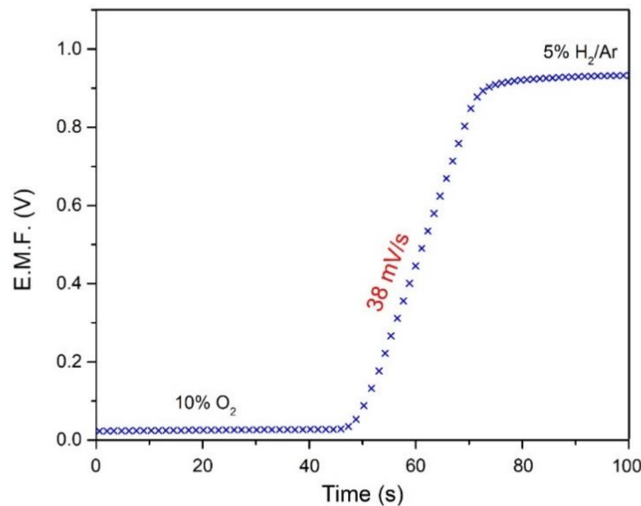

Figure 5.19. Sensor's voltage response after exposure to a reducing atmosphere at 518 ºC

The measurements presented hereby showed the great potential of the proposed technology for commercialization and adoption in operating environments where the need of low energy consumption and harsh temperatures are characteristic. Nevertheless, more tests must be performed specially targeting the adequate characterization of the time response (regarding the test chamber intrinsic delay) and selectivity of the electrodes in relevant environment (including cross-sensitivity to relevant gases like water vapor).

5.5 Conclusions

This chapter provides a validation of the microfabrication concepts studied in this thesis. Indeed, the combination of ceramic thin film deposition techniques and mainstream clean-room processes led to the successful miniaturization of a potentiometric electrochemical oxygen sensor with internal reference atmosphere that can be operated at intermediate and high temperatures.

A reproducible fabrication process for silicon-based sensing platforms was achieved at large scale onto 4-inches silicon wafers, highlighting its potential for mass-scale production. The platform comprising of a suspended YSZ-OVSZ ceramic membrane with LSC symmetrical electrodes for oxygen sensing was encapsulated with a micro-machined HOYA glass and glass-ceramic sealing that can operate up to 600 ºC, while assuring the thermal expansion compatibility of the materials.

This fully integrated miniaturized oxygen sensor was therefore tested at a temperature of 518 ºC and oxygen partial pressure in the range 0.01-100%, showing stable and reproducible response, and comparable time-response with commercial bulk technology (without major drawbacks of conventional sensors such as use of noble metal catalysts or long warming-up times). The sensor's voltage signal showed good agreement with the theoretical values calculated from the Nernst equation, i.e. a linear dependence with the logarithm of the oxygen partial

pressure. Whereas further characterization is needed to assess the absolute time-response and selectivity of the sensing unit towards oxygen, a MIEC-based air electrode with higher surface exchange kinetics at intermediate temperatures is needed to take full advantage of the miniaturization, thus leading to very fast time-response upon small changes in oxygen partial pressure.

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CHAPTER 6

STANDALONE MICRO-REFORMER FOR ON-DEMAND HYDROGEN PRODUCTION FROM DIMETHYL ETHER

Standalone micro-reformer unit for on-demand hydrogen production from dimethyl ether

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6.1 Introduction

Since the beginning of this century, technological advancements in microelectronics made it possible to reduce the size of portable devices while achieving greater quality and efficiency. However, the power consumption rises proportionately to the new functionalities these devices are able to operate [1]. The last generation of portable devices mostly relies on lithium-ion batteries; despite the limited energy density they provide. In order to fulfill the energy gap between power consumption and the specific energy provided by portable power generators, innovative approaches to generate electric power from fuels have been explored [2–8].

Entering a new era of sustainable energy generation and consumption based on renewable energies, hydrogen is expected to tackle an important role as green energy carrier with the greatest gravimetric energy density and low contamination [9]. Nevertheless, it suffers from many drawbacks related with safety and storage when it comes to portable applications. The use of catalytic reformers for hydrogen and synthesis gas (syngas) production is an established alternative to direct hydrogen storage, and especially the micro-scale catalytic reactors have been pointed out as a solution for the integration of fuel-based micro-power sources in portable devices, as previously described in chapter 1.3.2.

While a multitude of micro-reactors fabrication techniques have been reviewed for a wide range of construction materials [10], combination with advances in integrated circuit (IC) and micro-electromechanical systems (MEMS) arouse great interest in the scientific community, enabling the fabrication of high-aspect-ratio structures with high accuracy and allowing for the integration of functional features such as temperature sensors and micro-heaters onto the same platform [11]. These techniques (photolithography, wet and dry etching, chemical and physical vapor depositions) can be effectively used to create micro-channels on polymer, glass or silicon substrates. Indeed, silicon is an ideal material for the fabrication of micro-reactors because of its low cost, large operating temperature range and chemical inertness.

In this chapter, we demonstrate the fabrication of a MEMS-based suspended micro reforming unit and its catalytic performance for conversion of dimethyl ether (DME) to syngas, especially designed for hybrid start-up of the micro-SOFC stack power generator described elsewhere [12]. The advantages of choosing DME as alternative fuel were described in Chapter 1.1.2. Here, the coupling of electric heating from the embedded micro-heater with an exothermic reaction is tested for the start-up of DME reforming using a 3D printed ceramic packaging, simulating real-life operating conditions.

Finally, a fully scalable catalyst fabrication route based on atomic layer deposition (ALD) has been implemented, tackling one of the most commonly reported issues for coated-wall micro-reactors, i.e., the uniform surface coating and dispersion of metal nanoparticles on high-aspect-ratio structures [13]. This technique has received increasing interest in recent years for its self-limiting reaction character, leading to layer-by-layer growth of conformal coatings and outstanding precision on thickness control. This technique and its numerous applications for energy devices and catalysis have been extensively reviewed [14–17], remarking its great potential for the fabrication of homogeneous coatings or well-dispersed particles onto high-aspect-ratio structures or highly porous materials. Conversely, the most typical coating

technique, i.e., dip coating (or washcoating) from a liquid suspension or sol mixture, suffers from non-uniform surface tension of the micro-reactor's walls and the resulting coating tends to collect at the corners of the reactor [13]. This study reports, for the first time in our knowledge, the effective coating of MEMS-embedded micro-channels by a combination of clean-room-compatible techniques (ALD and RTP) to fabricate a catalytic fuel micro-reformer, and it aims at showing the potential of such technique for large-scale industrial adoption. Here, a heterogeneous catalyst based on Pt nanoparticles dispersed onto γ-Al_2O_3 support was chosen as a model catalyst suitable for DME reforming [18–22]. In fact, Pt has been shown to limit coking, so that more active surface area is available for reaction [23] while γ-Al_2O_3 is a well-known support for its high surface area and acidic properties [24].

6.2 Micro-reformer unit

In the following, the design and microfabrication of a silicon-based micro-reformer unit based on vertically aligned micro-channels is presented. Moreover, the functionalization of the superficial area inside the micro-channels was achieved by ALD and RTP and properly characterized prior testing of the DME reforming reactions.

6.2.1 Micro-reactor design

The micro-reformer unit presented in this work is designed as a monolithic reactor with an array of vertically aligned micro-channels etched through a silicon substrate, ensuring compatibility with the other elements of the micro-SOFC power generator. More than 8000 micro-channels, 50 μm in diameter and 500 μm in length, are thus fabricated into a 1x1cm^2 silicon platform, accounting for an overall surface area of about 120 cm^2/cm^3. This design takes inspiration from Llorca *et al.* [25,26] silicon monolith micro-reactor, comprising a million channels of a diameter size that was scaled from mm-scale to only few microns, achieving three orders of magnitude enhancement in specific volumetric production of hydrogen [27].

This reactor comprises a serpentine-like heater defined on top of the device for efficient start-up and the active area is thermally insulated by means of a Si_3N_4 membrane, preventing lateral heat losses that would occur through the bulk silicon substrate. More details about the design and a FEM analysis are reported elsewhere [28], while a schematic view of the reactor is included in Figure 6.1.

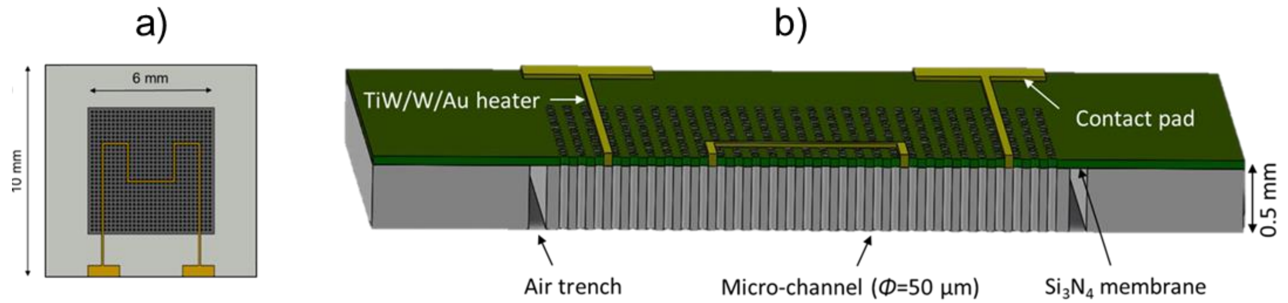

Figure 6.1. Description of the micro-reactor design. a) Schematic top view of the micro-reactor; d) schematic cross-section of the device with the description of its main components

The low thermal mass of the device allows to reach very fast reaction start-up times, making it possible to feed enough hydrogen-syngas mixture to the micro-power generator within a very short time and limiting the power consumption needed to reach steady operation of the device (that in real condition would be provided by a supercapacitor or similar device).

6.2.2 Microfabrication

For the fabrication of the device, single crystal (100)-oriented p-type silicon wafers of 4 inches in diameter and 500 µm in thickness are first passivated on both sides with a dielectric bilayer consisting of 100 nm-thick thermally grown SiO_2 and 300 nm of plasma-enhanced chemical vapor deposition (PECVD) Si_3N_4 deposited on top. Photolithography is used throughout the whole fabrication to transfer patterns onto the substrate. Three layers of 30 nm TiW, 250 nm W and 20 nm Au are sputtered on the top side of the wafer and subsequently the micro-heater is defined by lift-off of the patterned photoresist. A parallel process was performed before this step, in which the metallic layers are evaporated on the whole substrate and photolithography performed on top of it, eventually defining the serpentine heater by metal etching. Nevertheless, this process may result in an uncomplete etching of the metal, thus the lift-off procedure was preferred.

A 2.5 µm-thick SiO_2 layer is deposited by PECVD on both sides of the wafer and etched by Deep Reactive Ion Etching (DRIE) on the back side of the wafer creating a mask for the micro-channels and the trench. About 80 µm of silicon are etched from the top side, and the micro-channels and air trench are eventually completely etched by repeating the same process on the back side. Finally, the PECVD SiO_2 left on the surface of the microreactor is removed by dipping the wafers in HF 1:10 aqueous solution. A schematic view of the microfabrication flow is presented in Figure 6.2.

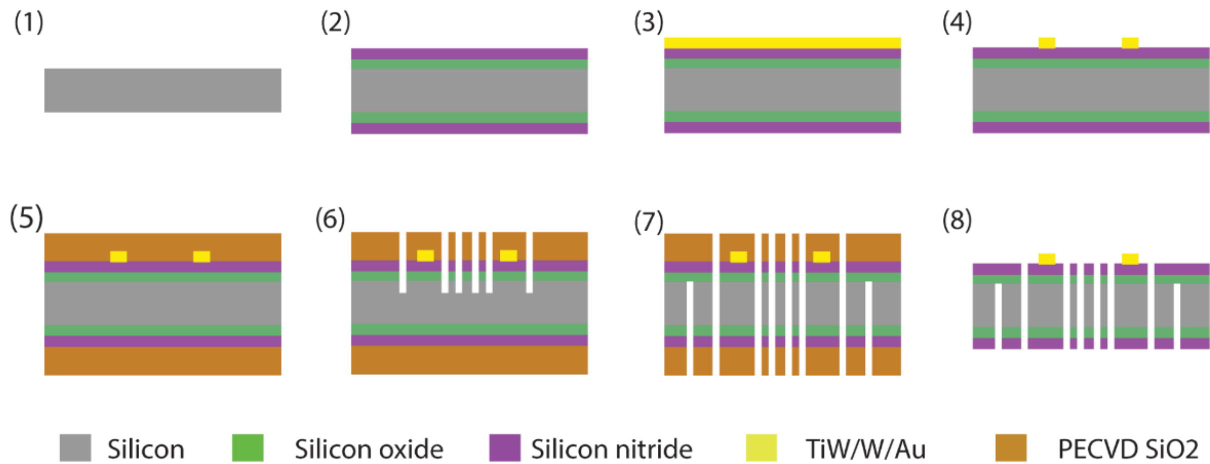

Figure 6.2. Micro-reactor fabrication process flow. (1) Double-side polished Si wafer, (100)-oriented and 500 µm-thick; (2) 100 nm thermal SiO_2 growth and 300 nm Si_3N_4 deposited by PECVD on both sides of the wafer; (3) photolithography to define the heater pattern and metal sputtering on top of the photoresist; (4) lift-off; (5) deposition of 2.5 um of SiO_2 by PECVD on both sides; (6) photolithography and etching of the dielectric mask by RIE to define the micro-channels on the top side and 80 µm etching of bulk silicon; (7) photolithography and RIE to remove the dielectric layers on the top side and open the micro-channels and etch the air-trench; (8) HF bath (1:10 solution) to open the heater contacts and remove the PECVD SiO_2

All the 4-inches processed wafers comprise more than 50 devices (Figure 6.3-a) successfully fabricated thanks to an optimal thermalization of the specimen during the DRIE process. Moreover, multiple wafers were processed simultaneously, highlighting the potential of micro-fabrication approach to industrial large-scale production.

The 1x1x0.05 cm3 device (Figure 6.3-b) consisted of about 8000 micro-channels (50 µm diameter, Figure 6.3-c) corresponding to an active area within the channels greater than 6 cm^2. The 50 µm-wide trench was defined on the back side, ensuring thermal insulation of the reactor frame from the catalytically active region. The surface of the heater was inspected after the HF treatment and it was found free of SiO_2, showing a nominal resistance of $R = 80 \pm 2\ \Omega$, while no macro-defects were detected on the metallic layers. Indeed, the presence of silica in the gas mixture can be a source of contamination for fuel cells electrodes containing nickel, although nowadays some mitigation strategies include the fabrication of smart catalysts that can be regenerated through redox cycles.

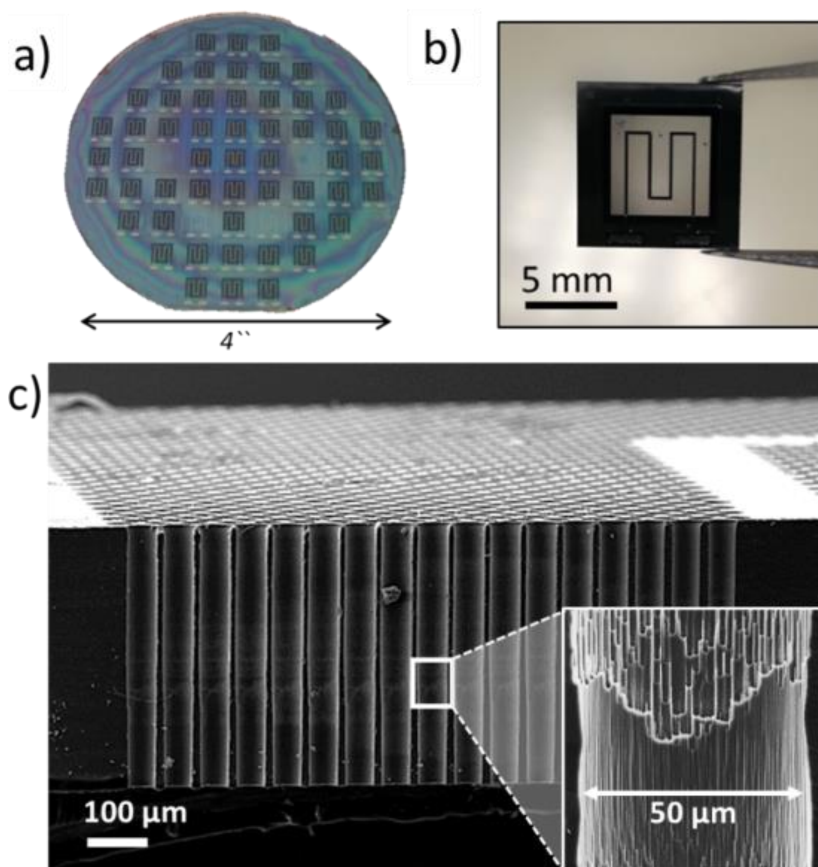

Figure 6.3. Micro-fabrication results. a) optical image of the Si wafer after processing, comprising more than 50 devices; b) optical image of the fabricated micro-reactor showing the transparent active region where the opened micro-channels are located; c) Cross-section SEM image of the device showing the through-silicon channels and the heater path, and higher magnification of a single channel (inlet)

Catalyst deposition was performed by atomic layer deposition (ALD) with a PicoSun R-200 system as previously described in section 2.2.2.2. Crystallization of the as-deposited amorphous Al_2O_3 layer was obtained by rapid thermal processing (RTP). This quick and surface annealing process based on IR lamps (opposite to furnace-like treatments employing hot boxes) has indeed the advantage of triggering crystallization in thin films without damaging a MEMS device itself or the features it includes, such as the micro-heater described in this work.

Nevertheless, carrying on such strategy presumes solving some issues related to the full coverage of the substrate's surface with non-selective chemical deposition technique. Figure 6.4 shows a SEM image of the micro-heater, taken after Al_2O_3 deposition and RTP. It is noticeable the exfoliation of the alumina layer due to residual stresses and subsequent dewetting of the gold layer, eventually resulting in an array of coarsened particles.

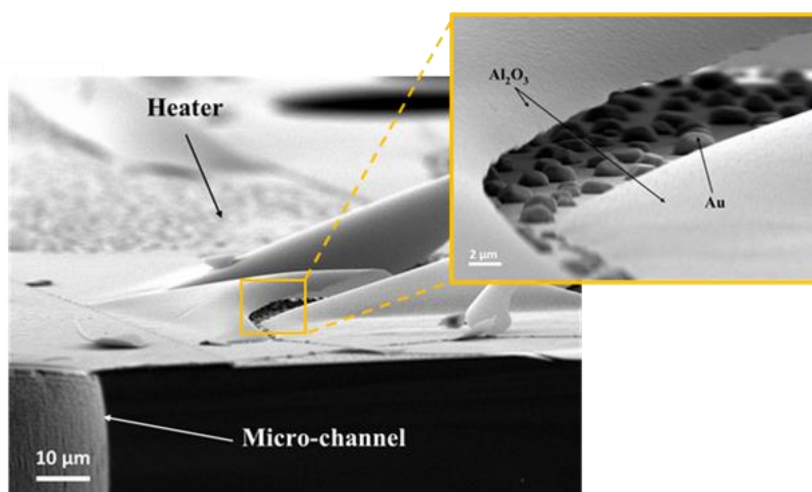

Figure 6.4. SEM imaging of a damaged micro-reactor and the alumina coating on top of the heater after RTP treatment and a detail of its delamination and gold coarsening below (inlet)

As a mitigation strategy, the masking of the micro-heater during ALD depositions was necessary to avoid stresses caused by the deposition of a uniform layer onto the substrate, and it was achieved by placing the top side of the wafer, the one with the heater, in direct contact with a dummy silicon wafer and putting a weight on top of it, forcing the two surfaces closer to each other. The shading effect was sufficient to avoid full coverage of the heater and to avoid the abovementioned stress-related issues.

6.2.3 Catalyst characterization

The 100 nm-thick Al_2O_3 active support layer that coated homogeneously all the micro-channels´ walls (Figure 6.5) was found to be amorphous after deposition, as expected. Therefore, RTP was performed at different temperature set points and the resulting optical and crystallographic properties examined by ellipsometry and GIXRD (Figure 6.6), respectively. Here, part of the pattern (2θ = 50-60º) was not included due to the presence of Si (113) substrate reflection.

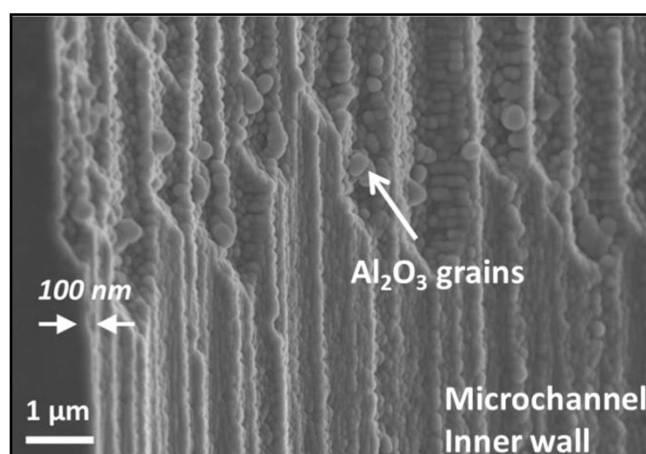

Figure 6.5. SEM image of a micro-channel's wall after Al_2O_3 deposition by ALD

All the samples presented diffraction peaks related to either gamma- (JCPDS 00-020-0425) or theta- (JCPDS 00-035-0121) alumina phases. Increasing the RTP temperature set point boosts the amount of crystalline phase in the sample, as it can be observed from the evolution of the peaks around 32°, where increasing intensity of the reflection theta (004) with respect to the gamma (220). Also, Figure 6.6-b reports a shift of the most intense peak around 2θ = 67°, corresponding to the (215) theta plane and (440) gamma plane, supporting the evolving trend towards the θ- Al_2O_3 phase.

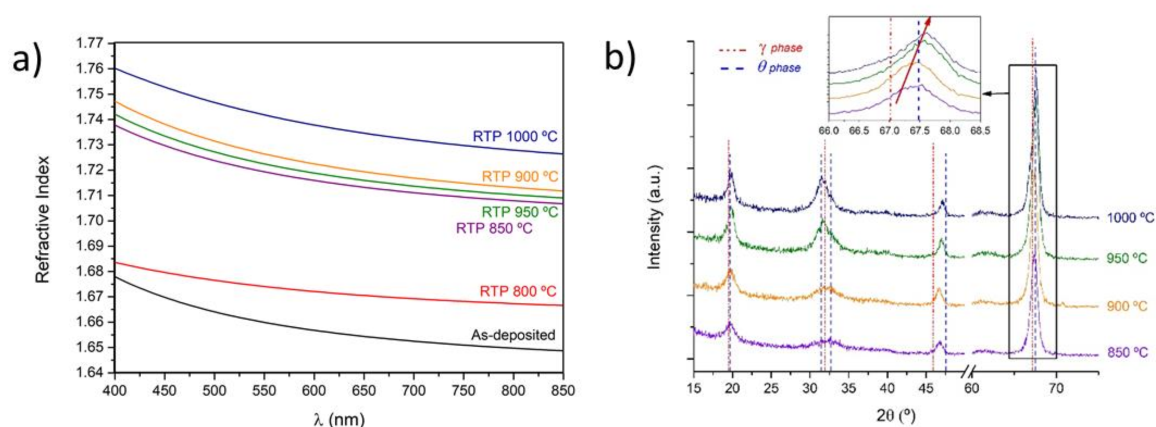

Figure 6.6. Optical and structural properties of Al2O3 upon RTP treatment at different temperature set-points. (a) Refractive index extrapolated from spectroscopic ellipsometry and (b) GIXRD patterns

In this case, limiting the amount of θ-Al_2O_3 phase is beneficial because of its basicity, making it catalytically inactive. Conversely, γ- Al_2O_3 is a common catalytic support for its acidity that is known to trigger dehydration [24,29]. Hence, a RTP temperature set point T_{RTP} = 850 °C was chosen for the fabrication of the γ- phase-rich catalytic alumina support.

A uniform coverage of the micro-channels walls with platinum nanoparticles was successfully achieved *via* 80 ALD cycles. From the SEM characterization and especially analyzing the images taken with a backscattered electrons detector (Figure 6.7-a), one can notice that a uniform coverage along the micro-channels walls was obtained. The presence of platinum was also confirmed by XRD (Figure 6.7-b). A broad peak around 39.7° was observed, either corresponding to the (111) reflection of Pt metal (JCPDS 00-001-1190) or (020) and (200) reflection of PtO_2 (JCPDS 00-043-1045).

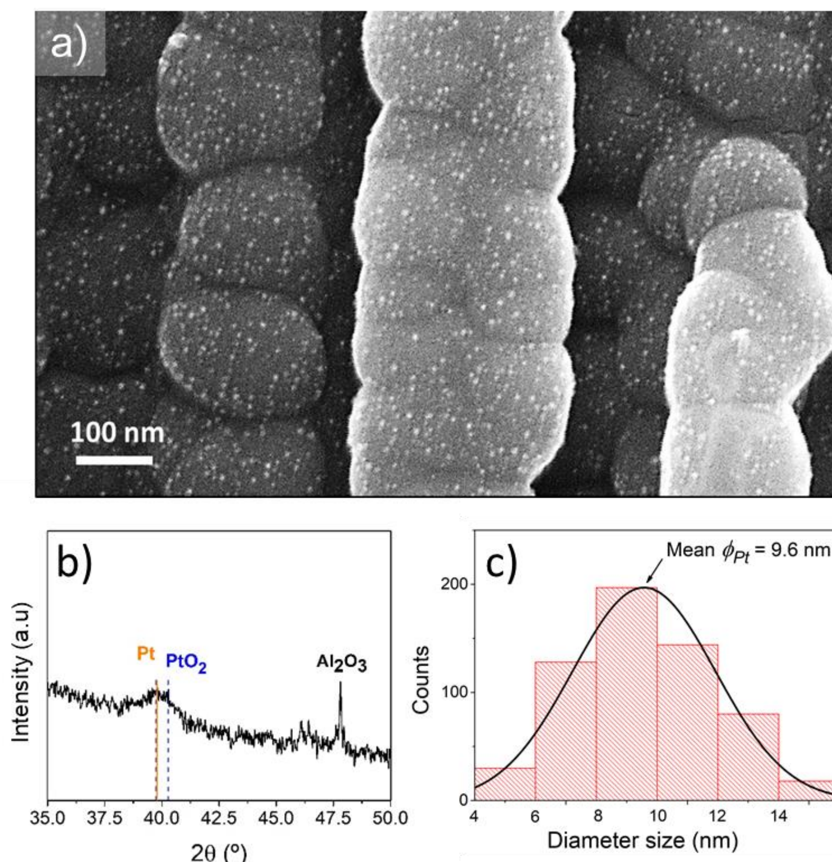

Figure 6.7. Structural and morphological characterization of the metal catalyst. a) High-magnification back-scattered electrons SEM image of the fabricated catalyst (micro-channel cross section) comprising Pt nanoparticle dispersion on Al2O3 layer; b) XRD pattern of the catalyst deposited on Si(100) recorded with a θ offset of 1°; c) Histogram and normal distribution of Pt nanoparticles in the channels

A reducing treatment in 5%-H_2/Ar atmosphere at 300 °C was therefore applied prior to DME reforming experiments to avoid any platinum dioxide in the micro-reactor. At this temperature, the syngas produced has a reducing character and would activate the remaining catalyst even without this pre-reduction step, although resulting in longer reaction start-up times in practical applications.

The particle size distribution is reported in Figure 6.7-c, where particles with diameter size ranging from 5 to 14 nm were observed. The average diameter size estimated is 9.6 nm. An estimation of the platinum surface coverage can be made accounting for the over 300 particles μm^{-2} observed along the micro-channels that is around 3% of the exposed surface. Correspondingly, the metal loading can be estimated assuming hemispherical shape of the particles and it was found to be around 1%wt of the alumina support layer.

For an increasing number of ALD cycles, a broader particle distribution was indeed expected as shown before by Rontu *et al.*[30]. Surface chemical modification is thereby pointed out as an effective route to obtain more hydroxyl-terminate surface, thus reducing the number of ALD cycles and obtaining a narrower distribution and smaller particles, usually more active in catalysis.

Finally, the catalyst morphology and performance are maintained throughout the whole experiment. i.e., 3 hours at 600 °C, as shown in Figure 6.8.

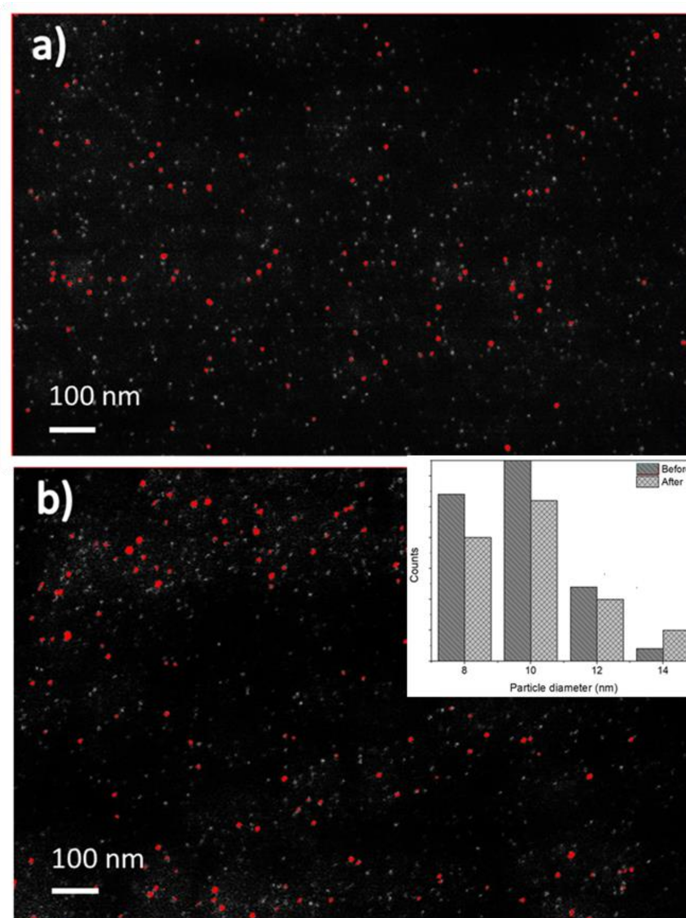

Figure 6.8. High-contrast SEM images of the catalyst coating (a) before and (b) after operation (3 hours at 600 °C). The analysis was performed on the biggest particles (red color for visualization) found on planar surfaces and highlighted by Z contrast at high acceleration voltage, to observe any possible particle coarsening upon operation. The particle diameter distribution is reported in the inlet.

While this result suggests a strong adhesion of the nucleated platinum by chemical interaction with alumina surface, as previously observed for other catalytic systems fabricated by ALD [31], further tests on long-term operation of the catalyst and its thermal cycling behavior are on-going.

6.3 Micro-reactor performances on DME conversion

Two different catalytic reactions were carried out in order to estimate the viability of this technology for on-demand hydrogen production from DME, namely steam reforming (SR) and partial oxidation (POX). The former is the most common reaction employed for industrial purposes due to its high H_2 output and it occurs according to the following consecutive reactions:

$$CH_3OCH_3 + H_2O \rightleftarrows 2CH_3OH \qquad (1)$$

$$2CH_3OH+2H_2O \rightleftarrows 2CO_2+6H_2 \quad (2)$$

With overall ΔH^o = 135 kJ mol^{-1} (endothermic).

Nevertheless, for a portable solid oxide fuel cell, POX is more favorable from an energy balance perspective for its exothermic character at the expenses of the H_2 yield and it is described by the following reaction:

$$CH_3OCH_3+0.5O_2 \rightleftarrows 2CO + 3H_2 \qquad \Delta H^o = -37 \text{ kJ mol}^{-1} \text{ (exothermic)} \quad (3)$$

For the evaluation of the temperature effects on the catalytic performance, a customized fixed bed reactor made of stainless steel was employed and placed inside a furnace at a temperature range between 400 °C and 650 °C (ramp rate of 3 °C min^{-1}). DME flow was set at 2 mL min^{-1} and mixed with steam (steam to carbon ratio S/C=1.5) or air (O_2/DME=0.5) at the reactor inlet together with N_2 inert gas, accounting for a total volumetric flow of 15 mL min^{-1}.

6.3.1 Temperature effects

The effect of temperature on DME conversion and product selectivity was investigated by placing the micro-reformer unit inside a customized fixed bed reactor and into a furnace.

For the steam reforming reaction, a temperature range between 500 °C and 650 °C was selected for the experiment. The main products of reaction are H_2, CH_4, CH_3OH, CO and CO_2. As shown in Figure 6.9-a, the DME conversion is below 10% at 500 °C, while further increasing up to 74% at 650 °C. Hydrogen selectivity close to 60% is observed above 600 °C. Selectivity of the products is only reported for temperatures above 575 °C where the error in the calculation was found acceptable.

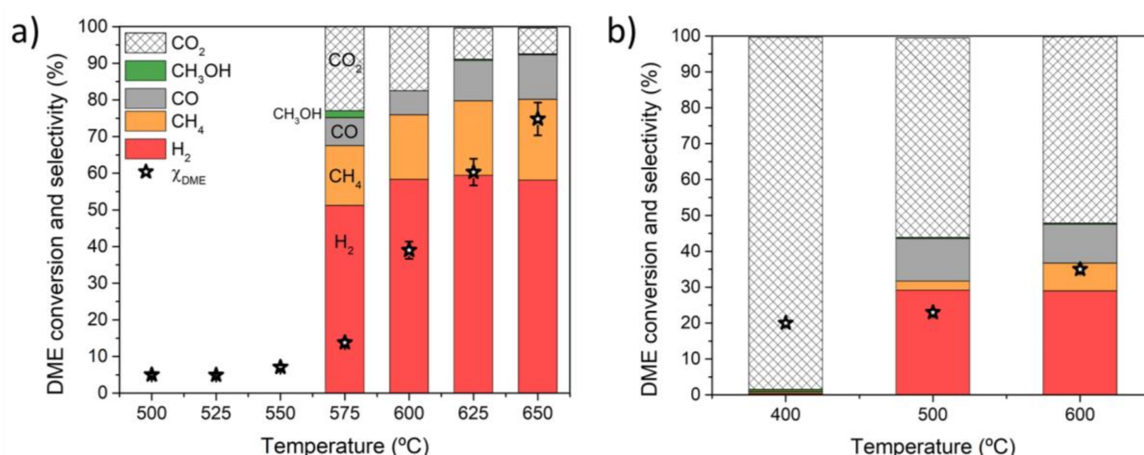

Figure 6.9. Product selectivity (column bars) and DME conversion (black stars) as a function of temperature for a) SR reaction (S/C=1.5) and b) POX reaction (O2/DME=0.5). The same legend is used for both graphs.

As expected, the DME conversion is quite low at temperature lower than 575 °C. Methanol is observed at the lower temperature range highlighting the role of the acidic Al_2O_3 active support to the hydration of DME (equation 1). At higher temperatures, CH_3OH disappears suggesting

a complete methanol steam reforming (equation 2) is occurring. Here, selectivity to H_2 reaches values as high as 60%. However, as the temperature increases the amount of CH_4 and CO rises because of both the reverse water-gas shift reaction (r-WGS, eq. 4) and DME decomposition (eq. 5) are favored at higher temperature[32,33]:

$$CO_2+H_2 \rightleftarrows CO+H_2O \quad (4)$$

$$CH_3OCH_3 \rightleftarrows CH_4+CO+H_2 \quad (5)$$

This trend leading to CH_4 formation was already reported for Pt-loaded Al_2O_3 catalysts, where the addition of Pd to the catalytic system helped inhibiting methane formation[19].

The effect of temperature on DME POX was studied within a lower temperature range (i.e. 400-600 °C), as it is expected to take place at lower temperature than steam reforming. Hydrogen selectivity of about 30% and DME conversion of 36% were obtained (Figure 6.9-b).

At 400 °C no hydrogen was detected while carbon dioxide was present due to a low-temperature complete oxidation of the fuel (eq. 6).

$$CH_3OCH_3+3O_2 \rightleftarrows 2CO_2+3H_2O \quad (6)$$

The main products of DME POX reaction, carbon monoxide and hydrogen, were found at temperature greater than 460 °C. An increasing concentration of methane is observed at higher temperature, which is associated to DME decomposition (eq. 5), since CO methanation is not favored at high temperature due to the chemical equilibrium. The H_2 yield in the transient regime during start-up of the device was further characterized and will be presented in the following section for the standalone device.

The hydrogen-to-carbon monoxide ratio was found to be around 2.5, higher than the stoichiometric value of 1.5. This result can be attributed to the water-gas shift reaction where CO reacts with the steam produced by DME full oxidation.

When comparing the amount of hydrogen produced by these two processes at 600 °C in Figure 6.10, it is noticeable that steam reforming leads to the generation of twice the amount of hydrogen per mole of reformed gas with respect to the POX reaction. Overall, the syngas production from DME SR doubles its POX counterpart but for an endothermic reaction such as SR a higher amount of energy must be provided to the system. For this reason, the next section focuses on the POX reaction only.

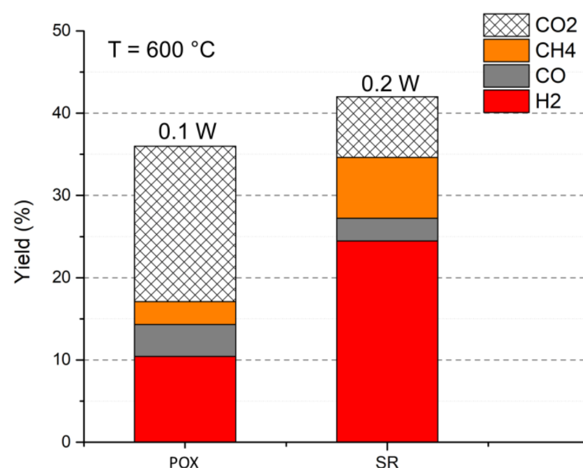

Figure 6.10. Comparison between yield of products for POX and SR reactions at T=600 ºC and resulting power obtained by an ideal fuel cell power generator (eq. 7)

The results shown above demonstrate the potential for integration of such micro-reforming unit in portable power generator, delivering approximately 0.1 and 0.2 W from DME POX and SR respectively, calculated from equation 7, pointing out the present technology as a promising route for a fully scalable production of on-demand fuel micro-reformers.

$$W = \Delta G^{\circ}_{H_2} \cdot \dot{n}_{H_2} + \Delta G^{\circ}_{CH4} \cdot \dot{n}_{CH_4} + \Delta G^{\circ}_{CO} \cdot \dot{n}_{CO} + \Delta G^{\circ}_{CH3OH} \cdot \dot{n}_{CH_3OH} \quad (7)$$

In fact, one must consider that this standalone device has been especially designed for the start-up of a micro-SOFC, while a full device also comprises a bulk reforming unit[12] that would greatly enhance the DME conversion, the syngas productivity as well as the selectivity to hydrogen by implementing the appropriate catalysts. Indeed, the deposition technique employed in this work can be easily applied to the fabrication of different catalytic systems, including for instance Pd, Cu, Zn, Ru, Ni metal catalysts and ZrO_2 or CeO_2 active supports, to mention some. Furthermore, the MEMS fabrication route allows for easy routes to scale-up the number of micro-channels as well as their length (hence the contact time between fuel and catalyst), making it possible to tune the syngas production for specific applications. This can be achieved by either changing the mask used during the RIE process or by stacking of multiple micro-reformer units with wafer bonding techniques (silicon/eutectic bonding or glass frits, for instance).

6.3.2 Standalone operation of the DME POX reactor

The integration of a micro-reformer in a micro-SOFC requires an embedded internal heating element for an efficient start-up of the device. In this case, it is obtained by fabricating a thin-film W/Au serpentine heater on top of the suspended micro-channels platform in the device (see Figure 6.1).

DME POX was chosen as the most suitable reaction for micro-reactors to be included in micro-SOFC portable systems: because of its exothermic character and easier integration (without the need of steam generation on-board) it would enable a hybrid electrical-catalytic start-up.

Therefore, the only measurements presented in this section concern the hybrid start-up of the POX reaction. The detailed setup adopted for measurements in real operating environment is presented in Figure 6.11.

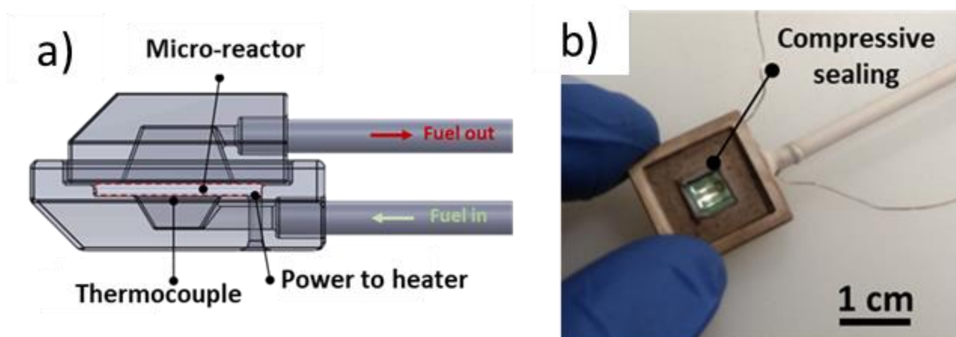

Figure 6.11. (a) schematic view of the 3D printed ceramic holder enabling hybrid reaction start-up; (b) optical image of the ceramic housing and compressive sealing used in the experiment.

Figure 6.12-a shows the temperature evolution of the embedded heater, i.e. the reactor channels, during the start-up (when a constant power is applied and the DME:Air:N2 mixture is fed into the system at a flow of 15 ml min-1). Complementary, Figure 6.12-b presents the hydrogen production rate generated during the same start-up transient regime. As clearly observed in the figures, the hydrogen production reaction starts around 300 °C.

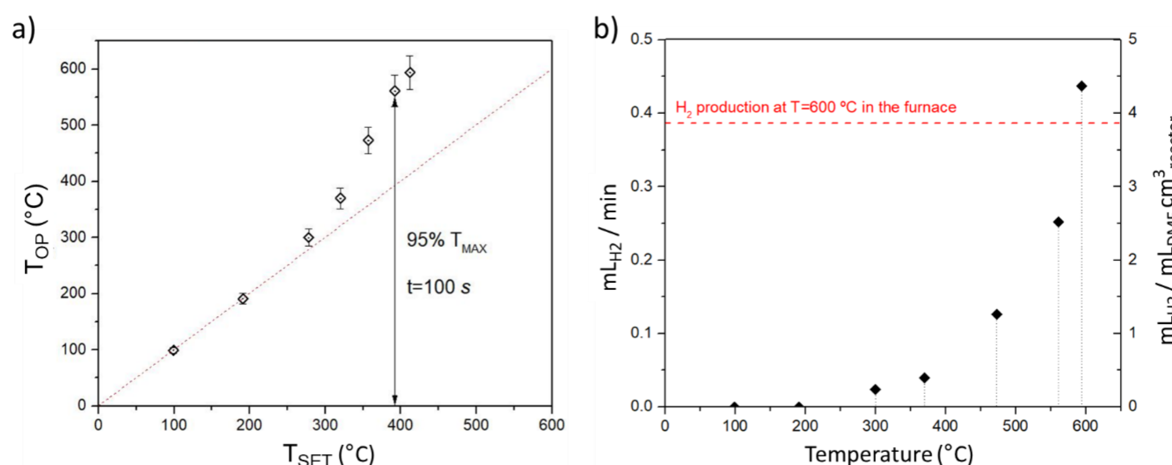

Figure 6.12. (a) Characteristic temperature behavior of the thin-film heater during testing with a total inlet flow rate of 15 mL min-1; (b) hydrogen production rate (left Y-axis) and specific volumetric production of hydrogen (right Y-axis) during start-up. O2/DME ratio was fixed to 0.5.

Once this occurs, the difference between the temperature set point (without gas flowing) and operating temperature becomes evident, ultimately reaching a maximum temperature of 595 °C when the temperature was set at 400 °C. In other words, the system is self-heated by the exothermal reaction when it starts. Beyond this point, the thermally self-sustained mode is enabled. Provided a thermal insulation matching with the specific requirements, an O_2/DME ratio greater than 0.68 should be employed to self-sustain the reaction, while switching off the heater, according to the thermodynamic calculations reported in Table 6.1.

	Reagents		Products	
SPECIE	DME	O_2	CO	H_2
H_F 25	-184	0	-110	0
ΔH_F 600C (kJ/mol)	37,3749	19,5168	18,0348	16,872
H_F 600C (kJ/mol)	-146,6251	19,5168	-91,9652	16,872
Molar coefficient	1	0,68	2	3
Molar mass (g/mol)	46	32	28	2
Cp (KJ/Kg K)		1,07	1,13	14,8
Cp (J / K mol)	65,57			

Table 6.1. Enthalpy of formation and specific heat values used to calculate the enthalpy of reaction at the equilibrium and the minimum O2/DME ratio needed to sustain the exothermic reaction

For the measurement setup developed in this work, the start-up temperature is reached after 100 *s* which is thrice the time reported by the authors for measurements carried out under vacuum [28]. Although the reactor embedded in the final system is expected to behave approaching the values under vacuum, the energy consumption required here for the start-up was still below 500 J, a value considered feasible for a hybrid heating solution based on electrical heating and catalytic oxidation [12]. Moreover, these results show that above 300 ºC the hydrogen production exponentially increases due to the temperature increase, achieving values of hydrogen yield surprisingly higher than those reported in section 6.3.1 (Figure 6.9) at the same temperature and a H_2+CO yield consistent with the previous experiments (about 19% syngas yield, with a H_2-to-CO ratio of about 2.4). Whereas further work is on-going to fully understand this behaviour and the potential effects of local heating, these results suggest that the same side-reactions previously observed are also occurring in these measurements, limiting the reaction efficiency to 65% compared to stoichiometry.

Finally, Figure 6.12-b (right Y-axis) shows great values of specific volumetric production of hydrogen from the volume of the fuel of choice (~ 4.5 $mL_{H2}\ mL^{-1}_{DME}\ cm^{-3}$). This is a crucial parameter for the design of an efficient catalytic conversion micro-reactor, especially when aims portable applications. In this regard, this work reinforces previous reports by the authors where a reduction of the micro-channel diameter size from one millimeter to 2 μm resulted in three orders of magnitude enhancement of the same parameter [27].

Overall, this section proves the possibility to operate a silicon-based micro-reactor for DME conversion with excellent hydrogen production per unit volume by reaching the thermally self-sustained mode using embedded micro-heaters.

6.4 Conclusions

In this chapter, wafer-level fabrication of a suspended Si-based micro-reformer unit for DME-to-syngas conversion is presented. The micro-reactor, fabricated by means of mainstream micro-fabrication processes, comprises an array of vertically aligned micro-channels of 50 μm in diameter for a total active area of about 6 cm^2, a thin-film heater for efficient reaction start-up and a suspended Si_3N_4 membrane for thermal insulation of the active area.

The micro-channels walls were effectively coated with a Pt nanoparticle dispersion (1%wt of the active support, 9.6 nm the average diameter) supported on 100 nm-thick Al_2O_3 layer by means of atomic layer deposition (ALD) and rapid thermal processing (RTP), a combination of clean-room-compatible techniques for the fabrication of complex catalytic systems with precise control on coating thickness and metal loading (1%wt in this work). The system was tested for both DME steam reforming (SR) and partial oxidation (POX) at intermediate temperatures. A 74% DME conversion with hydrogen selectivity around 60% was obtained at 650 °C from DME steam reforming, while results on partial oxidation showed 36% DME conversion and 30% hydrogen selectivity at 600 °C. The heterogeneous catalyst chosen for this proof-of-concept showed relatively high selectivity to CH_4 and CO because of the side reactions involved.

Efficient POX reaction start-up (energy consumption < 500 J) was demonstrated in standalone configuration using a 3D printed ceramic holder simulating real-life thermal packaging. State-of-art specific volumetric hydrogen production rates of 4.5 mL_{H2} mL^{-1}_{DME} cm^{-3} were achieved after reaching thermally self-sustained mode using the embedded micro-heater in combination with the exothermic reaction.

All in all, this work shows the great potential of monolithic MEMS-based micro-reactors (and their flexibility to reform different types of fuels depending on selective deposition of catalysts) for the final application in on-demand hydrogen production for portable systems.

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CONCLUSIONS

The present work was devoted to the development of scalable processes to fabricate thin-film devices with a focus on high-temperature technologies such as micro-SOFCs systems and miniaturized oxygen sensors.

In the first place, the deposition of functional materials on large-area substrates (4-inches silicon wafers) was optimized using different deposition methods. Next, the wafer-level microfabrication of different component forming the energy generator and the sensor was presented, e.g., micro-SOFC units, miniaturized oxygen-sensing platforms, and micro-reactors for on-demand gas reforming. The strategies designed to reach these goals open new horizons for the commercialization of such devices by either allowing for more efficient operation, cheap mass-scale production, or wider temperature range for operation.

The highlights selected from the present thesis are listed below:

- **Optimization of the large-area deposition of ceramic materials by PLD, ALD and SALD**: the combination of these techniques allowed for the uniform deposition of high-quality functional layers with tunable properties.

    - **Large-area PLD** was used to deposit the ceramic electrolyte (3YSZ) and MIEC electrodes (CGO and LSC) with controlled thicknesses and micro-structural and morphological properties. Indeed, it was possible to achieve very dense and crystalline as-deposited films as well as porous and amorphous, carefully selecting the deposition parameters depending on the desired output. Finally, dense 3YSZ and LSC82, and porous CGO82 were chosen as model materials for integration in real devices, allowing operation at temperature above 600 ºC.
    - **ALD** was performed to deposit oxygen vacancy-stabilized zirconia (OVSZ) that was combined with the 3YSZ deposited by PLD to form a superior electrolyte, preventing typical short-circuit problems originating from particle ejection and pinholes. The as-deposited material showed a typical high-temperature phase (tetragonal) without extrinsic doping, metastable up to 700 ºC, and presenting an ionic conductivity character without any relevant electronic contribution, making it ideal for applications as high-temperature electrolyte.
    Moreover, the conformal character of ALD coatings allowed for the functionalization of the active area of a micro-reformer with a Al_2O_3/Pt catalytic system. A uniform Al_2O_3 coating (catalyst support) was indeed achieved within the active area of the micro-reactor, constituted by an array of vertically aligned micro-channels with high aspect-ratio. Crystallization of such amorphous coating was achieved by **RTP**. Subsequently, the ALD deposition of Pt on top of Al_2O_3, showing an island-like growth, was optimized to achieve a uniform dispersion of nanoparticles (9.6 nm in diameter) accounting for 1%wt with respect to the catalytic support.
    - **SALD** deposition technique was developed during this thesis for the fast deposition of high-quality ceramic layers based on ceria for future application in high-temperature catalytic devices. The careful selection of a non-toxic cerium precursor with sufficient volatility together with the optimization of the SALD hardware (and its thermal management) allowed for the deposition of dense $CeO_{2-\delta}$ thin films using H_2O as co-reactant. This method resulted in growth rates 15 times higher than conventional ALD and showed very low carbon contamination, making it suitable for application in catalysis and micro-SOCs.

- **Scalable microfabrication of thin-film devices for micro-SOFCs and oxygen sensing**: the integration of ceramic functional layers in silicon technology allowed for a high-throughput and scalable method to fabricate micro-devices. Indeed, the optimization of clean-room processes allowed to obtain more than 50 devices for each processed 4-inches wafer, showing high reproducibility.

    - **Micro-SOFC units** based on suspended ceramic membranes (cathode-electrolyte-anode) were fabricated including the electrolyte bilayer (3YSZ and OVSZ) to prevent pinholes formation. Moreover, with the optimization of the fabrication flow considering the effect of the residual stress of the films on the buckling of the free-standing membranes, the yield of fabrication was increased 4-fold.
    Furthermore, a new design was proposed to increase the active area per unit cell and the area utilization of the membranes. **Large-area membranes** (1 to 82 mm^2) were designed and fabricated including a doped-silicon grid as a mechanical support for the array of small circular membranes (200 μm in diameter), increasing the active area by two orders of magnitude compared to the **standard squared membranes** (0.04 to 0.64 mm^2). The electrochemical characterization performed showed that the inclusion of the OVSZ layer allowed for OCV values close to the theoretical, while for a small membrane, a maximum power output of 40 mW/cm^2 at 600 °C was obtained.
    Finally, the design of a micro-SOFC power generator based on the vertical stacking of multiple components, namely micro-SOFC units, **interconnects**, and glass lids, was proposed.
    A complete micro-power generator for use in portable applications should be fed by hydrocarbon-based fuels for compactness and safety reasons. To this end, a **micro-reformer unit** for on-demand hydrogen production from DME was fabricated in this work. It comprised an array of vertically aligned micro-channels with an overall active area of about 120 $cm^2\,cm^{-3}$ and functionalized with a model catalyst (Al_2O_3/Pt), and an embedded thin-film heater for efficient hybrid start-up of the partial oxidation reaction.
    Finally, advanced ceramic **3D printing** was applied to the fabrication of customized insulation packaging for testing micro-SOFC components in real operating conditions, as in the case of the micro-reformer unit, indeed able to start up a reforming reaction with an energy consumption <500 J.
    - **Miniaturized oxygen sensors** were designed for IoT applications and real-time monitoring in high-temperature environments. Here, micro-machined silicon platforms included a squared suspended membrane, i.e., the sensing unit, comprising a thin-film electrolyte (3YSZ+OVSZ) and two symmetric LSC air electrodes (plus current collectors). The novel design developed in this thesis included a through silicon via made of doped silicon to contact the bottom electrode from the top of the sensor. This innovation in the design allowed to create a gas-tight cavity as a reference, while both electrodes are contacted from the same side.
    The platform was encapsulated with a HOYA glass lid, previously micro-machined, and gas-tightness was provided by the **glass-ceramic sealing**.

Thorough characterization and optimization of the slurry deposition by robocasting were essential to the results obtained, guaranteeing safe operation up to 600 ºC.
The sensor's performances showed excellent performance comparable to commercial technology (operating at higher temperature and including Pt electrodes), showing a stable and reproducible response in a range between 0.01-100% of oxygen content and with a voltage output in agreement with theoretical values.

The aim of this thesis was to put hands-on technologies that are particularly challenging to fabricate due to the harsh conditions at which they are supposed to operate. A mixed approach, in which materials engineering at the nanoscale and microscale meet, was the key to achieve the fabrication of game-changing energy devices for the world of portable devices and IoT sensing.

ANNEX

TOWARDS A MICRO-SOFC PORTABLE POWER GENERATOR

Annex - Towards a micro-SOFC portable power generator

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A.1 Introduction

The development of portable power sources with outstanding energy density has been a challenging target for scientists and engineers that want to overcome the limitations of the current technology. In the specific case of micro-SOFCs, a few different designs (see chapter 1.3.4) have been proposed to optimize the overall performances as well as to overcome technological issues of such systems.

On one hand, the power source should be designed with a modular approach, allowing for integration in portable devices with different power requirements. The stacking of multiple fuel cell units is thus necessary to achieve the desired power density for a certain application.

On the other hand, many challenges to fabricate micro-SOFC originate from the stacking itself. For instance, the planar stacking design adopted in the Lilliputian system [1] has the great advantage of simplifying the microfluidics for gas distribution and the electrical connections between fuel cell units, but the main drawback is linked to thermal gradients across the device length. It is indeed harder to insulate the planar device due to higher surface-to-volume ratio and eventually this can lead to failure and breakage.

Improved thermal management can be achieved by vertical stacking of fuel cell units, as chosen by scientists at ETH Zurich [2] or at IREC [3]. Nevertheless, vertical stacking presumes higher complexity especially for electrical and microfluidic connections between multiple fuel cell units at the high temperatures required. Simplification of such configuration was obtained by using a single-chamber configuration [4], where two stacked anodes (or cathodes) are facing each other, and a single gas channel is used to feed two electrodes. Unfortunately, this design is restricted to two cells per stack.

Hence, the goal of this Annex was the design of a vertical stacking strategy and the fabrication of interconnected micro-SOFC components to demonstrate the feasibility of integration in a complete micro-SOFC system working at high temperature and based on previous studies from this group [3].

A.2 Micro-SOFC system

The micro-SOFC system presented in this work aimed at breaking the temperature limits of operation for micro-SOFC devices operating on hydrocarbons, designing a compact high-temperature unit comprising of a fuel processing unit, a fuel cells stack, and a post-combustor. Moreover, the fabrication of a thermally insulating packaging was necessary to implement such technology for portable applications.

The next sections introduce the chosen design for the micro-SOFC system and the micro-fabrication processes associated to the remaining components that have not been described in this thesis.

A.2.1 System design

With referring to the previous section, the portable power generator's design chosen in this work is founded on vertical stacking of squared silicon-based fuel cell units and on previous feasibility studies done by our group [3]. As consequence, the first step of this work consisted of designing proper electrical connections between electrochemical cells as well as microfluidic channels to feed the fuel (syngas generated by DME POX, see chapter 4) and the oxidant (synthetic air) to separate chambers containing the anode and cathode, respectively.

To do so, this work takes inspiration from traditional (bulk) SOFC technology and from silicon-based components fabricated for micro-PEMFC applications. Typical vertically stacked SOFC components used to provide microfluidic and electrical connections are known as interconnects, usually made of stainless steel embedding a protective coating to avoid degradation issues (e.g., chromium migration) caused by the harsh operating conditions [5]. These interconnects are usually structured to create a gas-diffusion layer to distribute the gas across the whole cell's active area. Finally, two configurations can be chosen depending on the power output specifications: serial stacking or parallel stacking, represented from a microfluidic perspective in Figure A.1 below.

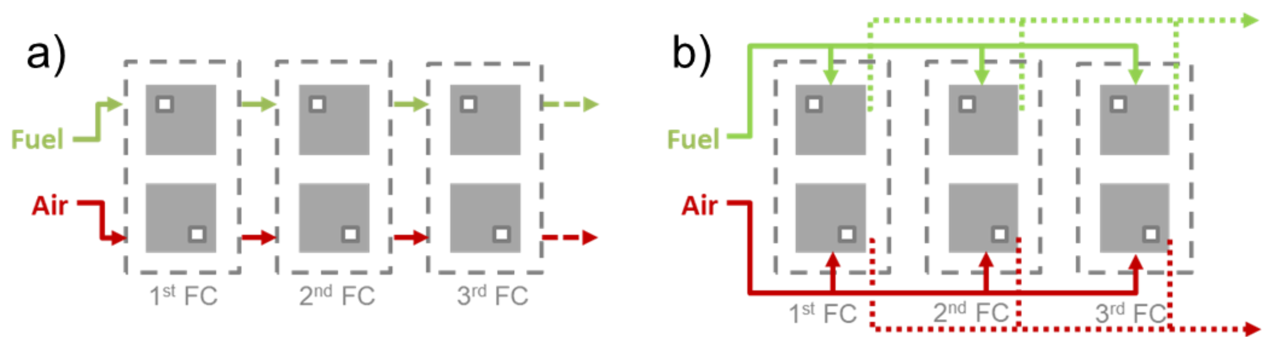

Figure A.1. Schematic view of the (a) serial or (b) parallel microfluidic connections

A silicon-based interconnect design was presented in [6], where bipolar plates were fabricated using clean room-compatible processes and demonstrated both in serial and parallel configuration. This design could indeed simplify the system thanks to the rotational symmetry and silicon micro-structuring to create a gas diffusion layer.

Nevertheless, to maximize the volumetric energy density of the device, the adoption of a serial configuration would allow to halve the number of interconnects per stack. Moreover, the serial electrical connection between consecutive cells results way easier than the alternate connection required by the parallel configuration. For this reason, the micro-SOFC power generator design hereby presented is based on the serial configuration depicted in Figure A.2.

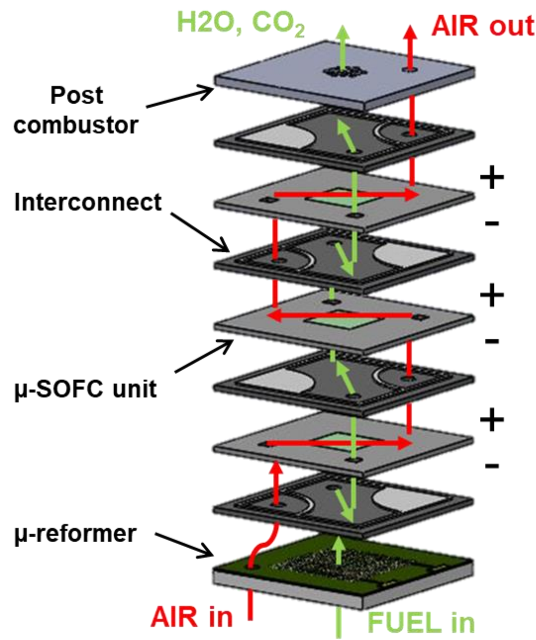

Figure A.2. Schematic view of the micro-SOFC stack with serial connection, labelling its multiple components. The fuel flow is marked with green lines, while the oxidant flow is marked in red color.

In the next sections, the interconnect design, fabrication, and characterization will be presented. Moreover, the optimization of a high-temperature sealant used to stack and hermetically seal the fluidic channels will also be discussed. This is indeed a critical component of fuel cells, as gas leakages are one of the main causes for voltage losses and reduced fuel consumption.

A.2.2 Micro-interconnects

The design and subsequent microfabrication of an interconnect unit for application in micro-SOFCs focused on minimizing the volume of the final stacked device. Considering a serial stacking approach, one single interconnect unit could function as electrical conductor to transfer electrons from one electrode to the next with opposite polarity. To do so, the interconnect must satisfy the following requirements:

- Low electrical resistivity
- Thermal stability and CTE compatibility with silicon
- Microfluidic channels and gas diffusion layer (GDL) on both sides of the chip with mirror symmetry and presenting negligible pressure drop
- Guidelines for sealant deposition

To meet these requirements, a new design for a micro-interconnect based on degenerated-silicon was elaborated, therefore ensuring optimal CTE compatibility with the silicon-based micro-SOFC units. The interconnect comprised of two vertical micro-channels and specially designed guidelines for GDL and sealing deposition, obtained following a micro-fabrication approach. The schematic view of the interconnect is included in Figure A.3.

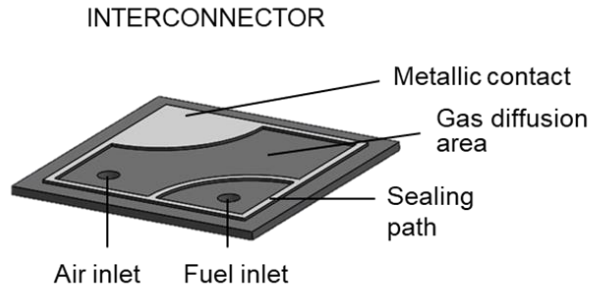

Figure A.3. Schematic representation of a micro-interconnect unit

The fabrication of such interconnect with symmetric micromachining on both sides is non-trivial due to the need of steps with controlled height and the opening of channels throughout the bulk silicon wafer. The microfabrication flow adopted for such purpose is hereby described (see Figure A.4). A (1) 500 µm-thick degenerated silicon wafer (ρ = 0.005 Ω cm) and double-side polished is coated on both sides with (2) 1.5 µm thermally grown SiO_2. The GDL pattern is then transferred by (3) photolithography and reactive-ion etching (RIE) into the oxide layer (both sides). (4) A 100 nm-thick layer of Si_3N_4 is then deposited by LPCVD on both sides as well as (5) 4 µm of SiO_2 on the top face. (6) The microchannel mask is then used to transfer the pattern on the top face and etch it through by RIE until reaching the bulk silicon. The remaining oxide and nitride layers on the top face are used as mask for the (7) wet KOH etching of 270 µm into the bulk silicon. At this point, (8) the LPCVD-deposited films are wet-etched, leaving the wafer with the original GDL thermal SiO_2 mask. (9) A deep-RIE etching on the top face allows for creating a 150 µm-thick step, used as GDL and to accommodate the sealant. (10) The same process is then repeated on the back side, obtaining another 150 µm-thick step and finally opening the microchannels. The remaining oxide mask (11) is finally etched in HF solution. (12) Metallization with 10 nm of Ti (adhesion layer) and 100 nm of Pt by evaporation is carried out after the HF bath, to avoid the presence of native silicon oxide on the wafer surface.

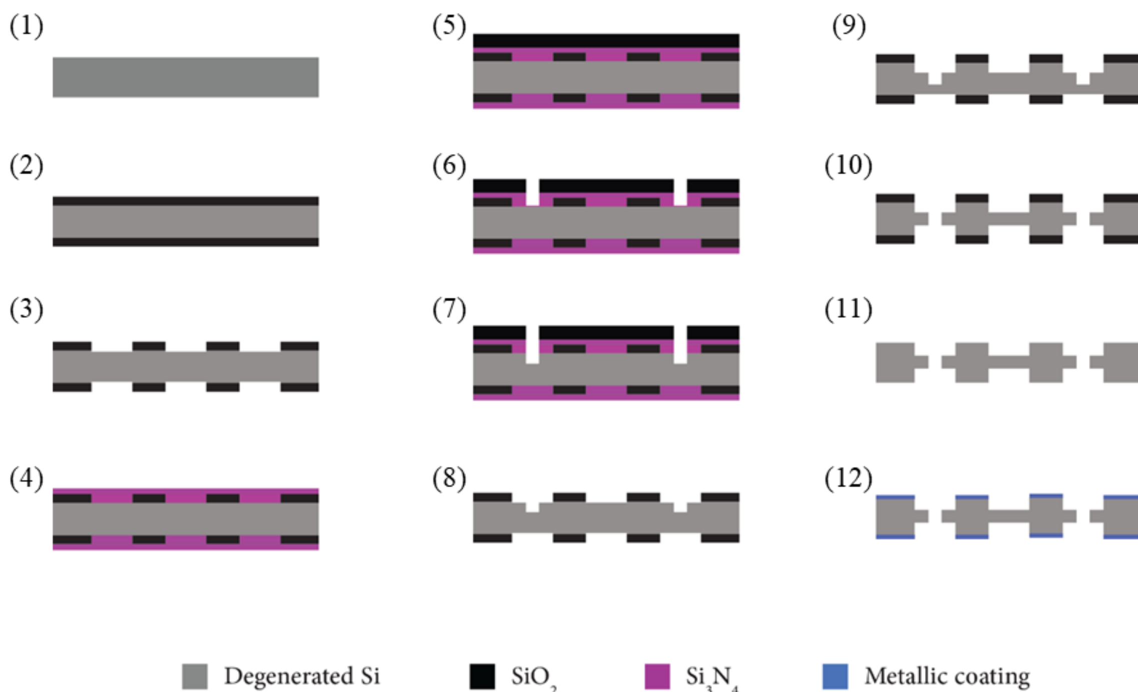

Figure A.4. Microfabrication flow for interconnects.

Figure A.5 included below shows the lithographic mask designed to transfer the pattern for the etching processes on both sides of the wafer. Two different pathways for the sealing deposition are included in 1x1 cm^2 interconnect units.

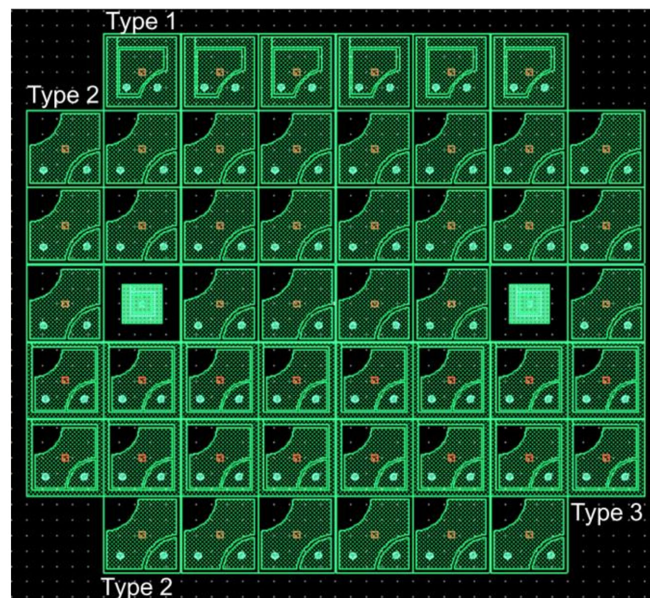

Figure A.5. Photolithography mask for the fabrication of silicon-based interconnects (in green) overlapped to a 1 mm^2 membrane (in red)

The microfabrication was carried out successfully, resulting in 42 interconnect units per processed wafer (Figure A.6). Slight over-etching of the channel was observed during the last RIE process, but two 150 µm-deep pools for gas diffusion were successfully obtained on the two sides of the wafer.

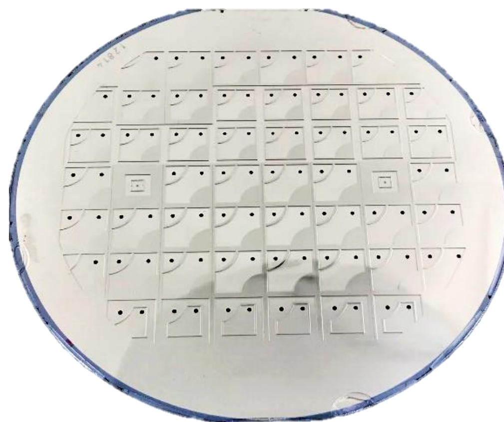

Figure A.6. Micro-machined degenerated silicon wafer (4-inches) for micro-SOFC interconnectors

Out-of-plane electrical measurements were performed to evaluate the resistance contribution of the interconnect to the stack and to optimize the metallization process, for instance by performing it right after the etching in HF solution. This way, the interconnect results protected from the atmosphere, impeding the growth of a native oxide layer (about 2.5 nm in thickness) that would drastically increase the electrical resistance as shown in Figure A.7.

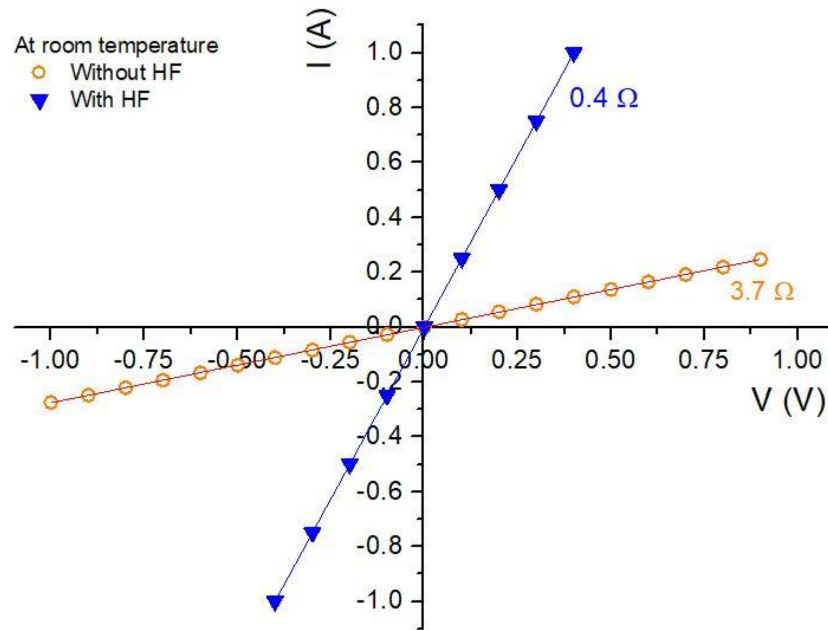

Figure A.7. Cross-plane DC electrical measurement of interconnects and the related resistance according to different metallization processes

A.2.3 Stack assembly

As previously mentioned in section 5.2.1, the micro-SOFC stack is designed with a serial configuration, meaning that it is necessary to create microfluidic connections between consecutive electrochemical cells and interconnects.

For this purpose, the fuel cell unit is specifically designed comprising a 0.36-0.64 mm^2 suspended membrane in the center of 1x1 cm^2 chip and two 0.8x0.8 mm^2 channels to drive the gas flows vertically across the stack[3]. The gas channels are fabricated following the same procedure used to fabricate suspended ceramic membranes but masking that region prior deposition of the electrodes, thus avoiding short-circuits once the channels are opened. Figure A.8 shows the features of a micro-SOFC unit and interconnector used for the stack assembly.

[3] For the sake of simplification, in this thesis, the dimension of the membrane has been limited to 0.64 mm^2 during the development of the stack. However, the dimension of the suspended membrane could be enlarged without mayor modification of the stack design (as shown in section A.2.1)

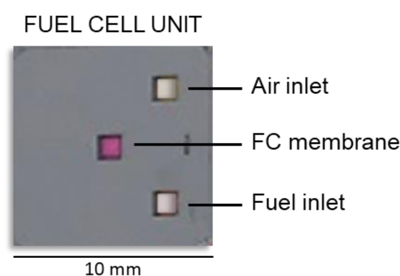

Figure A.8. Optical image of a micro-SOFC unit comprising of microfluidic channels

On the other hand, absolute gas tightness and reliable electrical connections can be achieved by optimization of the glass-sealing deposition procedure. Indeed, a thorough characterization of sealing was performed together with the optimization of the deposition procedure, previously presented in Chapter 5.3. Figure A.9 below shows an optical image taken during the sealing deposition.

Figure A.9. Optical image representing the extrusion of the slurry from a nozzle (robocasting)

An in-house fabricated holder for the micro-SOFC components, 1x1 cm^2 and with different thicknesses, was used to allow for the reproducible deposition of the sealant on multiple assembly components. Finally, all the components were stacked following a specific order within a special metallic holder (1.1x1.1 cm^2) that was eventually placed in furnace, leading to the good alignment of all the micro-fluidic features.

As a reminder, the optimization of the joint procedure included the following steps:

- A drying step (at 70 ºC, 5 min) was performed between the paste deposition and the assembly
- A 200 g weight is placed on the stacked parts upon thermal treatment
- Dispensed paste thickness was about 33% higher than the interconnect step (150 µm-deep), to compensate for the volumetric shrinkage of the sealing upon firing.

Figure A.10 shows the X-ray inspection performed in order to assess the quality of the stacked parts, i.e., a fuel cell and an interconnector. Figure A.10-(a,b) report the result of the assembly with insufficient sealing line height (h ~ 175 µm) where open porosities are evident. Indeed, considering that the glass seal showed very high wettability on the substrates used in this thesis, diffusion and coarsening had to be expected. Increasing the amount of paste dispensed and the sealing line height to ~250 µm allowed for a better quality of the sealing, although many voids are still observed in the sealing as shown in Figure A.10-(c,d). Finally, the addition of a drying

step prior assembly allowed for evaporation of the solvent and resulted in an optimal glass-ceramic sealing with low porosity and controlled width. The result that had been replicated for all the assembled stacks in shown in Figure A.10-(e,f).

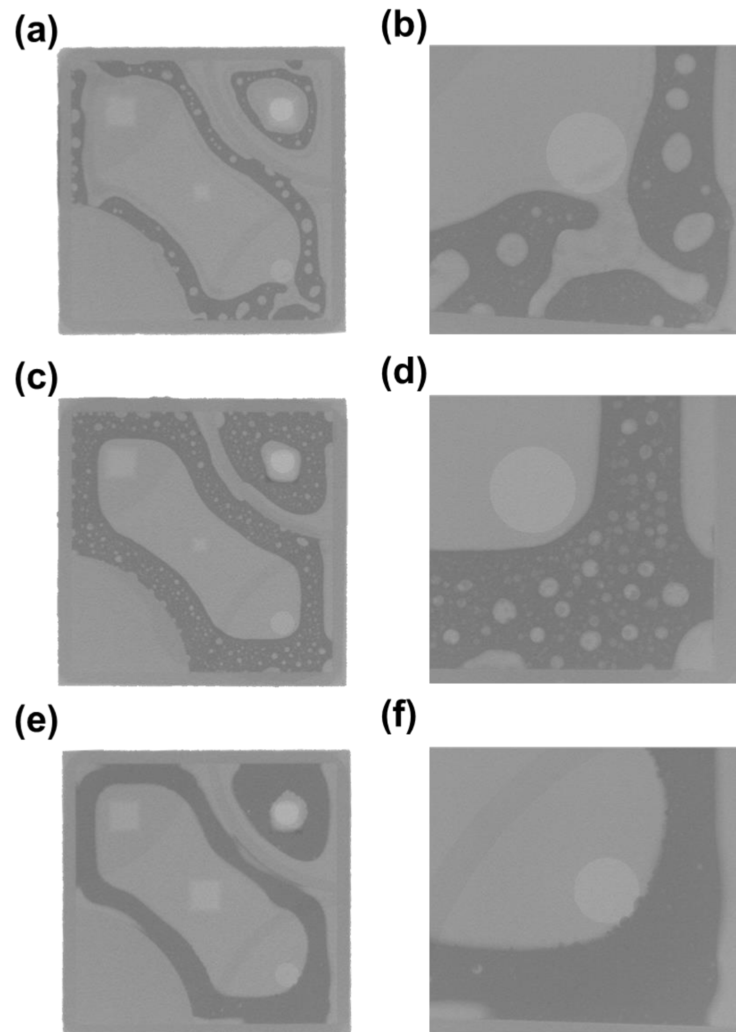

Figure A.10. Top-view X-ray inspection of the joint obtained between a micro-SOFC unit and an interconnector, where (a,b) the dispensed line had insufficient height; (c,d) no drying step was applied; and (e,f) a drying step prior assembly was performed.

Finally, once the optimal conditions for the sealing were met, multiple components of the final devices were stacked on top of each other. Specifically, the proof-of-concept stack hereby presented was obtained by "sandwiching" two micro-SOFC units in between three interconnectors, and two glass lids (1 mm-thick) were eventually stacked at the extremities in order to provide a mechanically robust interface with the ceramic packaging.

A cross-section SEM image of the obtained micro-SOFC stack is presented in Figure A.11. Here, a good alignment between the two stacked parts can be observed. The width of the sealing was usually observed to be about 300 to 600 μm in width, providing good hermeticity. Here, some void in the sealing could be noticed, yet no open porosities were detected. Moreover, thanks to the interconnect design, the height of the GDL (150 μm) was very reproducible.

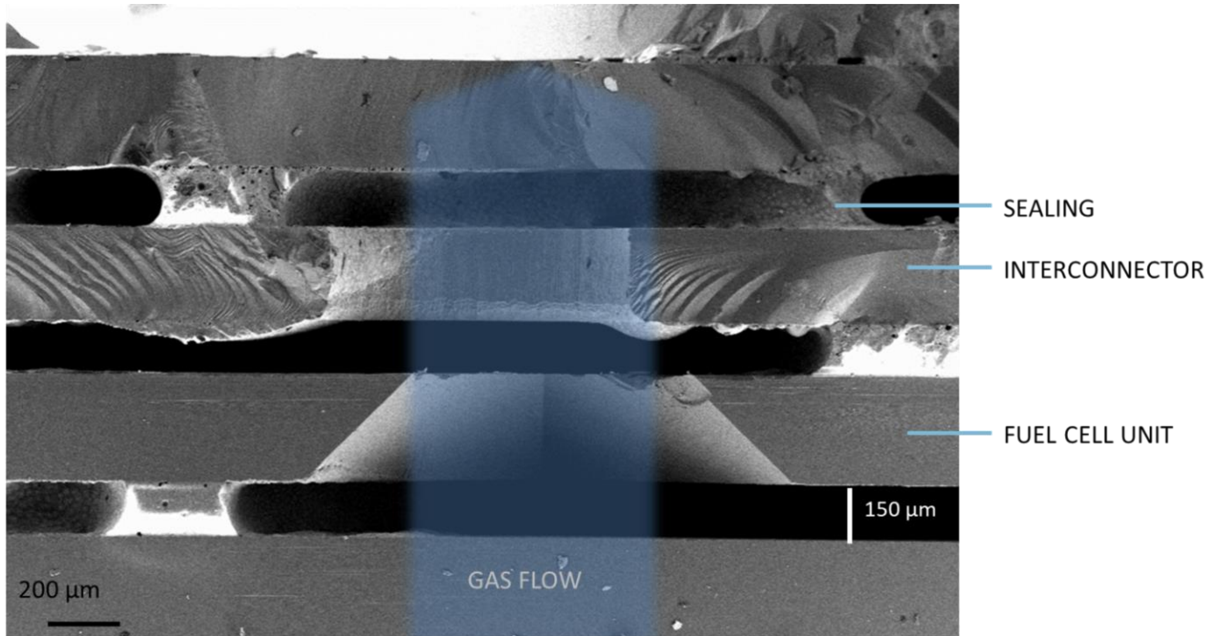

Figure A.11. Cross-section SEM image of a micro-SOFC stack showing the alignment between microfluidic channels

A.2.4 Packaging with ceramic 3D printing

Recent advances in 3D printing for advanced ceramic materials had opened the doors for new applications in energy devices (see Chapter 2.3.2) [7]. Previous feasibility studies within our ERC UltraSOFC project framework [3,8,9] provided useful insights on the design of a ceramic packaging for thermal insulation of the hot module of a micro-SOFC. 3D printing was therefore chosen for the customization of a ceramic packaging designed to accommodate the micro-SOFC stack described in A.2.3 and shown in Figure A.12.

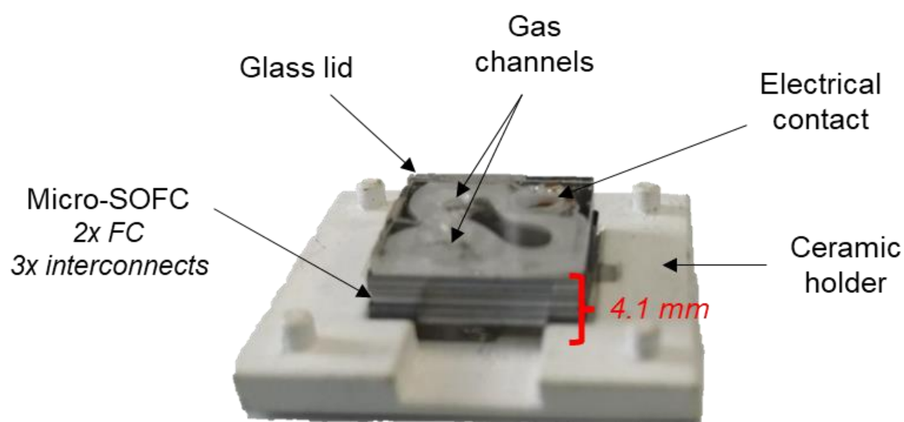

Figure A.12. Optical image of a two-cells micro-SOFC stack

The micro-SOFC stack presented above, comprising of two fuel cell units and the components necessary to perform microfluidic and electrochemical tests, measured exactly 4.1 mm in thickness. Two glass lids were also included in the assembly in order to provide a gas connection

between the ceramic holders and micro-SOFC stack without risking breaking some more fragile components such as those based on silicon.

Therefore, the in-house fabrication of a ceramic packaging accommodating the stack considered such thickness for a perfect matching with a compressive sealing system based on alumina felt, preventing any gas leakages between the packaging and micro-SOFC stack. For better understanding of the experimental set-up, a schematic representation is included in Figure A.13.

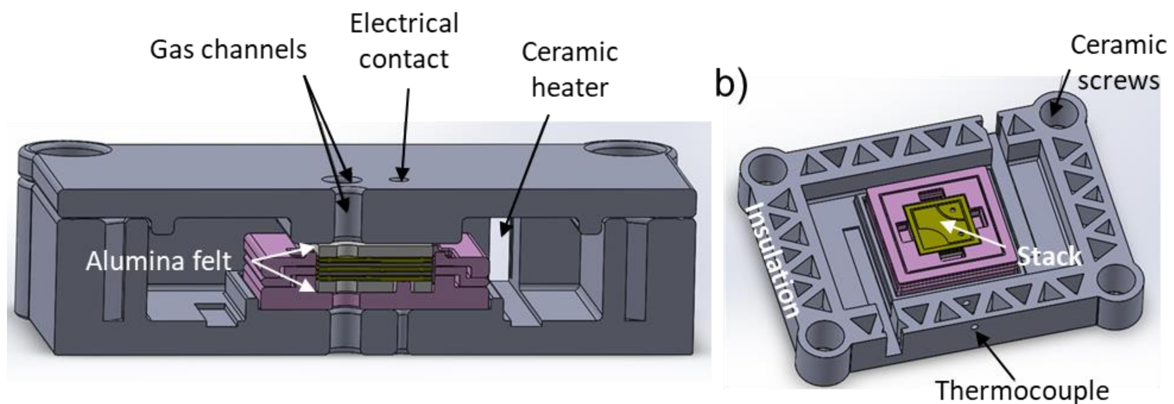

Figure A.13. (a) Cross-section and (b) top view schematic representation of the experimental setup for micro-SOFC stack testing based on a 3D-printed ceramic packaging

The design of the packaging presented above aimed at providing a reusable and efficient platform for micro-SOFC testing, while adapting its geometry to the microfluidic and electrical configuration of the micro-SOFC stack. Moreover, it included space for two ceramic heaters (AlN-based glow igniters from Bach RC GmbH) that were used to heat up evenly the specimen.

Finally, the SLA ceramic printing method described in Chapter 2.3.2 was applied to the fabrication of the experimental setups presented above. Indeed, Figure A.14 shows the results of the 3D printing processes after removing the ceramic paste in excess that did not polymerize. The green bodies shown here did undergo a de-binding thermal process to remove all the organics from the solid and was then sintered at 1550 ºC. This thermal treatment resulted in very hard ceramic pieces showing great compressive strength, hence ideal for performing a compressive sealing with an alumina felt sealant.

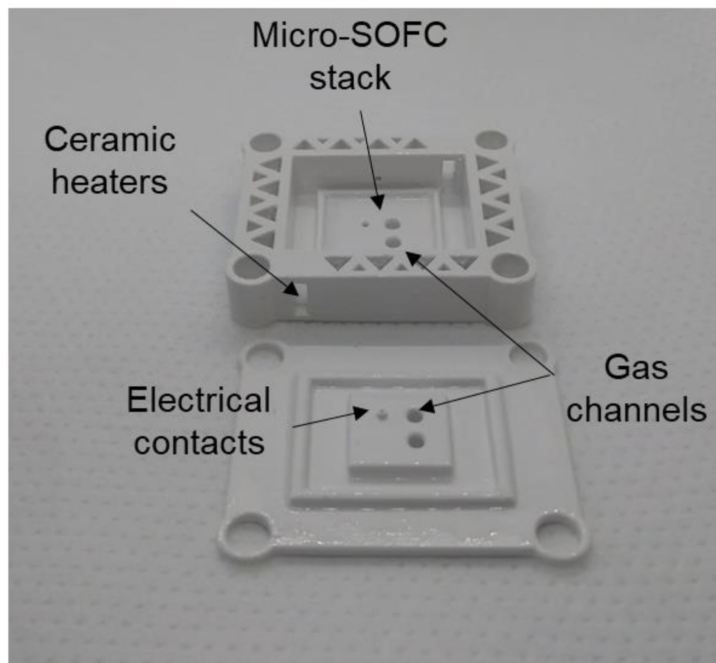

Figure A.14. Optical image of the 3D-printed ceramic packaging for the functional characterization of the 2-cells micro-SOFC stack

Nevertheless, it was observed that the maximum temperature reached during sintering was not sufficient to obtain the ideal density of a ceramic insulator. Specific density measurements showed indeed that the sintered body could reach only 81% density. Moreover, the thermal conductivity of the sintered alumina was observed to be way higher than expected for this type of material. Indeed, the thermal conductivity of this alumina pieces was found to be five times higher than the desired value of 5 mW m^{-1} K^{-1} from [3].

For this reason, further optimization of the ceramic paste and especially of the sintering process is necessary to ensure the experimental conditions required by such complex high-temperature measurements, where great thermal insulation is especially important for the self-sustained operation of high-temperature devices.

A.3 Conclusions

In this work, a new design for micro-SOFC portable power generators based on serial connections between micro-SOFC units and interconnects stacked vertically on top of each other was presented.

This design allows simplification of the system, offering high compactness of the micro-SOFC stack and therefore a better thermal management. To this end, a new design of an interconnect unit based on degenerated silicon substrates was presented aiming at connecting two alternated micro-SOFC units in series (whose goal was therefore increasing the voltage output of the device). This design was perfectly aligned with the features included in a micro-SOFC unit, i.e., the suspended membrane and two micro-channels used to drive either the fuel or the oxidant to the respective chambers. The successful fabrication of these components was achieved using clean-room compatible processes.

Moreover, the assembly of all the components of a micro-SOFC stack was presented, implementing the deposition of glass-ceramic sealing by robocasting presented in Chapters 2.3.1 and 5.3. The alternated deposition of sealant on the interconnects, flip-chip, and alignment of micro-SOFC units using tools fabricated in-house ensured very reproducible results. To this end, a strategy for optimizing the sealing and the thermal treatment was presented to achieve the many requirements this technology presents. X-ray inspection confirmed the quality of the sealing and the absence of voids between components.

Finally, the application of SLA technology to ceramic manufacturing was employed in this work to obtain customized insulating packaging for the micro-SOFC stack. This packaging aimed at containing the high operating temperatures of the micro-SOFC and enabling a better thermal management, as well as providing suitable electrical and microfluidic connections between the packaging and the micro-SOFC stack.

All in all, this chapter provided a solid and reproducible fabrication method for micro-SOFC stacking and a tool for the functional characterization of micro-power generators based on such technology. Ceramic 3D printing demonstrated a potential candidate for the fabrication of insulating and hermetic packaging comprising of complex shapes.

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