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Advanced characterization methodologies of the time dependent variability in CMOS technologies

Gerard Pedreira Rincón

Universitat Autònoma de Barcelona

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Author:

Gerard Pedreira Rincón

Supervisors:

Dr. Javier Martín Martínez

Dra. Montserrat Nafría Maqueda

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Universitat Autònoma de Barcelona

The undersigned, Dr. Javier Martíin Martíinez and Dr. Montserrat Nafría Maqueda

CERTIFY:

that the thesis entitled "*Advanced characterization methodologies of the time dependent variability in CMOS technologies*" has been written by the Ph.D candidate **Gerard Pedreira Rincón** under their supervision, in fulfilment of the requirements for the Ph.D degree of Electrical Engineering and Telecommunications program.

Bellaterra (Barcelona), March 2023

Agraïments:

M'agradaria començar els agraïments de la meva tesis doctoral donant les gracies a totes les persones que han compartit part d'aquest procés durant aquests anys.

Primer de tot, donar les gracies als meus dos directors, la Dra. Montserrat Nafría Maqueda i el Dr. Javier Martín Martínez. Ambdós heu sigut una font d'inspiració i us vull comunicar el meu agraïment per guiar-me i orientar-me durant tota la duració de la tesis doctoral. Tot i els entrebancs que la situació del COVID-19 ha provocat en el punt mig de la realització de la tesis, m'heu demostrat la paciència i adaptabilitat necessària per superar aquests entrebancs i que he intentat imitar per tal d'aconseguir finalitzar el doctorat.

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Preface

From the invention of the first working transistor, the point-contact transistor, in 1947, passing through the invention and creation of the first Metal Oxide Semiconductor Field Effect Transistor (MOSFET) in 1960 to nowadays transistors, the semiconductor industry has been evolving at an exponential rate. The constant reduction on the size of the new transistors over time have taken the technology from micrometers to the newly developed 3 nm size transistors, not yet commercialized.

The exponential scaling that has characterized this industry the past 50+ years has demonstrated to add a lot of benefits when it comes to, for example, power, device density and performance. Despite that, the size reduction made apparent that when approaching sizes closer and closer to the atomic level, several new critical effects appear that pose a detriment to many aspects of highly scaled devices. Some of those effects can be high variability of device characteristics between devices with the exact same design or the aging effects that get proportionally more significant. Also the reduction on the oxide thickness makes leakage currents due to tunneling way more significant. Under these circumstances, the industry have ideated new and innovative ways to counteract this effects. Some examples can be changes in architecture like FinFET or FD-SOI devices, engineering of ney High-K materials to reduce the gate oxide tunneling. This has allowed the industry to continue the scaling trend but this scaling has a hard limit concerning the size of the atoms. In this scenario, the importance of reliability and aging characterization is higher than ever before.

As most of the effects regarding variability are stochastic in nature, the characterization of those effects has the need of a high number of devices for each technology under a plethora of conditions in order to obtain statistically accurate information. These the variability effects can be divided between two main groups. The first being time-zero variability, that encompass all the variability effects that come from the fabrication process and can produce a random or systematic shift in the devices properties. The second one being time dependent variability, that encompasses the shifts on the device or circuit parameters caused by the active use of it. The time dependent variability can come from transient effects like for example Random Telegraph noise or aging effects like Bias Temperature Instabilities or Hot Carrier Injection, etc.

If the circuit designers want to reduce or mitigate the effects that those variability effects cause, a deep characterization of these phenomena is absolutely necessary. As those variability effects are stochastic in nature, a high number of devices are needed to characterize them, and some of the mentioned effects can have lasting effects with duration of years, making the necessary experimental times unfeasible.

Under this pretext, the present thesis will present a new characterization method followed by its validation and application to a plethora of experimental conditions in order to demonstrate its usability and advantages. The presented method focuses on the ability to

reduce experimental times exponentially when the tests involve long measurement times and a high number of devices under test.

In this context, the first chapter of this thesis will introduce the reader to the main sources of variability in today's technology CMOS devices, followed by the description of the main Methodologies used in the duration of this thesis. The methodologies will describe the main methods used in literature and also describe the main methodology used during this thesis, involving measurement techniques, the main studied devices from the ENDURANCE chip, originated from a previous thesis project from this group, from Javi Diaz Fortuny, and the hardware and software set-up considerations.

Following this introduction, the second chapter will start presenting a traditional characterization method, Weighted time lag plot, that will become the reference point for the validation of the proposed method. This will be followed by the description of the proposed method and its operation. Finally this chapter will end with the validation of the method with the help of Random telegraph noise experiments and several statistical and mathematical studies regarding the proposed method.

Finally the third chapter will present an expansion of the proposed characterization method to add aging phenomena to its considerations, followed by the description and analysis of different designed experiments with the proposed method . The testing conditions presented in this third chapter will involve accelerated aging BTI experiments, accelerated aging BTI plus HCI experiments with a wide range of gate and drain stress voltages, FD-SOI device characterization and finally long time RTN experiments.

Publications related with this thesis:

International Journal papers as first author.

1- G. Pedreira, J. Martin-Martinez, P. Saraza-Canflanca, R. Castro-Lopez, R. Rodriguez, E. Roca, F.V. Fernandez, M. Nafria, "Unified RTN and BTI statistical compact modeling from a defect-centric perspective", Solid-State Electronics, Volume 185, November 2021, 108112

Conference Contributions as first author:

1- G. Pedreira, J. Martin-Martinez, J. Diaz-Fortuny, P. Saraza-Canflanca, R. Rodriguez, R. Castro-Lopez, E. Roca, F. V. Fernandez and M. Nafria, "A new time efficient methodology for the massive characterization of RTN in CMOS devices", in Proc. International Reliability Phisics Symposium (IRPS), April 2019. Monterey, CA, USA, pp. 1-5
2- G. Pedreira, J. Martin-Martinez , P. Saraza-Canflanca , R. Castro-Lopez , R. Rodriguez , E. Roca , F. V. Fernandez , M. Nafria, "Unified RTN and BTI Statistical Compact Modeling from a Defect-Centric Perspective", in 22TH Conference on Insulating Films (INFOS), July 2021 published in Solid-State Electronics, Volume 185, November 2021, 108112
3- G. Pedreira, F. Gammarota, J. Martin-Martinez, A. Crespo-Yepes, E. Amat, R. Rodriguez, M. Nafria, "RTN and BTI statistical characterization of Ω-gate FDSOI devices at low voltages" accepted on International conference on Ultimate Integration on Silicon (ULIS), May 2023
4- G. Pedreira, J. Martin-Martinez, R. Castro-Lopez, E. Roca, R. Rodriguez, F. V. Fernandez, M. Nafria, "Model parameter extraction of CMOS Time-Dependent Variability in a wide range of gate and drain voltages", pending of revision 14th Spanish conference on Electron Devices, June 2023

Conference Contributions as a co-author:

5- J.Martin-Martinez, G. Pedreira, P. Saraza-Canflanca, J.Diaz-Fortuny, R. Castro, R. Rodriguez, E. Roca, X. Aymerich, F.V. Fernandez, M. Nafria. "A complete smart approach for the RTN characterization and modelling of scaled MOSFETs" – Spanish Conference on Electronic Devices (CDE), June 2021

Chapter 1

Variability and reliability Phenomena in deeply scaled transistors.

As the electronics technology evolves over time, the downscaling trend that this entails creates higher variability as the technology size approaches more and more to the atomic size. This creates variations in transistor parameters, like threshold voltage (Vth), at the fabrication process level and an increasing variability during operation time. These variability is a major culprit behind performance variations that can fatally impact the device or integrated circuits (IC) performance, for this reason, the involved phenomena have been statistically characterized and modeled for many years [1-3]. The variability origins have been traditionally divided in two groups, time-zero variability (TZV) and time-dependent variability (TDV), and the effects comprised on both categories can negatively compromise the reliability and the intended lifetime of highly scaled devices.

In this context, this first chapter will describe the most relevant sources of TZV and TDV that affect nanometer scale transistor devices. Moreover, the methodology used to experimentally characterize devices involving both for TZV and TDV effects.

1.1 - Time-zero variability

Time-zero variability (TZV) is described as the permanent deviations of the transistor parameters from the nominal values occurred during the fabrication process. Although this thesis will not focus on this kind of variability a brief description of the origins of these deviations will be presented in this section.

The main sources of TZV affecting CMOS transistor device fabrications are: Random Dopant Fluctuations (RDF), Line-Edge Roughness (LER) and Line-Width Roughness (LWR), Oxide Thickness Variations (OTV), among others. [4,5]

1.1.1 - Random Dopant Fluctuations

Random Dopant Fluctuations (RDF) are caused by the statistical variation in the number and location of the dopant atoms in the channel region of a transistor. This distribution determines, for example, the threshold voltage (Vth) of the transistors or the on current of that device. Figure 1.1 shows a schematic representation of the main Time-Zero variability sources. The case of the RDF is located on the substrate region of the transistor were a random number of dopant atoms are located.

With the technology downscaling, the number of dopant atoms is reduced exponentially with the size of the devices [6,7]. This makes these fluctuations even more prominent due to one atom being a higher change in dopant density, for example, having 1 more dopant atom on a 10000 dopant atoms group is a 0.01% variation but when 1 more atom is introduced to a group of 100 dopant atoms, that sole atom is a much more significant variation of 1%.

1.1.2 - Line-Edge and Line- Width roughness

Another source of variability related to the downscaling of devices at the nanometer scale are both Line-Edge (LER) and Line-Width roughness (LWR). Both of these sources of variability come from imperfections or variations in the gate edges of transistors that result in uneven shape with respect to a linear edge. In this case, the source of this imperfections is related to both lithography and etching processes during fabrication.

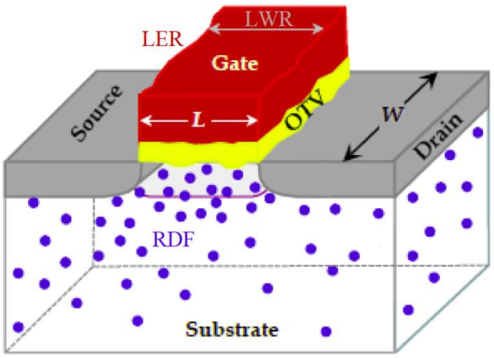

Figure 1.1: Example of LER/LWR, RDF and OTV in a MOSFET device [3]

The same way as RDF, both LER and LWR are not scalable according to the CMOS technology trend. These effects were not a relevant variability origin in larger transistors (> 100 nm channel length as these effects remains at an approximately ~5 nm

independently of the fabrication process. However, in nowadays downscaled technologies, this 5 nm is a significant fraction of the transistors L or W making these two effects much more relevant [8,9]. Moreover, when modeling the transistors behavior, the inclusion of these two effects shows an increase of the TZV on transistor of identical design [10,11]

Combined studies of RDF, LER and LWR effects have been presented and concluded that both phenomena are statistically independent. Moreover, when studying devices with a channel length below the 20-nm LER/LWR becomes the main source of TZV, while for devices with higher channel lengths, RDF becomes dominant. [8,10,11]

1.1.3 - Oxide Thickness Variations

In advanced technology nodes, device insulator thickness below 10 nm is an important source of intrinsic parameter fluctuations such as Oxide Thickness Variation (OTV). OTV is caused by imperfections or roughness in the Silicon/insulator and the gate/insulator interfaces across the gate of transistors. This fluctuation in thickness can cause variations in Vth or gate tunneling current [12,13] between identically fabricated devices.

1.2 – Time dependent Variability

Apart from the influence of the TDV effects presented in the previous section, the description of the device characteristic parameters must be completed with the study of both transient effects and degradation effects during its operation time. In this scenario, the Random Telegraph Noise (RTN) phenomena as a transient effect, the Bias Temperature Instability (BTI) and Hot-Carrier Injection (HCI) as aging effects are the critical issues that the nowadays technology is facing [14-17]. Both RTN and BTI mechanisms are thought to be related to a charge trapping/detrapping in/from device defects located on the device insulator, bulk, or interfaces and present a stochastic nature, while HCI consists of a degradation mechanism were highly energetic carriers accelerated by the present electric field breaks into the dielectric creating a permanent alteration of the electrical properties. The origins of the defects can be attributed to both being originated during the fabrication process or generated during operation time as a consequence of aging. [18]

The trapped/detrapped charges cause a variation on transistor performance from the as-fabricated values over operation time that can ultimately cause a malfunction or permanent failure [19]. Each individual defect appearing in a device is described by three different parameters: mean emission time (τe), mean capture time (τc) and the drain current shift (ΔId) associated with the trapping/detrapping of charge. The ΔId can be also equivalently translated in to a ΔVth. The analysis of these parameters in literature revealed some key characteristics. The first being, both capture and emission times constants are uncorrelated and are bias and temperature dependent [20]. The second key characteristic is that capture and emission defect time constants can vary of up to decades

of time, making the election of an appropriate time window to characterize them is of high importance. [21,22]

The Time dependent variability (TDV) effects referred as aging (BTI/HCI) entail the progressive degradation of devices operational parameters after a long use time (months or years) at nominal operation conditions. Some of the mechanisms included in aging are Bias Temperature Instabilities (BTI) or Hot carrier Injection (HCI). With a timescale of months or years, these two mechanisms characterization becomes unfeasible.

For this reason, accelerated aging tests are the typical method used to characterize these phenomena. These kinds of tests usually entail having temperature, gate and/or drain voltage raised above nominal operation levels over a shorter period of time to achieve a device parameter degradation with a significantly reduced experimental and measurement times. The experimental time while the experimental conditions are raised is called stress, while the devices are measured after the stress under nominal operation conditions.

This section will present an overview of the TDV effects relevant for this thesis and its traditional characterization methods, starting with random telegraph noise (RTN).

1.2.1 - Random Telegraph noise

Random Telegraph noise (RTN) is an effect that causes the random switch of the Ids current between two or more states over time (fig. 1.2). This has been recognized to be a significant source of variability since it's responsible for the variation of the device parameters like Vth [23]. The fluctuations on the current levels are associated to the charge trapping/detrapping on defects located on the oxide and interfaces, and it shows a large dependence on biasing and temperature conditions. Moreover, this phenomenon scales inversely with area size, making it a higher analysis priority for highly scaled devices[24,25]. This effect is not only present in traditional transistor technologies as it has been reported to appear in Resistive Random Access Memories (RRAM) [26], Fully Depleted FET (FD-SOI) [27], FinFET [28], Multigate FET [29,30], nanowire FET[31] devices and digital circuits. [32]

The standard RTN characterization on MOSFET devices starts with the measurement of Ids with Vgs and Vds bias at a constant voltage over a period of time. This allows the study of the current trace fluctuations and extract different parameters from its analysis like the capture and emission times or the current shift that each appearing defects cause [33]. As the values of these fluctuations can be in the order of nanoamps, an accurate measurement toolset is necessary. On the other hand, the measurement time required to properly characterize the RTN will depend on the intrinsic capture and emission characteristic times of the defects present on the studied devices, as RTN defects can have capture and emission times longer than what is feasible (months or years) for an experimental characterization.

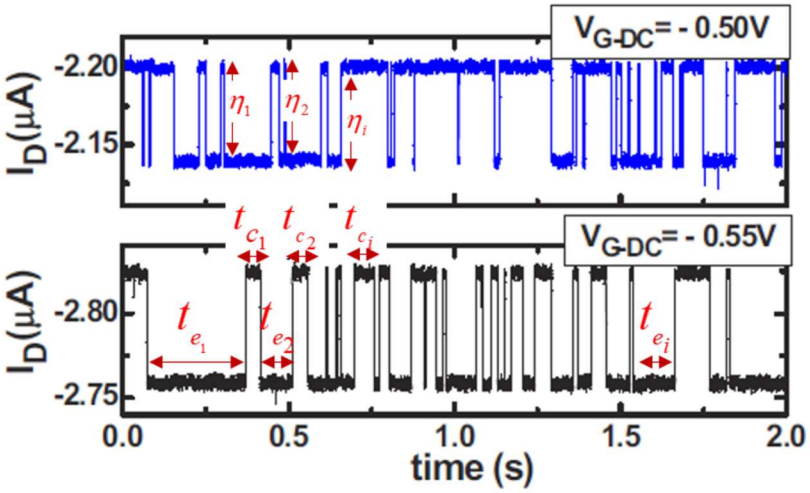

Figure 1.2: Figura de ejemplo de traza RTN

On the following section an example of a traditional RTN characterization method that analyzes the full ID trace will be described. This method called Weighted Time Lag Plot will be used in this thesis during the validation of the newly proposed characterization method that this thesis focuses on.

1.2.2 - Weighted Time lag plot (WTLP) characterization:

The Weighted Time Lag Plot (WTLP) is a full trace analysis method that allows the parameter extraction for random telegraph noise (RTN). When pertaining to the full trace analysis, the key parameters to analyze the RTN behavior and its impact in the technology under study are the number of defects (N) and the current shift (η) that those defects entail [45].

The weighted time lag plot (WTLP) is an analysis method that is an improvement of the Time Lag plot analysis (TLP) [46]. The TLP allows the accurate identification of different current levels when the background noise is elevated. This is achieved by plotting each current levels vs the current of the next data point on the Id vs time trace (fig. 1.3 a). This results in a point distribution where most of the points are located on the diagonal where the current of the next data point is approximately the same as the previous data point. Each of the large accumulations of points on the diagonal corresponds to each of the RTN levels, while if there are accumulations out of the diagonal they correspond to the transition between each of the RTN current levels. If the analyzed trace has a high background noise, then the identification of individual current levels from the point distribution becomes unreliable when those levels are too close, and so the TLP method becomes inaccurate.

The Weighted time lag plot (WTLP) improves on the TLP by assigning a normal distribution to each of those points with a standard deviation σ similar to the background

noise. Considering the a point of the plotted TLP, with coordinates (Ii , Ii+1) for this point it is defined:

$$\varphi_i(x,y) = \frac{1}{2\pi\alpha^2}\exp\left(\frac{-[(I_i - x)^2 + (I_{i+1} - y)^2]}{2\alpha^2}\right) \quad (1)$$

where x and y are the coordinates of space where the TLP is considered. Note that ϕi is a normal bivariate distribution with standard deviation α and correlation coefficient 0. Then ϕi (x, y) represents the probability that the point with coordinates (Ii , Ii+1)corresponds to a level or to a transition in the location (x, y) of the TLP space. After the ϕi definition, we define the weighted time lag function Ψ as:

$$\Psi\,(x,y) = K\sum_{i=1}^{N-1}\varphi_i \quad (2)$$

Being K a normalization constant chosen to get the maximum value of Ψ to be 1 and N being the number of point in the studied trace. Figure 1.3 b shows the WTLP corresponding to 8a TLP where the maximum on each current level can be seen more clearly.

The diagonal (x=y) profile is corresponds to the current values that did not change between ti and ti+1, indicating the different RTN levels for this trace. The diagonal alone gives information about the current levels and relative appearance on the trace, while the rest of the WTLP gives information about the transitions and the noise spread of that trace. Considering that each defect within a device causes two different current levels, the number of defects in each trace can be calculated from

$$N_{def} = \text{Int}\,[Log_2(N_{Lev})] \quad (3)$$

being the Int [] the integer-valued function of [Log2(NLev)] and NLev the number of current levels.

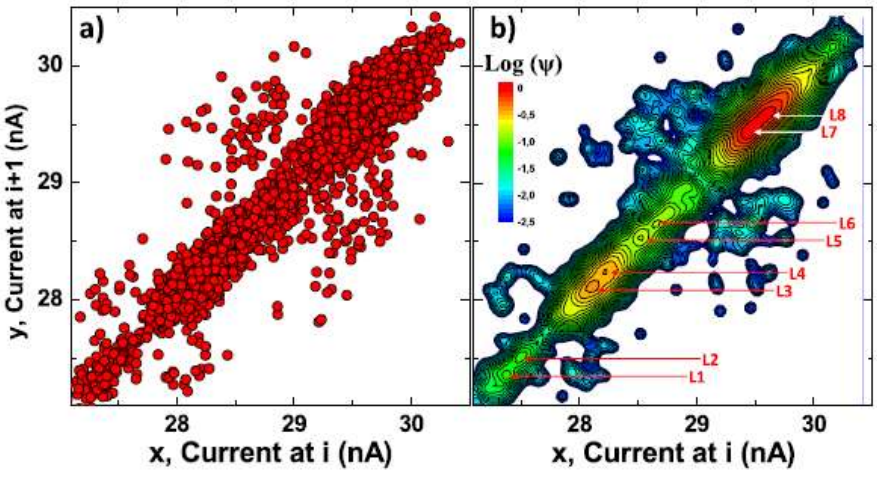

Figure 1.3: example of (a) Conventional TLP, (b) WTLP [45]

The calculation of the current shifts (η) has been performed as the following. For current traces where only one active defect was detected, the current shift (η) corresponds to the difference between the two appearing peaks. If the traces have two defects, the current shift of the first defect is calculated between the first and second peak and the second defect current shift is calculated between the first and third peak. For simplicity, during this validation devices with more than two defects were not taken into account in the calculation of the current shift η but were counted for the number of defects Ndef.

1.2.3 - Bias temperature instabilities

Bias temperature instabilities (BTI) is one of the most relevant sources of TDV in nowadays nanoscale semiconductor industry. This effect is triggered when a gate voltage is applied to the device under test, causing a shift on the Vth that recovers over time. BTI has two different nomenclatures depending on if it's affecting a nMOS transistor or a pMOS transistor. For nMOS, BTI is referred as positive BTI as it appears when the gate is positively biased, and the rest of the terminals are grounded. On the other hand, for pMOS, BTI is referred as negative BTI where the gate is negatively biased. This gate biasing causes charge to accumulate on the gate oxide insulator. This charges in turn change the Ids current on the transistor and, in the last instance, a change in the Vth.

After the BTI stress conditions are applied to a transistor, the parameters have shifted due to the accumulated charge, but after starting measurement-stress-measurement (MSM) tests, typically observed behavior of those parameters is tendency to recover towards the original nondegraded values. This is known as BTI relaxation or recovery, and it can take among several decades in measurement time. Fig. 1.4 shows an example Ids current trace of NBTI behavior after stress where it can be observed how the current goes back to the original current exponentially over time. Each of the discrete steps observed in fig. 1.4 correspond to one release of a negative trapped charges on the oxide of the transistor. For higher length devices (e.g., 1 μm) the recovery would appear as a smoother line as the contribution of each charge in the total current would be proportionally smaller.

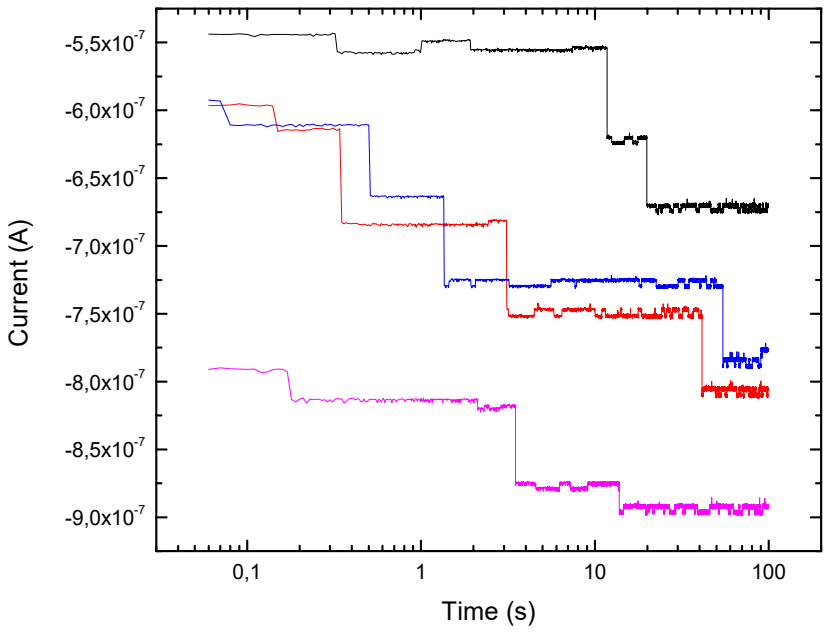

Figure 1.4: Example figure of BTI current traces over time.

BTI defects are considered to have the same origin as the RTN switching phenomenon. As both of these phenomena are heavily dependent on biasing conditions, the RTN effect appear when measuring at a constant bias while BTI appears when a gate stress is applied at a higher biasing conditions.

1.2.4 - Hot carrier Injection

The Hot carrier injection (HCI) is a degradation mechanism that consist of the alteration of the transistor operational parameters caused by the acceleration of carriers that travel through the channel with enough energy to break into the dielectric, creating permanent damage and altering the electrical properties of the device. [16,47]

HCI degradation can be considered a quasi-permanent change in the intrinsic parameters of a transistor device, such as Vth or the saturation current, etc. In nowadays highly scaled technologies, it's understood that the worst biasing conditions to observe HCI degradation are when Vgs=Vds, although in older technologies it was reported that HCI degradation was worse when Vgs=Vds/2 [48-50].

HCI is affected by temperature and frequency (if AC). It is accepted that HCI degradation is larger at lower temperatures but also AC degradation has been reported to be lower in comparison with the aging that appears when applying DC stress conditions [51].

To describe HCI degradation effects, the traditional Lucky Electron model (LEM) [52] based on direct electron excitation was widely accepted for long channel devices. As LEM postulates, the cause for HCI degradation involves defect generation by electrons (e−) or holes (h+) that breaks into the device interface thanks to the high electric lateral fields in the device.

Extrapolating this theory to nowadays nanometric devices, it can be expected that HCI degradation would almost disappear because electric fields are reduced due to low supply voltages. Nevertheless, recent literature shows that HCI degradation remains significant for ultra-scaled MOSFETs and therefore new models are needed. In contrast to the conventional field driven LEM, recent literature proposed novel energy-driven theories [53,54] to describe HCI phenomenon and accurately explain and model the mechanism of carrier induced degradation and to overcome with the limitation imposed by the traditional LEM [50, 53, 55].

1.2.5 - Aging phenomena Modeling

To achieve an accurate model that describes the effects of aging mechanisms such as BTI or HCI, several physical models have been proposed by the scientific community to predict the aging a device would suffer under nominal operation conditions from the accelerated aging degradation experiments. Some of those physical based models such as the Reaction-Diffusion model [56,57] were not suitable to completely describe the aging behavior in nanometer devices [58,59]. There is several newer models that describe the effects of BTI/HCI and RTN: the Two- Stage Model [60,61], the Two-energy-well model

[62], the Non-radiative two-stage Multi-Phonon (NMP) model [63] or the four-state NMP model [64]

Although some of the mentioned models provide an accurate representation of the aging effects, they typically need a high computational power and involve a high number of different physical parameters. In this context, defect-centric models such as capture/emission time map (CET) [65] or Probabilistic Defect Occupancy (PDO) model [66], which the characterization method that this thesis presents is based on, were presented as a more computationally efficient alternative when compared to other physical models because of their reduced number of parameters that those models need.

As the base for the proposed characterization method on this thesis, the PDO model will be described in the following section as it will be one of the main starting point of the proposed method later explained in Chapter 2 and expanded in Chapter 3.

1.2.6 - Probabilistic Defect occupancy model

The probabilistic defect occupancy model (PDO) [66] proposes a model to describe the trapping/detrapping of charge in/from single defects in a device. The main proposition of this model is that at any given time interval (Δt) the defect has a probability of being charged or not charged that depends on two uncorrelated parameters, the mean capture and emission times (τc and τe respectively). The magnitude of those parameters is dependent on temperature and bias. Using these parameters, this model allows the description of the evolution of drain current/Vth on RTN transient phenomenon and BTI and HCI aging phenomena and is the base of this thesis proposition. The capture and emission probabilities can be calculated by using the time parameters described earlier, being Pe=Δt/τe and Pc=Δt/τc. The value of Vth at a given time (t) can be described with the following equation 4:

$$\Delta Vth(t) = \sum_{j=1}^{Ndef} Ocj(t) \cdot \eta j \qquad (4)$$

Where Ndef is the number of defects, ηj is the Vth increase of the j-th defect, Ocj is 0 or 1 depending on the occupation state of a defect.

Some considerations, as the τc and τe are parameters extracted from a technology at a given temperature and experimental bias, each value of those parameters is very specific hardly extrapolated. The capture and emission times for RTN BTI and HCI can expand several orders of magnitude in time as commented in previous sections, this makes the evaluation of those parameters hardly covered experimentally. Under these constraints, the next section of this thesis will describe the measuring method used during most of this thesis experiments and one characterization method, weighted time lag plot(WTLP) that has been used during this thesis to validate the newly developed characterization method explained in Chapter 2.

1.3 - BTI/HCI aging Characterization.

Unlike RTN measurements, where a constant bias is applied to a device during a certain amount of time, when it comes to accelerated aging experiments, the implementation is not as simple. To obtain the parameter shifts occurring on a device due to the BTI/HCI effects the Measurement-Stress-Measurement (MSM) technique has been the most used methodology for device characterization. This technique consists of the concatenation of a pre-stress measurement period of the device under test drain current, followed by a stress time with higher-than-normal biasing conditions and finally another post-stress measurement period. The stress period, as mentioned in previous sections, serves the purpose of acceleration of the aging process of the studied devices. Usually an Ids-Vgs is measured pre and post stress to account for the device parameter degradation.

This MSM sequence can be repeated in sequence to obtain measurements of different degrees of degradation. Normally the stress time is increased each repetition, but the experimental conditions can be different depending on the specific research needs.

This type of measurement methodology has some caveats. It can suffer from loss of data as the aging mechanisms start to recover just after the stress removal [67,68]. To overcome this issue, several techniques have been proposed in the past like Ultra-Fast On-The-Fly (UF-OTF) [69,70], Ultra-fast MSM (UF-MSM)[71] among others.

All of the mentioned techniques have different shortcomings. Both MSM and UF-MSM suffer from recovery data loss due to the time required to compute the Ids-Vgs curve after each stress. In the case of UF-OTF, this technique assumes that all the degradation involves the Vth and does not take in to account the mobility degradation which can impact its accuracy. Finally, the OSDD characterizes the Ids-t at nominal operation biasing has been the most accurate when characterizing the step-like behavior that BTI or HCI present. But OSDD has the problem of loss of recovery data due to the time gap needed to change from stress to measurement at wafer level.

For those reasons, a measurement technique and coupled with both hardware and software to implement it was previously developed by this group, specifically in Javi Diaz phd thesis [72]. This methodology has been used to perform almost all the measurements presented in Chapter. 2 and 3 except the measurements involving FD-SOI devices.

On the following sections the measurement techniques, the devices used in this thesis, the experimental setup and the related control software will be described.

1.3.1 The Measurement-Stress-Measurement aging characterization methodology.

The Measurement-Stress-Measurement method (MSM) is the measurement methodology chosen during this thesis. It performs an initial Ids-Vgs to account for the nondegraded device characteristics followed by multiple stress-measure cycles executed sequentially to account for the accelerated device aging parameters shifts. The after-stress measurements consist of an Id vs time of varying length to measure the current/Vth

relaxation followed by an Ids-Vgs to account for the degraded parameters after the relaxation period measurement.

To obtain reliable characterization results, it is assumed that the time gap between switching from stress to measurement should be characterizable and as short as possible to not lose any critical information during the measurements. It is also assumed that the characteristics of one device measurement are the same as the next device and the process is precisely controlled. This would avoid an unnecessary complex data post-processing and standardize data acquisition.

Although using this method would provide accurate and standardized data collection, it still holds the main problem of the stress characterization experiments, time. As the studied effects like BTI or HCI have a stochastic nature the need to perform the same experiments to a high number of devices is necessary. For example, if a similar experiment to the once performed during this thesis consisting of a 100-device experiment that have MSM cycles with 1,10,100,1000 s stress and 50 s measurements and a 5 s Ids-Vgs, without taking in to account any extra processing times on the set-up/software side, the experimental time becomes around 32.39 h.

To reduce this infeasibly long experimental times, the next sections will describe the experimental setup necessary to implement a parallelization of the stress phases of the MSM technique and its main advantages thanks to the help of an array-based IC solution. Secondly, the characteristics of the method that this thesis is based on, described on chapter 2, will open the opportunity to greatly reduce the measurement times on both RTN and aging experiments.

1.4 - Array-based IC: ENDURANCE chip

The ENDURANCE IC consists in a full-custom array-based IC fabricated in a commercial 1.2V 65-nm CMOS technology, image in Fig 1.5. This IC integrates all the required capabilities for an accurate characterization of the most relevant variability effects required by this thesis: RTN, BTI and HCI in a single chipset, including the parallelization of aging experiments, the accurate biasing and measurements utilizing force-sense set-ups and others. This chip was designed and fabricated by Javi Diaz, the predecessor on this project line in our investigation group, Reliability on Electronic Devices and Circuits (REDEC).

This thesis will take advantage of the capabilities of this chip in order to implement a new characterization methodology that will reduce experimental times when compared to on-wafer traditional characterization and will aim to the characterization of a high number of devices and experimental conditions that would have been impossible otherwise.

In this section the principal characteristics and considerations regarding the ENDURANCE chip will be described.

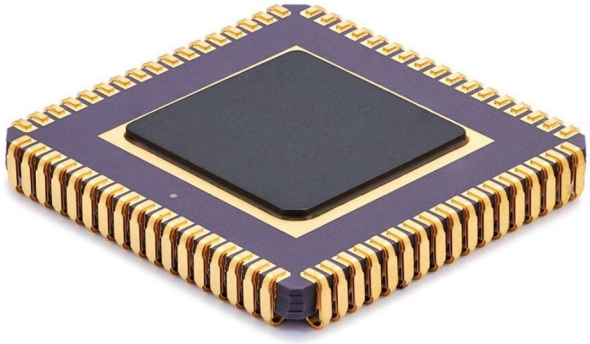

Figure 1.5: The ENDURANCE IC chip encapsulated in a JLCC68 package.

This chip was designed with three main key considerations to overcome testing limitations of previous IC designs and on-wafer testing restrictions:

- The ENDURANCE CHIP is a highly robust IC as it was specifically designed to withstand high stress voltages experiments.

- To mitigate the voltage drops between the chip terminals and the DUT terminals during characterization, the ENDURANCE chip is equipped with Force-&-Sense paths to sense the DUT voltages and adjust the external forced voltages in accordance.

- A circuit design tailored for the characterization of variability phenomena with enough versatility to carry out parallel stress testing algorithms to greatly reduce the aging testing time.

The basic architecture of the ENDURANCE chip can be described as the following. The chip is divided in a set of fundamental blocks to facilitate understanding of the overall IC circuit design, shown in Fig. 1.6. The devices under test (DUTs) of the IC are divided in two main matrices, one for nMOS transistors and one for pMOS transistors. Each of those matrices is divided between 2 submatrices with the “left” and “right” designations, each containing a 56 rows x 14 columns array of DUTs, making it a total of 784 devices per submatrix or a total of 3136 devices per chip.

The chip allows the user to test one of the submatrices at a time and has individual access to each of the DUT. All the devices in the left submatrices and the majority of the devices in this chip (1376 for both pMOS and nMOS) have the same size, being W/L=80/60nm, that will be the devices used during this thesis. The rest of the devices have a combination of devices with sizes W/L= 200/60,600/60, 800/60, 1000/60, 1000/100, 1000/500, 1000/1000 but will not be utilized during this thesis.

The individual access to each DUT is achieved using their individual unit cell (fig. 1.6) with two row and column twin decoders as shown in fig. 1.7 Using the control block, the unit cell can be programed between 4 different modes:

- Measurement mode: DUTs measurement under nominal conditions, from 0 V to 1.2 V
- Stress mode: High biasing mode, from 1.2V to 3.3V
- Standby mode: DUT’s at zero bias. Vds=Vgs=0

- Off mode: Terminals disconnection.

The different modes allow the connection of the DUT to the different biasing paths inside the chip. The precise timing of the described operation modes allows the execution of user-defined serial or parallel stress experiments.

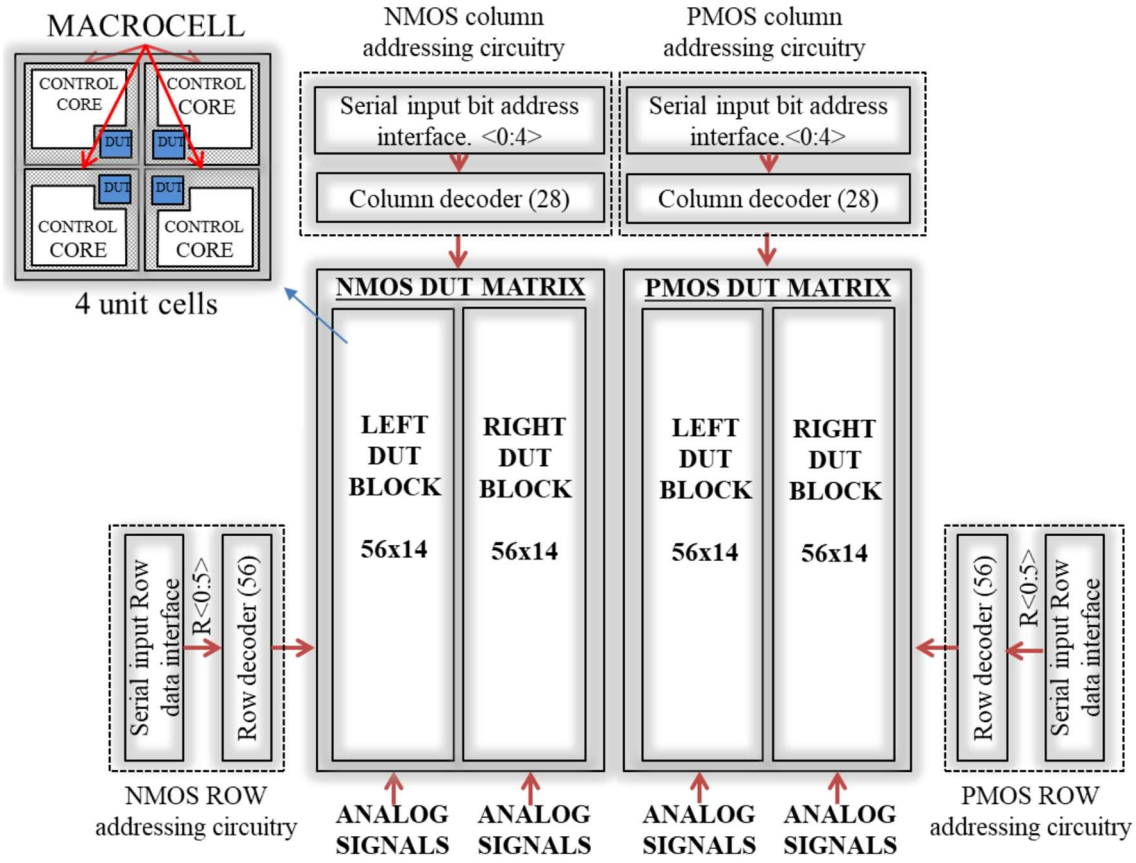

Figure 1.6: ENDURANCE IC fundamental building blocks.

Figure 1.8 summarized the schematic of the DUTs connections in each matrix. Different operation modes can be programed to stablish parallel connection between drain and gate DUT terminals using the control cores (CC), the transmition gates and the biasing paths. Under these pretexts, the control units can allow the connection of multiple DUTs to the same biasing paths at the same time, mostly stress and standby as having the measurement connected to more than one device at the same time would make little sense. For the explained reasons, during an aging experiment multiple DUTs can be under stress at the same time, ergo parallelizing the stress.

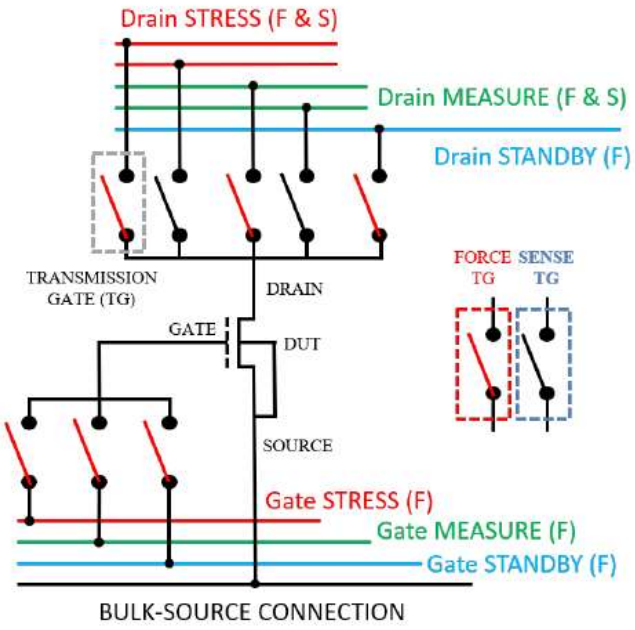

Figure 1.7: Unit cell individual Drain and Gate connections.

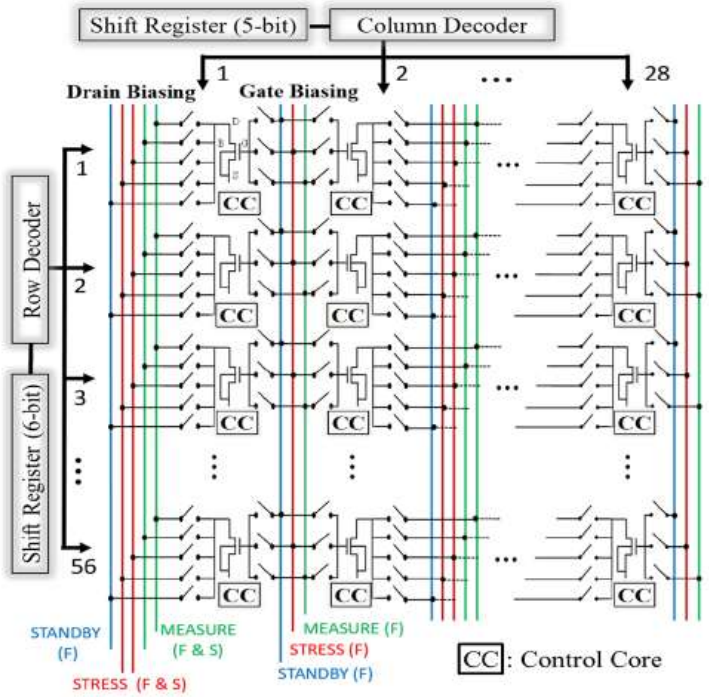

Figure 1.8: Schematic illustration of the unit cell distribution (28 columns and 56 rows) inside an nMOS or pMOS DUT matrix of the ENDURANCE IC chip.

Under these considerations, the ENDURANCE chip has been used during this thesis to statistically characterize TDV phenomena with high accuracy and to perform a high number of experiments with a variety of experimental conditions. The full experimental setup and the control software used during this thesis will be presented on the following 1.6 section.

1.5 – Aging parallelization hardware system

In order to achieve a reliable transistor characterization, the first step is having an accurate and reliable hardware setup. Fig 1.9 shows a schematic of the experimental setup used during the characterization of the devices in the ENDURANCE chip transistor devices during this thesis.

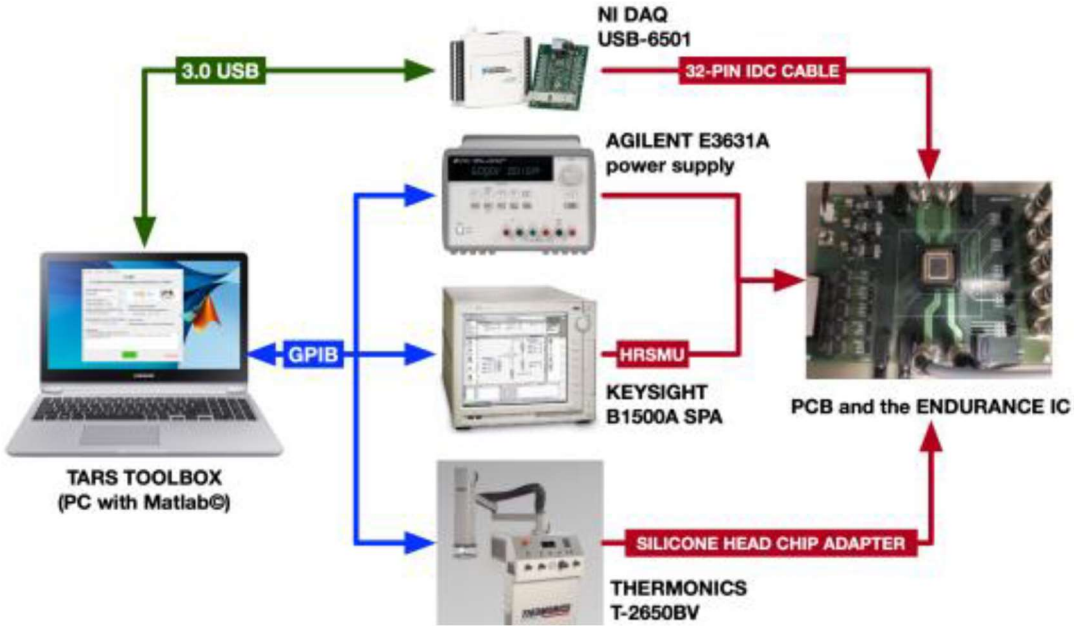

Figure 1.9. Original Experimental setup used to automate the characterization of the 784 pMOS transistors with W/L=80nm/60nm from the chip ENDURANCE. [72]

The original hardware setup has de following equipment:

- Main control unit: A Computer equipped with Matlab® software where the TARS toolbox software (descrived in the next section) is executed.
- Data acquisition: A USB Digital Adquisition System (DAQ) model USB-6501 from National Instruments, equipped with 24 digital IO channels [73].
- Power supply: The Agilent E3631A power supply for PCB biasing using a 5V/1A DC output voltage [74]
- Measuring tool: The Keysight Semiconductor Parameter Analyzer (SPA) model B1500A. This equipment has Force & Sense capabilities for precise biasing and low current measurement [75]
- Temperature control: Although not used during this thesis, a T-2650BV Thermonics temperature system capable of controlling the chip temperature [76].
- Device under test connections: A custom printed circuit board (PCB), where the ENDURANCE chip is inserted using a Zero insertion force socket model JLCC68.

The original hardware setup described is located in the Instituto de Microelectrónica de Sevilla, where the initial experiments to the ENDURANCE chip were performed. Soon after the start of this thesis, an adaptation of the set-up to the Universitat Autonoma de

Barcelona equipment was prepared. The substituted parts from the original setup that have been used in UAB are the following:

- Agilent 4156C Precision Semiconductor Parameter Analyzer as the measurement equipment [77].
- Keithley 2230 as the power supply [78].
- The temperature regulator available on the original set-up was not implemented in the new set-up as no temperature dependance measurements were designed on the duration of this thesis.

The major caveat that this new set-up has is the lower temporal resolution on the measurements (from 2 ms to 10 ms) although this fact will not impact the implementation of the proposed characterization method in chapter 2.

1.5.1 - TARS Control Software and user interface.

The TARS control software was designed as a tool to control all the hardware involved in the characterization of the devices on the ENDURANCE chip. The software was programed using Matlab®. This software with a user-friendly GUI allows the user to define the massive of I-V, RTN or aging tests while maintaining synchronization between all hardware devices, the predicted experimental timeline and the TARS software. As this software was not designed during this thesis, a summarized description will be provided referencing the Javi Diaz Thesis project [72] where the creation of this software was developed. The fig. 1.10 shows the main TARS software GUI window.

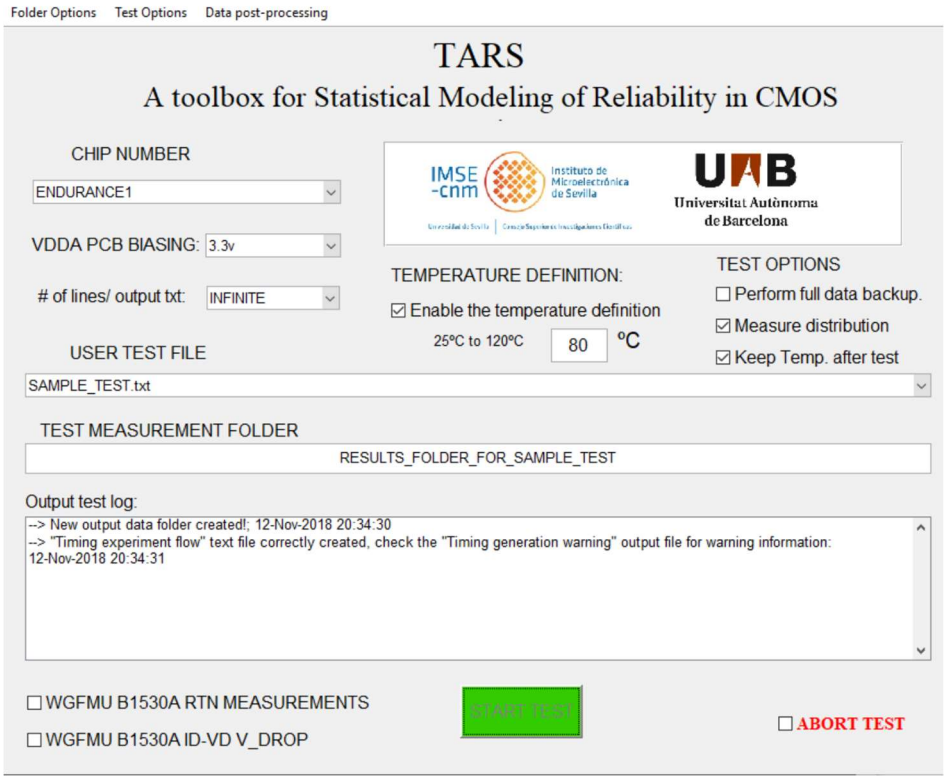

Figure 1.10: The TARS main test setup and monitoring GUI.

This interface allows the user to select between many options: Chip under test number, analog voltage biasing, temperature definition, test file selection, test measurement folder definition and other more specific options. Also in the presented interface the output test log can be seen, showing the test progress over time or any error during the experiments.

On the test options tab, an extra window can be selected in order to generate the test file that will be used by the software to perform the defined experiment (fig. 1.11). In this GUI the user can define which transistors are under test and all the experimental parameters necessary to perform the tests. The TARS software autogenerates the test file and uses an All DUT Parallel Stress Pipeline (ADPSP) algorithm [72] to define each experimental steps and its timing synchronization.

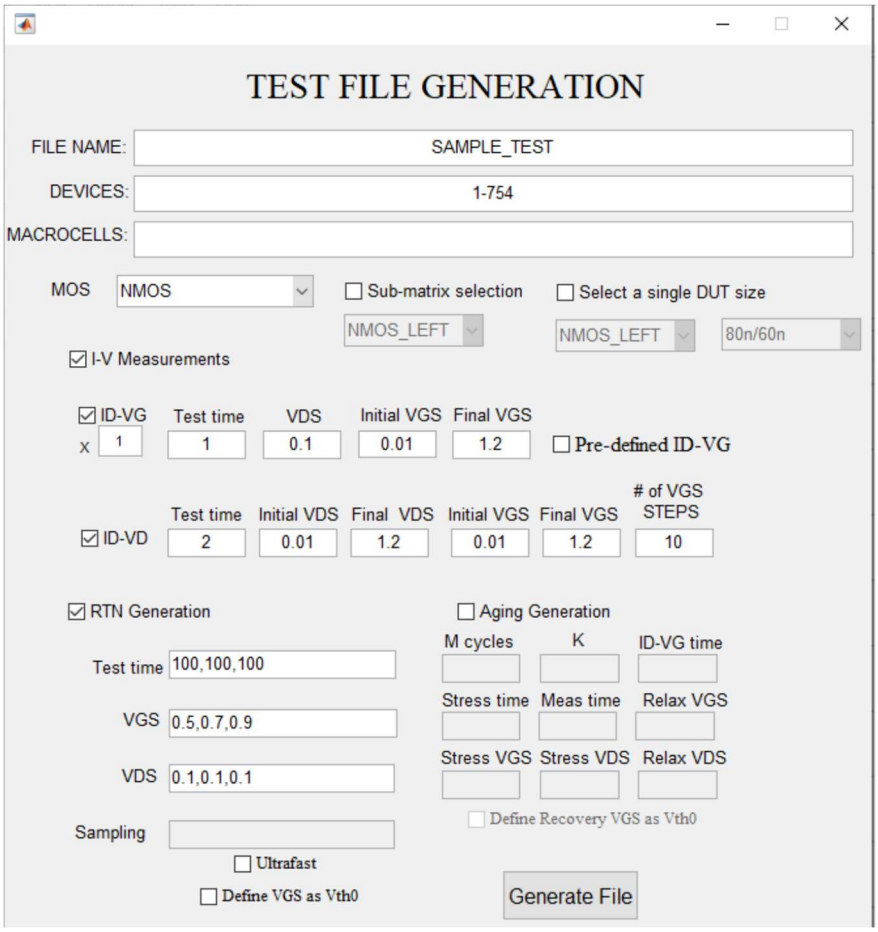

Figure 1.11: The Test File Generation GUI of the TARS toolbox.

The software also allows a simple visualization of the results, but the analysis of the resulting data has been performed using the output data files and not the data post-processing GUI present in the TARS software.

1.5.2 – Stress Parallelization.

One of the main problems, if the number of devices under test and the experimental time per device is high, is the necessary experimental time becomes unfeasibly long. For this reason, with the help of the ENDURANCE Chip, the control software and the

experimental set-up described in the following sections, the parallelization of the stress periods of an MSM aging characterization methodology can be achieved.

Unlike the traditional methodologies where one device is measured or stressed at a time (Fig. 1.12) the parallelization of the stress periods consists of stressing each device under test at the same time while the measurements on each device are going on (fig. 1.13). Although this process seems simple when observing the example on figure 1.13, when the number of devices is higher, stand-by periods need to be implemented as no more than 1 device can be measuring at the same time and the devices need to be measured immediately after the stress period if a good aging characterization is to be performed. Although the calculations of the stand-by periods can be done manually, an optimization algorithm to calculate the experimental timeline have been implemented on the software, as mentioned in section 1.5.1

The advantages of the stress parallelization can be easily deduced from observing the examples on figures 1.12 and 1.13, but simple calculations can be made in order to characterize the time saving using the parallelization methodology. Considering Tp as the total process time, Ts being the stress time and Tm being the measurement time, for a traditional MSM measurements the total procedure time would be Tp= (2Tm+Ts)·Ndev, where Ndev is the number of devices under test, exemplified in Fig. 1.12 . On the other hand, when parallelizing the stress time the total procedure time would become Tp=Tm·(Ndev+1) +Ts, exemplified in Fig.1.13.

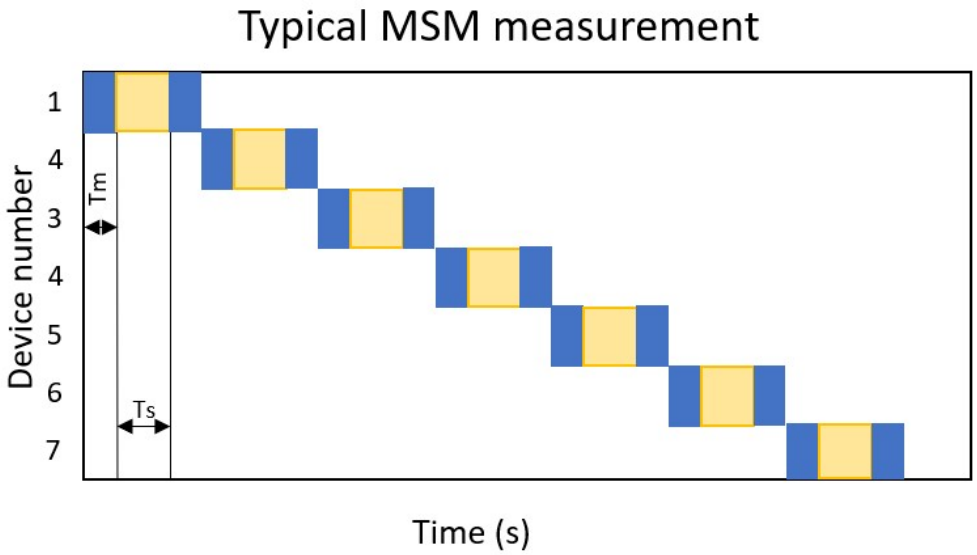

Figure 1.12: Schematic of a typical MSM measurement exemplified for 7 devices. Blue representing measurement time, yellow representing stress time. The total experimental (Tp) time would become Tp=(2Tm+Ts)·Ndev.

As a numerical example, an aging experiment applied to Ndev=100 device and a measurement time of Tm=50s will be applied with a simple MSM of 1000s of stress time (Ts). The traditional MSM measurement total procedure time would become Tp=(2·50s+1000s)·100=20000s→30.5 h. On the other hand, the parallelized version of this same aging procedure would become Tp= 50·(100+1)+1000=5070s →1.7h. Taking in to account that this is a simple MSM calculation without any extra stress-measure cycles, the time reduction on the performed experiments could become higher the longer the experiment or the higher the number of devices under test.

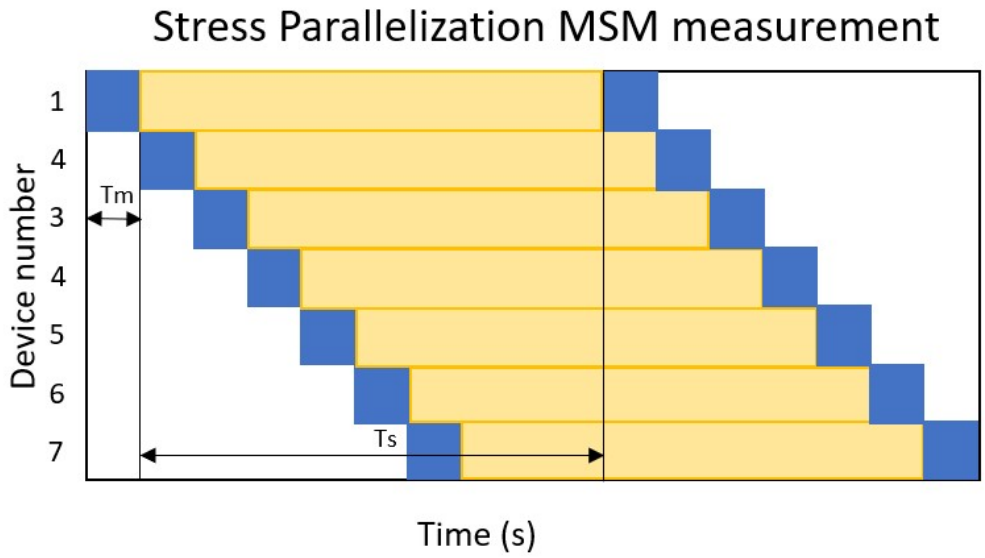

Figure 1.13: Schematic of a parallelized MSM measurement exemplified for 7 devices. Blue representing measurement time, yellow representing stress time. The total experimental (Tp) time would become Tp=Tm (Ndev+1) + Ts.

Under this premise, the following section will describe the array-based IC solution and the experimental setup that have been used during this thesis and allowed the stress parallelization of the performed aging experiments.

1.6 – Contributions of this Thesis

The main goal of this thesis is to contribute in both the understanding of the studied variability phenomena at a device level and designing new tools that allow a faster characterization and shorter experimental times. As the industry technology nodes become smaller and smaller, the variability effects will become the main cause of failure on highly scaled devices. For this reason it is imperative to perform fast and reliable device characterization and provide accurate model parameters for the main variability phenomena from an statistic point of view.

To achieve this goals, firstly the development of a characterization method that will allow to perform fast and reliable variability test without the need to design experiments that would last unfeasibly long times.

The second major contribution of this thesis is the design and execution of wide variety of transistor characterization experiments with a plethora of biasing conditions that range from low voltages designed for RTN characterization, high gate stress designed for BTI, a wide combination of gate and drain stress to accommodate the ranges involving both BTI and HCI and also low voltage RTN characterization with a extensively long experimental time. All the mentioned experiments have been characterized and analyzed with the help of the presented method and will contribute to the understanding of those effects in the scientific community.

Since the time-dependent variability is and will continue to be one of the most important reliability effects on the next decade, any methodology that will enables an increased

number of fast and quality characterization of the involved effects will help the industry have the necessary data to counteract or reduce the detrimental effects that all the variability sources can cause.

Chapter 2

Proposed Characterization method.

For a long time, the characterization of charge trapping/detrapping on transistor devices has provided highly valuable information about its reliability and aging behavior [79]. For this reason, many different methods have been proposed in the literature to analyze the defects in RTN, BTI and HCI [14-17]. All of the presented methods rely on the full analysis of current traces Ids vs time for RTN, BTI and HCI or the characterization of Ids-Vgs before and after stress for aging mechanisms. As all those TDV mechanisms have a stochastic nature, the characterization of those effects needs to be performed to a high number of devices, this way the extracted statistical parameters are reliable and accurate for the studied devices. For these reason, the experimental time necessary to characterize TDV effects for a high number of devices and during a sufficiently long traces to account for all the available defects becomes extremely long.

Under this pretext, this thesis has been dedicated to developing, validation and use of a newly developed characterization method. This new characterization method is based in the statistical reproduction of the experimental current difference between two sufficiently separated instances of time using the defining statistical parameters that describe RTN, BTI and HCI defects.

Regarding this chapter, firstly, a traditional method calculation using WTLP described in chapter 1 section 1.2.2 will be used to characterize RTN measurements. After the WTLP characterization, an in-depth description of the proposed characterization method followed with the characterization of the same RTN measurements in order to validate the proposed method. Finally, a description of a mathematical analysis and the main advantages over traditional characterization methods respectively will be presented.

2.1 – Traditional RTN characterization: WTLP

The proposed characterization method described in the following section is a newly developed characterization method, as a result it needed to be validated. For this reason, a set of RTN focused experiments using the ENDURANCE chip [72] has been performed.

As a point of reference for the proposed method results, the traditional characterization method WTLP was used to obtain the baseline defining parameter statistical distributions to later compare the results with the proposed method. The weighted time lag plot (WTLP) presented in section 1.2.2, is a characterization method based on a conventional RTN characterization that obtains the information from the full analysis of each individual ID trace. The second one being the proposed method that is the center point of this chapter.

2.1.1 – RTN Experiments:

A set of 784 pMOS devices has been used during these section experiments. As described in chapter 1, 784 devices is the maximum number of devices that the ENDURANCE chip allows for single procedure experiment.

These experiments involved measuring the drain current of those 784 devices during 40 s with the measuring conditions being the gate bias (VGS) at 0.5 V and the drain bias (VDS) being 0.1 V. The equipment time sampling resolution is 2 ms. Figure 2.1 shows some examples of the drain current measurements for some devices. All of them show some form of RTN behavior with a variety of different capture and emission times, number of levels and current shifts. In order to better visualize the RTN behavior only 10 s of the 40 s measurements are shown in the figure 2.1.

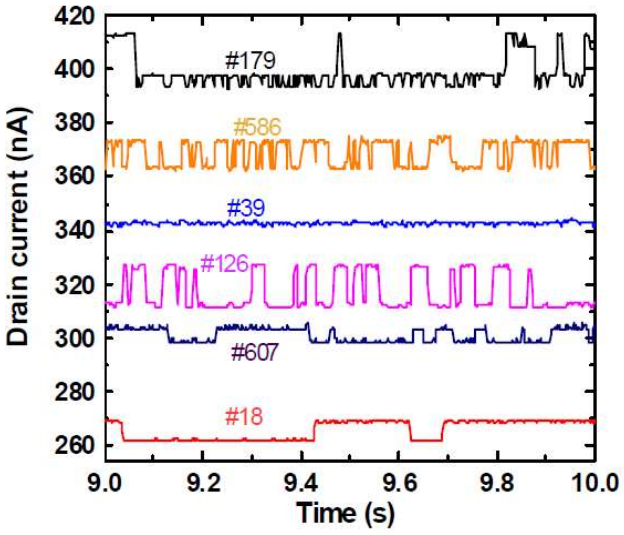

Figure 2.1: Some representative shots of the ID traces obtained in a set of 784 pMOS transistors with W/L = 80nm/60nm (VGS = 0.5V and VDS = 100mV). The drain current (ID) was registered during 40s, with a sampling time of 2ms. Some traces show RTN. To better visualize the associated current levels, only 10s out of the 40s long waveforms is shown.

As the proposed characterization method, several studies have been performed in order to validate the method usability and its characteristics. The following sections will present the comparison between the full trace analysis with WTLP, and the results obtained with

the proposed characterization method. After the comparison, the limit ranges of the method have been tested and analyzed, for example the number of devices to be statistically significant.

2.1.2 – WTLP parameter distributions.

This section will describe the results obtained using the WTLP characterization method using the Id traces described in the previous section. WTLP method have been explained in chapter 1. As an example of the results obtained using WTLP for one of the studied devices, Figure 2.2 top image show the WTLP plot applied to the #179 trace from figure 2.1. Figure 2.2 bottom show the corresponding WTLP diagonal showing 4 differentiated levels, making the number of active defects on this device 2. The WTLP was applied to all 784 devices and the number of defects, and their current shifts were calculated. These results were used to calculate the Ndef and η statistical distributions whose probability density functions are plotted in Figure 2.3(symbols).

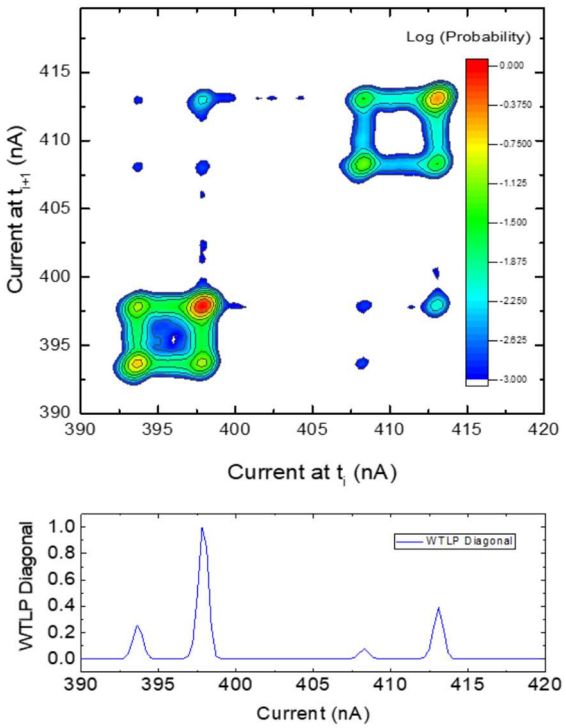

Figure 2.2: (top) Example of the WTL plot used to characterize the ID traces. The complete Trace #179 in Fig. 2.1 was considered for this example. (bottom) From the peaks across the plot diagonal (x = y) the number of defects, NDef, and their impact in the drain current, η, can be estimated.

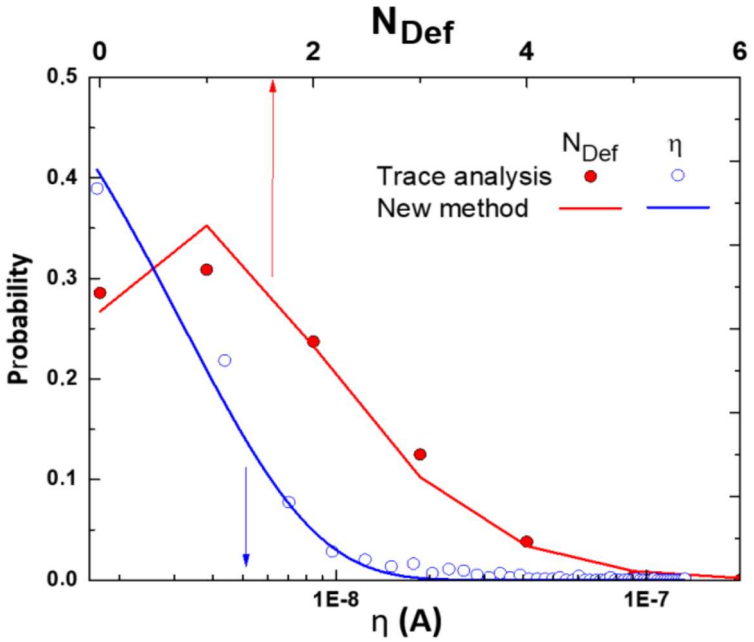

Figure 2.3: NDef and η distributions obtained from the analysis of the complete set of 784 ID traces using the WLTP method (symbols). Red and blue lines correspond to Poisson and exponential distributions obtained with the mean parameters (<Ndef_min> = 1.37 and <ηdevmin > = 3.8 nA) derived from our method. Note the good fitting of the experimental data.

2.2 – Basic principles and description of the proposed method

In this section the basic principles of the newly developed characterization method will be described, followed by the explanation of how it has been implemented and the chosen fitting procedures utilized during this thesis.

To begin with, the proposed method has been applied to RTN characterization. The proposed method aims to describe the drain currents behavior (or threshold voltages) between two given instants t1 and t2 using the RTN statistical parameters. When the difference between the simulated and experimental sets of current differences match the most, the used simulation parameters would be the best fitting the experimental device characteristics. From those parameters, the current difference between t1 and t2 can be expressed as: ΔIDsim = IDsim(t2) – IDsim(t1) for each simulated device, where ID is the drain current. In order to obtain the best fitting parameters that describe the current shift distribution to the experimental results, a Montecarlo simulation has been the chosen method. The input statistical parameters are randomized and iterated on to obtain the parameters that best reproduces the experimental data.

This first iteration of the method started by considering only RTN phenomena, so the ΔID will depend on the occupancy states of the RTN defects and their corresponding current values (η). On Chapter 3, an expansion of the method to include aging effects will be presented.

This is illustrated in Fig. 2.4 where two schematic RTN traces are represented and the times t1 and t2 are indicated. As an example, trace #1 and #2 have only one active defect, which in #1 is at the same occupancy state at t1 and t2. Therefore, in this case ΔID#1 =

0. On the other hand, trace #2 occupancy states are different at t1 and t2. Consequently, the current difference measured at both times corresponds to the shift caused by the capture/emission of charge in this defect and its value is ΔID#2 = η. In more complex RTN traces, where more than one defect can be active, ΔID can be a combination of the different η values of each of the defects on that device depending on their occupancy states.

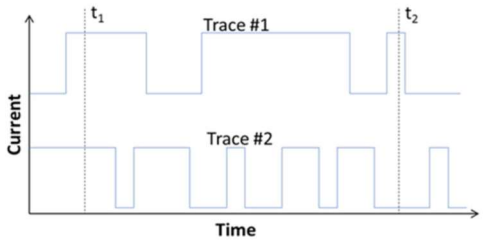

Figure 2.4: Schematic waveforms to illustrate the new method used to characterize RTN in a large number of devices. To apply this method the current at only two instants is required.

Using the experimental traces (example in fig 2.1), a set of ΔID can be extracted for each set of studied devices. Originally, the method used histograms (probability density function, PDF) of the ΔID to compare between the simulated and the experimental results, but the method was changed to a Cumulative Density Function (CDF). This change improved the accuracy of the method when compared to using PDF as the results showed that the experimental and simulated data matched more closely, and also the PDF variant showed higher parameter variance.

The fig. 2.5 shows the corresponding CDF (and the PDF on the top corner for comparison). Most of the values of ΔID of these devices can be observed fall closer to 0. This can be associated to the cases where either there is no active defect in the specific device or the defects on that device are at the same occupancy state at t1 and t2. The small variations on the near 0 values are related to the background noise of the measurement system. On the other hand, the tail ends of the ΔID CDF are indicative of an ID shift of the active defects in the evaluated time interval and can be a consequence of the occupancy of one or more defects has changed.

In more detail, the proposed method has the following simulation pipeline. Firstly, a set of simulated ΔID values would be created, namely ΔIDmth, following the known statistical rules that govern the charge capture effects in deeply scaled MOSFETs [80]. The main input parameters to consider are the number of defects (Ndef) distribution represented with a Poisson distribution and the second one is the current shift (η) that those defects generate, represented with an exponential distribution. The flow diagram for the generation of one ΔIDmth value is illustrated in the diagram of Fig. 2.6. The method starts an iteration with the generation random mean number of defects <NDef_mth> and a random mean current shift <ηmth> within the designated ranges (due to the Montecarlo fitting method). Using the mentioned Poisson distributions and the <Ndef_mth> parameter, a defect number (NDef_mth) is assigned to each individual simulated device. Next, from the exponential <ηmth> distribution a random current shift is generated for each one of the device's NDef_mth defects, which represents the associated current shift value η of those defects.

Once the defects and its current shift are assigned, the occupation of those defects at the two instants of time is calculated. The probability that one defect is occupied, Pocc, is assumed to be uniformly distributed [66]. This assumption is originated from the premise that firstly, as the time difference between t1 and t2 is large enough, the probability of a defect to be on each state will depend only on the ratio between capture and emission times, and as presented in the introductory chapter 1, if the devices under test sample set is big enough the capture and emission times statistical distribution mean value would be 0.5. For these reasons, a probability of occupation Pocc between 0 and 1 is randomly generated and assigned to each defect. Finally, using this probability Pocc, the occupancy state oc (0 or 1) of each defect at t1 and t2 and the difference between both times comparing oc(t1) and oc(t2) is calculated. This makes the simulated ΔID possible values for each defect be ηmth, 0 or -ηmth. With all these considerations, the ΔIDmth for each device can be described with the following equation 1:

$$\Delta I_{D_{mth}} = [\sum_{i=1}^{i=N_{Def\_mt}} \eta_{mth,i}(oc_i(t2) - oc_i(t1))] + randn(\sigma); \qquad (5)$$

where NDef_mth is the number of defects resulting from the Poisson random number generator, ηmth,i is the corresponding η value of the i-th defect, and oci represents the occupancy of the i-th defect and is 0 if the defect appears at low current state and 1 if the defect appears at high current state. Finally, randn(σ) is a Gaussian distributed number with mean value 0 and standard deviation σ, included to account for the background noise in the measurement system.

This process is repeated to create the ΔID_mth for each virtual device. For a pair of input parameters <NDef_mth> and <ηmth> a new simulated CDF is created. This virtual CDF will then be compared with the experimental CDF. The resulting error value between experimental and simulated is created for that set of <NDef_mth> and <ηmth> which is stored.

As a Montecarlo simulation was chosen as the fitting procedure, the described process is is repeated a large number of times, 5000 iterations specifically in the case of this thesis experiments, with new randomized sets of <NDef_mth> and <ηmth> to reach for which pair of <NDef_mth> and <ηmth> the error between the experimental and the simulated CDF is minimum, which would be the best fitting parameters to the experimental results.

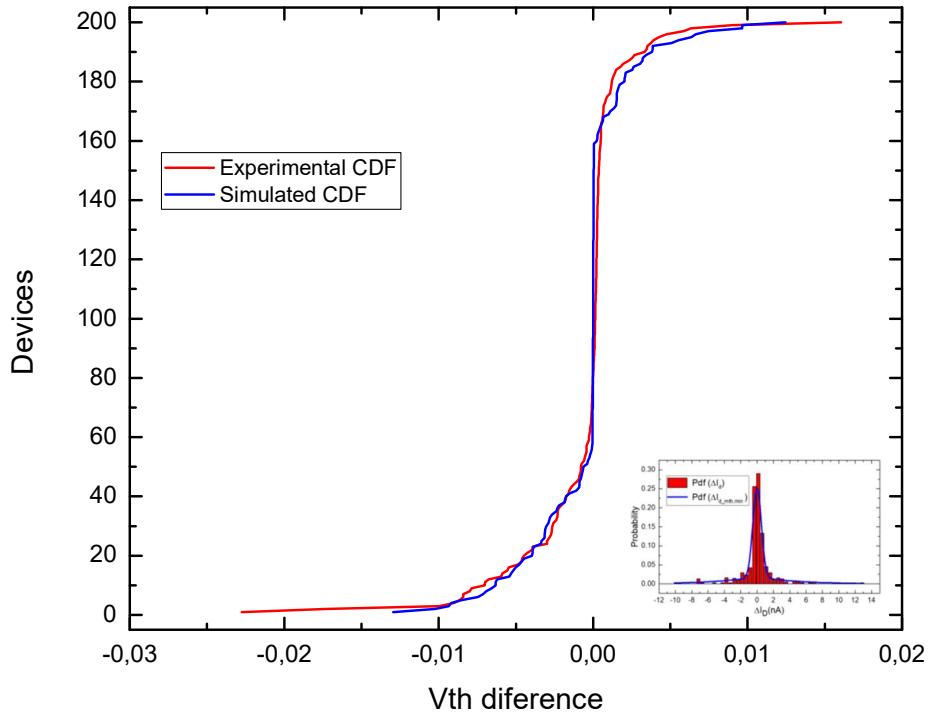

Figure 2.5: Example of 2 CDFs, one experimental(red) and one simulated (blue). On the small graph it shows another example in this case, the first iteration involving PDFs instead of CDFs.

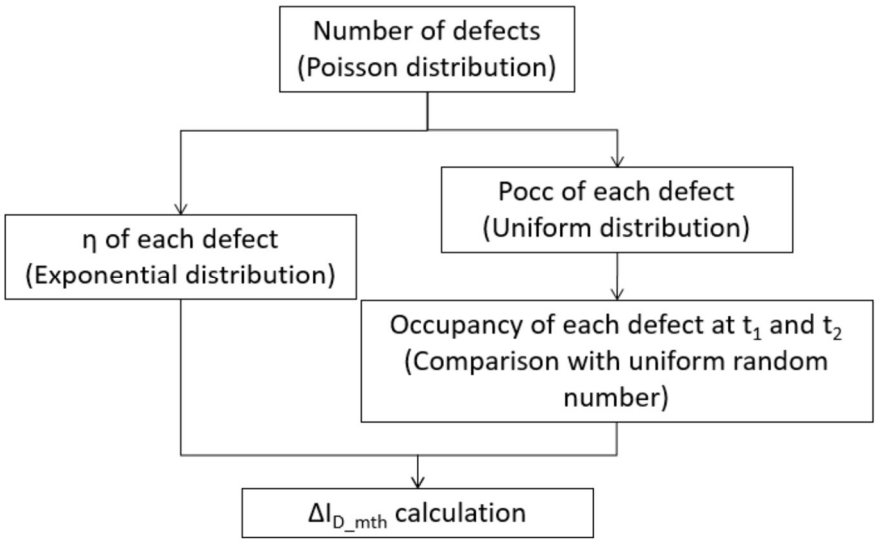

Figure 2.6: Flow diagram of the procedure designed to generate one ΔID_mth value for each of the simulated devices.

To find the minimum error parameters, an error map can be created as a function of <NDef_mth> and <ηmth>, and using the error values a fitted surfaces can be created, example shown in Fig 2.7. The resulting error map in fig. 2.7 shows a minimum located in this case at <NDef_mth,min> = 1.37 and <ηmth,min> = 3.8nA.

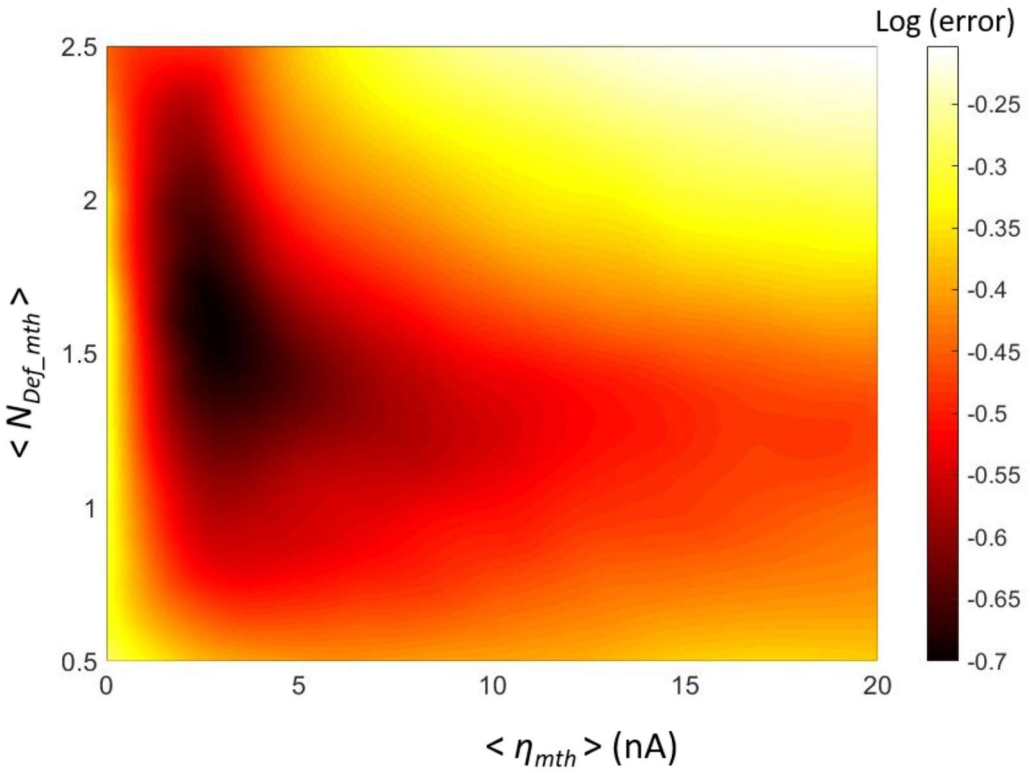

Figure 2.7: Error function ΔID -ΔID_mth resulting from our method (z depending on the <NDef_mth> and <ηmth> that respectively represent the mean number of defects in a device and the mean current shift caused by the trapping/detrapping of the defects.

With the minimum error parameters, the corresponding ΔID_mth distribution is shown in Fig. 2.3 (blue line). It can be seen in Fig. 2.3 that it correctly describes the experimental ΔID CDF, making the extracted minimum error parameters the correct representation of the studied devices properties.

Although both methods arrived at very similar statistical parameters, the computational time used by the WTLP method to analyze all the RTN traces starts at the order of several hours, while the application of the proposed characterization method does not last more than 30 minutes depending on the specific simulation specifications.

More importantly, when comparing the WTLP analysis shown in Figure 2.3 (Symbols) and the resulting distributions from the extracted parameters using the proposed method (Lines) it can be concluded that both of them match almost perfectly, taking in to account the stochastic nature of the studied phenomenon. The resulting parameters extracted with the proposed method are the following: the mean number of defects <Ndef_min> = 1.37 and the mean current shift being <η>= 3.8 nA. This result indicates that the statistical distribution of NDef and η can be obtained by measuring only two points of the ID traces separated by a time interval t2-t1. Consequently, the ID measurement can be parallelized, making a considerable reduction on the total measurement time. This concept will be expanded on the following section, supported with some mathematical calculations.

2.3 – Measurement Parallelization:

Due to the characteristics of the proposed characterization method, measurements that would have been unfeasibly long can have a highly reduced experimental time. The main reason for this reduction is that the proposed method it gives the user the option to parallelize the measurements when performing RTN measurements due to the characteristics that the proposed method has. As the proposed characterization method doesn't need the full analysis of ID-t traces but instead only needs measures at instance t1 and t2, all the measurement time between t1 and t2 that our equipment would have been measuring a single device and obtaining a full current trace can be spend on measuring the rest of the t1 and t2 on the other devices under test.

On a more mathematical approach, considering the parallelization for an RTN measurement if we had a number of devices (Ndev) with a measurement time (Tm) and minimum measurement time (t) for the traditional approach, the non-parallelized experiment procedure time (Tp) would become: $Tp = Ndev \cdot (Tm)$. The schematic of this example is shown on Fig 2.8 for seven devices. On the other hand, utilizing the parallelization on our RTN measurements to be used with the proposed method, the stress on our devices would make the resulting time: $Tp = Tm + Ndev \cdot t$. Schematic shown in Fig 2.9.

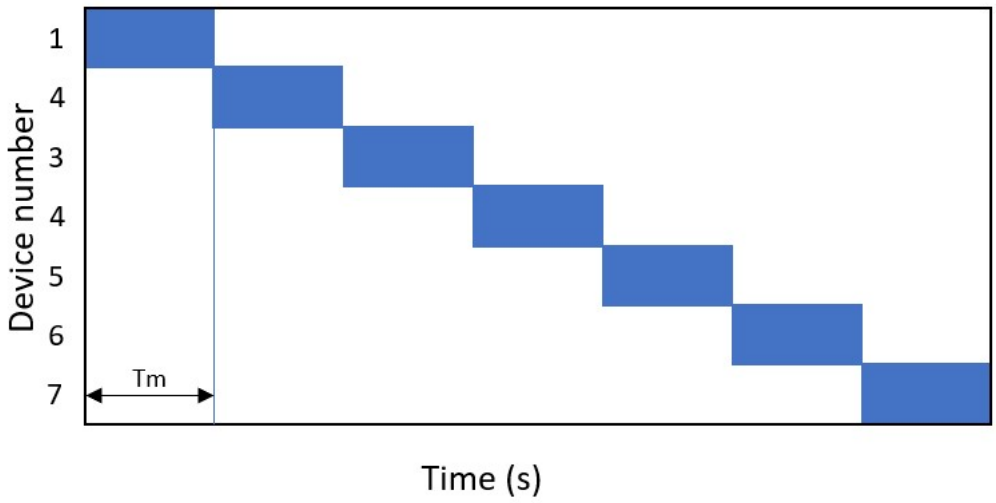

Figure 2.8: Schematic of a traditional RTN measurement exemplified for 7 devices. Blue representing measurement time. The total experimental (Tp) time would become Tp=Ndev·tm.

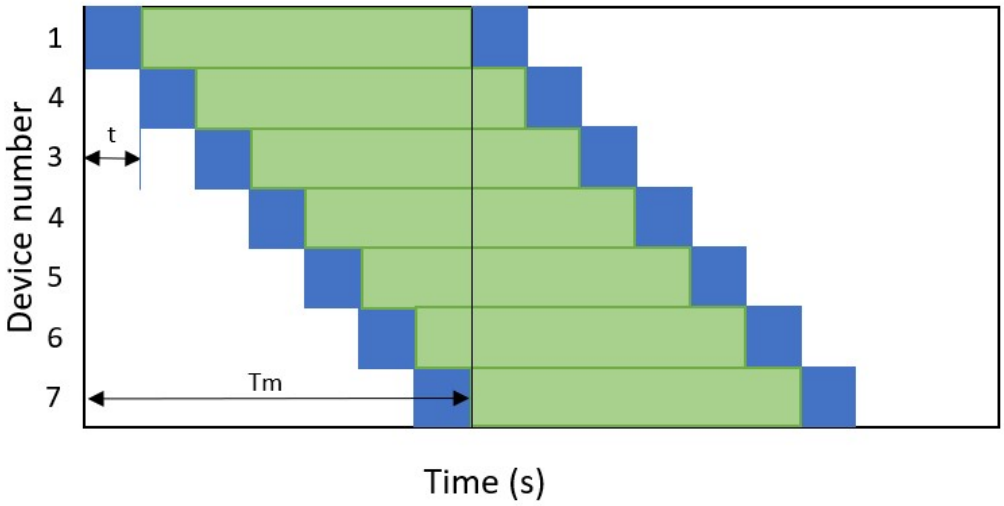

Figure 2.9: Schematic of a RTN measurement to be used with the proposed method, exemplified for 7 devices. Blue representing measurement time, green representing non measuring but applying the same biasing conditions. The total experimental (Tp) time would become Tp=Tm+Ndev·t.

As a numerical example, the following calculations for each case (RTN and aging) are presented.

For the RTN case, a set of 100 devices with a measurement of 50s RTN trace will be calculated with a minimum measurement time t=0.01s. On the typical RTN measurement the total procedure time would be Tp= 100·50s=5000s → 1.38 h. On the other hand, for the proposed method RTN experiment, the total procedure time would be Tp= 50s+100·0.01s = 51s. The experimental time goes from 1.38h to 51s in this example.

With the presented schematics and calculations, this newly developed characterization method has been demonstrated to allow the user to greatly reduce the experimental times for RTN experiments with large number of devices under test and/or long measurements times. The unfeasibly long characterization necessary to a large number of devices to characterize RTN stochastic phenomena becomes achievable and easily implemented to obtain reliable and accurate defining parameters with promising results.

2.4 – Analytical study:

A theoretical framework is proposed in this thesis which supports the validity of our approach when obtaining the mean value of Ndef. If it is assumed that the mean occupation probability of the studied defects is 0.5 (emission and capture are not correlated), the resulting probability that in one device all the defects are on the same occupation state (oc(t1) = oc(t2)) at t1 and t2 is ½·Ndef. That makes that probability be 1 when the number of defects is zero (Ndef=0), 1/2 when there is 1 defect, 1/4 for 2 defects, etc.
Considering that the Ndef varies from device to device according to a Poisson distribution the probability of having ΔID = 0 is given by eq. 6

$$Prob(\Delta I_D = 0) = \sum_{i=0}^{\infty} \left[\left(\frac{Pi(<N_{def}>)}{2^i} \right) \right] \qquad (6)$$

Where Pi (<Ndef>) are the values of the Poisson distribution with mean value <Ndef> and can be calculated as:

$$P_i(< N_{def} >) = \frac{e^{-<N_{def}>} <N_{def}>^i}{i!} \qquad (7)$$

When joining eq. 7 on eq. 6, the results of the sum of infinite terms becomes

$$Prob(\Delta I_D = 0) = e^{\frac{-<N_{def}>}{2}} \qquad (8)$$

The resulting eq. 8 shows that the probability that the occupancy states at two different independent instants decays exponentially with the mean number of defects. This results can be numerically calculated using our method and applying eq. 2 assuming that the background noise is 0 (σ = 0) and evaluating the probability that ΔID=0 . Figure 2.10 shows the probability of not having a current change (Prob(ΔID=0)) as a function of <Ndef> calculated with eq. 8 (line) and the two-point method (blue symbols).

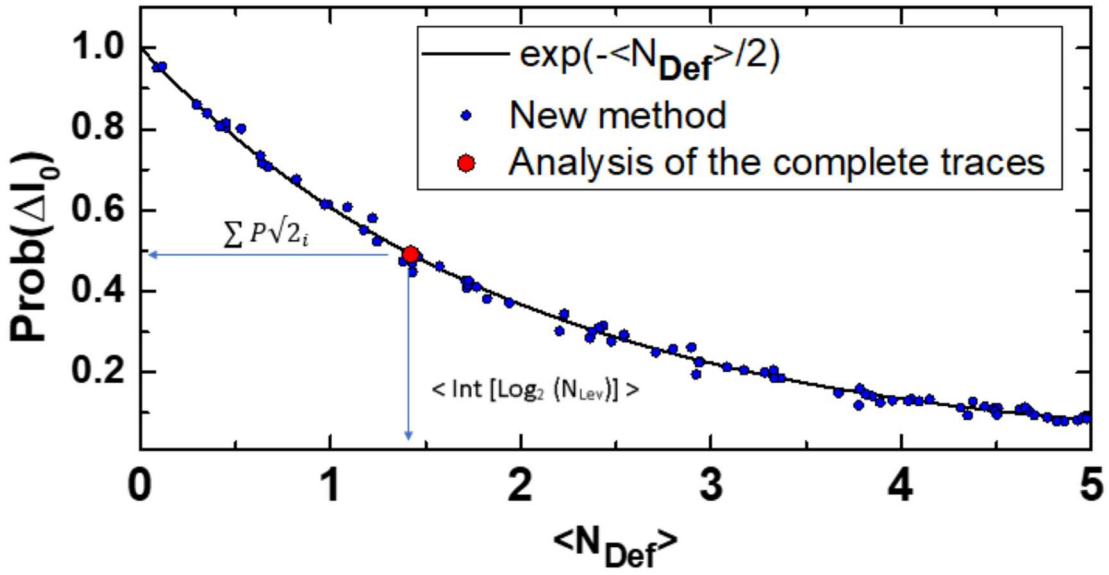

Figure 2.10: The probability that oc(t1) = oc(t2) for all the defects in a device, Prob (ΔI0), has been calculated according to combinatory theory (eq. 1) (line), with Monte Carlo simulations performed using the two-point method (blue symbols) and from the analysis of the complete traces (red symbol). In this last case, eq. 6 has been used, where Pi have been evaluated from the experimental distribution of NDef (red symbols in Fig. 2.3) and <NDef> is calculated using eq. 5.

For further support of this results, the <Ndef> and Prob(ΔID=0) using the full trace analysis with the WTLP are also shown on fig. 2.10. For the WTLP results, <Ndef> have been calculated using eq.5 and the Prob(ΔID=0) has been calculated from eq. 6 using as Pi the values of the experimental Ndef distribution from the analysis (red symbol in fig. 2.10). The perfect match between the results provided by the three different procedures demonstrates the validity of the calculations using the two-point method presented in this thesis.

2.5 – Proposed method examination:

After the full trace analysis comparison using WTLP and the mathematical framework presented on the previous sections, two different studies using the experimental data will be presented, the first one being the evolution of the resulting extracted parameters depending on the time difference between T1 and T2 when using the method and the second one being a study of the evolution of those parameters depending on how many devices are under test. All of these experiments have been performed for a single type of device and technology and the method may have different results on other devices depending on their intrinsic properties, device variability, architecture, etc.

2.5.1 Time Difference:

For the time difference analysis, the data have been checked changing the time exponentially, being the minimum time different 0.002 and the maximum time being 40 s. The results are shown in figure 2.11. When looking at the current shift parameter (<η>) (fig. 2.11 blue graph) it can be observed that at shorter times the value fluctuates a lot and has no consistent values but when the time difference for (t2-t1) is greater than 0.1 s the <η > value stabilizes at the previously found solution (3.8 nA). The variability on the results when the time difference is too short is attributed to the low number of detected defects as shorter times won't allow for most of the defects to perform a capture/emission event as the capture and emission times may be longer.

This correlates to the results obtained for the number of defects (fig. 2.11 red graph), where we can see that for shorter times the number of detected defects is greatly reduced as most of the defects did not have enough time to change state. On the other hand, as the time difference increases, a higher number of defects can be detected with the method as the longer capture and emission times defects start to appear. Although that graph shows an upward trend it is expected that for longer times this graph would stabilize around a certain number of defects.

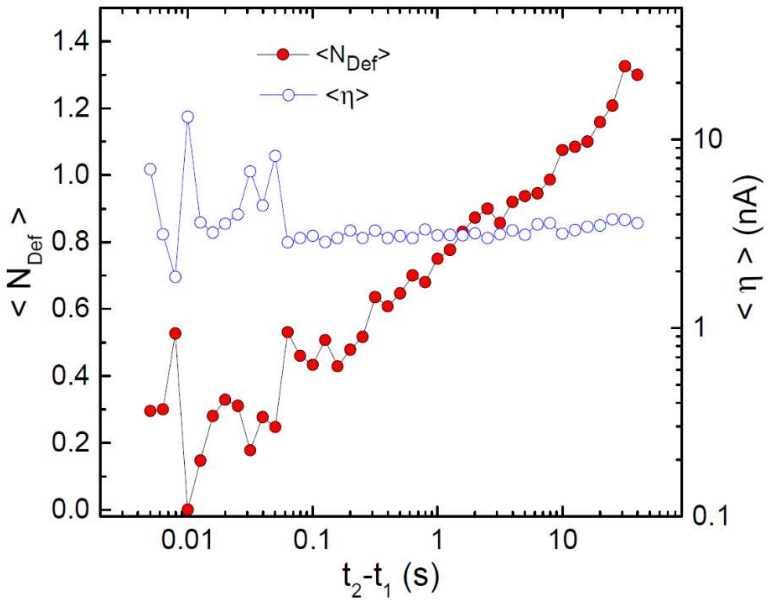

Figure 2.11: Obtained values of <NDef> and <η> as a function of the time elapsed between the two measurements of ID.

2.5.2 Number of devices under Test:

The method is designed to be applied to a large number of devices as it takes advantage of the statistical representation of the ΔID samples, so the higher the number of devices under test, the better the accuracy in the extracted NDef and η statistical distributions. However, the fabrication and use of many devices can be expensive. Therefore, it is important to investigate which are the effects of the number of devices used with the method to obtain acceptable results. To investigate this point, the method has been applied to sets of the experimental RTN traces varying the number of devices used in each one.

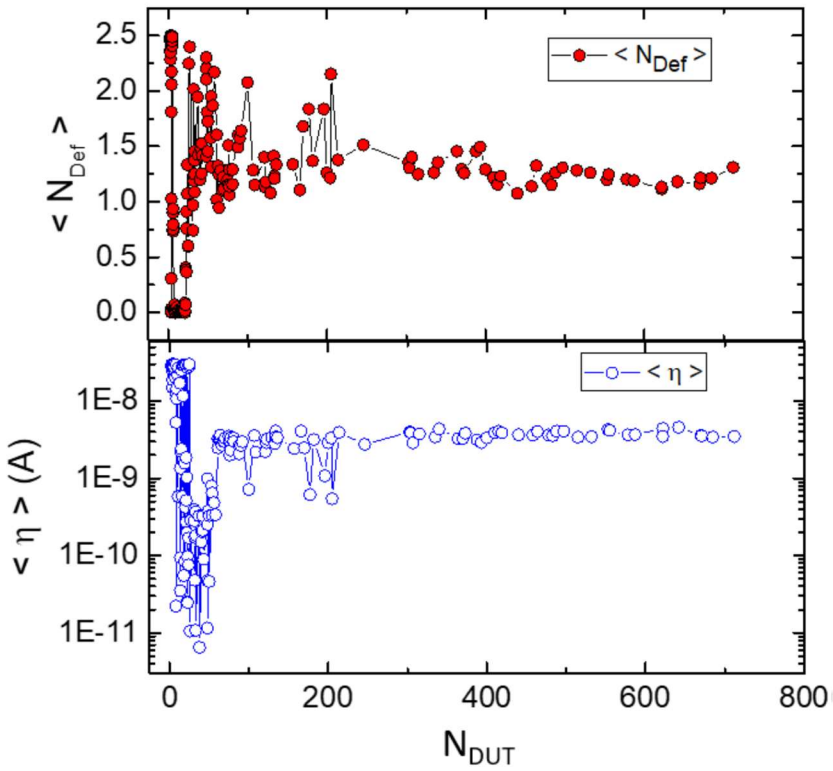

Figure 2.12: Mean number of defects <NDef > (top) and mean current shift <η > (bottom) as a function of the number of devices under test (NDUT).

In Fig. 2.12 the <NDef > (top) and <η > (bottom) values obtained as a function of the number of devices considered is plotted. It can be observed that if less than approximately 100 devices are used in the analysis, <NDef > and <ηmth > parameters fluctuate indicating that the values obtained have a high variability and can be identified as not representative enough. However, <NDef > and <η > converge to the same final solution for the full 784 device set if more than 250 devices are used and have reasonable results after 100 devices. This number, which is valid for our particular devices, should be considered only as an indicator if the Two-point method is to be applied for other technologies.

2.6 – Conclusions

In this chapter a new characterization method has been presented, analyzed, and validated through a plethora of processes. Those involving the comparison with a traditional

characterization method, a mathematical framework from a probability perspective, and an statistic overview of the limits of the proposed method on the studied technology.

Although the presented method has its caveats, for example the impossibility to characterize capture and emission times that a full analysis of traces with methods like WTLP would be able to, the possibility to reduce the necessary experimental and computational time makes this method an highly efficient alternative to the traditional characterization methods.

The use of this method allows the design of experiments with a highly reduced measurement time. This originates the possibility to only measure the current at two different instants (t1 and t2) instead of a full trace measurement. Another time saving origin when using the presented method is a faster analysis of the experimental results due to lower computational requirements. Due to only having to analyze the ΔI CDFs created from two data points in order to extract the statistical parameters for our studied phenomena, instead of analyzing the thousands of data points of each trace from each device, the method computation times when compared with traditional methods like WTLP in the case of this thesis become way faster and agile with almost the same exact resulting parameters as demonstrated on the validation.

Furthermore, the statistical evaluation results show great promise on the usability of this new characterization method, showing that approximately only 100 devices are needed to obtain significant statistical parameters for this technology and that the ability to perform longer experiment times would allow for a high quality characterization of the RTN phenomenon .

Finally. the mathematical framework analysis shows that the approach of assuming a uniformly distributed capture and emission times with a mean value at 50% follow the correct occupation probabilities and coincide with the WTLP characterization results.

Chapter 3

Proposed Method expansion for aging experiments.

After the description and validation of the Two-point method presented on the previous chapter, the characterization of the RTN phenomena have been characterized successfully. On the other hand, the original RTN method is not useful if your devices present the sings of aging. Aging effects like Bias Temperature Instabilities (BTI) or Hot Carrier Injection (HCI) are the cause of a huge part of the reliability issues that appear on transistors during their operation lifetime.

For this reasons, an extension of the Two-point Method to include these two aging phenomena will be presented in this chapter, followed by the characterization of these effects under many different stress biasing conditions involving BTI/HCI experiments and RTN experiments for long times (on which even though the stress conditions are under nominal operation conditions, due to the long experimental time, show the starting appearance of BTI/HCI). Finally, a characterization of FD-SOI Ω-gate transistors using the expanded method will also be presented.

3.1- BTI and HCI extension.

The present section will be dedicated to the description of the expansion of the method to include firstly BTI (only gate bias stress) and later sections experiments will include the CHC degradation (gate and drain bias stress).

There are some considerations regarding the BTI phenomena that must be mentioned in order to understand the development process. As a device is put under gate stress bias, the appearance of a drain-source current shift due to the influence of a newly charged BTI defect will be dictated by that stress bias and the stress time that the device has undergone. It is assumed that those defects will always translate into a current shift of the same sign (positive or negative) due to the applied stress being positive or negative on the duration

the experiment. When compared with RTN defects current shifts, that can be positive or negative with a mirrored distribution due to the occupation being randomized, BTI defects will be considered to always start on the high current state at T1 and charged at T2. This way, as a norm this thesis has considered those current shifts as positive by convention.

Another consideration with this method would be that in order to obtain a correct characterization of the BTI effects it's preferable to observe the current change between the fresh current to the after-stress current. A normal BTI current trace that shows relaxation could not show all the BTI defects that appeared the same way as an RTN trace as the relaxation time can become extremely long. Because of that, the calculation for the method when using the BTI expansion would be comparing the fresh device current (as if it was T1) and the first current measurement available after the stress (as T2). This will not influence the appearance of RTN on the characterization as this phenomenon will appear in both the RTN and the BTI type of parameter extraction. This caveat only affects the creation of the CDF, so the rest of the method will have the same process with the changes that are going to be explained in this section.

With these considerations in hand, the current shift between t1 and t2 on a device with both RTN and BTI would be expressed with the following equation:

$$\Delta I_{D_{mt}} = [\sum_{i=1}^{i=N_{Def_{mt\ RTN}}} \eta_{mth_{RTN},i}(oc_i(t2) - oc_i(t1))] + [\sum_{i=1}^{i=N_{Def\_mth\_BTI}} \eta_{mth\_BTI,i}] + randn(\sigma); \quad (9)$$

Where Ndef_mth_BTI being the number of BTI defects and ηmth_BTI,I the current shift associated to each i-th defect.

If we take a look at Eq. 2, the first bracket corresponds to the RTN part present on the Eq. 1 of the original RTN only Two-Point method and the second brackets corresponding to the BTI defects. As it can be seen in the equation, the BTI does not consider the occupation due to the previously mentioned current shift being on one singular sign (positive or negative) that depends on η. The BTI introduction will have some consequences. Firstly, the method will go from having 2 randomized parameters to having 4, those being the number of defects for each of the two effects ($< N_{Def_{mt\ \_RTN}} > and < N_{Def_{mth_{BTI}}} >$) and the current shifts that each of those defects cause ($<\eta_{mt\ \_RTN,i} > and < \eta_{mt\ \_BTI,i} >$).

With these 2 new variables, the identification of the best fitting parameters becomes more complex as the visualization of a minimum involving 4 different variables is counterintuitive. Luckily, due to the nature of these two phenomena, on most experiments one phenomenon will dominate over the other as normally when the stress is high, the presence of BTI overshadow the RTN current shifts, and vice versa, when the stress is too low, BTI is nonexistent and the RTN is the only observable phenomena.

As those parameters are paired to represent each of the phenomena, it was decided to do two different fitting adjustments, one for RTN parameters and one for BTI parameters. This allows the user to easily discern which of the two phenomena is more prevalent as the error map will show a mostly uniform distribution when RTN is not prevalent, and a minimum at zero traps and/or zero current shift for BTI when it's not present.

Although HCI degradation physical mechanism is different from both BTI and RTN, as this method only takes in to account current shift before and after stress, if the stress conditions are right, both BTI and HCI will appear in our devices so the current degradation will include a mix of both phenomena.

As this method has been newly developed during this thesis, a validation is required. To validate the usability of the method, an extensive characterization and analysis of experimental data have been performed with both the developed method and a full trace analysis method, being the weighted time lag plot (WTLP). As this characterization and comparison involves experimental results, this will be presented the first section of Chapter 4 of this thesis.

Another observation of the method is pertaining to the parallelization process. Using the proposed method, the measurement time periods on the aging experiments could also be reduced to the minimum measurement time allowed by the equipment like in the RTN case, when the experiments are focused on the characterization of mainly the after-stress defect detection/current shift, as it's the case of this thesis case.

3.2- Bias Temperature Instabilities experiments.

This section will present the experiments performed to characterize BTI phenomenon in a wide range of biasing conditions and the consequences that stress time and relaxation time after stress have under the studied conditions.

3.2.1 - Experimental procedure.

The devices used for this work are the devices described in Chapter 1, pMOS transistors with W/L=80nm/60nm. The experiments consisted in several phases. First, an ID-VG characteristic was measured to obtain the initial fresh threshold voltage of each device Vth0.

After that, devices were subjected to a Measurement-Stress- Measurement (MSM) scheme [82] (Fig. 3.1a). The stress phases were applied with a duration of tS=1s, 10s, 100s and 1000s and a wide range of gate stress voltage Vs=-1.2V, -1.5V, -2V and -2.5V while the other terminals were grounded.

We will refer to the stress phase when we apply the voltage VS to the studied devices as this is the usual nomenclature, however, in the case of Vs = -1.2V we cannot consider that the devices are actually subjected to accelerated electrical stress, since this biasing conditions fall under nominal operating conditions.

Fig. 3.1b and Fig. 3.1c show two examples of ΔVth trace over time. It can be observed that, at VS=-1.2V, ΔVth alternates between two different levels, which indicates that RTN is dominating the Vth fluctuations (Fig. 3.1b); however, for VS=- 2.5V several Vth drops can be observed, which correspond to the emission of charges that have been trapped during the previous stress phases, (Fig. 3.1c), which is typical of BTI.

During the after-stress measurement phases, with a duration of tm=100s, the drain current was continuously measured applying Vm=-0.6V to the gate and VD=--0.1 V to the drain.

From the measured current, the threshold voltage after the stress, Vthf, was calculated with the method presented in [83].

For these experiments, sets of 200 devices were tested for each stress biasing condition, which if calculated, means that more than 100 days would have been required to perform these experiments without parallelization. However, using our approach, all the measurements were performed in less than a week of experimental time.

Following the Two-Point characterization method, for each device, the threshold voltage shift ΔVth=|Vthf|-|Vth0| was calculated for each device.

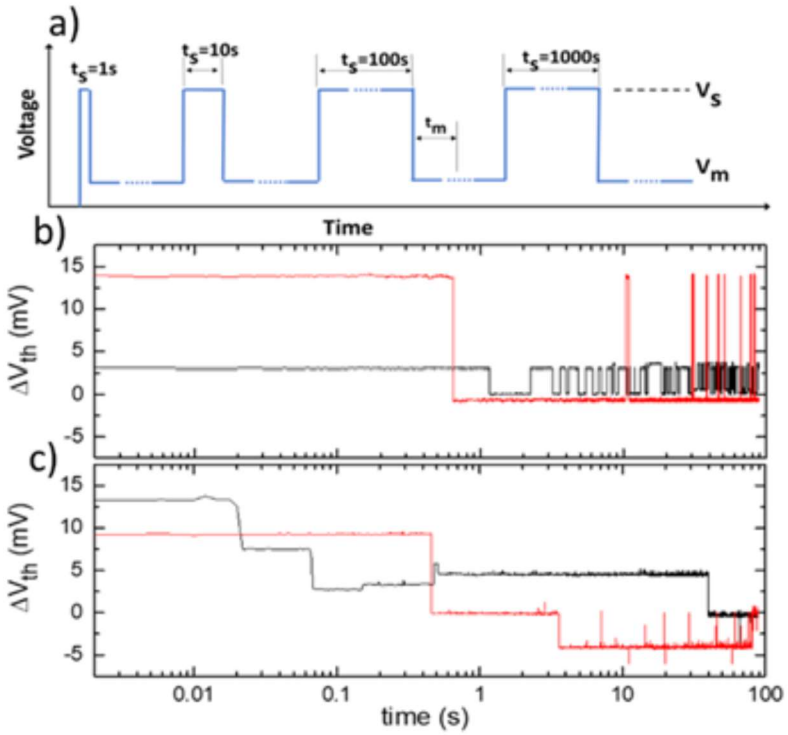

Figure 3.1: (a) MSM scheme used to investigate RTN and BTI in pMOS devices. b and c) ΔVth evolution in 2 pMOS devices (W/L=80nm/60nm) measured at Vm = □0.6V, for the cases of (b) VS = □1.2V and (c) VS= □2.5V. ΔVth is defined as the difference between Vth(tm) and Vth measured on the pristine device.

3.2.2 – Results

Δ Vth traces over time of Fig. 3.1b and c are illustrative examples of our measurements, however due to the stochastic behavior of the defects, a large spread is expected in measurements performed under nominally identical conditions. Therefore, in order to obtain an accurate enough extracted parameters for a useful modeling these phenomena it's necessary to statistically analyze the results. For that reason, Fig. 3.2 shows the Δ Vth cumulative distribution functions (CDF) of the performed experiments at VS= -1.2V and VS= -2.5V and at different stress duration, tS. Positive/negative values of Δ Vth are attributed to a net trapping/detrapping process during the test.

The symmetry of the distributions at VS=-1.2V hints at a similar number of trapping and detrapping events, which is consistent with the dominant presence of RTN during

nominal biasing conditions, as shown in Fig. 3.1b. Many devices show a close to Δ Vth=0 behavior, which indicates that either there are no defects in the device or, if there are, they do not effectively change their occupancy state during the measurement.

For VS=-2.5V, Δ Vth rapidly increases with tS because of the larger trapping probability for larger stress times. Defect charge trapping also increased (and, thus, Δ Vth) with VS (Fig. 3.3a). In Fig. 3.3b, the shift of the distributions to lower values as tm increases indicates the progressive detrapping of charges that were trapped during the stress, signifying a recovery towards the original CDF. Note that for all the Δ Vth distributions of Fig. 3.2 and Fig. 3.3 Δ Vth is negative in the low percentile tails, which implies that a net detrapping is not negligible. Therefore, even for the most aggressive stress conditions applied in these experiments (VS=-2.5V) detrapping caused by RTN can still be relevant and consequently should be considered for modeling purposes.

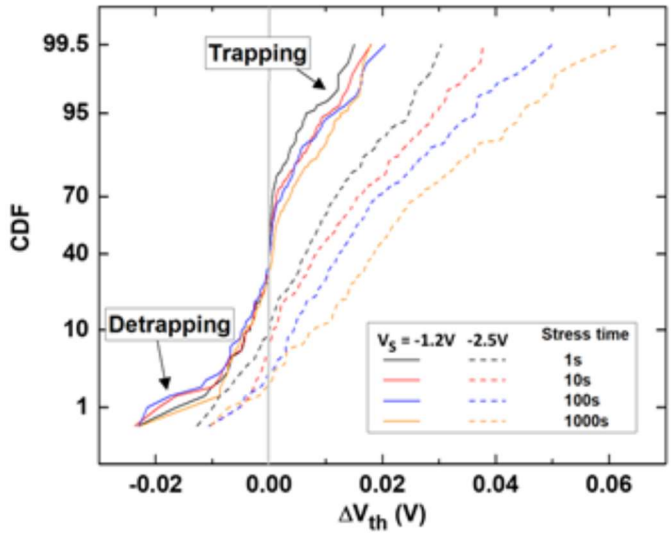

Figure 3.2. Examples of ΔVth distributions measured at tm=100s for different values of VS and ts. 200 devices are considered in each distribution.

The values of RTN parameters <N0>=1.37 and <η0>=3.2mV have been obtained from the experiments at low voltages. On the other hand the values of the RTN parameters have been added to the fitting of the higher biased experiments. The good fitting of the experimental data as shown in fig. 3.3, demonstrates that the BTI and HCI expansion explained in the previous 4.1 section, despite its simplicity, it's sufficient to describe the Δ Vth distributions measured when RTN and BTI phenomena are simultaneously active. Consequently, the effects of stress are reflected in the resulting extracted parameters, being the mean number of BTI defects <Ns> and the mean current shift <ηs> that those cause.

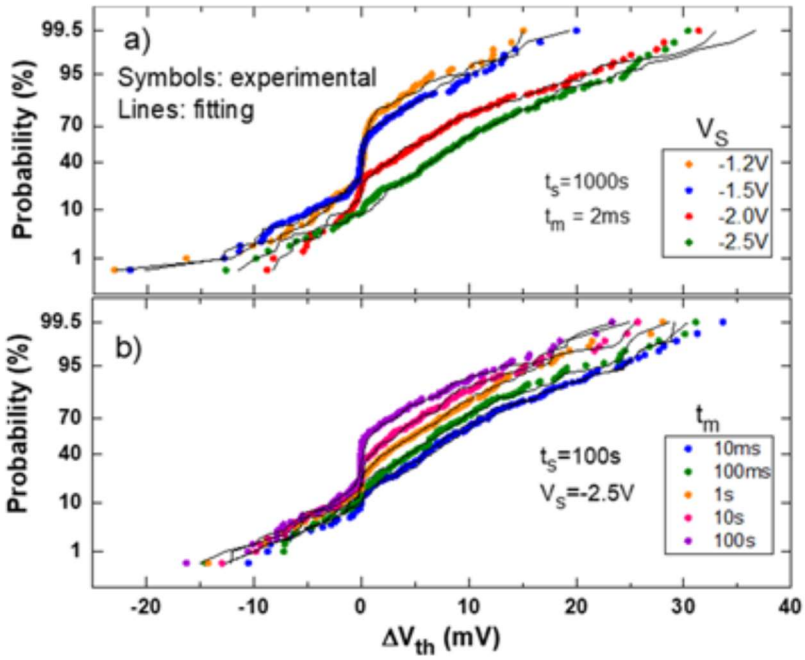

Figure 3.3 ΔVth distributions obtained for (a) different VS and (b) different measurement times, tm. Lines show the fittings obtained with eq. 2.

The full modelling of the ΔVth distributions requires the evaluation of their dependencies on the biasing conditions, so the voltage dependencies of <NS> and <ηS>have been analyzed. Fig. 3.4 shows <NS> as a function of the stress time, tS, and measurement, tm, times, at which the T2 for the method was used, for different values of gate stress bias. Note that <NS> is the only parameter required to describe the statistical distribution of NS, therefore, the results in Fig 3.4 are sufficient to estimate the number of defects in a device that will be active as a consequence of the stress. In the time range investigated in these experiments, <NS> exponentially increases with tS, due to charge trapping during the stress segment, and exponentially decreases with tm, due to detrapping of previously trapped charges when measuring at lower biasing conditions.

As expected, the number of defects that trap charges increases with VS. If we compare the results of Fig. 3.4 with those at lower voltages (i.e. <N0>=1.37), it is clear that for |VS|≤1.5V the number of appearing BTI defects, <NS>, is smaller than the base mean RTN active defects <N0>, though the contribution of <NS> should not be considered negligible.

If |VS|≥2V, <NS> appears to be clearly larger than <N0>, but even in the most aggressive biasing tested condition (VS=- 2.5V, ts=1000s and tm=10ms), its maximum value (<NS>=6.7) is not large enough to consider that the contribution of RTN defects <N0> is negligible.

Then, from this discussion, we can conclude that for the accurate description of the ΔVth in a large voltage range (from nearthreshold up to voltages more than double the nominal values), the whole range of active defects should be considered. That is, those defects that would be only observed at low voltages (leading to RTN) and those that will be only activated at the larger voltages (observed as BTI).

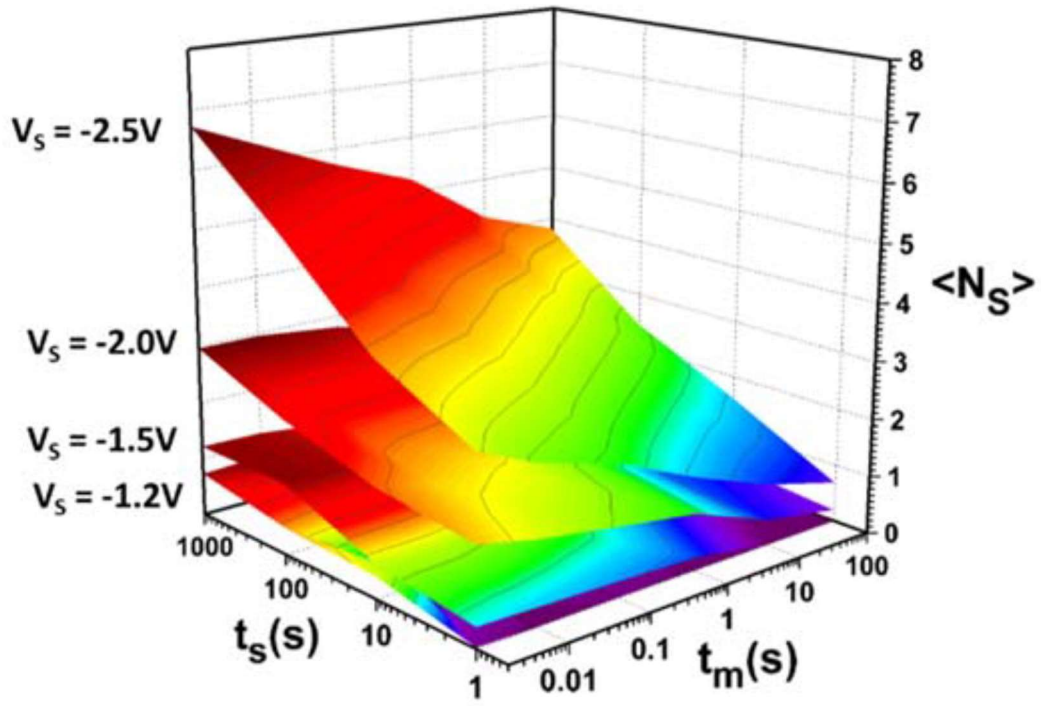

Figure 4 3.4: <Ns> as a function of the stress and measurement conditions VS, ts and tm.

To provide a simple kinetics model valid for the considered technology, <NS> has been described using the following semiempirical expression based in the Universal Relaxation Function for BTI [84]

$$< Ns >= \frac{K \cdot (t_s)^{\alpha}}{1+B(\frac{t_m}{t_s})^{\beta}} \qquad (10)$$

|Vs| (V)	α	B	β
1.2	0.22	11.49	0.68
1.5	0.26	2.67	0.34
2	0.098	2.88	0.32
2.5	0.066	2.01	0.15

Table 1: α, β and B values of eq. 3 obtained at the different voltage conditions tested.

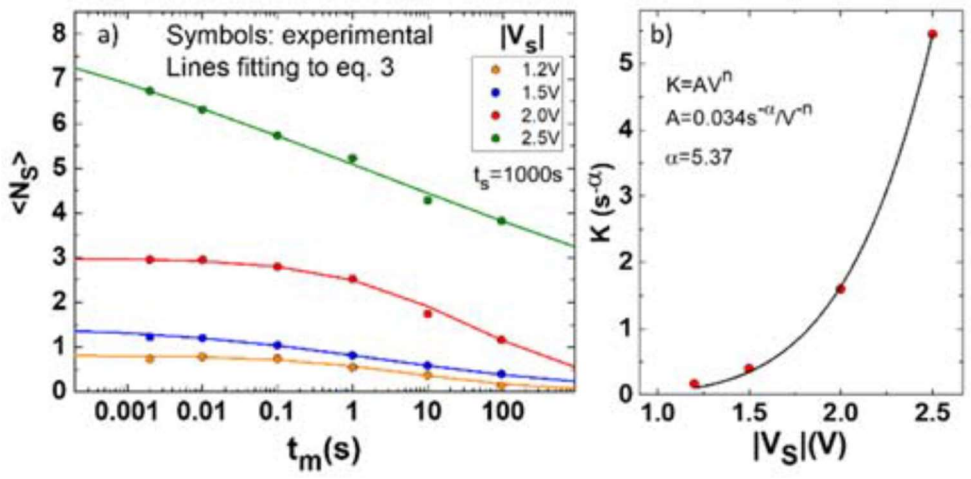

Figure 3.5: a shows the fittings of <NS> to eq. 3 for ts=1,000s, while the extracted values of the parameters α, β *and B are given in Table 1. Fig. b shows that the K parameter fits to a power law with VS.*

Finally, the dependence of <ηS> with the voltage conditions have been investigated. It should be remarked that <ηS> is the only parameter needed to evaluate the ηS distribution, therefore it is enough to describe the magnitude of the Vth shift at larger stress bias. The symbols in Fig. 3.6 shows the estimated <ηS> at tm=2ms and ts=100s for the investigated VS from the fitting of the Vth shift distributions. There is no observable dependence of <ηS> on VS. Interestingly, the values found are very similar to those reported in [85] (black line), where the full trace analysis of all the temporal traces measured after the stress (as those in Fig. 3.1) was done to directly assess the ΔVth contribution of individual defect discharges, which supports the validity the two-point characterization method. Note also that the <ηS> values are close to <η0>. This similarity indicates that the charging/discharging of defects produces a ΔVth that does not depend on the gate voltage in a large voltage range. The results in Fig. 3.4 and Fig. 3.6 show that stress (i.e. large voltages) has an impact mainly on the number of active defects but a negligible effect on the magnitude of their associated Vth shift distribution. Therefore, an accurate characterization of <NS> is crucial for an accurate modeling, however, is not enough because of the contribution of those defects acting without apply any stress, ergo RTN defects.

In this section, the simultaneous impact of RTN and BTI has been statistically investigated in a large range of gate stress biasing conditions. The analysis of the experimental data demonstrates that RTN and BTI coexist, though one may dominate over the other depending on the stress conditions. The two-point characterization model describes, in a wide range of gate biasing conditions, from near threshold to high stress voltage, covering the nominal operation conditions, the ΔVth statistics when RTN and BTI are simultaneously present. These results show that the stress affects only the statistical distribution of the number of active defects, which in our model can be described with a single statistical parameter.

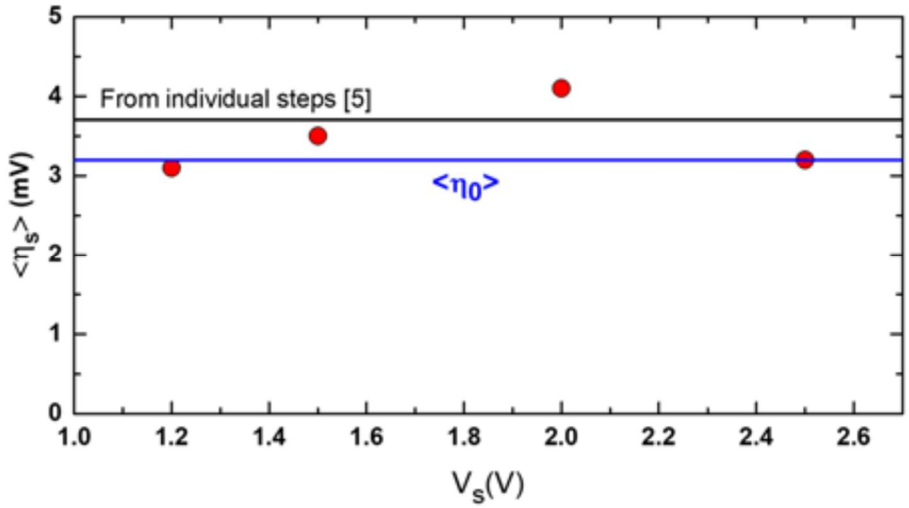

Figure 3.6:Symbols: <ηs> as a function of VS. The black line corresponds to the reported value in [86], which was obtained from the full analysis of the experimental traces.

3.3 – FD-SOI Characterization

Another set of experiments have been designed to perform a characterization of FD-SOI type of device. In contrast with the devices used in the rest of this thesis, the FD-SOI devices used in this section are fabricated on a wafer instead of a specialized chip and were measured manually one by one. For this reason, the number of studied devices is lower, and the experimental time are reduced. Despite that, this section will focus on its characterization using the proposed method and its discussion.

The devices under test in this section are nMOS Ω-gate FD-SOI devices with 30 nm channel width and 40 nm channel length. The average threshold voltage and nominal operation voltage are ~0,3V and from 0 to 1V, respectively. An in-depth detailed description of the devices can be found in [87]. The measurements performed on these devices have been applied with a traditional, on wafer, RTN measurements over time. Several combinations of constant gate, drain, source and back gate voltages were applied (see Table 1) during 50s, while the drain current was measured. Near-threshold and nominal voltages were selected, to operate the transistor in the linear (VG =0,3 V) or saturation regimes (VG = 0,5 V and 1 V). For each voltage combination, 38 devices were measured. The shift (if any) in the performance of the devices was evaluated using the proposed characterization method, based on the evaluation of the drain current shift at two different time instants, ΔID=ID(t2)-ID(t1), (Fig. 3.7); in this work, t1= 0s and t2=50s. The extracted parameters have been performed with the proposed characterization method presented in chapter 2 and expanded on section 3.1 of this chapter.

With the set of ΔID evaluated from the different devices, from the currents ID traces, as those shown in Fig. 3.7, a cumulative distribution function (CDF) is constructed for each of the biasing conditions (see experimental CDFs in Fig. 3.8). Once those CDFs were fitted with the proposed characterization method, the statistical parameters were extracted, the average number of defect (both <NRTN> and <NBTI>) and the impact (i.e., current shift amplitude, <ηRTN> and <ηBTI>) linked to RTN and BTI defects (see

Table 2). Although the experiments were performed as a RTN experiments, the higher biases started to show few BTI defects. Fig. 3.9-3.11 show the fitting of the experimental distributions, for several of the biasing conditions.

Biasing Conditions				
Condition nº	Gate Bias (V)	Drain Bias (V)	Source Bias (V)	Back gate Bias (V)
1	0.3	0.3	0	0
2	0.5	0.5	0	0
3	0.5	0.5	0	-15
4	0.5	1	0	0
5	0.5	0.05	0	0
6	1	0.05	0	0
7	0.5	0	0.5	0
8	0.5	0	0.05	0

Table 1: Several combinations of drain/gate/source/back gate voltage were studied, to evaluate their impact on the drain current shift during biasing.

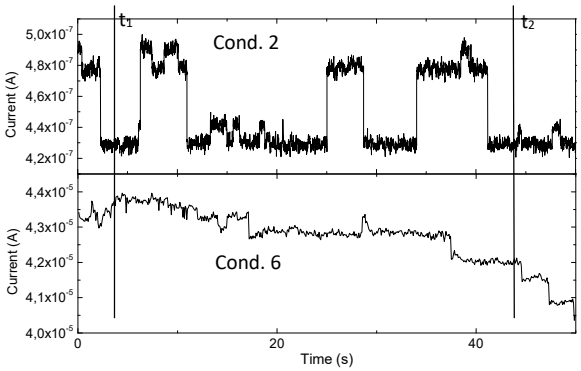

Figure 3.7: Examples of experimental ID current traces measured at two different conditions. (top) RTN is dominant. (bottom) BTI and RTN are simultaneously observed. For the determination of the defect-centric model parameters, the current shift is evaluated as the difference of the currents measured at two given time instants. In our case, t1=0s and t2=50s

Several conclusions can be drawn from the parameters in Table 2 together with the observations from the CDFs. RTN is present in all the studied conditions, but the observed number of defects depend on the biasing conditions. The back-gate voltage has a negligible effect in the RTN (conditions #2 and #3), as the CDFs in Fig. 3.9 show. Increasing VD and VG leads to the appearance of more RTN defects (conditions #1 and #2). But VG and VD may impact differently. Larger effects are observed when the device is operated in saturation (conditions #2, #4 and #5, same VG, different VD). But, for the highest VD, a BTI component also appeared (condition #4), even when the device is operated within the nominal biasing range (without stress). Conditions #5 and #6 show that VG has a large impact in RTN since, despite the low VD, a large RTN component is measured (the largest <ηRTN> is also obtained). Moreover, BTI is larger (i.e., larger <NBTI> and <ηBTI> parameters) than the conditions where a large VD is applied (condition #4). Note that the BTI component in Fig. 3.10 for the largest VG shows the largest negative current shifts. The exchange of drain and source, either when in the linear (conditions #5 and #8) or saturation (conditions #2 and #7) regimes, shows no remarkable differences (Fig. 3.11), which suggests that, at these low voltages, RTN defects are quite uniformly distributed along the channel.

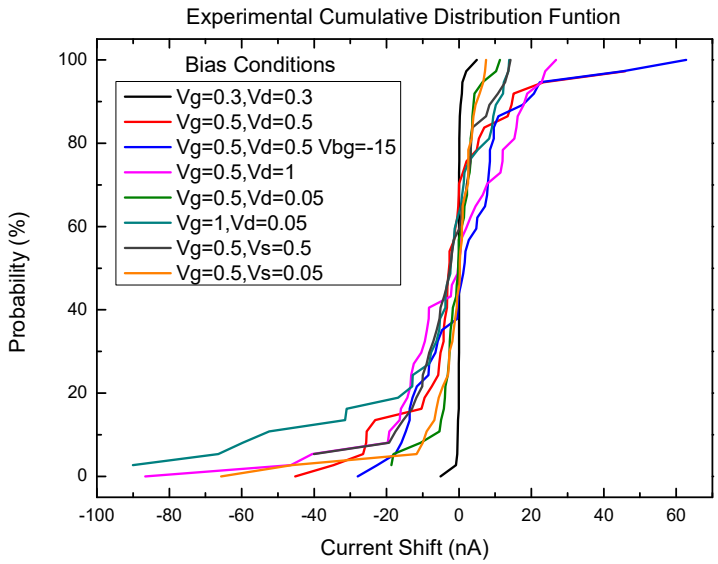

Figure 3.8: Experimental CDFs of the current shifts measured for all the biasing conditions.

The statistical characterization described in this section of on-wafer Ω-gate FDSOI devices measured at several bias (near threshold and nominal) and operated in linear or saturation has been carried out and interpreted in the context of a defect-centric model. The comparison of the observed performance shifts and the extracted average model parameters show that RTN is the dominant TDV mechanism in this voltage range, but BTI can be also observed at nominal conditions when close to the operational limits.

As for the RTN effects several observations can be deduced. Firstly, the body bias has a negligible impact on the performance of these devices. Secondly, when the devices are operated in the saturation regime a higher impact is observed on the extracted parameters. And finally, gate bias (VG) has the larger impact on the observed RTN defect number and current shift.

Parameter Results				
Condition Nº	$<N_{RTN}>$	$<\eta_{RTN}>$ (nA)	$<N_{BTI}>$	$<\eta_{BTI}>$(nA)
1	0.9679	1.0918		-
2	6.4624	8.0086	-	-
3	7.1045	7.9030	-	-
4	9.6954	7.7154	0.0500	5.2023
5	5.6140	2.6713	-	-
6	4,3624	14,833	0.5569	9.9656
7	9.4443	4.5242	-	-
8	6.8948	1.8843	-	-

Table 2: Average values of the model parameters obtained from the fitting of the ΔID CDFs to eq. (1), for the different experimental conditions.

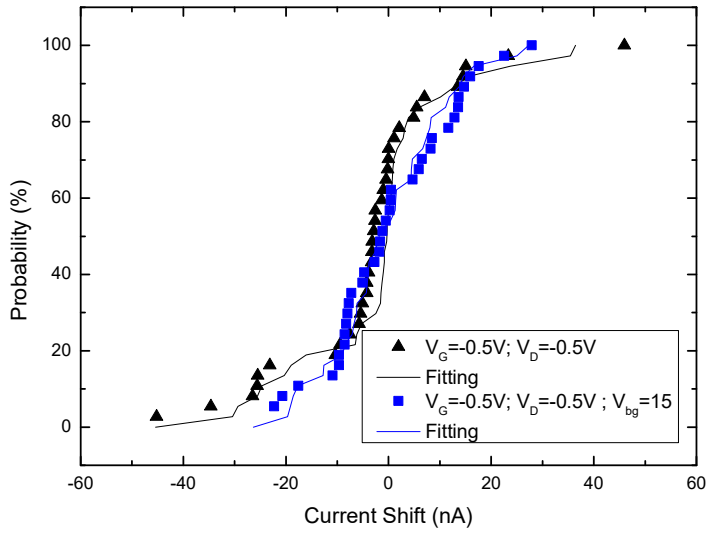

Figure 3.9: CDFs of the current shifts obtained with and without back bias (conditions #2 and #3).

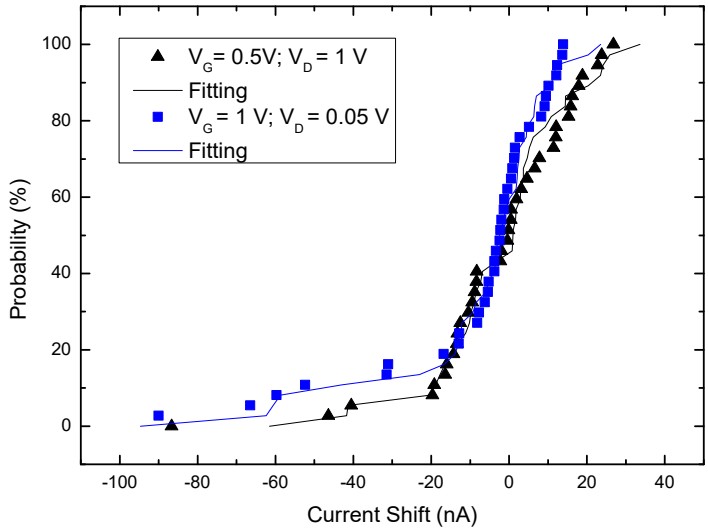

Figure 3.10: CDFs for the cases where a BTI component is observed, which correspond to either a 'large' VG or VD (conditions 4 and 6). The BTI degradation is larger for the VG = 1 V case (blue curve/squares).

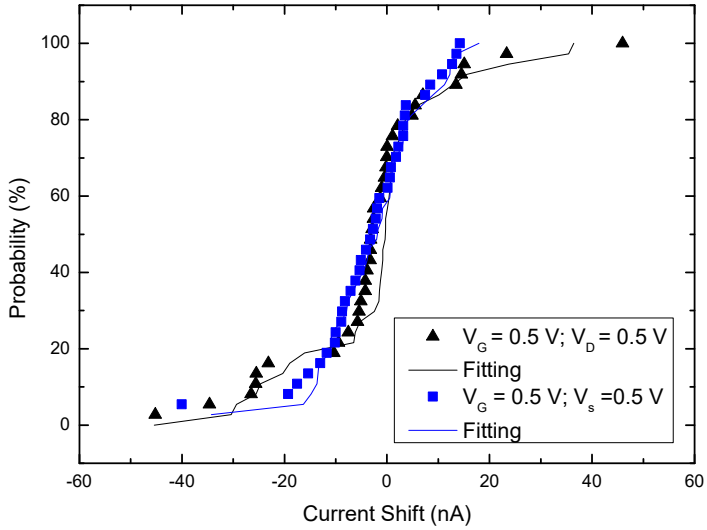

Figure 3.11: CDFs of the current shifts measured when source and drain are exchanged, and the device is operated in saturation (conditions #2 and #7).

3.4 – TDV in a wide range of biasing conditions

Following the experiments involving BTI experimental conditions presented in the previous section, a new set of aging experiments was designed in order to characterize both BTI and HCI for a wide range of biasing conditions.

Experimental conditions:

The same MSM technique and devices as in the previous section, utilizing the capabilities of the ENDURANCE chip coupled with the TARS control software, was used. In the case of these experiments, the Measurement phases consisted in the acquisition of fresh drain current measurement during 100s with Vg=-0.6V and Vd=-0.1V followed by a fresh Id-Vg. The Stress phases biasing of the performed experiments consisted in all the possible combinations of the following Vg and Vd stress conditions: VG= 1.2, 1.5, 2, 2.5 V and VD=0, 1.2, 1.5, 2, 2.5 V, being the conditions with Vd=0 the experiments presented on the previous section. The experiments consisted in four stress phases with exponentially increasing times of 1s, 10s, 100s and 1000s. The measurement phases were applied at the beginning of the experiment and after each stress phase. Each stress experiment condition was applied to 100 devices set in order to perform statistical analysis of the results. In summary, in this section, 2000 transistors were investigated.

Figures 3.12 and 3.13 show some examples of the Id-t traces measured in the studied devices. In Fig. 3.12 the biasing during the stress, was Vg=1.2V and Vd=1.2V that is under the nominal operation conditions for this technology and shows the typical RTN behavior. On the other hand, Fig. 3.13 shows some examples of a trace that shows BTI behavior when a higher stress biasing conditions are applied.

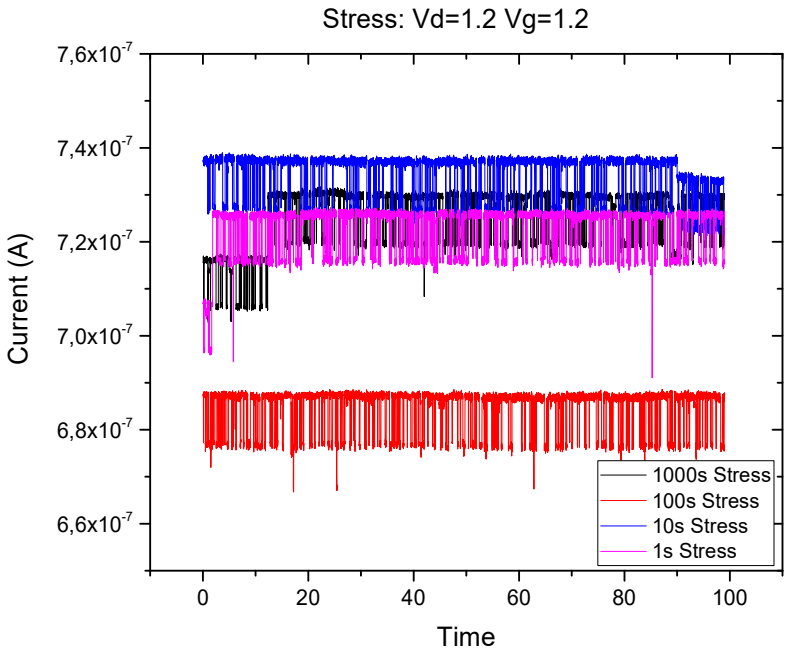

Figure 3.12: Example traces of low stress voltages at different stress times exhibiting RTN behavior.

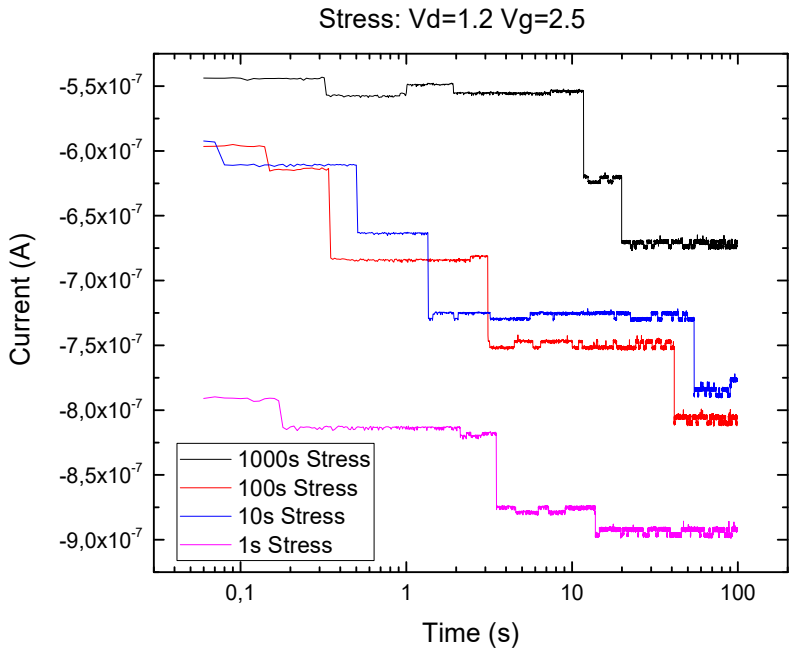

Figure 3.13: Ejemplo de trazas Id a diferentes tiempos de estrés a Vd=1.2V y Vg=1.2V.

Firstly, the evolution of the measured Id-Vg allows us to extract the threshold voltage increase (ΔVth) due to the stress applied. The obtained results are shown in Fig.3.14. As expected, the degradation of Vth is more pronounced when both the stress times and the stress biasing are higher. Using sets of 100 s measurements of Id-t, a CDF of the ΔID necessary for the proposed method will be created for each 100 device set for each studied stress conditions. Fig. 3.15 shows the full range of CDFs (experimental data) used during these experiments. Just looking at the evolution of those CDF, the results show a clear distinction between the highly stressed CDFs and the experiments with lower stress bias.

After analyzing each stress conditions with the proposed method, different observations can be made with the resulting ΔId CDFs and the corresponding extracted RTN and BTI parameters.

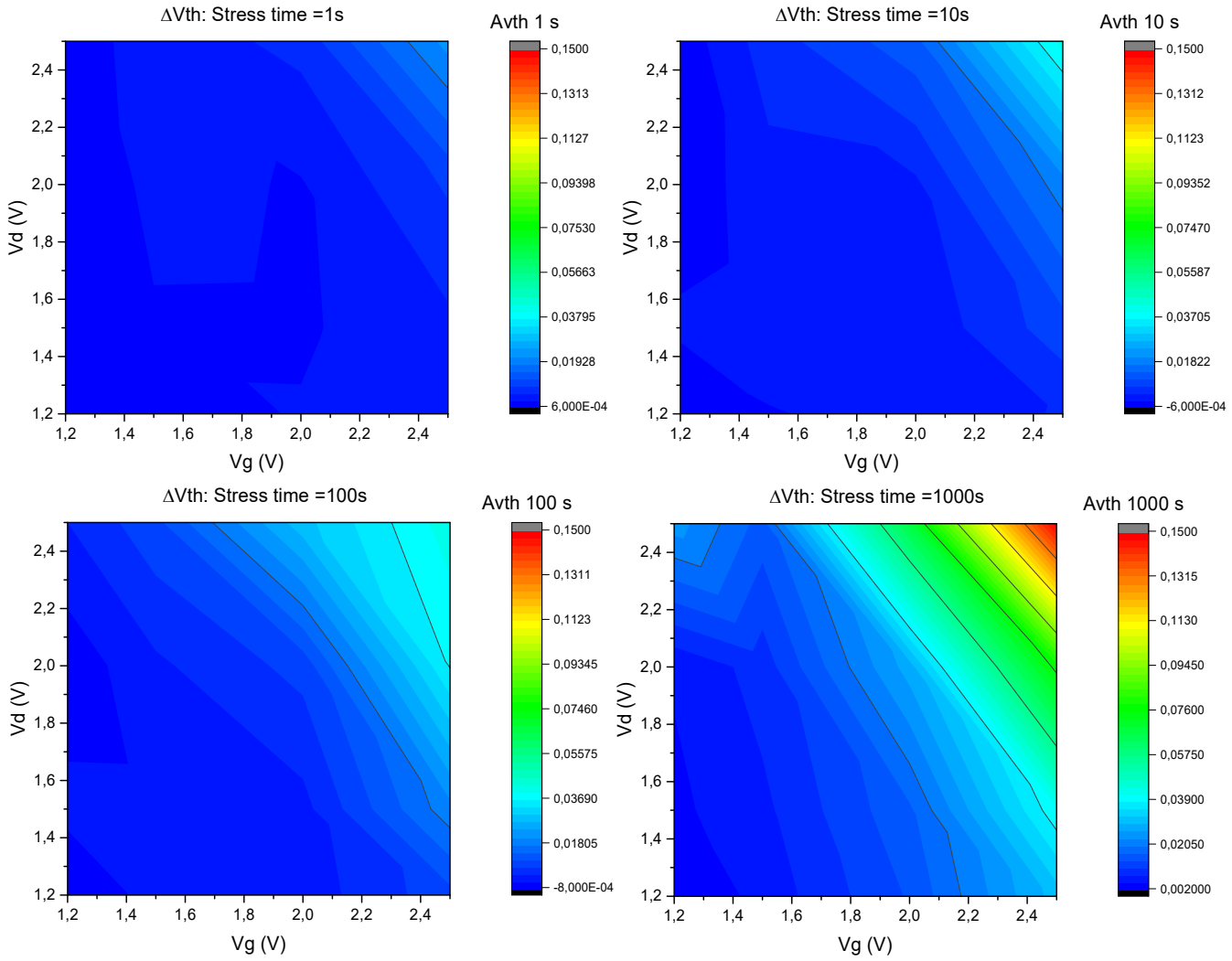

Figure 3.14: ΔVth evolution depending on the stress time and the applied stress conditions

The following fig. 3.16-3.19. shows an example of the parameter results for 100 s for the case of BTI type defects. In the case of the number of BTI defects that appear in each device, the results show a higher dependency on Vg than on Vd, and as expected higher stress translate to higher number of defects. On the other hand, in the case of the current jump that those defects create, it can be observed that the base current jump obtained on a previous work [81] where the devices were only stressed in Vg is much more precise due to that work having a 786 device per stress condition, making that study much more statistically precise. Despite that, the data obtained on this work shows that the mean current jump are still concentrated around the same value of around 350 nA but with more statistical dispersion. This leads this team to believe that the created defects are of the same type as the ones of the previous work and. This behavior appears in all the different stress times, that show a progressively more degraded as the stress time increases.

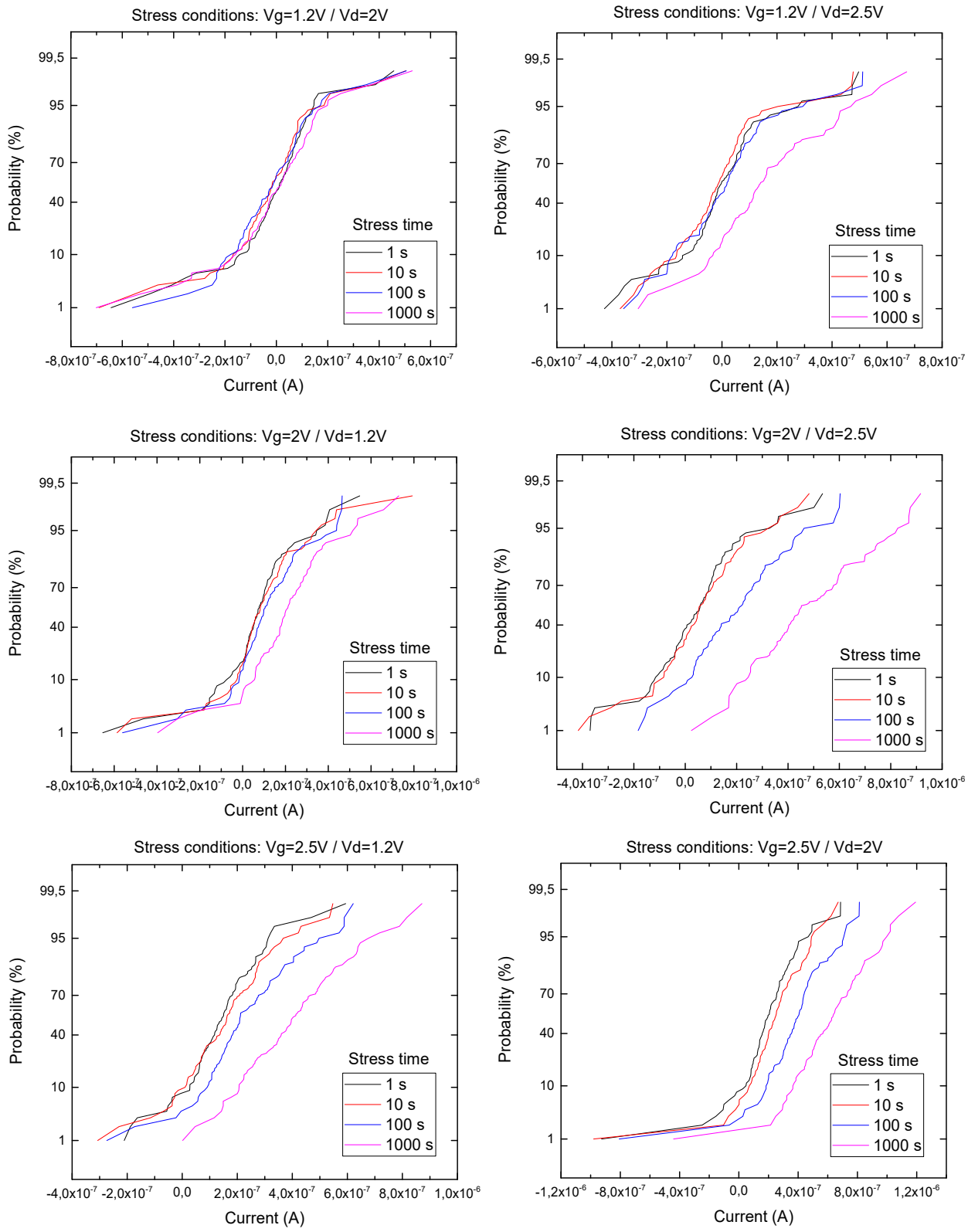

Figure 3.15: Sets of CDF corresponding to each of the analyzed stress conditions and showing each stress times applied.

In the case of RTN (fig. 3.20) as the experiments performed during this study are more dominated by BTI defects than the base RTN defects the results don't show a clear pattern as the number of RTN defects is not statistically significant enough to show reliable

results. This could be solved by analyzing a higher number of devices for each of the experiments. Only the stress conditions of Vg=1.2V and Vd=1.2 V would have a higher RTN influence, but if we observe the CDF corresponding to these conditions, both BTI and RTN can be observed.

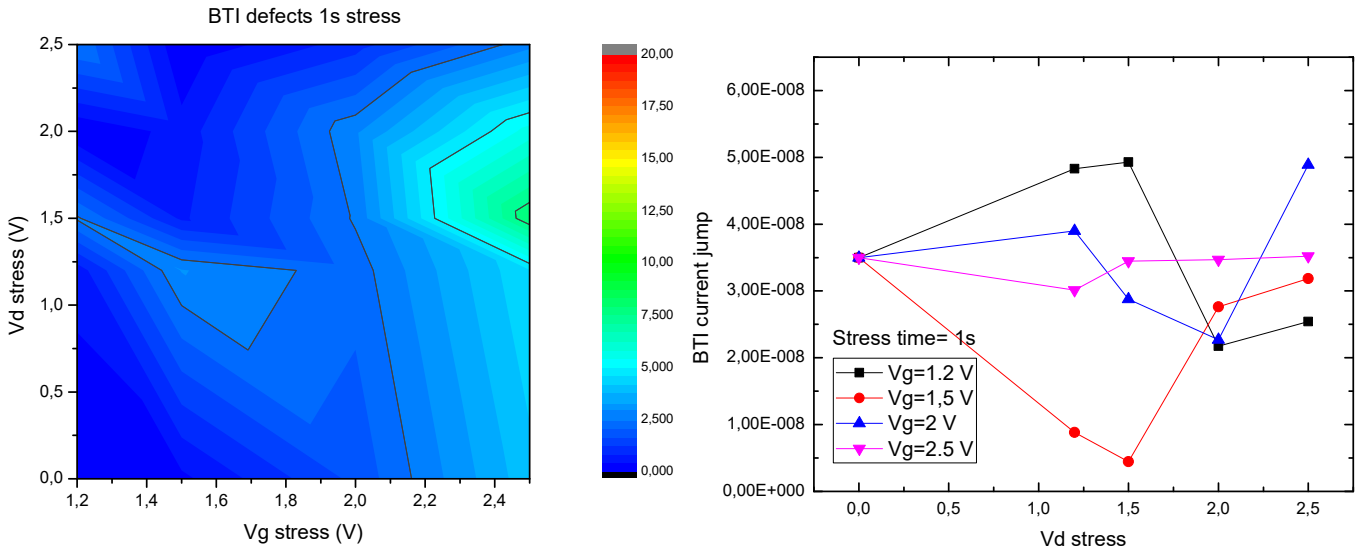

Figure 3.16: BTI parameters extracted with the proposed method for 1 s stress. (left) Mean number of defects. (Right) Mean current change.

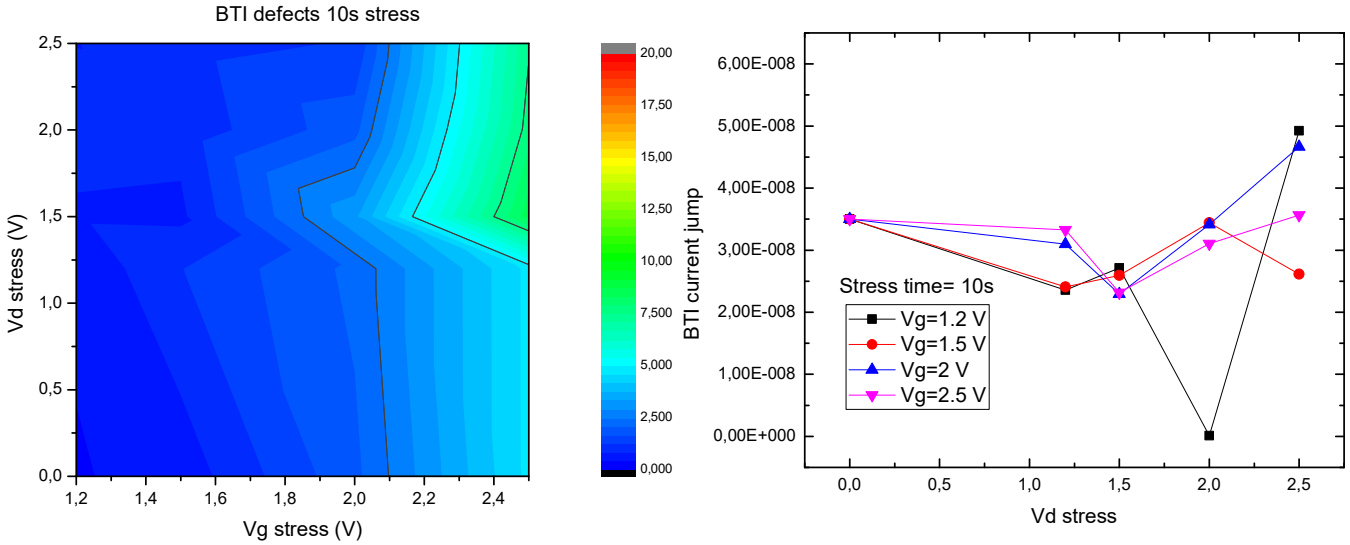

Figure 3.17:BTI parameters extracted with the proposed method for 10 s stress. (left) Mean number of defects. (Right) Mean current change.

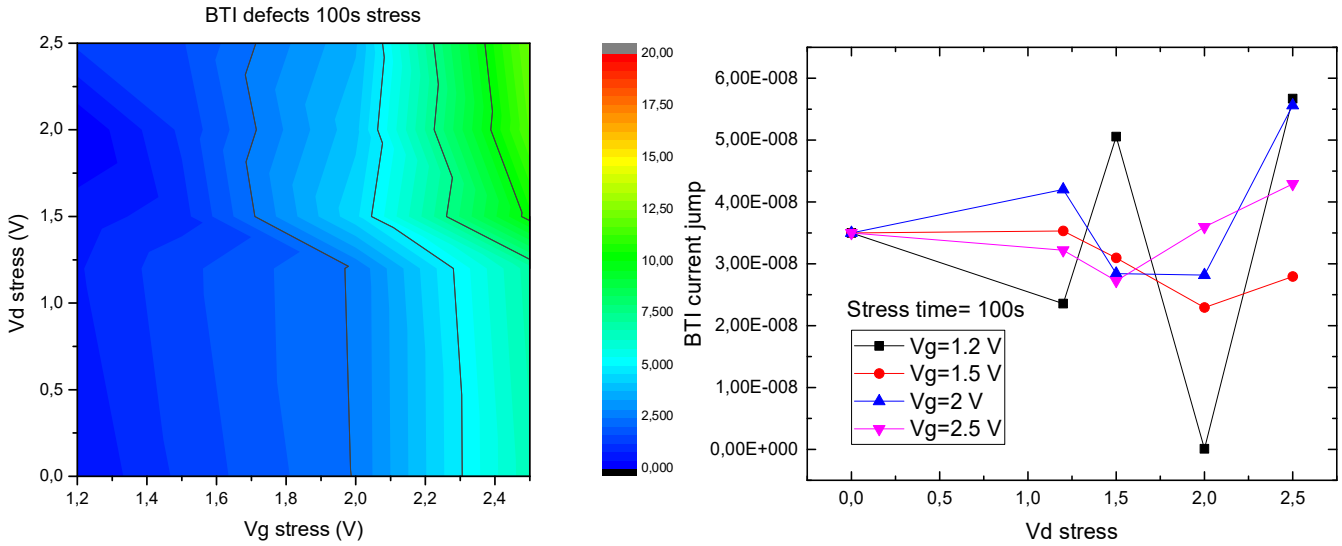

Figure 3.18: BTI parameters extracted with the proposed method for 100 s stress. (left) Mean number of defects. (Right) Mean current change.

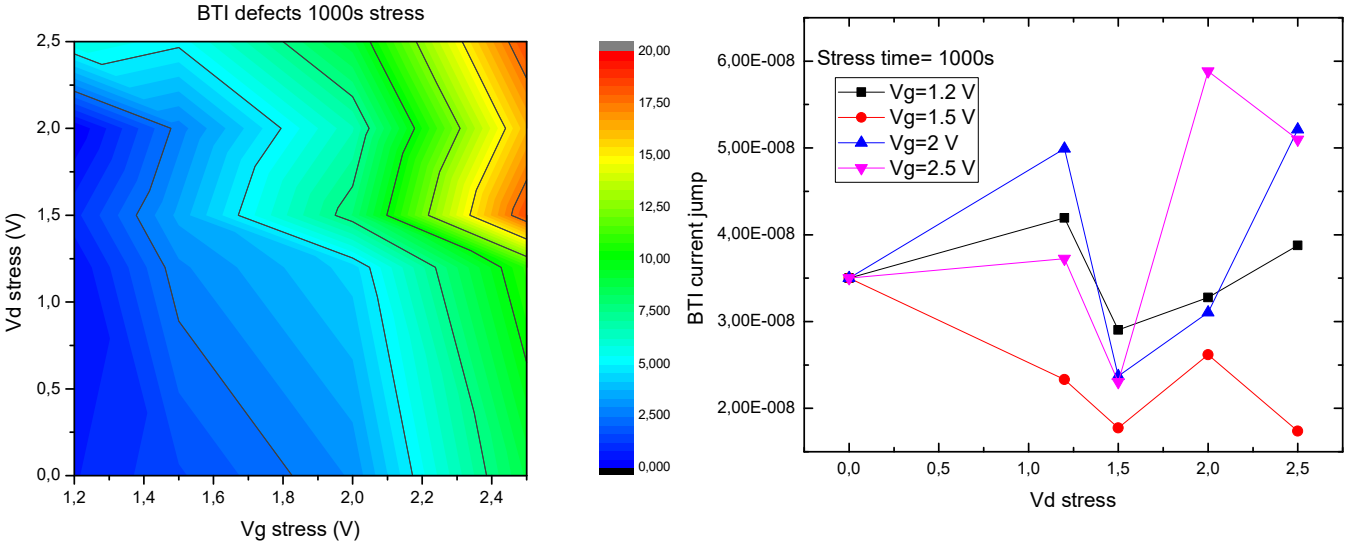

Figure 3.19: BTI parameters extracted with the proposed method for 1000 s stress. (left) Mean number of defects. (Right) Mean current change.

Fig. 3.14 shows that the threshold voltage is affected by both Vg and Vd almost the same way, but in case of the number of defects that appear, this is not the case. The number of created BTI defects (fig. 3.16-3.19 left) is dominated by the value of gate stress voltage and less influenced by the drain stress voltage, although not negligible.

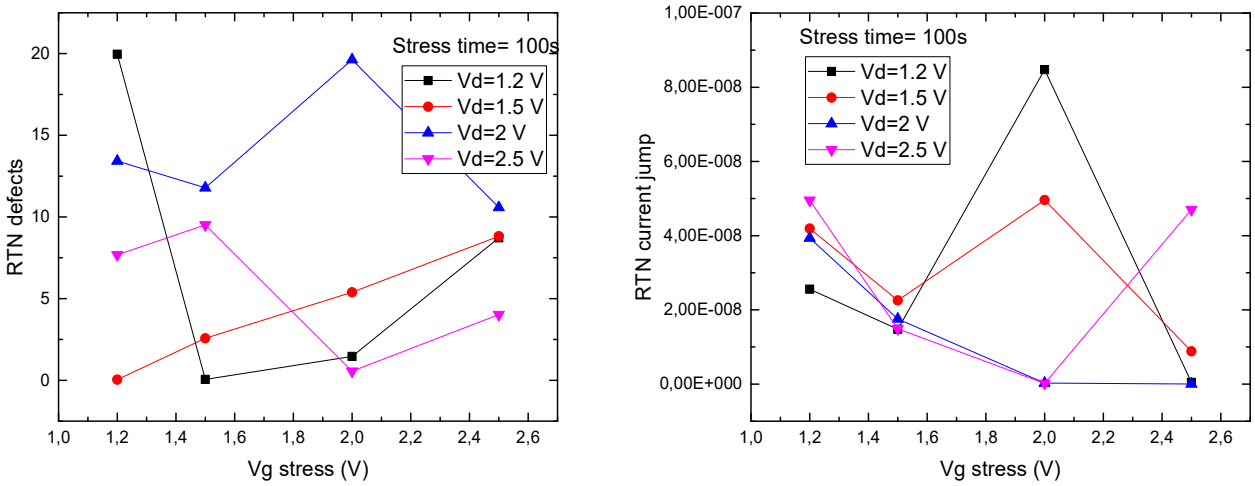

Figure 3.20: Example of RTN parameters extracted with the proposed characterization method. (left) Mean number of defects. (Right) Mean current change.

Observing the mean BTI current increase (fig. 3.16-3.19, 3.20) fluctuating around the same value due to the statistical error, it can be concluded that the defects created by the different stress follow the same statistics in every stress condition.

In the case of the RTN effect, due to the stochastic nature of this characterization method and the domination of the BTI effect on most of the studied stress conditions, the significance of the RTN parameters is almost negligible, appearing almost randomized between the studied values. But in order to obtain fitting simulated CDFs, the RTN portion of the eq. (1) when creating the simulated CDF is absolutely necessary, as making the simulation without these parameters makes the simulated CDF to have a higher discrepancy with the experimental data.

3.5– Long time RTN experiments

With the help of both the parallelization of the measurements thanks to the proposed characterization method and the parallelization on the stress that the use of the ENDURANCE chip allowed, a new set of experiments with the aim of performing a long time RTN characterization were designed. These experiments will be described, and the results will be analyzed during this section.

The biasing experimental conditions used in these experiments is shown in table 3 alongside an extra experiment using Vg=0.8 V and Vds=0.1 V later explained. Those conditions have been applied to sets of 100 devices and it must be poined that all the applied voltages are within the operation values of the studied devices. Each of the described experimental conditions have been applied to the devices under test with cycles of a 10 s measurement with a gate bias of Vg=0.6 and drain bias Vd=0.1 followed by a period where the biasing conditions in table 3 are applied but not measured with durations of 1 s, 10 s, 100 s, 1.000 s, 10.000 s, 100.000 s similarly to what the MSM measurements described at the start of this chapter and used during the aging experiments. Although the

process is similar, as all the bias conditions are under operational specifications it can't be referred to as stress periods.

During these experiments both the stress and the measurements have been parallelized. Although the measurement time could be reduced even more when using the proposed characterization method, 10 s measurements were chosen as a save option and to be able to see if the measurements were performed correctly.

Biasing conditions	Vg=1 V	Vg=0.8 V
Vd=0.6 V	x	x
Vd=0.8 V	x	x
Vd=1 V	x	x

Table 3: Experimental conditions used during the RTN long time experiments.

A quick calculation can be made regarding the time used in these experiments compared to the time that these experiments would use when performing them with a traditional RTN measurements. For the traditional RTN measurements the calculation of the experimental process time would be Tp = Time*Ndev = 100.000 s *100 =10.000.000s = 115.74 days of measurement time, where Ndev is the number of devices. This would be assuming that only a 100.000s measurement is applied and not all the other time periods. If the calculations are made for all the different time intervals, the Tp=128.6 days instead. These times make these experiments practically impossible due to its length. On the other hand, when we calculate all the experimental time necessary when applying both parallelization on non-measurement biasing and on the measurements used in these experiments the process time becomes: $Tp=Tm+(Ndev+Nc)\cdot t$ = 111111s+(100+6)*10s=31.16h=1.3 days where Nc is the number of cycles (6 in the case of these experiments) and Tm the studied time difference (T1-T2) and t is the time measured (10s measurements).

As it can be clearly seen with the results of these simple calculations, experiments that would last approximately third of a year lasts less than a day and a half, making the proposed characterization method a very useful tool and extreme time saving process.

All the experimental CDFs shown in fig. 3.21. represent the ΔID between the first measurement performed and each of the measurements performed after each non-measurement period. As it can be seen, most of the experiments show a tendency where an ID shift appeared after the 100 or 1000 s periods, showing a clear BTI behavior. Although the experimental conditions applied to these devices are within the operational parameters, the appearance of the current shift attributed to BTI indicates that the number of active defects is increased even when the devices function under operation conditions.

Table 4 show and example of the resulting RTN and BTI parameters for the experiment of Vg=1V and Vd=1V when the proposed characterization method was applied. The obtained parameters show a clear correlation with the observed behavior of the CDFs, where the lower times show a clear RTN dominated behavior and the following longer times show a clear BTI dominance. With the appearance of BTI, the minimum RTN parameters become unreliable as RTN is no longer dominant. This shows as the evolution of the parameters for RTN shown in this table have no apparent correlation and the performed fitting show no clear minimum during the proposed characterization method.

The rest of the biasing conditions have a very similar behavior having lower number of defects when the conditions on Vg and Vd are lower.

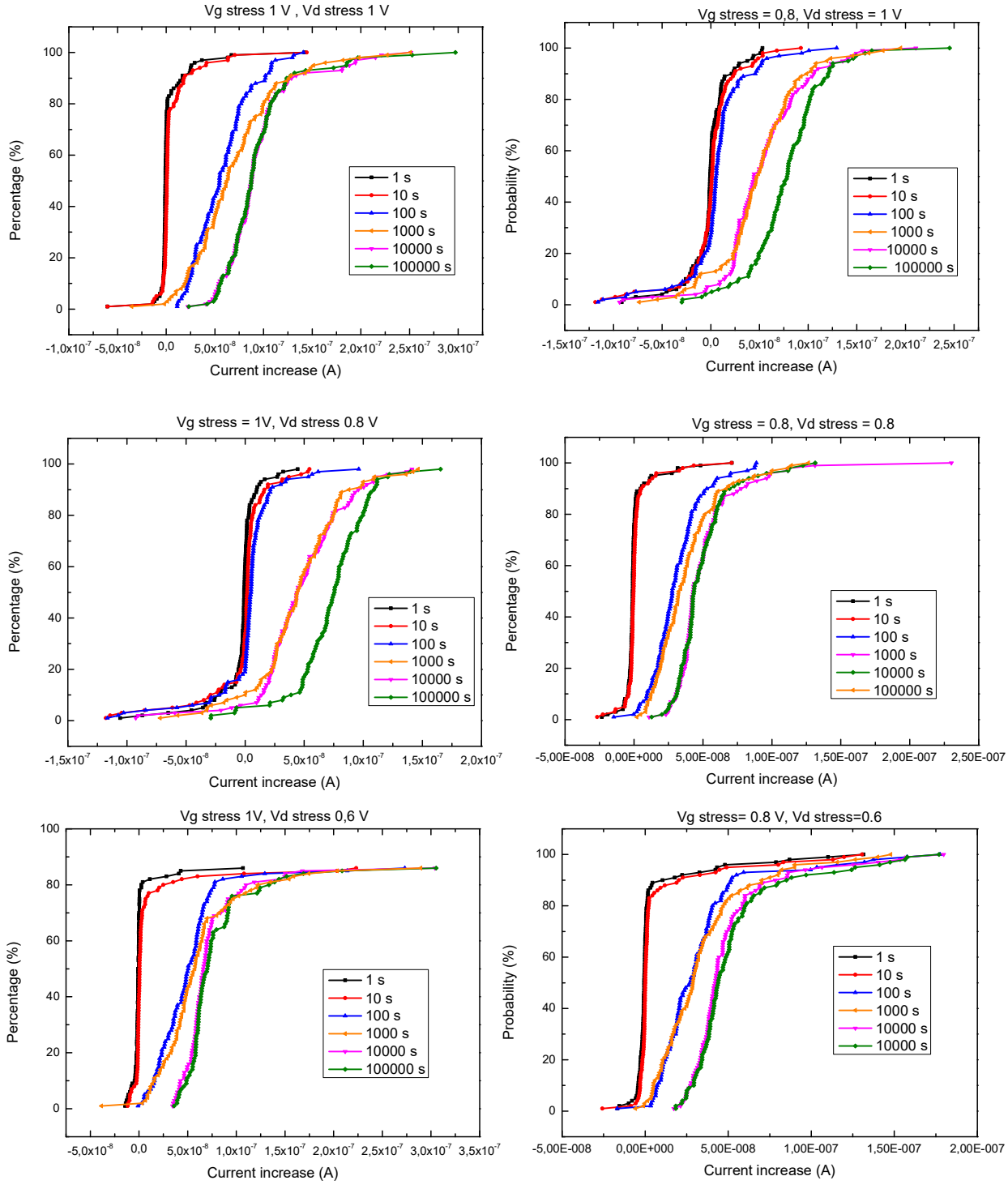

Figure 3.21: Experimental CDF of long time RTN experiments.

Time	<N> RTN	<η> RTN	<N> BTI	<η> BTI
1	1,2249	1,1233E-8		
10	1,3122	1,4965E-8		
100	0,7401*	4,094E-9*	4,7617	1,1882E-8
1000	0,0048*	1,0913E-8*	5,3592	1,3515E-8
10000	0,1306*	4,9933E-8*	7,0864	1,2474E-8
100000	1,95*	8,8438E-11*	7,4347	1,2515E-8

Table 4: Example of the resulting parameters of the experiments with Vg=1V and Vd=1V. the RTN parameters marked with an asterisk correspond to the characterization where no clear minimum is observable, due to BTI being the dominant effect.

An extra experiment was performed with Vg=0.8 and Vd=0.1 in order to observe the resulting RTN when the Vd becomes the same value as the performed measurements. As it can be seen in the CDFs shown in fig. 3.22 these experiments show almost nonexistent BTI behavior and a similar behavior during the studied time intervals. This effect is reflected on the parameters shown in table 5 that show a clear RTN dominance with a low BTI appearance.

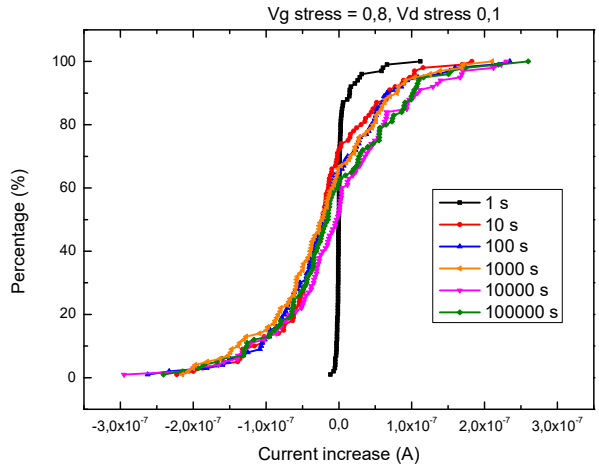

Figure 3.22: Experimental CDF of long time RTN experiments at Vg=0.8V and Vd=0.1V.

Time	<N> RTN	<η> RTN	<N> BTI	<η> BTI
1	2.4376	3.1419e-09	-	-
10	9.5648	2.6226e-08	-	-
100	8.7624	3.1487e-08	-	-
1000	6.6856	4.0836e-08	0.4058	3.9710e-08
10000	10.6402	2.9476e-08	1.0288	1.8549e-08
100000	8.7977	3.3118e-08	2.5723	1.2142e-08

Table 5: Example of the resulting parameters of the experiments with Vg=0.8V and Vd=0.1V. In the case of these experiments, the devices show a dominance of RTN with the small appearance of BTI for longer times.

With the results obtained during these experiments some observations can be made. Firstly, the experiments performed in this section have been experiments that would be unfeasibly long if both the non-measuring period and the measurements were not parallelized. This proves that the proposed characterization method shows great promise

when statistical characterization on a great number of devices and in great lengths of time is needed.

The second observation to be made, for these experiments, even though the devices were being operated under nominal bias parameters, they show BTI behavior when the times are long enough. The experiments also show that decreasing the drain bias during the non-measuring periods translates into a significantly lower appearance of aging effects as seen when comparing the experimental CDFs and its parameters.

Finally, even though these results are useful, new experiments for a deeper characterization of the behavior of the studied devices can be designed in the future to further information on their reliability and aging degradation.

3.6 – Conclusions

On this chapter the proposed characterization method presented in chapter 2 has been expanded on to take in to account aging mechanisms, more specifically BTI and HCL. The expansion of the method has been described and applied to a wide range of experimental conditions.

Firstly a pure BTI experiments with a wide range of gate stress voltage have been described and analyzed using the expanded proposed method. The resulting parameters evolution depending on stress voltage, stress time, relaxation time have been obtained and analyzed. Also a kinetic adjustment to the results have been applied to describe the evolution of the studied devices parameters over the BTI relaxation time. The current shift obtained in these experiments show almost the same values as the ones obtained during the RTN characterization, making the assumption that the RTN and the BTI defects have the same physical origins be reinforced.

After these experiments, the same method has been applied to characterize a set of 38 FD-SOI devices. The results showed that even though the number of studied devices is not that high, the resulting parameters show the expected behavior although they have a relatively high variability. Although this characterization is useful as a proof that the proposed method is usable for multiple technologies, to obtain a higher quality characterization the number of studied devices would have to be increased.

Following this section, the following section presented several experiments to characterize the coexistence of both BTI and HCI have been presented. These experiments cover a wide range of experimental conditions utilizing the flexibility of the 60nm CMOS transistors present on the ENDURANCE chipset. The results show that the devices have the highest degradation under the stress conditions Vg=Vd but the number of aging defects is dominated by the gate stress bias. Similarly to the BTI results, the current shift that BTI and HCI cause are still around the same value as the RTN experiments but with higher variability. This could have several different origins, like the HCI defects having a wider range of current shifts or that the inclusion of Vd stress could affect the reflected characteristics of those defects.

Finally, on the last section of this chapter, a set of long time RTN experiments have been presented for several conditions. These experiments would have lasted more than 120

days if they were performed using the traditional methods, but with the use of the measurement parallelization that the proposed characterization method allows, the +120 days are reduced to 30 h. Apart from the time saving demonstration, this measurements showed the appearance of BTI defects even when performing under nominal operation conditions. As an extra experiment was performed with a reduced Vd value, it can be seen how the experiment with those characteristics show a significantly lower number of BTI defects and they appear at later execution times. Although these last experiments show some promising results, more data is necessary and new tests would have to be performed.

Summary and conclusions

From the initial invention of transistors to the nowadays nanometer sized devices, the CMOS industry have been advancing at a faster and faster pace during the last decades. The dimensions downscaling trend to achieve a higher device density allowing the increase of computational power without increasing the chip size has been the basis for this rapid growth. This scaling trends contribute in many factors like reducing the power consumption, manufacturing cost, increasing processing speed, etc. Nevertheless, the scaling trend also has its negative caveats. As devices size approach the lengths of the atom, effects like increasing variability between identically designed devise, appearing variations over time of higher current leakage can pose a threat to the correct operation of CMOS transistors. For this reason, CMOS variability and reliability in nanoscale devices have been one of the focuses of the last decades.

In this scenario, this thesis continued the efforts in the study of time dependent variability phenomena in nanometric CMOS. The main contribution of this thesis is the development of a characterization method that aims to reduce the experimental and computational time required when characterizing variability effects. This thesis studies were focused to the following variability effects: Random Telegraph noise (RTN), Bias Temperature Instabilities (BTI) and Hot Carrier Injection (HCI). In this context, Chapter 1 described the fundamentals of these variability phenomena. Furthermore, this chapter reports the characteristics of the devices present in an array-based IC (ENDURANCE) used in this thesis together with the full experimental methodology developed by this group (REDEC) especially designed for the statistical characterization in a high number of devices and the stress parallelization on aging experiments.

The presented ENDURANCE IC was designed in previous works in order overcome the extremely long experimental times that on-wafer measurements entail, and at the same time allow the accurate and systematic characterization for a high number of devices under test. This makes the presented experimental set-up the perfect choice to perform high quality statistical characterization of variability phenomena.

The second chapter of this thesis is focused to the description, analysis and validation of the proposed characterization method involving RTN characterization. The presented method is based in the statistical reproduction of a distribution of current shifts appearing between two instances of time in the drain current of the set of studied transistor device. To validate the usability of this method, a traditional full current trace analysis, Weighted time lag plot (WTLP), have been used to compare the resulting statistical parameters.

The use of the proposed method allows for the reduction of experimental and computational times. The experimental time reduction comes from the ability to only measure the current of your devices under test at the two different instances, instead of a full current over time measurement that traditional methods like WTLP need. For this reason, the proposed method allows for the parallelization of the measurement processes, making long time experiments that would be traditionally unfeasible become easily implemented. Furthermore, the computational time necessary to analyze 2 points of data per device (two instants), when compared to thousands of data point when using traditional method, is highly diminished, making the proposed method a very efficient alternative. The results demonstrated that the proposed methos achieve a very similar final statistical parameters than the traditional WTLP method.

This chapter also performed several evaluations on the method involving a mathematical framework based on probability, a study of parameter variability depending on number of studied devices and the time difference between the two instances used with the method.

To complete the set of mentioned variability phenomena, the third and last chapter of this thesis focused on two main things: firstly the expansion of the proposed method, that originally only took in to account RTN, to include aging mechanisms like BTI and HCI, secondly the use of the proposed method to characterize several experiment involving a wide range of biasing conditions, experimental times and also includes some experiments performed to on-wafer FD-SOI devices.

The first section of the chapter describes the necessary changes applied to the original proposed method in order to include the current reduction that our devices would suffer under higher than nominal operation conditions causing stress aging. This method is then applied to characterize a set of experiments involving BTI experimental conditions, ergo only gate stress. The expanded method has proved to be able to reproduce the experimental results with great accuracy and a study of the evolution of the extracted parameters involving the stress time and the relaxation time was performed and analyzed. A simple kinetic model has been presented to adjust the evolution of the parameters over the relaxation time. During these experiments the current shift values that the detected BTI defects cause appears to be very similar to the previous RTN experiments, making the overall premise that both them have the same physical origin corroborate this results.

The next set of experiments presented in chapter 3 are the experiments involving FD-SOI devices under nominal operation conditions. As these devices measurements are performed on-wafer one by one, only a set of 38 devices were analyzed during these experiments under several biasing conditions. The resulting parameters showed that even though the number of studied devices is not high enough to get a clear statistical representation, the resulting parameters show the expected behavior although with a higher parameter variability. Although this characterization is useful as a proof that the proposed method is usable for multiple technologies, to obtain a higher quality characterization the number of studied devices would have to be increased.

Following these tests, a set of experiments involving the coexistence of BTI and HCI were presented. These test involve sets of 100 devices for each of the extensive number of aging biasing conditions and stress times. As expected the highest degradation

appeared for conditions where Vgs=Vds, as this conditions maximize the appearance of HCI. Although the characterization method does not allow the user to distinct between a current shift originated by a HCI event or by a BTI defect, the statistical characterization of this current shift is still relevant and is able to reproduce experimental data with the same accuracy. Similarly to the BTI only experiments, the current shift values are still around the same value as the ones obtained during RTN experiments but appear to have higher variability.

Finally, the last experiments presented in this thesis involved RTN measurements for a long time with several biasing conditions. A simple calculation of the time needed to perform these experiments with a traditional method showed a reduction of experimental time from around 120 days to a merely 30 h. Furthermore, the results analysis show that the studied conditions favored the appearance of BTI defects and most of the analyzed conditions show a BTI current shift after 100s or 1000s of experimentation. With the help of extra experiments, this appearance is attributed to the use of higher Vd values in tandem with the applied Vg than in other experiments, and as Vd is reduced, the number of appearing BTI current shift is reduced drastically when under nominal operation conditions. Although these experiments results have been analyzed, more experiments would have to be designed in the future to achieve a better understanding of these effects under long time experiments.

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