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Dual-Gate OTFTs and Multiplexer Chips: Advancing the Next Generation of Flexible EG-ISFET Sensor Chips

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The undersigned Prof. Dr. **Jordi Carrabina Bordoll**, from the Department of Microelectronics and Electronic Systems, of the Universitat Autònoma de Barcelona,

CERTIFY

That the dissertation entitled “Dual-Gate OTFTs and Multiplexer Chips: Advancing the Next Generation of Flexible EG-ISFET Sensor Chips” has been written by **Ashkan Rezaee** under their supervision, in partial fulfillment of the requirements for the degree of Doctor of Philosophy.

And hereby to acknowledge the above, sign the present

Signature **Jordi Carrabina Bordoll**

Barcelona, Spain, 20th June 2023.

Declaration

I hereby declare that, except where specific reference is made to the work of others, the contents of this dissertation are original and have not been submitted in whole or in part for consideration for any other degree or qualification in this, or any other University.

Ashkan Rezaee

June 2023

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WOMAN, LIFE, FREEDOM

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Chapter 1. Motivation and Objective

The advent of semiconductors has transformed human existence through the introduction of modern electronic devices and systems [1], [2]. These semiconductor devices have revolutionized almost all application domains, where they serve as fundamental components for computation, sensing, control, automation, communication, storage, and energy, among others[3]–[7]. The progress in fabrication techniques has enabled the miniaturization of semiconductor devices, resulting in compact, powerful, intelligent, and cost-effective systems. These advancements have facilitated scalability and the convenient deployment of field-ready solutions, ultimately realizing the potential of Internet of Things (IoT) applications at an unprecedented scale [8]–[11].

Notably, silicon metal-oxide-semiconductor field-effect transistors (MOSFETs) have emerged as pivotal building blocks within these systems [12]. The continuous scaling of MOSFETs in accordance with empirical Moore's law has presented the integrated circuit (IC) industry with both remarkable challenges and promising opportunities [13], [14]. This progression has enabled a doubling of transistor density approximately every 18 months. Consequently, it has spurred the development and evolution of complementary metal-oxide-semiconductor (CMOS) based systems, which offer low power consumption, high-density ICs, and high computational speed [15], [16].

The exploration of semiconductors as a foundation for the advancement of sensors and transducers has captivated the interest of researchers [17], [18]. Through the utilization of microfabrication and nanofabrication techniques, sensor arrays have been developed, encompassing mechanical [19]–[21], chemical [22], [23], optical [24], [25], thermal [26], magnetic [27], acoustic [28], and numerous other sensing modalities. These sensors find applications in various domains, including automobiles, smartphones, biomedical devices, and environmental monitoring, to name a few [29], [30].

Optical computational systems, despite their high sensitivity, suffer from limitations such as high cost, large size, and the requirement for sophisticated instruments, making them challenging to promote or integrate into portable devices [31]. However, these limitations are not inherent to optical computing and can be addressed by further research and development [32], [33]. On the other hand, the classic three-electrode system, which utilizes potentiometric and amperometric methods, offers advantages including high sensitivity and low cost. However, the mass production and integration of the three-electrode system into other systems pose difficulties due to the lack of a unified manufacturing standard [34]. To address these challenges, the ion-sensitive field-effect transistor (ISFET) has garnered significant attention since its introduction in 1970 [35]. The ISFET technology presents a promising solution by offering a balance between sensitivity, cost-effectiveness, and ease of integration.

ISFETs represent a class of potentiometric sensors where the ion-sensing membrane is directly integrated onto the gate region of a field-effect transistor (FET). FETs, as solid-state active devices, possess favorable characteristics including high-input impedance and low-output impedance, making them suitable for investigating charge accumulation across the gate oxide and translating

it into a measurable electrical current through the modulation of the conducting channel at the semiconductor-oxide interface. The use of ISFETs offers several advantages, including compatibility with complementary metal-oxide-semiconductor (CMOS) analog and digital circuits, low power consumption, rapid response, miniaturization capability, and ease integration with readout and communication circuits.

When monitoring electrochemical reactions, ISFET has various benefits. ISFET can be mass-produced and further integrated into various sensing systems [36], [37]. Second, ISFET has a bigger size advantage over the three-electrode system since it only needs one reference electrode (RE) to perform chemical assays. As an all-solid-state sensor with no delicate components, ISFET is thus robust to acid, alkali, and water as well as being crash- and water-resistant in real-world applications[38]–[40]. Finally, ISFET is simple to use and has the following operating principle.

The ISFET and RE make up the entire sensor system. Source, Drain, and Gate are the three terminals that make up an ISFET. The RE supplies the bias on the electrolyte and the insulated gate. Meanwhile, by applying a voltage to the RE, the switching of the conduction channel can be modified. The channel current can then be affected by the drain voltage. Particularly, the positive charges near the gate substrate travel downward when a positive voltage is applied to the RE, leaving the negative charges behind. The substrate's negative charges are drawn to rise upward at the same time. A conductive channel can form between the source and drain as a result of this charge accumulating under the gate. The threshold voltage corresponds to the voltage at which the channel forms. Negative charges will then create a drain current (I_{DS}) in the direction of the voltage when a low voltage is placed between the source and drain. The voltage on the RE creates an internal electric field that controls the conductivity of the channel by regulating the quantity of charges in the channel since the gate bias during the turn-on phase can modifies I_{DS}.

When the ISFET is submerged in an electrolyte, the surface hydrolysis of the gate dielectric layer will vary due to the ion concentration in the solution, and this will affect the threshold voltage and the current of the ISFET[41], [42]. The depletion or accumulation of carriers in the channel will then depend on how the potential distribution on the gate surface changes. The ISFET's electrical output can fluctuate and reflect the process [43]. Electric signals can therefore be used to track the electrochemical processes taking place in the electrolyte. For instance, Si_3N_4 can absorb H^+ when employed as the ISFET gate because the surface hydroxyl groups can react with H^+ and produce a redistribution of charge on the ISFET gate. The ISFET's threshold voltage will change as a result of the change in charge distribution, which will modify the current I_{DS} and can be reflected in the ISFET's electrical output through external circuits. ISFET, an electrochemical sensor that has just been developed, has the advantages of compactness, low cost, all-solid construction, high sensitivity, and simplicity of operation. ISFET is now one of the primary branches of modern sensors, and its success is a result of the collaboration of research organizations around the world.

1.1 Background and motivation

The transducer and sensing element that make up the ISFET sensor have a well-established history of development. FET devices, initially introduced by Julius Edgar Lilienfeld in 1925, are the

ancestors of the ISFET idea. Depending on the gate construction, there are many types of FETs, such as junction FETs (JFET), metal-semiconductor FETs (MESFET), and insulated gate FETs.

W. Shockley proposed the first JFET in 1952[44]. Two heavily doped p-type areas are used to create JFETs on an n-type semiconductor. Gate is the name of the electrode that is taken from the p-type area. The drain and source electrodes are taken from the two ends of the n-type semiconductor. The JFET is a double p-n junction that controls the conductive channel and depletion layer using the gate voltage and drain voltage. As a result, the channel's conductivity will alter, which the external circuit reflects.

In order to facilitate simpler fabrication procedures and increase working speed, Metal Semiconductor Field Effect Transistors (MESFET) was also accomplished using a metal-semiconductor junction to replace the p-n junction of JFET [16]. High-frequency applications frequently use MESFETs. These transistors are made up of source and drain terminals, a semiconductor layer, and a metal contact. The properties and behavior of MESFETs have been examined in a number of research[45], [46]. In contrast to MESFET, the representative insulated gate FET was first developed by Mohamed M. Atalla and Dawan Kahng at Bell Lab in 1960 to address the issue of "surface state" that can be reduced by a sandwich structure of metal (M)-oxide (O)-semiconductor (S), namely the well-known MOS structure. This structure uses a metal with an insulated layer (such as SiO_2) below to fabricate the gate[17]. However, due to its slow operation and susceptibility to damage in the early stages, the true value of the MOSFET as a signal transducer with advantages such as low cost, easy fabrication, and integration into large-scale circuits was only realized after a few years [47]. Recognizing the advancements in MOSFET technology, Piet Bergveld preserved the structure of the MOSFET transducer and further expanded its application in ion sensing. This was achieved by eliminating the metal gate of the M-O-S structure, enabling direct contact between the solution and the oxide layer for linear detection of ions. In 1970, the world's first ISFET sensor achieved quantitative detection of Na^+ through the output of drain-source current (I_{DS}) [48]. Upon removing the metal gate from the oxide-semiconductor structure, it becomes possible to immobilize an additional sensitive film on the oxide layer, enabling the detection of various types of ions and molecules. This leads to the formation of the widely recognized classic ISFET structure, with the sensing film typically serving as the gate. The choice of gate materials on the sensing film plays a crucial role in determining the sensing performance of the ISFET. For instance, in the detection of H^+ ions, depositing different sensitive films (such as Si_3N_4, Al_2O_3, Ta_2O_5) onto the insulating oxide layer can alter the sensitivity of H^+ from 25 to 55 mV/pH, indicating a broad range of detection capabilities [49]. The successful explanation of this phenomenon is provided by the site dissociation model proposed by Bousse et al. in 1983 [50]. Furthermore, by replacing the sensitive film materials of the gates, the detection of ions other than H^+ can be expanded.

By leveraging the extensive research on ionic detection using ISFET, the capabilities of this technology were further extended to detect other types of analytes, including gases and biomolecules, through the versatile design of the ISFET gate. In 1975, a significant breakthrough was achieved as an ISFET with a gate composed of a noble metal successfully detected gases for the first time [51]. Subsequently, in 1980, Steve Caras and Jiri Janata reported the identification of

the biomolecule penicillin through enzymatic reactions using ISFET [52]. This paved the way for the establishment of numerous ISFET-based biosensors. For instance, since 1983, urea detection has been accomplished using various functional materials, such as acetylcellulose, polyvinyl alcohol, and albumin, immobilized on the ISFET gate [49].

The sensor's size was further optimized in 1984 when Jun-ichi Anzai et al. developed a miniature urea sensor based on enzymatic functionalities on the ISFET gate [53]. Additionally, the practicality of the sensor was examined by detecting urea in human serum, employing improved enzymatic modification techniques on the gate [54]. In 1985, Yuji Miyahara et al. enhanced the sensor's anti-interference performance, enabling simultaneous detection of urea and glucose with minimal interference [55]. Thus, the initial applications of ISFET in gas and biomolecule detection were successfully validated. Subsequent developments of ISFET sensors focused on clinical applications, with an emphasis on detecting glucose, DNA, antibodies, and cells [56]. For instance, in 1996, Vjacheslav Volotovsky et al. expanded the dynamic detection range of glucose by enzymatically modifying the ISFET gate [57]. In 2002, Maya Zayats et al. developed a novel immunosensor by forming an antigen-antibody complex on the ISFET device [58]. In 2006, Sunil Purushothaman et al. reported a new method for identifying nucleotide polymorphisms using ISFET sensors [59]. Furthermore, in 2008, Gonçalves et al. utilized amorphous silicon-based ISFETs for label-free detection of DNA hybridization [55]. These pioneering works demonstrated the versatility of ISFET sensors, expanding their scope from ionic detection to biochemical sensing and showcasing their potential for practical clinical applications.

One notable issue with ISFETs is their vulnerability to Electrostatic Discharge (ESD), a common risk that can have catastrophic consequences and cause irreparable damage to the device or microchip. ESD refers to the sudden and rapid flow of a high current through electronic components, typically occurring within a very short duration of time. This discharge can result from an accumulation of static electricity and poses a significant threat to the dependability and reliability of electronic components.

In everyday life, ESD is a common occurrence. When two different-charged objects are near one another, the electric field either causes the insulating medium between them to break down and create a conductive path, neutralizing the charge transfer, or the different-charged objects directly contact one another, neutralizing the charge transfer.

When a conductive path is created, ESD happens [60]. The human body can be electrified in daily life because to the fact that it is an electrostatic conductor and that shoes and socks are typically constructed of materials that act as an electrostatic insulator, allowing the electrified human body to temporarily store its electric charge. When two persons with different sorts of charges come into contact, a conductive path is immediately formed, the charges are neutralized, and the human body is directly affected, causing tingling, which is also a type of ESD occurrence. The equivalent capacitance and discharge resistance of the human body are each about 100 pF and 1.5 kΩ[61], respectively. The charged human body will produce an instantaneous discharge current of ampere (A) level in hundreds of nanoseconds when it comes into touch with other items and creates a conductive route (ns) [62].

Without adequate safeguards, a transitory current acting directly on a chip or other device can be enough to seriously harm it. Any stage of a device's lifecycle, from the beginning of production to the time of final use, might expose it to ESD events. ESD events take place in a matter of nanoseconds and account for a sizable portion of recorded failure rates overall.

The motivation behind this project thesis from the pressing need to overcome the limitations and challenges faced by conventional electronic devices and sensing systems. While inorganic transistors have been the cornerstone of modern electronics, their rigid nature and expensive fabrication processes have hindered their integration into emerging applications such as flexible electronics, wearable devices, and IoT sensing platforms.

Organic thin film transistors (OTFTs) are field-effect transistors comprising a semiconductor in the form of a thin, typically polycrystalline layer of conjugated organic molecules[63]. They can be fabricated at moderate temperatures and through cost-effective solution-based processes on a wide range of low-cost flexible and deformable substrates[64]. They have great potential for a wide variety of applications, especially for new products that rely on their unique characteristics, such as electronic newspapers, inexpensive smart tags for inventory control, and large-area flexible displays[63], [64].

One of the applications of OTFTs is in sensors, where they can be used to detect various physical, chemical, or biological stimuli. For example, OTFTs can be used to sense pressure, temperature, humidity, light, gas, pH, DNA, enzymes, antibodies, and more[65]. The sensing mechanism can be based on the change in the electrical properties of the organic semiconductor or the gate dielectric layer in response to the stimulus. The advantages of OTFT sensors include their low cost, flexibility, biocompatibility, and easy integration with other electronic components[65].

One of the advantages of OTFTs against ESD is that they can be fabricated on flexible substrates, which can reduce the risk of mechanical stress and contact-induced ESD events. Moreover, some organic materials have self-healing properties that can recover from ESD damage to some extent. However, these advantages are not sufficient to overcome the inherent weakness of OTFTs against ESD. Therefore, more research is needed to improve the ESD robustness of OTFTs by optimizing the device structure, materials, and fabrication processes[65]–[67].

The advent of OTFTs offers a promising solution to address these limitations by providing flexibility, scalability, and cost-effectiveness. By harnessing the potential of OTFTs and combining them with EG-ISFETs, which exhibit selective and sensitive ion sensing capabilities, we aim to develop high-performance analog MUX with enhanced sensing functionalities. This project aims to advance the field of integrated sensing systems by exploring the design, fabrication, and characterization of analog MUXs using OTFTs with EG-ISFETs, with the ultimate goal of enabling innovative applications in healthcare, environmental monitoring, and beyond. By leveraging the unique properties of these technologies, we strive to contribute to the development of more versatile, cost-effective, and efficient sensing platforms that can address real-world challenges and pave the way for a new generation of electronic devices.

1.2 Challenges and Limitations

The implementation of ISFETs integrated with MUX OTFT technology in electronic sensing systems brings forth various challenges and limitations that need to be addressed to ensure their successful deployment. These challenges encompass technical limitations, practical considerations, and potential drawbacks associated with this approach.

The first difference is that ISFETs can be implemented in a unipolar device (p-type or n-type process) while multiplexors usually need to have both types to block analog signals. We address that challenge by the use of dual-gate (p-type) OTFTs.

One significant challenge is the optimization of EG-ISFETs for reusability. While the concept of utilizing extended gates to maximize the utilization of ISFETs is promising, it requires careful design and engineering to ensure reliable and consistent performance across multiple applications. The development of robust and durable extended gate structures, as well as effective gate control mechanisms, becomes crucial to enable the reuse of ISFETs without compromising their sensing capabilities. In order to overcome this difficulty, we suggest a unique EG-ISFET design that includes a flexible and removable extended gate electrode that can be quickly replaced or cleaned after each use. In order to overcome this difficulty, we suggest using an EG-ISFET design that includes a flexible and removable extended gate electrode that can be quickly replaced or cleaned after each use.

One practical limitation is the avoidance of increasing the number of ISFETs. While the goal is to maximize the utilization of ISFETs through the use of extended gates, there may still be instances where additional ISFETs are required to meet specific sensing requirements. Balancing the need for optimal sensitivity and performance with the limitations of ISFET quantity poses a significant challenge. Therefore, efficient selection and control mechanisms, such as MUX OTFT technology, become crucial for dynamically choosing desirable ISFETs based on sensitivity or required structures. By creating a revolutionary MUX OTFT technology that can efficiently select and control numerous ISFETs, we attempt to overcome this problem. To accomplish precise switching between several ISFETs, our MUX OTFT technology takes advantage of the high mobility and low leakage current of organic semiconductors.

Additionally, the integration of parallel ISFETs introduces both benefits and limitations. While the use of parallel ISFETs provides redundancy and coverage, allowing for continued sensing even if one ISFET fails, it also presents challenges in terms of system complexity and increased power consumption. Ensuring proper coordination and synchronization among parallel ISFETs, as well as implementing efficient signal processing techniques, becomes essential to harness the benefits of redundancy while minimizing the drawbacks.

Furthermore, there may be challenges related to the compatibility and integration of ISFETs with MUX OTFT technology. The design and fabrication of MUX OTFTs that can effectively interface with ISFETs and provide reliable and accurate selection of desirable sensing elements require thorough investigation. Ensuring seamless communication and interaction between ISFETs and MUX OTFTs is critical for achieving optimal performance and functionality. We propose a novel

hybrid integration scheme to overcome this problem, integrating ISFETs and MUX OTFTs on a single flexible substrate. The problems of thermal mismatch and interfacial defects are avoided by our hybrid integration scheme, which uses a low-temperature, solution-based process that is suitable for both ISFETs and MUX OTFTs.

Overall, the challenges and limitations associated with the integration of ISFETs with MUX OTFT technology in electronic sensing systems encompass aspects such as reusability, ESD protection, ISFET quantity management, parallel ISFET coordination, and compatibility with MUX OTFTs. Addressing these challenges through innovative design approaches, advanced fabrication techniques, and robust system-level integration will pave the way for the realization of highly reliable, adaptable, and efficient ISFET-based sensing systems.

1.3 Smartkem OTFT flexible and ecofriendly technology

SmartKem is a UK company that produces organic semiconductor inks that can be used to create flexible OTFT (organic-TFT) devices with low-temperature solution processing. The company's inks include organic semiconductor, organic gate insulator, passivation layer and base layer, which are all compatible with printing methods.

Modern IC fabrication in the CMOS technology nodes requires a lot of power and has a significant environmental impact [68]. SmartKem offers a more energy-efficient and eco-friendly alternative with its organic electronics process. Moreover, SmartKem's organic electronics process involves organic materials and fewer steps than the CMOS process, which reduces the greenhouse emissions.

One of the most scalable and efficient techniques for coating large areas with minimal material loss is slot-die coating, which is widely used in display production lines. SmartKem's inks are designed for slot-die or spin coating, but they can also be adapted for digital printing (ink-jet) with further development to achieve the same high uniformity. The spin coated OTFT devices have mobilities of 2.5cm^2/Vs at short channel with low variability (<10%) and turn on voltage of +2V to +4V (on single gate transistors). The baking steps for the semiconductor and dielectric are mainly for solvent evaporation, so they can be easily reduced without affecting the performance or stability of the transistors. The technology is focused on the redesign of cross-linking chemistry of the passivation material, which can be replaced by more intense UV light exposure and lower temperature baking while the rest of fabrication steps can be changed without any measured impact and the photolithographic ones lowered in temperature with acceptable changes in dimension of processed features.

It has recently demonstrated the lowering of the complete fabrication process temperature from 180˚C down to 80˚C [69]. This ecofriendly fabrication process will: (1) require overall lower energy use in manufacturing (since no PECVD is required); (2) use wider choice of plastics with improved properties concerning transparency, biodegradability (<12 months), bio-derived (e.g. cellulose), low-cost and (3) be able to be integrated with other processes without destroying their devices (e.g. OTFT backplane could be processed on top of the OLED device) that also open potential for R2R manufacturing.

Moreover, SmartKem is one of the first companies to enable digital design on OFETs (organic field-effect transistors) with non-complimentary logic and 3V power supplies. This creates new opportunities for designing fully OE (organic electronics) computers, but these computers require rethinking all design decisions from scratch.

Finally, and important, Smartkem devices fabricated on flexible substrates show good degradation results with bending [70] what allows adapting their sensors and circuits to different environments (wearables, industrial, etc.). A positive V_T shift in OTFT devices is observed in the atmosphere under different bending conditions. That degradation comes from two mechanisms: the contribution of oxygen for a positive V_T shift and the contribution of mechanical tensile bending stress for a negative one. The main difference in degradation is the change in the molecular distance due to different bending conditions (tensile/compressive).

1.4 Research objectives and problem statement

The primary focus of this research is to investigate the utilization of ISFETs integrated with MUX OTFT technology in electronic sensing systems, with the aim of addressing several key challenges and limitations. The research objectives encompass various aspects related to the application and optimization of ISFETs and MUX OTFTs in electronic sensing.

One of the main research objectives is to explore the feasibility and benefits of employing EG-ISFETs that are reusable. By incorporating extended gates, it becomes possible to maximize the utilization of ISFETs without the need to increase the amount of different devices. This approach offers the advantage of cost-effectiveness and resource efficiency, as the same ISFETs can be used across multiple sensing applications.

Another important aspect that the research addresses is the mitigation of ESD by minimizing human touch as much as possible. By reducing direct human contact with the sensing elements, the risk of ESD-induced damage to the sensitive ISFETs is minimized. This approach ensures the reliability and longevity of the sensing system, enhancing its overall performance and stability.

The research also aims to overcome the limitation of increasing the number of ISFETs by utilizing MUX OTFT technology. By incorporating MUX OTFTs into the system architecture, the selection and control of desirable ISFETs become feasible. This enables the customization of the sensing system based on desired sensitivity levels or specific structures required for different applications. Additionally, the use of parallel ISFETs provides redundancy and coverage, ensuring that if one ISFET becomes damaged or faulty, the others can compensate and maintain accurate sensing capabilities.

The problem statement revolves around the need to enhance the reliability, efficiency, and versatility of ISFET-based sensing systems. By addressing the challenges of reusability, ESD protection, minimizing ISFET quantity, and implementing MUX selection, the research aims to contribute to the development of robust and adaptable electronic sensing systems. These advancements have the potential to impact various fields such as biomedical diagnostics, environmental monitoring, and chemical analysis, where accurate and reliable sensing capabilities are crucial.

This research focuses on investigating the integration of ISFETs with MUX OTFT technology to overcome challenges and limitations in electronic sensing systems. The objectives encompass the utilization of reusable EG-ISFETs, ESD mitigation, minimizing ISFET quantity, implementing MUX selection, and utilizing parallel ISFETs for increased reliability. By addressing these objectives, the research aims to advance the performance and applicability of ISFET-based sensing systems, enabling their wider adoption and improving their overall effectiveness in diverse sensing applications.

Chapter 2. State-of-the-Art

In living things, the presence of protons, ions, and small molecules frequently results in the generation of biological signals. In order to interpret the electrical signal generated by the biological signal and monitor the levels of these species in situ, biosensors are essential. Among these signals, cellular pH levels play a crucial role because they reveal important details about intracellular processes like cell membrane transport. To ensure normal cellular function, intercellular processes, and cell growth, proper pH levels must be maintained[71], [72]. Consequently, monitoring and controlling pH in cells hold significant potential for diagnostic and therapeutic applications [73]. In the realm of biosensors, electrical sensors in the form of wireless wearable platforms offer excellent prospects for medical applications due to their accurate detection, high sensitivity, low power consumption, rapid response, and ease of signal processing [74]. While ion-selective electrodes are commonly used in electrical biosensors, FETs have emerged as a versatile alternative, excelling in the continuous monitoring of small-scale analyte levels [75].

While conventional ISFETs integrate the sensing and transducer units, they have certain drawbacks such as chemical instability and optical interference with sensitivity. In contrast, extended-gate ion-sensitive field-effect transistors (EG-ISFETs) offer the advantage of reusability by replacing only the detachable sensing unit when the sensing membrane is damaged. Since the sensing unit is more cost-effective to produce compared to the transducer unit, EG-ISFETs are suitable for disposable biosensors. However, both conventional EG-ISFETs and ISFETs still face challenges in achieving high sensitivity, as they are limited by the Nernst limit of 59.15 mV/pH at room temperature.

Moreover, the fabrication of large arrays of EG-ISFETs using silicon-on-insulator (SOI) wafers for complementary metal-oxide-semiconductor (CMOS) processes is often associated with high costs and requires elevated process temperatures[76]. On the other hand, thin-film transistors (TFTs) based on low-temperature polycrystalline silicon (poly-Si) or metal oxide semiconductors have been extensively studied for the production of large-area liquid crystal displays (LCDs) and organic light-emitting diode (OLED) display panels. These TFT technologies offer the potential for large-area device manufacturing at lower costs [77]. Metal oxide TFTs, in particular, hold promise for transparent, flexible, and wearable electronic device fabrication on temperature-sensitive substrates [78].

2.1 Advancements in OTFT Technology

Since the inception of thin-film transistor (TFT) technology in 1962 [79]–[81], it has made significant strides and found widespread application across various fields. The rapid progress of liquid crystal display (LCD) technology in the 1970s created new opportunities for TFT, particularly in fulfilling the pressing need of the LCD industry for a semiconductor switch device capable of driving large area active matrix (AM) on glass [82]. In response to this demand, Le

Comber et al. introduced amorphous silicon (a-Si) based TFT devices for AM LCD (AMLCD) in 1979 [83]. The subsequent introduction of hydrogenated a-Si (a-Si:H) in 1980 further enhanced the mobility of TFT, catering to the requirements of AMLCD [84].

Over time, TFT technology has advanced in tandem with the growth of flat panel display (FPD) technology, which relies on TFT as its fundamental component. However, the mobility of a-Si:H TFT falls short for FPD devices that necessitate higher TFT mobility to optimize driving performance. In 1980, Depp et al. demonstrated that poly-crystalline silicon (p-Si) TFT devices, boasting a typical carrier mobility of 102 cm^2/Vs, serve as an excellent alternative to meet the demands of high resolution and substantial current driving requirements [85]. Although TFT mobility reached 50 cm2 cm^2/Vs, its practical application was severely limited by the high process temperature exceeding 300 °C. Consequently, various techniques for producing low-temperature polysilicon were explored, leading to the development of low-temperature polysilicon (LTPS). In 1989, Serikawa et al. pioneered the use of laser irradiation to lower the annealing temperature of polysilicon [86]. However, the commercial promotion of TFT faced constraints due to the requirement of annealing at 300 °C to achieve reliable results. By reducing the LTPS process temperature to below 150 °C, it became possible to manufacture LTPS TFT arrays on the same glass substrate as amorphous Si TFT arrays [87]. Compared to a-Si:H TFT, LTPS TFT exhibits carrier mobility tens to hundreds of times greater. Notably, LTPS LCD offers advantages such as quick response times, excellent resolution, and high aperture ratio. With the recent advancements in internet of things (IoT) technology, TFT arrays have also found application in the low-cost integrated circuit (IC) industry. In 2021, Biggs et al. published a 32-bit Arm microprocessor constructed with metal-oxide TFT technology on a flexible substrate, opening the door for the development of affordable, fully flexible smart integrated systems [88].

In addition to traditional silicon-based technologies, extensive research has been conducted on various novel materials to fabricate TFTs. Among these materials, organic semiconductors (OSCs) have garnered significant attention. OSCs present a promising option for flexible electronics, as they can function effectively within a specific range of mechanical deformation. The first OTFT, which utilized polyacetylene as the semiconductor, was described by Ebisawa et al. in 1983 [89]. Further advancements in the field led to the development of flexible polyimide substrates for all-polymer integrated circuits by Drury et al. in 1998 [90]. OTFT devices offer several advantages, including low cost, structural flexibility, and the ability to fabricate large-area structures through solution-based techniques. However, they still face challenges in terms of performance uniformity and device stability [67], [91], [92]. Despite these challenges, OTFTs have found applications in electrophoretic displays, radio frequency identification (RFID), biomedical sensors, and driving arrays for mini-LED backlight sources [93]–[97].

In recent decades, extensive efforts have been devoted to improving the device mobility of OTFTs through material chemistry and processing techniques [98]–[103]. In power-constrained electronic systems, reducing leakage current is of paramount importance [104]. The quality and thickness of the Organic Gate Insulator (OGI) layer play a crucial role in controlling leakage, and patterning the OSC layer can effectively suppress parasitic leakage from the channel region [105]–[107]. One significant challenge to overcome is the intrinsic channel leakage current caused by small carrier

injection from the drain contact [108]. The carrier mobility (μ) of OTFTs has now exceeded 2 cm^2/Vs, surpassing that of amorphous silicon transistors (cm^2/Vs) [109]–[112]. However, for high-resolution displays, the mobility of OTFTs still falls behind that of inorganic semiconductor materials such as LTPS TFTs and oxide semiconductors like IGZO TFTs [113]–[115]. Therefore, enhancing the output current and improving reliability are crucial considerations for the commercialization of OTFTs.

In the case of p-type OTFTs, minority carrier electrons can be injected from the drain electrode into the lowest unoccupied molecular orbital (LUMO) states of the OSC under the application of a moderately positive gate voltage in the OFF-state or deep subthreshold regime. This minority carrier injection becomes more severe for narrow bandgap (E_g) OSCs, such as donor-acceptor (D-A) structure molecules that have been extensively studied for their high mobility due to strong intermolecular contacts enabling efficient intermolecular charge transport [116], [117]. The injection of minority carriers leads to performance instability and trapped electrons in the OSC layer or at the interfaces [118], [119]. To mitigate the adverse effects of minority carrier injection, two different techniques have been developed for electrons in p-type OTFTs [120]–[124]. One approach involves incorporating molecular additives into the channel as specific charge-carrier electron traps, preventing the injected electrons from contributing to conduction [121], [122]. However, achieving complete electron avoidance while maintaining hole conduction in the ON-state presents challenges [125]. The other technique aims to limit electron injection by increasing the height of the electron injection barrier through contact doping or incorporating a wide bandgap interfacial layer at the contact interface [120], [123], [124]. However, complete elimination of electron injection is not achieved due to the limitations of charge transfer doping in OSCs, and the migration of dopants within the OSC layer can lead to device instability [126], [127].

The utilization of dual gate p-type organic thin-film transistors (OTFTs) represents a state-of-the-art approach in the field of organic electronics. Dual gate OTFTs offer enhanced control over device performance by allowing independent modulation of both the threshold voltage and the subthreshold swing. This unique feature enables precise tuning of the transistor characteristics, such as the on/off ratio and the output current. Furthermore, dual gate OTFTs exhibit improved stability and reduced hysteresis, which are critical for reliable operation in various applications. The use of a self-assembled monolayer (SAM) interfacial layer at the metal-semiconductor contact enhances carrier injection and reduces contact resistance, leading to enhanced device performance. Additionally, the incorporation of a sputtering-resistant polymer gate insulator layer and carefully designed ultra-thin organic semiconductor islands helps mitigate leakage current and parasitic effects, further improving the overall device reliability. The advancements in dual gate p-type OTFTs pave the way for the development of high-performance and reliable organic electronic devices for a wide range of applications, including flexible displays, sensors, and low-power integrated circuits.

2.2 Progress in EG-ISFETs and Ion Sensing

Significant progress has been made in the field of EG-ISFETs and ion sensing, offering promising advancements in sensing technologies. EG-ISFETs have emerged as powerful tools for ion detection and have witnessed notable developments in recent years [128]–[130].

EG-ISFETs are solid-state devices that utilize a sensitive ion-sensitive membrane in conjunction with a field-effect transistor structure to detect ions in a solution[131]. These devices offer several advantages, including high sensitivity, miniaturization potential, and compatibility with CMOS technology for integrated circuit applications. The progress in EG-ISFETs has led to enhanced ion sensing capabilities and broader application prospects.[132], [133]

Over time, there have been successful demonstrations of large-scale integration of these sensors, creating microarrays of ISFET primarily for neurophysiological measurements [134], [135]. Another significant application that requires sensing capabilities is DNA sequencing. Traditional DNA sequencing methods rely on optical techniques, such as fluorescent dyes and plasmon resonance, for detecting hybridizations. However, these optical methods have drawbacks such as increased size, cost, power requirements, low robustness, and longer processing times [136]–[138], which make them unsuitable for portable point-of-care (PoC) platforms. To overcome these limitations, researchers have explored non-optical methods.

To address the challenges and improve the accessibility of DNA sequencing, the US National Human Genome Research Institute (NHGRI) initiated the $1000 genome project in 2004. The goal was to significantly reduce the cost of DNA sequencing from $10 million to below $1000 [139]. This cost reduction has had a profound impact, enabling real-time monitoring and rapid detection of infectious diseases like COVID-19, as well as potential breakthroughs in diseases like cancer. ISFET-based pixel array technology has emerged as a promising option to realize the vision of a more scalable, low-cost, and portable sequencing solution. Additionally, the advent of biochip revolution has shifted the focus of lab-on-chip (LoC) sensor platforms towards electrolyte imaging and DNA sequencing [140]–[142]. These LoC devices streamline large-scale laboratory processes by integrating multiple stages of sample handling into a single microchip. This integration not only minimizes contamination risks but also reduces the reliance on specialized laboratory equipment and trained clinicians.

As extensively discussed in [143], the utilization of ISFET pixel arrays offers the capability to monitor and control multiple reactions concurrently, which is crucial for various applications including genetic sequencing and extracellular imaging [144]–[146]. Moreover, these arrays enable spatial averaging to enhance readout resolution and provide the added benefit of sensor redundancy [142]. However, despite the significant advancements in ISFET applications, the readout architectures based on ISFETs often encounter several imperfections that hinder their widespread use in commercial point-of-care (PoC) applications.

One significant area of advancement is the improvement in the performance parameters of EG-ISFETs. Efforts have been made to enhance the sensitivity, selectivity, response time, and stability of these devices [131]–[133]. Through the development of novel ion-sensitive materials and

optimization of device structures, researchers have achieved higher sensitivities, enabling the detection of ions at lower concentrations. Selectivity has been enhanced by utilizing ion-specific membranes and surface modifications that allow for targeted ion detection.

2.3 Integration of OTFTs and EG-ISFETs in Analog MUXs

ISFETs, despite their advantageous features, experience non-idealities in the form of trapped charge and drift [147]. Trapped charge introduces non-uniform DC offsets across an ISFET array, with reported values reaching several volts [148], [149]. Drift causes temporal signal variations, arising from either chemical or electrical factors, and even affects the ISFET's gate voltage at chemical equilibrium [150], [151]. Consequently, various compensation methods have been proposed, broadly classified into two categories: chip post-processing and on-chip circuit compensation [152]. Chip post-processing involves UV light irradiation to eliminate trapped charge, but this additional step increases fabrication costs and time [153].

Alternatively, on-chip circuit compensation techniques can be employed, which can be further subdivided into two main categories: Programmable Gate ISFETs (PG-ISFET) [154] and the use of a reset switch on the floating gate [155]. PG-ISFETs utilize a capacitor on the floating gate to compensate for trapped charge, albeit at the expense of reducing pH sensitivity. In contrast, direct feedback to the floating gate through a reset switch effectively sets the gate voltage, eliminating the effect of trapped charge. Moreover, periodic resetting can minimize the impact of chemical drift. However, the addition of a reset switch introduces electrical drift through leakage, which can affect long-term measurements. Nonetheless, this approach is suitable for high-speed applications where the frequency of resetting is high enough to minimize the leakage effect.

Presently, there is a strong emphasis on implementing robust sensing arrays with adequate compensation for these non-idealities. ISFET arrays are commonly employed in low-frequency biomedical applications such as DNA amplification detection [156], where speed and resolution requirements are relatively low. Other applications mentioned in the literature include enzyme kinetics monitoring [157], food safety assessment [158], and neural activity recording [159].

To achieve high-speed readout, current mode signal processing methods are being explored and applied. These methods eliminate the need for op-amps and charging of voltage nodes, which can reduce bandwidth compared to traditional voltage mode methods [160]. Analog signal processing is accomplished using the current conveyor, which plays a similar role to an op-amp in voltage mode. Other signal operations, such as amplification, addition, and subtraction, are simplified by joining current branches or utilizing current mirrors [161]. Multiple CMOS arrays have employed current mode operation, particularly in motion imagers [162], [163]. Several of these arrays demonstrate high resolution and high-speed performance, such as a 40×40 array with 25,000 frames per second (fps) in a 0.35µm process [164], and a 192×124 array with 48,000 fps in 0.5µm CMOS technology [165]. Consequently, similar techniques can be applied in the context of high-speed ion imaging.

However, while the recent research endeavors have primarily focused on increasing the number of ISFETs in sensing arrays, it is important to acknowledge that this competitive race may not lead

to a definitive winner. Instead, a more meaningful and conclusive outcome can be achieved by incorporating OTFT MUXs into the system. These MUXs offer a potential solution for selecting the desired EG-ISFET and customizing the sensitivity or performance according to specific requirements.

By integrating OTFT MUXs into the ISFET array architecture, researchers can introduce a higher level of control and versatility. These MUXs act as intelligent electronic switches, allowing for precise and selective activation of individual EG-ISFETs within the array. This capability enables the tailoring of sensitivity or performance, ensuring optimal functionality for diverse applications.

The incorporation of OTFT MUXs introduces a dynamic element to the traditional static configuration of ISFET arrays. Instead of being limited to a fixed setup, the system can adapt and respond to specific sensing needs by activating or deactivating specific EG-ISFETs as desired. This flexibility empowers researchers to optimize the array's performance for different analytes or operating conditions, enhancing its overall efficiency and accuracy.

Moreover, the utilization of OTFT MUXs opens up possibilities for advanced signal processing and data acquisition techniques. By selectively routing signals from chosen EG-ISFETs, complex algorithms and data fusion methodologies can be applied to extract valuable information and improve the reliability of measurements. This intelligent signal routing contributes to more robust and sophisticated sensing systems.

Furthermore, the integration of OTFT technology with ISFET arrays offers additional benefits. OTFTs are known for their characteristics such as low power consumption, flexibility, and compatibility with large-scale manufacturing processes. These advantages enable the development of flexible and conformable sensor arrays that can be seamlessly integrated into various applications, including wearable devices, biomedical diagnostics, environmental monitoring, and beyond.

2.4 Theoretical Framework

The theoretical framework provides the groundwork for comprehending the fundamental ideas and concepts that guide the investigation. Analog Multiplexers (MUXs), Organic Thin-Film Transistors (OTFTs), Extended Gate Ion-Sensitive Field-Effect Transistors (EG-ISFETs), and the benefits of dual gate architecture will all be covered in this part.

Organic Thin-Film Transistors (OTFTs) are a class of transistors that utilize organic materials as the semiconducting layer. These materials offer unique properties such as flexibility, low-cost manufacturing, and compatibility with large-area fabrication processes. The operation of OTFTs is based on the modulation of charge carriers within the organic semiconductor layer, controlled by the application of voltages to the gate, source, and drain terminals. Understanding the fundamental theories behind the operation and performance of OTFTs is essential for optimizing their design and exploring their potential applications in various fields, including sensing, displays, and electronic circuits.

Extended Gate Ion-Sensitive Field-Effect Transistors (EG-ISFETs) are a specialized type of ISFETs that incorporate an extended gate electrode. ISFETs are devices used for ion sensing, particularly for measuring pH levels in various biological and chemical applications. The extended gate in EG-ISFETs enhances their sensitivity to ion concentrations and provides a means for selective ion detection. By understanding the working principles of EG-ISFETs, researchers can develop strategies to improve their sensitivity, stability, and selectivity for specific ion species.

Analog MUXs are electronic devices that enable the selection and routing of analog signals from multiple input channels to a single output channel. They play a crucial role in data acquisition and sensor array applications. MUXs allow for efficient utilization of limited resources by enabling the sharing of common components, among multiple sensors or signal sources. Exploring the working principles of MUXs is important for designing effective signal routing architectures and optimizing the overall performance of sensor arrays.

Dual gate architecture is a concept that involves the incorporation of two gate electrodes in a transistor device. This configuration offers several advantages, including enhanced control over the device characteristics, improved signal-to-noise ratio, and increased stability. By utilizing a dual gate architecture, researchers can optimize the performance of transistors and sensors, particularly in terms of sensitivity, linearity, and noise reduction. Understanding the advantages and design considerations associated with dual gate architecture is essential for developing advanced transistor devices and sensor systems.

By delving into the theoretical framework of OTFTs, EG-ISFETs, MUXs, and dual gate architecture, researchers can gain valuable insights into the principles governing their operation, performance, and potential applications. This knowledge will serve as a solid foundation for the subsequent sections, where we will explore the working principles and applications of each of these components in more detail.

2.4.1 Dual gate architecture and its advantages

The minority carrier electrons may be injected from the drain electrode into the OSC's lowest unoccupied molecular orbital (LUMO) states when a moderately positive gate voltage is used for the OFF-state or deep subthreshold regime. For narrow bandgap (E_g) OSCs, such as donor-acceptor (D-A) structure molecules, which have been extensively researched for high mobility because of their strong intermolecular contacts permitting efficient intermolecular charge transport, the minority carrier injection is more severe[166], [167].Electron injection led to abnormal electrical behavior and a rise in leakage current[168]–[170]. Performance instability was also brought on by the trapped electrons in the OSC layer or at the interfaces[171]–[173]. In order to reduce the negative consequences of minority carrier injection, two different types of techniques have been developed (electrons in p-type OTFTs)[174]–[178].

One method is to add molecular additives to the channel as specific charge-carrier electron traps, which prohibit the injected electrons from assisting in conduction[57], [58]. Unfortunately, it is challenging to manage this approach in processes for complete electron avoidance without interfering with the transit of holes in the ON-state [179]. The other technique is to limit electron injection by increasing the height of the electron injection barrier by contact doping or adding a

broad E_g interfacial layer at the contact interface[56], [59], [180]. When the rise in electron current begins to outpace the fall in hole current, there is a current minimum. Leakage current caused by electron injection starts to take precedence when V_{GS} moves toward a more positive value in the OFF-state.

One method to lower electron injection by raising the height of the electron injection barrier is the dual gate structure. The electrons can be repelled from the OSC layer and both sour-to-drain and leakage current can be reduced by applying a negative voltage to the back gate [63], [181], [182]. We indicate that the dual gate OTFTs display excellent performance, stability, low-voltage operation, and logic capabilities.

2.4.2 Measuring Microfluidics materials

Microfluidics is a burgeoning area of study that deals with the microscale treatment of fluids; it is most often distinguished by objects that have critical dimensions less than 1 mm. Researchers can use a variety of physical laws that scale well at this scale, including quick diffusion [183], laminar flows [184], Dean flow [185], rapid heat transport [186], and taking advantage of the high surface area to volume ratio [187]. Microfluidics is used in a wide range of industries, including analytical chemistry [186], molecular biology [188], energy production [189], cell separations [185], and energy generation.

A large portion of the work in the subject of microfluidics was carried out utilizing soft lithography, which Whitesides [190] first developed in 1998. Soft lithography techniques, particularly for polydimethylsiloxane (PDMS), have been extensively studied [191], [192]. The need for cleanroom manufacturing, while well-developed by the microelectromechanical systems (MEMS) community, is still expensive and time-consuming, and was one of the key challenges of soft lithography in the beginning. Recently, this has been somewhat mitigated by low-cost mold-making techniques, as discussed by Faustino [193]. In addition to soft lithography, other fabrication techniques for submillimeter channels have been developed by microfluidic engineers for several reasons, including lower costs, quicker turnaround times, less expensive materials and tools, and improved functionality.

One way to measure pH levels of microfluidics systems is using ISFETs. ISFETs are a type of sensor that can detect changes in ion concentrations, including hydrogen ions (H+), which are responsible for pH. The ISFET consists of a thin film of metal oxide that acts as the sensing element and is placed near the gate of a FET. The FET modulates its threshold voltage in response to changes in the concentration of ions in the film, allowing for the detection of pH levels [194]–[196].

When monitoring electrochemical reactions, ISFET has many benefits. ISFET can be mass produced and further integrated into other sensing systems because it is based on the common complementary metal-oxide-semiconductor technique[194]–[198].

ISFETs can be implemented with OTFTs by connecting the top gate electrode to the media where the pH measurement must be performed. In this way, the drain to source current will depend on the electrical charge related to the pH. Furthermore, pH electrode and gate electrode can be

separated (while connected with a good conductor) to produce the extended gate electrode. This allows an easier integration of the electrode with the measurement environment and increase the level of reuse of the ISFET sensors, expensive than electrodes, that can trap chemical materials and degrade its behavior.

2.5 Fundamentals of OTFT and EG-ISFET

Over the past few decades, significant efforts have been made to gradually replace conventional inorganic semiconductors (such as silicon and gallium arsenide), silicon oxide insulators, and metals (like aluminum and copper) with environmentally friendly organic materials that can be manufactured using cost-effective techniques. The primary focus of these efforts has been to enhance the electrical properties and stability of organic materials. The electrical characteristics of basic devices, such as organic transistors, play a crucial role in improving the performance of electronic circuits.

In electronic applications, it is essential for transistors to exhibit a large current modulation ratio (known as I_{on}/I_{off} ratio) since they are commonly utilized as switches. In the "on" state, a transistor should allow a substantial drain current to flow, while in the "off" state, the drain current should be negligible. Achieving this combination of requirements is most effectively accomplished with a semiconductor material that possesses a high intrinsic resistivity and a large carrier mobility. These properties enable efficient switching and reliable operation in electronic circuits, thereby enhancing their overall performance.

2.5.1 Substrates

Many of the OTFT devices focus on utilizing cost-effective and flexible substrates, enabling the production of large-area products with enhanced design flexibility. Various materials are employed in different applications, such as sensors, OLED lighting and displays, organic photovoltaic (OPV) cells, and flexible dye-sensitized solar cells [199]–[202]. Glass and metals like stainless steel, alumina, or titanium foil, known for their excellent barrier properties, find extensive use in these applications. Additionally, flexible and lightweight plastics and polyesters like PET and PEN have gained significant attention in roll-to-roll production for large-area applications [203]–[208]. Paper, being derived from renewable resources, has emerged as a promising candidate for affordable and eco-friendly electronic applications [209]–[211].

2.5.2 Organic Semiconductors

The two main categories of organic semiconductors are small molecules and polymers. The chemical structures of small molecules, as opposed to polymers, are clearly defined, guaranteeing the certainty of intrinsic properties like the energies of the highest occupied molecular orbitals (HOMO) and lowest unoccupied molecular orbitals (LUMO) [212]–[214]. This characteristic allows small molecules to possess relatively definite crystal structures and lattice parameters, resulting in high crystallinity. Furthermore, organic small molecules offer the possibility of achieving single crystals with ultrahigh purity and low trap density, leading to enhanced carrier mobility in thin films, as the mobility is strongly influenced by the crystallinity, defects, and traps present in the film [215].

Thermal evaporation is a commonly employed method for growing organic small molecule films. The molecular and crystal structure of these molecules allows for precise control of the processing conditions during evaporation, as their known thermodynamic properties, such as boiling point and vapor pressure, can be accurately predicted [216], [217]. This level of control enables real-time monitoring and tracking of the film's growth speed and thickness. Although challenges like surface roughness and the existence of polymorphs can arise during evaporation [218]–[220], the evaporability of organic small molecules provides significant advantages in optimizing the morphology and uniformity of the thin film, thus mitigating device variation.

Organic small molecules can be further classified based on their conductivity type, namely p-type, n-type, and ambipolar materials. It is important to note that while ambipolar or n-type behavior typically occurs in vacuum or inert atmospheres, these materials tend to exhibit p-type conductivity in ambient environments [221]. Among the widely studied p-type small molecules is pentacene, and to enhance its solubility for solution processing, triisopropyl-silylethynyl (TIPS) groups are often added to its molecular structure [222]. Additionally, rubrene and copper phthalocyanine (CuPc) have also received considerable attention in the early 2000s [223]. Recent advancements have led to the development of new series of p-type organic small molecule semiconductors.

Compared to p-type materials, high-performance and high-stability n-type organic small molecules are relatively less common [224], [225]. This can be attributed to the fact that the LUMO energy of organic semiconductors is often high, making the injected electrons prone to trapping by oxygen and water in the surrounding air, thereby suppressing electron transport. Additionally, commonly used air-stable metals with high work functions result in the formation of high Schottky barriers at the contacts, which are not suitable for efficient electron injection [226]. Notable examples of n-type small molecules include fullerene (C60) and its derivatives, naphthalene carbodiimide (NTCDI), and fluorinated copper phthalocyanine (FCuPc) [227]–[229]. However, these materials still face challenges in terms of performance and stability compared to p-type materials. Recent studies indicate a preference for p-type-only architectures in organic circuits, despite efforts to develop complementary circuits [230]. Nevertheless, there are some exceptional n-type semiconductors that exhibit the potential for application in complementary circuits. One such example is the derivative of 4,8-bis[5-(3-cyanophenyl)thiophene-2-yl] benzo[1,2-c:4,5-c′]bis[1,2,5]thiadiazole (TU-3) with a low-lying LUMO energy of 4.3 eV, good solubility, and air stability [231].

Semiconducting polymers represent another category of organic semiconducting materials. The first organic transistor was based on poly(3-hexylthiophene) (P3HT), emphasizing the significance of semiconducting polymers [232]. Unlike small molecules, semiconducting polymers exhibit variations in polymerization degrees, molecular weights, and packing structures due to differences in synthesis routes and thin film deposition conditions. Obtaining a single crystal in semiconducting polymer thin films is generally challenging, and traditional thermal evaporation methods used for small molecules are not applicable to polymers. Charge transport in semiconducting polymers heavily relies on chain alignment and aggregation states in the thin film, necessitating consideration at multiple length scales. Recent advancements in the understanding of crystal structures in conjugated polymers have been noteworthy [233]. Furthermore, significant

progress has been made in improving the structural precision and sequence homogeneity of polymers, reducing structural and energetic disorder and enhancing charge transport in bulk or thin films [234], [235]. Researchers have developed various polymerization and assembly strategies to achieve controlled molecular weight and low dispersity, contributing to improved charge transport [236]–[238].

However, semiconducting polymers offer excellent versatility for modification. By adjusting alkyl side chains and conjugating units in the polymer backbone, the solubility, molecular packing, and charge transport properties can be finely tuned [239]–[241]. Solution processing methods also enable the production of high-quality and uniform thin films, making semiconducting polymers suitable for circuit fabrication. Additionally, certain semiconducting polymers possess inherent stretchability, which can be further enhanced through side-chain engineering, offering potential applications in stretchable and wearable devices [242].

Semiconducting polymers encompass a wide range of materials, and one extensively researched branch is diketopyrrolopyrrole (DPP)-based polymers. By incorporating donor moieties like dithienylthieno[3,2-b]thiophene (DTT) to form a donor-acceptor (D-A) structure, DPP-based polymers can exhibit high carrier mobility, stability, and solution processability [243]. Introducing DPP-based polymers into polymer elastomers such as polystyrene-block-poly(ethylene-ran-butylene)-block-polystyrene (SEBS) allows for precise adjustment of the mechanical properties of the semiconducting layer, particularly improving stretchability [244]. Recently, several commercially available semiconducting polymers with good performance and solution processability have been developed, including Lisicon® SP500, which can achieve a mobility of up to 2 cm^2/Vs [245].

2.5.3 Gate Insulator

The gate insulator assumes a crucial role in the operation of OTFTs. Its functions include preventing undesirable leakage charge between the gate electrode and the semiconductor, as well as accumulating charge carriers at the semiconductor interface to facilitate the flow of charge between the source (S) and drain (D) electrodes. As a result, the properties of the gate insulator significantly impact the device performance of OTFTs, including factors such as operating voltage [246] and operational stability [247]. Moreover, since the gate insulator directly interfaces with the organic semiconductor, it has a substantial influence on the crystallinity of the semiconductor, which, in turn, affects the charge mobility of the OTFT [248]. Therefore, the development of new gate insulators that possess excellent insulation properties and suitable interfacial properties matching those of the semiconductor is crucial for optimizing OTFT performance [249]–[251].

Among the available options, polymers have emerged as favorable candidates for gate insulator materials in OTFTs. This is primarily due to their mechanical flexibility, cost-effectiveness, and superior processability in comparison to inorganic materials [251], [252]. Furthermore, the chemical functionalities present in polymers play a vital role in optimizing and precisely controlling interfacial properties, thus influencing device performance [253]–[255]. For instance, the inclusion of surface fluorine functionalities in fluoropolymers has been proposed to enhance the operational stability of p-type OTFTs [247], [253], [256], [257].

Polymer gate dielectrics provide benefits such as high process throughput, low fabrication costs, and a lower thermal budget compared to inorganic dielectrics. Since OTFTs are intended for inexpensive applications, achieving high throughput and utilizing low-cost processes are crucial considerations. Therefore, high-quality, solution-processed polymer gate dielectrics are the most suitable choice for fabricating OTFTs and integrated circuits. The first organic integrated circuits with a solution-processed polyvinyl phenol gate dielectric were reported by Duray et al. in 1998 [90]. Subsequently, in 2000, a solution-processed photoresist (Olin Hunt Model SC100) was employed as the gate dielectric layer in OTFTs and even in fairly complex integrated circuits [258].

One notable disadvantage of solution-processed polymer gate dielectrics is their minimum film thickness. In contrast, high-temperature, vacuum-deposited inorganic gate dielectrics offer the advantage of scalable thickness with relative ease. When utilizing solution-processing techniques for polymers, the resulting films tend to have thicknesses greater than 100nm. However, there is a complementary technique that can address this limitation and improve the characteristics of polymer dielectrics while reducing their thickness.

This technique involves the use of insulating, organic Self-Assembled Monolayers (SAMs). By incorporating SAMs, it becomes possible to enhance the properties of polymer dielectrics and reduce their thickness, thereby enabling the fabrication of fast integrated circuits with lower power consumption. These SAMs can achieve thicknesses ranging between 2 and 3nm and provide leakage currents comparable to, or even smaller than, those typically obtained with high-quality silicon oxide films [259].

2.5.4 Conductor Materials

2.5.4.1 Silver inks

Silver (Ag) is widely regarded as a highly advanced electrode material in the field of printed electronics due to its excellent oxidation resistance and chemical stability [260], [261]. Previous studies by Y. Ueoka have demonstrated the feasibility of utilizing Ag as an electrode material for IGZO-based TFTs within specific operating ranges [262]. However, when sintering the printed Ag electrode, the application of heat affects both the Ag electrode and the IGZO layer, leading to the deterioration of TFT performance due to certain additives present in the Ag ink that contaminate the IGZO channel [263], [264]. To mitigate these interfacial reactions, the implementation of an interlayer between the IGZO channel and the electrode has been explored [265]. Unfortunately, the sintering process of the interlayer not only requires additional heat treatment but also significantly prolongs the overall process time, resulting in inefficiencies.

2.5.4.2 Metal

Metals are commonly used as conductor materials in thin-film electronics. Copper (Cu) [266], [267], gold (Au) [268]–[272], and aluminum (Al) [273]–[275] are popular choices due to their high electrical conductivity, with values of 59.8 10^6 \$S/m, 42.6 10^6\$S/m , and 37.7 10^6\$S/m, respectively [276]. Chromium (Cr) [268], [269], [277] and titanium (Ti) [266], [278], [279] have lower electrical conductivity but are often used as adhesive layers to improve the adhesion of other metals like Au, platinum (Pt) [280], [281], and palladium (Pd) [282]. However, Cr has limited

ductility and a smaller rupture strain level (0.5%) compared to metals like Cu, which restricts the minimum achievable bending radius [283].

Molybdenum (Mo) [284], [285] and magnesium (Mg) [286] are commonly employed in thin-film electronics due to their biodegradability and biocompatibility. Mg is also water-soluble, making it suitable for bioresorbable implants, while Mo can degrade in an acidic environment like zinc (Zn) or iron (Fe) [287].

2.5.5 Biosensors based on EG-ISFET

One way to measure pH levels in cells is using ISFETs. ISFETs are a type of biosensor that can detect changes in ion concentrations, including hydrogen ions (H^+), which are responsible for pH. The ISFET consists of a thin film of metal oxide that acts as the sensing element and is placed near the gate of a FET. The FET modulates its threshold voltage in response to changes in the concentration of ions in the film, allowing for the detection of pH levels [288]–[290].

When monitoring electrochemical reactions, ISFET has many benefits. ISFET can be mass produced and further integrated into other sensing systems because it is based on the common complementary metal-oxide-semiconductor technique[194]–[198].

Ion-sensitive field-effect transistors with extended gates are known as EG-ISFETs. It is a particular kind of sensor that can determine the amount of ions present in a solution by observing changes in the surface potential of a sensing oxide layer [291]. By adopting an extended conductive layer to separate the sensing oxide layer from the gate oxide of a thin-film transistor (TFT), the gate oxide is shielded from the electrolyte solution and the sensor's stability and robustness are increased. Many applications, including biosensors, environmental monitoring, and food quality management, are possible with EG-ISFET sensors[130]. Microelectrode array (MEA) is the gate material of the EG-ISFET, enabling the simultaneous detection of numerous analytes in a single sample. Because of its ability to monitor pH levels in cells as well as other ionic species, the EG-multiplexing ISFET is a useful tool.

The EG-ISFET has been used in a variety of applications, including the measurement of pH levels in cells, tissues, and biofluids [292]–[295]. It has been used in cancer cell research, where changes in pH levels can indicate the presence of cancerous cells [294]. It has also been used in stem cell research, where pH levels are used to monitor stem cell differentiation into specific cell types[296], [297]. In addition to its use in medical applications, the EG-ISFET has also been used in environmental monitoring, where it can be used to measure pH levels in water and soil [298], [299]. The EG-ISFET has also been used in food safety applications, where it can be used to detect the presence of harmful bacteria in food products [299].

2.6 Working principals of analog MUXs

Analogue multiplexers are electrical devices that pick one of numerous input signals and route it to a single output. They are widely utilized in many applications, such as data collecting systems, signal processing, and communication systems. [159], [300]–[304]. Analogue multiplexers can be built with a variety of technologies, including bipolar junction transistors (BJTs), FETs, Metal

Oxide Semiconductors (MOS) and OTFTs. Because of their distinct properties, OTFTs are a particularly appealing solution for multiplexer applications.

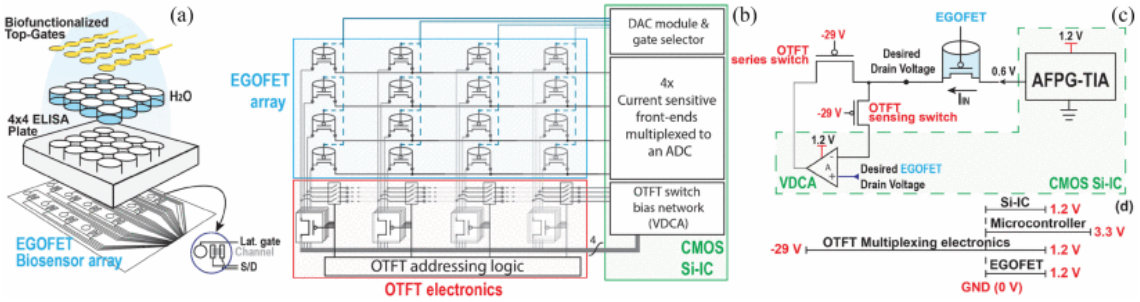


Figure 1. System-level architecture with focus on modules interconnections and components [300]

An analogue multiplexer based on OTFTs is commonly designed using a matrix of transistors, with each column representing an input signal and each row representing a select line (**Figure 1**). A series of select lines controls the matrix, which is used to pick the chosen input signal. The selected signal is then routed to the output after passing through a buffer amplifier.

When compared to standard silicon-based transistors, the usage of OTFTs in multiplexer circuits allows for low-noise operation, good signal quality, and improved performance[305]. To provide best performance, the design of an analogue multiplexer based on OTFTs must consider crosstalk between neighboring input signals.

Traditional sensor designs sometimes need complicated circuitry and wiring in order to handle several sensors and their associated connections. This may enhance the complexity of circuit design, signal routing, and overall system integration. Furthermore, managing and controlling several sensors can be difficult, especially in applications requiring a high number of sensors.

The suggested solution intends to simplify the sensor system design, speed up the integration process, and minimize the overall complexity associated with sensor deployment and operation by combining EG-ISFET technology with analogue OTFT multiplexers.

In this paper, we propose a novel approach where we merge EG-ISFET technology with analogue OTFT multiplexers. The primary objective of this integration is to address the issue of complexity and enhance the reusability of sensors. By combining these two technologies, we aim to leverage the unique characteristics of each component to create a more efficient and versatile sensing platform. The EG-ISFET provides sensitive and accurate ion detection capabilities, while the analogue OTFT multiplexers enable the integration of multiple sensors into a single device, reducing complexity and enhancing the scalability of the system. This integration offers a promising solution for applications requiring reusable sensors with improved performance and simplified circuitry.

The proposed integrated structure, as illustrated in **Figure 2**, showcases the successful merging of EG-ISFET technology with analogue OTFT multiplexers. This visual representation provides a clear understanding of the combined system and the interaction between the EG-ISFET and the OTFT components. The figure highlights the physical arrangement and connectivity of the

different elements, showcasing how the integration enhances the overall functionality and performance of the sensor platform. This visual aid aids in comprehending the design and serves as a valuable reference for further analysis and discussion of the integrated structure's capabilities and potential applications.

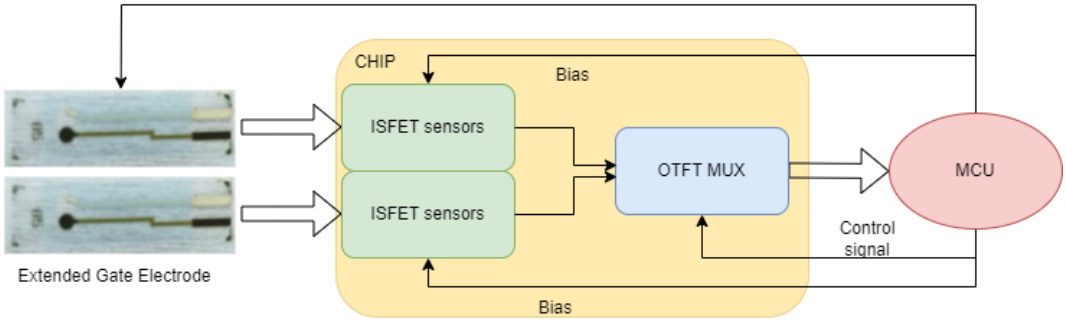


Figure 2. System architecture showcasing the integration of ISFETs and MUX for enhanced functionality connected to external components (electrodes and microcontroller unit)

2.7 Interdigitated transistors

The inverted/staggered and co-planar OTFT structures are the most widely used devices when looking for large transistor width [67]. Interdigitated electrodes are often used to compensate for the low OSC conductivity in OTFTs. The source and drain electrodes have a comb-like shape and their teeth are alternately interlocked with each other. This increases the channel width per unit of area and allows higher current density [306]. Maximizing the transistor width per unit area allows to place more transistors on the same substrate. However, this geometry still has some limitations in terms of performance, as it depends on careful alignment of OSC crystals along the Drain and Source (D/S) electrodes during OSC deposition. This involves using a nitrogen flow, changing the temperature, and adjusting the solvent type and ratio [307]–[309].

2.8 Corbino-shaped transistors

Circular-shaped transistors, also known as Corbino transistors, are less frequently employed in circuit designs; instead, this gate shape is more frequently used in the display field to open or close a light-emitting diode (LED). The channel in this transistor architecture is shaped like rings. The Corbino disk, first reported by M. Corbino in 1911, is a disk with inner and outer concentric ring contacts [310]. It has been primarily used in magneto-resistance measurements [311] and has more recently been adopted for organic thin-film transistor (TFT) architectures [312], [313].

An annular-shaped electrode was initially used in 1996 in hydrogenated amorphous silicon (a-Si:H) TFTs to give a lower gate-to-source capacitance and a lower photocurrent level in active-matrix liquid crystal displays (AM-LCDs) [314]. Ring-shaped and circular electrodes were utilized in the pseudometal-oxide semiconductor field-effect transistor in 1999 to describe the electrical properties of silicon-on-oxide wafers by device geometrical features [315].

For small transistor widths, the Corbino TFT's circular channel design reduces the drain capacitance per unit of transistor width. By decreasing the output capacitance, switching speed and

frequency response is boosting, and this improves the device's performance [316], [317]. The Corbino TFT is appropriate for sensors and other high-speed signal processing applications. To prevent the direct current (DC) component of the input signal from having an impact on the output signal, the suggested sensor makes use of the Corbino TFT. The sensor's operational point is set to the desired value by supplying a bias voltage to the Corbino TFT's gate terminal[316]. As a result, the input signal may be measured by the sensor more precisely and steadily. Because to its distinctive circular form and low drain capacitance, the Corbino TFT can detect signals regardless of the input signal's DC component. It also has a high switching speed. One example of such an application is a large-area active-matrix organic light-emitting diode (AMOLED) display pixel[318].

Chapter 3. Tools, Technology and System Level concerns

This section provides a top-down view of the design decisions driven by a prototype built for ISFET sensing and presents the technology details, EDA tools, and test components utilized in this research. In this section, we describe the experimental setup, outlining the specific equipment, instruments, and their interconnections.

Along this research work, it is crucial to note the unavailability of precise electrical (spice) models for OTFTs and dual-gate OTFTs for the available technologies, that let to work directly on a layout design to fabrication and test loop. As a result, our analysis and investigations primarily relied on experimental measurements and empirical observations rather than simulations. Despite the absence of simulation capabilities, we were able to obtain valuable insights and draw meaningful conclusions through rigorous experimental testing and characterization of the OTFTs. These practical findings contribute to a comprehensive understanding of the OTFTs' performance and their suitability for the intended application, highlighting the significance of experimental approaches in the absence of precise simulation models.

3.1 Full-custom IC Design Tools

FOSS (Free and Open-Source Software) [319] tools, including schematic capture, electrical simulation, and layout edition together with the related verification tools (DRC, ERC, LVS, etc.), play a crucial role for full-custom integrated circuit (IC) design by providing cost-effective and accessible solutions for engineers and designers. Two notable FOSS tools in the layout domain that have been using in this thesis are Glade and Klayout.

Glade is a well-known FOSS freeware program that offers a complete platform for IC layout design. Creating and altering integrated circuit layouts is made easier by its user-friendly interface and selection of functionalities. Glade supports several layout formats, including GDSII, a style that's used in the semiconductor sector.

One of the key strengths of Glade is its intuitive graphical user interface (GUI), inspired in the Cadence full-custom layout EDA tool, which allows designers to interact with the layout elements easily. The GUI provides tools for placing components, creating interconnections, defining layers, and managing design rules. It also offers features for visualization, such as zooming, panning, and highlighting specific layout areas.

Glade integrates cutting-edge layout optimization methods, enabling designers to boost the effectiveness and performance of their IC designs. Design rule checking (DRC) capabilities are offered to guarantee adherence to production requirements and restrictions. Glade also supports netlist extraction, making it possible to integrate it with other electrical design automation (EDA) tools in the design flow without any issues.

Another potent FOSS software tool for IC layout design and editing is called Klayout. It has a wide range of tools and functionalities to handle complicated layout editing tasks. Klayout is compatible with common file formats since it supports a number of layout formats, including

GDSII, OASIS, and CIF. Klayout has a number of noteworthy features, including the ability to script, which enables designers to automate layout modification activities using either the built-in scripting language or external scripting languages like Python and Ruby.

Klayout provides an extensive set of editing functions, including operations for geometry modification, layer manipulation, text handling, and merging of layout elements. It supports hierarchical layout editing, allowing designers to work with large and complex IC designs efficiently. The software also includes powerful visualization tools, such as 2D and 3D rendering, that aid in understanding and analyzing the layout structure.

Table 1. Main Layout editors in EDA tools

Software	Description & Creator/owner	License/Installation
Klayout	FOOS layout editor Matthias Köfferlein	Free software
Glade	FOOS layout editor Peardrop Design Systems	Free software
LinkCAD (v8)	FOOS layout file formats conversion Bay Technology	License based
Clewin (v4)	layout editor WieWeb software	License based
LayoutEditor	layout editor Juspertor GmbH	free, reduced, full License
Tanner L-Edit IC	professional layout editor Mentor (Siemens)	Network license pool Installation guide
Virtuoso Layout Suite	professional layout suite Cadence	License based
Expert	professional layout suite Silvaco	License based
AutoCAD	mechanical drawing AutoDESK	Paid CAD tools
Solidworks	mechanical drawing Dassault Systems	Paid CAD tools
GDSII Toolbox	Matlab/Octave GDSII import module Ulf Griesmann	Free addon/ functions for Matlab/Octave
Gdspy	Python GDS import/modify module. Lucas Heitzmann	Free addon/functions for Python

Both Glade and Klayout offer a rich set of features for IC layout design, making them valuable tools in the FOSS ecosystem. Their ease of use, compatibility with industry-standard file formats, and capabilities for automation and customization make them attractive choices for designers seeking reliable and efficient solutions for IC layout and schematic design. That's the main reason to choose theses tools, initially Glade, later on Klayout for most of my designs. Along this research

we also evolved from drawing layer shapes to generate them using python scripts for almost all my layout design.

Table 1 compares various software tools that can be used for designing and editing integrated circuits (ICs). Among them, Klayout and Glade are the most popular free and open-source software (FOSS) options for IC layout. However, Glade recently launched a premium service that offers additional features and support for a fee.

3.2 Characterization and Test tools

Along this thesis I used different tools. I'm citing in this section those that are more relevant.

3.2.1 B1500 Keysight

The B1500 Keysight device was selected as the best instrument for the initial characterization of the experimental setup because of its cutting-edge characteristics and compatibility with the necessary experimental parameters. This incredibly flexible semiconductor parameter analyzer provides a broad range of measurement options, enabling accurate assessment of the electrical characteristics of transistors. It offers insightful information regarding the operation and performance of the transistors under study. [320]–[322].

An advantage of the B1500 Keysight device is its ability to handle different types of semiconductor materials, including organic thin-film transistors (OTFTs) and inorganic semiconductors. This versatility enables comprehensive analysis and comparison of various transistor types, which is crucial for evaluating their performance and suitability for specific applications.

The user-friendly interface and intuitive software of the B1500 Keysight device make it easy to control and acquire data. Its advanced measurement capabilities, such as generating I-V curves, allow for the extraction of vital information about the transistor's characteristics. These measurements play a critical role in assessing transistor behavior, efficiency, and provide valuable insights for further analysis and optimization.

Considering its features, compatibility, and measurement capabilities, the B1500 Keysight device emerges as the most suitable instrument for the initial characterization of the experimental setup. Its ability to handle different semiconductor materials, user-friendly interface, and advanced measurement capabilities make it an indispensable tool for accurately assessing the electrical properties of transistors and gaining valuable insights into their performance characteristics.

3.2.2 Digilent Analog Discovery

The Analog Discovery 2 is a multifunctional and portable test and measurement device that combines various instruments, including an oscilloscope, waveform generator, logic analyzer, and power supplies. This versatility allows for seamless integration of different measurement techniques, making it an ideal choice for conducting multiple tests on the experimental devices. Its user-friendly software interface provides intuitive control and data visualization, allowing for easy configuration of measurements and comprehensive analysis of the device under test.

The flexibility of the Analog Discovery 2 is evident in its compact size and USB-powered functioning, which enable easy setup of the experimental environment anywhere. By simply plugging the device into a computer, rapid measurements can be performed in the lab or outdoors without the need for elaborate setups or heavy equipment. This portability, combined with its comprehensive software capabilities, makes the Analog Discovery 2 the most suitable tool for conducting numerous tests in the experimental setup. It streamlines the testing process, providing detailed insights into the electrical performance of the devices and facilitating thorough evaluation and analysis. With the Analog Discovery 2, the experimental setup can undergo a wide range of tests, ensuring comprehensive characterization and understanding of the devices under investigation.

3.2.3 Rigol dp832A

The Rigol DP832A is a programmable DC power supply with a wide range of capabilities and functionality for the testing setup. To address the power needs of diverse devices and components, it includes three separate output channels that can each give up to 30 volts and 3 amps of current. Additionally, it includes an intuitive user interface and a sizable color display that make monitoring and controlling the parameters of voltage, current, and power simple.

One of the most significant features of the DP832A is its programmability, which allows for the automation of test settings and the execution of complex sequences of voltage and current outputs. This improves experiment efficiency and frees up the researcher's time for data analysis and interpretation. The power supply also includes several protection systems, such as overvoltage, overcurrent, overtemperature, and short-circuit protection, to protect both the power supply and the associated devices or components.

The DP832A also provides excellent connectivity, accuracy, stability, and advanced features. It offers USB, LAN for seamless integration with computers and remote control and monitoring capabilities. It ensures precise and accurate power delivery with high-precision voltage and current measurements, low ripple output, and waveform generation and data logging capabilities. These features contribute to the reliability, flexibility, and versatility of the power supply in achieving the desired experimental outcomes and obtaining high-quality data.[323]–[325]

3.2.4 JMP Software

JMP software, an SAS Institute offering, is a complete and engaging platform for data analysis and visualization. It allows users to access, prepare, explore, analyze, model, share, and communicate data using a variety of tools and techniques. It also supports data quality and reliability, process and product optimization, data science and machine learning, and data education and learning resources. JMP software runs on both Windows and Mac OS X operating systems and connects with other SAS products and platforms.

One of the key features of JMP software is its interactive data visualization capabilities. Users can produce and modify interactive graphs, charts, and plots that facilitate successful data analysis and sharing. Users can quickly generate visual representations of their data and alter them to highlight significant patterns or trends using a straightforward drag-and-drop interface. These interactive visualizations make it easier to make decisions based on data.

Another important feature of JMP software is its comprehensive statistical analysis tools. Users can perform various analyses and hypothesis testing, from basic descriptive statistics to advanced multivariate analysis. Users can conduct regression analysis, ANOVA, factor analysis, cluster analysis, and more, all within the JMP environment. The software's interactive nature facilitates the exploration of different analysis options and the ability to visualize the results in real-time. JMP software also offers robust data cleaning and preprocessing tools, advanced modeling and predictive analytics tools, and reporting and presentation tools. These tools help users ensure the integrity and reliability of their data, build, and evaluate predictive models, and collaborate and share their analysis results with others.

JMP software supports integration with other data sources and software applications. It can connect to various data formats, including spreadsheets, databases, and statistical file formats. JMP also provides integration with programming languages like R and Python, allowing users to leverage the capabilities of these languages within the JMP environment. JMP software has been widely adopted in industries such as healthcare, manufacturing, finance, and academia. Its versatility and comprehensive feature set make it suitable for a wide range of applications, including quality control, process improvement, experimental design, and data exploration.

3.3 System level approach to integrating EG-ISFETs arrays

This subsection is intended to show the evolution of the design approaches in which I have been involved that lead to the research proposal that we will develop in following chapters.

3.3.1 1st EG-ISFET Array

The first attempt to implement an ISFET platform was using single gate OTFT fabrication process from Neudrive Ltd. Top-gate OTFT devices from Neudrive allows fabricating sensors with a five-mask process. First, 50 nm thick gold (Au) electrodes are defined as source and drain and evaporated onto the substrate (i.e., SU-8 planarized Corning Eagle glass). After that, a 20nm organic semiconductor (OSC) layer is spin coated. Then, 300nm of Organic Gate Insulator (OGI) are deposited. Another electrode is evaporated and photo-patterned over the OGI as gate's electrode. Gate's electrode is served as an etch mask for oxygen plasma removal for surplus areas of OSC and OGI. Finally, the passivation layers are coated and patterned photolithographically to implement as vias between source/drain metal and gate electrode with interconnection[326]. The process is shown in **Figure 3**.

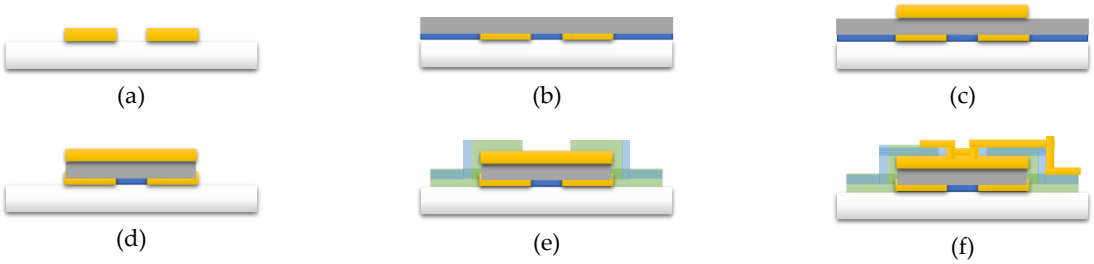


Figure 3. fabrication process of single gate OTFTs

Our first design **Figure 4** used an 8 ISFET sensor array with a reference electrode. In this design the extended gate was placed in the same chip that the ISFET. OTFTs drains and sources were connected to SoC board through a connector and a set of Op-Amps. Input Op-Amp change the digital output signal from the SoC to -3V to enter OTFT drains. OTFTs sources connect the SoC board through trans-conductance amplifiers. The SoC ADCs measure the converted voltages.

The outer metallic ring was designed with a double purpose: first, it allows biasing the reference electrode closer to the extended gate electrode and second, to check the connectivity between OTFT sensor array and the board. Thus, we can inject a signal there and sense it with the DAC of the SoC. There is also a reference OTFT (bottom) that can be used for test and calibration purposes.

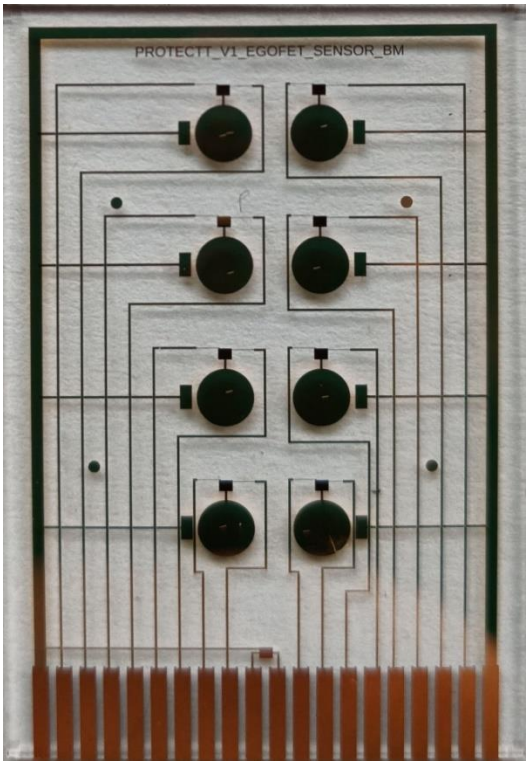


Figure 4. EG-ISFET array of 8 with a reference electrode

We selected the NXP-QN9080 (NXP, n.d.) SoC as a main component of the real-time embedded acquisition platform. QN9080 is an ultra-low power Bluetooth Low Energy (BLE) MCU with on-chip memory, USB 2.0 full-speed interface. It integrates a 32-bit ARM Cortex-M4F core with BLE (v5.0) compliant radio, link controller, host stack and GATT profiles.

The SoC has 8 ADC channels of 16 bits accuracy which can measure small changes from the sensors. To accelerate the development time, we used directly a prototyping board (NXP-QN9080DK in shown in **Figure 5**) containing that SoC. Between that prototyping board and the sensor array, we design an adaptation board, which inverts positive voltage coming from GPIOs to drive the OTFTs (shown in **Figure 6**.a). As said, OTFTs sources are connected to ADCs through a transconductance amplifier with a RC low-pass filter to reduce noise (**Figure 6**.b) shows.

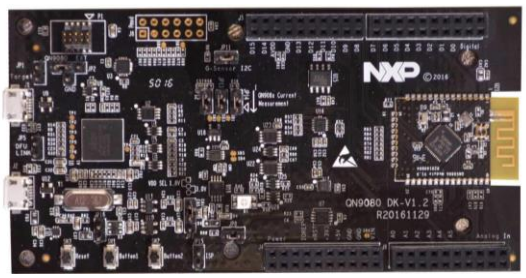
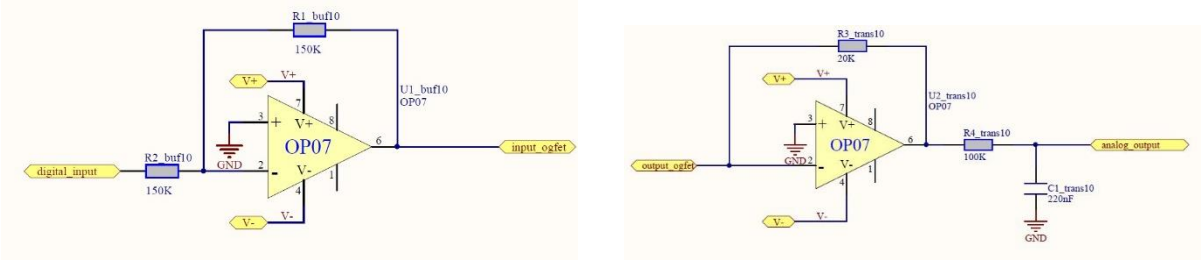


Figure 5. QN9080DK



(a) (b)

Figure 6. Voltage inverter schematic (a) and Trans-conductance schematic with 20KΩ resistor (b)

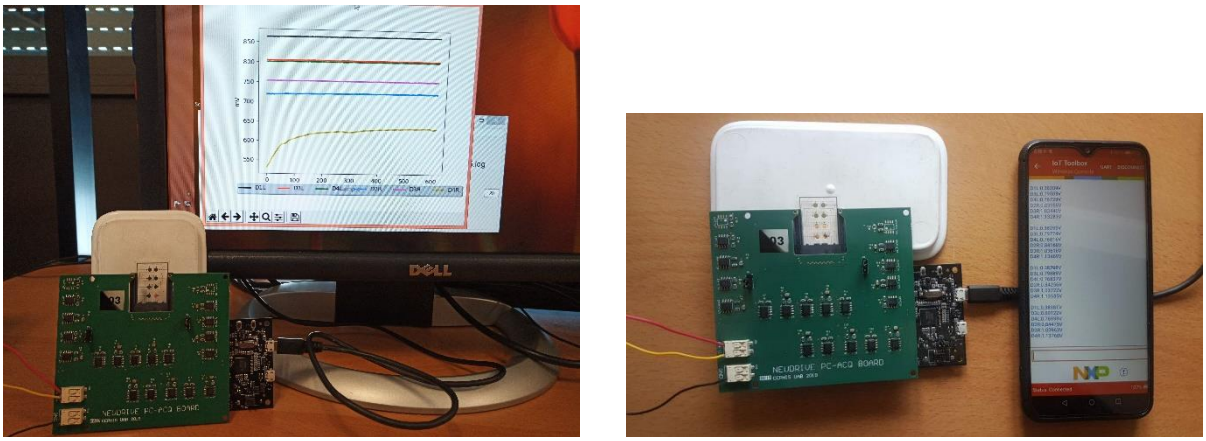
According to the actual OTFT current levels, we would like to have 50nA resolution. Thus, we need 20KΩ resistor:

$$\Delta I = \frac{\Delta V}{\mathrm{R}} = \frac{1mV}{20K\Omega} = 50nA \qquad (1)$$

The SoC ADC is set to 12 samples per second. In this implementation, we multiplex two of the channels of the array since we reserve two ADCs channels for the acquisition of the DAC value (that goes to the outer ring) and reference transistor for TFT calibration.

On this hardware platform, we have built the ARM SoC code for (1) the correct sensor connection; (2) the OTFT stimuli; (3) the OTFT response; (4) the protocol with the host (PC/Smartphone application); (5) the USB configuration and transmission; and (6) the Bluetooth configuration and transmission. We have also built the corresponding application for PC (in Python) while for the smartphone we have used the NXP app. PC USB and Smartphone Bluetooth instances are shown in **Figure 7**.a and **Figure 7**.b respectively.

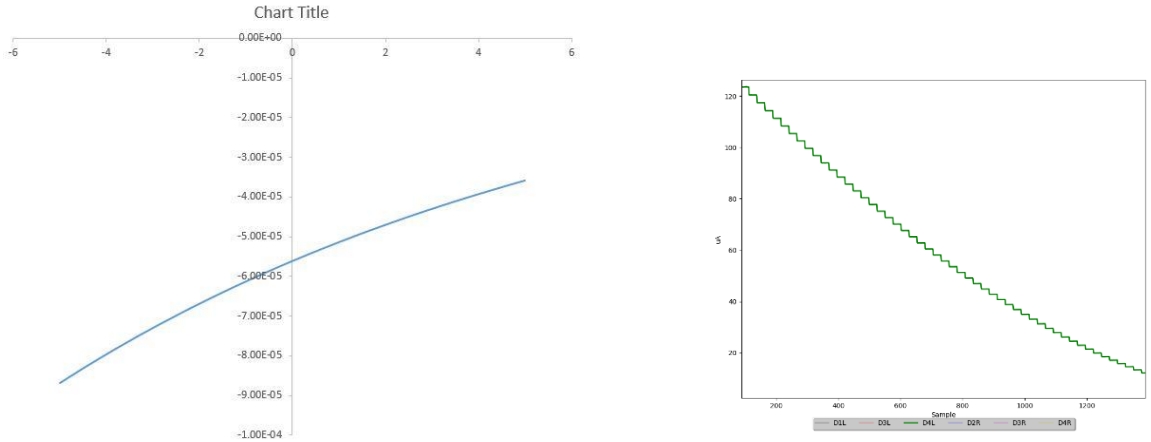
Thus, the PC software can display the values of the sources (voltage and current) in real-time and can store these values both instantaneous and average mode in two separated CSV files.



(a) (b)

Figure 7. USB connection for PC platform (a) and Bluetooth connection for smartphone platform (b)

Figure 8.a and **Figure 8**.b show the sensor currents while biasing voltages from -5V to 5V to its extended gate using a probe station and through PC software.



(a) (b)

Figure 8. Sensor current sample using Keysight B1500A (a) and PC software (b) to drive the extended gate in the range for -5V to 5V

The results obtained from Figure 6.a and Figure 6.b provide valuable insights into the accuracy of our initial system within the voltage range of -0.1V to -0.9V. The acquisition methods employed, utilizing the Keysight B1500A instrument and PC software, have demonstrated reliable and precise measurements. These findings validate the effectiveness of our approach in capturing the desired data with high precision.

However, along the course of implementing this strategy. First, we encountered restrictions in the study since we could only take measurements on a restricted number of transistors. This was mostly due to socket problems experienced while connecting the transistors to the PCB. Another difficulty we encountered was the danger of causing harm to the EG-ISFETs during the experiment. The presence of scratched lines on the EG-ISFETs resulted in their destruction, reducing the number of working devices available for testing. It was vital to develop procedures

and processes that ensured the safety and preservation of the EG-ISFETs throughout handling and experimentation, reducing the risk of damage and increasing the overall dependability of the results. Furthermore, we discovered ESD problems that hampered the system's performance. ESD can cause unintended electrical disturbances, affecting measurement precision and stability.

Due to the limits and constraints of the first strategy, a second approach was developed to overcome these concerns. The goal of this new strategy was to solve the socket concerns, prevent the destruction of EG-ISFETs due to scratched lines, and reduce the influence of ESD on the system.

3.3.2 2nd EG-ISFET array

To address the challenges and improve the overall system performance, the second approach incorporated several key elements. One notable improvement was the utilization of different substrates for the OTFTs and EG components. This distinction was crucial as it allowed for cost-effectiveness, with the disposable EG components being more affordable compared to the manufacturing of OTFTs. This approach enabled efficient and economical analysis for chemical and biological applications.

The second approach also involved IC design, specifically implementing two OTFTs per chip. This design choice provided enhanced functionality and expanded measurement capabilities. The integration of USB connection, power management, software analysis, and a prototype box further contributed to the overall system efficiency and convenience. This design is shown in **Figure 9**.

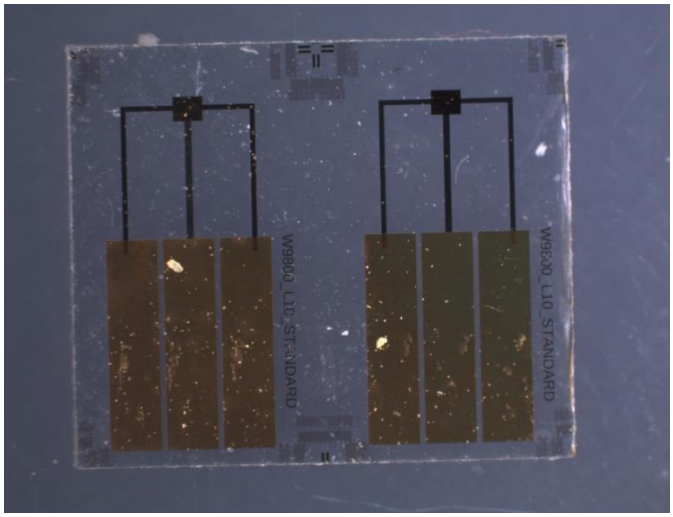
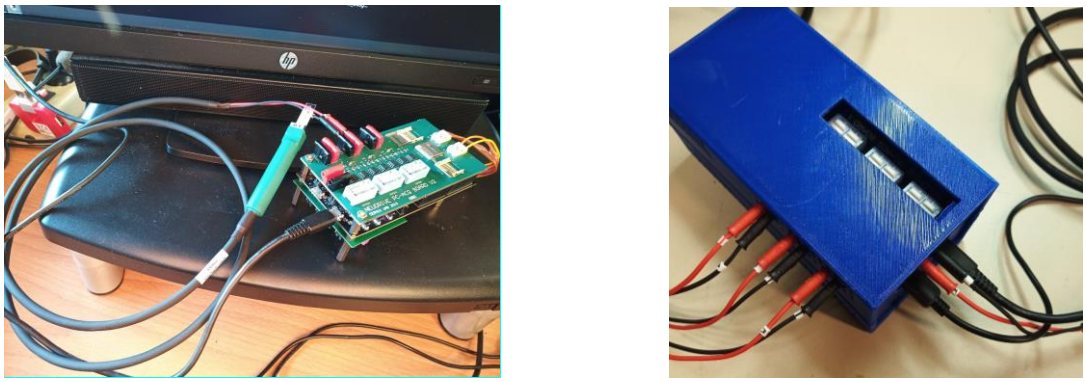


Figure 9. Two OTFTs on a chip

A notable advancement in the second approach was the ability to measure three EG-ISFETs simultaneously. This improvement was achieved by connecting the chips on the acquisition board to two electrodes, where the first electrode served as a reference and the second electrode was dedicated to the EG. This arrangement facilitated simultaneous and parallel measurements, significantly increasing the efficiency and throughput of the system.

To mitigate the risk of damage caused by ESD and eliminate the need for chip replacement, the second approach introduced the use of switches for selecting the appropriate OTFTs. This feature ensured that the system remained resilient to ESD events, reducing the chances of chip failure and improving the overall reliability of the measurement setup.

In terms of physical implementation, a mechanical box with switches was incorporated into the system. This box allowed for easy and efficient switching between different OTFTs, further enhancing the versatility and flexibility of the measurement setup. Additionally, the integration of SIM cardholders for individual replacement enabled convenient and rapid replacement of specific components when needed.



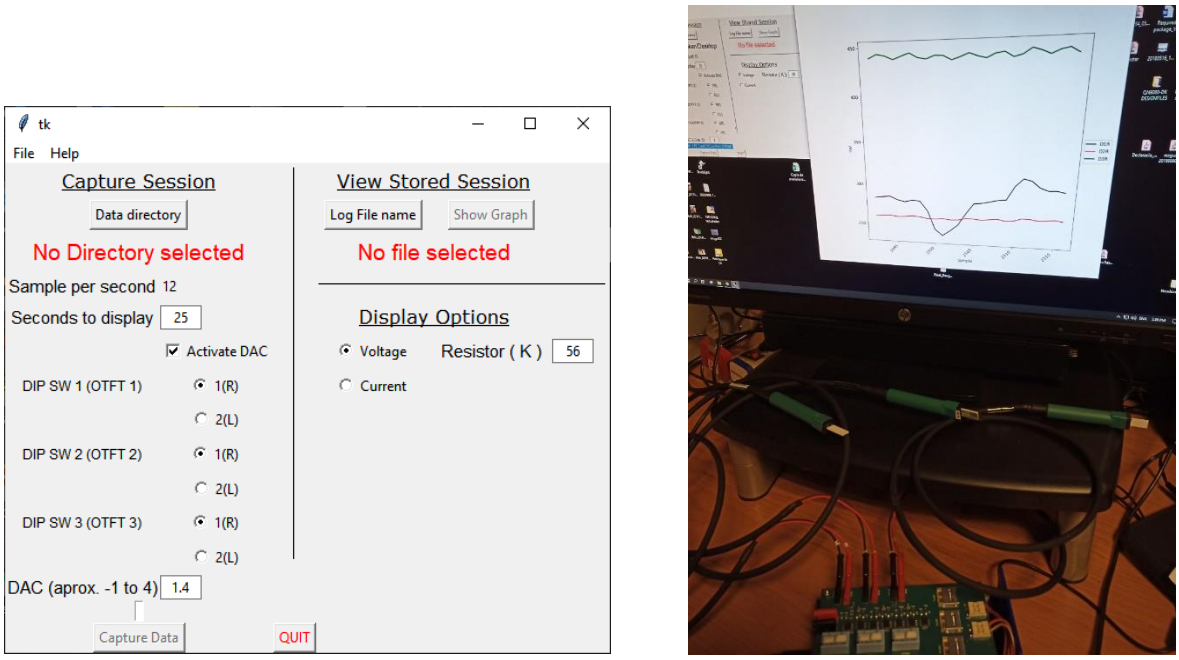
(a) (b)

Figure 10. (a) The system under test, (b) the system inside the box with all channels connected.

Figure 10.a provides a visual representation of the system under test, showcasing its components and configuration. This allows for a clear understanding of the setup and the arrangement of different channels within the system. On the other hand, **Figure 10**.b demonstrates the system with all channels connected inside a box, highlighting the comprehensive connectivity and integration achieved.

Figure 11.a showcases the software interface used in conjunction with the system. This intuitive and user-friendly interface allows for seamless control, monitoring, and data analysis. Through the software, users can easily configure test parameters, visualize real-time measurements, and extract relevant data for further analysis and interpretation. In **Figure 11**.b, a series of tests were performed on the system, exploring its capabilities and evaluating its performance under various conditions.

Despite the advantages offered by the second approach, there were still some noteworthy aspects to consider. On the positive side, the sensing process was executed accurately at the electronic level, ensuring reliable measurement results. Furthermore, for chemical measurements, collaborations with Neudrive and Indian partners provided expertise and resources, enabling comprehensive analysis in the field of chemistry.



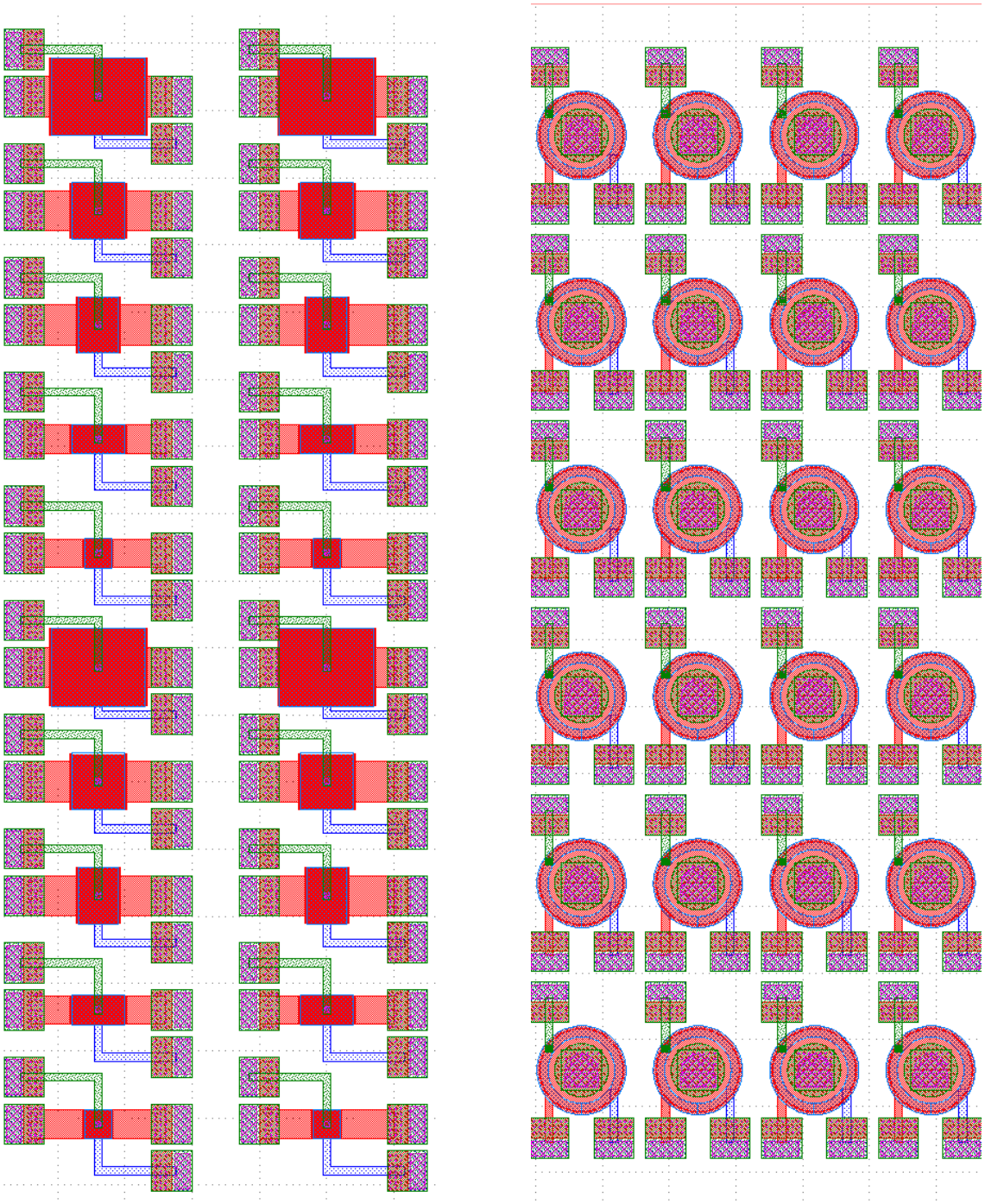
(a) (b)

Figure 11. (a) The software interface (b) the board under a test performance

However, one significant disadvantage of the second solution was reliability concerns with the physical switches. Although the switches were designed to aid in the selection of appropriate OTFTs and improve system efficiency, they faced reliability and durability difficulties. The physical switches tended to wear down over time, potentially resulting in malfunctions or incorrect measurements. This underlined the necessity for more improvements in switch design or the investigation of alternative options to assure long-term reliability.

Another issue that persisted despite the design's small size was the problem of ESD. While efforts were made to minimize the impact of ESD events by employing separated chips, the problem still persisted to some extent. ESD could adversely affect the functionality and performance of the system, potentially leading to measurement inaccuracies or chip failures. Addressing this issue would require implementing additional protective measures or exploring ESD-resistant materials or technologies to enhance the system's resilience against ESD events.

One of the problems we encountered during the testing process was related to NeuDrive's fabrication process. The stability of their process was not consistent, and their wafers exhibited unusual behavior with regards to output currents. Even when the W/L of the transistors were similar, they did not produce the same output values. During the testing process, an array of transistors fabricated by NeuDrive was evaluated, revealing numerous issues with their output. Figure 10.a and Figure 10.b show these arrays, which include transistors with different W/L. However, the behavior of these transistors did not align with our expectations. For instance, even when transistors had the same W/L, they did not consistently yield the same current on the arrays.



(a) (b)

Figure 12. (a) The array of interdigitated (b) the array of Corbinos

All these problems, including the issues with the fabrication process, have prompted us to develop a new chip proposal and collaborate with a different foundry for our work. The details of this new chip proposal will be discussed in the next chapter.

Chapter 4. A new generation of ISFET arrays

According to our previous design and test experience, we reach the conclusion that the best structure for an array of OTFT based ISFETs requires:

- Choosing a reliable fabrication process.
- Separating extended gates and reference electrodes from the ISFETs in order to separate spare parts from reusable measurement devices
- Integrating several ISFETs together with multiplexes in the same chip to allow: (i) substitute failing devices by good ones by SW and (ii) allow changing the sensitivity of the devices without changing the hardware.
- Disposing of good analog multiplexers that can block the source to drain signal when required. This cannot be done with single gate p-type OTFT.
- Establish simple communication to interface to any MCU.

This lets to the architecture shown in **Figure 2** from chapter 2.

4.1 Dual-gate OTFT fabrication process

This work uses a dual gate structure that consists of five metal masks to build ISFETs and MUXES, as shown in **Figure 13**. The structure is based on the technology of SmartKem Co. In this strategy, the first mask is used to sputter and shape Mo/Al/Mo back-gate metal by photolithography and wet etching with the thicknesses of 11nm/70nm/60nm (**Figure 13**a).

The back-gate layer was then spin coated with the base layer, which was then UV-cured (**Figure 13**b). This layer has a thickness of about 0.5 um. The second mask is devoted to gold deposition for the source and drain metals, is roughly 50nm thick and is photolithographically patterned (**Figure 13**c). Gate layer fabrication involves several stages.

Self-assembled monolayers (SAM) and organic semi-conductors (OSC) with a 30nm thickness are spin coated and baked as the initial stage (**Figure 13**d). Next, Organic Gate Insulator (OGI), (SRL) spin coating, and UV curing were applied (**Figure 13**e). The thicknesses of the OGI and SRL are 150nm and 400nm, respectively. Then, Mask 3 is used, followed by a photolithographic pattern (**Figure 13**f). All additional OGI, SAM, SPL, and OSC have been eliminated using mask 3 (**Figure 13**g). This layer is around 50 nm thick.

The remaining region is then spin coated with the passivation layer at a height of 2000 nm (**Figure 13**h). With the use of mask 4, the passivation layer copies the design using photoresist patterns. Finally, mask 5, also known as gate contact metal, is used for patterning sputtered gold, and wet etched in a technique identical to previous metal layers (**Figure 13**i).

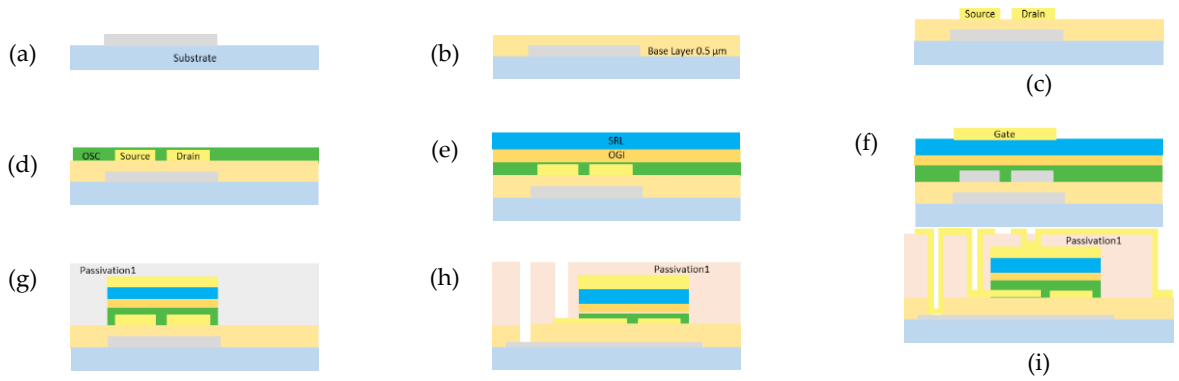


Figure 13. Different steps of mask process: (a) Fabrication of first layer (Mo/Al/Mo back-gate metal) by sputtering, photolithography and wet etching (thickness: 11 nm/70 nm/60 nm). (b) Spin coating and UV/thermal curing of base layer. (c) Sputtering, photolithography and wet etching of second metal layer. (d) Spin coating and baking of SAM and OSC layers (thickness: 30 nm OSC). (e) Spin coating and baking of OGI layer, spin coating and UV/thermal curing of SRL layer (thickness: 150 nm OGI and 400 nm SRL). (f) Sputtering, photolithography and wet etching of third metal layer (thickness: 50 nm). (g) Spin coating and UV/thermal curing of passivation layer (thickness: 2 um). (h) Patterning of passivation layer using photoresist and dry-etch transfer. (i) Sputtering, photolithography and wet etching of fifth layer.

Once we fabricated a similar set of test structures in this new process, the SmartKem chips, displayed stable results. Even so, some fabrication issues can be observed during the manufacturing process. In interdigitated transistors fabricated by SmartKem, the first row which has the smallest W/L the current flow is around 900uA when back-gate voltage is -40v. The second row which has twice W/L compared to the first row has a 1.8mA current when its back-gate voltage is -40v. This pattern has been followed by all other W/L ratios even row 5 which has W/L ten times bigger than row 1, has current ten times bigger than row 1 transistors. Corbino transistors also follow this pattern, and their current is half of row 1 of interdigitated transistors.

4.2 Design considerations

To ensure that the current passing through the MUXs does not have any significant effect on the ISFETs, a design consideration is made to adjust the width-to-length ratio (W/L) of the MUX transistors. In this approach, the W/L ratio of the MUX transistors is chosen to be larger than that of the ISFET transistors. By increasing the W/L ratio of the MUX transistors, their channel width is effectively widened relative to the channel length.

This design choice serves two important purposes. First, it helps to minimize the impact of MUX current on the operation of the ISFETs. The larger W/L ratio reduces the resistance in the MUX channels, allowing a higher current-carrying capacity and ensuring that the MUX current remains negligible compared to the ISFET current. This ensures that the ISFETs can function independently and accurately measure the ion concentrations without interference.

Second, the increased W/L ratio in the MUX transistors enables a higher current flow through the MUX channels when required. This ensures efficient switching and routing of signals in the MUX circuitry, facilitating the proper functioning of the analog multiplexing operation. By appropriately scaling the W/L ratio between the MUX and ISFET transistors, a clear separation is established

between their respective current paths, enabling reliable and accurate operation of both components within the integrated system.

In these designs, two different types of transistors have been employed: interdigitated transistors and Corbino transistors, both with various sizes. The Corbino transistors were built in parallel to increase the equivalent gain (W/L) for this type of transistor. This will be explained in more detail in the following paragraphs. The overall function of the circuit can be impacted by the performance characteristics that different transistor sizes may display. Hence, to make sure the circuit satisfies the specifications, a careful study and selection of the suitable transistor sizes are required. Increased sensitivity, improved signal-to-noise ratio, and decreased overall transistor resistance are all made possible by the simultaneous employment of Corbino transistors. Also, the ability to parallel various numbers of Corbino transistors in various areas of the circuit gives designers more choice when creating circuits with diverse requirements and standards.

The determination of the W/L for each transistor is crucial when considering the current flow through the ISFETs as calculated from equation (1)[327], [328]. The W/L ratio plays a significant role in determining the current-carrying capacity and overall performance of the ISFETs.

$$I_D = \frac{W}{L}\mu C_i \left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right] \quad (1)$$

By appropriately selecting the W/L ratio for each ISFET transistor, it is possible to optimize their electrical characteristics and ensure accurate measurement of ion concentrations. A larger W/L ratio allows for a wider channel width relative to the channel length, resulting in reduced resistance and improved current flow capability. This enhanced current capacity is particularly important in applications where the ISFETs need to handle higher currents or exhibit improved sensitivity.

The designed dies were created with four primary ideas in mind. The first design is comprised of a die containing all Corbino transistors with changing W/L ratios, whereas the second design has all interdigitated transistors with varying W/L ratios. The third design uses just identical W/L-sized interdigitated transistors. The fourth design, which combines Corbino and interdigitated transistors with comparable W/L ratios for both types, completes the set.

Achieving the desired W/L ratio for Corbino transistors can be a challenging task. To address this issue, several research papers have proposed formulations that offer guidance in determining the appropriate W/L ratio (2) where R_1 and R_2 are the inner and outer radii of the corresponding TFT, respectively[329]–[334]. In this thesis, we have adopted one such formulation to ensure accurate and consistent results.

$$\frac{W}{L} = \frac{2\pi}{\ln\frac{R_2}{R_1}} \quad (2)$$

The selected formulation, based on the recommendations from these papers, takes into account various factors such as device geometry, material properties, and desired performance characteristics. By following this formulation, we were able to establish a suitable W/L ratio for the Corbino transistors used in our study.

It is important to note that the chosen formulation serves as a starting point, and further optimization and fine-tuning may be required based on specific design requirements and experimental observations. Nonetheless, incorporating the suggested W/L ratio from reputable research papers has provided a valuable reference for achieving reliable and reproducible results in our thesis work.

Figure 14 shows the schematic circuit implemented in out chips according to the architecture presented in **Figure 2**. All OTFTs are dual-gate but they will be implemented using different topologies which will be explained later on.

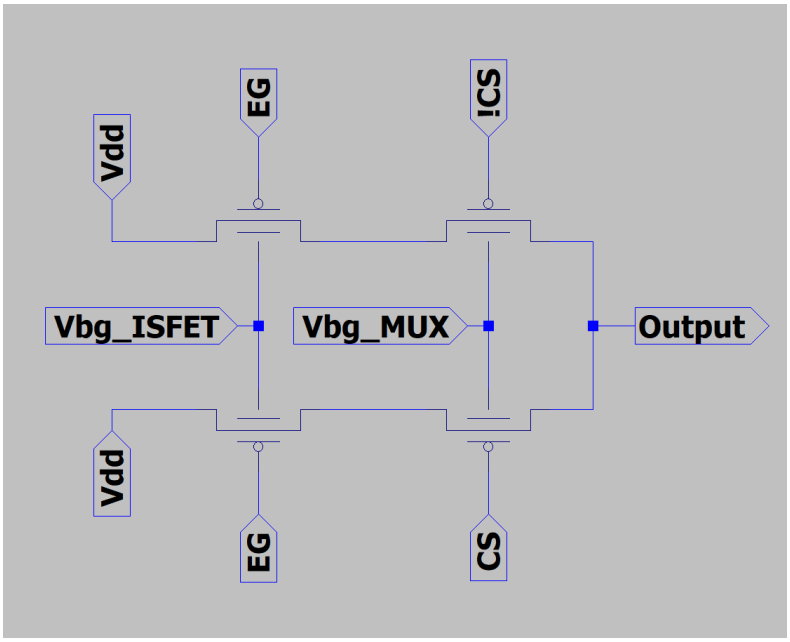


Figure 14. OTFT schematic of one eight of our sensor chips. The chip contains 8 similar structures implemented with different variants (transistor shape, dimension, etc.)

Our design strategy employs two different types of transistors for its further evaluation: interdigitated transistors and Corbino transistors, both with various sizes. The Corbino transistors were built in parallel to increase the equivalent gain (W/L) for this type of transistor (explained in more detail in the following paragraphs). The overall function of the circuit can be impacted by the performance characteristics that different transistor sizes may display. Hence, to make sure the circuit satisfies the specifications, a careful study and selection of the suitable transistor sizes are required. Increased gain, improved signal-to-noise ratio, and decreased overall transistor resistance are all made possible by the simultaneous employment of Corbino transistors. Also, the ability to parallel various numbers of Corbino transistors in various areas of the circuit gives designers more choice when creating circuits with diverse requirements and standards.

By considering the insights and recommendations from the literature, we have strived to enhance the accuracy and performance of the Corbino transistors. This approach ensures that our research aligns with established practices and contributes to the advancement of the field.

4.3 Packaging considerations

In order to ensure a consistent and standardized design approach, we opted for a unique design for all of the dies used in this thesis. To achieve this, we selected the QFN64[335]–[337] (Quad Flat No-Lead 64) design structure, which provided us with a versatile and accessible layout for our experiments and analyses. This package is shown in **Figure 15**.

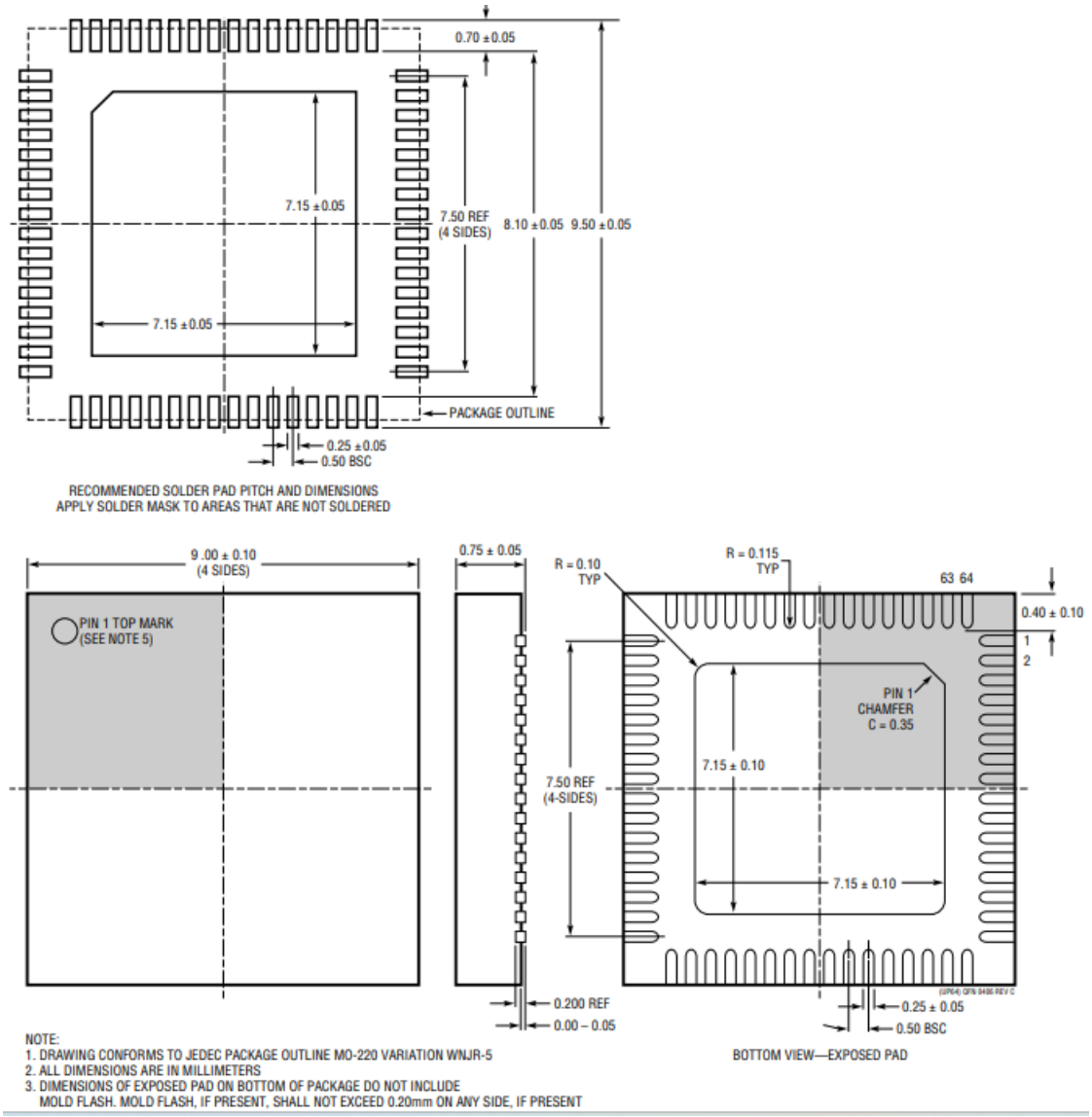


Figure 15. QFN 64-Lead package

The utilization of the QFN64 design structure offered several advantages. Firstly, it facilitated easy access to various components and test points within the die, enabling efficient probing and measurements. This accessibility played a crucial role in accurately characterizing the performance and behavior of the devices under investigation.

Furthermore, to enhance the uniformity and symmetry of the design, we implemented a quarter-repeating pattern in each corner of the die. This rotational symmetry ensured that each section of the die mirrored the others, allowing for consistent and balanced electrical properties throughout the entire device.

By adopting the QFN64 design structure and incorporating rotational symmetry, we aimed to streamline the fabrication and characterization processes while maintaining design consistency. This approach not only improved the reliability and reproducibility of our results but also facilitated comprehensive analysis and comparison across different sections and dies within the thesis.

These designs are shown in Figure 16. Corbino transistors (Figure 16.a) have been used in parallel, with varying numbers of transistors paralleled in each section. Each Corbino transistor has a size of W=1960 and L=4. The first set has four parallel Corbino transistors, the second set has eight parallel Corbino transistors, the third set has two parallel Corbino transistors, and the last set has just one parallel Corbino transistor.

Figure 16.b, the second design incorporates interdigitated transistors of varying sizes to produce varied sensitivity ranges on a single chip. The first circuit utilizes W/L ratios of 980, while the second circuit employs ratios of 1960 and the third circuit uses ratios of 3920. The final set of interdigitated transistors uses a W/L ratio of 2940 as well. The interdigitated transistor design uses a variety of W/L ratios across all of the transistors, in contrast to the Corbino transistor design, which uses parallel transistors. With this method, designers can alter the transistors' sensitivity and linearity in accordance with certain circuit needs, producing dependable and customized performance.

On the other hand, in Figure 16.c, a different design approach is adopted using interdigitated transistors with a consistent W/L ratio of 980. This design simplifies the circuit design process by eliminating the complexity of varying transistor sizes. By using matching transistor sizes, a more uniform performance across the circuit is achieved. The redundancy offered by interdigitated transistors with the same W/L ratio becomes advantageous, as it enhances circuit reliability.

In the event of a transistor failure, having identical-sized transistors allows for backup functionality, particularly critical in applications where a defective transistor can lead to severe consequences. However, it is important to note that this design strategy may limit the flexibility to customize the transistors' performance properties. Therefore, a thorough optimization of the circuit characteristics is required to strike the right balance between benefits and drawbacks, as previously discussed.

The advantages of Corbino and interdigitated transistors are combined (Figure 16.d) in the interdigitated/Corbino architecture. Corbino transistors can be chosen in this architecture from a group of interdigitated transistors using MUXs. This provides a compromise between the advantages of both types of transistors and allows for greater flexibility in circuit design.

The circuit's flexibility to accommodate varied requirements and standards is further improved using interdigitated transistors with a variety of W/L ratios and the ability to parallel varying

numbers of Corbino transistors in various regions of the circuit. The use of interdigitated transistors with the same W/L ratio also adds redundancy, enhancing the circuit's overall reliability.

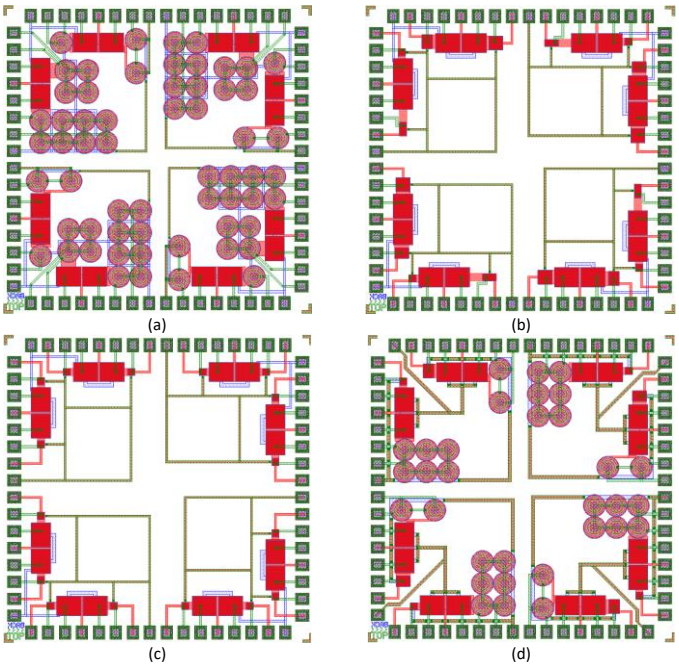


Figure 16. four designs that use the ISFET topology: (a) Corbinos with varying W/L ratios, (b) interdigitated structures with different W/L ratios, (c) interdigitated structures with similar W/L ratios, and (d) a combination of Corbinos and interdigitated structure.

A straightforward 90-degree rotation of the die can give access to similar transistors because each quarter of the dies is repeated four times on each die. This design strategy not only makes it simpler to test and characterize the transistors. Rotational access to similar transistors makes it possible to create intricate circuits that need many transistors with the same or similar properties.

The advantages of Corbino and interdigitated transistors are combined (Figure 16.d) in the interdigitated/Corbino architecture. Corbino transistors can be chosen in this architecture from a group of interdigitated transistors using MUXs. This provides a compromise between the advantages of both types of transistors and allows for greater flexibility in circuit design. The circuit's flexibility to accommodate varied requirements and standards is further improved using interdigitated transistors with a variety of W/L ratios and the ability to parallel varying numbers of Corbino transistors in various regions of the circuit. The use of interdigitated transistors with the same W/L ratio also adds redundancy, enhancing the circuit's overall reliability. **Table 2** presents the various types and sizes of W/L (width-to-length) ratios employed in this design. As evident from the data presented in **Table 2**, the corbino ISFETs occupy significantly larger areas compared to the interdigitated ISFETs.

Table 2. Different Types and Sizes of W/L Ratios in the different chips implemented.

Type	No. of transistors	W/L	Area (μm²)	Chip
Corbino	1	1960/4 = 490	445628.3072	(a)
Corbino	2 parallel	3920/4 = 980	1108114.167	(a), (d)
Corbino	4 parallel	7840/4 = 1960	1729239.002	(a)
Corbino	6 parallel	11760/4 = 2940	2596160.980	(d)
Corbino	8 parallel	15680/4 = 3920	3432244.521	(a)
Interdigitated	1	3920/4 = 980	49728	(b), (c)
Interdigitated	1	7840/4 = 1960	93240	(b)
Interdigitated	1	11760/4 = 2940	135884	(b), (d)
Interdigitated	1	15680/4 = 3920	177240	(b)

4.4 Characterization & Test

To assess the performance of the transistors in the EG-ISFET sensors and OTFT MUXs configuration, a series of preliminary characterization experiments were carried out. These experiments played a crucial role in gaining valuable insights into the behavior and efficiency of each transistor, with a specific focus on extracting its threshold voltage (V_{th}). To ensure accurate and consistent measurements, the experiments were conducted under tightly controlled environmental conditions, including fixed bias, and temperature.

By employing the B1500 Keysight and leveraging the expertise available at Integrated Circuits and Systems Testing Laboratory from the Institute of Microelectronics of Barcelona (IMB-CNM-CSIC) [338] facility, which offers cutting-edge capabilities for testing and characterization purposes, we were able to obtain comprehensive data regarding the electrical behavior of the transistors. This information was pivotal in assessing and optimizing the performance of the EG-ISFET sensors and OTFT MUXs configuration. The controlled experiments, carried out in a state-of-the-art facility, allowed us to draw meaningful conclusions about the effectiveness and efficiency of each transistor, enabling further enhancements and refinements to be made.

These preliminary tests uncovered crucial information about the functionality and behavior of each transistor. According to the results, the MUX transistors had the lowest V_{th} values, suggesting they could be the most susceptible to environmental changes. This information was instrumental in further testing and adjustment of the sensor structure.

4.5 Device Characterization

To evaluate the performance of different transistors in the EG-ISFET sensor and OTFT MUX configuration, we conducted preliminary characterization experiments. These experiments provided vital insights into the behavior and efficiency of each transistor by extracting its V_{th}, or threshold voltage. By measuring the V_{th}, we could determine the voltage at which the transistor begins to conduct and understand its operating characteristics. **Figure 17** and **Figure 18** show the arrays that are generated to measure I-V curves of transistors.

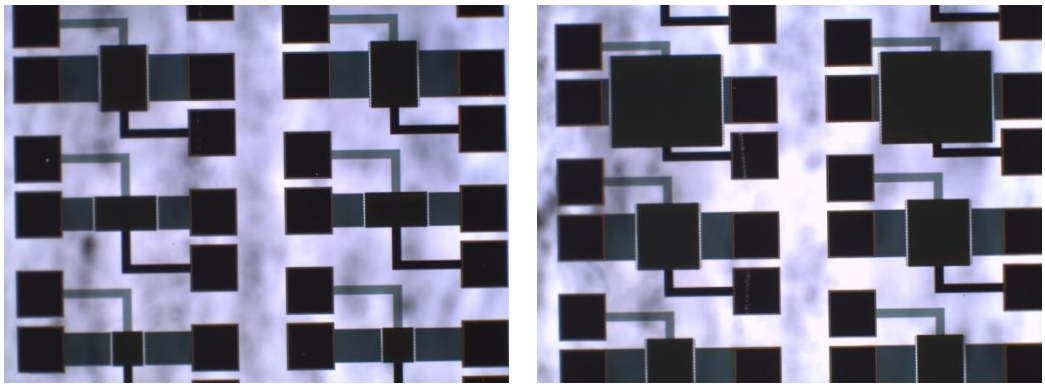


Figure 17. Photo of the fabricated array of interdigitated transistors

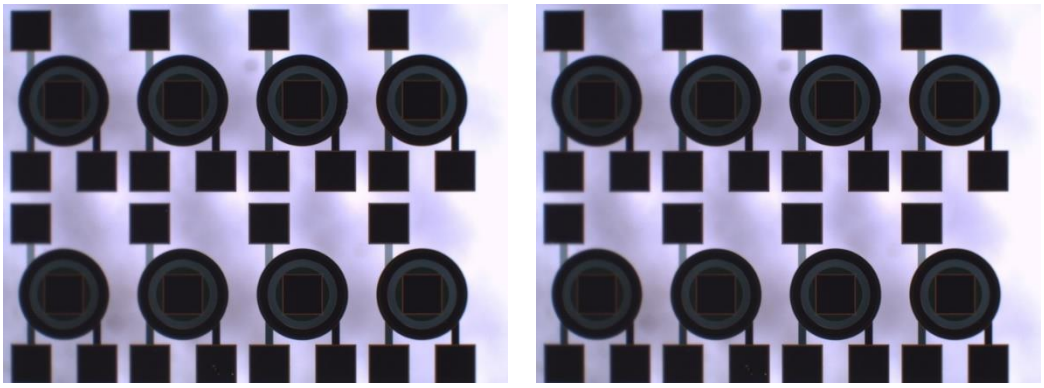


Figure 18. Photo of the fabricated array of Corbinos

The preliminary characterization experiments were conducted in controlled environments with fixed bias. This ensured consistent and reproducible results, allowing us to compare the performance of each transistor accurately. The experiments involved applying varying voltages to the transistors while monitoring their response, specifically focusing on the V_{th} values. These preliminary tests uncovered crucial information about the functionality and behavior of each transistor. By analyzing the V_{th} values, we gained insights into the electrical properties and sensitivity of the transistors.

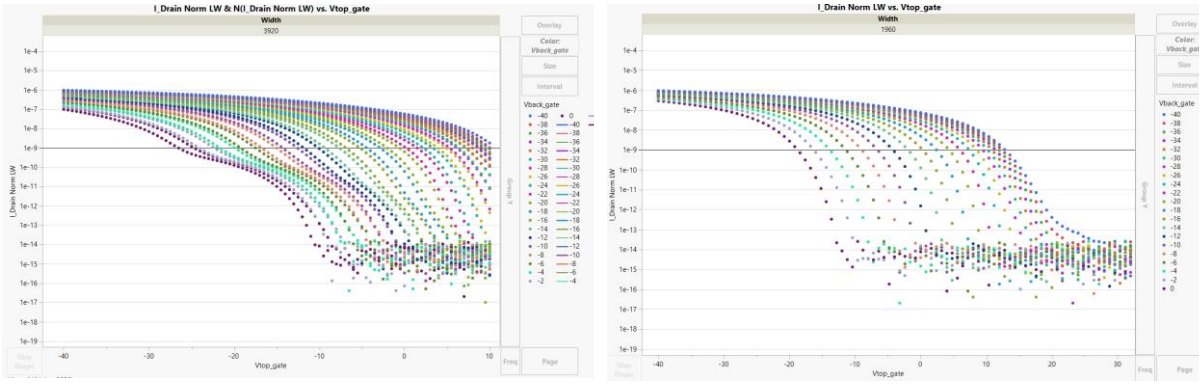
Once we obtained the V_{th} values for each transistor in our EG-ISFET sensor and OTFT MUX configuration, we were able to determine the optimal effective voltages. To enhance the gain and precision of the sensor, we selected the most effective voltages for each transistor. Our careful selection of voltages ensured that the sensor could detect even the smallest changes in its environment. To ensure the sensor's optimal performance in a variety of real-world applications, we employed these adjusted voltages in additional testing and calibration of the sensor.

To enhance the sensitivity and precision of the sensor, we carefully selected the most effective voltages for each transistor based on their V_{th} values. These optimized voltage levels were chosen to ensure that the transistors operated within their desired range, maximizing their performance and sensitivity. By utilizing these adjusted voltages, we aimed to improve the overall performance of the sensor in detecting and measuring target analytes.

To validate the effectiveness of the adjusted voltages and ensure the sensor's optimal performance in a variety of real-world applications, we conducted additional testing and calibration. This involved subjecting the sensor to different environmental conditions and measuring its response. By comparing the obtained results with the expected values, we could assess the accuracy and reliability of the sensor.

The I-V curve illustrates the relationship between the applied voltage and the resulting current flowing through the transistors. Based on the obtained results, a clear relationship between the V_{th} and the back-gate voltage ($V_{back\text{-}gate}$) of the transistors can be observed. It is evident that as the $V_{back\text{-}gate}$ voltage increases, the V_{th} of the transistors decreases. The decrease in V_{th} with an increase in $V_{back\text{-}gate}$ voltage suggests that a higher back-gate voltage facilitates the conduction of current through the transistors at lower applied voltages. This finding has practical implications for device design and operation, as it indicates that adjusting the back-gate voltage can effectively modulate the transistor's behavior and optimize its performance.

These preliminary tests uncovered crucial information about the functionality and behavior of each transistor. During this test, the voltage of V_{dd} was maintained at a fixed value of -5V. The $V_{back\text{-}gate}$ and $V_{top\text{-}gate}$ of the OTFTs were systematically varied to extract the V_{th} of each transistor. This information was instrumental in further testing and adjustment of the sensor structure. As the back gate voltage decreases, the threshold voltage increases. This behavior is evident in the data presented in **Table 3**, where the results for a back gate voltage of -38V are provided. According to the definition, $V_{th,1nA}$ represents the gate voltage intercept when the drain current is equal to 1nA for a specific channel length (L) and width (W). In **Figure 19**.a, the I-V curve illustrates that a drain current of 1nA intersects with the curve at a gate voltage of 9.5V when the back gate voltage is set to -38V. This behavior is observed consistently across the other OTFT structures tested. However, an interesting observation can be made when the $V_{back\text{-}gate}$ is increased to 0. In this case, it becomes evident that the interdigitated transistor with double the channel width experiences significant stress and ultimately fails under the same voltage condition of -27V. On the other hand, the corbinos structure (**Figure 19**.b) demonstrates remarkable stability under different $V_{back\text{-}gate}$ and $V_{top\text{-}gate}$ conditions. The corbinos configuration, with its distinct design and electrode arrangement, exhibits a robust performance and maintains its functionality even under varying voltage biases.



(a) (b)

Figure 19. I-V curves for interdigitated OTFTs with W/L = 3920/4

Table 3. Variation in V_{th} for OTFTs at $V_{back\text{-}gate}$ = -38V

Type	W/L	$V_{th,1nAmean}$(V)
Corbino	490	12.8±6%
Interdigitated	980	9.5±5%
Interdigitated	1960	9.6±5%
Interdigitated	2940	9.7±5%
Interdigitated	3920	9.8±5%
Interdigitated (MUX)	9800	9.9±5%

The extraction script used to obtain the V_{th} values from the I-V curves is provided in Appendix A. This script serves as a valuable tool in automating the data extraction process, ensuring accuracy and efficiency. By following the steps outlined in the script, researchers and practitioners can replicate the V_{th} extraction procedure and obtain consistent results. The script incorporates the necessary calculations and algorithms to extract the threshold voltage from the I-V curve data, considering the specific characteristics and parameters of the transistors under investigation. Its inclusion in the appendix allows for easy reference and provides transparency in the research methodology.

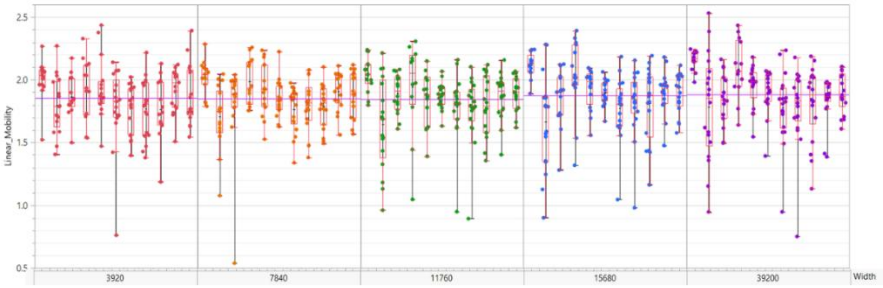
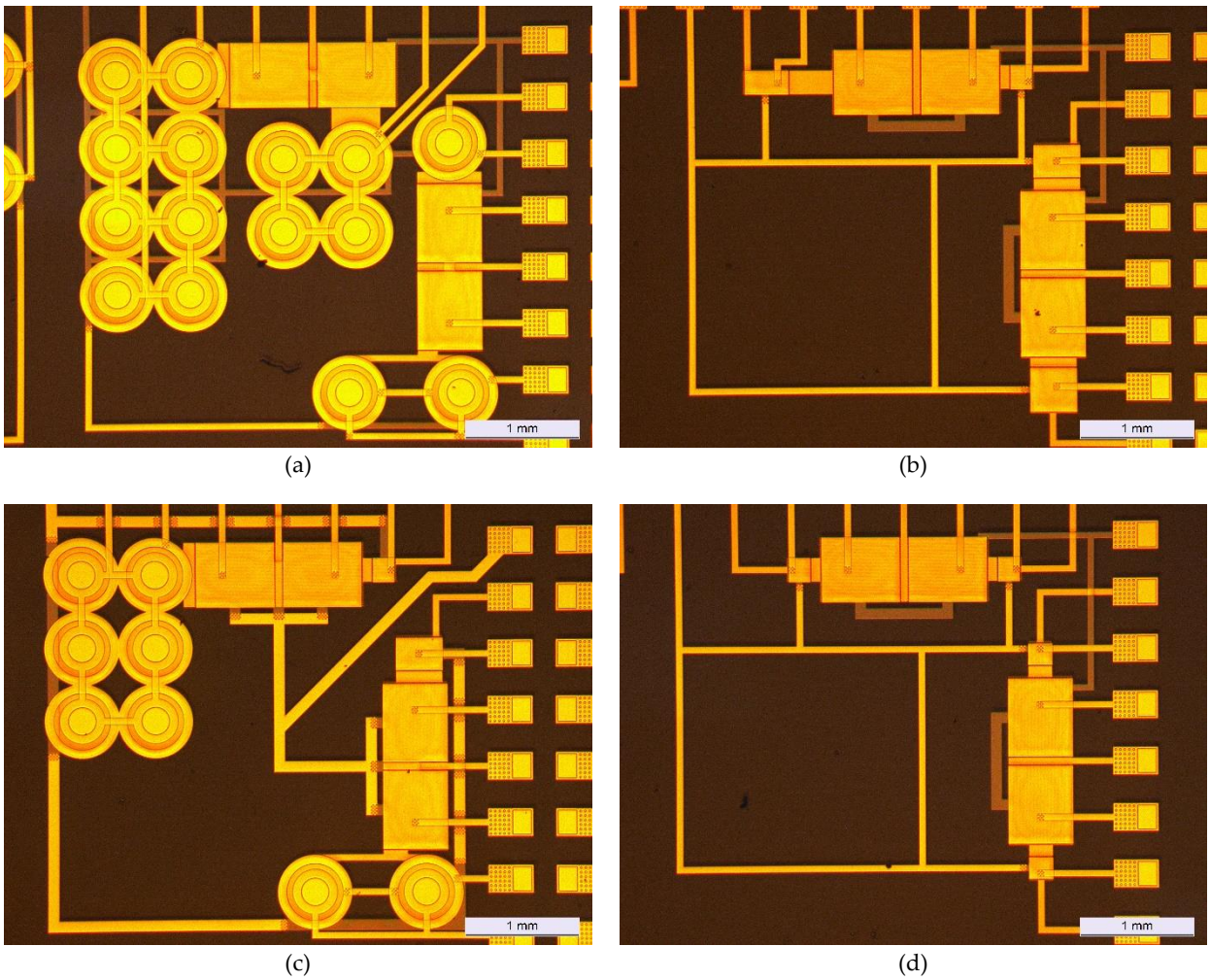


Figure 20. Mobility test of dual gate transistors

Figure 21 illustrates the fabricated design for different dies, showcasing the variations and diversity in the physical realization of the design across multiple instances. **Figure 22** shows the fabricated dies, which have been successfully produced on a 4-inch glass substrate provided by SmartKem.

The code found in Appendix B serves the purpose of generating interdigitated designs within the Glade software. It provides the necessary code to create intricate interdigitated patterns efficiently. By referring to this code, users can replicate or modify interdigitated designs with ease, enhancing their productivity and flexibility in the design process.



(a) (b)

(c) (d)

Figure 21. fabricated dies by SmartKem (a) all-corbinos design (b) all-interdigitated with different W/L ratio design (c) interdigitated/corbino design (d) all-interdigitated with same W/L ratio design

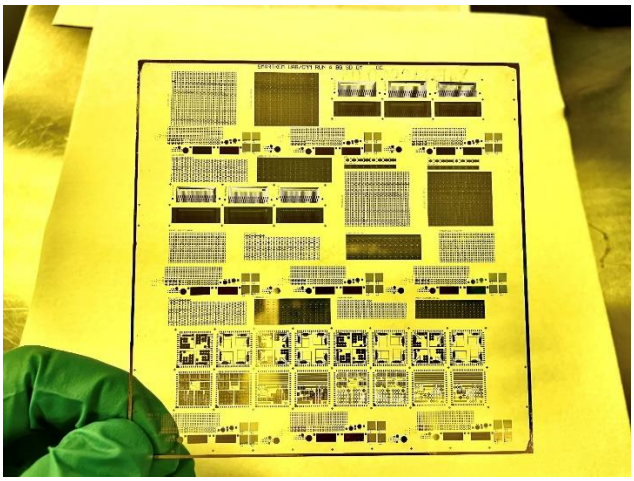


Figure 22. Fabricated dies on a 4inch square substrate

4.6 Performance Tests

In this section, we will delve into the performance of the conducted tests and thoroughly examine the obtained results. We will analyze the data to gain a deeper understanding of the outcomes and draw meaningful insights from them. The results obtained from the tests will be subjected to comprehensive analysis, enabling us to explore the underlying trends and patterns.

The performed tests have provided valuable insights into the behavior and characteristics of the components under investigation. By carefully examining the obtained results, we can uncover important information regarding their performance and functionality. The analysis will involve studying various parameters, such as current-voltage (I-V) curves, threshold voltage (V_{th}), and other relevant measurements. These results will be crucial in evaluating the suitability and effectiveness of the tested components for their intended applications.

Through meticulous data analysis, we will aim to draw meaningful conclusions and identify any noteworthy observations or trends. The obtained results will be compared and contrasted, enabling us to identify any significant variations or dependencies. By delving deeper into the data, we can gain a comprehensive understanding of the behavior of the components and make informed interpretations. This analysis will serve as a foundation for further optimization and refinement of the components, allowing for enhanced performance and functionality.

To evaluate the operational capabilities of the MUX and EG-ISFET sensors, our experimental setup involved the utilization of the Analog Discovery 2 [339] in conjunction with a standard power supply unit. In order to establish a consistent measurement system, we maintained fixed voltages for V_{DD}, V_{SS}, and V_{BG}. By configuring the measurement system accordingly, we systematically varied the voltage applied to the top gate of the EG-ISFET sensor and concurrently measured the resulting output current. At each step of the voltage sweep, we diligently recorded the corresponding values to capture the comprehensive characteristics of the sensor. Throughout the testing process, we ensured the uninterrupted connection of each sensor to the MUX, thus enabling reliable and continuous data collection. Notably, the experimental tests were conducted under controlled UV-light conditions, known to enhance the performance of OTFTs and provide a more representative assessment of their functionality.

The primary objective of the sensor circuit functionality test was to validate the proper functioning of both the EG-ISFET sensor and the analog MUX. To achieve this, we meticulously examined the performance of the MUX in terms of its ability to effectively control the signal flow originating from the various OTFT sensors. Additionally, we verified the accuracy of the transfer function between each OTFT MUX channel and the resulting output current. This transfer function was assessed by measuring the voltage across a resistor load. This comprehensive testing process enabled us to confidently ascertain the overall functionality and performance of the EG-ISFET sensor and analog MUX within the sensor circuit.

4.6.1 Multiplexing function

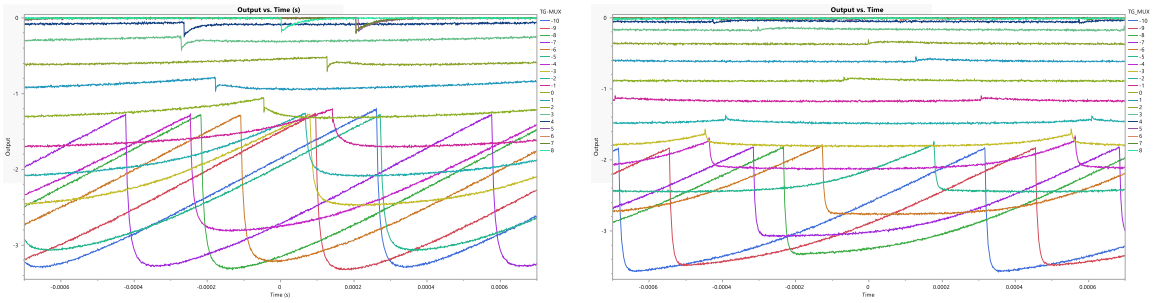
MUX OTFTs have been designed such that their W/L is much larger than the ISFET one to maximize sensitivity. All our designs have the same size W/L = 39200/4 (all dimensions are µm).

To test the multiplexing function, we set the voltages in the electrical nodes of schematic of our sensors represented in section 4 and according to the **Table 4**. And to convert the output current to a measurable voltage, a 1MΩ resistor was utilized during the testing phase. This resistor served the purpose of converting the varying current signals into corresponding voltage values. The obtained results, depicted in **Figure 23**, demonstrated the behavior of the input signal applied to the EG-ISFET electrode as it passed through the MUX under different control voltage conditions.

When the control voltage of the MUX was set to -10V, representing an "on" state, the input signal (-5V to +5V ramp signal) experienced maximum output range as indicated by the bottom blue curve in Figure 6. Conversely, when the MUX voltage reached +8V, indicating an "off" state, the output range was reduced to a minimum of 0±0.01V, as shown by the top green curve. This behavior confirmed that the MUX effectively blocked the input signal from reaching the output in the "off" state, while allowing it to pass through and achieve the maximum output range in the "on" state. To ensure clarity in **Figure 23** and highlight the behavior of the output signal, the applied input ramp signals for the various MUX control voltages were intentionally misaligned and not included in the illustration. This decision was made to better illustrate the distinctive output signal response corresponding to different MUX control voltage settings.

Table 4. Input values ranges for multiplexer test (dynamic)

I/O	Dir.	Unit	Value
V_{DD}	Input	Voltage	-5
$V_{BG,mux}$	Input	Voltage	-38
$V_{BG,sensor}$	Input	Voltage	-38
$V_{TG,mux}$	Input	Voltage	-10 ~ +8
$V_{TG,sensor}$	Input	Voltage	-5 ~ +5
Source	Output	Current	Measure



(a) (b)

Figure 23. Signal propagation from the EG-ISFET gate to the output of the MUX for different top-gate voltages and (a) an interdigitated and (b) a Corbino topology (W/L = 3920/4 for both)

Corbino transistors exhibit a faster response from input to output compared to other transistor configurations. This characteristic is manifested by the presence of less curved responses in the output. The reason behind this behavior lies in the larger output capacitance per width of the Interdigitated topologies employed in Corbino transistors. The larger output capacitance per width in the Interdigitated topologies allows for a more efficient transfer of signals from the input to the

output. This increased capacitance enables a higher rate of charge/discharge, resulting in a faster response time. As a result, the output waveform of Corbino transistors appears less curved, indicating a more direct and rapid transition from the input to the output. By leveraging the advantages of the Interdigitated topologies, Corbino transistors demonstrate enhanced performance in terms of speed and responsiveness. This makes them a favorable choice in applications where fast signal processing and efficient signal transfer are crucial.

4.6.2 Global sensing function

In this section, our objective is to examine the global transfer function that describes the relationship between the voltage applied to the input of the ISFET and the resulting output current after passing through the analog MUX. To facilitate this analysis, we employ a 1MΩ resistor at the output, which enables us to convert the output current into a corresponding voltage. This conversion is essential for obtaining accurate transconductance values for each of the circuit designs under evaluation. The outcomes of these tests are presented in **Figure 24**, where each bar represents the output current observed when the input signal is a square spanning from -5V to 5V. By analyzing the variations in output current for different input voltage levels, we can determine the transconductance values, which allows us to evaluate the effectiveness and efficiency of the circuit designs.

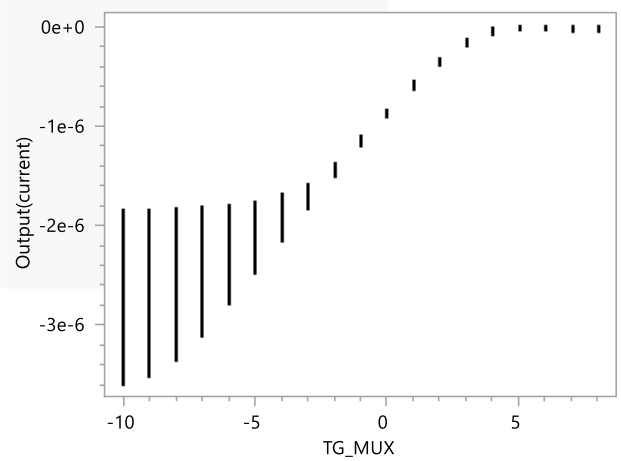


Figure 24. Global transfer function results showing the relationship between the input voltage applied to the ISFET and the corresponding output current after passing through the analog MUX.

4.6.3 Transconductance results

The Transconductance findings from the experimental measurements are shown in the **Table 5**. Brotherton [340] suggested calculating the transconductance (g_m) based on the following formula:

$$g_m \equiv \frac{dI_d}{dV_G} = \frac{\mu_n W C_i V_D}{L}$$

By considering a capacitance value of C_i = 6 nf/cm^2, we can calculate the transconductance for different transistor designs. By calculating the transconductance, we can assess the effectiveness of the transistor in controlling the flow of current through the channel.

Table 5 shows the summary of these findings offers a thorough comparison of the improvements made by various design configurations during the final test. The table makes it simple to evaluate each design's performance and makes it easier to determine which design is the most profitable. It is possible to learn a lot about the amplification potential and effectiveness of the various configurations by analyzing the gains made by each design. For assessing and choosing the best design for a given application, the gain values achieved are crucial information. Measurements have been done on 8 different chips fabricated in the same run.

Table 5. Transconductance comparison between different design under $V_{TG, MUX}$ = -10

No.	Design topology	g_m
1	1 Corbino (W/L=1960/4)	1.18e-07±5%
2	2 Corbinos (W/L=3920/4)	1.21e-07±5%
3	4 Corbinos (W/L=7840/4)	1.44e-07±5%
4	6 Corbinos (W/L=11760/4)	1.35e-07±5%
6	Interdigitated (W/L=3920/4)	1.49e-07±5%
7	Interdigitated (W/L=7840/4)	1.47e-07±5%
8	Interdigitated (W/L=11760/4)	1.09e-07±5%

Measurements for both the 8 corbinos (5.76e-08±5%) and large (W/L=15680/4) interdigitated (8.90e-08±5%) designs exhibit a decrease in the output voltage, suggesting that the input voltage needs to be lower than -5V to achieve maximum output range and the corresponding accurate transconductance.

4.7 Further advantages

Modern IC fabrication in the CMOS technology nodes requires a lot of power and has a significant environmental impact [68]. Smartkem offers a more energy-efficient and eco-friendly alternative with its organic electronics process. Moreover, Smartkem organic electronics process involves organic materials and fewer steps than the CMOS process, which reduces the greenhouse emissions.

One of the most scalable and efficient techniques for coating large areas with minimal material loss is slot-die coating, which is widely used in display production lines. Smartkem inks are designed for slot-die or spin coating, but they can also be adapted for digital printing (ink-jet) with further development to achieve the same high uniformity. The spin coated OTFT devices have mobilities of 2.5cm^2/Vs at short channel with low variability (<10%) and turn on voltage of +2V to +4V (on single gate transistors). The baking steps for the semiconductor and dielectric are mainly for solvent evaporation, so they can be easily reduced without affecting the performance or stability of the transistors. The technology is focused on the redesign of cross-linking chemistry of the passivation material, which can be replaced by more intense UV light exposure and lower temperature baking while the rest of fabrication steps can be changed without any measured impact , and the photolithographic ones lowered in temperature with acceptable changes in dimension of processed features.

It has recently demonstrated the lowering of the complete fabrication process temperature from 180˚C down to 80˚C [69]. This ecofriendly fabrication process will: (1) require overall lower energy use in manufacturing (since no PECVD is required); (2) use wider choice of plastics with improved properties concerning transparency, biodegradability (<12 months), bio-derived (e.g. cellulose), low-cost and (3) be able to be integrated with other processes without destroying their devices (e.g. OTFT backplane could be processed on top of the OLED device) that also open potential for R2R manufacturing.

Smartkem is one of the first companies to enable digital design on OFETs (organic field-effect transistors) with non-complimentary logic and 3V power supplies. This creates new opportunities for fully designing OE (organic electronics) computers, but these computers require rethinking all design decisions from scratch.

Smartkem devices fabricated on flexible substrates show good performance with bending [70] what allows adapting their sensors and circuits to different environments (wearables, industrial, etc.). A less than 18% positive V_T shift in OTFT devices is observed in the atmosphere under different bending conditions. That degradation comes from two mechanisms: the contribution of oxygen for a positive V_T shift and the contribution of mechanical tensile bending stress for a negative one. The main difference in degradation is the change in the molecular distance due to different bending conditions (tensile/compressive).

Figure 25 illustrates our design (together with other designs) implemented on a PEN (polyethylene naphthalate) substrate. The PEN substrate offers several advantages, such as flexibility, durability, and chemical resistance, making it suitable for various applications in flexible electronics. By utilizing the PEN substrate, the overall device becomes lightweight and bendable, allowing for seamless integration into wearable devices, flexible displays, and other portable electronic systems. The implementation on PEN demonstrates the feasibility of fabricating complex electronic circuits on flexible substrates, opening up new possibilities for the development of flexible and portable electronic devices.

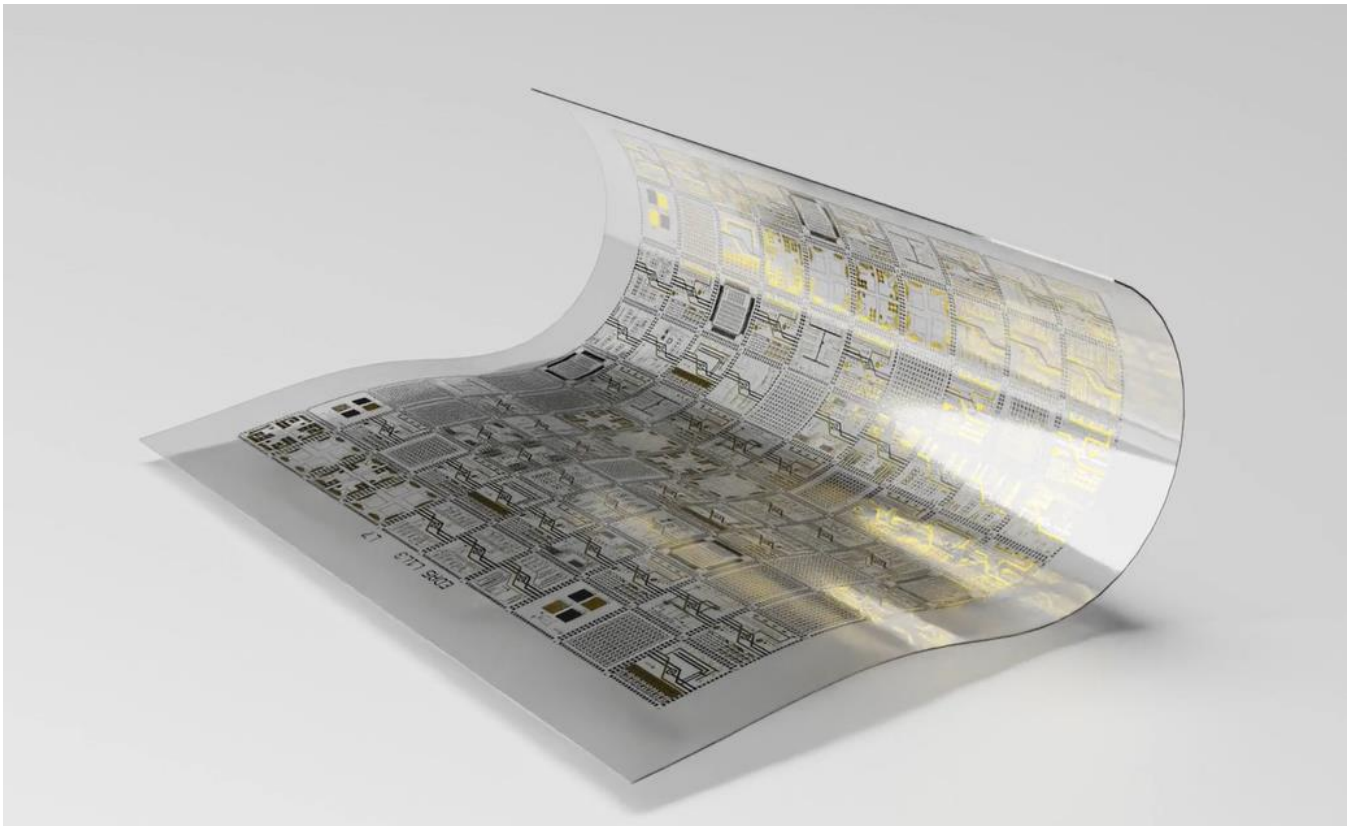


Figure 25. Implementation of several designs (including our sensors) on a flexible PEN substrate from Smartkem.

Chapter 5. Towards building more complex EG-ISFET arrays

In order to build more complex arrays with some digital control management embedded into the same chip, we started building a set of digital cells (library) aimed to be used on a classical back-end ASIC design flow. This way we will be able not only to handle the control of the multiplexing signals but also to embed a digital core to communicate with MCUs with a reduced number of input-output signals using common light protocols such as I2C or SPI.

Building that PDK requires several steps: (1) Defining a set of rules that will be common for all cells in the library (such as a common cell height); (2) Deciding the set of cells available in de cell library; (3) Designing the layout of these cells; (4) Fabricating and characterizing the performance parameters of the cells (capacitances, delays, energy consumption); and (5) building de set of files required but the IC design tools since all tools use almost the same format and data structures.

In this way, technology-specific data is converted by semiconductor foundries into a set of library files and programming scripts that may be used with commercial Electronic Design Automation (EDA) products [341]. A process design kit (PDK) is what these scripts and libraries are known as specifically.

Even that Moore's law seems to be ending for the silicon microelectronics when reaching the physical limits for devices, the evolution of silicon microelectronics is still alive nowadays as a worldwide deployment of foundries from major companies (TSMC, Intel, Global Foundries, Samsung, …) of advanced technology nodes as formerly predicted by International Technology Roadmap for Semiconductors (ITRS) and currently by International Roadmap for Devices and Systems (IRDS) [342]. Consequently, EDA tools and virtual components (IP) complexity has been evolving following the wave of manufacturing technologies also increasing complexity and cost.

Consequently, IC design and related training at under-graduate and post-graduate studies got difficult to follow that wave, even if the EDA tool providers facilitate tool and methodology trainings. Something similar happened with research activity due to the high cost of the tight chain founder-EDA-IP that require a many-man-power effort to build complex chips for research validation purposes, except for the cases when FPGAs can be used, with the corresponding penalty in energy, speed and portability.

To answer this problem several initiatives appeared that have been quickly diffused among the university research community. I grouped those different initiatives as OpenHW.

First great initiative was the offer of free silicon access through the eFabless.com Open MPW Program, sponsored by Google, on Open-source PdK for the 130nm CMOS from Skywater[343], As said by them, the shuttle program is open to anyone, provided that their project is fully open source and meets the other program requirements. Costs for fabrication, packaging, evaluation boards and shipping are covered by Google. Its currently in its 7th edition.

Second even great initiative was to integrate different existing open-source tools to build consistent EDA tool chains and methodologies for back-end digital design. OpenLane[344], [345], derived

from the OpenRoad project[346], consisting in integrating different existing open-source tools on a reliable methodology to build digital circuits from technology independent HDL (Verilog) descriptions. The success of the eFabless.com Open MPW Program is partly due to the use of OpenLane to build the circuits on the Skywater open source 130nm PDK. The Google SkyWater 130A open source PDK, is a joint venture between Google and SkyWater Technology foundry. It is used by OpenLane as its default PDK and provides a fully open-source Process Design Kit and associated materials. Designs can be created using this PDK to be later manufactured at SkyWater's facilities.

Third world-wide initiative is the widely diffused royalty-free open ISA for RISC-V [347] with many different deployment resources (e.g., HDL HW code, SW & OS resources, prototyping & deployment platforms). It boosted up the research of architectures and implementations for different domains: from ultra-low power devices (e.g., Pulpino [348] or SERV [349] platforms) to high-performance computer (HPC) oriented to vectorial processing (e.g.,[350]).

We strongly believe that the field of flexible digital electronic circuits can greatly benefit from the current wave of technological advancements, making their implementation more accessible and increasing their widespread adoption. One key advantage of these circuits is their expected low fabrication cost, which can significantly reduce the traditionally high costs associated with Application-Specific Integrated Circuits (ASICs) and provide easier access to virtual components for rapid system development, albeit with less complexity compared to silicon-based counterparts.

To support this vision, we have embarked on a project to develop open-source PDKs and customize EDA tools specifically for flexible digital circuits. Our initial focus is on building a 2.5µm PDK based on the Smartkem PMOS process, along with tailoring it to seamlessly integrate with the OpenLane EDA tools and with the goal of incorporating a RISC-V instance. Through these efforts, we aim to encourage a transition from traditional silicon designers to the realm of flexible digital integrated circuits, particularly in the realms of education and research.

By providing open-source PDKs and adapting EDA tools, we hope to democratize the development and utilization of flexible digital circuits, empowering a broader community of designers and researchers to explore their potential. This initiative seeks to foster innovation, collaboration, and knowledge-sharing in the field while driving advancements in flexible electronics.

5.1 Digital circuits with flexible organic electronics technologies

The history of digital IC implementations allows analysing their increase in according to technology evolution that impacts transistor count and transistor density. Initial circuits were implemented in PMOS or NMOS processes and later CMOS has been predominant. Remember that their corresponding transistor count per n input inverting gate is (n+1) in NMOS and 2n in CMOS. Looking at the implementations reported at the Wikipedia [351] and selecting only those below 800nm (shown in **Table 6**) we can get an estimate based on the CPUs released to the market.

Table 6. Early silicon CPU implementations

Processor	Tr count	Date	Tech (nm)	Area (mm^2)	Tr density
Intel 4004	2250	1971	10000	12	188
Intel 8008	3500	1972	10000	14	250
Intel 4040	3000	1974	10000	12	250
TMS 1000	8000	1974	8000	11	727
MOS Tech 6502	4528	1975	8000	21	216
Toshiba TLCS-12	11000	1973	6000	32	344
Motorola 6800	4100	1974	6000	16	256
Intel 8080	6000	1974	6000	20	300
Motorola 6809	9000	1978	5000	21	429
RCA 1802	5000	1976	5000	27	185
Zilog Z80	8500	1976	4000	18	472
Motorola 68000	68000	1979	3500	44	1545
Intel 8085	6500	1976	3000	20	325
Intel 8086	29000	1978	3000	33	879
Intel 8088	29000	1979	3000	33	879
WDC 65C02	11500	1981	3000	6	1917
Intel 80186	55000	1982	3000	60	917
WDC 65C816	22000	1983	3000	9	2444
ARM 1	25000	1985	3000	50	500
Motorola 68020	190000	1984	2000	85	2235
ARM 2	27000	1986	2000	30	893
Intel 80386	275000	1985	1500	104	2644
Intel 80286	134000	1982	1500	49	2735
DEC MultiTitan	180000	1988	1500	61	2951
ARM 3	310000	1989	1500	87	3563
R4000	1350000	1991	1000	213	6338
Motorola 68030	273000	1987	800	102	2676
Intel i960CA	600000	1989	800	143	4196
Hitachi SH-1	600000	1992	800	10	60000
Pentium	3100000	1993	800	294	10544

If we look at the circuit implementations published using organic electronics technologies in ***Table 7***, we can observe that they are far from these number probably because they include few memories (highly dense structures) and are not done full custom.

Table 7. Early organic IC implementations

Processor	Dev count	Date	Tech (nm)	Core (mm^2)	Tr dens
IMECPragmatIC 6502	16392	2022	800	24,9	658
PragmatIC Cortex-M	56340	2021	800	59,2	952
UMan. BNN FlexIC	3500	2020	800	5,86	766
UMan. Dedicated ML	3000	2019	800	5,6	559
IMEC RFIDtag	8000	2017	10000	50,55	34
IMEC 8-bit ALU	4528	2016	5000	225,6	16

Nevertheless, we can see from both tables that with a 2.5µm process, we can reach something like 30 tr/mm^2 (but a large surface with good yield is available).

Area, speed and power efficiency of a circuit are determined by standard cell library, circuit structure for its optimization, delay requirements, etc. Efficiency for one metric does not necessarily indicate that for another, and comparing logical designs based on variations in gate count is not a reliable way to determine how well-designed their expected hardware is. Comparisons are often done based on benchmark designs (ISCAS85 for combinational circuits, ISCAS89 for sequential circuits, ITC99 for test). The gate count is only a good representative of the design area in low-speeds, and it is never a proper indicator for power consumption.

Several European foundries (PragmatIC, KIT & ÌnnovationLab, Smartkem, IMEC) are considering offering their flexible organic electronics IC PDK (e.g., under the Europractice framework) as recently presented in webinars.

5.2 Open-PDK proposal for Smartkem 2.5μM PMOS

However, switching to organic semiconductors presents a number of new challenges, including a roughly 1,000-fold decrease in electron mobility compared to silicon, a requirement for unipolar design due to the typical p-type and n-type high-performance organic semiconductors, a larger minimum feature size limited by material degradation and dissolution during photolithographic patterning, and a significant variation in device current and threshold voltage.

Our design flow is based on building a PDK and tailoring it for OpenLane, the automated flow from RTL to GDSII. OpenLane is built on a variety of OpenROAD, Yosys, Magic, Netgen, CVC, SPEF-Extractor, CU-GR, Klayout, and other custom scripts for design exploration and optimization. The flow carries out all ASIC back-end implementation processes, starting with RTL HDL Verilog code and ending with GDSII descriptions for the layout masks. As for OpenRoad, PDF information follow OpenDB [352] and allows LEF/DEF conversion with RosettaStone for (1) Creating OpenDB databases from bookshelf and PDK information; (2) Missing information (e.g., cell types) are populated based on target PDK; (3) Existing macro blocks are properly scaled based on placement site definitions; etc.

OpenLane can work with any PDK that fulfils its requirements. OpenLane flow is composed of 39 stages. In the case of SmartKem 2.5μm PDK, only 2 metal layers are used for routing. Consequently, OpenLane transistor density decreases, and runtime increases significantly compared to Skywater PDK with 5 routing metals layers.

To build and add a new PDK platform in OpenLane, key technology and library components must be provided based on the technology node information. To get the proper design and physical layout for a PDK for SmartKem 2.5μm PMOS technology, several files and information must be submitted, that derive from the standard silicon CMOS PDK procedures[353].

The first step is to create a Design Exchange Format (.def) file that will be used at any stage of the layout generation process. Then, a Liberty (.lib) file must be generated for the standard cell library that contains input and output characteristics for every cell including area, timing and power parameters. The Liberty Timing Model (.lib) must be created next (NLDM). Generating the Liberty Wire Load Models (.lib) to account for parasitic estimations based on each net fanout can

also crucial (but not as much as for submicron processes). The HDL synthesis should ideally permit back-annotation of parasitic information. Finally, the Library Exchange Format (LEF) contains technological data on the design requirements for metal layers, vias, and spacing. The Macro LEF file of the standard cell PDK contains input/output pin designations along with MACRO specifications for every cell. The last step is A mapping from LEF/DEF to GDS layers and datatypes, which Klayout has been selected in this PDK.

Floor planning is supported by OpenLANE at both the entire chip top level and for soft macros. OpenROAD's integrated floorplanner and I/O placer is used by OpenLANE for soft macros [6]. Using the mapped netlists, the floorplanner creates a Design Exchange Format (DEF) file that specifies the macro die and core sizes. Additionally, it specifies the rows and tracks that will be utilized for standard-cell routing and placement. The generation of the power distribution network is done as part of the floorplan process. Around the macro core, OpenLANE builds power rings and straps that run horizontally and vertically. Decoupling capacitors and tap cells (if necessary) are positioned in the macro core area's open spaces at the conclusion of the floorplan stage.

For proper function of the typical cell-based physical design flow, we must also supply technology-dependent data, such as design rules, layer mapping, and parasitic models. The PDK must contain each of these files. The four separate mask layers of the described OTFT technology are listed in **Table 8** along with the fundamental design principles for each layer. The design guidelines were produced by Smartkem group and are based on the alignment limitations and fabrication experiences of our standard OTFT fabrication cycle.

Table 8. layer map

Layer name	Description	Mask depth	Min width	Min spacing
BG	Back gate metal (Ti)	100nm	3.5um	2.5um
SD	Metal layer for SD (Au)	50nm	3.5um	2.5um
TG	Top gate metal (Au)	50nm	3.5um	2.5um
PAS1	Via layer (SU8)	1um	3.5um	2.5um
Gate	Interconnection metal (Au)	50nm	3.5um	2.5um

5.3 Cell library proposal

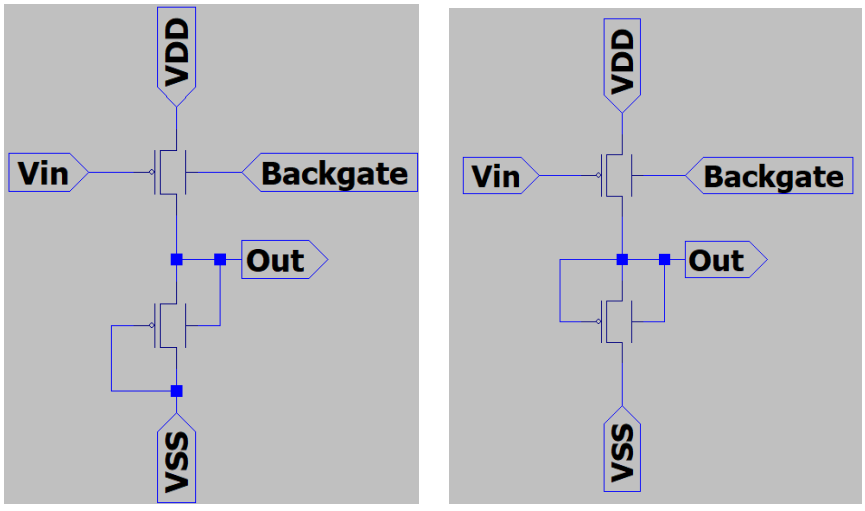
Nowadays, deployed OTFT circuits are still frequently device-based, and designers must hand-draw large final circuit designs, which is a non-scalable method of creating complex systems. The community must adopt a standardized design methodology and implement strict verification to facilitate the design of organic circuits and guarantee good yield for complicated circuit systems. We describe the creation of an organic standard cell library based on experimentally constructed and measured OTFTs in this section.

Current standard cell layout designs adhere to a particular architecture, which calls for a predetermined standard cell height in terms of horizontal metal routing rails. This is compatible with the back-end design flow's positioning of standard cells and power/ground rails in horizontal rows and are following 13 tracks structure.

There are three types of ratioed logic, each determined by the polarity of the threshold voltage: (1) Biased-load, (2) diode-load and (3) Zero-V_{gs}, which, depending on the device properties and circuit performance, each has advantages and disadvantages. Even though they have simpler architectures, biased-load and diode-load inverters perform poorly. The additional Zero-V_{gs} included in the pseudo inverter, on the other hand, allows the bias voltage of the load transistor to vary depending on the input voltage and offers a rail-to-rail output voltage swing. With the Zero-V_{gs}, the pseudo inverter's performance improves significantly. The pseudo-type inverter was chosen as the design style for the entire library despite requiring twice as many transistors since it offers more controlled and desirable performance.

When compared to a diode-load inverter which is shown in **Figure 26** (a), the Zero-V_{GS} inverter, displayed in **Figure 26** (b) produces gains and noise margins that are comparatively high. The larger gain of the first one reasons why it is currently quite frequent in an OTFT-based circuit design, despite there being some speed and robustness against big threshold voltage variation limitations. Additionally, pentacene is the industry standard for organic electronic circuitry's semiconducting materials, and pentacene OTFTs frequently exhibit depletion-mode p-type behavior with a positive threshold voltage (V_T>0). Therefore, Zero-V_{GS} is more frequently utilized in modern organic circuits[353].

The suggested standard cell library has nine fundamental logic cells that can be utilized to implement all necessary logic functions. We exclusively employ organic p-type TFTs in this work since they perform and operate more reliably than n-type TFTs.



(a) (b)

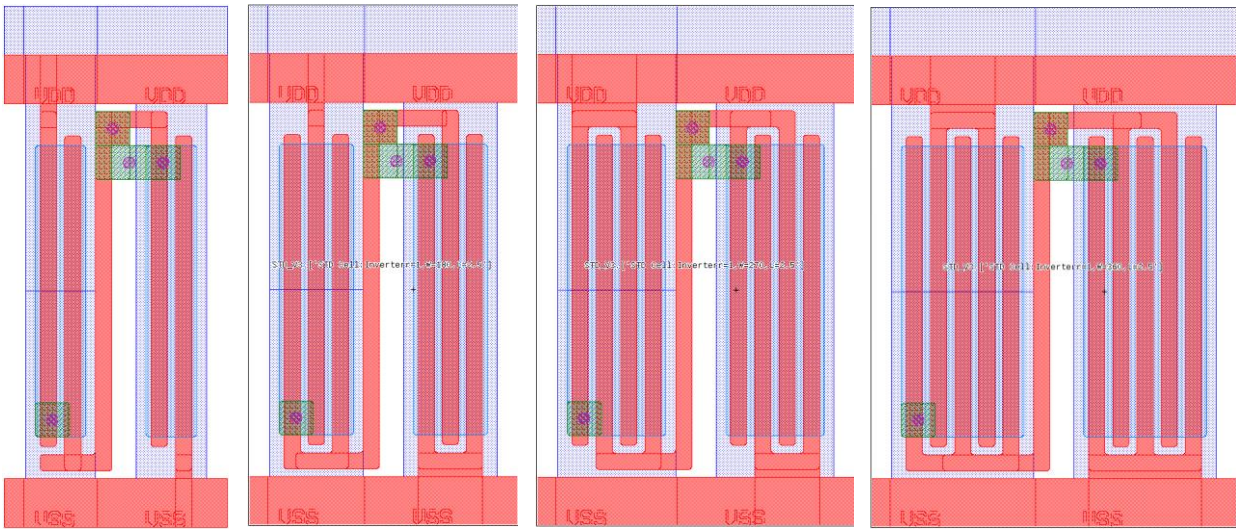
Figure 26. different type of inverter topologies (a) Diode load (b) Zero V_{GS}

The cell library includes a variety of combinational gates (from NOR2 to AOI23) and sequential gates (DFF, DFFS, DFFR) that operate at 3.3V and 5V supply voltages, as well as some macrocells built with them. PVT characterization is currently underway to complete the entire PDK and all cell datasheets. **Table 9**, provides an overview of the cell libraries used in our study, along with the corresponding number of transistors and their respective areas (one finger transistors).

Table 9. Cell Library Information

Cell Library	Number of Transistors	Cell Width	Area (μm^2)
Inverter	2	68.5	11028
NOR2	3	95	15295
NOR3	4	121.5	19561
NOR4	5	148	23828
NAND2	3	90	14490
NAND3	4	111.5	17951
XOR	14	416.5	67056
D-Latch	10	285.5	45965
DFF	22	624	100464
DFFS	23	645.5	103925
DFFR	23	645.5	103925
AOI21	4	116.5	18756
AOI211	5	143	23023
AOI31	5	138	22218
MUX2	11	329.5	53049
MUX4	25	723	116403

We created several widths for these libraries by adding fingers to these basic models, and as a result, we provided different models for each cell, including linear transistors as basic models and multi-finger transistors to increase transistor width. OpenLane will decide which models to use in the core (based on user-defined configurations). **Figure 27** displays inverter four variants made with various fingers. The linear inverter is shown in **Figure 27** (a). **Figure 27** (b) has two source fingers, while the **Figure 27** (c) has two sources and drain fingers. Three source and two drain fingers have been produced on the **Figure 27** (d).



(a) (b) (c) (d)

Figure 27. 4 different widths of inverter with ratio1

To measure the cell libraries accurately, we implemented them within a custom-designed QFN64 structure that we developed. This structure allows for easy access to the cell inputs, overcoming

the limitations of semiconductor tools like the B1500, which have a restricted number of inputs and outputs. By using our QFN64 structure, we can measure the performance of the cells.

The pad structure in the QFN64 design measures 9mm x 9mm, offering a compact footprint for efficient utilization of board space. The pin numbering convention follows a specific direction, where Pin 1 serves as a reference point for orientation. When viewing the QFN64 package from the top ("TOP" view), the pin numbering starts from the specified direction, ensuring consistent identification. Similarly, when observing the package from the back ("BACK" view), the pin numbering is visible, maintaining orientation consistency. This clocking mark is shown in **Figure 28**.

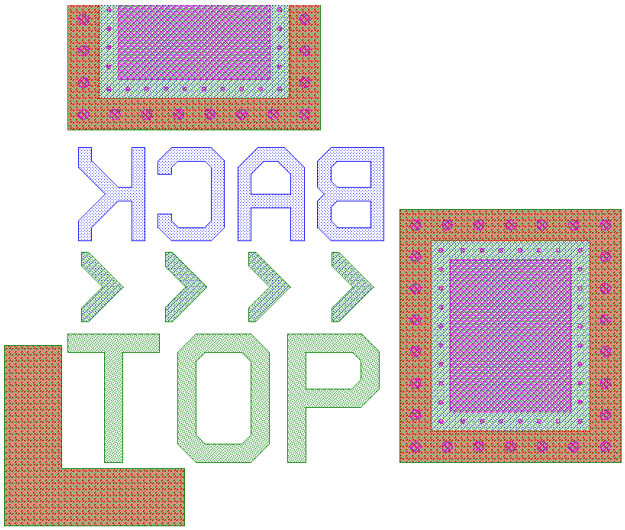


Figure 28. *The clocking mark of the QFN 64 pad design*

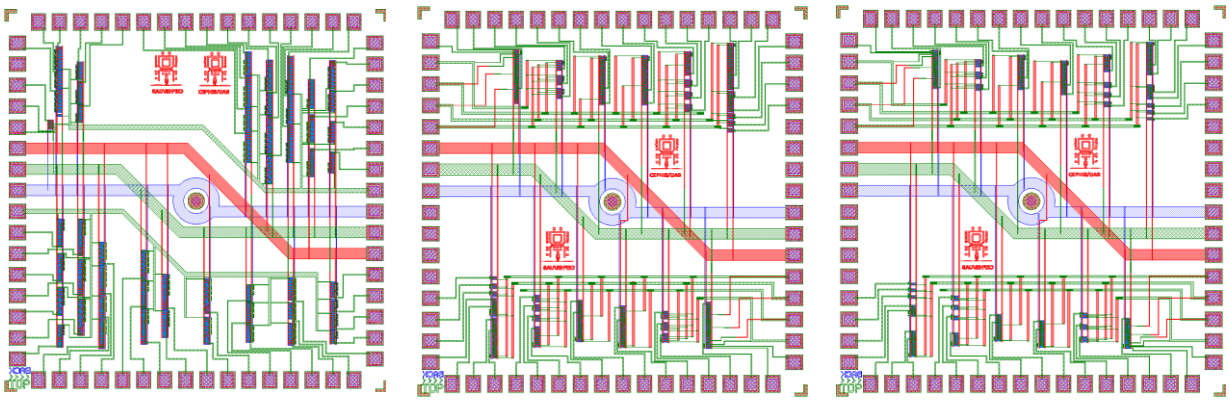
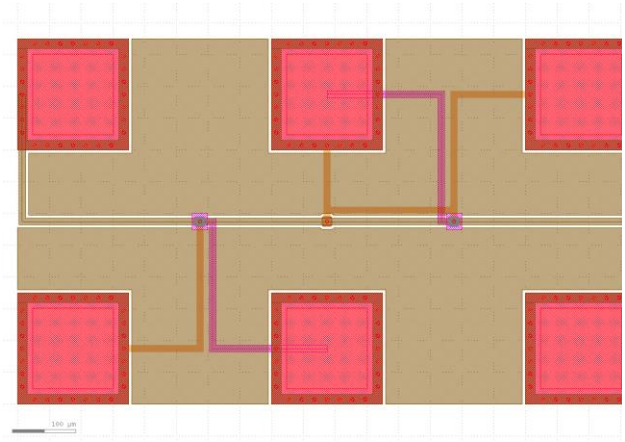


Figure 29. Different implemented positions of cell libraries: (a) Generating ring oscillators, (b) Implementing cell libraries with one and two fingers (each half), (c) Implementing cell libraries with three and four fingers (each half)

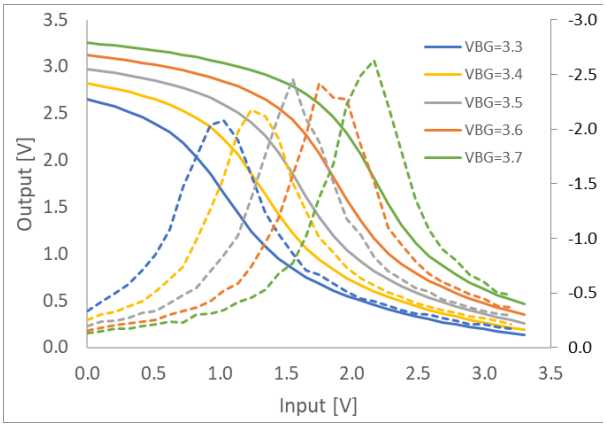
Figure 29 showcases the different implemented positions of cell libraries. In subfigure (a), ring oscillators are generated using the cell libraries. Subfigure (b) demonstrates the implementation of

cell libraries with one and two fingers (each half), while subfigure (c) illustrates the implementation of cell libraries with three and four fingers (each half). These variations in finger count offer flexibility in designing and optimizing the performance of integrated circuits.

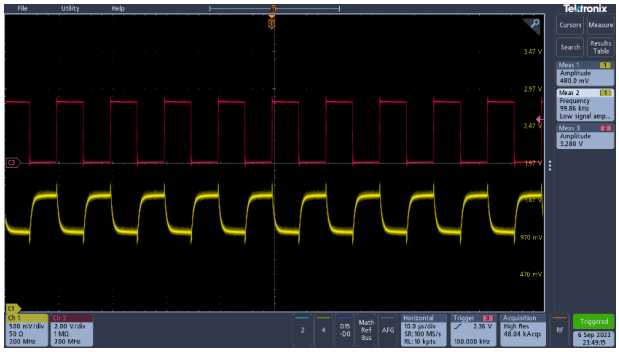
In order to comprehensively understand the static and dynamic characteristics of the cells, we conducted extensive characterizations on the inverters linked with technology and device optimization in order to achieve standardized voltage ranges (e.g. 0-3.3V supply voltage). **Figure 30** provides an insightful view of both the layout of the inverters and the corresponding characterization results at different development stages[354].



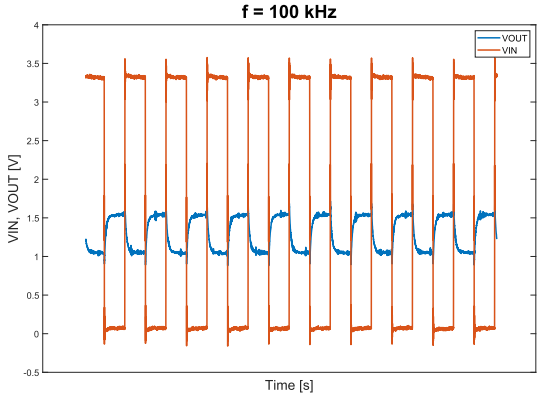
(a)



(b)



(c)

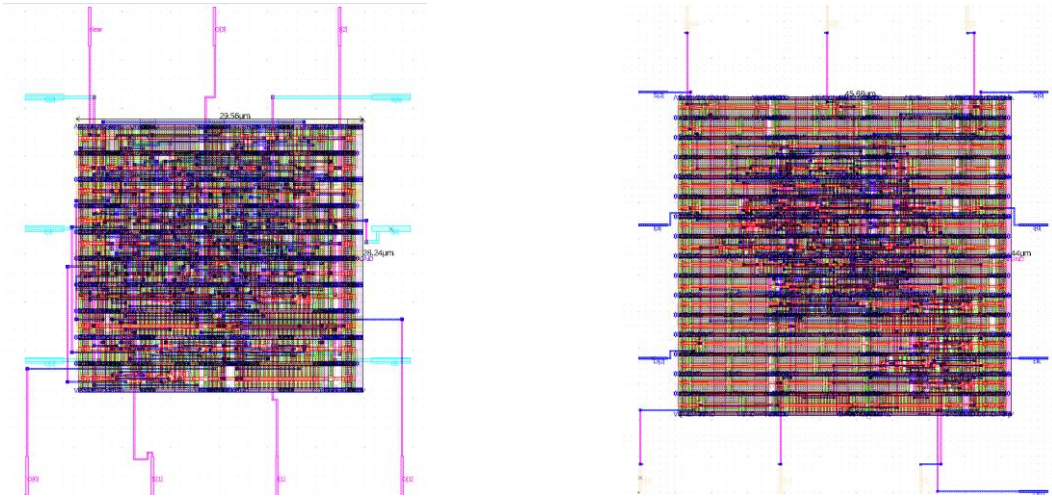


(d)

Figure 30. Extracted from [354]: (a) Test structure for an inverter (b) static characterization (V_{DD} = 3.3V, V_{IN} = 0 – 3.3 V, V_{BG} = 4.5 – 5.5 V) and (c) & (d) dynamic characterization with (V_{DD} = 10 V, V_{IN} = 3.3 V_{PP}, V_{BG} = 3.5 V, V_{OUT} = 500 mV_{PP}, f=100MHz)

We have also been personalizing the Open Lane tool to be used with our cell library. The main issue is to validate that the routing algorithms that work with 5 metal layers for wiring can be used for the Smartkem process that has only 2 metal layers available for wiring. We succeeded in this process for small and medium size benchmark circuits of similar complexity of those that we are targeting).

Figure 31 shows the results obtained with Open Lane for the **Universal Shift Register** circuit with 5 and 2 metal layers. The synthesis time spent by the tool are 1135 and 4013 seconds with the area of *472,88x471,04 um^2 1003,26x1001,44 um^2* respectively, what means that our goal of disposing of a tool to implement digital designs is achievable.



(a) (b)

Figure 31. (a) layout of Universal Shift Register in 5 metal layers and (b) the same layout in only 2 metal layers

Contained within Appendix C is the code specifically tailored for the creation of cell libraries using the Klayout software.

Chapter 6. Conclusion

The internet of things or ciber-physical systems paradigms structure the human knowledge in three elementary levels: the devices that sense the real-world magnitudes, the edge that is closer to the user and integrates data surrounding and reacts for critical issues, and the cloud that accounts for long term storage, analysis and predictions in a local/individual or global/population levels. Sensors are the most common and populated elements of this view and include many different types: mechanical, optical, chemical, biological, etc. Among them chemical and biochemical sensors are key for measuring relevant magnitudes for our quality of life, from environmental data (air, water, etc.) to our personal biometric constants or to the parameters controlling mass production industrial plants to name some examples. ISFETs are popular devices to measure many magnitudes and convert chemical parameters into electronic signals. Therefore, there are many implementation options to implement such sensors and add them into the information chain.

This thesis presents and demonstrates the validity of a proposal for the design and fabrication of eco-friendly organic chips integrating dual-gate OTFT-based EG-ISFETs with multiplexors to allow an easier system integration of sensor devices into the IoT chain.

The extended gate allows separating (1) the functionalization of the EG electrodes to measure different chemical and biochemical components from (2) the transduction effect implemented by ISFETs. Furthermore, it is possible to reuse the ISFET chip for many measurements since the EG is the only part that need to be changed for different measurements in time or material. The option to switch between several ISFETs integrated on the same chip is provided by analog multiplexors implemented with dual-gate OTFTs. That solution allows different functionalities, from (1) flexible gain adjustment or (2) the substitution of faulty sensors without changing the measurement system. The sensor system's overall functionality and durability are greatly improved as a result.

We have examined the performance of four alternative designs based on interdigitated and Corbino structures in terms of output voltage, current, area, and transconductance under various input conditions through comprehensive experimentation and evaluation. Our findings suggest that the best design option depends on the requirements of a particular application as well as the trade-offs between various sensor properties. However, it is clear from the acquired data that among the evaluated designs, the interdigitated transistors with a W/L ratio of 3920/4 demonstrate the most advantageous performance. The design in question has the maximum transconductance value, demonstrating how well it converts input voltage signals to output current. The interdigitated transistors' increased transconductance denotes their improved sensitivity and responsiveness, which makes them ideal for applications requiring accurate signal amplification and detection. This emphasizes how crucial it is to take the desired use case into account when choosing the best sensor design.

We have also noted areas that need further study and development. These include enhancing the devices' performance by optimizing their width-to-length (W/L) ratio, assuring long-term stability, and looking into integration possibilities with other parts or systems. By addressing these issues,

the field of EG-ISFETs and MUX OTFTs will advance, creating new opportunities for their use in a variety of fields.

This study has made significant contributions to the field of sensor technology and integrated circuit design by presenting a novel approach to enhance the performance and cost-effectiveness of ISFET sensors. By integrating extended gate ISFETs with MUX OTFTs, we have demonstrated improved sensor functionality and reduced manufacturing costs compared to conventional ISFET arrays. This innovative design enables the reuse of the same chip for multiple measurements, minimizing human interference and potential damage caused by electrostatic discharge.

One of the key contributions of this research is the development of different designs based on interdigitated and Corbino structures for EG-ISFETs connected to MUX OTFTs. Through rigorous experimentation and analysis, we have evaluated the performance of these designs. Moreover, this research has contributed to the field by uncovering the advantages and limitations of the proposed designs. We have demonstrated that the interdigitated structure excels in stability and performance under certain conditions, while the Corbino structure exhibits enhanced robustness against variations in back gate voltage and threshold voltage.

6.1 Limitations and future research directions

Despite the significant contributions and promising results obtained in this study, there are certain limitations that should be acknowledged. Firstly, the characterization and evaluation of the interdigitated transistors were primarily conducted under specific operating conditions and input ranges. It is important to further explore the performance of these transistors under real conditions and use microfluidic materials to assess their reliability in practical applications.

Secondly, while the chosen W/L ratio of 3920/4 for the interdigitated transistors demonstrated favorable performance, there may exist an optimal W/L ratio that could further enhance their functionality. Future research could focus on systematically varying the W/L ratio and investigating its impact on key performance parameters such as transconductance, output current, and stability. This would provide valuable insights into the trade-offs between device dimensions and performance, enabling the design of interdigitated transistors that are tailored for specific applications and requirements.

In addition to the mentioned limitations and future research directions, another crucial aspect that deserves attention is the development of accurate and reliable SPICE models for dual-gate OTFTs. SPICE models play a vital role in circuit simulation and allow for the prediction of the behavior and performance of complex electronic systems. Therefore, the generation of comprehensive SPICE models specifically tailored to dual-gate OTFTs would greatly facilitate their integration into larger circuit designs and enable efficient optimization and analysis.

Creating accurate SPICE models for dual-gate OTFTs poses certain challenges due to their unique operating principles and complex electrostatic interactions. Future research should focus on developing robust modeling techniques that capture the intricate interplay between the dual gates, channel material properties, and device geometry. Incorporating physically meaningful parameters and accurately characterizing key phenomena such as carrier mobility, threshold voltage, and

capacitance is crucial for achieving reliable and predictive SPICE models[355]–[357]. By developing comprehensive and validated SPICE models, researchers and circuit designers can simulate and optimize the behavior of dual-gate OTFTs within complex circuits, enabling the exploration of various design parameters, performance trade-offs, and system-level interactions. This advancement would greatly contribute to the widespread adoption and integration of dual-gate OTFTs in diverse applications, ranging from flexible displays and sensors to integrated circuits for wearable electronics and Internet of Things (IoT) devices.

Chapter 7. References

[1] S. M. Sze and K. K. Ng, "Physics of Semiconductor Devices," *Physics of Semiconductor Devices*, Oct. 2006, doi: 10.1002/0470068329.

[2] W. Shockley, "Cyclotron Resonances, Magnetoresistance, and Brillouin Zones in Semiconductors," *Physical Review*, vol. 90, no. 3, p. 491, May 1953, doi: 10.1103/PhysRev.90.491.

[3] Bose and B. K., "Power electronics and ac drives," *ph*, 1986.

[4] A. Yariv, *Optical Electronics*. Philadelphia: Saunders College Publishing, 1991.

[5] Green and M. A., "Solar cells: Operating principles, technology, and system applications," *ph*, 1982.

[6] D. A. Neamen, "Semiconductor physics and devices : basic principles," 2012.

[7] Schroder and D. K., "Semiconductor Material and Device Characterization, 3rd Edition," *smdc*, p. 840, 2005.

[8] H. Wong and H. Iwai, "The road to miniaturization," *Physics World*, vol. 18, no. 9, p. 40, Sep. 2005, doi: 10.1088/2058-7058/18/9/31.

[9] R. W. Keyes, "MINIATURIZATION OF ELECTRONICS AND ITS LIMITS.," *IBM J Res Dev*, vol. 32, no. 1, pp. 24–28, 1988, doi: 10.1147/RD.321.0024.

[10] F. Xia, L. T. Yang, L. Wang, and A. Vinel, "Internet of Things," *International Journal of Communication Systems*, vol. 25, no. 9, pp. 1101–1102, Sep. 2012, doi: 10.1002/DAC.2417.

[11] B. Raton, L. New, Y. Washington, and M. J. Madou, "Fundamentals of Microfabrication : The Science of Miniaturization, Second Edition," *Fundamentals of Microfabrication*, Oct. 2018, doi: 10.1201/9781482274004.

[12] W. Shockley, "A unipolar 'field-effect' transistor*," *Proceedings of the IRE*, vol. 40, no. 11, pp. 1365–1376, 1952, doi: 10.1109/JRPROC.1952.273964.

[13] C. Hu, "Future CMOS Scaling and Reliability," *Proceedings of the IEEE*, vol. 81, no. 5, pp. 682–689, 1993, doi: 10.1109/5.220900.

[14] D. L. Critchlow, "MOSFET Scaling-The Driver of VLSI Technology," *Proceedings of the IEEE*, vol. 87, no. 4, pp. 659–667, 1999, doi: 10.1109/JPROC.1999.752521.

[15] R. J. Baker and Institute of Electrical and Electronics Engineers., "CMOS circuit design, layout, and simulation," p. 1234.

[16] B. Razavi, "Design of Analog CMOS Integrated Circuits," p. 704, 2005.

[17] S. Sze, "Semicondutor sensors," pp. 550–550, 1994.

[18] C. Hierold, “Microsystems Technology Micro Resonators & Resonant Microsensors,” vol. 8, pp. 1–60, 2015.

[19] J. W. Gardner, V. K. Varadan, and O. O. Awadelkarim, “Microsensors, MEMS, and Smart Devices,” *Microsensors, MEMS, and Smart Devices*, Nov. 2001, doi: 10.1002/9780470846087.

[20] H. du and D. Chen, “Recent development of MEMS sensor technology,” *Sensor Review*, vol. 27, no. 1, pp. 75–88, Jan. 2007, doi: 10.1108/SR.2007.08727AAA.002/FULL/XML.

[21] S. P. Beeby, “MEMS Mechanical Sensors,” *Sensor Review*, vol. 24, no. 3, pp. 319–320, Sep. 2004, doi: 10.1108/SR.2004.24.3.319.2.

[22] J. Janata, “Principles of chemical sensors,” p. 373.

[23] B. R. Eggins, “Chemical Sensors and Biosensors (Google eBook),” p. 298, 2008.

[24] O. Levi, T. T. Lee, M. M. Lee, S. J. Smith, and J. S. Harris, “Integrated semiconductor optical sensors for cellular and neural imaging,” *Applied Optics, Vol. 46, Issue 10, pp. 1881-1889*, vol. 46, no. 10, pp. 1881–1889, Apr. 2007, doi: 10.1364/AO.46.001881.

[25] P. Werle, F. Slemr, K. Maurer, R. Kormann, R. Mücke, and B. Jänker, “Near- and mid-infrared laser-optical sensors for gas analysis,” *Opt Lasers Eng*, vol. 37, no. 2–3, pp. 101–114, Feb. 2002, doi: 10.1016/S0143-8166(01)00092-6.

[26] A. Bakker and J. Huijsing, “High-Accuracy CMOS Smart Temperature Sensors (The Kluwer International Series in Engineering and Computer Science Volume 595),” Nov. 2000.

[27] D. Niarchos, “Magnetic MEMS: key issues and some applications,” *Sens Actuators A Phys*, vol. 109, no. 1–2, pp. 166–173, Dec. 2003, doi: 10.1016/J.SNA.2003.09.010.

[28] S. Tadigadapa and K. Mateti, “Piezoelectric MEMS sensors: state-of-the-art and perspectives,” *Meas Sci Technol*, vol. 20, no. 9, p. 092001, Jul. 2009, doi: 10.1088/0957-0233/20/9/092001.

[29] J. W. Judy, “Microelectromechanical systems (MEMS): fabrication, design and applications,” *Smart Mater Struct*, vol. 10, no. 6, p. 1115, Nov. 2001, doi: 10.1088/0964-1726/10/6/301.

[30] R. Bogue, “Recent developments in MEMS sensors: A review of applications, markets and technologies,” *Sensor Review*, vol. 33, no. 4, pp. 300–304, 2013, doi: 10.1108/SR-05-2013-678/FULL/PDF.

[31] B. A. Prabowo, A. Purwidyantri, and K. C. Liu, “Surface Plasmon Resonance Optical Sensor: A Review on Light Source Technology,” *Biosensors 2018, Vol. 8, Page 80*, vol. 8, no. 3, p. 80, Aug. 2018, doi: 10.3390/BIOS8030080.

[32] G. Wetzstein *et al.*, “Inference in artificial intelligence with deep optics and photonics,” *Nature*, vol. 588, no. 7836, pp. 39–47, Dec. 2020, doi: 10.1038/s41586-020-2973-6.

[33] U. Teğin, M. Yıldırım, İ. Oğuz, C. Moser, and D. Psaltis, “Scalable optical learning operator,” *Nat Comput Sci*, vol. 1, no. 8, pp. 542–549, Aug. 2021, doi: 10.1038/s43588-021-00112-0.

[34] R. De Marco, G. Clarke, and B. Pejcic, “Ion-Selective Electrode Potentiometry in Environmental Analysis,” *Electroanalysis*, vol. 19, no. 19–20, pp. 1987–2001, Oct. 2007, doi: 10.1002/ELAN.200703916.

[35] P. Bergveld, “Thirty years of ISFETOLOGY: What happened in the past 30 years and what may happen in the next 30 years,” *Sens Actuators B Chem*, vol. 88, no. 1, pp. 1–20, Jan. 2003, doi: 10.1016/S0925-4005(02)00301-5.

[36] L. Te Yin, J. C. Chou, W. Y. Chung, T. P. Sun, and S. K. Hsiung, “Separate structure extended gate H+-ion sensitive field effect transistor on a glass substrate,” *Sens Actuators B Chem*, vol. 71, no. 1–2, pp. 106–111, Nov. 2000, doi: 10.1016/S0925-4005(00)00613-4.

[37] B. Zhao, T. Sai, A. Rahman, and K. Levon, “Floating-gate ion sensitive field-effect transistor for chemical and biological sensing,” *Materials Research Society Symposium Proceedings*, vol. 828, no. 1, pp. 349–354, Jan. 2005, doi: 10.1557/PROC-828-A7.8/METRICS.

[38] P. J. Bresnahan *et al.*, “Autonomous in situ calibration of ion-sensitive field effect transistor pH sensors,” *Limnol Oceanogr Methods*, vol. 19, no. 2, pp. 132–144, Feb. 2021, doi: 10.1002/LOM3.10410.

[39] X. Yuan *et al.*, “Development of an Electrochemical Sensor for Chloride ion Detection Using Ion-Sensitive Field-Effect Transistor Array,” *Int. J. Electrochem. Sci*, vol. 16, p. 150911, 2021, doi: 10.20964/2021.01.60.

[40] Z. Yue, W. Niu, W. Zhang, G. Liu, and W. J. Parak, “Detection of CO2 in solution with a Pt–NiO solid-state sensor,” *J Colloid Interface Sci*, vol. 348, no. 1, pp. 227–231, Aug. 2010, doi: 10.1016/J.JCIS.2010.04.020.

[41] X. Ma, R. Peng, W. Mao, Y. Lin, and H. Yu, “Recent advances in ion-sensitive field-effect transistors for biosensing applications,” *Electrochemical Science Advances*, p. e2100163, Feb. 2022, doi: 10.1002/elsa.202100163.

[42] V. Pachauri and S. Ingebrandt, “Biologically sensitive field-effect transistors: From ISFETs to NanoFETs,” *Essays Biochem*, vol. 60, no. 1, pp. 81–90, Jun. 2016, doi: 10.1042/EBC20150009.

[43] J. Artigas *et al.*, “Application of ion sensitive field effect transistor based sensors to soil analysis,” *Comput Electron Agric*, vol. 31, no. 3, pp. 281–293, May 2001, doi: 10.1016/S0168-1699(00)00187-3.

[44] W. Shockley, “A unipolar ‘field-effect’ transistor*,” *Proceedings of the IRE*, vol. 40, no. 11, pp. 1365–1376, 1952, doi: 10.1109/JRPROC.1952.273964.

[45] A. Ali, A. Ali, A. Hussain Zahid, G. Mustafa, and M. Waseem Razzaq, “A non linear model to analyze the DC performance of SiC MESFET,” *Ain Shams Engineering Journal*, vol. 13, no. 1, p. 101506, Jan. 2022, doi: 10.1016/j.asej.2021.05.020.

[46] S. E. Sussman-Fort, S. Narasimhan, and K. Mayaram, “A Complete GaAs MESFET Computer Model for SPICE,” *IEEE Trans Microw Theory Tech*, vol. 32, no. 4, pp. 471–473, 1984, doi: 10.1109/TMTT.1984.1132707.

[47] L. C. Clark and C. Lyons, “ELECTRODE SYSTEMS FOR CONTINUOUS MONITORING IN CARDIOVASCULAR SURGERY,” *Ann N Y Acad Sci*, vol. 102, no. 1, pp. 29–45, Oct. 1962, doi: 10.1111/J.1749-6632.1962.TB13623.X.

[48] P. Bergveld, “Short Communications: Development of an Ion-Sensitive Solid-State Device for Neurophysiological Measurements,” *IEEE Trans Biomed Eng*, vol. BME-17, no. 1, pp. 70–71, 1970, doi: 10.1109/TBME.1970.4502688.

[49] B. H. van der Schoot and P. Bergveld, “ISFET based enzyme sensors,” *Biosensors (Basel)*, vol. 3, no. 3, pp. 161–186, Jan. 1987, doi: 10.1016/0265-928X(87)80025-1.

[50] L. Bousse, L. Bousse, N. F. De Rood, and P. Bergveld, “Operation of Chemically Sensitive Field-Effect Sensors As a Function of the Insulator-Electrolyte Interface,” *IEEE Trans Electron Devices*, vol. 30, no. 10, pp. 1263–1270, 1983, doi: 10.1109/T-ED.1983.21284.

[51] S. Caras and J. Janata, “Field effect transistor sensitive to penicillin,” *Anal Chem*, vol. 52, no. 12, pp. 1935–1937, 2002, doi: 10.1021/AC50062A035.

[52] K. I. Lundström, M. S. Shivaraman, and C. M. Svensson, “A hydrogen-sensitive Pd-gate MOS transistor,” *J Appl Phys*, vol. 46, no. 9, pp. 3876–3881, Sep. 1975, doi: 10.1063/1.322185.

[53] J. ichi Anzai, H. Nakajima, T. Kusmio, T. Matsuo, and T. Osa, “UREA SENSOR BASED ON ION SENSITIVE FIELD EFFECT TRANSISTOR COATED WITH CROSS-LINKED UREASE-ALBUMIN MEMBRANE,” *BUNSEKI KAGAKU*, vol. 33, no. 4, pp. E131–E136, Apr. 1984, doi: 10.2116/BUNSEKIKAGAKU.33.4_E131.

[54] O. A. Boubriak, A. P. Soldatkin, N. F. Starodub, A. K. Sandrovsky, and A. K. El’skaya, “Determination of urea in blood serum by a urease biosensor based on an ion-sensitive field-effect transistor,” *Sens Actuators B Chem*, vol. 27, no. 1–3, pp. 429–431, Jun. 1995, doi: 10.1016/0925-4005(94)01633-S.

[55] X. F. Wu *et al.*, “Air Effect on the Ideality of p-Type Organic Field-Effect Transistors: A Double-Edged Sword,” *Adv Funct Mater*, vol. 29, no. 51, p. 1906653, Dec. 2019, doi: 10.1002/adfm.201906653.

[56] Z. Yang *et al.*, “Improving Bias-Stress Stability of p-Type Organic Field-Effect Transistors by Constructing an Electron Injection Barrier at the Drain Electrode/Semiconductor Interfaces,” *ACS Appl Mater Interfaces*, vol. 12, no. 37, pp. 41886–41895, Sep. 2020, doi: 10.1021/acsami.0c12188.

[57] M. Nikolka *et al.*, “High operational and environmental stability of high-mobility conjugated polymer field-effect transistors through the use of molecular additives,” *Nat Mater*, vol. 16, no. 3, pp. 356–362, Dec. 2017, doi: 10.1038/nmat4785.

[58] H. Phan *et al.*, “Improving Electrical Stability and Ideality in Organic Field-Effect Transistors by the Addition of Fullerenes: Understanding the Working Mechanism,” *Adv Funct Mater*, vol. 27, no. 38, p. 1701358, Oct. 2017, doi: 10.1002/adfm.201701358.

[59] Y. Xu *et al.*, “Planar-Processed Polymer Transistors,” *Advanced Materials*, vol. 28, no. 38, pp. 8531–8537, Oct. 2016, doi: 10.1002/adma.201601589.

[60] C. Duvvury and A. Amerasekera, “ESD: A Pervasive Reliability Concern for IC Technologies,” *Proceedings of the IEEE*, vol. 81, no. 5, pp. 690–702, 1993, doi: 10.1109/5.220901.

[61] M. T. Brandt, “Fundamentals of Electrostatic Discharge Part Five-Device Sensitivity and Testing,” 2010.

[62] Y. Xi, S. Malobabic, V. Vashchenko, and J. Liou, “Correlation between TLP, HMM, and system-level esd pulses for cu metallization,” *IEEE Transactions on Device and Materials Reliability*, vol. 14, no. 1, pp. 446–450, 2014, doi: 10.1109/TDMR.2013.2292039.

[63] U. Zschieschang, H. Klauk, and J. W. Borchert, “High-Resolution Lithography for High-Frequency Organic Thin-Film Transistors,” *Adv Mater Technol*, Apr. 2023, doi: 10.1002/admt.202201888.

[64] C. Reese, M. Roberts, M. M. Ling, and Z. Bao, “Organic thin film transistors,” *Materials Today*, vol. 7, no. 9, pp. 20–27, Sep. 2004, doi: 10.1016/S1369-7021(04)00398-0.

[65] A. Bilgaiyan, S. Il Cho, M. Abiko, K. Watanabe, and M. Mizukami, “Flexible, high mobility short-channel organic thin film transistors and logic circuits based on 4H–21DNTT,” *Sci Rep*, vol. 11, no. 1, p. 11710, Jun. 2021, doi: 10.1038/s41598-021-91239-7.

[66] O. A. Melville, B. H. Lessard, and T. P. Bender, “Phthalocyanine-Based Organic Thin-Film Transistors: A Review of Recent Advances,” *ACS Appl Mater Interfaces*, vol. 7, no. 24, pp. 13105–13118, Jun. 2015, doi: 10.1021/ACSAMI.5B01718/ASSET/IMAGES/LARGE/AM-2015-017188_0004.JPEG.

[67] X. Guo *et al.*, “Current Status and Opportunities of Organic Thin-Film Transistor Technologies,” *IEEE Trans Electron Devices*, vol. 64, no. 5, pp. 1906–1921, May 2017, doi: 10.1109/TED.2017.2677086.

[68] T. Pirson, T. Delhaye, A. Pip, G. Le Brun, J. P. Raskin, and D. Bol, "The Environmental Footprint of IC Production: Meta-Analysis and Historical Trends," in *European Solid-State Device Research Conference*, IEEE, Sep. 2022, pp. 352–355. doi: 10.1109/ESSDERC55479.2022.9947198.

[69] S. Ogier, D. Sharkey, A. Carreras, and S. Tsai, "Opportunities for High-Performance Display Manufacturing Enabled by OTFTs Using an 80*C Maximum Process Temperature," *Dig Tech Pap*, vol. 53, no. 1, pp. 929–932, Jun. 2022, doi: 10.1002/sdtp.15647.

[70] Y. Z. Zheng *et al.*, "Physical Mechanism of the Mechanical Bending of High-Performance Organic TFTs and the Effect of Atmospheric Factors," *ACS Appl Electron Mater*, vol. 4, no. 6, pp. 3000–3009, Jun. 2022, doi: 10.1021/ACSAELM.2C00430/ASSET/IMAGES/LARGE/EL2C00430_0012.JPEG.

[71] W. F. Boron, "Regulation of intracellular pH," *American Journal of Physiology - Advances in Physiology Education*, vol. 28, no. 4, pp. 160–179, 2004, doi: 10.1152/ADVAN.00045.2004/ASSET/IMAGES/LARGE/ZU10040402401018.JPEG.

[72] M. Flinck, S. H. Kramer, and S. F. Pedersen, "Roles of pH in control of cell proliferation," *Acta Physiologica*, vol. 223, no. 3, p. e13068, Jul. 2018, doi: 10.1111/APHA.13068.

[73] I. Pavlov, K. Kaila, D. M. Kullmann, and R. Miles, "Cortical inhibition, pH and cell excitability in epilepsy: what are optimal targets for antiepileptic interventions?," *J Physiol*, vol. 591, no. 4, pp. 765–774, Feb. 2013, doi: 10.1113/JPHYSIOL.2012.237958.

[74] N. J. Ronkainen, H. B. Halsall, and W. R. Heineman, "Electrochemical biosensors," *Chem Soc Rev*, vol. 39, no. 5, pp. 1747–1763, Apr. 2010, doi: 10.1039/b714449k.

[75] K. I. Chen, B. R. Li, and Y. T. Chen, "Silicon nanowire field-effect transistor-based biosensors for biomedical diagnosis and cellular recording investigation," *Nano Today*, vol. 6, no. 2. Elsevier, pp. 131–154, Apr. 01, 2011. doi: 10.1016/j.nantod.2011.02.001.

[76] S. Meyburg *et al.*, "N-Channel field-effect transistors with floating gates for extracellular recordings," *Biosens Bioelectron*, vol. 21, no. 7, pp. 1037–1044, Jan. 2006, doi: 10.1016/j.bios.2005.03.010.

[77] P. Estrela, S. D. Keighley, P. Li, and P. Migliorato, "Application of thin film transistors to label-free electrical biosensors," in *IEEE International Symposium on Industrial Electronics*, 2008, pp. 2034–2039. doi: 10.1109/ISIE.2008.4677045.

[78] J. T. Smith, S. S. Shah, M. Goryll, J. R. Stowell, and D. R. Allee, "Flexible ISFET biosensor using IGZO metal oxide TFTs and an ITO sensing layer," *IEEE Sens J*, vol. 14, no. 4, pp. 937–938, Apr. 2014, doi: 10.1109/JSEN.2013.2295057.

[79] A. Tixier-Mita *et al.*, "Review on thin-film transistor technology, its applications, and possible new applications to biological cells," *Japanese Journal of Applied Physics*, vol. 55,

no. 4. Japan Society of Applied Physics, p. 04EA08, Apr. 01, 2016. doi: 10.7567/JJAP.55.04EA08.

[80] A. Kumar, A. K. Goyal, and N. Gupta, "Review—Thin-Film Transistors (TFTs) for Highly Sensitive Biosensing Applications: A Review," *ECS Journal of Solid State Science and Technology*, vol. 9, no. 11, p. 115022, Sep. 2020, doi: 10.1149/2162-8777/abb2b3.

[81] P. K. Weimer, "The TFT—A New Thin-Film Transistor," *Proceedings of the IRE*, vol. 50, no. 6, pp. 1462–1469, 1962, doi: 10.1109/JRPROC.1962.288190.

[82] B. J. Lechner, F. J. Marlowe, E. O. Nester, and J. Tults, "Liquid Crystal Matrix Displays," *Proceedings of the IEEE*, vol. 59, no. 11, pp. 1566–1579, 1971, doi: 10.1109/PROC.1971.8489.

[83] P. G. Le Comber, W. E. Spear, and A. Ghaith, "Amorphous-silicon field-effect device and possible application," *Electron Lett*, vol. 15, no. 6, pp. 179–181, Mar. 1979, doi: 10.1049/el:19790126.

[84] T. Tiedje, B. Abeles, D. L. Morel, T. D. Moustakas, and C. R. Wronski, "Electron drift mobility in hydrogenated a-Si," *Appl Phys Lett*, vol. 36, no. 8, pp. 695–697, Jul. 1980, doi: 10.1063/1.91596.

[85] S. W. Depp, A. Juliana, and B. G. Huth, "Polysilicon Fet Devices for Large Area Input/Output Applications.," in *Technical Digest - International Electron Devices Meeting*, IEEE, 1980, pp. 703–706. doi: 10.1109/iedm.1980.189933.

[86] T. Serikawa, S. Shirai, A. Okamoto, and S. Suyama, "Low-temperature fabrication of high-mobility poly-Si TFT's for large-area LCD's," *IEEE Trans Electron Devices*, vol. 36, no. 9, pp. 1929–1933, 1989, doi: 10.1109/16.34272.

[87] Y. Miyata, M. Furuta, T. Yoshioka, and T. Kawamura, "Low-temperature polycrystalline silicon thin-film transistors for large-area liquid crystal display," *Jpn J Appl Phys*, vol. 31, no. 12 S, pp. 4559–4562, Dec. 1992, doi: 10.1143/JJAP.31.4559.

[88] J. Biggs *et al.*, "A natively flexible 32-bit Arm microprocessor," *Nature*, vol. 595, no. 7868, pp. 532–536, Jul. 2021, doi: 10.1038/s41586-021-03625-w.

[89] F. Ebisawa, T. Kurokawa, and S. Nara, "Electrical properties of polyacetylene/polysiloxane interface," *J Appl Phys*, vol. 54, no. 6, pp. 3255–3259, Aug. 1983, doi: 10.1063/1.332488.

[90] C. J. Drury, C. M. J. Mutsaers, C. M. Hart, M. Matters, and D. M. De Leeuw, "Low-cost all-polymer integrated circuits," *Appl Phys Lett*, vol. 73, no. 1, pp. 108–110, Jul. 1998, doi: 10.1063/1.121783.

[91] E. Jenkins, "High-performance apparel for outdoor pursuits," in *High-Performance Apparel: Materials, Development, and Applications*, Elsevier, 2017, pp. 421–449. doi: 10.1016/B978-0-08-100904-8.00021-3.

[92] H. Koezuka, A. Tsumura, and T. Ando, "Field-effect transistor with polythiophene thin film," *Synth Met*, vol. 18, no. 1–3, pp. 699–704, Feb. 1987, doi: 10.1016/0379-6779(87)90964-7.

[93] C. B. Park, K. M. Kim, J. E. Lee, H. Na, S. S. Yoo, and M. S. Yang, "Flexible electrophoretic display driven by solution-processed organic TFT with highly stable bending feature," *Org Electron*, vol. 15, no. 12, pp. 3538–3545, Dec. 2014, doi: 10.1016/j.orgel.2014.09.039.

[94] C. M. Chen *et al.*, "Towards wearable and flexible sensors and circuits integration for stress monitoring," *IEEE J Biomed Health Inform*, vol. 24, no. 8, pp. 2208–2215, Aug. 2020, doi: 10.1109/JBHI.2019.2957444.

[95] K. Myny *et al.*, "Organic RFID transponder chip with data rate compatible with electronic product coding," *Org Electron*, vol. 11, no. 7, pp. 1176–1179, Jul. 2010, doi: 10.1016/j.orgel.2010.04.013.

[96] V. Fiore *et al.*, "An integrated 13.56-MHz RFID tag in a printed organic complementary TFT technology on flexible substrate," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 6, pp. 1668–1677, Jun. 2015, doi: 10.1109/TCSI.2015.2415175.

[97] R. Shiwaku *et al.*, "A printed organic amplification system for wearable potentiometric electrochemical sensors," *Sci Rep*, vol. 8, no. 1, pp. 1–8, Mar. 2018, doi: 10.1038/s41598-018-22265-1.

[98] H. Minemawari *et al.*, "Inkjet printing of single-crystal films," *Nature*, vol. 475, no. 7356, pp. 364–367, Jul. 2011, doi: 10.1038/nature10313.

[99] D. Venkateshvaran *et al.*, "Approaching disorder-free transport in high-mobility conjugated polymers," *Nature*, vol. 515, no. 7527, pp. 384–388, Nov. 2014, doi: 10.1038/nature13854.

[100] H. Sirringhaus, "25th anniversary article: Organic field-effect transistors: The path beyond amorphous silicon," *Advanced Materials*, vol. 26, no. 9, pp. 1319–1335, Mar. 2014, doi: 10.1002/adma.201304346.

[101] Y. Shao, Z. Xiao, C. Bi, Y. Yuan, and J. Huang, "Origin and elimination of photocurrent hysteresis by fullerene passivation in CH3NH3PbI3 planar heterojunction solar cells," *Nat Commun*, vol. 5, no. 1, pp. 1–7, Dec. 2014, doi: 10.1038/ncomms6784.

[102] H. Fan *et al.*, "High-mobility organic single-crystalline transistors with anisotropic transport based on high symmetrical 'h'-shaped heteroarene derivatives," *J Mater Chem C Mater*, vol. 8, no. 33, pp. 11477–11484, Aug. 2020, doi: 10.1039/d0tc01390k.

[103] A. F. Paterson *et al.*, "Recent Progress in High-Mobility Organic Transistors: A Reality Check," *Advanced Materials*, vol. 30, no. 36. John Wiley & Sons, Ltd, p. 1801079, Sep. 01, 2018. doi: 10.1002/adma.201801079.

[104] N. S. Kim *et al.*, “Leakage Current: Moore’s Law Meets Static Power,” *Computer*, vol. 36, no. 12. IEEE Computer Society, pp. 68–75, 2003. doi: 10.1109/MC.2003.1250885.

[105] S. Steudel, K. Myny, S. De Vusser, J. Genoe, and P. Heremans, “Patterning of organic thin film transistors by oxygen plasma etch,” *Appl Phys Lett*, vol. 89, no. 18, p. 183503, Oct. 2006, doi: 10.1063/1.2374679.

[106] W. Tang, J. Zhao, L. Feng, P. Yu, W. Zhang, and X. Guo, “Top-gate dry-etching patterned polymer thin-film transistors with a protective layer on top of the channel,” *IEEE Electron Device Letters*, vol. 36, no. 1, pp. 59–61, Jan. 2015, doi: 10.1109/LED.2014.2367012.

[107] J. W. Borchert *et al.*, “Flexible low-voltage high-frequency organic thin-film transistors,” *Sci Adv*, vol. 6, no. 21, May 2020, doi: 10.1126/sciadv.aaz5156.

[108] T. K. Chang, C. W. Lin, and S. Chang, “LTPO TFT technology for amoleds,” in *Digest of Technical Papers - SID International Symposium*, John Wiley & Sons, Ltd, Jun. 2019, pp. 545–548. doi: 10.1002/sdtp.12978.

[109] T. Sameshima, S. Usui, and M. Sekiya, “XeCl EXCIMER LASER ANNEALING USED IN THE FABRICATION OF POLY-Si TFT’S’.,” *Electron device letters*, vol. EDL-7, no. 5, pp. 276–278, 1986, doi: 10.1109/edl.1986.26372.

[110] H. Klauk, M. Halik, U. Zschieschang, G. Schmid, W. Radlik, and W. Weber, “High-mobility polymer gate dielectric pentacene thin film transistors,” *J Appl Phys*, vol. 92, no. 9, pp. 5259–5263, Oct. 2002, doi: 10.1063/1.1511826.

[111] S. R. Forrest, “The path to ubiquitous and low-cost organic electronic appliances on plastic,” *Nature*, vol. 428, no. 6986. Nature Publishing Group, pp. 911–918, Apr. 29, 2004. doi: 10.1038/nature02498.

[112] Y. Zhang, D. Li, and C. Jiang, “Influence of grain size at first monolayer on bias-stress effect in pentacene-based thin film transistors,” *Appl Phys Lett*, vol. 103, no. 21, p. 213304, Nov. 2013, doi: 10.1063/1.4833251.

[113] S. P. Huang *et al.*, “Effect of ELA Energy Density on Self-Heating Stress in Low-Temperature Polycrystalline Silicon Thin-Film Transistors,” *IEEE Trans Electron Devices*, vol. 67, no. 8, pp. 3163–3166, Aug. 2020, doi: 10.1109/TED.2020.3005366.

[114] Y. Z. Zheng *et al.*, “Enhancement of Mechanical Bending Stress Endurance Using an Organic Trench Structure in Foldable Polycrystalline Silicon TFTs,” *IEEE Electron Device Letters*, vol. 41, no. 5, pp. 721–724, May 2020, doi: 10.1109/LED.2020.2980123.

[115] J. Lee *et al.*, “42.2: World’s Largest (15-inch) XGA AMLCD Panel Using IGZO Oxide TFT,” *SID Symposium Digest of Technical Papers*, vol. 39, no. 1, p. 625, May 2008, doi: 10.1889/1.3069740.

[116] M. Kim *et al.*, "Donor–Acceptor-Conjugated Polymer for High-Performance Organic Field-Effect Transistors: A Progress Report," *Advanced Functional Materials*, vol. 30, no. 20. John Wiley & Sons, Ltd, p. 1904545, May 01, 2020. doi: 10.1002/adfm.201904545.

[117] S. Fratini, M. Nikolka, A. Salleo, G. Schweicher, and H. Sirringhaus, "Charge transport in high-mobility conjugated polymers and molecular semiconductors," *Nature Materials*, vol. 19, no. 5. Nature Publishing Group, pp. 491–502, Apr. 15, 2020. doi: 10.1038/s41563-020-0647-2.

[118] H. Phan, M. Wang, G. C. Bazan, and T. Q. Nguyen, "Electrical Instability Induced by Electron Trapping in Low-Bandgap Donor-Acceptor Polymer Field-Effect Transistors," *Advanced Materials*, vol. 27, no. 43, pp. 7004–7009, Nov. 2015, doi: 10.1002/adma.201501757.

[119] X. Wu *et al.*, "Air Effect on the Ideality of p-Type Organic Field-Effect Transistors: A Double-Edged Sword," *Adv Funct Mater*, vol. 29, no. 51, p. 1906653, Dec. 2019, doi: 10.1002/adfm.201906653.

[120] Z. Yang *et al.*, "Improving Bias-Stress Stability of p-Type Organic Field-Effect Transistors by Constructing an Electron Injection Barrier at the Drain Electrode/Semiconductor Interfaces," *ACS Appl Mater Interfaces*, vol. 12, no. 37, pp. 41886–41895, Sep. 2020, doi: 10.1021/acsami.0c12188.

[121] M. Nikolka *et al.*, "High operational and environmental stability of high-mobility conjugated polymer field-effect transistors through the use of molecular additives," *Nat Mater*, vol. 16, no. 3, pp. 356–362, Dec. 2017, doi: 10.1038/nmat4785.

[122] H. Phan, M. J. Ford, A. T. Lill, M. Wang, G. C. Bazan, and T. Q. Nguyen, "Improving Electrical Stability and Ideality in Organic Field-Effect Transistors by the Addition of Fullerenes: Understanding the Working Mechanism," *Adv Funct Mater*, vol. 27, no. 38, p. 1701358, Oct. 2017, doi: 10.1002/adfm.201701358.

[123] Y. Xu, H. Sun, E. Y. Shin, Y. F. Lin, W. Li, and Y. Y. Noh, "Planar-Processed Polymer Transistors," *Advanced Materials*, vol. 28, no. 38, pp. 8531–8537, Oct. 2016, doi: 10.1002/adma.201601589.

[124] X. Wu *et al.*, "Improving Ideality of P-Type Organic Field-Effect Transistors via Preventing Undesired Minority Carrier Injection," *Adv Funct Mater*, vol. 31, no. 19, p. 2100202, May 2021, doi: 10.1002/adfm.202100202.

[125] C. Wang, H. Dong, L. Jiang, and W. Hu, "Organic semiconductor crystals," *Chemical Society Reviews*, vol. 47, no. 2. The Royal Society of Chemistry, pp. 422–500, Jan. 22, 2018. doi: 10.1039/c7cs00490g.

[126] C. Liu *et al.*, "Effect of doping concentration on microstructure of conjugated polymers and characteristics in n-type polymer field-effect transistors," *Adv Funct Mater*, vol. 25, no. 5, pp. 758–767, Feb. 2015, doi: 10.1002/adfm.201402321.

[127] B. Lüssem, C. M. Keum, D. Kasemann, B. Naab, Z. Bao, and K. Leo, "Doped Organic Transistors," *Chemical Reviews*, vol. 116, no. 22. American Chemical Society, pp. 13714–13751, Nov. 23, 2016. doi: 10.1021/acs.chemrev.6b00329.

[128] L. Sarcina *et al.*, "Enzyme based field effect transistor: State-of-the-art and future perspectives," *Electrochemical Science Advances*, p. e2100216, Feb. 2022, doi: 10.1002/elsa.202100216.

[129] S. Cao *et al.*, "ISFET-based sensors for (bio)chemical applications: A review," *Electrochemical Science Advances*, p. e2100207, Mar. 2022, doi: 10.1002/elsa.202100207.

[130] J. H. Jeon and W. J. Cho, "High-performance extended-gate ion-sensitive field-effect transistors with multi-gate structure for transparent, flexible, and wearable biosensors," *Sci Technol Adv Mater*, vol. 21, no. 1, pp. 371–378, Jan. 2020, doi: 10.1080/14686996.2020.1775477.

[131] K. B. Parizi, X. Xu, A. Pal, X. Hu, and H. S. Philip Wong, "ISFET pH Sensitivity: Counter-Ions Play a Key Role," *Sci Rep*, vol. 7, 2017, doi: 10.1038/srep41305.

[132] M. Kaisti, "Detection principles of biological and chemical FET sensors," *Biosensors and Bioelectronics*, vol. 98. Elsevier, pp. 437–448, Dec. 15, 2017. doi: 10.1016/j.bios.2017.07.010.

[133] L. L. Chi, J. C. Chou, W. Y. Chung, T. P. Sun, and S. K. Hsiung, "Study on extended gate field effect transistor with tin oxide sensing membrane," *Mater Chem Phys*, vol. 63, no. 1, pp. 19–23, Feb. 2000, doi: 10.1016/S0254-0584(99)00184-4.

[134] Y. Hu and P. Georgiou, "A robust ISFET pH-measuring front-end for chemical reaction monitoring," *IEEE Trans Biomed Circuits Syst*, vol. 8, no. 2, pp. 177–185, 2014, doi: 10.1109/TBCAS.2014.2313512.

[135] J. V. Pinto, R. Branquinho, P. Barquinha, E. Alves, R. Martins, and E. Fortunato, "Extended-gate ISFETs based on sputtered amorphous oxides," *IEEE/OSA Journal of Display Technology*, vol. 9, no. 9, pp. 729–734, Sep. 2013, doi: 10.1109/JDT.2012.2227298.

[136] J. M. Rothberg *et al.*, "An integrated semiconductor device enabling non-optical genome sequencing," *Nature*, vol. 475, no. 7356, pp. 348–352, Jul. 2011, doi: 10.1038/nature10242.

[137] J. R. Epstein, I. Biran, and D. R. Walt, "Fluorescence-based nucleic acid detection and microarrays," *Analytica Chimica Acta*, vol. 469, no. 1. Elsevier, pp. 3–36, Sep. 26, 2002. doi: 10.1016/S0003-2670(02)00030-2.

[138] L. Keeble, N. Moser, J. Rodriguez-Manzano, and P. Georgiou, "ISFET-Based Sensing and Electric Field Actuation of DNA for On-Chip Detection: A Review," *IEEE Sens J*, vol. 20, no. 19, pp. 11044–11065, Oct. 2020, doi: 10.1109/JSEN.2020.2998168.

[139] E. C. Hayden, "The $ 1,000 genome," *Nature*, vol. 507, no. 7492. pp. 294–295, 2014. doi: 10.1038/507294a.

[140] D. Ma, J. Rodriguez-Manzano, S. de M. Lopez, M. Kalofonou, P. Georgiou, and C. Toumazou, "Adapting ISFETs for Epigenetics: An Overview," *IEEE Trans Biomed Circuits Syst*, vol. 12, no. 5, pp. 1186–1201, Oct. 2018, doi: 10.1109/TBCAS.2018.2838153.

[141] L. Kuang, J. Zeng, and P. Georgiou, "Live Demonstration: Real-Time and High-Speed Ion Imaging Using CMOS ISFET Arrays," in *BioCAS 2021 - IEEE Biomedical Circuits and Systems Conference, Proceedings*, Institute of Electrical and Electronics Engineers Inc., 2021. doi: 10.1109/BioCAS49922.2021.9644955.

[142] N. Moser, L. Keeble, J. Rodriguez-Manzano, and P. Georgiou, "ISFET arrays for lab-on-chip technology: A review," *2019 26th IEEE International Conference on Electronics, Circuits and Systems, ICECS 2019*, pp. 57–60, Nov. 2019, doi: 10.1109/ICECS46596.2019.8965034.

[143] M. Douthwaite, N. Moser, and P. Georgiou, "CMOS ISFET Arrays for Integrated Electrochemical Sensing and Imaging Applications: A Tutorial," *IEEE Sens J*, vol. 21, no. 20, pp. 22155–22169, Oct. 2021, doi: 10.1109/JSEN.2021.3094206.

[144] P. Tripathi, N. Moser, and P. Georgiou, "Multiple Ion-channel ISFET Neuron for Lab-on-chip applications," in *BioCAS 2021 - IEEE Biomedical Circuits and Systems Conference, Proceedings*, Institute of Electrical and Electronics Engineers Inc., 2021. doi: 10.1109/BioCAS49922.2021.9645040.

[145] J. Han, M. Cacho-Soblechero, M. Douthwaite, and P. Georgiou, "A digital ISFET sensor with in-pixel ADC," in *Proceedings - IEEE International Symposium on Circuits and Systems*, Institute of Electrical and Electronics Engineers Inc., 2021. doi: 10.1109/ISCAS51556.2021.9401244.

[146] Q. Hua, M. Cacho-Soblechero, and P. Georgiou, "A multi-sensing ISFET array for simultaneous in-pixel detection of light, temperature, moisture and ions," in *Proceedings - IEEE International Symposium on Circuits and Systems*, 2021. doi: 10.1109/ISCAS51556.2021.9401778.

[147] N. Miscourides and P. Georgiou, "Mismatch Compensation in ISFET Arrays using a Parasitic Programmable Gate," in *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, IEEE, May 2019, pp. 1–5. doi: 10.1109/ISCAS.2019.8702148.

[148] M. J. Milgrew and D. R. S. Cumming, "Matching the Transconductance Characteristics of CMOS ISFET Arrays by Removing Trapped Charge," *IEEE Trans Electron Devices*, vol. 55, no. 4, pp. 1074–1079, Apr. 2008, doi: 10.1109/TED.2008.916680.

[149] Yuanqi Hu and P. Georgiou, "A Robust ISFET pH-Measuring Front-End for Chemical Reaction Monitoring," *IEEE Trans Biomed Circuits Syst*, vol. 8, no. 2, pp. 177–185, Apr. 2014, doi: 10.1109/TBCAS.2014.2313512.

[150] S. Jamasb, S. D. Collins, and R. L. Smith, “A physical model for threshold voltage instability in Si3N4-Gate H+-sensitive FET’s (pH ISFET’s),” *IEEE Trans Electron Devices*, vol. 45, no. 6, pp. 1239–1245, 1998, doi: 10.1109/16.678525.

[151] A. Elyasi, M. Fouladian, and S. Jamasb, “Counteracting Threshold-Voltage Drift in Ion-Selective Field Effect Transistors (ISFETs) Using Threshold-Setting Ion Implantation,” *IEEE Journal of the Electron Devices Society*, vol. 6, pp. 747–754, Jun. 2018, doi: 10.1109/JEDS.2018.2847740.

[152] N. Moser, T. S. Lande, C. Toumazou, and P. Georgiou, “ISFETs in CMOS and Emergent Trends in Instrumentation: A Review,” *IEEE Sensors Journal*, vol. 16, no. 17. Institute of Electrical and Electronics Engineers Inc., pp. 6496–6514, Sep. 01, 2016. doi: 10.1109/JSEN.2016.2585920.

[153] P. A. Hammond and D. R. S. Cumming, “Performance and system-on-chip integration of an unmodified CMOS ISFET,” in *Sensors and Actuators, B: Chemical*, Nov. 2005, pp. 254–258. doi: 10.1016/j.snb.2004.12.065.

[154] P. Georgiou and C. Toumazou, “An adaptive CMOS-based PG-ISFET for pH sensing,” *Proceedings - IEEE International Symposium on Circuits and Systems*, pp. 557–560, 2009, doi: 10.1109/ISCAS.2009.5117809.

[155] Y. Hu, N. Moser, and P. Georgiou, “A 32 $\times$ 32 ISFET Chemical Sensing Array With Integrated Trapped Charge and Gain Compensation,” *IEEE Sens J*, vol. 17, no. 16, pp. 5276–5284, Aug. 2017, doi: 10.1109/JSEN.2017.2722043.

[156] N. Miscourides, L. S. Yu, J. Rodriguez-Manzano, and P. Georgiou, “A 12.8 k Current-Mode Velocity-Saturation ISFET Array for On-Chip Real-Time DNA Detection,” *IEEE Trans Biomed Circuits Syst*, vol. 12, no. 5, pp. 1202–1214, Oct. 2018, doi: 10.1109/TBCAS.2018.2851448.

[157] B. C. Cheah *et al.*, “An Integrated Circuit for Chip-Based Analysis of Enzyme Kinetics and Metabolite Quantification,” *IEEE Trans Biomed Circuits Syst*, vol. 10, no. 3, pp. 721–730, Jun. 2016, doi: 10.1109/TBCAS.2015.2487603.

[158] Y. Jiang *et al.*, “A high-sensitivity potentiometric 65-nm CMOS ISFET sensor for rapid E. coli Screening,” *IEEE Trans Biomed Circuits Syst*, vol. 12, no. 2, pp. 402–415, Apr. 2018, doi: 10.1109/TBCAS.2018.2793861.

[159] B. Eversmann *et al.*, “A 128 128 CMOS Biosensor Array for Extracellular Recording of Neural Activity,” vol. 38, no. 12, pp. 2306–2317, 2003.

[160] V. Gruev, Z. Yang, J. Van Der Spiegel, and R. Etienne-Cummings, “Current mode image sensor with two transistors per pixel,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 6, pp. 1154–1165, 2010, doi: 10.1109/TCSI.2009.2030093.

[161] X. Wu, X. Liu, M. Zhang, and J. Van Der Spiegel, "Current mode image sensor with improved linearity and fixed-pattern noise," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 6, pp. 1666–1674, 2014, doi: 10.1109/TCSI.2013.2295009.

[162] S. Mehta and R. Etienne-Cummings, "A simplified normal optical flow measurement CMOS camera," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 53, no. 6, 2006, doi: 10.1109/TCSI.2006.875169.

[163] Y. L. Wong and P. A. Abshire, "A 144 × 144 current-mode image sensor with self-adapting mismatch reduction," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 8, 2007, doi: 10.1109/TCSI.2007.902505.

[164] V. Gruev, R. Etienne-Cummings, and T. Horiuchf, "Linear current mode imager with low fix pattern noise," in *Proceedings - IEEE International Symposium on Circuits and Systems*, 2004. doi: 10.1109/iscas.2004.1329140.

[165] S. Yoshimura, T. Sugiyama, K. Yonemot, and K. Ueda, "A 48kframe/s CMOS image sensor for real-time 3-D sensing and motion detection," in *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*, 2001. doi: 10.1109/isscc.2001.912561.

[166] M. Kim *et al.*, "Donor–Acceptor-Conjugated Polymer for High-Performance Organic Field-Effect Transistors: A Progress Report," *Adv Funct Mater*, vol. 30, no. 20, p. 1904545, May 2020, doi: 10.1002/ADFM.201904545.

[167] S. Fratini, M. Nikolka, A. Salleo, G. Schweicher, and H. Sirringhaus, "Charge transport in high-mobility conjugated polymers and molecular semiconductors," *Nature Materials 2020 19:5*, vol. 19, no. 5, pp. 491–502, Apr. 2020, doi: 10.1038/S41563-020-0647-2.

[168] T. Okachi, "Mobility overestimation due to minority carrier injection and trapping in organic field-effect transistors," *Org Electron*, vol. 57, pp. 34–44, Jun. 2018, doi: 10.1016/J.ORGEL.2018.02.034.

[169] T. Yang *et al.*, "Understanding, Optimizing, and Utilizing Nonideal Transistors Based on Organic or Organic Hybrid Semiconductors," *Adv Funct Mater*, vol. 30, no. 20, p. 1903889, May 2020, doi: 10.1002/ADFM.201903889.

[170] H. Phan *et al.*, "Electrical Double-Slope Nonideality in Organic Field-Effect Transistors," *Adv Funct Mater*, vol. 28, no. 17, p. 1707221, Apr. 2018, doi: 10.1002/ADFM.201707221.

[171] Z. Yang *et al.*, "Improving Bias-Stress Stability of p-Type Organic Field-Effect Transistors by Constructing an Electron Injection Barrier at the Drain Electrode/Semiconductor Interfaces," *Cite This: ACS Appl. Mater. Interfaces*, vol. 12, pp. 41886–41895, 2020, doi: 10.1021/acsami.0c12188.

[172] X. Wu *et al.*, "Air Effect on the Ideality of p-Type Organic Field-Effect Transistors: A Double-Edged Sword," *Adv Funct Mater*, vol. 29, no. 51, p. 1906653, Dec. 2019, doi: 10.1002/ADFM.201906653.

[173] H. Phan *et al.*, "Electrical Instability Induced by Electron Trapping in Low-Bandgap Donor–Acceptor Polymer Field-Effect Transistors," *Advanced Materials*, vol. 27, no. 43, pp. 7004–7009, Nov. 2015, doi: 10.1002/ADMA.201501757.

[174] Z. Yang *et al.*, "Improving Bias-Stress Stability of p-Type Organic Field-Effect Transistors by Constructing an Electron Injection Barrier at the Drain Electrode/Semiconductor Interfaces," *Cite This: ACS Appl. Mater. Interfaces*, vol. 12, pp. 41886–41895, 2020, doi: 10.1021/acsami.0c12188.

[175] M. Nikolka *et al.*, "High operational and environmental stability of high-mobility conjugated polymer field-effect transistors through the use of molecular additives," *Nature Materials 2017 16:3*, vol. 16, no. 3, pp. 356–362, Dec. 2016, doi: 10.1038/NMAT4785.

[176] H. Phan *et al.*, "Improving Electrical Stability and Ideality in Organic Field-Effect Transistors by the Addition of Fullerenes: Understanding the Working Mechanism," *Adv Funct Mater*, vol. 27, no. 38, p. 1701358, Oct. 2017, doi: 10.1002/ADFM.201701358.

[177] Y. Xu *et al.*, "Planar-Processed Polymer Transistors," *Advanced Materials*, vol. 28, no. 38, pp. 8531–8537, Oct. 2016, doi: 10.1002/ADMA.201601589.

[178] X. Wu *et al.*, "Improving Ideality of P-Type Organic Field-Effect Transistors via Preventing Undesired Minority Carrier Injection," *Adv Funct Mater*, vol. 31, no. 19, p. 2100202, May 2021, doi: 10.1002/ADFM.202100202.

[179] C. Wang *et al.*, *Organic semiconductor crystals*, vol. 47, no. 2. The Royal Society of Chemistry, 2018, pp. 422–500. doi: 10.1039/c7cs00490g.

[180] X. F. Wu *et al.*, "Improving Ideality of P-Type Organic Field-Effect Transistors via Preventing Undesired Minority Carrier Injection," *Adv Funct Mater*, vol. 31, no. 19, p. 2100202, May 2021, doi: 10.1002/adfm.202100202.

[181] M. R. Cavallari *et al.*, "Organic Thin-Film Transistors as Gas Sensors: A Review," *Materials (Basel)*, vol. 14, no. 1, pp. 1–32, Jan. 2020, doi: 10.3390/MA14010003.

[182] A. Bilgaiyan, S. Il Cho, M. Abiko, K. Watanabe, and M. Mizukami, "Flexible, high mobility short-channel organic thin film transistors and logic circuits based on 4H–21DNTT," *Scientific Reports 2021 11:1*, vol. 11, no. 1, pp. 1–12, Jun. 2021, doi: 10.1038/S41598-021-91239-7.

[183] C. L. Hansen, E. Skordalakest, J. M. Berger, and S. R. Quake, "A robust and scalable microfluidic metering method that allows protein crystal growth by free interface diffusion," *Proc Natl Acad Sci U S A*, vol. 99, no. 26, pp. 16531–16536, Dec. 2002, doi: 10.1073/pnas.262485199.

[184] S. Takayama, E. Ostuni, P. LeDuc, K. Naruse, D. E. Ingber, and G. M. Whitesides, "Subcellular positioning of small molecules," *Nature*, vol. 411, no. 6841, p. 1016, Jun. 2001, doi: 10.1038/35082637.

[185] J. Son, R. Samuel, B. K. Gale, D. T. Carrell, and J. M. Hotaling, “Separation of sperm cells from samples containing high concentrations of white blood cells using a spiral channel,” *Biomicrofluidics*, vol. 11, no. 5, Sep. 2017, doi: 10.1063/1.4994548.

[186] A. R. Jafek, S. Harbertson, H. Brady, R. Samuel, and B. K. Gale, “Instrumentation for xPCR Incorporating qPCR and HRMA,” *Anal Chem*, vol. 90, no. 12, pp. 7190–7196, Jun. 2018, doi: 10.1021/acs.analchem.7b05176.

[187] A. Bange, H. B. Halsall, and W. R. Heineman, “Microfluidic immunosensor systems,” *Biosensors and Bioelectronics*, vol. 20, no. 12. Biosens Bioelectron, pp. 2488–2503, Jun. 15, 2005. doi: 10.1016/j.bios.2004.10.016.

[188] M. T. Guo, A. Rotem, J. A. Heyman, and D. A. Weitz, “Droplet microfluidics for high-throughput biological assays,” *Lab on a Chip*, vol. 12, no. 12. Lab Chip, pp. 2146–2155, Jun. 21, 2012. doi: 10.1039/c2lc21147e.

[189] M. Safdar, J. Jänis, and S. Sánchez, “Microfluidic fuel cells for energy generation,” *Lab on a Chip*, vol. 16, no. 15. Lab Chip, pp. 2754–2758, 2016. doi: 10.1039/c6lc90070d.

[190] Y. Xia and G. M. Whitesides, “Soft lithography,” *Annual Review of Materials Science*, vol. 28, no. 1, pp. 153–184, Nov. 1998, doi: 10.1146/annurev.matsci.28.1.153.

[191] J. C. McDonald *et al.*, “Fabrication of microfluidic systems in poly(dimethylsiloxane),” *Electrophoresis*, vol. 21, no. 1. pp. 27–40, 2000. doi: 10.1002/(SICI)1522-2683(20000101)21:1<27::AID-ELPS27>3.0.CO;2-C.

[192] D. Qin, Y. Xia, and G. M. Whitesides, “Soft lithography for micro- and nanoscale patterning,” *Nat Protoc*, vol. 5, no. 3, pp. 491–502, Mar. 2010, doi: 10.1038/nprot.2009.234.

[193] V. Faustino, S. O. Catarino, R. Lima, and G. Minas, “Biomedical microfluidic devices by using low-cost fabrication techniques: A review,” *J Biomech*, vol. 49, no. 11, pp. 2280–2292, Jul. 2016, doi: 10.1016/j.jbiomech.2015.11.031.

[194] M. Telting-Diaz and E. Bakker, “Mass-Produced Ionophore-Based Fluorescent Microspheres for Trace Level Determination of Lead Ions,” *Anal Chem*, vol. 74, no. 20, pp. 5251–5256, Oct. 2002, doi: 10.1021/AC025596I.

[195] X. Wang and X. Zhang, “Electrochemical co-reduction synthesis of graphene/nano-gold composites and its application to electrochemical glucose biosensor,” *Electrochim Acta*, vol. 112, pp. 774–782, Dec. 2013, doi: 10.1016/J.ELECTACTA.2013.09.036.

[196] B. J. Privett, J. H. Shin, and M. H. Schoenfisch, “Electrochemical sensors,” *Anal Chem*, vol. 82, no. 12, pp. 4723–4741, Jun. 2010, doi: 10.1021/AC101075N/ASSET/IMAGES/AC-2010-01075N_M004.GIF.

[197] C. Chen, J. F. Khosrowabadi Kotyk, and S. W. Sheehan, “Progress toward Commercial Application of Electrochemical Carbon Dioxide Reduction,” *Chem*, vol. 4, no. 11, pp. 2571–2586, Nov. 2018, doi: 10.1016/J.CHEMPR.2018.08.019.

[198] Y. Wang, H. Xu, J. Zhang, and G. Li, "Electrochemical Sensors for Clinic Analysis," *Sensors 2008, Vol. 8, Pages 2043-2081*, vol. 8, no. 4, pp. 2043–2081, Mar. 2008, doi: 10.3390/S8042043.

[199] R. Soukup, A. Hamáček, and J. Řeboun, "Organic based sensors: Novel screen printing technique for sensing layers deposition," in *Proceedings of the International Spring Seminar on Electronics Technology*, IEEE, May 2012, pp. 19–24. doi: 10.1109/ISSE.2012.6273101.

[200] M. Koden, "Flexible substrates and non-ITO transparent electrodes for organic electronics," in *Proceedings of AM-FPD 2015 - 22nd International Workshop on Active-Matrix Flatpanel Displays and Devices: TFT Technologies and FPD Materials*, IEEE, Jul. 2015, pp. 13–16. doi: 10.1109/AM-FPD.2015.7173183.

[201] T. Sauter *et al.*, "Making optical MEMS sensors more compact using organic light sources and detectors," in *19th IEEE International Conference on Emerging Technologies and Factory Automation, ETFA 2014*, IEEE, Sep. 2014, pp. 1–4. doi: 10.1109/ETFA.2014.7005342.

[202] T. Komoda, N. Ide, K. Varutt, K. Yamae, H. Tsuji, and Y. Matsuhisa, "High-performance white OLEDs with high color-rendering index for next-generation solid-state lighting," *J Soc Inf Disp*, vol. 19, no. 11, p. 838, 2011, doi: 10.1889/jsid19.11.838.

[203] M. G. Kane *et al.*, "Analog and digital circuits using organic thin-film transistors on polyester substrates," *IEEE Electron Device Letters*, vol. 21, no. 11, pp. 534–536, Nov. 2000, doi: 10.1109/55.877202.

[204] G. H. Gelinck *et al.*, "X-Ray Detector-on-Plastic with High Sensitivity Using Low Cost, Solution-Processed Organic Photodiodes," *IEEE Trans Electron Devices*, vol. 63, no. 1, pp. 197–204, Jan. 2016, doi: 10.1109/TED.2015.2432572.

[205] M. S. Weaver *et al.*, "Organic light-emitting devices with extended operating lifetimes on plastic substrates," *Appl Phys Lett*, vol. 81, no. 16, pp. 2929–2931, Oct. 2002, doi: 10.1063/1.1514831.

[206] J. A. Rogers, Z. Bao, A. Dodabalapur, and A. Makhija, "Organic smart pixels and complementary inverter circuits formed on plastic substrates by casting and rubber stamping," *IEEE Electron Device Letters*, vol. 21, no. 3, pp. 100–103, Mar. 2000, doi: 10.1109/55.823569.

[207] M. Jung *et al.*, "All-Printed and roll-to-roll-printable 13.56-MHz-operated 1-bit RF tag on plastic foils," *IEEE Trans Electron Devices*, vol. 57, no. 3, pp. 571–580, Mar. 2010, doi: 10.1109/TED.2009.2039541.

[208] S. R. Forrest, "The path to ubiquitous and low-cost organic electronic appliances on plastic," *Nature 2004 428:6986*, vol. 428, no. 6986, pp. 911–918, Apr. 2004, doi: 10.1038/NATURE02498.

[209] J. Kawahara, P. A. Ersman, K. Katoh, and M. Berggren, "Fast-switching printed organic electrochemical transistors including electronic vias through plastic and paper substrates," *IEEE Trans Electron Devices*, vol. 60, no. 6, pp. 2052–2056, Jun. 2013, doi: 10.1109/TED.2013.2258923.

[210] G. Orecchini *et al.*, "Inkjet printed organic transistors for sustainable electronics," in *Proceedings - Electronic Components and Technology Conference*, IEEE, 2010, pp. 985–989. doi: 10.1109/ECTC.2010.5490659.

[211] S. R. Forrest, "The path to ubiquitous and low-cost organic electronic appliances on plastic," *Nature*, vol. 428, no. 6986, pp. 911–918, Apr. 2004, doi: 10.1038/nature02498.

[212] V. Lemaur, J. Cornil, R. Lazzaroni, H. Sirringhaus, D. Beljonne, and Y. Olivier, "Resilience to Conformational Fluctuations Controls Energetic Disorder in Conjugated Polymer Materials: Insights from Atomistic Simulations," *Chemistry of Materials*, vol. 31, no. 17, pp. 6889–6899, Sep. 2019, doi: 10.1021/acs.chemmater.9b01286.

[213] G. Schweicher *et al.*, "Chasing the 'Killer' Phonon Mode for the Rational Design of Low-Disorder, High-Mobility Molecular Semiconductors," *Advanced Materials*, vol. 31, no. 43, p. 1902407, Oct. 2019, doi: 10.1002/adma.201902407.

[214] D. Venkateshvaran *et al.*, "Approaching disorder-free transport in high-mobility conjugated polymers," *Nature*, vol. 515, no. 7527, pp. 384–388, Nov. 2014, doi: 10.1038/nature13854.

[215] O. D. Jurchescu, J. Baas, and T. T. M. Palstra, "Effect of impurities on the mobility of single crystal pentacene," *Appl Phys Lett*, vol. 84, no. 16, pp. 3061–3063, Apr. 2004, doi: 10.1063/1.1704874.

[216] S. H. Hilal, S. W. Karickhoff, and L. A. Carreira, "Prediction of the vapor pressure boiling point, heat of vaporization and diffusion coefficient of organic compounds," *QSAR Comb Sci*, vol. 22, no. 6, pp. 565–574, Aug. 2003, doi: 10.1002/qsar.200330812.

[217] A. V. Yakubovich, W. J. Son, O. Kwon, H. Choi, B. Choi, and S. Kim, "Accurate Vapor Pressure Prediction for Large Organic Molecules: Application to Materials Utilized in Organic Light-Emitting Diodes," *J Chem Theory Comput*, vol. 16, no. 9, pp. 5845–5851, Sep. 2020, doi: 10.1021/acs.jctc.9b01245.

[218] C. C. Mattheus *et al.*, "Identification of polymorphs of pentacene," *Synth Met*, vol. 138, no. 3, pp. 475–481, Jul. 2003, doi: 10.1016/S0379-6779(02)00467-8.

[219] B. Stadlober *et al.*, "Structural and electrical properties of polymorphic pentacene thin films," in *Organic Field Effect Transistors II*, C. D. Dimitrakopoulos, Ed., SPIE, Nov. 2003, p. 112. doi: 10.1117/12.505868.

[220] C. C. Mattheus, A. B. Dros, J. Baas, A. Meetsma, J. L. De Boer, and T. T. M. Palstra, "Polymorphism in pentacene," *Acta Crystallogr C*, vol. 57, no. 8, pp. 939–941, Aug. 2001, doi: 10.1107/S010827010100703X.

[221] M. H. Chowdhury, K. Aslan, S. N. Malyn, J. R. Lakowicz, and C. D. Geddes, “Metal-enhanced chemiluminescence: Radiating plasmons generated from chemically induced electronic excited states,” *Appl Phys Lett*, vol. 88, no. 17, p. 173104, Apr. 2006, doi: 10.1063/1.2195776.

[222] J. E. Anthony, J. S. Brooks, D. L. Eaton, and S. R. Parkin, “Functionalized pentacene: Improved electronic properties from control of solid-state order [20],” *J Am Chem Soc*, vol. 123, no. 38, pp. 9482–9483, Sep. 2001, doi: 10.1021/ja0162459.

[223] Z. Bao, A. J. Lovinger, and A. Dodabalapur, “Highly ordered vacuum-deposited thin films of metallophthalocyanines and their applications in field-effect transistors,” *Advanced Materials*, vol. 9, no. 1, pp. 42–44, Jan. 1997, doi: 10.1002/adma.19970090108.

[224] H. Yan *et al.*, “A high-mobility electron-transporting polymer for printed transistors,” *Nature*, vol. 457, no. 7230, pp. 679–686, Feb. 2009, doi: 10.1038/nature07727.

[225] J. Zaumseil and H. Sirringhaus, “Electron and ambipolar transport in organic field-effect transistors,” *Chem Rev*, vol. 107, no. 4, pp. 1296–1323, Apr. 2007, doi: 10.1021/cr0501543.

[226] J. C. Scott, “Metal–organic interface and charge injection in organic electronic devices,” *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, vol. 21, no. 3, pp. 521–531, May 2003, doi: 10.1116/1.1559919.

[227] Z. Bao, A. J. Lovinger, and J. Brown, “New air-stable n-channel organs thin film transistors,” *J Am Chem Soc*, vol. 120, no. 1, pp. 207–208, Jan. 1998, doi: 10.1021/ja9727629.

[228] J. G. Laquindanum, H. E. Katz, A. Dodabalapur, and A. J. Lovinger, “n-Channel organic transistor materials based on naphthalene frameworks,” *J Am Chem Soc*, vol. 118, no. 45, pp. 11331–11332, Nov. 1996, doi: 10.1021/ja962461j.

[229] R. C. Haddon, A. S. Perel, R. C. Morris, T. T. M. Palstra, A. F. Hebard, and R. M. Fleming, “C60 thin film transistors,” *Appl Phys Lett*, vol. 67, no. 1, p. 121, Jul. 1995, doi: 10.1063/1.115503.

[230] T. C. Huang *et al.*, “Pseudo-CMOS: A design style for low-cost and robust flexible electronics,” *IEEE Trans Electron Devices*, vol. 58, no. 1, pp. 141–150, Jan. 2011, doi: 10.1109/TED.2010.2088127.

[231] S. Inoue *et al.*, “Regioisomeric control of layered crystallinity in solution-processable organic semiconductors,” *Chem Sci*, vol. 11, no. 46, pp. 12493–12505, Dec. 2020, doi: 10.1039/d0sc04461j.

[232] A. Assadi, C. Svensson, M. Willander, and O. Inganäs, “Field-effect mobility of poly(3-hexylthiophene),” *Appl Phys Lett*, vol. 53, no. 3, pp. 195–197, Jul. 1988, doi: 10.1063/1.100171.

[233] Z. Yao *et al.*, "Building crystal structures of conjugated polymers through X-ray diffraction and molecular modeling," *SmartMat*, vol. 2, no. 3, pp. 378–387, Sep. 2021, doi: 10.1002/smm2.1053.

[234] J. Lee *et al.*, "Universal Suzuki-Miyaura Catalyst-Transfer Polymerization for Precision Synthesis of Strong Donor/Acceptor-Based Conjugated Polymers and Their Sequence Engineering," *J Am Chem Soc*, vol. 143, no. 29, pp. 11180–11190, Jul. 2021, doi: 10.1021/jacs.1c05080.

[235] A. Bhardwaj, J. Kaur, M. Wuest, and F. Wuest, "In situ click chemistry generation of cyclooxygenase-2 inhibitors," *Nat Commun*, vol. 8, no. 1, Dec. 2017, doi: 10.1038/s41467-016-0009-6.

[236] P. Pahlavanlu *et al.*, "Templated approach to well-defined, oxidatively coupled conjugated polymers," *Polym Chem*, vol. 12, no. 4, pp. 511–518, Feb. 2021, doi: 10.1039/d0py01620a.

[237] N. K. Obhi, C. N. Jarrett-Wilkins, G. E. J. Hicks, and D. S. Seferos, "Self-Assembly of Poly(3-hexylthiophene) Bottlebrush Polymers into End-On-End Linear Fiber Morphologies," *Macromolecules*, vol. 53, no. 19, pp. 8592–8599, 2020, doi: 10.1021/acs.macromol.0c01641.

[238] S. Li, K. He, E. Prince, Y. Li, and D. S. Seferos, "Selenophene and Thiophene-Based Conjugated Polymer Gels," *ACS Mater Lett*, vol. 2, no. 12, pp. 1617–1623, 2020, doi: 10.1021/acsmaterialslett.0c00406.

[239] J. Y. Back *et al.*, "Investigation of structure-property relationships in diketopyrrolopyrrole-based polymer semiconductors via side-chain engineering," *Chemistry of Materials*, vol. 27, no. 5, pp. 1732–1739, 2015, doi: 10.1021/cm504545e.

[240] H. Bronstein, C. B. Nielsen, B. C. Schroeder, and I. McCulloch, "The role of chemical design in the performance of organic semiconductors," *Nat Rev Chem*, vol. 4, no. 2, pp. 66–77, Jan. 2020, doi: 10.1038/s41570-019-0152-9.

[241] T. Lei, Y. Cao, X. Zhou, Y. Peng, J. Bian, and J. Pei, "Systematic investigation of isoindigo-based polymeric field-effect transistors: Design strategy and impact of polymer symmetry and backbone curvature," *Chemistry of Materials*, vol. 24, no. 10, pp. 1762–1770, 2012, doi: 10.1021/cm300117x.

[242] Y. C. Lin *et al.*, "Study on Intrinsic Stretchability of Diketopyrrolopyrrole-Based π-Conjugated Copolymers with Poly(acryl amide) Side Chains for Organic Field-Effect Transistors," *ACS Appl Mater Interfaces*, vol. 12, no. 29, pp. 33014–33027, 2020, doi: 10.1021/acsami.0c07496.

[243] J. Li *et al.*, "A stable solution-processed polymer semiconductor with record high-mobility for printed transistors," *Sci Rep*, vol. 2, no. 1, pp. 1–9, Oct. 2012, doi: 10.1038/srep00754.

[244] J. Xu *et al.*, "Highly stretchable polymer semiconductor films through the nanoconfinement effect," *Science (1979)*, vol. 355, no. 6320, Jan. 2017, doi: 10.1126/science.aah4496.

[245] M. Charbonneau *et al.*, "A large-area gravure printed process for P-type organic thin-film transistors on plastic substrates," *European Solid-State Device Research Conference*, vol. 2018-Septe, pp. 70–73, Oct. 2018, doi: 10.1109/ESSDERC.2018.8486895.

[246] U. Kraft *et al.*, "Fluoroalkylphosphonic acid self-assembled monolayer gate dielectrics for threshold-voltage control in low-voltage organic thin-film transistors," *J Mater Chem*, vol. 20, no. 31, pp. 6416–6418, Aug. 2010, doi: 10.1039/c0jm01292k.

[247] D. K. Hwang, C. Fuentes-Hernandez, J. Kim, W. J. Potscavage, S. J. Kim, and B. Kippelen, "Top-gate organic field-effect transistors with high environmental and operational stability," *Advanced Materials*, vol. 23, no. 10, pp. 1293–1298, Mar. 2011, doi: 10.1002/adma.201004278.

[248] H. Seong, K. Pak, M. Joo, J. Choi, and S. G. Im, "Vapor-Phase Deposited Ultrathin Polymer Gate Dielectrics for High-Performance Organic Thin Film Transistors," *Adv Electron Mater*, vol. 2, no. 2, Feb. 2016, doi: 10.1002/aelm.201500209.

[249] X. H. Zhang *et al.*, "High-performance pentacene field-effect transistors using Al2O3 gate dielectrics prepared by atomic layer deposition (ALD)," *Org Electron*, vol. 8, no. 6, pp. 718–726, 2007, doi: 10.1016/j.orgel.2007.06.009.

[250] M. Halik *et al.*, "Low-voltage organic transistors with an amorphous molecular gate dielectric," *Nature*, vol. 431, no. 7011, pp. 963–966, Oct. 2004, doi: 10.1038/nature02987.

[251] A. Facchetti, M. H. Yoon, and T. J. Marks, "Gate dielectrics for organic field-effect transistors: New opportunities for organic electronics," *Advanced Materials*, vol. 17, no. 14, pp. 1705–1725, Jul. 2005, doi: 10.1002/adma.200500517.

[252] C. Wang, W. Y. Lee, R. Nakajima, J. Mei, D. H. Kim, and Z. Bao, "Thiol-ene cross-linked polymer gate dielectrics for low-voltage organic thin-film transistors," *Chemistry of Materials*, vol. 25, no. 23, pp. 4806–4812, Dec. 2013, doi: 10.1021/cm403203k.

[253] J. Kim, J. Jang, K. Kim, H. Kim, S. H. Kim, and C. E. Park, "The Origin of Excellent Gate-Bias Stress Stability in Organic Field-Effect Transistors Employing Fluorinated-Polymer Gate Dielectrics," *Advanced Materials*, vol. 26, no. 42, pp. 7241–7246, Nov. 2014, doi: 10.1002/adma.201402363.

[254] S. Y. Yang, K. Shin, and C. E. Park, "The effect of gate-dielectric surface energy on pentacene morphology and organic field-effect transistor characteristics," *Adv Funct Mater*, vol. 15, no. 11, pp. 1806–1814, Nov. 2005, doi: 10.1002/adfm.200400486.

[255] H. Sakai, Y. Takahashi, and H. Murata, "Organic field effect transistors with dipole-polarized polymer gate dielectrics for control of threshold voltage," *Appl Phys Lett*, vol. 91, no. 11, 2007, doi: 10.1063/1.2783180.

[256] S. Bahrs, I. Stass, and S. Hildebrandt, "NEWS from pss in 2013," *physica status solidi (RRL) - Rapid Research Letters*, vol. 7, no. 1–2, pp. 1–2, Feb. 2013, doi: 10.1002/pssr.201350501.

[257] K. Kim *et al.*, “Grafting fluorinated polymer nanolayer for advancing the electrical stability of organic field-effect transistors,” *Chemistry of Materials*, vol. 26, no. 22, pp. 6467–6476, Sep. 2014, doi: 10.1021/cm5030266.

[258] G. H. Gelinck, T. C. T. Geuns, and D. M. De Leeuw, “High-performance all-polymer integrated circuits,” *Appl Phys Lett*, vol. 77, no. 10, pp. 1487–1489, Sep. 2000, doi: 10.1063/1.1290728.

[259] K. B. Blodgett and I. Langmuir, “Built-up films of barium stearate and their optical properties,” *Physical Review*, vol. 51, no. 11, pp. 964–982, 1937, doi: 10.1103/PhysRev.51.964.

[260] L. Li *et al.*, “Transparent Ag@Au-graphene patterns with conductive stability via inkjet printing,” *J Mater Chem C Mater*, vol. 5, no. 11, pp. 2800–2806, 2017, doi: 10.1039/c6tc05227d.

[261] C. Lee, N. R. Kim, J. Koo, Y. J. Lee, and H. M. Lee, “Cu-Ag core-shell nanoparticles with enhanced oxidation stability for printed electronics,” *Nanotechnology*, vol. 26, no. 45, p. 455601, Oct. 2015, doi: 10.1088/0957-4484/26/45/455601.

[262] Y. Ueoka *et al.*, “Effect of contact material on amorphous InGaZnO thin-film transistor characteristics,” *Jpn J Appl Phys*, vol. 53, no. 3 SPEC. ISSUE 1, p. 03CC04, Feb. 2014, doi: 10.7567/JJAP.53.03CC04.

[263] G. R. Hong *et al.*, “Unraveling the Issue of Ag Migration in Printable Source/Drain Electrodes Compatible with Versatile Solution-Processed Oxide Semiconductors for Printed Thin-Film Transistor Applications,” *ACS Appl Mater Interfaces*, vol. 9, no. 16, pp. 14058–14066, Apr. 2017, doi: 10.1021/acsami.7b00524.

[264] Y. Ueoka *et al.*, “Analysis of printed silver electrode on amorphous indium gallium zinc oxide,” *Jpn J Appl Phys*, vol. 53, no. 4 SPEC. ISSUE, p. 04EB03, Mar. 2014, doi: 10.7567/JJAP.53.04EB03.

[265] L. Gillan, J. Leppäniemi, K. Eiroma, H. Majumdar, and A. Alastalo, “High performance solution processed oxide thin-film transistors with inkjet printed Ag source-drain electrodes,” *J Mater Chem C Mater*, vol. 6, no. 13, pp. 3220–3225, Mar. 2018, doi: 10.1039/c7tc05679f.

[266] G. Cantarella *et al.*, “Buckled Thin-Film Transistors and Circuits on Soft Elastomers for Stretchable Electronics,” *ACS Appl Mater Interfaces*, vol. 9, no. 34, pp. 28750–28757, Aug. 2017, doi: 10.1021/acsami.7b08153.

[267] G. Cantarella *et al.*, “Design of Engineered Elastomeric Substrate for Stretchable Active Devices and Sensors,” *Adv Funct Mater*, vol. 28, no. 30, Jul. 2018, doi: 10.1002/adfm.201705132.

[268] D. Karnaushenko *et al.*, “Biomimetic Microelectronics for Regenerative Neuronal Cuff Implants,” *Advanced Materials*, vol. 27, no. 43, pp. 6797–6805, Nov. 2015, doi: 10.1002/adma.201503696.

[269] D. Karnaushenko *et al.*, “Microelectronics: Biomimetic Microelectronics for Regenerative Neuronal Cuff Implants (Adv. Mater. 43/2015),” *Advanced Materials*, vol. 27, no. 43, pp. 6769–6769, Nov. 2015, doi: 10.1002/adma.201570290.

[270] I. M. Graz, D. P. J. Cotton, A. Robinson, and S. P. Lacour, “Silicone substrate with in situ strain relief for stretchable thin-film transistors,” *Appl Phys Lett*, vol. 98, no. 12, Mar. 2011, doi: 10.1063/1.3570661.

[271] M. Kim *et al.*, “Fully-integrated, bezel-less transistor arrays using reversibly foldable interconnects and stretchable origami substrates,” *Nanoscale*, vol. 8, no. 18, pp. 9504–9510, May 2016, doi: 10.1039/c6nr02041k.

[272] S. P. Lacour and S. Wagner, “Thin film transistor circuits integrated onto elastomeric substrates for elastically stretchable electronics,” *Technical Digest - International Electron Devices Meeting, IEDM*, vol. 2005, pp. 101–104, 2005, doi: 10.1109/iedm.2005.1609278.

[273] J. Jin, J. H. Ko, S. Yang, and B. S. Bae, “Rollable transparent glass-fabric reinforced composite substrate for flexible devices,” *Advanced Materials*, vol. 22, no. 40, pp. 4510–4515, 2010, doi: 10.1002/adma.201002198.

[274] A. Marette, A. Poulin, N. Besse, S. Rosset, D. Briand, and H. Shea, “Flexible Zinc–Tin Oxide Thin Film Transistors Operating at 1 kV for Integrated Switching of Dielectric Elastomer Actuators Arrays,” *Advanced Materials*, vol. 29, no. 30, p. 1, Aug. 2017, doi: 10.1002/adma.201700880.

[275] J. Y. Oh *et al.*, “Spontaneously Formed Wrinkled Substrates for Stretchable Electronics Using Intrinsically Rigid Materials,” *IEEE Electron Device Letters*, vol. 37, no. 5, pp. 588–590, 2016, doi: 10.1109/LED.2016.2548019.

[276] M. de Podesta, N. P. Laboratory, and UK, *Understanding the Properties of Matter*. 1996. doi: 10.4324/9780203450611.

[277] N. Münzenrieder, G. Cantarella, L. Petti, and J. Costa, “Oxide Thin-Film Electronics for the Front-End Conditioning of Flexible Magnetic Field Sensors,” *Minerals, Metals and Materials Series*, vol. 5, pp. 294–302, 2021, doi: 10.1007/978-3-030-65261-6_26.

[278] V. K. Bandari *et al.*, “A flexible microsystem capable of controlled motion and actuation by wireless power transfer,” *Nat Electron*, vol. 3, no. 3, pp. 172–180, Mar. 2020, doi: 10.1038/s41928-020-0384-1.

[279] K. Torikai, R. Furlan De Oliveira, D. H. Starnini De Camargo, and C. C. Bof Bufon, “Low-Voltage, Flexible, and Self-Encapsulated Ultracompact Organic Thin-Film Transistors Based on Nanomembranes,” *Nano Lett*, vol. 18, no. 9, pp. 5552–5561, Sep. 2018, doi: 10.1021/acs.nanolett.8b01958.

[280] V. K. Bandari *et al.*, "A flexible microsystem capable of controlled motion and actuation by wireless power transfer," *Nat Electron*, vol. 3, no. 3, pp. 172–180, Mar. 2020, doi: 10.1038/s41928-020-0384-1.

[281] G. Lee *et al.*, "Nature-inspired rollable electronics," *NPG Asia Mater*, vol. 11, no. 1, Dec. 2019, doi: 10.1038/s41427-019-0169-z.

[282] S. H. Jin *et al.*, "Solution-processed single-walled carbon nanotube field effect transistors and bootstrapped inverters for disintegratable, transient electronics," *Appl Phys Lett*, vol. 105, no. 1, p. 154507, Jul. 2014, doi: 10.1063/1.4885761.

[283] N. Münzenrieder *et al.*, "Investigation of gate material ductility enables flexible a-IGZO TFTs bendable to a radius of 1.7 mm," *European Solid-State Device Research Conference*, pp. 362–365, 2013, doi: 10.1109/ESSDERC.2013.6818893.

[284] S. H. Jin *et al.*, "Solution-processed single-walled carbon nanotube field effect transistors and bootstrapped inverters for disintegratable, transient electronics," *Appl Phys Lett*, vol. 105, no. 1, p. 013506, Jul. 2014, doi: 10.1063/1.4885761.

[285] S. H. Jin *et al.*, "Water-soluble thin film transistors and circuits based on amorphous indium-gallium-zinc oxide," *ACS Appl Mater Interfaces*, vol. 7, no. 15, pp. 8268–8274, Apr. 2015, doi: 10.1021/acsami.5b00086.

[286] S.-W. Hwang *et al.*, "High-performance biodegradable/transient electronics on biodegradable polymers," *Wiley Online Library*, vol. 26, no. 23, pp. 3905–3911, Jun. 2014, doi: 10.1002/adma.201306050.

[287] H. Lopez Hernandez *et al.*, "Triggered transience of metastable poly (phthalaldehyde) for transient electronics," *Wiley Online Library*, vol. 26, no. 45, pp. 7637–7642, 2014, doi: 10.1002/adma.201403045.

[288] M. Flinck, S. H. Kramer, and S. F. Pedersen, "Roles of pH in control of cell proliferation," *Acta Physiologica*, vol. 223, no. 3, p. e13068, Jul. 2018, doi: 10.1111/APHA.13068.

[289] W. F. Boron, "Regulation of intracellular pH," *American Journal of Physiology - Advances in Physiology Education*, vol. 28, no. 4, pp. 160–179, 2004, doi: 10.1152/ADVAN.00045.2004/ASSET/IMAGES/LARGE/ZU10040402401018.JPEG.

[290] I. Pavlov, K. Kaila, D. M. Kullmann, and R. Miles, "Cortical inhibition, pH and cell excitability in epilepsy: what are optimal targets for antiepileptic interventions?," *J Physiol*, vol. 591, no. 4, pp. 765–774, Feb. 2013, doi: 10.1113/JPHYSIOL.2012.237958.

[291] M. Nurul Islam and B. Mazhari, "Organic thin film transistors with asymmetrically placed source and drain contact," *Org Electron*, vol. 14, no. 3, pp. 862–867, Mar. 2013, doi: 10.1016/J.ORGEL.2012.12.037.

[292] R. Zeng, J. Zhang, C. Sun, M. Xu, S. L. Zhang, and D. Wu, "A reference-less semiconductor ion sensor," *Sens Actuators B Chem*, vol. 254, pp. 102–109, Jan. 2018, doi: 10.1016/J.SNB.2017.06.152.

[293] J. H. Jeon and W. J. Cho, "High-performance extended-gate ion-sensitive field-effect transistors with multi-gate structure for transparent, flexible, and wearable biosensors," *http://www-tandfonline-com.are.uab.cat/action/journalInformation?show=aimsScope&journalCode=tsta20#.VmBmuzZFCUk*, vol. 21, no. 1, pp. 371–378, Jan. 2020, doi: 10.1080/14686996.2020.1775477.

[294] K. B. Parizi, "ADVANCES ON CHIP INSIDE A CELL FOR MONITORING PHYSIOLOGICAL CELL PARAMETERS A DISSERTATION SUBMITTED TO THE DEPARTMENT OF ELECTRICAL ENGINEERING AND THE COMMITTEE ON GRADUATE STUDIES OF STANFORD UNIVERSITY IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY," 2016.

[295] W. Vonau, F. Gerlach, and S. Herrmann, "Conception of a new technique in cell cultivation using a lab-on-chip aided miniaturised device with calibratable electrochemical sensors," *Microchimica Acta*, vol. 171, no. 3, pp. 451–456, Dec. 2010, doi: 10.1007/S00604-010-0427-9/FIGURES/6.

[296] M. Bouftas, "A Systematic Review on the Feasibility of Salivary Biomarkers for Alzheimer's Disease," *Journal of Prevention of Alzheimer's Disease*, vol. 8, no. 1, pp. 84–91, Jan. 2021, doi: 10.14283/JPAD.2020.57/TABLES/1.

[297] H. C. Lau *et al.*, "Non-Invasive Screening for Alzheimer's Disease by Sensing Salivary Sugar Using Drosophila Cells Expressing Gustatory Receptor (Gr5a) Immobilized on an Extended Gate Ion-Sensitive Field-Effect Transistor (EG-ISFET) Biosensor," *PLoS One*, vol. 10, no. 2, p. e0117810, Feb. 2015, doi: 10.1371/JOURNAL.PONE.0117810.

[298] B. A. McKinley, "ISFET and fiber optic sensor technologies: In vivo experience for critical care monitoring," *Chem Rev*, vol. 108, no. 2, pp. 826–844, Feb. 2008, doi: 10.1021/CR068120Y/ASSET/IMAGES/LARGE/CR068120YF00007.JPEG.

[299] M. S. Baghini, A. Vilouras, M. Douthwaite, P. Georgiou, and R. Dahiya, "Ultra-thin ISFET-based sensing systems," *Electrochemical Science Advances*, vol. 2, no. 6, p. e2100202, Dec. 2022, doi: 10.1002/ELSA.202100202.

[300] E. Genco *et al.*, " A 4 × 4 Biosensor Array With a 42- μ W/Channel Multiplexed Current Sensitive Front-End Featuring 137-dB DR and Zeptomolar Sensitivity ," *IEEE Open Journal of the Solid-State Circuits Society*, vol. 2, pp. 193–207, Nov. 2022, doi: 10.1109/ojsscs.2022.3217231.

[301] J. Zeng, L. Kuang, N. Miscourides, and P. Georgiou, "A 128 × 128 Current-Mode Ultra-High Frame Rate ISFET Array With In-Pixel Calibration for Real-Time Ion Imaging," *IEEE Trans Biomed Circuits Syst*, vol. 14, no. 2, pp. 359–372, Apr. 2020, doi: 10.1109/TBCAS.2020.2973508.

[302] J. Zeng, N. Miscourides, and P. Georgiou, “A 128×128 Current-Mode Ultra-High Frame Rate ISFET Array for Ion Imaging,” *Proceedings - IEEE International Symposium on Circuits and Systems*, vol. 2018-May, pp. 7–11, 2018, doi: 10.1109/ISCAS.2018.8351178.

[303] Y. Cong, M. Xu, D. Zhao, and D. Wu, “A 3600 × 3600 large-scale ISFET sensor array for high-throughput pH sensing,” *Proceedings of International Conference on ASIC*, vol. 2017-Octob, pp. 957–960, 2017, doi: 10.1109/ASICON.2017.8252636.

[304] W. P. Chan, B. Premanode, and C. Toumazou, “64 pH-ISFET averaging array employing global negative current feedback,” *Electron Lett*, vol. 45, no. 11, pp. 536–537, 2009, doi: 10.1049/el.2009.0215.

[305] Z. Luo *et al.*, “Sub-thermionic, ultra-high-gain organic transistors and circuits,” *Nature Communications 2021 12:1*, vol. 12, no. 1, pp. 1–9, Mar. 2021, doi: 10.1038/S41467-021-22192-2.

[306] M. B. Das and R. D. Josephy, “High Frequency, High Power Igfet With Interdigital Electrodes and Plural Loope) Gate,” Mar. 1971.

[307] J.-N. Tisserant *et al.*, “Growth and Alignment of Thin Film Organic Single Crystals from Dewetting Patterns,” *ACS Nano*, vol. 7, no. 6, pp. 5506–5513, Jun. 2013, doi: 10.1021/nn401679s.

[308] S. Bi, Z. He, J. Chen, and D. Li, “Solution-grown small-molecule organic semiconductor with enhanced crystal alignment and areal coverage for organic thin film transistors,” *AIP Adv*, vol. 5, no. 7, Jul. 2015, doi: 10.1063/1.4927577.

[309] Y. Fujisaki, D. Takahashi, Y. Nakajima, M. Nakata, H. Tsuji, and T. Yamamoto, “Alignment Control of Patterned Organic Semiconductor Crystals in Short-Channel Transistor Using Unidirectional Solvent Evaporation Process,” *IEEE Trans Electron Devices*, vol. 62, no. 7, pp. 2306–2312, Jul. 2015, doi: 10.1109/TED.2015.2431372.

[310] D. A. Kleinman and A. L. Schawlow, “Corbino disk,” *J Appl Phys*, vol. 31, no. 12, pp. 2176–2187, Jun. 1960, doi: 10.1063/1.1735520.

[311] V. A. Guzenko *et al.*, “Weak antilocalization measurements on a 2-dimensional electron gas in an InGaSb/InAlSb heterostructure,” in *Physica Status Solidi (C) Current Topics in Solid State Physics*, 2006, pp. 4227–4230. doi: 10.1002/pssc.200672848.

[312] H. Klauk, D. J. Gundlach, J. A. Nichols, and T. N. Jackson, “Pentacene organic thin-film transistors for circuit and display applications,” *IEEE Trans Electron Devices*, vol. 46, no. 6, pp. 1258–1263, 1999, doi: 10.1109/16.766895.

[313] A. Arnal, C. Martínez-Domingo, S. Ogier, L. Terés, and E. Ramon, “Monotype organic dual threshold voltage using different OTFT geometries,” *Crystals (Basel)*, vol. 9, no. 7, pp. 1–15, 2019, doi: 10.3390/cryst9070333.

[314] Young Hee Byun *et al.*, "An amorphous silicon TFT with annular-shaped channel and reduced gate-source capacitance," *IEEE Trans Electron Devices*, vol. 43, no. 5, pp. 839–841, May 1996, doi: 10.1109/16.491263.

[315] D. Munteanu, S. Cristoloveanu, and H. Hovel, "Circular pseudo-metal oxide semiconductor field effect transistor in silicon-on-insulator analytical model, simulation, and measurements," *Electrochemical and Solid-State Letters*, vol. 2, no. 5, pp. 242–243, May 1999, doi: 10.1149/1.1390798/XML.

[316] C. Zhao, T. C. Fung, and J. Kanicki, "Half-Corbino short-channel amorphous In–Ga–Zn–O thin-film transistors with a-SiOx or a-SiOx/a-SiNx passivation layers," *Solid State Electron*, vol. 120, pp. 25–31, Jun. 2016, doi: 10.1016/J.SSE.2016.03.003.

[317] M. Aldrigo *et al.*, "Characteristics of Offset Corbino Thin Film Transistor: A Physical Model," *Electronics 2023, Vol. 12, Page 2195*, vol. 12, no. 10, p. 2195, May 2023, doi: 10.3390/ELECTRONICS12102195.

[318] M. Mativenga *et al.*, "49.2: Corbino TFTs for Large-Area AMOLED Displays," *SID Symposium Digest of Technical Papers*, vol. 45, no. 1, pp. 705–708, Jun. 2014, doi: 10.1002/J.2168-0159.2014.TB00185.X.

[319] A. Prakash, "What is FOSS? What is Open Source? Are They the Same Thing?," 2022, [Online]. Available: https://itsfoss.com/what-is-foss/

[320] "Semiconductor." https://www.appliedmaterials.com/us/en/semiconductor.html

[321] "Semiconductor Process," 2020. http://www.buysemi.net/?r=s142801&c=95/106

[322] "Semiconductor | Keysight." https://www.keysight.com/us/en/industries/semiconductor.html

[323] "Rigol DP832A Programmable DC Power Supply (3 Channels) | TEquipment." https://www.tequipment.net/RigolDP832A.html

[324] "Power supplies," *Electronic Design*, vol. 50, no. 1, p. 110, 2002, [Online]. Available: https://rigolshop.eu/products/power-supply/dp800/dp832a.html

[325] Rigol, "DP800 High Performance Linear DC Power Supplies." https://www.rigolna.com/products/dc-power-loads/dp800/

[326] C. P. Watson, B. A. Brown, J. Carter, J. Morgan, and D. M. Taylor, "Organic Ring Oscillators with Sub-200 ns Stage Delay Based on a Solution-Processed p-type Semiconductor Blend," *Adv Electron Mater*, vol. 2, no. 3, p. 1500322, Mar. 2016, doi: 10.1002/aelm.201500322.

[327] F. Torricelli *et al.*, "Unified drain-current model of complementary p- and n-type OTFTs," *Org Electron*, vol. 22, pp. 5–11, Jul. 2015, doi: 10.1016/j.orgel.2015.03.021.

[328] K. D. Jung, Y. C. Kim, B. J. Kim, B. G. Park, H. Shin, and J. D. Lee, "An analytic current-voltage equation for top-contact organic thin film transistors including the effects of variable

series resistance," *Jpn J Appl Phys*, vol. 47, no. 4 PART 2, pp. 3174–3178, Apr. 2008, doi: 10.1143/JJAP.47.3174.

[329] Young Hee Byun, W. Den Boer, Mohshi Yang, and Tieer Gu, "An amorphous silicon TFT with annular-shaped channel and reduced gate-source capacitance," *IEEE Trans Electron Devices*, vol. 43, no. 5, pp. 839–841, May 1996, doi: 10.1109/16.491263.

[330] M. Mativenga *et al.*, "Infinite output resistance of corbino thin-film transistors with an amorphous-In ga znO active layer for large-area AMOLED displays," *IEEE Trans Electron Devices*, vol. 61, no. 9, pp. 3199–3205, Sep. 2014, doi: 10.1109/TED.2014.2338306.

[331] R. A. Martin, S. Member, V. M. Da Costa, M. Hack, and J. G. Shaw, "High-Voltage Amorphous Silicon Thin-Film Transistors," *IEEE Trans Electron Devices*, vol. 40, no. 3, 1993.

[332] T. Unagami and O. Kogure, "High-Voltage TFT Fabricated in Recrystallized Polycrystalline Silicon," *IEEE Trans Electron Devices*, vol. 35, no. 3, pp. 314–319, 1988, doi: 10.1109/16.2457.

[333] V. K. Khanna, "Amorphous Si TFT," *Flexible Electronics, Volume 2*, pp. 1-1-1–27, Jul. 2019, doi: 10.1088/2053-2563/ab0d18ch1.

[334] D. H. Jeon, W. B. Jeong, J. S. Park, H. J. Chung, and S. W. Lee, "A high-gain two-stage amplifier using low-temperature poly-si oxide thin-film transistors with a Corbino structure," *Journal of Information Display*, vol. 23, no. 4, pp. 281–286, 2022, doi: 10.1080/15980316.2022.2102681.

[335] I. A. Technologies, "AN72845 - Design guidelines for Infineon quad flat no-lead (QFN) packaged devices," 2022, [Online]. Available: www.infineon.com

[336] W. Bond, "Assembly and PCB Layout Guidelines for QFN," *Assembly*, no. May, pp. 1–15, 2008.

[337] N. Semiconductors, "AN1902 Assembly guidelines for QFN (quad flat no-lead) and SON (small outline no-lead) packages Rev. 9-28 April 2021 Application note Document information Information Content NXP Semiconductors AN1902 Assembly guidelines for QFN (quad flat no-lead) and SO", [Online]. Available: www.nxp.com

[338] "Centro Nacional de Intoxicaciones." https://www.argentina.gob.ar/salud/hospital-nacional-posadas/intoxicaciones

[339] Digilent, "Analog Discovery 2 - Digilent Reference," *Digilent*, 2022. https://digilent.com/reference/test-and-measurement/analog-discovery-2/start (accessed May 19, 2023).

[340] S. D. Brotherton, *Introduction to thin film transistors: Physics and technology of TFTs*, vol. 9783319000. Springer International Publishing, 2013. doi: 10.1007/978-3-319-00002-2.

[341] S. Ataei and R. Manohar, “AMC: An asynchronous memory compiler,” in *Proceedings - International Symposium on Asynchronous Circuits and Systems*, IEEE, May 2019, pp. 1–8. doi: 10.1109/ASYNC.2019.00009.

[342] “IEEE International Roadmap for Devices and Systems - IEEE IRDS,” 2020. https://irds.ieee.org/

[343] “Efabless Open MPW Program.” https://platform.efabless.com/shuttles/MPW-7

[344] R. T. Edwards, M. Shalan, and M. Kassem, “Real Silicon Using Open-Source EDA,” *IEEE Des Test*, vol. 38, no. 2, pp. 38–44, Apr. 2021, doi: 10.1109/MDAT.2021.3050000.

[345] “OpenLane EDA tool repository.” https://github.com/The-OpenROAD-Project/OpenLane

[346] T. Ajayi *et al.*, “INVITED: Toward an open-source digital flow: First learnings from the OpenROAD project,” in *Proceedings - Design Automation Conference*, 2019. doi: 10.1145/3316781.3326334.

[347] “RISC-V International – RISC-V: The Open Standard RISC Instruction Set Architecture,” *3rd RISCV Workshop* , 2016. https://riscv.org/

[348] A. Traber *et al.*, “PULPino: A small single-core RISC-V SoC,” *riscv.org*, Accessed: Jun. 19, 2023. [Online]. Available: https://riscv.org/wp-content/uploads/2016/01/Wed1315-PULP-riscv3_noanim.pdf

[349] “SERV - The SErial RISC-V CPU.” https://github.com/olofk/serv

[350] D. Ditzel *et al.*, “Accelerating ML recommendation with over a thousand RISC-V/Tensor processors on esperanto’s ET-SoC-1 Chip,” *2021 IEEE Hot Chips 33 Symposium, HCS 2021*, Aug. 2021, doi: 10.1109/HCS52781.2021.9566904.

[351] “Transistor count - Wikipedia.” https://en.wikipedia.org/wiki/Transistor_count

[352] T. Spyrou, “OpenDB, OpenROAD’s Database,” *Proc. Workshop on Open-Source EDA Technology*, 2019, Accessed: Jun. 19, 2023. [Online]. Available: https://vlsicad.ucsd.edu/~tspyrouhttps://github.com/

[353] M. Mashayekhi, M. Llamas, J. Carrabina, J. Pallares, F. Vila, and L. Teres, “Development of a standard cell library and ASPEC design flow for Organic Thin Film Transistor technology,” *Proceedings of the 2014 29th Conference on Design of Circuits and Integrated Systems, DCIS 2014*, 2014, doi: 10.1109/DCIS.2014.7035529.

[354] S. Ogier, D. Sharkey, and A. Carreras, “Organic thin-film transistors with mobility of 3cm2/vs at L=5μm and a process temperature of 80 degrees celsius,” in *Digest of Technical Papers - SID International Symposium*, 2021. doi: 10.1002/sdtp.15218.

[355] A. D. D. Dwivedi and P. Kumari, “TCAD SIMULATION and PERFORMANCE ANALYSIS of SINGLE and DUAL GATE OTFTs,” *Surface Review and Letters*, vol. 27, no. 5, p. 1950145, May 2020, doi: 10.1142/S0218625X19501452.

[356] S. Pal and B. Kumar, “Low-Voltage Dual-Gate Organic Thin Film Transistors with Distinctly Placed Source and Drain,” *Communications in Computer and Information Science*, vol. 1066, pp. 727–738, 2019, doi: 10.1007/978-981-32-9767-8_60.

[357] B. Kumar, B. K. Kaushik, and Y. S. Negi, “Static and dynamic characteristics of dual gate organic TFT based NAND and NOR circuits,” *J Comput Electron*, vol. 13, no. 3, pp. 627–638, Sep. 2014, doi: 10.1007/s10825-014-0580-1.

Appendix A

In Appendix A, we present the extracted script used in JMP software for the calculation of the V_{th}. This script encompasses the specific steps and functions utilized to extract the V_{th} values from the obtained data. The script includes data manipulation techniques, statistical calculations, and graphical representations to facilitate the V_{th} extraction process.

```
Variability Chart(
	Y( :"VTH (Vd=-5V)"n ),
	X( :Width, :Vback_gate ),
	Model( "Main Effect" ),
	Historical Sigma( 0 ),
	Analysis Type( "Choose best analysis (EMS REML Bayesian)" ),
	Connect Cell Means( 1 ),
	Show Group Means( Vtop_gate, Vback_gate ),
	Show Grand Median( 1 ),
	Variability Summary Report( 1 ),
	XBar Control Limits( 1 ),
	"Gauge R&R"n( 6, 0, 0, 0 ),
	"Gauge R&R Report"n( 1 ),
	Points Jittered( 1 ),
	Show Box Plots( 1 ),
	Mean Diamonds( 1 ),
	Mean Plots( 1 ),
	Local Data Filter(
		Add Filter(
			columns(
				:Vtop_gate, :Vback_gate, :Vdrain, :Sweep Direction, :Test,
:Width
			),
			Display( :Vtop_gate, N Items( 4 ), Size( 178, 68 ) ),
			Display( :Vback_gate, N Items( 4 ), Size( 178, 68 ) ),
			Display( :Sweep Direction, N Items( 4 ), Size( 178, 68 ) )
		)
	),
	SendToReport(
		Dispatch(
			{"Variability Chart for VTH (Vd=-5V)"},
			"2",
			ScaleBox,
			{Format( "Fixed Dec", 12, 1 ), Min( -0.03125 ), Max( 2 ), Inc( 0.1
),
			Minor Ticks( 1 ), Add Ref Line(
				0, "Dotted", "Medium Light Gray", "", 1
			), Label Row( {Show Major Grid( 1 ), Show Minor Grid( 1 )} )}
		),
		Dispatch(
			{"Variability Chart for VTH (Vd=-5V)"},
			"Variability Chart",
			FrameBox,
			{Frame Size( 1183, 329 )}
		),
```

```
		Dispatch(
			{"Variability Chart for VTH (Vd=-5V)"},
			"Variability",
			FrameBox,
			{Frame Size( 77, 329 )}
		),
		Dispatch(
			{"Variability Chart for VTH (Vd=-5V)"},
			"2",
			ScaleBox( 2 ),
			{Format( "Fixed Dec", 12, 1 ), Min( -0.03125 ), Max( 2 ), Inc( 0.1
),
			Minor Ticks( 1 ), Add Ref Line(
				0, "Dotted", "Medium Light Gray", "", 1
			), Label Row( {Show Major Grid( 1 ), Show Minor Grid( 1 )} )}
		),
		Dispatch(
			{"Variability Chart for VTH (Vd=-5V)"},
			"Variability Chart",
			FrameBox( 2 ),
			{Frame Size( 1183, 329 )}
		),

		Dispatch(
			{"Gauge R&R Mean Plots", "Mean of VTH (Vd=-5V) by Vback_gate"},
			"2",
			ScaleBox,
			{Format( "Fixed Dec", 12, 1 ), Min( -0.03125 ), Max( 2 ), Inc( 0.1
),
			Minor Ticks( 1 ), Add Ref Line(
				0, "Dotted", "Medium Light Gray", "", 1
			), Label Row( {Show Major Grid( 1 ), Show Minor Grid( 1 )} )}
		),

	)
)
```

Appendix B

In Appendix B, we provide the PCell code used for generating interdigitated transistors on Glade-Python language. PCell (Parameterized Cell) is a technique commonly used in layout design automation to generate repetitive structures with varying parameters. The PCell code allows for the efficient generation of interdigitated transistor layouts with different dimensions and geometries, providing flexibility and automation in the design process.

```
################################################################################
# Cell Name: Partially-Overlapped OTFT with connections for test pads
# Technology: SmartKem-CPI
# v1 12/2020 A.Rezaee
# Contact: ashkan.rezaee@uab.cat
################################################################################

from ui import *
from DRCrules import * # Follow rules for the parametrized cell

def P_OTFT_K(cv, w=100, l=4, nf=4) :

    # Device layers

    player1="PasI"  # Passivation 1 layer
    player2="PasO"  # Passivation 2 layer
    # player3="PasO2"  # Passivation 3 layer
    clayer1="MET1"  # Metal 1 layer
    clayer2="MET2"  # Metal 2 layer
    clayer3="MET3"  # Metal 3 layer
    clayer4="MET4"  # Metal 4 layer
    tlayer="TEXTA"  # Text layer

    #Initial position -100,25
    posx = -100
    posy = 25
    # Max and min values for enter in the caracterization cell
    w_max = 200
    w_min = 28
    a_max = 200
    a_min = 28
    l_max = 200

    # Check rules and change to minimum or maximum.
    if l < M1_S:
        l = M1_S
        cv.dbReplaceProp("l", l)
        print("\n *** Warning *** transistor length lower than allowed")
        print("Finger length set to", l ,"um\n")

    if l > l_max:
        l = l_max
        cv.dbReplaceProp("l", l)
        print("\n *** Warning *** transistor length higher than allowed")
```

```
        print("Finger length set to", l ,"um\n")

    if w > w_max:
        w = w_max
        cv.dbReplaceProp("w", w)
        print("\n *** Warning *** transistor width higher than allowed")
        print("Finger width set to", w ,"um\n")

    if w < w_min:
        w = w_min
        cv.dbReplaceProp("w", w)
        print("\n *** Warning *** transistor width lower than allowed")
        print("Finger width set to", w ,"um\n")

    lib = cv.lib()
    tech = lib.tech()
    dbu = lib.dbuPerUU()

    height_dib = M1_W*(nf+1)+(2*M2M1_Os)+nf*l
    h_flag = False

    while height_dib < a_min:
        nf+=1
        height_dib = M1_W*(nf+1)+(2*M2M1_Os)+nf*l
        h_flag = True

    while height_dib > a_max:
        nf-=1
        height_dib = M1_W*(nf+1)+(2*M2M1_Os)+nf*l
        h_flag = True

    if h_flag == True:
        cv.dbReplaceProp("nf", nf)
        print("\n *** Warning *** transistor number of fingers and length not allowed")
        print("Finger number set to", nf ,"\n")

    # Create transistors layers
    wd= int(w*dbu)
    ld= int(l*dbu)

    # Met3 F-Gate
    layer = tech.getLayerNum(clayer3, "drawing")
    rectangle = Rect( int(-wd/2), 0, int(wd/2), height_dib*dbu)
    cv.dbCreateRect(rectangle, layer)

    # Met1 B-Gate
    layer = tech.getLayerNum(clayer1, "drawing")
    back_gate = Rect( int(-wd/2), 0, int(wd/2), height_dib*dbu)
    cv.dbCreateRect(back_gate, layer)

    # Met2 source
    layer = tech.getLayerNum(clayer2, "drawing")
    rectangle = Rect( int(-M1_W-M1_S-M1M2_U-w/2)*dbu, M2M1_Os*dbu, int(-M1_S-M1M2_U-
w/2)*dbu, dbu*(M1_W*(nf+1)+(1*M2M1_Os)+nf*l))
```

```
    cv.dbCreateRect(rectangle, layer)

    # Met2 drain
    layer = tech.getLayerNum(clayer2, "drawing")
    rectangle       =       Rect(       int(+M1_S+M1M2_U+w/2)*dbu,       M2M1_Os*dbu,
int(M1_W+M1_S+M1M2_U+w/2)*dbu, dbu*(M1_W*(nf+1)+(1*M2M1_Os)+nf*l))
    cv.dbCreateRect(rectangle, layer)

    # Fingers in MET2
    for i in range(nf+1):
        layer = tech.getLayerNum(clayer2, "drawing")
        rectangle = Rect(int(-M1_S*(1-i%2)-M1M2_U-w/2)*dbu, (M2M1_Os+(M1_W+l)*i)*dbu,
int(M1_S*(i%2)+M1M2_U+w/2)*dbu, (M1_W+M2M1_Os+(M1_W+l)*i)*dbu)
        cv.dbCreateRect(rectangle, layer)

     gate_via   =   Rect(   int(-(P2_D/2)-6)*dbu,   (P2M2_O)*dbu,   int(P2_D/2+6)*dbu,
(P2M2_O+P2_D)*dbu)

##  # Pads
    len_path = 150
    # Source Pad
    origin_pad1 = Point((-250)*dbu, (-200)*dbu)           # Point where the origin of
the pad 1 will be located
    end_pad1 = Point((2*len_path-400)*dbu, (2*len_path-350)*dbu) # Point where the pad
1 will end
    # Gate Pad
    origin_pad2 = Point((2*len_path-190)*dbu, (-200)*dbu)           # Point where the
origin of the pad 2 will be located
    end_pad2 = Point((2*len_path-40)*dbu, (2*len_path-350)*dbu) # Point where the pad
1 will end
    # Drain Pad
    origin_pad3 = Point((2*len_path-150)*dbu, (50)*dbu)            # Point where the
origin of the pad 3 will be located
    end_pad3 = Point((2*len_path)*dbu, (2*len_path-100)*dbu) # Point where the pad 1
will end
    # Back Gate Pad
    origin_pad4 = Point((2*len_path-600)*dbu, (50)*dbu)            # Point where the
origin of the pad 3 will be located
    end_pad4 = Point((2*len_path-450)*dbu, (2*len_path-100)*dbu) # Point where the pad
1 will end
    # layer = tech.getLayerNum(clayer1, "drawing")
    r1 = Rect(origin_pad1, end_pad1)
    r2 = Rect(origin_pad2, end_pad2)
    r3 = Rect(origin_pad3, end_pad3)
    r4 = Rect(origin_pad4, end_pad4)
    R=[r1,r2,r3,r4]

    layerlist=[clayer1,clayer4]
    for layer in layerlist:
        layer = tech.getLayerNum(layer, "drawing")
        for element in R:
            cv.dbCreateRect(element, layer);
    layer = tech.getLayerNum(clayer2, "drawing")
    cv.dbCreateRect(r1, layer);
```

```
    cv.dbCreateRect(r3, layer);
    # layer = tech.getLayerNum(clayer3, "drawing")
    # cv.dbCreateRect(r2, layer);
    layer = tech.getLayerNum(player1, "drawing")# Passivation layer 1
    r1 = Rect(r1.left()+5*dbu,r1.bottom()+5*dbu,r1.right()-5*dbu,r1.top()-5*dbu)
    r2 = Rect(r2.left()+5*dbu,r2.bottom()+5*dbu,r2.right()-5*dbu,r2.top()-5*dbu)
    r3 = Rect(r3.left()+5*dbu,r3.bottom()+5*dbu,r3.right()-5*dbu,r3.top()-5*dbu)
    r4 = Rect(r4.left()+5*dbu,r4.bottom()+5*dbu,r4.right()-5*dbu,r4.top()-5*dbu)
    cv.dbCreateRect(r1, layer);
    cv.dbCreateRect(r2, layer);
    cv.dbCreateRect(r3, layer);
    cv.dbCreateRect(r4, layer);

##  # Test Pads conecions
    # Source
    layer = tech.getLayerNum(clayer2, "drawing")
    a=max((M1_W*(nf+1)+(1*M2M1_Os)+nf*l),28)
    #   rectangle   =   Rect(   (-110)*dbu,   (2*len_path-355)*dbu,int(-M1_S-M1M2_U-
w/2)*dbu,a*dbu)
    rectangle = Rect( int(-20-M1_S-M1M2_U-w/2)*dbu, (2*len_path-355)*dbu, int(-M1_S-
M1M2_U-w/2)*dbu, (P2_D+2*P2M2_O)*dbu)
    cv.dbCreateRect(rectangle, layer)
    rectangle = Rect( (-250)*dbu, (-70)*dbu, int(-M1_S-M1M2_U-w/2)*dbu, (-40)*dbu)
    cv.dbCreateRect(rectangle, layer)
    # Drain
    layer = tech.getLayerNum(clayer2, "drawing")
    rectangle         =         Rect(int(+M1_S+M1M2_U+w/2)*dbu,         M2M1_Os*dbu,
int(20+M1_S+M1M2_U+w/2)*dbu, (125)*dbu)
    cv.dbCreateRect(rectangle, layer)
    rectangle = Rect(int(+M1_S+M1M2_U+w/2)*dbu, (100)*dbu, (225)*dbu, (125)*dbu)
    cv.dbCreateRect(rectangle, layer)

    # F-Gate
    layer = tech.getLayerNum(player1, "drawing")# Passivation layer 1
    rectangle = Rect((-5)*dbu, 5*dbu, (5)*dbu, (15)*dbu)
    cv.dbCreateRect(rectangle, layer)
    layer = tech.getLayerNum(clayer4, "drawing")
    gate_via.setBottom(-20*dbu)
    cv.dbCreateRect(gate_via, layer)
    gate_via.setRight((int(len_path/2)+len_path-40+P2_D)*dbu)
    gate_via.setTop((-30-P2_D)*dbu)
    cv.dbCreateRect(gate_via, layer)
    gate_via.setBottom((len_path-205)*dbu)
    gate_via.setLeft((int(len_path/2)+len_path-60)*dbu)
    cv.dbCreateRect(gate_via, layer)

    # B-Gate
    layer = tech.getLayerNum(clayer1, "drawing")

    BGate = Rect(Point((-10)*dbu, (20)*dbu), Point((10)*dbu, (200)*dbu))
    cv.dbCreateRect(BGate, layer);
    BGate = Rect(Point((-225)*dbu, (180)*dbu), Point((10)*dbu, (200)*dbu))
    cv.dbCreateRect(BGate, layer);
```

```
cv.update()
```

Appendix C

In Appendix C, we present the PCell code implemented in the Klayout-Python language for generating interdigitated transistors. This code serves as the core component of each cell library, allowing for the generation of transistors based on the specific design requirements. By calling this code, designers can easily generate the desired number of transistors needed for their circuit design.

...

```
def transistor(self, level, x, y, w_i, n_i, l_i, bg, load, Int_Con, ov_l, ov_r,
out):
    # Other design rules and other "fixed" variables
    # Layer properties
    dbu = self.layout.dbu
    # Assign layers using list comprehension
    layers = [self.layout.layer(i, 0) for i in [0, 1, 2, 3, 4, 6, 7, 9]]
    # Unpack layers into variables
    txt, bm, bl, sd, gm, pv, gc, pv2 = layers



    # fetch the parameters
    nr = 128  # Number of points in a circle
    # Global variables
    metal_ov = self.o / dbu
    via = self.via / dbu
    via_ov = self.via_ov / dbu
    finger_sep = self.s / dbu
    PDN_S_dbu = self.PDN_S / dbu
    finger_width = self.fw / dbu
    gm_ov = self.gm_ov / dbu
    # Local variables
    ov_l /= dbu
    ov_r /= dbu
```

```
    vd_vs = self.vd_vs
    bg_ov = metal_ov
    n = n_i
    channel_length = l_i / dbu
    channel_width_per_f = w_i / dbu
    posx = x / dbu
    posy = y / dbu
    round = 1 / dbu
    # Calculations
    via_size = (via + 2 * via_ov)

    Top_Edge = posy + channel_width_per_f / 2 + metal_ov +\
         2 * finger_sep + finger_width + PDN_S_dbu  # Top edge of Cell
    Bottom_Edge = posy -(channel_width_per_f / 2 + metal_ov +\
        2 * finger_sep + finger_width + self.rail * finger_width + PDN_S_dbu) #
Bottom edge of Cell
    VDD_B_E = Top_Edge  # VDD bottom edge
    VDD_T_E = VDD_B_E + (self.rail * finger_width) # VDD top edge
    VSS_B_E = Bottom_Edge # Vss top edge
    VSS_T_E = VSS_B_E + (self.rail * finger_width) # Vss bottom edge

    finger_length = finger_sep + channel_width_per_f + 2 * metal_ov # Correct


    # Create a region for a single finger with the given length and width
    single_finger_region = pya.Region(pya.Box(0, 0, finger_length, finger_width))

    # Move the single finger to the center of the bounding box
    single_finger_region.move(-single_finger_region.bbox().center())
```

```
    # Create an empty region for all fingers
    finger_region = pya.Region()

    # For each finger, create a new region by moving the single finger region horizontally by half the
    # finger separation multiplied by -1 or 1 (depending on the index), and vertically by the finger + channel length
    for i in range(n + 1): # For each finger
        if i % 2 == 1:
            lr = 1
        else:
            lr = -1
        finger_region = finger_region + single_finger_region.moved(
            lr * (finger_sep / 2), (finger_width + channel_length) * i)
    # Centring the fingers
    finger_region.move(-finger_region.bbox().center())

    # Generating region for source backbone using pya.Box function and calculating its position with respect to finger_region bounding box
    source_backbone_region = pya.Region(pya.Box(
            0, 0,
            finger_width,
            (n - n % 2) * (finger_width + channel_length) + finger_width))
    source_backbone_region = source_backbone_region.moved(
            finger_region.bbox().left - finger_width, finger_region.bbox().bottom)

    # Generating region for drain backbone using pya.Box function and calculating its position with respect to finger_region bounding box
    drain_backbone_region = pya.Region(pya.Box(
```

```
            0, 0,
            finger_width,
            (n - 2 + n % 2) * (finger_width + channel_length) + finger_width))
    drain_backbone_region = drain_backbone_region.moved(
            finger_region.bbox().right,
            finger_region.bbox().top - drain_backbone_region.bbox().top\
                - (((n + 1) % 2) * (finger_width + channel_length)))


    source_drain_region = pya.Region()
    source_drain_region = source_drain_region + finger_region
    source_drain_region = source_drain_region + source_backbone_region
    source_drain_region = source_drain_region + drain_backbone_region
    source_drain_region.merge()
    source_drain_region.round_corners(round, round, nr)


    Left_Edge = posx + source_drain_region.bbox().bottom - finger_width #Left edge
of Cell


    if (level == 0):
        rotation = pya.ICplxTrans(float (1), float(90), True, posx, posy)
    else:
        rotation = pya.ICplxTrans(float (1), float(90), False, posx, posy)


    self.cell.shapes(sd).insert(source_drain_region, rotation)


    # Gate - Gate height calculations, Region creation and adding the region to
the "gm" layer
    gate_height = (n) * channel_length + (n + 1) * finger_width + 2 * gm_ov
```

```
    gate_region = pya.Region(pya.Box(
        0,0,channel_width_per_f,gate_height)).round_corners(round, round, nr)

    gate_region.move(-pya.Box(0, 0, channel_width_per_f, gate_height).center()) #
Centre the gate
    self.cell.shapes(gm).insert(gate_region, rotation)


    # Back gate layer
    vbg_cover = pya.Region(pya.Box(
        VDD_B_E,
        gate_region.bbox().bottom - bg_ov,
        VSS_T_E,
        gate_region.bbox().top + bg_ov
        ))


    self.cell.shapes(bm).insert(vbg_cover, rotation)


    # Passivation layer for Transistor
    # Drive transistors
    if load == False:
        # Back gate connection
        VBG_Ele_out = pya.Region(pya.Box(
            posx - vbg_cover.bbox().top, VDD_T_E, posx - vbg_cover.bbox().bottom,
posy)) # Vbg electrode
        self.cell.shapes(bm).insert(VBG_Ele_out)
        if level != 0:
            # If the lower via selected
            if out != 1:
```

```
                PV_Region = pya.Region(pya.Box(
                    gate_region.bbox().left,
                    gate_region.bbox().top,
                    gate_region.bbox().left + via_size,
                    gate_region.bbox().top-via_size
                    )).round_corners(round, round, nr)
                self.cell.shapes(gc).insert(PV_Region, rotation)
                self.cell.shapes(gm).insert(PV_Region, rotation)
                self.cell.shapes(pv).insert(PV_Region.sized(-
via_ov).round_corners(via_size, via_size, nr), rotation)
            # If the upper via selected
            if out != 0:
                PV_Region = pya.Region(pya.Box(
                    gate_region.bbox().right,
                    gate_region.bbox().top,
                    gate_region.bbox().right - via_size,
                    gate_region.bbox().top - via_size
                    )).round_corners(round, round, nr)
                self.cell.shapes(gc).insert(PV_Region, rotation)
                self.cell.shapes(gm).insert(PV_Region, rotation)
                self.cell.shapes(pv).insert(PV_Region.sized(-
via_ov).round_corners(via_size, via_size, nr), rotation)
        # Reversed tarnsistor
        if level == 0:
            # If the lower via selected
            if out != 1:
                PV_Region = pya.Region(pya.Box(
                    gate_region.bbox().left,
                    gate_region.bbox().bottom,
```

```
                    gate_region.bbox().left + via_size,
                    gate_region.bbox().bottom + via_size
                    )).round_corners(round, round, nr)
                self.cell.shapes(gc).insert(PV_Region, rotation)
                self.cell.shapes(gm).insert(PV_Region, rotation)
                self.cell.shapes(pv).insert(PV_Region.sized(-
via_ov).round_corners(via_size, via_size, nr), rotation)
            # If the upper via selected
            if out != 0:
                PV_Region = pya.Region(pya.Box(
                    gate_region.bbox().right,
                    gate_region.bbox().bottom,
                    gate_region.bbox().right - via_size,
                    gate_region.bbox().bottom + via_size
                    )).round_corners(round, round, nr)
                self.cell.shapes(gc).insert(PV_Region, rotation)
                self.cell.shapes(gm).insert(PV_Region, rotation)
                self.cell.shapes(pv).insert(PV_Region.sized(-
via_ov).round_corners(via_size, via_size, nr), rotation)
    # Load transistors
    if load==True:
        if out != 0:
            # Gate via
            PV_Region_gm = pya.Region(pya.Box(
                gate_region.bbox().right,
                gate_region.bbox().top,
                gate_region.bbox().right - via_size,
                gate_region.bbox().top - via_size))
            self.cell.shapes(gc).insert(PV_Region_gm, rotation)
```

```
            self.cell.shapes(gm).insert(PV_Region_gm, rotation)
            self.cell.shapes(pv).insert(
                PV_Region_gm.sized(-via_ov).round_corners(via_size,     via_size,
nr),
                rotation)


            # Back gate via
            PV_Region_bm = PV_Region_gm.move(0, via_size)
            self.cell.shapes(gc).insert(PV_Region_bm, rotation)
            self.cell.shapes(bm).insert(PV_Region_bm, rotation)
            self.cell.shapes(pv).insert(
                PV_Region_bm.sized(-via_ov).round_corners(via_size,     via_size,
nr),
                rotation)


            # Output SD via
            PV_Region_sq_via = PV_Region_bm.move(via_size, finger_width)
            self.cell.shapes(gc).insert(PV_Region_sq_via, rotation)
            self.cell.shapes(sd).insert(PV_Region_sq_via, rotation)
            self.cell.shapes(pv).insert(
                PV_Region_bm.sized(-via_ov).round_corners(via_size,     via_size,
nr),
                rotation)


            # SD to BG via
            sd_gc_via = pya.Region(pya.Box(
                PV_Region_sq_via.bbox().right,
                PV_Region_bm.bbox().top,
```

```
                PV_Region_sq_via.bbox().left - via_size,
                PV_Region_bm.bbox().bottom
                )).round_corners(round, round, nr)
            self.cell.shapes(gc).insert(sd_gc_via, rotation)


            # SD_out
            sd_out = pya.Region(pya.Box(
                posx - channel_length / 2,
                posy + drain_backbone_region.bbox().right,
                posx - sd_gc_via.bbox().top,
                posy + drain_backbone_region.bbox().right - finger_width,
                )).round_corners(round, round, nr)
            self.cell.shapes(sd).insert(sd_out)


            if out == 2:
                PV_Region = pya.Region(pya.Box(
                    gate_region.bbox().left,
                    gate_region.bbox().top,
                    gate_region.bbox().left + via_size,
                    gate_region.bbox().top-via_size
                    )).round_corners(round, round, nr)
                self.cell.shapes(gc).insert(PV_Region, rotation)
                self.cell.shapes(gm).insert(PV_Region, rotation)
                self.cell.shapes(pv).insert(PV_Region.sized(-
via_ov).round_corners(via_size, via_size, nr), rotation)
```

```
    # Vdd and Vss Positions
    if level == 0 or level == 1:
        if level == 1:
            offset = n % 2 * (-1) * (finger_sep + finger_width)
        else:
            offset = 0
        bottom = drain_backbone_region.bbox().bottom + offset
        top = drain_backbone_region.bbox().top + offset
        vdd = pya.Region(pya.Box(posx + top, VDD_B_E - finger_sep - finger_width
- PDN_S_dbu, posx + bottom, VDD_T_E))
        self.cell.shapes(sd).insert(vdd)



    elif level == 3:
        bottom = source_backbone_region.bbox().bottom
        top = source_backbone_region.bbox().top
        vss = pya.Region(pya.Box(posx - bottom, VSS_T_E + finger_sep + finger_width
+ PDN_S_dbu, posx - top, VSS_B_E))
        self.cell.shapes(sd).insert(vss)


    # Define variables
    right_edge = posx + source_drain_region.bbox().top + finger_width # Right edge
of Cell
    if vd_vs is True:
        vdd_box = pya.Box(Left_Edge - ov_l, VDD_B_E, right_edge + ov_r, VDD_T_E)
# VDD rail box
        vss_box = pya.Box(Left_Edge - ov_l, VSS_B_E, right_edge + ov_r, VSS_T_E)
# VSS rail box


        # Create Regions and insert into layout
        vdd_ele = pya.Region(vdd_box) # Create VDD rail region
```

```
        vss_ele = pya.Region(vss_box) # Create VSS rail region

        v_ele = vdd_ele + vss_ele # Add regions together to create combined voltage
regions

        self.cell.shapes(sd).insert(v_ele) # Insert into cell shape in layout


        VBG_Ele = pya.Region(pya.Box(Left_Edge - ov_l, VDD_T_E, right_edge + ov_r,
VDD_T_E + self.rail * finger_width)) # Vgb rail

        self.cell.shapes(bm).insert(VBG_Ele)



        VDDTregion = pya.TextGenerator.default_generator().text\

            ("VDD",   0.001,   2*self.via).move(posx   -   gate_region.bbox().top,
VDD_B_E)

        VSSTregion = pya.TextGenerator.default_generator().text\

            ("VSS",   0.001,   2*self.via).move(posx   -   gate_region.bbox().top,
VSS_B_E)

        Tregion = VDDTregion + VSSTregion

        self.cell.shapes(sd).insert(Tregion)


    # Connection

    # Source/Drain to Gate

    if Int_Con == 1:

        # Lower output

        if out != 1:

            D1_D2 = pya.Polygon([

                pya.Point(posx - vbg_cover.bbox().top,

                    posy - gate_region.bbox().right + via_size),

                pya.Point(posx - vbg_cover.bbox().top,

                    posy + source_backbone_region.bbox().left),

                pya.Point(posx     -     2     *     vbg_cover.bbox().top     -
gate_region.bbox().top,
```

```
                posy + source_backbone_region.bbox().left),
            pya.Point(posx - 2 * vbg_cover.bbox().top -
gate_region.bbox().top,
                posy + source_backbone_region.bbox().left + finger_width),
            pya.Point(posx - vbg_cover.bbox().top - via_size,
                posy + source_backbone_region.bbox().left + finger_width),
            pya.Point(posx - vbg_cover.bbox().top - via_size,
                posy - gate_region.bbox().right + via_size)
            ]).round_corners(round, round, nr)
        self.cell.shapes(sd).insert(D1_D2)

        # Out via connection
        PV_Region_sq = pya.Region(pya.Box(
            posx - vbg_cover.bbox().top,
            posy - gate_region.bbox().right + via_size,
            posx - vbg_cover.bbox().top - via_size,
            posy - gate_region.bbox().right)).round_corners(round, round, nr)
        self.cell.shapes(gc).insert(PV_Region_sq)
        self.cell.shapes(sd).insert(PV_Region_sq)
        self.cell.shapes(pv).insert(
            PV_Region_sq.sized(-via_ov).rounded_corners(via_size, via_size,
nr))

        #Connection
        conn = pya.Region(pya.Box(
            PV_Region_sq.bbox().left,
            posy - gate_region.bbox().right + via_size,
            PV_Region_sq.bbox().left + metal_ov + 2 * via_size,
            posy - gate_region.bbox().right)).round_corners(round, round, nr)
```

```
            self.cell.shapes(gc).insert(conn)
        # Higher output
        if out != 0:
            D1_D2 = pya.Polygon([
                pya.Point(posx - vbg_cover.bbox().top,
                    posy + gate_region.bbox().right - via_size),
                pya.Point(posx - vbg_cover.bbox().top,
                    posy + drain_backbone_region.bbox().right),
                pya.Point(posx - 2 * vbg_cover.bbox().top -
gate_region.bbox().top,
                    posy + drain_backbone_region.bbox().right),
                pya.Point(posx - 2 * vbg_cover.bbox().top -
gate_region.bbox().top,
                    posy + drain_backbone_region.bbox().right - finger_width),
                pya.Point(posx - vbg_cover.bbox().top - via_size,
                    posy + drain_backbone_region.bbox().right - finger_width),
                pya.Point(posx - vbg_cover.bbox().top - via_size,
                    posy + gate_region.bbox().right - via_size)
                ]).round_corners(round, round, nr)
            self.cell.shapes(sd).insert(D1_D2)


            # Out via connection
            PV_Region_sq = pya.Region(pya.Box(
                posx - vbg_cover.bbox().top,
                posy + gate_region.bbox().right - via_size,
                posx - vbg_cover.bbox().top - via_size,
                posy + gate_region.bbox().right)).round_corners(round, round, nr)
            self.cell.shapes(gc).insert(PV_Region_sq)
            self.cell.shapes(sd).insert(PV_Region_sq)
```

```
            self.cell.shapes(pv).insert(
                PV_Region_sq.sized(-via_ov).rounded_corners(via_size,   via_size,
nr))

            #Connection
            conn = pya.Region(pya.Box(
                PV_Region_sq.bbox().left,
                posy + gate_region.bbox().right - via_size,
                PV_Region_sq.bbox().left + metal_ov + 2 * via_size,
                posy + gate_region.bbox().right)).round_corners(round, round, nr)
            self.cell.shapes(gc).insert(conn)


    # Drain to Drain
    if Int_Con == 100:
        D1_D2 = pya.Region(pya.Box(
            posx  + channel_length / 2 + finger_width,
            posy - source_drain_region.bbox().right,
            posx - channel_length / 2 - 2 * vbg_cover.bbox().top - finger_width,
            posy - source_drain_region.bbox().right + finger_width
            )).round_corners(round, round, nr)
        self.cell.shapes(sd).insert(D1_D2)


    # Drain to Source
    if Int_Con == 110:
        # Load
        if load == True:
            D1_D2 = pya.Polygon([
                pya.Point(sd_out.bbox().left,
```

```
                    sd_out.bbox().top),
                pya.Point(posx - PV_Region_gm.bbox().top,
                    posy + source_backbone_region.bbox().left + finger_width),
                pya.Point(posx - PV_Region_gm.bbox().top - vbg_cover.bbox().top -
finger_width - channel_length / 2,
                    posy + source_backbone_region.bbox().left + finger_width),
                pya.Point(posx - PV_Region_gm.bbox().top - vbg_cover.bbox().top -
finger_width - channel_length / 2,
                    posy + source_backbone_region.bbox().left),
                pya.Point(sd_out.bbox().left + finger_width,
                    posy + source_backbone_region.bbox().left),
                pya.Point(sd_out.bbox().left + finger_width,
                    posy + drain_backbone_region.bbox().right)
                ]).round_corners(round, round, nr)
            self.cell.shapes(sd).insert(D1_D2)
        # Drive
        if load == False:
            D1_D2 = pya.Polygon([
                pya.Point(posx - channel_length / 2,
                    posy + drain_backbone_region.bbox().right),
                pya.Point(posx - vbg_cover.bbox().top - finger_width,
                    posy + drain_backbone_region.bbox().right),
                pya.Point(posx - vbg_cover.bbox().top - finger_width,
                    posy + source_backbone_region.bbox().left + finger_width),
                pya.Point(posx - 2 * vbg_cover.bbox().top - 2 * finger_width -
channel_length / 2,
                    posy + source_backbone_region.bbox().left + finger_width),
                pya.Point(posx - 2 * vbg_cover.bbox().top - 2 * finger_width -
channel_length / 2,
                    posy + source_backbone_region.bbox().left),
```

```
                pya.Point(posx - vbg_cover.bbox().top,
                    posy + source_backbone_region.bbox().left),
                pya.Point(posx - vbg_cover.bbox().top,
                    posy + drain_backbone_region.bbox().right - finger_width),
                pya.Point(posx - channel_length / 2,
                    posy + drain_backbone_region.bbox().right - finger_width)
                ]).round_corners(round, round, nr)
            self.cell.shapes(sd).insert(D1_D2)


    # Source to Drain
    if (Int_Con == 101):
        D1_D2 = pya.Polygon([
            pya.Point(posx + channel_length / 2 + finger_width,
                posy + source_backbone_region.bbox().left),
            pya.Point(posx - vbg_cover.bbox().top - finger_width,
                posy + source_backbone_region.bbox().left),
            pya.Point(posx - vbg_cover.bbox().top - finger_width,
                posy + drain_backbone_region.bbox().right - finger_width),
            pya.Point(posx - 2 * vbg_cover.bbox().top - 2 * finger_width -
channel_length / 2,
                posy + drain_backbone_region.bbox().right - finger_width),
            pya.Point(posx - 2 * vbg_cover.bbox().top - 2 * finger_width -
channel_length / 2,
                posy + drain_backbone_region.bbox().right),
            pya.Point(posx - vbg_cover.bbox().top,
                posy + drain_backbone_region.bbox().right),
            pya.Point(posx - vbg_cover.bbox().top,
                posy + source_backbone_region.bbox().left + finger_width),
            pya.Point(posx + channel_length / 2 + finger_width,
```

```
                posy + source_backbone_region.bbox().left + finger_width),
            ]).round_corners(round, round, nr)
        self.cell.shapes(sd).insert(D1_D2)


    #Drain to Drain
    if (Int_Con == 111):
        D1_D2 = pya.Region(pya.Box(
            posx - channel_length / 2,
            posy + drain_backbone_region.bbox().right - finger_width,
            posx - channel_length / 2 - 2 * finger_width - 2 * vbg_cover.bbox().top,
            posy + drain_backbone_region.bbox().right
            )).round_corners(round, round, nr)
        self.cell.shapes(sd).insert(D1_D2)
…
```