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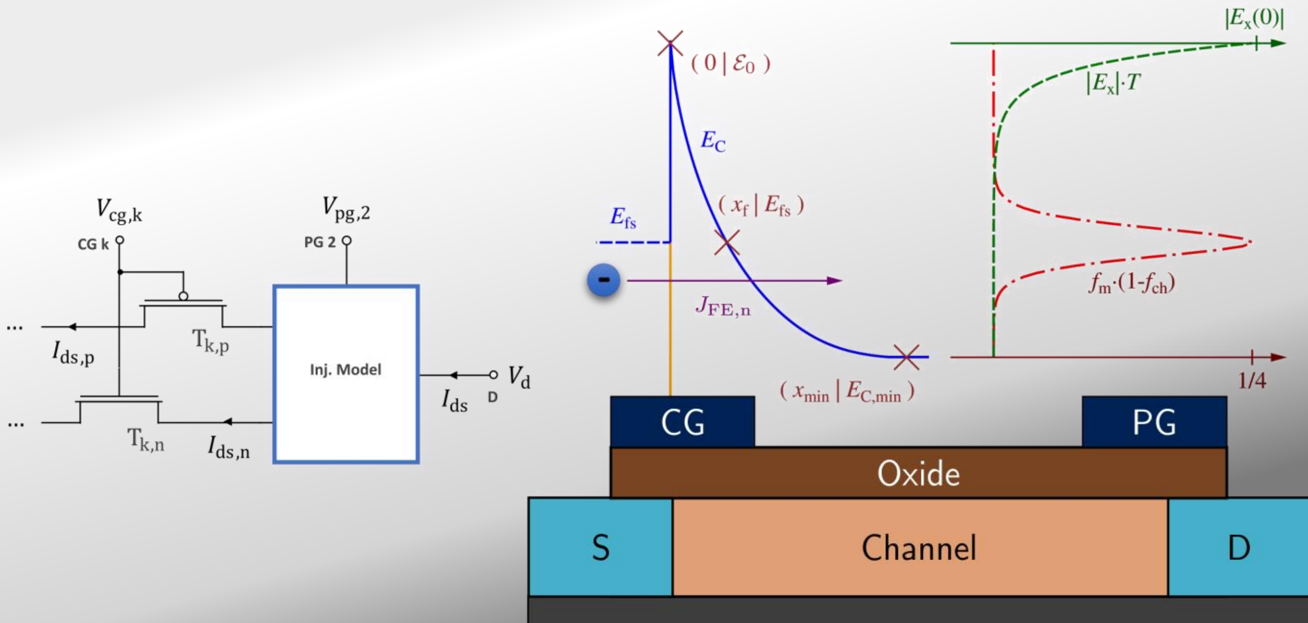
Compact Modeling of Schottky Barrier and Reconfigurable Field-Effect Transistors

CHRISTIAN RÖMER



DOCTORAL THESIS
2024

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Christian Römer

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Compact Modeling of Schottky Barrier and Reconfigurable Field-Effect Transistors

DOCTORAL THESIS

Supervised by Prof. Dr. Benjamín Iñíguez
and Prof. Dr.-Ing. Alexander Kloes

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Abstract

Schottky barrier field-effect transistors (SBFETs) and other devices based on Schottky barrier formation are a stable but also a niche technology in electronic applications. However, SBFETs and other devices based on this technology are still promising for a wide spectrum of future applications. While in recent research SBFETs have been proven to be a good candidate for deep cryogenic temperature applications, new type of devices like the reconfigurable field-effect transistor (RFET) which use and improve several characteristics of SBFETs are currently under investigation. In this work a physics-based and closed-form compact model is derived which is used to calculate the DC current of SBFETs. The presented compact model comes with different variations and can be used for room temperature and for deep cryogenic temperature environmental applications. The model can be applied to regular SBFETs, as well as to programmed RFETs. In addition, the DC compact model includes several second order effects like channel resistance in RFETs and the band tail effect at deep cryogenic temperatures. The model verification is done on measurements of the devices and on numerical TCAD simulations, performed with TCAD Sentaurus.

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List of Publications

Journals

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- Nadine Dersch, Christian Roemer, Eduardo Perez, Christian Wenger, Mike Schwarz, Benjamín Iñíguez and Alexander Kloes "Efficient Simulation of Memristive Crossbar Arrays with Bimodal Stochastic Synaptic Weights," (under review for conference proceedings).

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List of Symbols

Latin Alphabet

Symbol	Description	Unit
a	Coefficient for the tunneling equation	$[\mathrm{eV}^{-2}]$
A^*	Effective Richardson constant	$[\mathrm{A\,cm^{-2}\,K^{-2}}]$
A_0	Amplitude of the wave function	$[-]$
b	Coefficient for the tunneling equation	$[\mathrm{V\,cm^{-1}}]$
B_{PAT}	Phonon-assisted tunneling reduction parameter	$[-]$
c	Coefficient for the tunneling equation	$[\mathrm{eV}^{-1}]$
C_1	Coefficient of the Schwarz Christoffel Transformation	$[-]$
C_2	Coefficient of the Schwarz Christoffel Transformation	$[-]$
C_{NW}	Nanowire circumference	$[\mathrm{nm}]$
C'_{ox}	Oxide capacitance per gate area	$[\mathrm{A\,s\,V^{-1}\,cm^{-2}}]$
$C'_{\mathrm{ox},\kappa}$	Replacement oxide capacitance per gate area for the RFET	$[\mathrm{A\,s\,V^{-1}\,cm^{-2}}]$
$\vec{E}$	Electric field	$[\mathrm{V\,cm^{-1}}]$
$\mathcal{E}_0$	Energy at position $x = 0$	$[\mathrm{eV}]$
E_{C}	Conduction band energy	$[\mathrm{eV}]$
E_{f}	Fermi energy	$[\mathrm{J}]$
E_{fi}	Intrinsic Fermi energy	$[\mathrm{eV}]$
$E_{\mathrm{f,m}}$	Metal's Fermi energy	$[\mathrm{eV}]$
$E_{\mathrm{f,n}}$	Quasi-Fermi energy level for electrons	$[\mathrm{eV}]$
$E_{\mathrm{f,p}}$	Quasi-Fermi energy level for holes	$[\mathrm{eV}]$
E_{fs}	Fermi energy of the source contact	$[\mathrm{eV}]$
E_{g}	Semiconductor's energy band gap	$[\mathrm{eV}]$

$\vec{E}_{\mathrm{img}}$	Image-force induced electric field	[$\mathrm{V\,cm^{-1}}$]
$\mathcal{E}_{\mathrm{max}}$	Upper energy integration boundary	[J]
$\mathcal{E}_{\mathrm{min}}$	Lower energy integration boundary	[J]
$\mathcal{E}$	Energy	[eV]
$\mathcal{E}_{\rho}$	Carriers' longitudinal energy component	[eV]
$\mathcal{E}_{\mathrm{tot}}$	Total carrier energy	[eV]
$\mathcal{E}_{\mathrm{ts,fit}}$	Band tail states distribution fitting parameter	[eV]
$\mathcal{E}_{\mathrm{ts,min}}$	Lower limit of the band tail distribution integral	[eV]
E_{V}	Valence band energy	[eV]
E_{vac}	Vacuum energy level	[eV]
E_{x}	x-component of the electric field	[$\mathrm{V\,cm^{-1}}$]
f	Fermi distribution function or arbitrary function	[−]
f_{ch}	Semiconductor's Fermi distribution function	[−]
f_{m}	Metal's Fermi distribution function	[−]
g_{C3D}	Density of states	[$\mathrm{cm^{-3}}$]
g_{ts}	Band tail states distribution function	[−]
h	Planck constant	[J s]
$\hbar$	Reduced Planck constant	[J s]
i	Imaginary unit	[−]
I_{ds}	Drain-source current	[A]
$I_{\mathrm{ds,inj}}$	Drain-source current calculated by the injection model	[A]
$I_{\mathrm{ds,n}}$	Electron drain-source current contribution	[A]
$I_{\mathrm{ds,p}}$	Hole drain-source current contribution	[A]
$I_{\mathrm{ds,TE,n}}$	Electron thermionic emission drain-source current contribution	[A]
$I_{\mathrm{ds,TE,p}}$	Hole thermionic emission drain-source current contribution	[A]
I_{MOSFET}	Current calculated by the channel MOSFET model	[A]
J_{FE}	Field emission current density	[$\mathrm{A\,cm^{-2}}$]
$J_{\mathrm{FE,d,n}}$	Drain-side injection field emission current density for electrons	[$\mathrm{A\,cm^{-2}}$]
$J_{\mathrm{FE,d,p}}$	Drain-side injection field emission current density for holes	[$\mathrm{A\,cm^{-2}}$]
$J_{\mathrm{FE,n}}$	Field emission current density for electrons	[$\mathrm{A\,cm^{-2}}$]
$J_{\mathrm{FE,n,ts}}$	Current density of the band tail states model	[$\mathrm{A\,cm^{-2}}$]
$J_{\mathrm{FE,p}}$	Field emission current density for holes	[$\mathrm{A\,cm^{-2}}$]
$J_{\mathrm{FE,s,n}}$	Source-side injection field emission current density for electrons	[$\mathrm{A\,cm^{-2}}$]

$J_{\mathrm{FE,s,p}}$	Source-side injection field emission current density for holes	$[\mathrm{A\,cm^{-2}}]$
J_{TE}	Thermionic emission current density	$[\mathrm{A\,cm^{-2}}]$
$J_{\mathrm{TE,d,n}}$	Drain-side injection thermionic emission current density for electrons	$[\mathrm{A\,cm^{-2}}]$
$J_{\mathrm{TE,d,p}}$	Drain-side injection thermionic emission current density for holes	$[\mathrm{A\,cm^{-2}}]$
$J_{\mathrm{TE,n}}$	Thermionic emission current density for electrons	$[\mathrm{A\,cm^{-2}}]$
$J_{\mathrm{TE,p}}$	Thermionic emission current density for holes	$[\mathrm{A\,cm^{-2}}]$
$J_{\mathrm{TE,s,n}}$	Source-side injection thermionic emission current density for electrons	$[\mathrm{A\,cm^{-2}}]$
$J_{\mathrm{TE,s,p}}$	Source-side injection thermionic emission current density for holes	$[\mathrm{A\,cm^{-2}}]$
J_{tun}	Tunneling current density	$[\mathrm{A\,cm^{-2}}]$
$\vec{k}$	Wave vector	$[\mathrm{m^{-1}}]$
k	Wave number	$[\mathrm{m^{-1}}]$
k_{b}	Boltzmann constant	$[\mathrm{J\,K^{-1}}]$
K_{sat}	Saturation constant of the cryogenic saturation model	$[\mathrm{V^{2/3}}]$
L_{CG}	Control gate length	$[\mathrm{nm}]$
L_{ch}	Transistor's channel length	$[\mathrm{nm}]$
L_{ung}	Gate-to-gate distance of the RFET	$[\mathrm{m}]$
L_{PG}	Program gate length	$[\mathrm{nm}]$
m	Carrier / particle mass	$[\mathrm{kg}]$
m^*	Effective carrier mass	$[\mathrm{kg}]$
$m_{\mathrm{n,tun}}$	Electron tunneling mass	$[\mathrm{A}]$
$m_{\mathrm{p,tun}}$	Hole tunneling mass	$[\mathrm{A}]$
m_{n}	Electrons' relative tunneling mass	$[-]$
m_{p}	Holes' relative tunneling mass	$[-]$
N	Supply function	$[-]$
n	Electron concentration	$[\mathrm{cm^{-3}}]$
N_{A}	Doping concentration of acceptors	$[\mathrm{cm^{-3}}]$
N_{C}	Effective density of states in the conduction band	$[\mathrm{cm^{-3}}]$
N_{V}	Effective density of states in the valence band	$[\mathrm{cm^{-3}}]$
$\vec{p}$	Particle's impulse	$[\mathrm{kg\,m\,s^{-1}}]$

$P_{\text{particle in V}}$	Probability of the particle being located inside V	[−]
q	Elementary charge	[A s]
Q'_{d}	Drain-related charge densities per gate area	[A s cm^{-2}]
Q'_{s}	Source-related charge densities per gate area	[A s cm^{-2}]
$\vec{r}$	Position vector	[m]
R_{NW}	Nanowire radius	[nm]
S	Subthreshold swing	[mV/dec]
s_{n}	Electron contribution switching factor of the RFET model	[−]
s_{p}	Hole contribution switching factor of the RFET model	[−]
t	time	[s]
T	Tunneling probability	[−]
t_{box}	Transistor's Substrate thickness	[nm]
t_{ch}	Transistor's channel thickness	[nm]
T_{cryo}	Approximated cryogenic tunneling probability including quantum oscillations	[−]
$T_{\mathrm{cryo,0}}$	Initial approximated cryogenic tunneling probability	[−]
$t_{\mathrm{eff,FE}}$	Effective thickness where the field emission current is flowing	[−]
$t_{\mathrm{eff,TE}}$	Effective thickness where the thermionic emission current is flowing	[−]
T_{NEGF}	Tunneling probability of the non-equilibrium Green's function	[−]
t_{ox}	Oxide layer thickness	[nm]
t'_{ox}	Transformed oxide thickness	[nm]
T_{rect}	Tunneling probability through a rectangular barrier	[−]
T_{ts}	Tunneling probability of the tail states	[−]
t_{tun}	Tunneling thickness	[nm]
T_{WKB}	Tunneling probability of the Wentzel-Kramers-Brillouin approximation	[−]
u	u-coordinate / real part of the w-plane	[m]
U	Energy barrier	[J]
u_{a}	Integration boundary	[m]
u_{b}	Integration boundary	[m]
$u_{\mathrm{s,3}}$	Normalized surface potential	[−]
v	V-coordinate / imaginary part of the w-plane	[m]

V	Voltage	[V]
$V_{0,\mathrm{limit}}$	Limiting voltage parameter of the empirical accumulation charge function	[V]
$V_{\mathrm{b,d}}$	Potential bending from the channel to the drain side contact	[V]
$V_{\mathrm{b,s}}$	Potential bending from the channel to the source side contact	[V]
V_{cg}	Control gate voltage	[V]
V_{d}	Applied drain potential	[V]
V_{ds}	Drain-source voltage	[V]
V_{fb}	Flatband voltage	[V]
V_{g}	Applied gate potential	[V]
V_{gd}	Gate-drain voltage	[V]
$\tilde{V}_{\mathrm{gd,MOS}}$	Averaged gate-drain voltage of the channel MOSFET for RFETs	[V]
V_{gs}	Gate-source voltage	[V]
$V_{\mathrm{gs,bound}}$	Boundary gate-source voltage of the cryogenic saturation model	[V]
$V_{\mathrm{gs,eff,TFET}}$	Effective gate-source voltage of the TFET model	[V]
$\tilde{V}_{\mathrm{gs,MOS}}$	Averaged gate-source voltage of the channel MOSFET for RFETs	[V]
$V_{\mathrm{gs,sat}}$	saturated gate-source voltage of the cryogenic saturation model	[V]
$V_{\mathrm{gs,eff}}$	Effective gate-source voltage	[V]
V'_{gs}	Flatband voltage corrected Gate-source voltage	[V]
V_{limit}	Limiting voltage of the empirical accumulation charge function	[V]
V_{pg}	Program gate voltage	[V]
V_{s}	Applied source potential	[V]
V_{T0}	Threshold voltage of the MOSFET model	[V]
V_{ϑ}	Thermal voltage	[V]
w	Complex w-plane	[m]
W_0	Principal branch of the Lambert W	[−]
W_{ch}	Transistor's channel width	[nm]
w_{i}	Vertex position of vertex i in the w-plane of the Schwarz Christoffel Transformation	[m]
x	Room coordinate in x-direction	[m]
x_{f}	x-position in the channel where $E_{\mathrm{fs}} = E_{\mathrm{C}}$	[m]

y	Room coordinate in y-direction	[m]
z	Room coordinate in z-direction / complex 2D plane	[m]

Greek Alphabet

Symbol	Description	Unit
α	Accumulation charge blending factor	[−]
α_{i}	Vertex angle of vertex i in the w-plane of the Schwarz Christoffel Transformation	[−]
α_{ts}	Band tail states penetration depth parameter	[−]
γ_{MOS}	Smoothing parameter of the channel MOSFET model	[−]
γ_{n}	Fitting parameter for the slope of the electron field emission current	[−]
γ_{p}	Fitting parameter for the slope of the hole field emission current	[−]
γ_{sat}	Smoothing parameter of the cryogenic saturation model	[−]
$\gamma_{\mathrm{Vg,eff}}$	Smoothing parameter of the empirical accumulation charge function	[−]
Δ	Laplace operator	[−]
$\Delta V_{\mathrm{bound}}$	Boundary voltage fitting parameter of the cryogenic saturation model	[V]
ε	Permittivity	[$\mathrm{A\,s\,V^{-1}\,m^{-1}}$]
$\varepsilon_{\mathrm{ox}}$	Oxide permittivity	[$\mathrm{A\,s\,V^{-1}\,m^{-1}}$]
$\varepsilon_{\mathrm{r,ox}}$	Relative oxide permittivity	[−]
$\varepsilon_{\mathrm{r,sc}}$	Relative semiconductor permittivity	[−]
$\varepsilon_{\mathrm{sc}}$	Semiconductor permittivity	[$\mathrm{A\,s\,V^{-1}\,m^{-1}}$]
ϑ	temperature	[K]
κ_{ung}	Ungated channel factor	[−]
λ	Natural length	[nm]
μ	Charge carrier mobility	[$\mathrm{cm^2\,V^{-1}\,s^{-1}}$]
μ_{n}	Electron mobility	[$\mathrm{cm^2\,V^{-1}\,s^{-1}}$]
μ_{tn}	Electron tunneling mobility	[$\mathrm{cm^2\,V^{-1}\,s^{-1}}$]
μ_{p}	Hole mobility	[$\mathrm{cm^2\,V^{-1}\,s^{-1}}$]

μ_{tp}	Hole tunneling mobility	[$\mathrm{cm^2\,V^{-1}\,s^{-1}}$]
ρ	Space charge	[$\mathrm{A\,s\,cm^{-3}}$]
Φ	Potential (in general)	[V]
φ_0	Initial phase for the quantum oscillation model	[−]
Φ_{2D}	Potential calculated by the 2D potential model	[V]
$\Phi_{\mathrm{2D,d}}$	Drain-related potential calculated by the 2D potential model	[V]
$\Phi_{\mathrm{2D,s}}$	Source-related potential calculated by the 2D potential model	[V]
Φ_{bar}	Potential barrier	[V]
Φ_{bi}	Built-in potential	[V]
Φ_{bks}	Backside potential of the quasi 2D potential model	[V]
$\Phi_{\mathrm{B,n}}$	Schottky barrier height for electrons	[V]
Φ_{bnd}	Boundary potential	[V]
$\Phi_{\mathrm{B,n0}}$	Initial Schottky barrier height for electrons	[V]
$\Phi_{\mathrm{B,p}}$	Schottky barrier height for holes	[V]
$\Phi_{\mathrm{B,p0}}$	Initial Schottky barrier height for holes	[V]
Φ_{bs}	Bulk potential of the quasi 2D potential model	[V]
Φ_{cen}	Center potential	[V]
$\Phi_{\mathrm{cen,p}}$	Center potential at position p	[V]
φ_{comp}	Compact potential	[V]
Φ_{const}	Constant potential	[V]
$\Phi_{\mathrm{const,Drain}}$	Constant potential boundary drain	[V]
$\Phi_{\mathrm{const,Gate1}}$	Constant potential boundary gate 1	[V]
$\Phi_{\mathrm{const,Gate2}}$	Constant potential boundary gate 2	[V]
$\Phi_{\mathrm{const,Source}}$	Constant potential boundary source	[V]
Φ_{frs}	Frontside potential of the quasi 2D potential model	[V]
$\Phi_{\mathrm{lin,Oxide1}}$	Linear potential boundary along the oxide 1	[V]
$\Phi_{\mathrm{lin,Oxide2}}$	Linear potential boundary along the oxide 1	[V]
Φ_{m}	Metal's work function	[V]
Φ_{q2D}	Potential calculated by the quasi 2D potential model	[V]
Φ_{sur}	Surface potential	[V]
$\Phi_{\mathrm{sur,p}}$	Surface potential at position p	[V]
$\Phi_{\mathrm{sur,sat}}$	Saturated surface potnential of the cryogenic saturation model	[V]
$\Phi_{\mathrm{sur,bound}}$	Boundary surface potential of the cryogenic saturation model	[V]

χ	Semiconductor's Electron affinity	[V]
Ψ	Wave function	[−]
ψ_{b}	Wave function inside the energy barrier	[−]
ψ_{i}	Incoming wave	[−]
ψ_{r}	Reflected wave	[−]
ψ_{t}	Transmitted wave	[−]
ψ_{I}	Wave function inside region I	[−]
ψ_{II}	Wave function inside region II	[−]
ω	Angular frequency	[s^{-1}]
ω_E	Angular frequency for the quantum oscillation model	[eV^{-1}]

Other

Symbol	**Description**	**Unit**
∇	Nabla operator	[−]
∂	Partial differential operator	[−]

List of Acronyms

Symbol	Description
1D	One-dimensional
2D	Two-dimensional
3D	Three-dimensional
AC	Alternating current
BJT	Bipolar junction transistor
CG	Control gate
CMOS	Complementary metal–oxide–semiconductor
DC	Direct Current
DG	Double gate
DIBL	Drain-induced barrier lowering
FE	Field emission
FEM	Finite element method
FET	Field-effect transistor
GAA	Gate-all-around
IC	Integrated circuit
IP	Intellectual property
MOSFET	Metal–oxide–semiconductor field-effect transistor
NEGF	Non-equilibrium Green's function
NLM	Nonlocal Mesh
PAT	Phonon-assisted tunneling
PG	Program gate / Polarity gate
PhD	Philosophiae Doctor
RFET	Reconfigurable field-effect transistor
SB	Schottky barrier
SBFET	Schottky barrier field-effect transistor

SBL	Schottky barrier lowering
SCE	Short channel effect
SCT	Schwarz Christoffel Transformation
SOI	Silicon-on-insulator
SPICE	Simulation Program with Integrated Circuit Emphasis
TCAD	Technology computer-aided design
TE	Thermionic emission
TFET	Tunnel field-effect transistor
TIG-RFET	Three independent gates reconfigurable field-effect transistor
WKB	Wentzel-Kramers-Brillouin

CHAPTER 1

Introduction

In the year 2023 the transistor celebrated its 75. anniversary. An invention in the field of electronics that impacted economy, society, and research. The transistor has probably been one of the most impactful inventions since today, as it is part of nearly every electronic device like computers, smartphones, TVs and much more. The first transistor was a bipolar point-contact transistor invented by *John Bardeen*, *Walter Brattain*, and *William Shockley* in 1947 at the Bell Telephone Laboratories. This transistor type was improved to the bipolar junction transistor (BJT) in the following year, which quickly became state-of-the-art in the field of electronics. While the BJT technology still has its fields of application, especially in digital circuits it has been mainly replaced by the complementary metal–oxide–semiconductor (CMOS) technology, coming up in the 1960s. This CMOS technology consists of p-type and n-type field-effect transistors (FETs), mostly metal–oxide–semiconductor field-effect transistors (MOSFETs) with symmetric characteristics. In this technology, p- and n-type MOSFETs are integrated into small chips to build up logical functions (e.g. "NOT", "NAND" or "NOR"). While the transistor in general started as a single electronic device, today's electronic hardware components can have billions of FETs integrated in a single chip.

1.1 Metal–Oxide–Semiconductor Field-Effect Transistor Technology

The FET technology goes back to *Julius Edgar Lilienfeld* who patented the first FET in [1]. The main FET technology used for decades in the history of electronics was the MOSFET, which consists of a doped semiconductor (usually silicon) bulk, a metallic gate electrode and an oxide that isolates the semiconductor from the metallic gate. The source and drain contacts are attached to reversely-doped semiconductor regions, which are located at the opposing fringes of the bulk. A schematic MOSFET structure is shown in Fig. 1.1. The doping profile at the source-bulk-drain regions determines the type of MOSFET. An n-p-n doping profile leads to an n-type MOSFET which conducts a positive drain current I_{ds} in case of positive gate-source

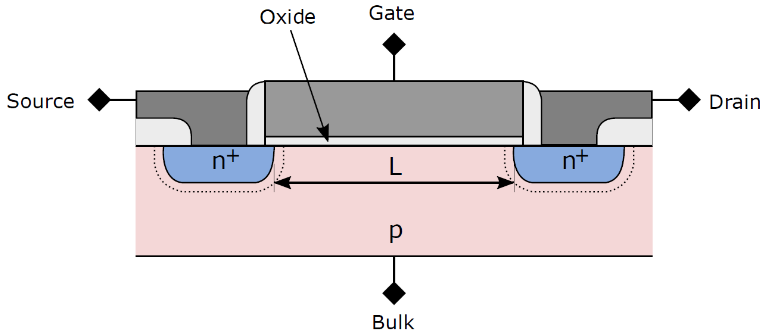

Figure 1.1: Schematic slice of a MOSFET. The dark gray sections are metallic contacts, and the light gray sections are isolating parts. The bulk (red) consists of a p-type semiconductor in this case, which is attached to the n-type semiconductor regions at the source and drain contacts (blue), making this device an n-type MOSFET. The figure is taken from [2].

V_{gs} and drain-source V_{ds} voltages. A p-n-p doping profile leads to a p-type MOSFET which conducts a negative drain current I_{ds} in case of negative gate-source V_{gs} and drain-source V_{ds} voltages [2].

Since the invention of the MOSFET, its further development of shrinking a single device's geometries and its power consumption in order to increase the integration density has been mainly determined by improving fabrication methods [2, 3].

In 1965 *Gordon Moore* (co-founder of Intel Corporation) predicted a doubling of the number of FETs (or more general 'components') that can be integrated on the same size of chip every two years [4]. As his prediction has shown to be very accurate, this statement - "Moore's Law" - became famous and is still omnipresent in today's technological discussions about FETs. During this era of microelectronics, the main idea was to scale down the MOSFET's geometries (channel length, channel width and oxide thickness), as well as the supply voltage, leading to reduced feature sizes and power consumption.

1.2 Transition from Microelectronics to Nanoelectronics

The down-scaling effectiveness of the MOSFET geometries gradually became more inefficient by the time feature sizes approached nanometer scale. While shrinking down geometries further in the scale of nanometers, short channel effects (SCEs) are appearing and getting more dominant. Those SCEs are mainly caused by quantum mechanical effects. Especially, the quantum mechanical tunnel effect (see Sec. 2.3) causes leakage currents in device operation modes at which a device should be switched off, leading to an increased power usage of circuits. Another SCE that can appear in short-channel device's is the so-called drain-induced barrier lowering (DIBL) effect. This effect appears in case the electrostatic coupling of the drain on

the potential in the center of the transistor's channel cannot be neglected any more. In this case the MOSFET's threshold voltage changes with the drain voltage, leading to a reduced gate control of the device [2, 5, 6].

The field or era of electronics which are impacted by SCE's is called nanoelectronics. In the era of nanoelectronics, the scaling rules used in microelectronics can no longer be used to improve the transistors characteristics. New technologies had to emerge instead. Some technologies, like the already established FinFET technology, shall counter out the SCE's by increasing the electrostatic gate coupling on the transistors channel. Other technologies try to abuse the quantum mechanical effects appearing in the field of nanoelectronics, like the tunnel field-effect transistor (TFET) [2].

The field of nanoelectronics, including the challenge of scaling down device's or coming up with new technologies, still is a global research field and important for future electronic applications.

1.3 Schottky Junctions and Devices Based on Them

This work focuses on several types of transistors that are based on Schottky barriers (SBs), named after *Walter Hans Schottky*. SBs are energy / potential barriers for charge carriers that can lead to similar current blocking mechanisms as pn-junctions of MOSFETs. Those SBs form at metal-semiconductor junctions (Schottky junctions). While SBs can potentially lead to unwanted parasitic resistances in semiconductor devices in case they are not considered properly, their mechanisms are particularly abused for example in Schottky diodes [2]. Their formation and physical description are explained in Sec. 2.4.

There are some devices based on SBs that can act as good candidates for replacing MOSFETs in certain fields of application. This device family, which is also the main topic of this work, are transistors based on charge transport over SBs. Unlike in MOSFET application, where a device's current blocking and letting pass mechanisms are determined by doped regions and the resulting pn-junctions and potential barrier in the transistor's channel, in SB devices these mechanisms are mainly given by Schottky junctions between metal and semiconductor regions leading to the formation of SBs [2].

The simplest electronic device abusing the effects of the SB formation is the Schottky diode, which consists of a single metal-semiconductor junction. The Schottky diode works similar to a pn-diode, but compared to pn-diodes, the Schottky diode supports higher operation frequencies and works at higher power [2, 7]. Beside the Schottky diode, which is a metal-semiconductor junction based diode structure, there are several transistor types that are based on SBs. The two most important types for this work are introduced in the following sections.

1.3.1 Schottky Barrier Field-Effect Transistor

A basic transistor type that is based on SBs is the SBFET (Schottky barrier field-effect transistor or also often referred to as SB-MOSFET). Compared to a regular MOSFET, in this device the source and drain regions consist of metal, while the channel / bulk region is still made of semiconductor but does not necessarily need to be doped. This material combination leads to the formation of SBs at the source-channel and drain-channel interfaces which lead to the current control mechanism, instead of the pn-junctions in regular MOSFETs [2, 6]. A more detailed physical description of SBFETs is given in Chapter 3.

Since SBFETs are usually outperformed by other transistor types, their field of application is more restricted. However, in emerging technologies those kinds of transistors are promising candidates for new fields of application. In several modern technical applications (e.g. quantum computing, superconductor, biomedical applications) a deep cryogenic temperature environment of only a few kelvins is necessary, where the SBFET has been proposed as good candidate for electronic applications in this environment [8–11]. At cryogenic temperatures, the SBFET benefits from a leakage / off-current reduction, due to the reduced thermal energy, which improves the device's subthreshold behavior [9, 11]. Additionally, compared to regular MOSFET application, the SBFET does not rely on doping and is not affected by dopant freeze-out effects.

There are several other devices and applications based on the SBFET technology [7]. For example, there are reported SBFETs rearranged as source-gated transistors, that are based on organic materials reported in [12, 13]. SBFETs or SB devices based on 2D channel materials are shown for example in [14–16]. The principle of ferroelectric SBFETs with a memory effect, possibly used in neuromorphic computing application is demonstrated in [17, 18]. Although these devices and technologies are not directly covered by the modeling approach of this work, the introduced compact model still might be a good basis for further extension.

1.3.2 Reconfigurable Field-Effect Transistor

Another field of application, where the SBFET is used as a basis, is the reconfigurable field-effect transistor (RFET), which is also covered by this work. RFETs are usually based on SBFETs and exist in several variations [19]. These transistors have at least one additional gate which is used to change the device's polarity during runtime, so the transistor can switch between p-type and n-type device behavior. Although RFETs have a bigger device footprint due to the additional gate compared to SBFETs, the goal of using RFETs is to increase the functionality of a single device and therefore, reduce the complexity of the electronic circuit [19–22]. In [21, 22] it is shown that RFETs can be used in order to create reconfigurable logic circuits that can change their functionality, in the given example from NAND to NOR logic by using four RFETs. Dependent on the application, the usage of RFETs can potentially reduce the logical effort of circuits and increase their performance [21, 22]. Another discussed use case

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scenario of RFETs is the hardware security application for protecting intellectual properties (IPs), by using RFETs for logic locking mechanisms [23–25]. A more detailed introduction of the RFET's working principle is given in Chapter 3.

1.4 Simulation and Modeling

Modern integrated circuits (ICs) may consist of more than thousands of electronic components (transistors, resistors, capacitors, etc.) which need to work properly, so the IC can fulfill its purpose. Therefore, even before production a proper planning of the IC must be done. In modern days such planning processes cannot be done on test boards anymore, due to the number of devices and the different physical effects in highly integrated circuits. That is why hardware planning and testing is done theoretically and computer-aided with the help of various models that are capable of describing the hardware behavior. There are different variations and levels of such mathematical models. In this work, a compact model for the SBFET devices is mathematically derived, which is a device-level model, because it describes the characteristics of a single device. Such a device model can be used to simulate an entire circuit, by creating a circuit-level model. This can be done by using a circuit simulator, like SPICE (Simulation Program with Integrated Circuit Emphasis), to simulate the entire circuit numerically. There are various electrical properties of devices that can be modeled and simulated. The model that is derived in this work focuses on the direct current (DC) behavior of the investigated transistors, so the steady-state device current dependents on the applied voltages. Additional properties that can be investigate are for example the alternating current (AC) or the noise behavior of such devices [26, 27].

In order to understand the physics behind certain electronic devices and to create compact device level models, simulations on that level can be performed. In this work device-level simulations of SB devices are performed and shown which are done using the technology computer-aided design (TCAD) software TCAD Sentaurus (Synopsys, Inc.). This simulator uses the finite element method (FEM) to solve numerical equation inside electronic devices to calculate relevant variables (e.g. charges, potentials, and currents) [28].

1.5 Compact Modeling

The aim of this work is to provide a compact model for SBFETs and RFETs that is physics based and mathematically solvable in closed form. Physics based relates to the origin of the model equations being as close as possible to real device physics. This physics-based approach shall make the compact model scalable with device parameters, like the geometries for example, since a physics-based model is supposed to consider the impact of the device parameters on its characteristics. Additionally, often physics-based models can be also extended or adapted to include other physical effects (e.g. adapting silicon-based models to organic transistors or

include short channel effects into MOSFET equations), and they fulfill an academia aspiration. In contrast to the physics-based model, there are other model variants like a table model which uses measured or simulated device characteristics as a base, requiring a lot of data for accurate device behavior predictions. There is also the empirical model that uses empirical mathematical equations which match the device's characteristics, but don't have physical parameters or relations. Empirical model often come with several fitting parameters for the model to be fitted to measured data. It shall be mentioned that the presented compact model of this work also uses smoothing functions and fitting parameters at some positions, since several physical equations cannot be solved in closed form.

A closed-form model relates to the model equation being mathematically solvable in closed form. This leads to a set of equations which can successively be used for calculating a bias point of the device. In contrast to the closed-form model is the numerical model (for example TCAD simulations) using basic physical relations, which do not need to be solved analytically or simplified and solves them with numeric methods. These models can be more precise in their results (depending on their configuration) and can be more easily extended with other physical relations. However, since they are using numerical methods for solving, they take a much higher effort for the calculation and therefore, much more time consumption to calculate a single bias point, making them nearly impossible to use for the simulation of bigger circuits. Due to the numerical methods, in some cases it can also happen that the numerical model is not converging and does not lead to a conclusion at all.

1.6 Outline of This Work

This document focuses on the physics-based compact modeling of SBFETs and RFETs considering the main DC injection current over the devices' SBs, as well as some second order effects of the devices, which can appear in some circumstances.

For the better understanding of the physical background of the investigated devices and the discussed compact modeling approaches, Chap. 2 briefly summarizes the basic physical effects and models, like the tunnel effect and thermionic emission model. Additionally, some basic models that are used in later chapters are summarized, like the used potential models or a current transport model in MOSFETs.

Chapter 3 explicitly explains the structure, working principle and the characteristics of the SBFETs and RFETs which are under investigation in this work, underpinned by simulation results performed with TCAD Sentaurus. In this chapter there is also a discussion about the device variation and the state-of-the-art in compact modeling of those devices.

The compact modeling approaches are separated into three chapters, each covering a different variation of the model. Chap. 4 explains the derivation of the physics-based compact model, used for the DC injection current of SBFETs in room temperature environment. This

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chapter also presents the inclusion of additional effects like the SBFET's drain-side SB and the channel resistance of long channel devices. The compact model is validated using TCAD simulation results.

While the first part of the compact modeling approach focuses on SBFETs at room temperature, the second major part of the compact model, described in Chap. 5, explicitly derives an injection current model for SBFETs at deep cryogenic temperatures (for $\vartheta \approx 0\,\mathrm{K}$). Here, the changes to the room temperature model are discussed and some second order effects that are appearing at this temperature environment are mentioned and included into the model. The compact model results are validated using measurements which are performed at about 4...6 K.

The last modeling chapter - Chap. 6 - uses the room temperature model for the SBFETs and translates the model for the usage as a RFET compact model. In this chapter, the model usage to describe the characteristics of programmed RFETs is shown. In addition, the inclusion of a second gate and the inclusion of long channel / ungated channel effects are described. This part of the model is also verified using measurements and TCAD simulation results.

Finally, Chap. 7 concludes this work by summarizing the field of application and status of the described compact model and shows some possibilities for future extensions of the model.

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CHAPTER 2

Physical Effects and Basic Models

The compact modeling approaches shown in this work are all physics-based and rely on basic mathematical and physical models. This chapter aims to introduce the important physical effects, as well as the basic models that are used or strongly related to the compact models of the main modeling chapters.

This chapter starts with the introduction of two potential models in Sec. 2.1, based on either Poisson's or Laplace equation. Section 2.2 covers basic transport mechanisms in field-effect transistors and shows a closed-form compact model for those. Section 2.3 explains the basics of the quantum mechanical tunneling effect and derives some equations to calculate tunnel current densities. Finally, Sec. 2.4 explains the formation and physical effects coming to the fore at SBs.

2.1 Potential Model

In the physics of semiconductor, or rather in electronics in general, the physical parameters like voltages V, currents I, charges q, etc. are all related to each other. This relation is often given by differential equations. In contrast to this, for a compact model it is desired to have simple and analytically solvable equations. It is a common practice to divide one mathematical problem into minor parts that are easier manageable. For example, there are many compact modeling approaches for various transistor types that calculate a closed-form potential Φ inside of a transistor in a first step (for example [29–32]). This closed-form potential is then used in order to calculate other physical parameters, for example the DC drain current I_{ds}, without any recursions (V_{gs},$V_{\mathrm{ds}} \rightarrow \Phi \rightarrow \ldots \rightarrow I_{\mathrm{ds}}$).

The described compact model of this work is also based on potential models. This section describes the basics of the used potential models, starting with the fundamental Poisson's and Laplace equation in Sec. 2.1.1. There are two potential models that are used in different

model extensions and which are introduced in this section, where the first one is a 1D potential model described in Sec. 2.1.2. The second potential model is based on the conformal mapping technique where its working principle is explained in Sec. 2.1.3, followed up by a special conformal mapping method that is called Schwarz Christoffel transformation in Sec. 2.1.4. Finally, a closed-form 2D potential model from [31–33] is introduced in Sec. 2.1.5 and an addition for considering accumulated charges in the channel is presented in Sec. 2.1.6.

2.1.1 Poisson's and Laplace Equation

One of the fundamental equations of the electrostatics is the Poisson equation which is given by:

$$\Delta\Phi(\vec{r}) = -\frac{\rho(\vec{r})}{\varepsilon}, \tag{2.1}$$

and describes the relation between the electrostatic potential $\Phi(\vec{r})$ and the space charge $\rho(\vec{r})$, both dependent on the position vector $\vec{r}$. In a 3D system the position vector can be represented by its three room coordinates $\vec{r} = (x,y,z)$. In Eq. (2.1), the parameter ε is the material's permittivity and Δ is the so-called Laplace operator, which in case of 3D system and applied to an arbitrary function $f(\vec{r})$, is defined as:

$$\Delta f(\vec{r}) = \frac{\partial^2}{\partial x^2} f(x,y,z) + \frac{\partial^2}{\partial y^2} f(x,y,z) + \frac{\partial^2}{\partial z^2} f(x,y,z). \tag{2.2}$$

In case the Poisson equation is applied to a space charge free room ($\rho = 0$), Eq. (2.1) can be simplified into:

$$\Delta\Phi(\vec{r}) = 0, \tag{2.3}$$

which is called Laplace equation (not to be confused with the Laplace operator).

Additionally, the electric field inside a region is defined as:

$$\vec{E}(\vec{r}) = -\nabla\Phi(\vec{r}) = -\begin{pmatrix} \frac{\partial}{\partial x} \\ \frac{\partial}{\partial y} \\ \frac{\partial}{\partial z} \end{pmatrix} \Phi(x,y,z), \tag{2.4}$$

where ∇ is the nabla operator, defined as the derivation of the scalar field Φ to all three room coordinates.

All equations, Eq. (2.1), Eq. (2.3), and Eq. (2.4) are essential for calculating the electrostatic Potential or the electric field inside semiconductor devices and are used in upcoming sections.

2.1.2 Closed-Form Analytical 1D Potential

This firstly described potential model is a 1D / quasi 2D potential model which is summarized from the work of [34, 35]. This approach is done for 2D structures, like shown in Fig. 2.1 and uses the Poisson equation Eq. (2.1) for two dimensions. However, it neglects accumulated charge carriers and uses the doping concentration N_A (acceptors in this case) only as space charge, which results in:

$$\Delta\Phi_\mathrm{q2D}(x,y) = \frac{\partial^2}{\partial x^2}\Phi_\mathrm{q2D}(x,y) + \frac{\partial^2}{\partial y^2}\Phi_\mathrm{q2D}(x,y) = \frac{qN_\mathrm{A}}{\varepsilon_\mathrm{sc}}. \tag{2.5}$$

It uses a parabolic approximation of the potential in the y-direction (bulk-gate direction),

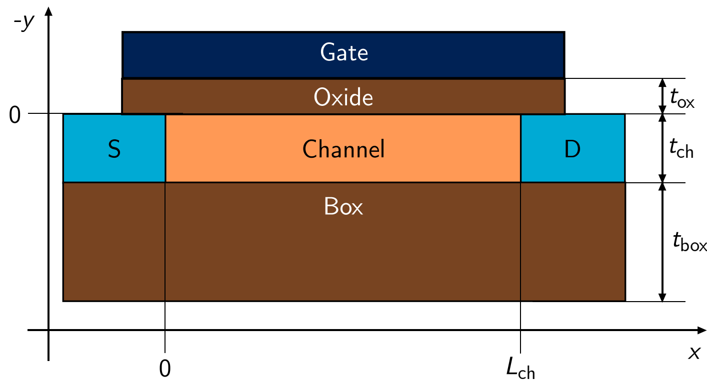

Figure 2.1: Primary transistor structure where the 1D potential model is derived for [34].

given by:

$$\Phi_\mathrm{q2D}(x,y) \approx c_0(x) + c_1(x)\cdot y + c_2(x)\cdot y^2, \tag{2.6}$$

where c_i are functions that are only x dependent. Additional assumptions are made for the boundary conditions in the derivation, given as the front-side (oxide-semiconductor interface) potential Φ_frs at $y = 0$:

$$\Phi_\mathrm{q2D}(x,0) = \Phi_\mathrm{frs}(x) = c_0(x), \tag{2.7}$$

the electric field at $y = 0$ which is determined by the gate-source voltage $V'_\mathrm{gs} = V_\mathrm{gs} - V_\mathrm{fb}$:

$$\frac{\partial}{\partial y}\Phi_\mathrm{q2D}(x,y)\bigg|_{y=0} = \frac{\varepsilon_\mathrm{ox}}{\varepsilon_\mathrm{sc}}\cdot\frac{\Phi_\mathrm{frs}(x) - V'_\mathrm{gs}}{t_\mathrm{ox}} = c_1(x), \tag{2.8}$$

and the electric field at the bottom of the bulk:

$$\frac{\partial}{\partial y}\Phi_\mathrm{q2D}(x,y)\bigg|_{y=t_\mathrm{sc}} = \frac{\varepsilon_\mathrm{ox}}{\varepsilon_\mathrm{sc}}\cdot\frac{\Phi_\mathrm{bs} - \Phi_\mathrm{bks}(x)}{t_\mathrm{box}} = c_1(x) + 2t_\mathrm{ch}\cdot c_2(x) \approx 0, \tag{2.9}$$

with Φ_{bks} as the backside (buried oxide-semiconductor interface) potential, Φ_{bs} as the bulk potential, and t_{box} as the oxide layer thickness. As a simplification, the bulk is supposed to be floating so that Eq. (2.9) is set to zero. Using the Eq. (2.7), Eq. (2.8), and Eq. (2.9) with Eq. (2.6) and Eq. (2.5) leads to:

$$\Phi_{\mathrm{q2D}}(x) = \Phi_{\mathrm{frs}}(x) - V'_{\mathrm{gs}} + \frac{qN_{\mathrm{A}}}{\varepsilon_{\mathrm{sc}}} \cdot \lambda^2, \tag{2.10}$$

and:

$$\frac{\partial^2}{\partial x^2}\Phi_{\mathrm{q2D}}(x) - \frac{1}{\lambda^2} \cdot \Phi_{\mathrm{q2D}}(x) = 0, \tag{2.11}$$

with:

$$\lambda = \sqrt{\frac{\varepsilon_{\mathrm{sc}}}{\varepsilon_{\mathrm{ox}}} \cdot t_{\mathrm{ox}} t_{\mathrm{ch}}}. \tag{2.12}$$

The parameter λ is called natural length and depends on the device's structure. Equation (2.12) is an expression for a bulk MOSFET.

By using two additional boundary conditions for $x = 0$ and $x = L_{\mathrm{ch}}$, as:

$$\Phi_{\mathrm{q2D}}(0) = V_{\mathrm{s}} = \Phi_{\mathrm{bi}} - V'_{\mathrm{gs}} + \frac{qN_{\mathrm{A}}}{\varepsilon_{\mathrm{sc}}} \cdot \lambda^2, \tag{2.13}$$

and:

$$\Phi_{\mathrm{q2D}}(L_{\mathrm{ch}}) = V_{\mathrm{d}} = V_{\mathrm{ds}} + \Phi_{\mathrm{bi}} - V'_{\mathrm{gs}} + \frac{qN_{\mathrm{A}}}{\varepsilon_{\mathrm{sc}}} \cdot \lambda^2. \tag{2.14}$$

The boundary conditions use either the applied source V_{s} or drain voltage V_{d}. The device's built-in potential Φ_{bi}, used in the equations, is caused by source-channel or drain-channel material junction, and is explained in Sec. 2.4.1 for SBFETs. Using these conditions Eq. (2.13) and Eq. (2.14) with Eq. (2.11), solves to the final equation:

$$\Phi_{\mathrm{q2D}}(x) = V'_{\mathrm{gs}} + \frac{V_{\mathrm{b,s}} \cdot p(L_{\mathrm{ch}} - x) + V_{\mathrm{b,d}} \cdot p(x)}{p(L_{\mathrm{ch}})}\,, \tag{2.15}$$

with:

$$p(x') = \exp\left(\frac{x'}{\lambda}\right) - \exp\left(-\frac{x'}{\lambda}\right)\,, \tag{2.16}$$

and the source / drain potential bending $V_{\mathrm{b,s/d}} = \Phi_{\mathrm{bi}} - V'_{\mathrm{gs}} + V_{\mathrm{s/d}}$. Besides the natural length given by Eq. (2.12), there are additional λ for other device structures. For example, [34] presents a solution for the natural length of a gate-all-around (GAA) structure, given as:

$$\lambda = \sqrt{\frac{\varepsilon_{\mathrm{sc}}}{2\varepsilon_{\mathrm{ox}}} \cdot t_{\mathrm{ox}} \cdot 2R_{\mathrm{NW}}}. \tag{2.17}$$

The solution $\Phi_{\mathrm{q2D}}(x)$ of Eq. (2.15) is used in Chapter 5. A more detailed derivation of this potential model can be found in [34].

2.1.3 Conformal Mapping

There are various well-known solutions for electrostatic problems which can be applied on simplified or symmetric problems, like a plated capacitor, point charges in a room, or a very long cylindrical cable. However, in most applications the problem that has to be solved is not symmetrical and takes more effort to solve (in case it is analytically solvable at all). Figure 2.2 shows a schematic cross-section of a double gate (DG) transistor with three different potentials at the device's boundaries.

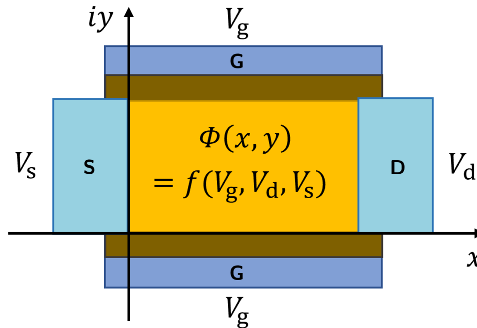

Figure 2.2: DG transistor structure represented in a complex plane, showing the applied bias potentials at the boundaries. The electrostatic potential inside the device is a function of the geometry and all applied bias potentials.

The shown problem is partially symmetric but solving it in a closed-form expression is still challenging. In order to solve a (full) 2D electrostatic potential ($\Phi_{\mathrm{2D}}(x,y)$) within such a device, the conformal mapping method can be used [36, 37]. In this method, the axes of a 2D problem (e.g. the transistor from Fig. 2.2) are represented in a complex plane, called the z-plane, with $z = x + iy$, where i is the imaginary unit [36]. The goal of the conformal mapping method is to find another complex 2D plane, the w-plane with $w = u + iv$, at which the mathematical problem is solvable, as well as a transformation method f, with $f(z) = w$ [36].

2.1.4 Schwarz Christoffel Transformation

A special conformal mapping method has been worked on by *Schwarz* [38] and *Christoffel* [39, 40], which is often referred to as Schwarz Christoffel Transformation (SCT) and summarized in [36]. The SCT is a systematic transformation method which is used to map the inside region of a polygon described in a 2D plane $z = x + iy$ to the upper half of a $w = u + iv$ plane. Therefore, the outer edges of the polygon, traversed counterclockwise, are "opened up" on the u-axis of the z-plane. An example illustration is shown in Fig. 2.3. The SCT is mathematically

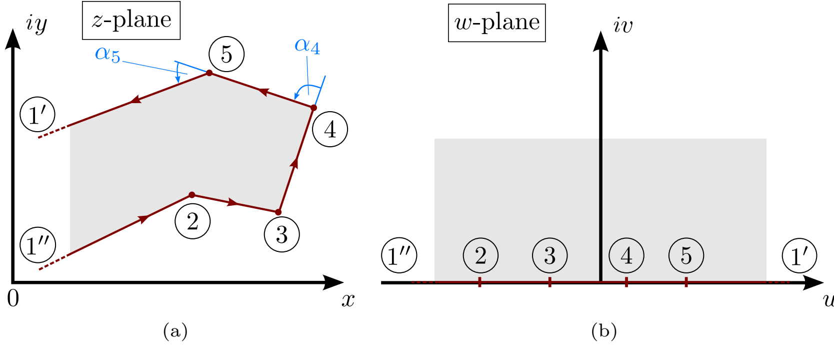

Figure 2.3: Example of a polygon, which is opened to the left side, (a) represented in the complex z-plane and (b) transformed on the u-axis of the complex w-plane. The images are taken from [33].

described by

$$z = f(w) = C_1 \cdot \int \prod_{i=1}^{n} (w - w_\mathrm{i})^{-\frac{\alpha_i}{\pi}}\, dw + C_2. \tag{2.18}$$

In Eq. (2.18), every vertex of the z-plane polygon is represented by one factor, where n is the number of vertices. The coefficient w_i is the position of the vertices on the w-plane, α_i is the corresponding counterclockwise angle change. The coefficient C_2 is the offset of the z-plane and in case that the mapped polygon has two parallel edges which start / end at ∞ (see Fig. 2.3), C_1 can be expressed as:

$$C_1 = \frac{z''_\mathrm{k} - z'_\mathrm{k}}{i\pi}, \tag{2.19}$$

which is an important special case.

The SCT is used in the 2D potential model described in the upcoming section. An in-depth investigation of the SCT and the conformal mapping method is beyond the scope of this work. The author would kindly ask to refer to [36] for a more extensive view on this topic.

2.1.5 Closed-Form Analytical 2D Potential

This section briefly summarizes the closed-form 2D potential from [29, 33, 41, 42] by using the theory from Sec. 2.1.1, Sec. 2.1.3, and Sec. 2.1.4 as basis. A more detailed model derivation can be found in the mentioned references. The potential model presented in this section is derived for 2D DG device structures, as shown in Fig. 2.4(a), although a derivation for other structures (e.g. single gate devices) would be possible as well. It calculates a 2D potential $\Phi_{\mathrm{2D}}(x,y)$ inside the device's channel region (including the gate oxide regions), dependent on the coordinates x and y. The coordinate x is the source-to-drain direction, with $x = 0$ as source-channel junction and $x = L_{\mathrm{ch}}$ as drain-channel junction and y is the gate-to-gate direction, with $y = 0$ at one

gate to $y = t_{\mathrm{ch}}$ at the opposing gate. The algorithm for obtaining Φ_{2D} can be divided into four different steps which are explained one by one.

In a first step, the DG device is split up in the middle of the channel (at $x = L_{\mathrm{ch}}/2$), which results in two partial devices - the source side and the drain side. This is represented in Fig. 2.4(a). Both partial devices have a fixed starting point on the x-axis and for the calculation they are supposed to have an infinite length in the opposing x direction. This step, which is a good approximation in case of $L_{\mathrm{ch}} \gg t_{\mathrm{ch}}$, leads to a reduction of the calculations complexity when applying the SCT in a later step, because instead of an enclosed polygon with four corners (four-corner problem), the mathematical problem is split up into two polygons with two corners and open in one direction (two-corner problem). The upcoming two steps are solved for each partial device individually.

The second step is the equalization of the oxide's permittivity, which means that the permittivity for the oxide $\varepsilon_{\mathrm{ox}}$ is equalized to the semiconductor's permittivity $\varepsilon_{\mathrm{sc}}$. This is done by calculating a transformed oxide thickness t'_{ox} by:

$$t'_{\mathrm{ox}} = \frac{\varepsilon_{\mathrm{sc}}}{\varepsilon_{\mathrm{ox}}} \cdot t_{\mathrm{ox}}, \tag{2.20}$$

which is illustrated in Fig. 2.4(b). This equalization leads to a uniform distribution of the electric field and therefore, the electrostatic potential inside the device and prevents the necessity of a further device split up into oxide and channel regions.

In the third step, the SCT from Sec. 2.1.4 is applied, which is illustrated in Fig. 2.4(c). In this special case of the two-corner device structure, as shown in Fig. 2.4(c), the SCT Eq. (2.18) and Eq. (2.19) become:

$$z(w) = \frac{\Delta y}{\pi} \cosh^{-1}(w) = \frac{2t'_{\mathrm{ox}} + t_{\mathrm{ch}}}{\pi} \cosh^{-1}(w), \tag{2.21}$$

where Δy is the distance of the two horizontal edges. Translated to the DG transistor it can be represented by $\Delta y = 2t'_{\mathrm{ox}} + t_{\mathrm{ch}}$. By reversing the transformation of Eq. (2.21) as

$$w(z) = f^{-1}(z) = \cosh\left(\frac{\pi(x + iy)}{2t'_{\mathrm{ox}} + t_{\mathrm{ch}}}\right), \tag{2.22}$$

an expression for the given two-corner problem for an arbitrary point which is at $(x|y)$ inside the channel ($t_{\mathrm{ox}} \leq y \leq t_{\mathrm{ox}} + t_{\mathrm{ch}}$) can be stated as:

$$w_{\mathrm{s}}(x,y) = \cosh\left(\frac{\pi(x + iy)}{2t'_{\mathrm{ox}} + t_{\mathrm{ch}}}\right), \tag{2.23}$$

in the corresponding w-plane of the source-side transformation, and:

$$w_{\mathrm{d}}(x,y) = \cosh\left(\frac{\pi(L_{\mathrm{ch}} - x + iy)}{2t'_{\mathrm{ox}} + t_{\mathrm{ch}}}\right), \tag{2.24}$$

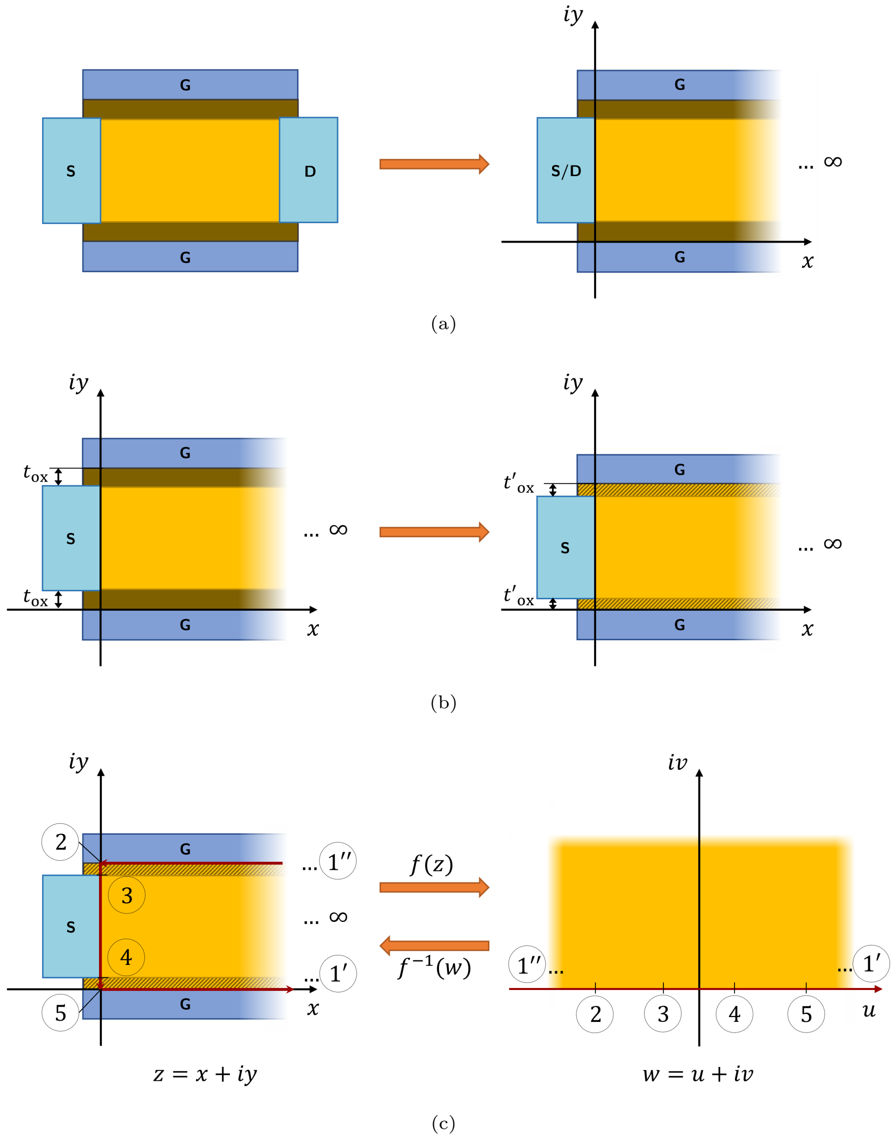

Figure 2.4: Various steps of the 2D potential model. (a): The transistor is split into two partial problems - a source and a drain related case, each represented in the complex z-plane. (b): The oxide thickness is adjusted, so the permittivity of the oxide matches the semiconductor's permittivity. (c): The partial devices are transformed, using the SCT, so the potential solution can be calculated in the complex w-plane.

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for the drain-side transformation. With Eq. (2.22) the positions $1'$, $1''$, 2 to 5 shown in Fig. 2.4(c) can be mapped and described by their x and y coordinates, as:

$$u'_{1'} = \cosh\left(\frac{\pi(3L_{\mathrm{ch}} + i(2t'_{\mathrm{ox}} + t_{\mathrm{ch}}))}{2t'_{\mathrm{ox}} + t_{\mathrm{ch}}}\right), \tag{2.25}$$

$$u'_{2} = \cosh\left(\frac{\pi(0 + i(2t'_{\mathrm{ox}} + t_{\mathrm{ch}}))}{2t'_{\mathrm{ox}} + t_{\mathrm{ch}}}\right), \tag{2.26}$$

$$u'_{3} = \cosh\left(\frac{\pi(0 + i(t'_{\mathrm{ox}} + t_{\mathrm{ch}}))}{2t'_{\mathrm{ox}} + t_{\mathrm{ch}}}\right), \tag{2.27}$$

$$u'_{4} = \cosh\left(\frac{\pi(0 + it'_{\mathrm{ox}})}{2t'_{\mathrm{ox}} + t_{\mathrm{ch}}}\right), \tag{2.28}$$

$$u'_{5} = \cosh\left(\frac{\pi(0 + i0)}{2t'_{\mathrm{ox}} + t_{\mathrm{ch}}}\right), \tag{2.29}$$

and:

$$u'_{1''} = \cosh\left(\frac{\pi(3L_{\mathrm{ch}} + i0)}{2t'_{\mathrm{ox}} + t_{\mathrm{ch}}}\right). \tag{2.30}$$

The term $3L_{\mathrm{ch}}$ in Eq. (2.25) and Eq. (2.30) indicates that the point is far over L_{ch} and is used instead of ∞.

The actual potential inside the w-plane is calculated by the Poisson integral:

$$\Phi(u,v) = \frac{1}{\pi}\int_{-\infty}^{\infty} \frac{v}{(u-u')^2 + v^2} \cdot \Phi_{\mathrm{bnd}}(u') \cdot du', \tag{2.31}$$

where $\Phi_{\mathrm{bnd}}(u')$ is the Dirichlet boundary condition along the edge between two u'_{i}. These boundary conditions must be defined at the device's edges that are transformed onto the u-axis. Two types of boundary conditions are used. For constant boundary conditions, $\Phi_{\mathrm{bnd}}(u') = \Phi_{\mathrm{const}}$ is used, leading to the Poisson integral:

$$\Phi_{\mathrm{const}}(u,v) = \frac{1}{\pi}\int_{-\infty}^{\infty} \frac{v}{(u-u')^2 + v^2} \cdot \Phi_{\mathrm{const}} \cdot du', \tag{2.32}$$

which solves to:

$$\Phi_{\mathrm{const}}(u,v) = \left[-\frac{\Phi_{\mathrm{const}} \cdot \tan^{-1}\left(\frac{u-u'}{v}\right)}{\pi}\right]_{u_{\mathrm{a}}}^{u_{\mathrm{b}}}. \tag{2.33}$$

For linear boundary conditions, using the electric field component E_{y}, the Poisson integral

becomes:

$$\Phi_{\mathrm{lin}}(u,v) = \frac{1}{\pi}\int_{-\infty}^{\infty} \frac{v}{(u-u')^2+v^2} \cdot E_{\mathrm{y}}\frac{\Delta y}{\pi} \cdot \cosh^{-1}(u) \cdot du', \tag{2.34}$$

which needs to be simplified and solved. For the solution of Eq. (2.34) please refer to [29].

After applying the SCT and set up the equations for the potentials, the actual boundary conditions have to be defined at the device's edges in the next step. At these edges, boundary conditions are used, which are shown in Fig. 2.5. These boundaries are given as:

Gate 1 (1” to 2):	$V_{\mathrm{g}} - V_{\mathrm{fb}}$ (constant)
Oxide 1 (2 to 3):	linear function from Gate 1 to Source/Drain
Source/Drain (3 to 4):	$V_{\mathrm{s/d}} + \Phi_{\mathrm{bi}}$ (constant)
Oxide 2 (4 to 5):	linear function from Source/Drain to Gate 2
Gate 2 (5 to 1’):	$V_{\mathrm{g}} - V_{\mathrm{fb}}$ (constant)

In case of both gate boundaries, the applied gate voltage V_{g} minus the gate material induced flatband voltage V_{fb} is used. The source or drain boundary uses either the applied source V_{s} or drain voltage V_{d} plus the device's built-in potential Φ_{bi}, which is caused by source-channel or drain-channel material junction. The potential Φ_{bi} for SBFETs is explained in Sec. 2.4.1. Finally, for the oxide regions a linear potential drop is expected, which leads to a linear function as boundary condition, connecting the potential of the gates to the potential of the source/drain region.

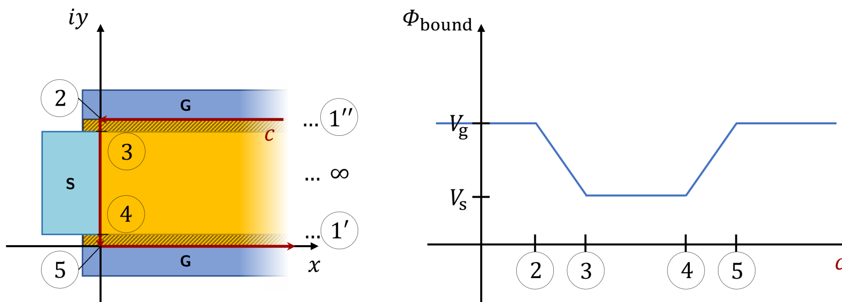

Figure 2.5: Boundary potentials along the red path c at the device's edges, showing the constant and linear boundaries.

The last step performed in the 2D potential algorithm is superposing the calculated potentials. This is done by using Eq. (2.33) and Eq. (2.34) with the defined boundary conditions. First, the potentials per terminal / partial device are superposed, as:

$$\Phi_{\mathrm{2D,s}}(x,y) = \Phi_{\mathrm{const,Gate1}} + \Phi_{\mathrm{const,Source}} + \Phi_{\mathrm{const,Gate2}} + \Phi_{\mathrm{lin,Oxide1}} + \Phi_{\mathrm{lin,Oxide2}}, \tag{2.35}$$

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for the source-related case and:

$$\Phi_{\mathrm{2D,d}}(x,y) = \Phi_{\mathrm{const,Drain}} + \Phi_{\mathrm{lin,Oxide1}} + \Phi_{\mathrm{lin,Oxide2}}, \tag{2.36}$$

for the drain-related case. Both partial potential solutions are then added together, as

$$\Phi_{\mathrm{2D}}(x,y) = \Phi_{\mathrm{2D,s}}(x,y) + \Phi_{\mathrm{2D,d}}(x,y), \tag{2.37}$$

for the final 2D potential. This superposition leads to the enclosed device solution and adds the impact of the drain terminal to the source side, as well as the source terminal to the drain side. By using Eq. (2.37) and the coordinates of an arbitrary point inside the device $(x|y), 0 \leq x \leq L_{\mathrm{ch}}, t_{\mathrm{ox}} \leq y \leq t_{\mathrm{ox}} + t_{\mathrm{ch}}$, the potential at this point Φ_{2D} can be determined. A more extensive derivation and discussion about this model can be found in [29].

2.1.6 Consideration of Accumulated Charges

At high gate voltage charges will be accumulated inside a transistors channel, which lead to the transistor's charge-carrier transport, but also affect the potential inside the channel. These charges are usually (in case of a transistor using doped regions) referred to as inversion charges, but in case of SBFETs using intrinsic or lightly doped silicon as channel material, are more accurately named as accumulated charges, since the carrier type is not inverting in this case.

Accumulated charges inside the device's channel at the semiconductor-oxide interface lead to a reduction of the surface potential. However, the 2D potential model from Sec. 2.1.5 is based on the Laplace equation, neglecting space charges. Therefore, the accumulated charges need to be considered for a correctly behaving model at all bias voltages. For this, a model addition has been included which is introduced and described in the tunnel field-effect transistor model from [33], following and using approaches from [43–46].

For a proper integration of the accumulation effects into the 2D potential model, an expression for an effective gate-source voltage $V_{\mathrm{gs,eff,TFET}}$ is obtained, which replaces the actual gate-source voltage when using this model. This voltage $V_{\mathrm{gs,eff,TFET}}$ must be equal to V_{gs} at small biases, but saturate at about $V_{\mathrm{gs}} > V_{\mathrm{ds}}$, and is expressed as:

$$V_{\mathrm{gs,eff,TFET}}(V_{\mathrm{gs}},V_{\mathrm{ds}}) = \frac{k_{\mathrm{b}}\vartheta}{q} \cdot u_{\mathrm{s,3}}, \tag{2.38}$$

with the Boltzmann constant k_{b}, the temperature ϑ and the elementary charge q. The coefficient $u_{\mathrm{s,3}}$ is the normalized surface potential, which cannot be obtained analytically, but is calculated using the Newton method on a proposed 1D Poisson equation, performing three iteration steps. The entire method is beyond the scope of this work. For the full derivation and discussion of this method, the author would like to refer to [33].

2.2 Charge-Based MOSFET Model

The current flowing through a SBFET is mainly dominated by the carrier injection over the device's SBs. However, in some cases it is necessary to consider the carrier transport inside a device's channel. This section introduces a simple MOSFET model that is needed for the SBFET/RFET model in later chapters.

In literature, there are a lot of different MOSFET compact models. A good overview of various models for undoped DG MOSFETs can be found in [47]. The model that is used in this work is a charge-based MOSFET model, given by:

$$I_{\mathrm{DGMOSFET}} = 2\mu \frac{W_{\mathrm{ch}}}{L_{\mathrm{ch}}} \cdot \left[V_{\vartheta} \cdot \left(Q'_{\mathrm{s}} - Q'_{\mathrm{d}} \right) + \frac{Q'^{2}_{\mathrm{s}} - Q'^{2}_{\mathrm{d}}}{2 \cdot C'_{\mathrm{ox}}} \right], \tag{2.39}$$

using the device geometries W_{ch} and L_{ch}, the carrier mobility μ (μ_{n} in case of electrons and μ_{p} in case of holes), the oxide capacitance per gate area C_{ox}, and the thermal voltage $V_{\vartheta} = k_{\mathrm{b}}\vartheta/q$ [47, 48]. The charge densities per gate area can be calculated, according to [48], by:

$$Q'_{\mathrm{s}} = \frac{S}{\ln(10)} \cdot C'_{\mathrm{ox}} \cdot W_0 \left(\exp\left(\frac{V_{\mathrm{gs}} - V_{\mathrm{T0}}}{S/\ln(10)} \right) \right), \tag{2.40}$$

for the source-related charge density and:

$$Q'_{\mathrm{d}} = \frac{S}{\ln(10)} \cdot C'_{\mathrm{ox}} \cdot W_0 \left(\exp\left(\frac{V_{\mathrm{gd}} - V_{\mathrm{T0}}}{S/\ln(10)} \right) \right), \tag{2.41}$$

for the drain-related charge density. The given charge densities are dependent on the corresponding voltages, which are either V_{gs} as the gate-source voltage or V_{gd} as the gate-drain voltage. The parameter S and V_{T0} are used as fitting parameters, which are the subthreshold swing S and the threshold voltage V_{T0} of the device. The function $W_0(x)$ is the principal branch of the Lambert W function, which is implicitly defined as:

$$W_0(x) \cdot \exp\left(W_0(x)\right) = x,\ W_0(x) \geq -1, \tag{2.42}$$

and approximated in this work, by:

$$W_0(x) \approx \ln(1{+}\mathrm{x}) \cdot \left(1 - \frac{\ln(1 + \ln(1 + x))}{2 + \ln(1 + x)} \right), \tag{2.43}$$

according to [49]. An extensive mathematical study on the Lambert W function can be found in [49].

The presented model is used in the document's main chapter for modeling the SBFETs' and RFETs' channel resistances.

2.3 Tunnel Effect

One of the most important charge carrier transport mechanisms that is part of the SB devices' working principle is the so-called tunneling effect, which is an effect appearing in quantum mechanics. This section introduces some basics about quantum mechanics, the tunnel effect and discusses basic models for a mathematical description of carrier transport through tunneling. The following sub-sections are summarized from [50, 51] in case it is not noted differently.

2.3.1 Wave Function and Schrödinger Equation

In 1926 the physicist *Erwin Schrödinger* published his postulated wave equation [52, 53]. This equation, which got famous under the term of *Schrödinger equation* was a milestone in the field of theoretical quantum mechanics and has proven to be a valid approach for solving problems in the field of quantum mechanics until today. The Schrödinger equation can be represented in various forms. A common form of this equation is:

$$i\hbar\frac{\partial}{\partial t}\Psi(\vec{r},t) = \left(-\frac{\hbar^2}{2m}\Delta + U(\vec{r},t)\right)\Psi(\vec{r},t), \tag{2.44}$$

which describes a particle's behavior as wave function $\Psi(\vec{r},t)$ dependent on the 3D position vector $\vec{r} = (x,y,z)^{\mathrm{T}}$ and the time t. In Eq. (2.44), $\hbar$ is the reduced Planck constant, m is the particle's mass, and Δ is the Laplace operator given as the squared nabla operator $\Delta = \nabla \cdot \nabla$, which is $\nabla = (\partial/\partial x, \partial/\partial y, \partial/\partial z)^{\mathrm{T}}$ in the 3D Cartesian coordinate system. $U(\vec{r},t)$ is the environmental potential where the particle exists in (e.g. gravitational potential or electrostatic potential) and i is the imaginary unit (with $i^2 = -1$). The wave function can be used to determine the probability of the particle being located at a certain position in a volume V at a certain time t, in case the normalization condition is met, given as:

$$P_{\text{particle in V}} = \int\limits_V |\Psi(\vec{r})|^2 \cdot d^3r = 1. \tag{2.45}$$

A simple application of the Schrödinger equation is the description of a free particle in a potential free environment ($U(\vec{r},t) = 0$). In this case, the common form of the wave function, given as

$$\Psi(\vec{r},t) = A_0 \cdot \exp\left(i(\vec{k}\cdot\vec{r} - \omega t)\right), \tag{2.46}$$

with the wave function's amplitude A_0, the wave vector $\vec{k}$, and the angular frequency ω, it can be used to solve Eq. (2.44). Therefore, Eq. (2.46) can be derived as:

$$\frac{\partial}{\partial t}\Psi(\vec{r},t) = -A_0 \cdot i\omega \cdot \exp\left(i(\vec{k}\cdot\vec{r} - \omega t)\right), \tag{2.47}$$

and

$$\Delta\Psi(\vec{r},t) = -A_0 \cdot |\vec{k}|^2 \cdot \exp\left(i(\vec{k}\cdot\vec{r} - \omega t)\right). \tag{2.48}$$

Using Eq. (2.47) and Eq. (2.48) in Eq. (2.44) leads to $|\vec{k}|^2 = 2m \cdot \omega/\hbar$, which matches the *de Broglie* relations for the particle's impulse $\vec{p} = \hbar \cdot \vec{k}$ and energy $\mathcal{E} = \hbar \cdot \omega = |\vec{p}|/(2m)$.

2.3.2 Tunneling Probability

One essential mechanism for the device's discussed in this work is the quantum mechanical tunnel effect, which can only be explained by quantum physics. Since most of the tunneling problems that need to be discussed in this work deal with tunneling in only one direction (for transistors the source-drain direction), it is a legit simplification to describe the problem only in one dimension, so instead of $\vec{r}$ only x is used. In classical particle physics, it would be only possible for a particle to overcome an energy barrier in case the particles energy $\mathcal{E}$ was higher that the barrier U_0 or be reflected from the barrier in case of $\mathcal{E} < U_0$. By describing particles as waves, the wave theory offers the possibility that an incoming wave ψ_i partially passes an energy barrier (transmission), leading to a reduced amplitude of the transmitted wave ψ_t, and a second wave that is the reflected wave ψ_r in the opposing direction of the incoming wave with the "missing" amplitude. This is demonstrated in Fig. 2.6. Figure 2.6 breaks the

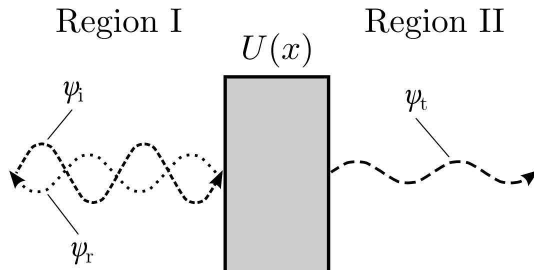

Figure 2.6: Particle as incoming plane wave ψ_i hitting an energy barrier, which results in a reflected wave ψ_r and a transmitted wave ψ_t. The image is taken from [33].

x-axis into the two regions I and II with their corresponding wave functions $\psi_\mathrm{I} = \psi_\mathrm{i} + \psi_\mathrm{r}$ and $\psi_\mathrm{II} = \psi_\mathrm{t}$. According to the normalization condition of Eq. (2.45), the absolute squared wave function is measure of probability to find the described particle at a certain position. With this dependency, a coefficient can be expressed that describes the probability of a single particle described as wave to tunnel through an arbitrary energy barrier, as

$$T = \frac{|\psi_\mathrm{t}|^2}{|\psi_\mathrm{i}|^2}. \tag{2.49}$$

In this case T is called the tunneling probability or transmission probability, which is dependent on the shape and height of the energy barrier and the initial particle's energy.

For a mathematical description, Eq. (2.44) is used again, but in a simplified version. The equation:

$$\left(-\frac{\hbar^2}{2m}\frac{\partial^2}{\partial x^2}+U(x)\right)\psi(x)=\mathcal{E}\cdot\psi(x), \tag{2.50}$$

is the one-dimensional and time-independent Schrödinger equation, with $\mathcal{E}$ as the particle's initial energy and $\psi(x)$ as the time-independent part of the wave function with the relation $\Psi(x,t)=\psi(x)\cdot\exp(-i\mathcal{E}t/\hbar)$. This results in the corresponding time-independent wave equation for a free particle (in case of $U(x)=0$):

$$\psi(x)=A_0\cdot\exp\left(ik\cdot x\right), \tag{2.51}$$

where k is the wave number, representing a scalar parameter instead of a vector, given as:

$$k=\sqrt{\frac{2m\cdot\mathcal{E}}{\hbar^2}}. \tag{2.52}$$

2.3.2.1 Tunneling Through Rectangular Barriers

An analytically solvable example of the tunneling probability is a tunneling process through a rectangular energy barrier, as shown in Fig. 2.7. In order to obtain an expression for the

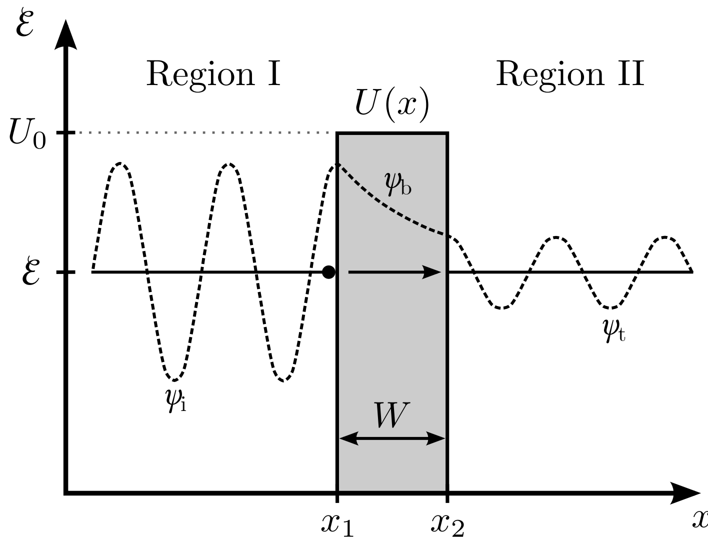

Figure 2.7: Particle as wave with the energy $\mathcal{E}$ tunneling through a rectangular energy barrier with the height U_0 and the thickness W. The image is taken from [33].

tunneling probability at the rectangular barrier T_{rect}, Eq. (2.49) is used with the incoming

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plane wave given as $\psi_\mathrm{i}(x) = A_\mathrm{i} \cdot \exp(ik_1 \cdot x)$, the reflected wave $\psi_\mathrm{r}(x) = A_\mathrm{r} \cdot \exp(-ik_1 \cdot x)$, and the transmitted wave given as $\psi_\mathrm{t}(x) = A_\mathrm{t} \cdot \exp(ik_1 \cdot x)$, according to Eq. (2.51) and Eq. (2.52). The wave function inside the barrier ψ_b (between regions I and II) needs to be described by the Schrödinger equation Eq. (2.50), as

$$\left(-\frac{\hbar^2}{2m}\frac{\partial^2}{\partial x^2} + (U_0 - \mathcal{E})\right)\psi_\mathrm{b}(x) = 0, \tag{2.53}$$

where U_0 is the constant barrier height. In case of $\mathcal{E} < U_0$, the equation:

$$\psi_\mathrm{b}(x) = C_1 \cdot \exp(k_2 \cdot x) + C_2 \cdot \exp(-k_2 \cdot x), \tag{2.54}$$

with:

$$k_2 = \frac{\sqrt{2m \cdot (U_0 - \mathcal{E})}}{\hbar}, \tag{2.55}$$

is a solution of Eq. (2.53)

With the discussed partial wave functions in both regions $\psi_\mathrm{I} = \psi_\mathrm{i} + \psi_\mathrm{r}$ and $\psi_\mathrm{II} = \psi_\mathrm{t}$, as well as ψ_b inside the energy barrier, a total wave function can be expressed, as:

$$\psi(x) = \begin{cases} A_\mathrm{i} \cdot \exp(ik_1 \cdot x) + A_\mathrm{r} \cdot \exp(-ik_1 \cdot x), & x < x_1 \\ C_1 \cdot \exp(k_2 \cdot x) + C_2 \cdot \exp(-k_2 \cdot x), & x_1 < x < x_2 \\ A_\mathrm{t} \cdot \exp(ik_1 \cdot x), & x > x_2 \end{cases}. \tag{2.56}$$

In order to find a way to determine the tunneling probability T_rect using Eq. (2.49), as:

$$T_\mathrm{rect} = \frac{|\psi_\mathrm{t}|^2}{|\psi_\mathrm{i}|^2} = \frac{|A_\mathrm{t} \cdot \exp(ik_1 \cdot x)|^2}{|A_\mathrm{i} \cdot \exp(ik_1 \cdot x)|^2} = \frac{|A_\mathrm{t}|^2}{|A_\mathrm{i}|^2}, \tag{2.57}$$

the coefficients A_i, A_r, C_1, C_2, A_t of Eq. (2.56) need to be related to each other. This is done by fulfilling the steadiness conditions of $\psi(x)$ and $d\psi(x)/dx$ at $x = x_1$ and $x = x_2$.

This calculation is not performed here but can be found in various publications (e.g. [50]). Following [50], Eq. (2.57) solves into:

$$T_\mathrm{rect} = \frac{1}{1 + \frac{1}{4}\eta^2 \sinh^2(k_2 \cdot W)}, \tag{2.58}$$

with

$$\eta = \frac{k_2}{k_1} - \frac{k_1}{k_2}. \tag{2.59}$$

2.3.2.2 Tunneling Through Triangular Barriers

In the previous section, an exact and analytical way of calculating the tunneling probability for a rectangular barrier is shown. This however is only possible due to the simplicity of the barrier's shape. Usually, it is not possible to find a closed-form solution without any approximation for

more complex barrier shapes than the rectangular shape. Figure 2.8 shows an example for a tunneling process through a triangular barrier. A very commonly used approximation to

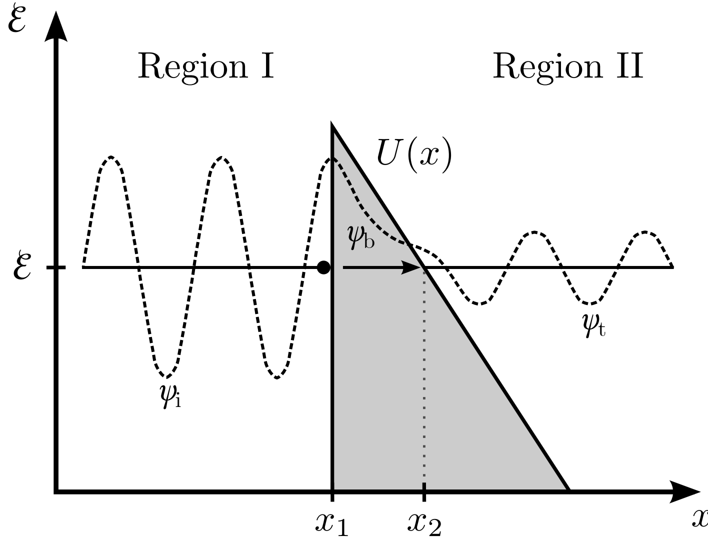

Figure 2.8: Particle as wave with the energy $\mathcal{E}$ tunneling through a triangular energy barrier. The image is taken from [33].

calculate the tunneling probability through non-rectangular barriers is the approach by *Kramers* [54], using the work from *Wentzel* [55] and *Brillouin* [56], which is commonly be referred to as Wentzel-Kramers-Brillouin (WKB) approximation. The basic idea of this approximation is to use the solutions Eq. (2.54), Eq. (2.55) from the rectangular barrier in Eq. (2.50) and treat the potential U_0 as it was (almost) constant. In this approach, the wave number inside the tunneling barrier is represented by:

$$k_2(x) = \frac{\sqrt{2m \cdot (\mathcal{E} - U(x))}}{\hbar}, \tag{2.60}$$

and it is estimated that the wave's argument can be described in infinitesimally small phase parts, which lead to the integral:

$$\psi_\mathrm{b}(x) = \psi_\mathrm{b}(x_0) \cdot \exp\left(\pm i \int_{x}^{x_0} k_2(x')dx' \right), \tag{2.61}$$

Since it makes no sense that a wave's wavelength $\lambda = 2\pi/k$ changes (quickly) along the x-axis, the WKB approximation is only valid in case that the potential U_x and therefore, the wave number k varies very slowly so the condition:

$$\left| \frac{d\lambda}{dx} \right| \ll 1, \tag{2.62}$$

is fulfilled [50]. A mathematical derivation of the WKB approximation is not discussed further in this work but can be found for example in [51].

The tunneling probability of the WKB method can be written as:

$$T_{\mathrm{WKB}} = \frac{|\psi_{\mathrm{t}}|^2}{|\psi_{\mathrm{i}}|^2} = \left| \frac{\exp\left(i \int\limits_{-\infty}^{x_2} k_2(x')dx' \right)}{\exp\left(i \int\limits_{-\infty}^{x_1} k_2(x')dx' \right)} \right|^2 = \left| \exp\left(i \int\limits_{x_1}^{x_2} k_2(x')dx' \right) \right|^2$$
$$= \exp\left(2i \int\limits_{x_1}^{x_2} k_2(x')dx' \right) = \exp\left(-\frac{2}{\hbar} \int\limits_{x_1}^{x_2} \sqrt{2m \cdot (U(x') - \mathcal{E})} dx' \right), \tag{2.63}$$

In the next step, the WKB approximation is applied on a triangular energy barrier, as shown in Fig. 2.8. This barrier is mathematically described as:

$$U(x) = -\frac{U(x_1) - \mathcal{E}}{x_2 - x_1} \cdot (x - x_2) + \mathcal{E}. \tag{2.64}$$

Using Eq. (2.64) in Eq. (2.63) and solving the integral leads to:

$$\begin{aligned} T_{\mathrm{WKB}}(\mathcal{E}) &= \exp\left(-\frac{4}{3\hbar} \cdot \sqrt{2m \cdot (U(x_1) - \mathcal{E})} \cdot (x_2 - x_1) \right) \\ &= \exp\left(-\frac{4}{3\hbar} \cdot \sqrt{2m \cdot (U_0 - \mathcal{E})} \cdot (t_{\mathrm{tun}}(\mathcal{E})) \right), \end{aligned} \tag{2.65}$$

valid at $\mathcal{E} < U_0$, with the maximum barrier height U_0 at x_1, and the tunneling thickness at the given particle energy $t_{\mathrm{tun}}(\mathcal{E})$.

2.3.3 Tunneling of Charge Carriers

In the previous sections the tunneling probability was determined for arbitrary particles which are described by wave functions. For electronic devices that rely on the tunnel effect as transport mechanism, like SBFETs, the tunneling particles are electrons or holes, which make up the charge-carrier current. This section shows two basic models that use the tunneling probability of an arbitrary barrier in order to calculate a tunneling current density. Additionally, Sec. 2.3.3.3 qualitatively describes a wave-based numerical method used to calculate the current transmission through energy barriers.

2.3.3.1 Tsu-Esaki Tunnel Equation

The Tsu-Esaki tunnel model approach [57, 58] can be used to determine a current density given by tunneling charge carriers from a region I to a second region II. For the derivation shown in this section, both [33, 59] are used as references.

The tunneling current density J_{tun} is described as a balance of charge carriers tunneling from region I to region II ($J_{\text{I}\to\text{II}}$) and those tunneling backwards ($J_{\text{II}\to\text{I}}$), as:

$$J_{\text{tun}} = J_{\text{I}\to\text{II}} - J_{\text{II}\to\text{I}}. \tag{2.66}$$

As shown in [59], the current components can be represented as:

$$J_{\text{I}\to\text{II}} = \frac{4\pi \cdot q \cdot m^*}{h^3} \cdot \int_{\mathcal{E}_{\text{min}}}^{\mathcal{E}_{\text{max}}} T(\mathcal{E}) \cdot d\mathcal{E} \cdot \int_0^\infty f_{\text{I}}(\mathcal{E}_{\text{tot}}) \left(1 - f_{\text{II}}(\mathcal{E}_{\text{tot}})\right) \cdot d\mathcal{E}_\rho \,, \tag{2.67}$$

and:

$$J_{\text{II}\to\text{I}} = \frac{4\pi \cdot q \cdot m^*}{h^3} \cdot \int_{\mathcal{E}_{\text{min}}}^{\mathcal{E}_{\text{max}}} T(\mathcal{E}) \cdot d\mathcal{E} \cdot \int_0^\infty f_{\text{II}}(\mathcal{E}_{\text{tot}}) \left(1 - f_{\text{I}}(\mathcal{E}_{\text{tot}})\right) \cdot d\mathcal{E}_\rho \,, \tag{2.68}$$

respectively, with the effective mass of the charge carrier m^*, the elementary charge q and the Planck constant h. In the given equations, $\mathcal{E}$ is the transversal energy component (in direction of the tunnel process). The carriers' longitudinal energy $\mathcal{E}_\rho$ is the energy component related to the longitudinal wave-components of the carrier, where the total carrier's energy can be expressed as $\mathcal{E}_{\text{tot}} = \mathcal{E} + \mathcal{E}_\rho$. The inner integral over all longitudinal energies contains the product of the Fermi distribution functions, describing the filled electron states in region I as $f_{\text{I}}(\mathcal{E}_{\text{tot}})$ and the free electron states in region II as $(1 - f_{\text{II}}(\mathcal{E}_{\text{tot}}))$. The outer integral contains the tunneling probability $T(\mathcal{E})$, which can be calculated for example by using Eq. (2.63). The boundaries $\mathcal{E}_{\text{min}}$ and $\mathcal{E}_{\text{max}}$ are the minimum and maximum energies of the tunneling barriers (e.g. the top and the bottom of a SB).

By using Eq. (2.67) and Eq. (2.68) in Eq. (2.66), it can be expressed as:

$$J_{\text{tun}} = \frac{4\pi \cdot q \cdot m^*}{h^3} \cdot \int_{\mathcal{E}_{\text{min}}}^{\mathcal{E}_{\text{max}}} T(\mathcal{E}) \cdot d\mathcal{E} \cdot \int_0^\infty \left(f_{\text{I}}(\mathcal{E}_{\text{tot}}) - f_{\text{II}}(\mathcal{E}_{\text{tot}})\right) \cdot d\mathcal{E}_\rho \,. \tag{2.69}$$

The changed inner integral of Eq. (2.69) is called supply function $N(\mathcal{E})$, written as:

$$N(\mathcal{E}) = \int_0^\infty \left(f_{\text{I}}(\mathcal{E}_{\text{tot}}) - f_{\text{II}}(\mathcal{E}_{\text{tot}})\right) \cdot d\mathcal{E}_\rho \,. \tag{2.70}$$

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Using the Fermi distribution function:

$$f(\mathcal{E}) = \frac{1}{1 + \exp\left(\frac{\mathcal{E} - E_\mathrm{f}}{k_\mathrm{b}\vartheta}\right)}\,, \tag{2.71}$$

the Eq. (2.70) can be solved to:

$$N(\mathcal{E}) = k\vartheta \cdot \ln\left[\frac{1 + \exp\left(-\frac{\mathcal{E} - E_\mathrm{f,I}}{k_\mathrm{b}\vartheta}\right)}{1 + \exp\left(-\frac{\mathcal{E} - E_\mathrm{f,II}}{k_\mathrm{b}\vartheta}\right)}\right]\,, \tag{2.72}$$

with $E_\mathrm{f,I}$ and $E_\mathrm{f,II}$ as the Fermi energy levels in the two regions, the Boltzmann constant k_b and the temperature ϑ.

With the supply function the Tsu-Esaki tunneling equation can be stated as:

$$J_\mathrm{tun} = \frac{4\pi \cdot q \cdot m^*}{h^3} \cdot \int_{\mathcal{E}_\mathrm{min}}^{\mathcal{E}_\mathrm{max}} T(\mathcal{E}) \cdot N(\mathcal{E}) \cdot d\mathcal{E}\,. \tag{2.73}$$

For a more detailed derivation of the equation, please refer to [33, 59].

2.3.3.2 Sze-Chang Tunnel Equation

The tunnel current model proposed by Sze and Chang, which is described in [6, 60], is used to describe the tunneling charge carriers through SBs. The model is proposed as:

$$J_\mathrm{I\to II} = \frac{A^{**}\vartheta^2}{k_\mathrm{b}\vartheta} \cdot \int_{\mathcal{E}_\mathrm{min}}^{\mathcal{E}_\mathrm{max}} f_\mathrm{I}(\mathcal{E}) \cdot T(\mathcal{E}) \cdot [1 - f_\mathrm{II}(\mathcal{E})] \cdot d\mathcal{E}\,, \tag{2.74}$$

where only one tunneling direction (from region I to region II) is considered in the equation. The boundaries $\mathcal{E}_\mathrm{min}$ and $\mathcal{E}_\mathrm{max}$ are the minimum and maximum energies of the tunneling barriers, $f_\mathrm{I}(\mathcal{E})$ represent the filled electron states in region I and $(1 - f_\mathrm{II}(\mathcal{E}))$ represent the free electron states in region II. The constant k_b is the Boltzmann constant, ϑ is the temperature and A^{**} is, dependent on the used model variation, either the Richardson constant or an expression from the thermionic-emission-diffusion theory by Crowell and Sze [6, 61].

Although, this approach neglects some parts compared to the Tsu-Esaki approach from Sec. 2.3.3.1, for example the backwards current $J_\mathrm{II\to I}$ or the longitudinal energy components, it has been shown in [6, 29, 62] that the approach can be used for a compact model description of the tunneling current at SBs.

2.3.3.3 Non-Equilibrium Green's Function Method

Another method used to describe the transmission of charge carriers through a transistor, also considering tunneling barriers, is the so-called non-equilibrium Green's function (NEGF) Method. This method is a wave-based approach which separates the simulated device into different regions, where the so-called Hamiltonian of any region is represented in a matrix [63]. The resulting system is solved with the Green's function in order obtain a transmission coefficient T_{NEGF}, which can be used to calculate the device current [63]. The NEGF method is not used for calculations in this work, but it is used to explain the approach in Sec. 5.3.1, so a more in-depth discussion on the topic is omitted. For more details on the mathematical and physical details of the NEGF method the author would like to refer to [63–65].

2.4 Physical Description of Schottky Barriers

In the last section of this chapter, the physics of SBs are discussed. A SB is an energy barrier for charge carriers that forms as a result of a metal to semiconductor junction. This section explains the formation of SBs and the charge carrier injection mechanisms and reviews some of the well-known physical descriptions.

2.4.1 Band Diagram Construction

An energy band diagram of this junction for a material combination of nickel silicide (as metal) and silicon (as semiconductor) is shown in Fig. 2.9. In the state of Fig. 2.9(a) both

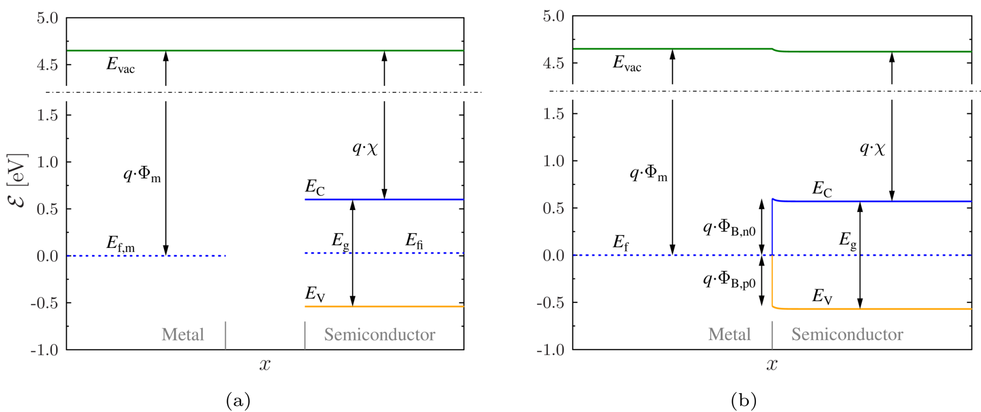


Figure 2.9: Band diagram of a material junction between nickel silicide as metal and silicon as semiconductor. (a) shows the band diagrams of the individual materials without contact. (b) shows band diagram of both materials in contact and in thermal equilibrium.

materials without contact are shown, with the metal's Fermi energy $E_{\mathrm{f}} = E_{\mathrm{f,m}}$ at the left

side and the semiconductor with its band diagram parameters at the right side. $E_\mathrm{f} = E_\mathrm{fi}$ is the semiconductor's intrinsic Fermi energy, E_C and E_V are the conduction and valence band energies, respectively, and the band gap E_g denotes their distance. E_vac is the vacuum energy level with $q\Phi_\mathrm{m} = E_\mathrm{vac} - E_\mathrm{f,m}$ as the metal's work function and $q\chi = E_\mathrm{vac} - E_\mathrm{C}$ as the semiconductors electron affinity. As they are contacting each other (shown in Fig. 2.9(b)), the material combination reaches the thermal equilibrium and therefore, the Fermi energy E_f is constant along the entire structure. The steadiness condition of the E_vac leads to a space charge region (t_scr) close to the metal-semiconductor junction and a band bending inside that region. The band bending results in the shown SB heights for electrons $q \cdot \Phi_\mathrm{B,n0}$ and for holes $q \cdot \Phi_\mathrm{B,p0}$, respectively. The SB heights can be calculated by using the material parameters, as:

$$q\Phi_\mathrm{B,n0} = q\Phi_\mathrm{m} - q\chi, \tag{2.75}$$

for electrons and:

$$q\Phi_\mathrm{B,p0} = E_\mathrm{g} - q\Phi_\mathrm{B,n0}, \tag{2.76}$$

for holes. The built-in potential Φ_bi determines the potential change over the space charge region and can be determined by:

$$q\Phi_\mathrm{bi} = (E_\mathrm{C} - E_\mathrm{f}) - q\Phi_\mathrm{B,n0} \approx \frac{E_\mathrm{g}}{2} - q\Phi_\mathrm{B,n0}. \tag{2.77}$$

2.4.2 Charge Carrier Transport over Schottky Barriers

The existence of a SB inside a device results in a blocking mechanism for charge carriers. Figure 2.10 shows the Schottky junction of Fig. 2.9(b) with a positive applied voltage at the semiconductor region (Fig. 2.10). There are two ways for charge carriers to pass a SB. Charge carriers with a reasonably high thermal energy can overcome the SB, which is shown as purple arrow in Fig. 2.10. This transport mechanism is called thermionic emission (TE). A second way for charge carriers to pass the barrier is by tunneling through it, in case the thickness of the barrier is thin enough. This transport mechanism is called field emission (FE) and is indicated by the green arrow in Fig. 2.10. There is also the possible combination of both mechanisms where carriers with high thermal energy can tunnel through the barrier above the metal's work function (thermionic field emission).

2.4.2.1 Thermionic Emission

The TE theory, which can be found for example in [2, 6, 7], is a state-of-the-art theory used to describe a charge carrier transport over an energy/potential barrier. Due to the thermal energy of a charge carrier and the Fermi statistics, it can overcome an arbitrary potential barrier Φ_bar, if the temperature is bigger than zero Kelvin and the barrier height is much bigger than $k_\mathrm{b}\vartheta$. The amount of the carriers overcoming the barrier is exponentially dropping with the barrier

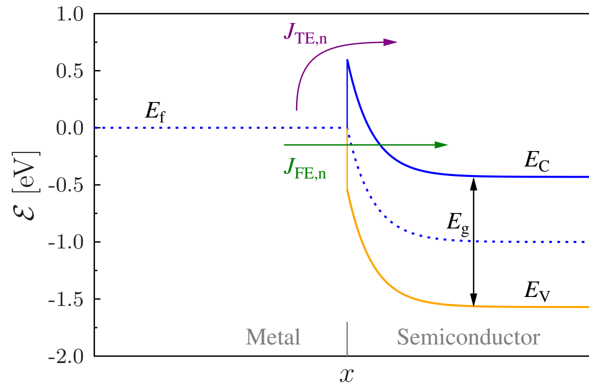


Figure 2.10: Biased SB with a positive potential difference from semiconductor to metal region. The injection electron currents from metal into the semiconductor are shown, where $J_{\mathrm{TE,n}}$ is the electron thermionic emission current and $J_{\mathrm{FE,n}}$ is the electron field emission current. The currents from the semiconductor into the metal region are neglected in this figure. Normally, in the space charge region, the Fermi energy would split up into two quasi-Fermi energies for each carrier type. To keep the graphic simple, this has been neglected.

height Φ_{bar}. The shape of the energy does not matter, as long as the barrier width reasonably small, so the carrier's drift-diffusion behavior inside the barrier region can be neglected.

The TE current density for a charge carrier overcoming an energy barrier from one region into another in a device's thermal equilibrium condition can be expressed by:

$$J_{\mathrm{TE,0}} = A^* \cdot \vartheta^2 \cdot \exp\left(-\frac{q \cdot \Phi_{\mathrm{bar}}}{k_{\mathrm{b}}\vartheta}\right). \tag{2.78}$$

In thermal equilibrium it needs to be considered that the TE current density from one region I to second region II over an energy barrier needs to be as big as the reverse current density ($J_{\mathrm{TE,0}} = J_{\mathrm{TE,0,I}\rightarrow\mathrm{II}} = J_{\mathrm{TE,0,II}\rightarrow\mathrm{I}}$), in order to prevent a net current flow. The parameter A^* in Eq. (2.78) is the Richardson constant, given as:

$$A^* = \frac{qm^* k_{\mathrm{b}}^2}{2\pi^2 \cdot \hbar^3}. \tag{2.79}$$

The coefficients of Eq. (2.78) and Eq. (2.79) are the Boltzmann constant k_{b}, the temperature ϑ, the elementary charge q, the reduced Planck constant $\hbar$ and the charge carriers' effective mass inside the material m^*.

As soon as an external voltage V is applied over the energy barrier, the current density increases exponentially with the applied voltage, by:

$$J_{\mathrm{TE}} = J_{\mathrm{TE,0}} \cdot \exp\left(\frac{q \cdot V}{k_{\mathrm{b}}\vartheta} - 1\right). \tag{2.80}$$

Equation (2.80) is a well-known equation that is used to calculate the current density for

Schottky diodes, for instance. It can also be used to calculate the TE current for SBFETs, which will be part of the modeling chapters.

2.4.2.2 Field Emission

The FE current contribution is the part of the total injection current that is made up by charge-carriers tunneling through the SB. The FE current is shown as green arrow in Fig. 2.10. In contrast to the TE current from Sec. 2.4.2.1, there is no closed-form mathematical expression for the FE current contribution. In order to calculate the FE current contribution, either an approach like those shown in Sec. 2.3.3 can be used and solved numerically (this is part of the work in [62]), or some simplifications and approximations have to be done for being able to solve the equations analytically. The second method is one of the main parts of this work's compact modeling attempts and is discussed in the main modeling chapters 4 to 6.

In some works, there is a distinction between the FE current given as direct tunneling process at the metal's Fermi energy level $E_{\mathrm{f,m}}$ and a mixed thermionic field emission current as a term for tunneling carriers which have a higher thermal energy than $E_{\mathrm{f,m}}$. This distinction is not made in this work, so every current contribution related to a tunneling process through the SB is called FE current.

2.4.3 Image-Force Lowering

Although the effect is not used in the compact model discussed in this work, as an additional effect at SBs, the Schottky barrier lowering (SBL) or image-force lowering effect shall be briefly discussed in this section, according to [6]. In case of the presence of an electric field over a SB, causing electrons to be injected over the SB in the semiconductor, a positive image charge will accumulate at the SB on the metal surface. The force (called image force) between the electron and the image charge causes an additional electric field $\vec{E}_{img}$ which counteracts the external field. This electric field causes a potential drop $\Delta\Phi$ over the SB, which leads to a reduced SB height and a change of the SB's curvature. As derived in [6], the SB height reduction can be expressed as:

$$\Delta\Phi = \sqrt{\frac{q \cdot |\vec{E}_{img}|}{4\pi\varepsilon_{\mathrm{sc}}}}, \tag{2.81}$$

leading to a reduced SB height of:

$$\Phi_{\mathrm{B,n}} = \Phi_{\mathrm{B,n0}} - \Delta\Phi, \tag{2.82}$$

in case of electrons. This effect works similarly for holes. Since the SBL effect has been neglected in this work, $\Delta\Phi = 0$ for this work, resulting in $\Phi_{\mathrm{B,n}} = \Phi_{\mathrm{B,n0}}$. For a further analysis and more information of the SBL effect, please refer to [6].

CHAPTER 3

Device Working Principles

After the fundamentals, presented in the previous chapters, this chapter introduces the covered devices and their working principle in more detail. The given explanations in this chapter are supported by TCAD device simulation results that have been performed on these transistors. The simulations and used parameters are briefly described in Sec. 3.1. After this, the SBFET is discussed in Sec. 3.2. In Sec. 3.3, using the basics of the SBFET, the RFET is introduced and explained. Finally, Sec. 3.4 shortly describes and reviews several compact models for SBFETs or RFETs.

3.1 TCAD Simulation Parameters

The explanation in this chapter is supported by a TCAD simulation studies of SBFET / RFET devices. The results of these simulations are shown as figures containing device characteristics or energy band diagrams. For running the simulation with TCAD Sentaurus, the devices use silicon as channel material with an oxide made of SiO_2, nickel silicide as source and drain metal and titanium as gate electrode material. The performed simulations are calibrated to the results of [66, 67], so some default parameters like metal work functions and tunnel masses haven been slightly adjusted, as shown in Tab. 3.1. In the simulation the device is simulated as cylindrical nanowire and the Nonlocal Mesh (NLM) together with the NLM tunneling model are used at the source and drain side of the device, in order to simulate tunneling charge carriers through the SB [28]. The simulation parameters can be found in Tab. 3.1, which is valid for all shown results in this chapter unless it is noted differently in some sections. If a parameter is not mentioned in the table, it is kept as default (see [28]).

The parameter $L_{\mathrm{CG/PG}}$ refers to the control gate and program gate lengths and is only applicable to the simulated RFETs.

Table 3.1: Parameters used in the TCAD simulations

Parameter	Value
L_{ch} [nm]	220
R_{NW} [nm]	6
t_{ox} [nm]	8
$L_{\mathrm{CG/PG}}$ [nm]	50
μ_{n} [cm^2 V^{-1} s^{-1}]	1417
μ_{p} [cm^2 V^{-1} s^{-1}]	471
μ_{tn} [cm^2 V^{-1} s^{-1}]	0.05
μ_{tp} [cm^2 V^{-1} s^{-1}]	0.05
m_{n} [-]	0.252
m_{p} [-]	0.202
$E_{\mathrm{g,Si}}$ [eV]	1.16964
$\Phi_{\mathrm{m,Ti}}$ [V]	4.63
$\Phi_{\mathrm{m,NiSi}}$ [V]	4.65

3.2 Schottky Barrier Field-Effect Transistor Working Principle

With the knowledge of SBs, their properties and working principle, discussed in the previous chapter, the SBFET is an electronic device that is relying on the existence on those. In classic MOSFET application, a transistor's (drain) current is controlled by pn-junctions, blocking the current flow in the device's off-state, and a conductive accumulation/inversion channel occurring in the device's on-state. Unlike this MOSFET working principle, the SBFET uses SBs at the source and drain side of the device in order to block the device current in the off-state. By biasing the device's gate electrode, the SBs become thinner due to the band bending and therefore, more conductive. This section explains the structure, working principle and electrical properties of SBFETs.

3.2.1 Device Structure

The SBFET consists of a metal-semiconductor-metal material combination in source-drain direction. The metallic source and drain regions connecting to the semiconductor channel lead to a SB at the source-channel and the drain-channel interface. The SBFET's channel is covered by an oxide and the gate electrode, that controls the current flow. The form of how the gate covers the channel is generally not predefined, which means that a SBFET can have a single top gate (as in classic MOSFET application), a double gate structure (which is a more theoretical device), or a structure with a higher gate control, similar to FinFET or gate-all-around nanowire structures. Figure 3.1(a) shows a schematic 2D-cross-sectional structure of a SBFET and Fig. 3.2 shows a 3D example of a SBFET. The compact model for SBFETs, which is introduced in Chap. 4, uses a DG structure device (see Fig. 3.2(a)), while real devices usually are GAA nanowire or similar structures [11, 68].

Figure 3.1(b) shows the band diagram of the simulated SBFET in source-to-drain direction with no bias voltages applied. The given figure shows the most important band diagram related parameters of the device. E_g is the bandgap of the channel's semiconductor material, $\Phi_\mathrm{B,n}$ is the SB height for electrons and $\Phi_\mathrm{B,p}$ is the SB height for holes. In the shown example of Fig. 3.1(b) the slight initial band bending is caused by the SBs' built-in potential (see Sec. 2.4.1).

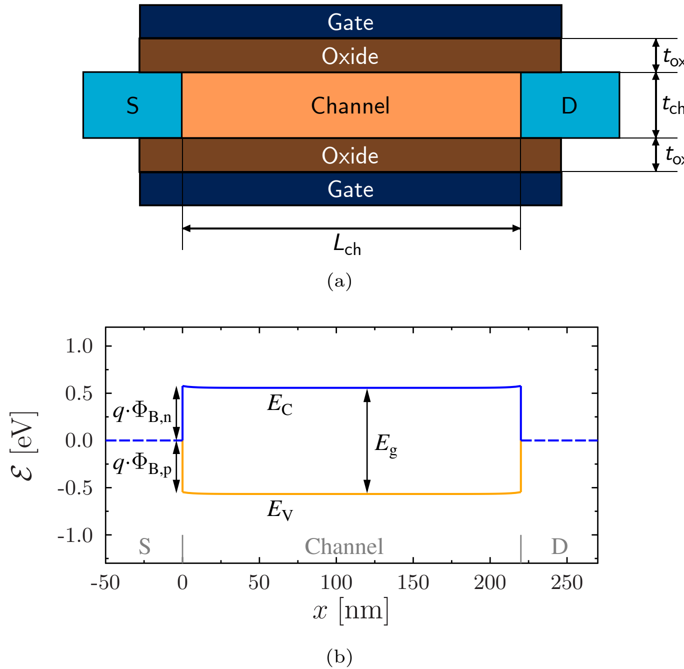


Figure 3.1: (a) schematic cross-section of a nanowire or double gate SBFET with its geometric parameters, and (b) example band diagram of the SBFET in thermal equilibrium (unbiased).

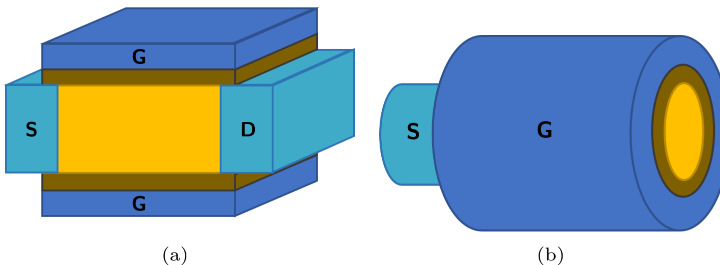


Figure 3.2: Possible schematic 3D shapes of the SBFET showing the different regions. The S/D are the source and drain regions and G is the gate electrode. The brown colored regions are the oxide regions and yellow is the semiconductor channel. (a) shows a DG structure which is extended in the width-direction. This structure is used in the compact model of Chapter 4, but usually not for real devices. (b) shows the source-side section of a gate-all-around nanowire SBFET, which is a more realistic device structure.

3.2.2 Working Principle and Characteristics

The I/V-characteristics of a SBFET can be split into three parts. An example transfer curve is shown in Fig. 3.3. The given transfer curve shows such a transistor for $V_{\mathrm{ds}} > 0\,\mathrm{V}$ which means it operates in n-type mode during the device's on-state. Fig. 3.4 shows the source-to-drain band diagram along the channel at the three different states shown in Fig. 3.3. These can be used in order to explain the SBFETs operation states and the characteristics.

- Figure 3.4(a) describes the SBFET's off-state at the given drain voltage. In the off-state the drain current of the device is the lowest and it is supposed to be switched off. For the given material combination with almost equally high SB heights for electrons and holes, this operation mode is given at the gate voltage where the gate-source and the drain-gate potential differences are about equally high, as it can be seen in the figure. In this state electrons can be injected at the source side of the device, as well as holes can be injected at the drain side through TE and FE. However, for the given material combination, the SBs at both sides are thicker compared to the other operation modes which leads to a reduced FE current, since this current contribution depends exponentially on the barrier thickness. Because of this dependency, the device's off-state is also dependent on the applied drain voltage.
- Figure 3.4(b) shows the device's on-state (where the SBFET is supposed to be switched on). In this operation state the conduction band is bent down due to the high gate voltage, so that the source-side SB is very thin and even a direct tunneling can occur. The drain-side hole current contribution is gone in this state; however, the source-side electron FE current is even higher by several decades.
- Figure 3.4(c) shows the ambipolar operation mode of the SBFET. This mode is usually unwanted, because in this state the device's drain current is increasing again, although V_{gs} is lower than the off-state gate voltage. In the ambipolar state, the drain-side SB has become very small and therefore, an increasing hole FE current is flowing from the drain to the source terminal[1].

As the previously shown band diagrams (Fig. 3.1(b) and Fig. 3.4) demonstrate, in the example SBFET of this section the SB heights for electrons $\Phi_{\mathrm{B,n}}$ and for holes $\Phi_{\mathrm{B,p}}$ are almost equally high. This device can also be used as a p-type device with $V_{\mathrm{ds}} < 0\,\mathrm{V}$. This is shown as an example transfer curve in Fig. 3.5. The characteristics in this case are similar to the n-type characteristics but with negative voltages and currents. The absolute current values of p- and n-type operation mode are not exactly similar (even if $\Phi_{\mathrm{B,p}}$ and $\Phi_{\mathrm{B,n}}$ were exactly

1 It shall be noted here that usually, the transistor's source is the terminal where electrons or holes are injected into the device and the transistor's drain is the terminal where the carriers flow out of the device. While in the ambipolar case this rule does not apply, the author keeps the terminal descriptions the same, because the ambipolar operation mode is an unwanted mode, and in order to avoid the confusion of changing the transistors terminals.

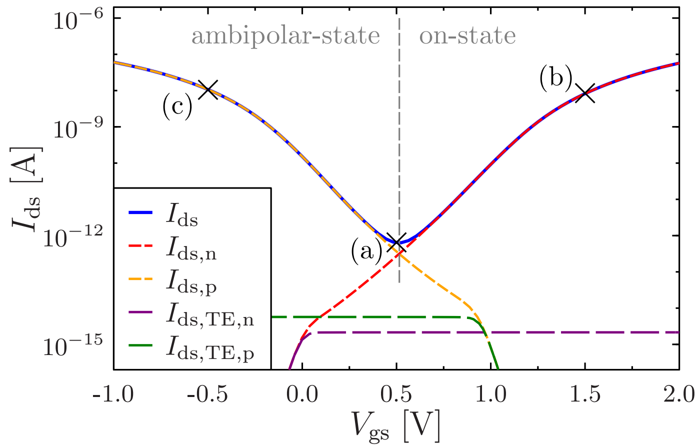


Figure 3.3: Single transfer curve of the simulated SBFET at the drain voltage $V_{ds} = 1\,V$, showing the total drain current I_{ds} and its current's components in logarithmic scale. $I_{ds,TE,n}$ and $I_{ds,TE,p}$ are the TE current contributions fo electrons and holes, respectively. $I_{ds,n}$ and $I_{ds,p}$ are the TE and FE current contributions of electrons and holes, respectively, that determine the on-current or ambipolar currents. (a), (b) and (c) refer to Fig. 3.4 marking the bias conditions at which the band diagrams are captured.

same), because the injected current over the SB not only depends on the SB height, but also on the charge carrier properties (injected electrons or holes), as it is demonstrated in Sec. 2.3.2.2. Figure 3.6 shows the different operation states in the p-type mode which are the off-state (a), the on-state (b), and the ambipolar state (c).

For a better overview of the SBFETs characteristics, Fig. 3.7 shows the device's transfer characteristics for multiple drain voltages, used as p-type (a) or n-type (b) device. The shown characteristics demonstrate the symmetry for the simulated SBFET, which is important for the RFET application explained in Sec. 3.3. Also, clearly visible in the shown characteristics is the device's absolute off-state current increasing and the off-state itself shifting to a higher absolute V_{gs} with an increasing absolute drain voltage V_{ds}. This is the case, because the lowest injection currents of the device flow in the state, where the surface potential (and therefore, the gate voltage) is almost exactly between the source and the drain potential, so at $V_{gs} \approx V_{ds}/2$, which is shown in the band diagrams of Fig. 3.4(a) and Fig. 3.6(a).

Figure 3.8 shows the output characteristics of the simulated SBFET at the n-type operation mode on-state ($V_{ds} > 0\,V$), where Fig. 3.8(a) focuses on applied gate voltages from 0.7 V to 1.3 V and Fig. 3.8(b) shows the applied gate voltages from 1.4 V to 2.0 V. In the shown characteristics of Fig. 3.8(a) it can be observed that, in case of the lowest gate voltages, the drain current suddenly starts to increase at about $V_{ds} > 1.5\,V$. This is caused by the device reaching the ambipolar operation state at $V_{ds} \gg V_{gs}$, which means that holes start to be injected at the drain side and the hole current surpasses the source-side electron current. Another typical

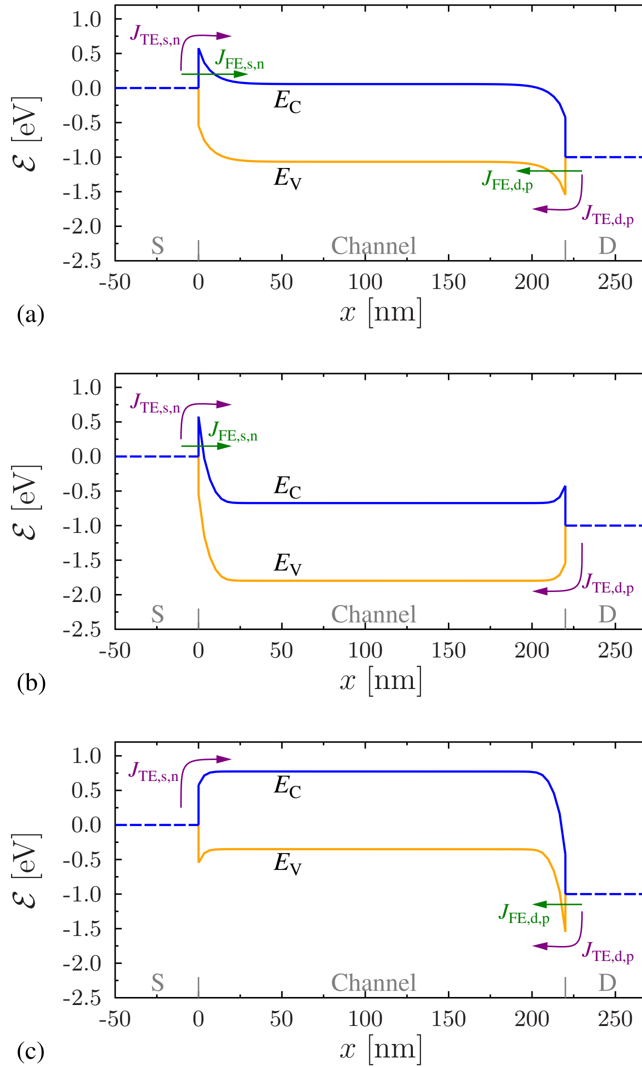


Figure 3.4: Band diagrams matching the markings of the simulated transfer curve from Fig. 3.3, showing the current contributions that are injected at the device's SBs. $J_{\mathrm{FE,s,n}}$ and $J_{\mathrm{TE,s,n}}$ are the source-side FE and TE electron current densities. $J_{\mathrm{FE,d,p}}$ and $J_{\mathrm{TE,d,p}}$ are the drain-side FE and TE hole current densities.
(a) shows the device's off-state band diagram. In this state all listed current densities are contributing to the total current, however, their total value is the lowest possible at the given drain voltage.
(b) shows the device's on-state band diagram. In this state, the TE contributions are still present, but the dominating on-current contribution is given by the source-side FE electron current density ($J_{\mathrm{FE,s,n}}$).
(c) shows the device's ambipolar state band diagram, which is usually an unwanted device state. In this state, the TE contributions are also still present, but the dominating current contribution is given by the drain-side FE hole current density ($J_{\mathrm{FE,d,p}}$).

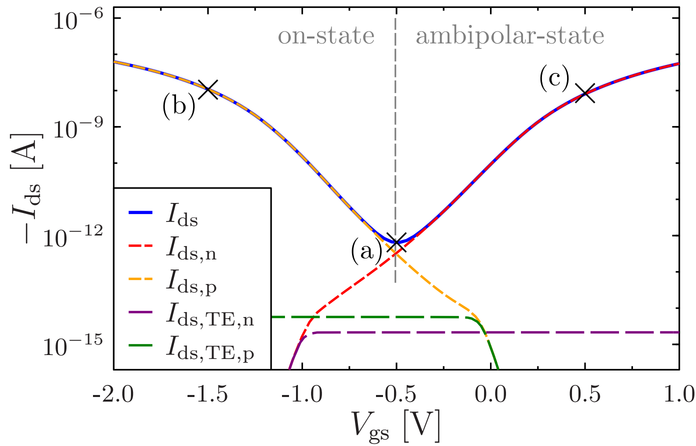


Figure 3.5: Single transfer curve of the simulated SBFET at the drain voltage $V_{ds} = -1\,V$, showing the total drain current I_{ds} and its current's components on a negative and logarithmic scaled y-axis. $I_{ds,TE,n}$ and $I_{ds,TE,p}$ are the TE current contributions fo electrons and holes, respectively. $I_{ds,n}$ and $I_{ds,p}$ are the TE and FE current contributions of electrons and holes, respectively, that determine the on-current or ambipolar currents. (a), (b) and (c) refer to Fig. 3.6 marking the bias conditions at which the band diagrams are captured.

SBFET effect is the s-shape effect which can be observed in all curves, which describes the behavior of the curve of slowly increasing (in the range of $0\,V < V_{ds} < 0.5\,V$), before reaching the linear and finally, the saturation region with increasing V_{ds}. The initial s-shape effect, in case of the simulated device, is likely being caused by the drain-side SB which acts as an additional energy barrier, blocking electrons at low V_{ds}, but vanishes at higher V_{ds}.

3.2.2.1 Symmetrical vs. Unsymmetrical Device Characteristics

The characteristics of Fig. 3.7 show a device that is nearly symmetrical for electrons and for holes, which means that the absolute drain current is nearly equally high when reversing the gate and drain voltage (switching between p-type and n-type operation). The symmetric behavior is mainly determined by the semiconductor's doping and the source / drain metal work function Φ_m but can also be fine-tuned by adjusting the semiconductor's lattice parameters by straining it, as proposed in [66]. The metal work function impact can be observed in the shown band diagrams of this chapter (e.g. Fig. 3.1(b), Fig. 3.4 and Fig. 3.6), where the SB height for electrons $\Phi_{B,n}$ is almost equally high to the SB height holes $\Phi_{B,p}$. Using a device with symmetric characteristics is useful in case that the device is planned to be used as switchable between p-type or n-type operation mode in later application, as for example the RFET.

In case that a SBFET shall be used only for one single operation type (either n-type or p-type operation), it can make sense to use a material combination that pronounces the on-state carrier type and suppresses the ambipolar one. Figure 3.9 shows a simulated example transfer

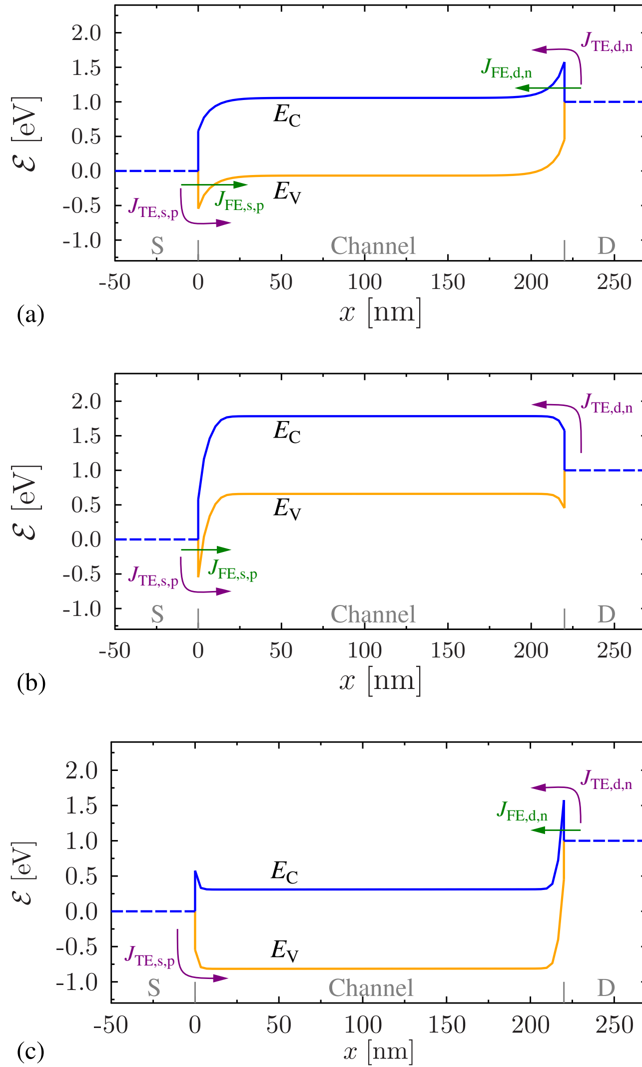
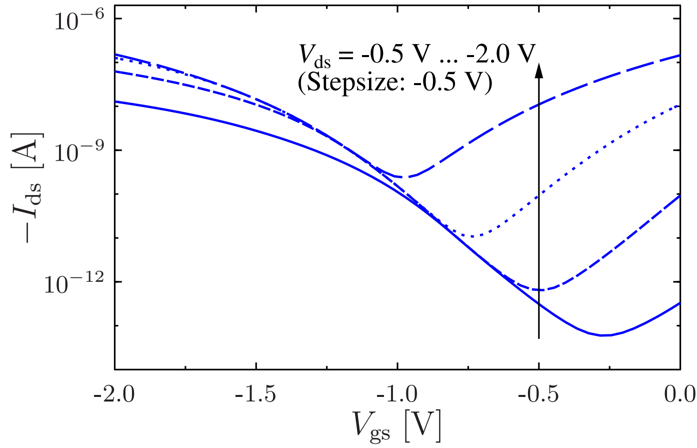
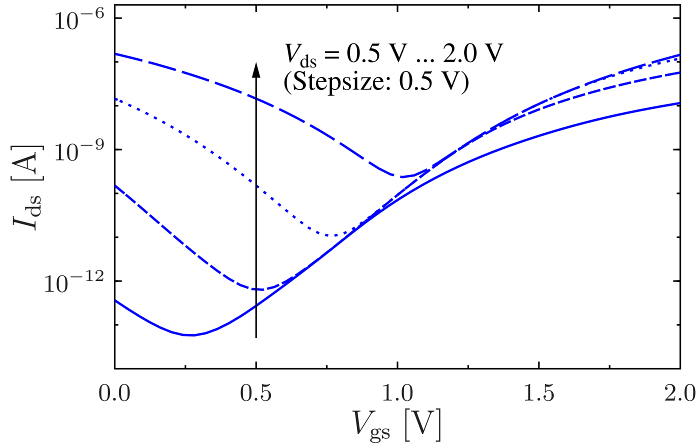


Figure 3.6: Band diagrams matching the markings of the simulated transfer curve from Fig. 3.5, showing the current contributions that are injected at the device's SBs. $J_{FE,s,p}$ and $J_{TE,s,p}$ are the source-side FE and TE hole current densities. $J_{FE,d,n}$ and $J_{TE,d,n}$ are the drain-side FE and TE electron current densities.
(a) shows the device's off-state band diagram. In this state all listed current densities are contributing to the total current, however, their total value is the lowest possible at the given drain voltage.
(b) shows the device's on-state band diagram. In this state, the TE contributions are still present, but the dominating on-current contribution is given by the source-side FE hole current density ($J_{FE,s,p}$).
(c) shows the device's ambipolar state band diagram, which is usually an unwanted device state. In this state, the TE contributions are also still present, but the dominating current contribution is given by the drain-side FE electron current density ($J_{FE,d,n}$).

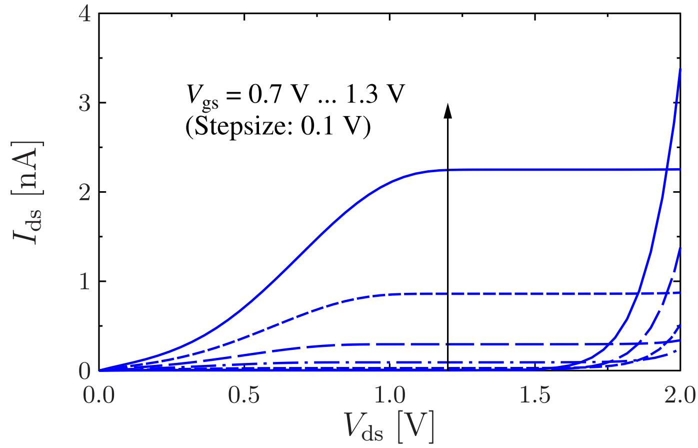


(a)

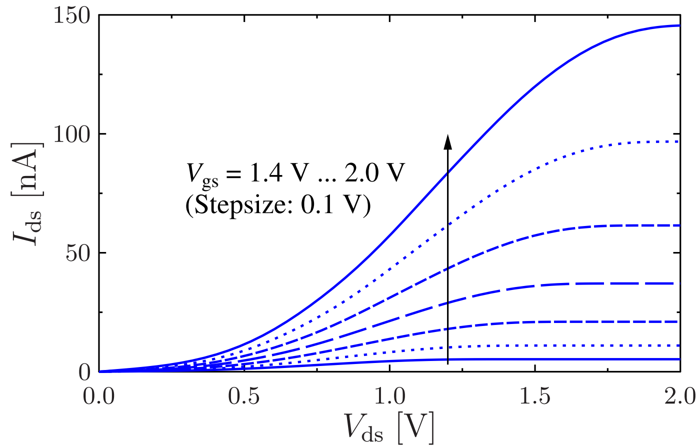


(b)

Figure 3.7: Transfer characteristics of the simulated SBFET at the given drain voltages showing the total drain current I_{ds} in logarithmic scale. (a) shows the p-type operation state with negative drain-voltages and a negative scaled y-axis. (b) shows the n-type operation state with positive drain-voltages.



(a)



(b)

Figure 3.8: Output characteristics of the simulated SBFET at the given gate voltages showing the total drain current I_{ds} in linear scale. The characteristics show the n-type operation mode only. (a) shows the lower gate voltages from 0.7 V to 1.3 V. (b) shows the higher gate voltages from 1.4 V to 2.0 V.

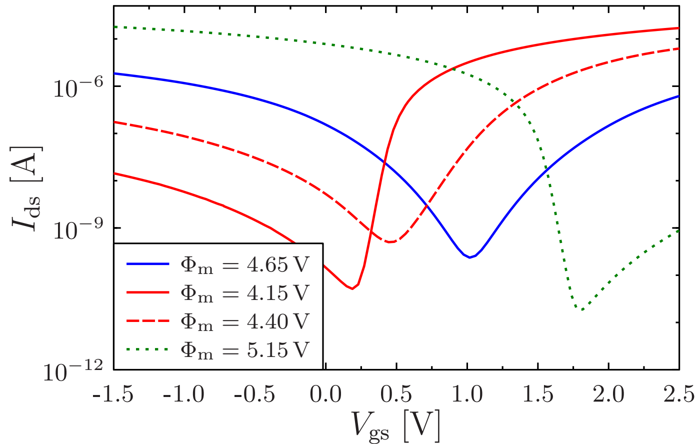


Figure 3.9: Single transfer curve of the simulated SBFET at the drain voltage $V_{ds} = 2$ V, compared to simulated devices with varying source / drain metal work functions Φ_m, showing the total drain currents I_{ds} in logarithmic scale. The red lines are simulations using lower work functions and the green dotted line uses a higher work function. The used metal work functions are presented in the legend. Besides the one from the blue curve, they are chosen for demonstration purposes only, without any relation to real metals.

curve of the already investigated transistor which is used in the previous sections (blue line). This single transfer curve is compared to other simulated curves of the same device, which only uses a different metal work function, as shown in the figure. The used work functions do not necessarily relate to realistic metals, they are just randomly chosen by increasing or reducing the used Φ_m in 0.5 V steps. All curves are simulated in the n-type operation mode's on-state, using the same drain voltage of $V_{ds} = 2$ V. As it can be seen in the simulation, reducing the metal work function Φ_m (red lines), which leads to a reduced SB height for electrons $\Phi_{B,n}$ and an increased SB height for holes $\Phi_{B,p}$, results in a better conductivity for electrons and a higher suppression of holes. Increasing the metal work function (green line), leads to the opposite effect and makes the on-state of the simulated n-type device worse. However, the green curves material combination, which increases the hole currents, would be preferable for p-type SBFETs.

The compact model presented in this work focuses completely on devices with a symmetric behavior, since it is also made for modeling RFETs. Therefore, the unsymmetrical characteristics that is demonstrated in the examples of Fig. 3.9 will not be discussed further.

3.2.2.2 Channel Length Impact

Usually in SBFET devices, when considering the working principle of current passing and blocking mechanisms, the injection over a transistor's SB is considered, because the SB is supposed to have the highest resistance inside the device. However, it needs to be considered

that the SBFET's channel consists of a semiconductor material (in this work it intrinsic or lightly doped silicon) covered up by a gate, which leads to a classic MOSFET-like structure. A MOSFET's current characteristic in the on-state follows the rule $I_{\text{ds}} \sim 1/L_{\text{ch}}$, so in case that a SBFET's channel is long, and the SB is conductive due to the applied gate voltage, the resistance of the internal channel MOSFET can get to the same order of magnitude than the SB's resistance. In this case, the characteristics in the SBFET's on-state is affected by the channel length. This effect needs to be considered, especially for RFETs, since those devices generally have a bigger footprint. For the SBFET's investigated in this work, it has been found that a channel resistance should be considered for devices with $L_{\text{ch}} > 1\,\mu\text{m}$. Figure 3.10 shows the transfer curve of the simulated 220 nm device at $V_{\text{ds}} = 2\,\text{V}$ (blue curve), compared to longer channel devices. It can be observed that, especially in the on-state the drain current reduction increases with longer channel lengths.

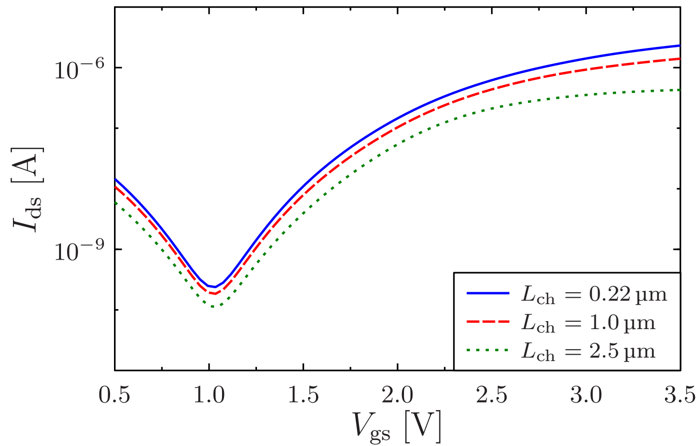


Figure 3.10: Single transfer curve of the simulated SBFET at the drain voltage $V_{\text{ds}} = 2\,\text{V}$, compared to simulated devices with increased channel lengths L_{ch}, showing the total drain currents I_{ds} in logarithmic scale. The used channel lengths are shown in the legend.

3.2.2.3 Temperature Dependencies

The FE current and especially the TE current of the SBFET are temperature dependent. Both current contributions are expected to increase with an increasing environmental temperature, however, due to the increasing phonon scattering events inside the transistors' channels, the semiconductor's conductivity also supposed to decrease with higher temperatures. Since the TE current in SBFETs is also a leakage current and the subthreshold swing reduces with lower temperatures, the usage of SBFETs at lower temperatures can be advantageous in some applications. In [11] a temperature study has been done by measuring a nanowire SBFET in a range of room temperature ($\vartheta = 300\,\text{K}$) down to deep cryogenic temperatures ($\vartheta = 5.5\,\text{K}$). A measured subthreshold swing reduction from 62 mV/dec. to 4.2 mV/dec. has been reported

[11]. The fact that SBFETs do not necessarily rely on doping and show good characteristics at deep cryogenic temperatures, make them a good candidate for electronic applications in this temperature environment. Both temperature regions (room temperature and deep cryogenic temperature) have been modeled in this work in Chapter 4 and Chapter 5, respectively. A TCAD studies of SBFETs at deep cryogenic temperatures is not done in this work, due to convergence issues of the simulations.

3.3 Reconfigurable Field-Effect Transistor Working Principle

The second type of device covered in this work is the RFET. More specific, this work mostly covers the dually gated RFET variation shown in [20]. It shall be noted here, that term RFET is ambiguous, because this term describes a device behavior (of being reconfigurable) and not a clear device structure. Some RFET variations are discussed in this section. In this work, unless specified otherwise, the term RFET refers to the dually gated variant described in Sec. 3.3.1 and that is mainly used in the modeling approach later. The band diagrams and characteristics shown in this section are created by using TCAD. The same device as in Sec. 3.2, but modified to a RFET, is used.

3.3.1 Structure of the Dually-Gated Reconfigurable Field-Effect Transistor

The basic idea of the dually gated RFET derives from the SBFET and extends that device in a certain way. Since a SBFET is mainly determined by the carrier injection over the transistor's SBs (if the channel resistance impact can be neglected), it is mandatory that the device's gate electrode covers the SBs themselves, but not necessarily the entire device channel. The (dually gated) RFET uses this SBFET property, by not having a single gate covering the entire channel, but having two gates, where each gate covers one SB. A schematic cross-section of such a RFET is shown in Fig. 3.11. The reconfigurability of the device is given by the property, that each gate can be biased independently, so it is a four-terminal device instead of having the usual three terminals. The source-side (injection-side) gate is called control gate (CG) and the drain-side is the program gate or polarity gate (PG). The device property of having an additional gate, in general, leads to a bigger device's footprint, because of the space requirement of this second gate and the necessity to contact it. However, the main achievement for this device is to increase the complexity of that single transistor, instead of just reducing a device's size.

3.3.2 Working Principle and Operations Modes

The two gates of the RFET differ in their purposes. The CG serves as the "regular" gate like for MOSFETs or SBFETs. It is biased in order to control the injection-side SB to steadily

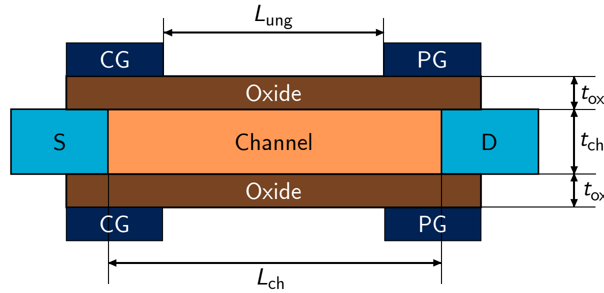


Figure 3.11: Schematic cross-section of a nanowire or double gate RFET with its geometric parameters.

determine the drain current flow. The second gate (PG) at the drain side is usually biased constantly, either positively or negatively. This sets the drain-side SB in a state where it is only passable by either electrons (in case it is biased positively) or holes (in case it is biased negatively), independent of the CG bias.

In Fig. 3.12 and Fig. 3.13, different operation modes of the RFET are shown. Figure 3.12 shows the p-type configuration, where the program gate voltage V_{pg}, as well as the drain voltage V_{ds} are smaller than zero volt. In this configuration, the PG's SB is only passable by holes. Figure 3.12(b) shows the device's off-state, caused by a control gate voltage of $V_{\mathrm{cg}} = 0\,\mathrm{V}$. In this state, neither electrons nor holes can be injected at the source side SB, besides a small leakage current. An increasing negative CG voltage leads to the on-state in p-type mode. This is shown in Fig. 3.12(a), where holes can pass both SBs and flow from source to drain. In the third case, starting from a CG voltage of $V_{\mathrm{cg}} = 0\,\mathrm{V}$ and increasing the voltage would have led to the ambipolar state, if the device was a SBFET. However, due to the RFET's negatively biased PG, shown in Fig. 3.12(c), electrons are blocked by the drain-side SB and an ambipolar current is suppressed. In this state the current is even lower than in the $V_{\mathrm{pg}} = 0\,\mathrm{V}$ state, because in this opposite polarity mode of CG and PG each gate suppresses one type of carrier. The result of the described p-type operation mode is shown as transfer curve in Fig. 3.14(i) with references to the discussed band diagrams shown in the figure.

The n-type configuration of the RFET works similarly and is shown in Fig. 3.13. In this case V_{pg} and V_{ds} are bigger than zero volt and only an electron current flow is possible through the device. Figures 3.13(a) and 3.13(b) show the device's off-state, because in these states the CG voltage does not fit to the PG's voltage. By increasing the CG voltage, device switches on, which is shown in Fig. 3.13(c). In this state, electrons can pass both SBs and flow from source to drain. A transfer curve of the n-type characteristics is shown in Fig. 3.14(ii), which also shows the references to the states of Fig. 3.13. The output characteristics of the device in p-type operation mode ($V_{\mathrm{ds}} < 0\,\mathrm{V}$) is not shown at this point, since it shows similar effects as the n-type characteristics, but with negative voltages and drain current.

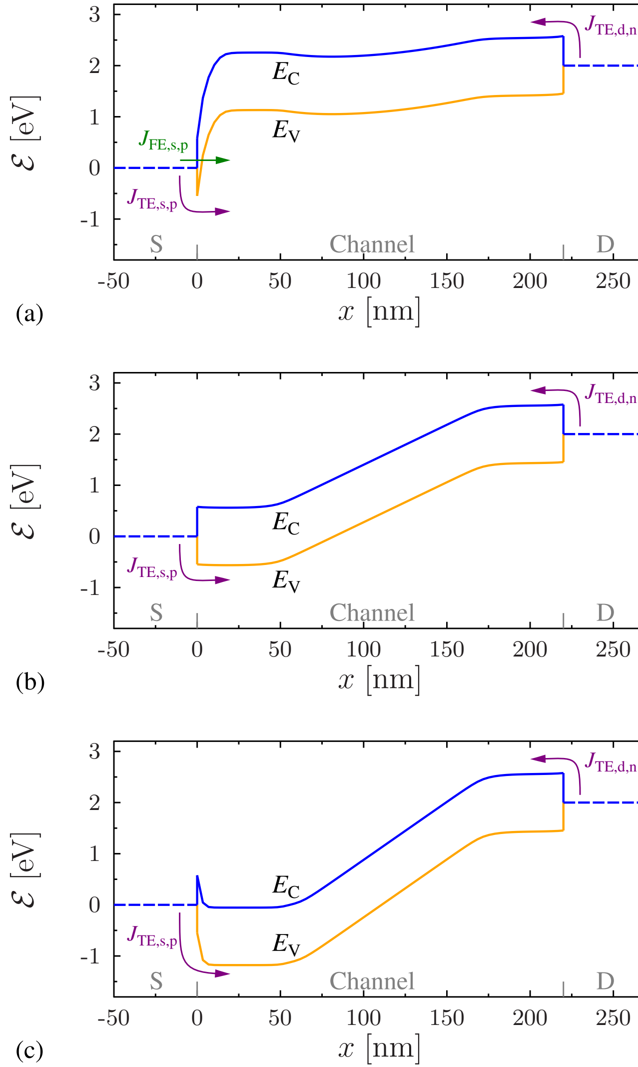


Figure 3.12: Various operations modes of a RFET in p-type operation mode, with $V_{pg} = V_{ds} = -2\,V$. (a) shows the on-state of the transistor with $V_{cg} = -2\,V$. (b) and (c) show the off-state regions of the device with $V_{cg} = 0\,V$ and $V_{cg} = 2\,V$, respectively. In these states the source-side injection current is blocked by the CG and the drain-side injection current is blocked by the PG.

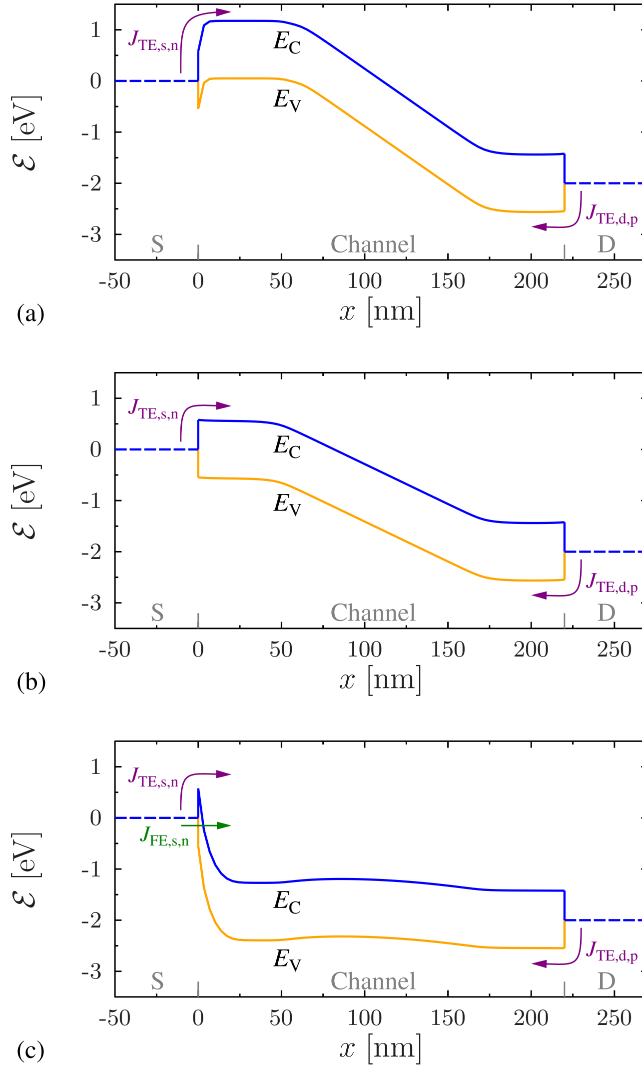
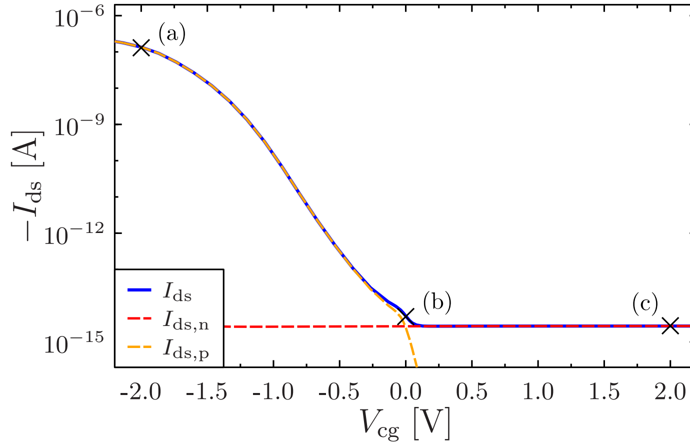
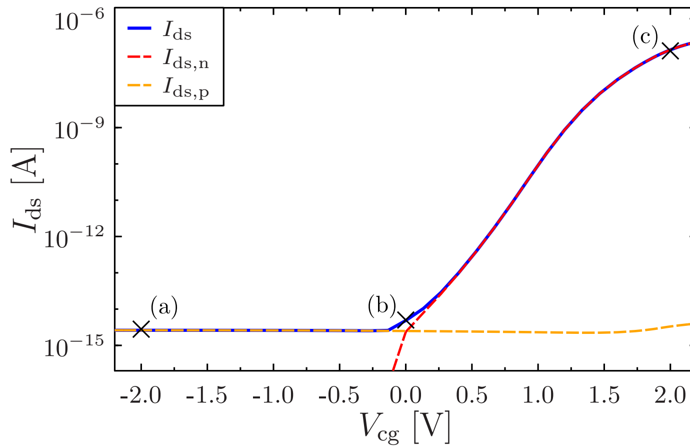


Figure 3.13: Various operations modes of a RFET in n-type operation mode, with $V_{pg} = V_{ds} = 2\,V$. (a) and (b) show the off-state regions of the device with $V_{cg} = -2\,V$ and $V_{cg} = 0\,V$, respectively. In these states the source-side injection current is blocked by the CG and the drain-side injection current is blocked by the PG. (c) shows the on-state of the transistor with $V_{cg} = 2\,V$



(i)



(ii)

Figure 3.14: Single transfer curve of the simulated RFETs at the different operation modes, showing the total drain current I_{ds}, as well as the electron ($I_{ds,n}$) and hole ($I_{ds,p}$) current components in logarithmic scale. (i) shows one curve at p-type operation mode, with $V_{pg} = V_{ds} = -2\,V$. The markers (a), (b) and (c) refer to the bias conditions at which the band diagrams of Fig. 3.12 are captured. (ii) shows one curve at n-type operation mode, with $V_{pg} = V_{ds} = 2\,V$. The markers (a), (b) and (c) refer to the bias conditions at which the band diagrams of Fig. 3.13 are captured.

The discussed operation modes of the RFET enable a configurability of the device as either p-type or n-type transistor. This is also schematically demonstrated in Fig. 3.15. This reconfigurability can be used, for example, to create at runtime switchable logic circuits, as described in [21, 22].

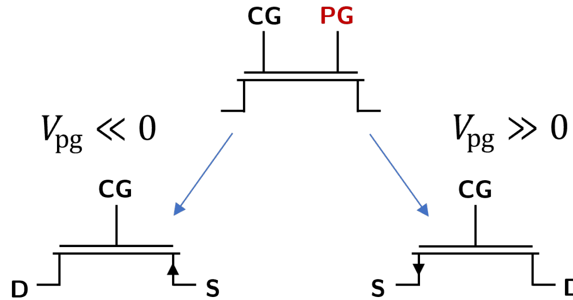


Figure 3.15: Schematic demonstration of the RFET being substituted to either a p-type transistor in case of $V_{pg} \ll 0\,V$ or n-type transistor in case of $V_{pg} \gg 0\,V$.

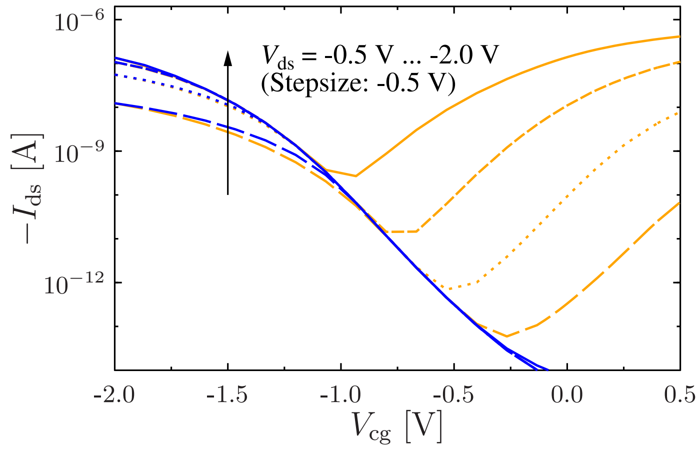
3.3.2.1 Device Characteristics

Compared to SBFET's characteristics, the RFET has no ambipolar current. This leads to an improved on/off ratio of the device and a drain voltage independent off-state position on the V_{gs} (or rather V_{cg}) axis. For further demonstration, Fig. 3.16 shows that comparison. The transfer characteristics of the simulated device is shown with a fixed PG voltage (blue lines) and in case that $V_{pg} = V_{cg}$ (orange lines). That second case leads to a SBFET-like behavior of the RFET, since both gates have the same bias then as it was one single gate. Figure 3.16(a) shows the characteristics for p-type and (b) for n-type operation mode.

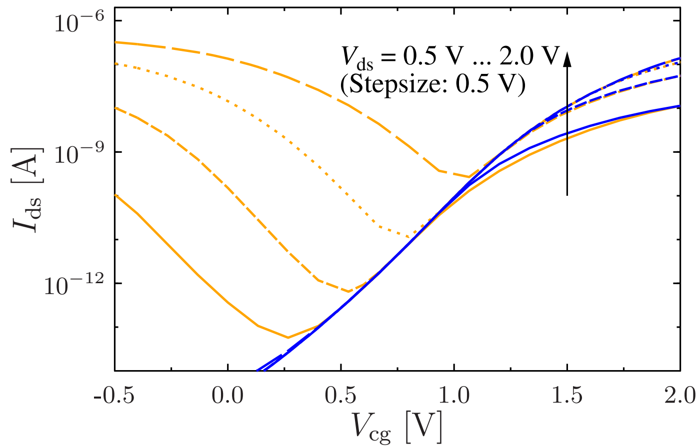
Finally, a part of the n-type mode output characteristics is shown in Fig. 3.17. These characteristics correspond to the lower voltage output characteristics of the SBFET, shown in Fig. 3.8(a). The difference in Fig. 3.17 is that the RFET is programmed to the n-type operation mode with $V_{pg} = 2\,V$, which leads to a suppression of the ambipolar current contributions from Fig. 3.8(a). The characteristics for higher V_{cg} are not shown, because there is no difference compared to the results of Fig. 3.8(b).

3.3.2.2 Gate-to-Gate Distance

In general, RFETs have a bigger footprint than SBFETs, because they need at least two independent gates covering the transistor's channel. This results in an ungated region between the CG and the PG, which further reduces the electrostatic coupling of the two gates on the device's ungated channel. Figure 3.18 shows the simulation results for the accumulated electrons directly along the semiconductor-oxide interface. The first kink in the results (between



(a)



(b)

Figure 3.16: Transfer characteristics of the simulated RFET at the given drain voltages showing the total drain current I_{ds} in logarithmic scale. The blue lines show the device in fixed programmed state with a constant V_{pg}. The orange lines show the device characteristics with $V_{pg} = V_{cg}$, similarly used as a SBFET (see Fig. 3.7). (a) shows the p-type operation mode with negative drain-voltages, a negative scaled y-axis and $V_{pg} = -2\,V$ for the blue curves. (b) shows the n-type operation mode with positive drain-voltages and $V_{pg} = 2\,V$ for the blue curves.

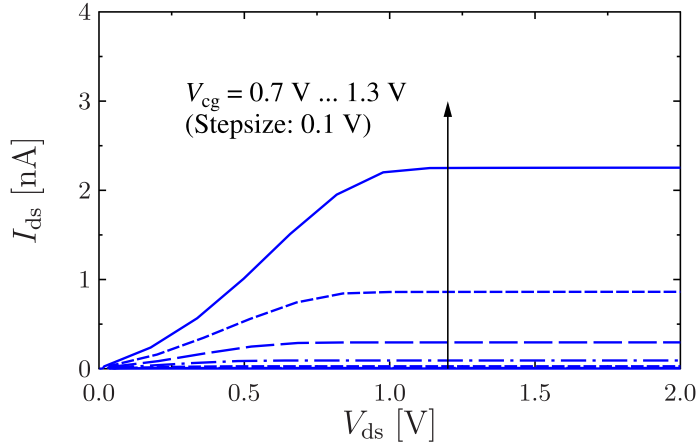


Figure 3.17: Output characteristics of the simulated RFET at the given CG voltages and at $V_{pg} = 2$ V (n-type operation mode) showing the total drain current I_{ds} in linear scale.

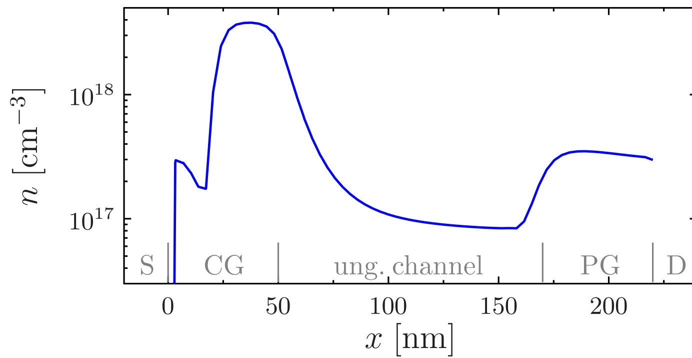


Figure 3.18: Electron density n along the simulated RFET's channel-oxide interface at $V_{ds} = V_{pg} = V_{cg} = 2$ V (n-type operation mode) in logarithmic scale. The gray labels show the different regions inside the device. The results of the first 20 nm (especially the first kink) are incorrect, which is caused by the TCAD tunneling model, and can be ignored [28].

0 nm and 20 nm) is caused by the simulation specific tunnel generation rate and can be ignored [28]. For a device with one continuous gate, a nearly uniform distribution of the accumulated charges, dropping towards the drain side, would be expected. In case of the simulated RFET, the biggest drop in the carrier concentration is inside the ungated region, which is caused by the worse electrostatic coupling, and which leads to less electrons available for the current transport. This effect needs to be considered in the compact model and is discussed in Sec. 6.1.2.

3.3.3 Other RFET Structures and Concepts

There are several possible RFET structures based on the SB injection besides the dually-gated version, which is the mainly used structure in this work. A good overview of the technology and the structures can be found in [19]. Figure 3.19 shows two example RFET variations besides the dually-gated variant.

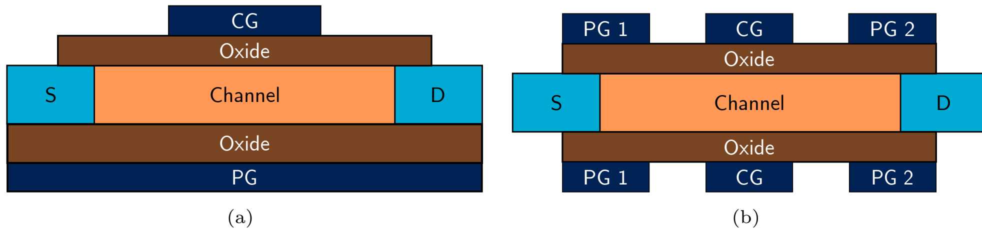


Figure 3.19: Examples of other RFET variations as schematics, according to [19]. (a) shows a top gate / bottom gate RFET. (b) shows a Three gate RFET.

The first variation is the top gate / bottom gate RFET shown in Fig. 3.19(a). The top of this device is similar to a SBFET, but it comes with an additional bottom gate below the substrate, which is used as PG. This structure is not feasible with GAA nanowire structures but can be manufactured e.g. as silicon-on-insulator (SOI) technology, where the PG is located underneath the substrate [19]. The advantage of this structure is the reduced length demand in the channel length direction of the transistor, since only one gate has to be deposited on top of the device. One disadvantage of the device is the demand for a much higher PG voltage since the electrostatic coupling of the PG to the SBs is worse in this structure.

The second variation, shown in Fig. 3.19(b), is the three-gate RFET. This device has its PG split up into two PGs, each covering one SB of the device, while the CG is located in the middle of the channel. The advantage of this structure is that the two PGs can be biased individually, leading to a three independent gates RFET (TIG-RFET), which further enhances the functionality of the single transistor. For example, the TIG-RFET can change some device parameter (like the threshold voltage or subthreshold swing), by just changing the biased gates. A disadvantage of this device is the increased device footprint, compared to the dually gated RFET, since the three gated variant needs to have all three gates integrated in the device structure side by side.

There are many other RFET concepts discussed in research. In [69–71] various RFET structures based on alternative materials are discussed, like Aluminum-Silicon junctions for the SBs, or germanium / germanium-silicon compound as semiconductor, demonstrating symmetric RFET characteristics. The concept of RFETs based 2D materials (e.g. black phosphorus or molybdenum disulfide) are discussed in [15, 16, 72, 73]. It shall be noted that most of the mentioned technologies are beyond the scope of this modeling work.

UNIVERSITAT ROVIRA I VIRGILI
COMPACT MODELING OF SCHOTTKY BARRIER AND RECONFIGURABLE FIELD-EFFECT TRANSISTORS
Christian Römer

3.4 State-of-the-Art Compact Models

This section shortly describes and reviews several compact models for SBFETs or RFETs.

The first model presented in this section is a DC compact model developed for DG SBFETs and published in [30, 62, 74]. This model is the basis of the room temperature SBFET / RFET model, which is derived in Chapter 4 and Chapter 6, so its derivation is part of Sec. 4.2.1. It is based on the FE current model approach of Sze, Chang, and Crowell from Sec. 2.3.3.2, as well as the TE model from Sec. 2.4.2.1, and it uses the described 2D potential model, introduced in Sec. 2.1.5.

In [75] a DC compact drain current model is introduced which specifically models the behavior of a RFET with three gate terminals, like those shown in Fig. 3.19(b). As a simplification of the tunneling current calculation, this model uses an effective SB height, similar to suggestions in [6]. In order to obtain the total device current, this model numerically combines the injection current over the SB with the drift-diffusion current controlled by the central gate, which is not efficient for circuit simulation.

A similar model is proposed in [76] where the injection current of a dually-gated RFET is calculated by using an effective SB height and the TE current contribution. This model also uses a numerical approach to combine the injection and the channel current contributions.

The DC model from [77] is made for the three gate RFET. This model specifically focuses on an effect called impact ionization and uses this effect to calculate the RFET's drain current. This model shows the dependency of the device's subthreshold slope to the applied drain-source voltage, caused by the described impact ionization. However, this model uses several empirical parameters to obtain a closed-form equation and it strictly relies on the impact ionization effect.

The work of [78] presents a model which focuses on the potential calculation inside dually-gated RFETs and its current calculation is based on the approach from Kane [79]. The model is used for comparison to TCAD results.

In the work of [80] the behavior of logic-gates based on RFETs is investigated, especially regarding their power consumption and time responses. For this investigation, some standard MOSFET equations are fitted to measured data. This procedure allows the investigation of characteristic parameters for various circuit concepts but cannot be used for exact circuit simulation with a continuous voltage range.

CHAPTER 4

Compact Modeling of Schottky Barrier Field-Effect transistors

This chapter describes the modeling approach of the compact model for SBFETs in detail which has been published in [81–83]. The presented closed-form and physics-based DC compact model is applicable on DG SBFETs and tested at room temperature environment ($\vartheta \approx 300\,\mathrm{K}$). It needs the device's geometric and material parameters as model inputs, as well as some fitting parameters and the applied bias conditions. With the described input parameters, the model calculates the device's DC-current by performing the following steps:

- The potential inside of the device's channel is calculated, in order to reconstruct the band diagram in that region. (See Sec. 4.1)
- The current components at the source-side SB are calculated by using the reconstructed potential / band diagram at the SB. The current components consist of the TE-current (charge-carriers overcoming the SB) and FE-current (charge-carriers tunneling through the SB). (See Sec. 4.2)
- By adding both current types and using a balancing model, the total injection current of the device is calculated. (See Sec. 4.3)
- As an addition for devices with a non-negligible channel resistance (long-channel devices) a MOSFET equation is used in order to limit the current and the channel resistance current is combined with the SB injection current. (See Sec. 4.4)

In the upcoming sections 4.1 to 4.4 the modeling approach is explained in detail. Finally, Sec. 4.5 shows and discusses some results of the model, compared to TCAD simulations.

4.1 Potential Model Simplification and Band Diagram Reconstruction

Section 2.1 introduces a 2D analytical closed-form potential model based on the nonlinear transformation method by Schwarz and Christoffel and applicable on 2D double gate FET-structures. In a first step, the electrostatic potential in the device's channel region is calculated

and thereto the band diagram and the electric field close to the junctions. The determination of the potential is split into two steps. First, an adapted version of the 2D analytical closed-form potential model, described in Sec. 2.1.5, is used to calculate the electrostatic potential at some auxiliary points close to the Schottky junctions and in the middle of the channel. This model uses the SCT method to calculate the potential inside a DG FET structure, like the one shown in Fig. 3.1(a) [29, 31]. However, this potential model does not consider accumulated charges in the channel at higher gate-source voltages $V_{\rm gs}$.

4.1.1 Effective Gate-Source Voltage

In order to increase the accuracy of this calculation even for higher $V_{\rm gs}$, an effective gate-source voltage $V_{\rm gs,eff}$ is calculated, which shall include the effect of accumulated charges in the device's channel. There are two methods that have been proven as useful in different cases, depending on the channel length, or rather depending on the inclusion of the channel resistance model introduced in Sec. 4.4.

$V_{\rm gs,eff}$ for short channel devices

For the shorter channel devices, the effective gate-source voltage $V_{\rm gs,eff,TFET}$ is adapted, according to the model from Sec. 2.1.6, which is used in the tunnel field-effect transistor model from [32, 33]. However, compact model comparisons to measurements and TCAD simulations showed that $V_{\rm gs,eff} = V_{\rm gs,eff,TFET}$ (see Eq. (2.38)) is not fully applicable on the tested SBFET devices for all used bias conditions. Therefore, an empirical equation was included, given by

$$V_{\rm gs,eff} = \left[\alpha \cdot V_{\rm gs,eff,TFET} + (1-\alpha) \cdot (V_{\rm gs} - V_{\rm fb})\right], \tag{4.1}$$

where α is a fitting parameter to increase or reduce the effect of the $V_{\rm gs,eff}$ saturation and $V_{\rm fb}$ is the flatband voltage which is defined by the gate materials work function and compensates the band bending at $V_{\rm gs} = 0\,\rm V$.

$V_{\rm gs,eff}$ for long channel devices

In case of longer channel lengths and the inclusion of the channel resistance, it has been found that the $V_{\rm gs,eff}$-calculation from Eq. (4.1) does not lead to a sufficient solution. Therefore, a set of empirical equations have been implemented, dependent on the gate-source and drain-source voltage, given as:

$$V_{\rm limit} = \left[\exp(V_{\rm ds} \cdot 1\,\rm V^{-1}) - 1\right] \cdot 1\,\rm V + V_{0,\rm limit}, \tag{4.2}$$

and:

$$V_{\mathrm{gs,eff}} = \frac{V_{\mathrm{limit}}}{\sqrt[\gamma_{\mathrm{Vg,eff}}]{1 + \left(\frac{V_{\mathrm{limit}}}{V_{\mathrm{gs}}}\right)^{\gamma_{\mathrm{Vg,eff}}}}}. \tag{4.3}$$

V_{limit} marks a drain-source voltage dependent limiting point towards which the effective gate voltages saturate in case the applied gate voltages are getting high compared to the drain-source voltage. The parameters $V_{0,\mathrm{limit}}$ and $\gamma_{\mathrm{Vg,eff}}$ are empirical fitting parameters which are used to control the behavior of the drain current, mainly in the region of $V_{\mathrm{gs}} > V_{\mathrm{ds}}$.

4.1.2 Potential Simplification

Using the effective gate-source voltage $V_{\mathrm{gs,eff}}$ from either Eq. (4.1) or Eq. (4.3) and the applied drain-source voltage V_{ds}, the 2D potential can be calculated by Eq. (2.37). The obtained potential $\Phi_{\mathrm{2D}}(x,y)$ can be calculated for each point inside the SBFET's channel, but there are only few regions which are interesting for the injection current calculation.

For the y-coordinate (gate-to-gate direction), there are two values of interest, which are the surface potential and the center potential. The surface potential, given as

$$\Phi_{\mathrm{sur}}(x) = \Phi_{\mathrm{2D}}(x,y=0)\,, \tag{4.4}$$

is located along the oxide-semiconductor interface of one gate. This potential is especially of interest in the transistor's on-state at high V_{gs}, since this potential is mostly affected by band bending. The center potential, given as

$$\Phi_{\mathrm{cen}}(x) = \Phi_{\mathrm{2D}}(x,y=t_{\mathrm{ch}}/2)\,, \tag{4.5}$$

is located in the middle of the channel and is used mainly for the off-state current. It shall be mentioned that in a DG device structure there is a second surface potential along the second gate's oxide-semiconductor interface at $y = t_{\mathrm{ch}}$. However, due to the device symmetry this potential is equal to the other surface potential $\Phi_{\mathrm{sur}}(x) = \Phi_{\mathrm{2D}}(x,y=0) = \Phi_{\mathrm{2D}}(x,y=t_{\mathrm{ch}})$, so this potential does not have to be calculated again.

For the x-coordinate (drain-to-source direction), the interesting regions to calculate the potential are close to the source and drain-side SBs, as well as the center of the device in x-direction. The center in x-direction is estimated to be at least affected by the source and drain potentials and therefore, the potential at this position is mostly determined by V_{gs}. These potentials can be calculated as surface potential:

$$\Phi_{\mathrm{sur,L/2}} = \Phi_{\mathrm{sur}}(x = L_{\mathrm{ch}}/2)\,, \tag{4.6}$$

and as center potential:

$$\Phi_{\mathrm{cen,L/2}} = \Phi_{\mathrm{cen}}(x = L_{\mathrm{ch}}/2)\,. \tag{4.7}$$

The potentials close to the transistor's SBs are used to describe the form of the SB. For the source-side SB the potential directly at the Schottky junction is used as:

$$\Phi_{\mathrm{cen,S1}} = \Phi_{\mathrm{cen}}(x = 0)\,, \tag{4.8}$$

and a second auxiliary potential is calculated slightly inside the channel, as:

$$\Phi_{\mathrm{cen,S2}} = \Phi_{\mathrm{cen}}(x = \Delta x)\,. \tag{4.9}$$

The second point is needed for the upcoming simplification of the potential. For the drain-side SB the potentials are calculated similarly, as:

$$\Phi_{\mathrm{cen,D1}} = \Phi_{\mathrm{cen}}(x = L_{\mathrm{ch}})\,, \tag{4.10}$$

and

$$\Phi_{\mathrm{cen,D2}} = \Phi_{\mathrm{cen}}(x = L_{\mathrm{ch}} - \Delta x)\,. \tag{4.11}$$

With the same procedure the corresponding surface potentials are calculated as:

$$\Phi_{\mathrm{sur,S1}} = \Phi_{\mathrm{sur}}(x = 0)\,, \tag{4.12}$$

$$\Phi_{\mathrm{sur,S2}} = \Phi_{\mathrm{sur}}(x = \Delta x)\,, \tag{4.13}$$

$$\Phi_{\mathrm{sur,D1}} = \Phi_{\mathrm{sur}}(x = L_{\mathrm{ch}})\,, \tag{4.14}$$

and:

$$\Phi_{\mathrm{sur,D2}} = \Phi_{\mathrm{sur}}(x = L_{\mathrm{ch}} - \Delta x)\,. \tag{4.15}$$

With the auxiliary points from Eq. (4.8) to Eq. (4.15), similar to [32], in a second step a compact analytical expression (φ_{comp}) for the potential along the channel is introduced:

$$\varphi_{\mathrm{comp}}(x) = \frac{k}{x - l} + m\,. \tag{4.16}$$

This expression is evaluated at the oxide-channel interface for each Schottky junction (source and drain), where the x-direction is the source-drain direction. The parameters k, l and m are reconstructed by using the auxiliary potentials $\varphi_{\mathrm{comp}}(0) = \Phi_{\mathrm{sur,S1}}$, $\varphi_{\mathrm{comp}}(\Delta x) = \Phi_{\mathrm{sur,S2}}$ and $\varphi_{\mathrm{comp}}(L_{\mathrm{ch}}/2) = \Phi_{\mathrm{sur,L/2}}$. For the reconstruction, a value of $\Delta x \approx 10\,\mathrm{nm}$ has shown to be useful. With this expression for the compact potential, it is possible to calculate the electric field in x-direction along the channel by

$$E_{\mathrm{x}}(x) = -\frac{d\varphi_{\mathrm{comp}}(x)}{dx} = \frac{k}{(x - l)^2}\,. \tag{4.17}$$

and the band diagram by adding or subtracting the band parameters $\Phi_{\mathrm{B,n}}$ or $\Phi_{\mathrm{B,p}}$. Figure 4.1(b) shows the 2D analytical closed-form potential model as well as the compact potential compared

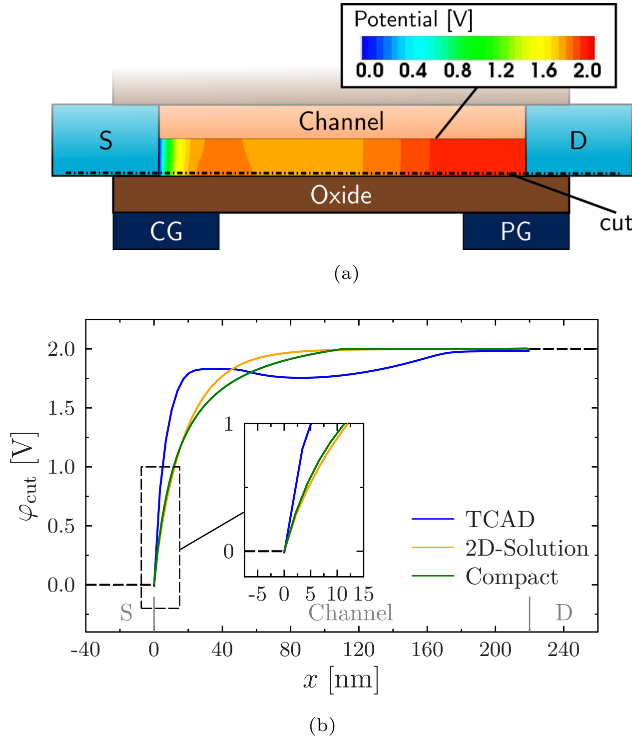


Figure 4.1: Electrostatic potential of the device from Sec. 3.3 at $V_{\mathrm{ds}} = V_{\mathrm{pg}} = V_{\mathrm{cg}} = 2\,\mathrm{V}$. (a) device structure with the simulated 2D potential along the channel. The 2D potential was simulated using TCAD Sentaurus. (b) potential along the cut line shown in (a) and comparison of the TCAD simulated value (blue) to the result of the 2D analytic closed-form potential model (orange) and the compact potential solution (green) from Eq. (4.16). The dashed box shows a zoom of the potential at the SB. Although, the shown device is a RFET, the potential at the SB of a SBFET looks similarly.

to TCAD Sentaurus simulations at the given bias conditions for the device from Sec. 3.3. The shown transistor is a RFET, but the SBFET's potential directly at the SB looks similarly. This comparison shows that both potential models have a deviation compared to the TCAD simulation between the source-channel junction and the control gate, which is most likely caused by the influence of the accumulated charges in the channel at the given bias condition, due to their empirical consideration. However, the most important part is close to the source-channel junction in order to estimate the SB thickness correctly for the tunneling process. In this region the potentials calculated by the compact model show an acceptable agreement to the TCAD simulation.

4.2 Injection Current Modeling Approach

Unlike in MOSFET application where the device behavior is dominated by the charge-carrier accumulation in a device's channel, the main current blocking / controlling mechanism in SBFETs is the injection-side SB. In this section, the compact modeling approaches of both injection current sources, FE (Sec. 4.2.1) and TE (Sec. 4.2.2) are introduced. The model derivation in this section is done for the injection of electrons but works similarly for holes.

4.2.1 Field Emission Injection Current

The FE current is given by charge carriers tunneling through the SBs. For this case the bands have to be sufficiently bent so the thickness of the barrier becomes small enough, as it is shown in the left part of Fig. 4.2. In order to find a way to describe the FE current density (J_{FE}) analytically, an approach from [30] is used, which is based on the approach from Sec. 2.3.3.2. In this approach the equation:

$$J_{\mathrm{FE}} = \frac{q\mu_{\mathrm{tn}}N_{\mathrm{C}}}{k_{\mathrm{b}}\vartheta} \cdot \int\limits_{\mathcal{E}_{\min}}^{\mathcal{E}_0} f_{\mathrm{m}}(\mathcal{E})[1 - f_{\mathrm{ch}}(\mathcal{E})] \times |\vec{E}(\mathcal{E})| \cdot T(\mathcal{E}) \cdot d\mathcal{E}\,, \tag{4.18}$$

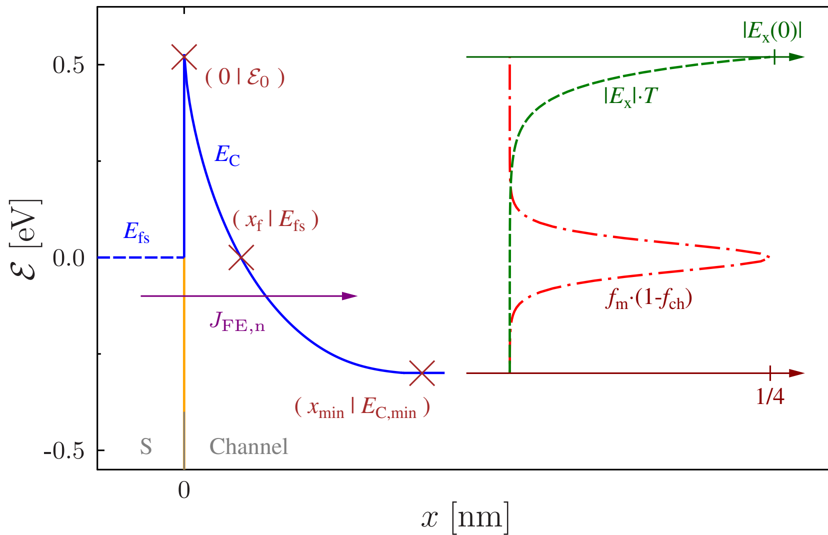


Figure 4.2: Visualization of the tunneling equation components at the source-side SB for tunneling of electrons. The figure shows some important variables of the compact model, as well as the components of Eq. (4.18) as a function of the energy $\mathcal{E}$, which are the electric field multiplied with the tunneling probability (green) and the product of the Fermi functions (red).

that describes the tunneling process through the SB is used as a calculation basis [30]. In this equation q is the elementary charge, N_{C} is the effective density of states in the conduction band (for tunneling holes the effective density of states in the valence band N_{V} is used), k_{b} is the Boltzmann constant and ϑ is the temperature. The tunneling mobility μ_{tn} for electrons (or μ_{tp} for holes) is used as an adjustable fitting parameter of the model, which is part of Eq. (4.18), because this equation combines tunneling with drift-diffusion effects. The first part of the integral in Eq. (4.18) is the product of the Fermi functions and represents the occupation probability $f_{\mathrm{m}}(\mathcal{E})$ for electrons in the source region at energy $\mathcal{E}$ and $[1 - f_{\mathrm{ch}}(\mathcal{E})]$ for holes in the channel region [6, 30].

The problem with Eq. (4.18) for a compact model is the integral which contains the product of the Fermi distribution functions in the metal $f_{\mathrm{m}}(\mathcal{E})$ and in the channel $f_{\mathrm{ch}}(\mathcal{E})$, as well as the tunneling probability $T(\mathcal{E})$ and the electric field $|\vec{E}(\mathcal{E})|$. In Eq. (2.65) a possibility is shown which can be used to calculate the tunneling probability through triangular barriers, which is a good approximation for SBs. However, due to the general form of this equation it cannot be solved analytically in an integral. Therefore, following the proposal of [30], Eq. (4.18) is approximated by a similar approach, as:

$$J_{\mathrm{FE}} \approx \frac{q\mu_{\mathrm{tn}}N_{\mathrm{C}}}{k_{\mathrm{b}}\vartheta} \cdot \int\limits_{\mathcal{E}_{\mathrm{min}}}^{\mathcal{E}_0} \frac{1}{4}\exp\left(-\frac{a}{\gamma_{\mathrm{n}}}(\mathcal{E} - E_{\mathrm{f,n}})^2\right) \times b \cdot \exp(-c(\mathcal{E}_0 - \mathcal{E})) \cdot d\mathcal{E} \,. \tag{4.19}$$

In the approximation from Eq. (4.19) the first part of the integral is replaced by a Gaussian distribution shaped function $1/4 \cdot \exp(-a/\gamma_{\mathrm{n}}(\mathcal{E} - E_{\mathrm{f,n}})^2)$, where $E_{\mathrm{f,n}}$ is the quasi Fermi energy level for electrons [30]. It is estimated in this approach that the device is in the on-state and the injection-side SB is highly conductive, leading to almost no change in the quasi Fermi level for electrons $E_{\mathrm{f,n}}$ through the SB. This results in $f_{\mathrm{m}}(\mathcal{E}) \approx f_{\mathrm{ch}}(\mathcal{E})$, which leads to a maximum of the product $f_{\mathrm{m}}(\mathcal{E})[1 - f_{\mathrm{ch}}(\mathcal{E})]$ at $\mathcal{E} = E_{\mathrm{f,n}}$. This maximum of 1/4 is represented in Gaussian part of Eq. (4.19). The second part of the integral in Eq. (4.18) is the electric field multiplied with the tunneling probability $|\vec{E}(\mathcal{E})| \cdot T(\mathcal{E})$, which is approximated by an exponential function $b \cdot \exp(-c(\mathcal{E}_0 - \mathcal{E}))$ in Eq. (4.19).

The Fermi energy level $E_{\mathrm{f,n}}$ that is used for the tunneling calculation is equal to the Fermi level of the (source-side) metal E_{fs}. The x-position where the bent conduction band E_{C} (or the valence band E_{V} in case of tunneling holes) reaches the metal's Fermi level is called x_{f}. This position is estimated to have the highest FE-current contribution per energy level, as shown in Fig. 4.2. The relation between $E_{\mathrm{f,n}}$ and x_{f} is expressed by using Eq. (4.16), as:

$$E_{\mathrm{f,n}} = -q \cdot \varphi_{\mathrm{comp}}(x_{\mathrm{f}}) + q \cdot \Phi_{\mathrm{B,n}} \,, \tag{4.20}$$

in case of tunneling of electrons where the conduction band is bent below $E_{\mathrm{f,n}}$. For tunneling of

holes the valence band is relevant for the tunneling process and $-q \cdot \Phi_{\mathrm{B,p}}$ is used in Eq. (4.20) instead of $+q \cdot \Phi_{\mathrm{B,n}}$. If the conduction band is not bent below the metal's Fermi level, x_{f} will be limited to $L_{\mathrm{ch}}/2$.

The upper boundary of the integrals ($\mathcal{E}_0$) is the highest energy value where tunneling can occur, which is the top of the SB (see also $\mathcal{E}_0$ in Fig. 4.2). The lower limit of the integrals in Eq. (4.18) and Eq. (4.19) is positioned in the middle of the channel, so it can be expressed as:

$$\mathcal{E}_{\min} = -q \cdot \Phi_{\mathrm{sur,L/2}} + \frac{E_{\mathrm{g}}}{2}\,. \tag{4.21}$$

This lower boundary is the lowest energy value where tunneling charge carriers are theoretically possible. However, due to the increasing tunneling lengths, the tunneling current contributions lower than $E_{\mathrm{f,n}}$ are decreasing rapidly, so that $\mathcal{E}_{\min}$ is a formal minimum.

The parameters a, b and c of Eq. (4.19) are energy independent coefficients, which are reconstructed similar as shown in [30]. For parameter a, the integral over the Fermi function product of Eq. (4.18) and the integral over the Gaussian function of Eq. (4.19) are set equal to achieve a normalization between the two parts. This is given by:

$$\int_{-\infty}^{\infty} f_{\mathrm{m}}(\mathcal{E})[1 - f_{\mathrm{ch}}(\mathcal{E})]d\mathcal{E} = \int_{-\infty}^{\infty} \frac{1}{4}\exp\left(-\frac{a}{\gamma_{\mathrm{n}}}(\mathcal{E} - E_{\mathrm{f}})^2\right) d\mathcal{E}\,. \tag{4.22}$$

The left-hand side of Eq. (4.22) can be solved with the mentioned approximation $f_{\mathrm{m}}(\mathcal{E}) \approx f_{\mathrm{ch}}(\mathcal{E})$ as:

$$\int_{-\infty}^{\infty} f_{\mathrm{m}}(\mathcal{E})[1 - f_{\mathrm{ch}}(\mathcal{E})]d\mathcal{E} = \int_{-\infty}^{\infty} \frac{d\mathcal{E}}{2 + \exp\left(\frac{\mathcal{E}-E_{\mathrm{f,n}}}{k_{\mathrm{b}}\vartheta}\right) + \exp\left(-\frac{\mathcal{E}-E_{\mathrm{f,n}}}{k_{\mathrm{b}}\vartheta}\right)}\,, \tag{4.23}$$

with the substitution u, given as:

$$u = \frac{\mathcal{E} - E_{\mathrm{f,n}}}{k_{\mathrm{b}}\vartheta},\ \frac{du}{d\mathcal{E}} = \frac{1}{k_{\mathrm{b}}\vartheta}\,, \tag{4.24}$$

to:

$$\int_{-\infty}^{\infty} f_{\mathrm{m}}(\mathcal{E})[1 - f_{\mathrm{ch}}(\mathcal{E})]d\mathcal{E} = k_{\mathrm{b}}\vartheta \cdot \int_{-\infty}^{\infty} \frac{\exp(u)}{(\exp(u)+1)^2} du \tag{4.25}$$

$$= k_{\mathrm{b}}\vartheta \cdot \left[-\frac{1}{\exp(u)+1}\right]_{-\infty}^{\infty} = k_{\mathrm{b}}\vartheta\,. \tag{4.26}$$

The right-hand side of Eq. (4.22) can be solved by a substitution z, which is given as:

$$-\frac{1}{2}z^2 = -\frac{a}{\gamma_{\mathrm{n}}}(\mathcal{E} - E_{\mathrm{f,n}})^2,\ \frac{dz}{d\mathcal{E}} = \sqrt{2\frac{a}{\gamma_{\mathrm{n}}}}\,. \tag{4.27}$$

The right-hand side of Eq. (4.22) with Eq. (4.27) lead to a standard normal distribution in z-space. This can be solved as:

$$\frac{1}{4}\int_{-\infty}^{\infty} \exp\left(-\frac{a}{\gamma_{\mathrm{n}}}(\mathcal{E}-E_{\mathrm{f,n}})^2\right) d\mathcal{E} = \frac{\sqrt{\gamma_{\mathrm{n}}}}{4\cdot\sqrt{2a}} \cdot \int_{-\infty}^{\infty} \exp\left(-\frac{1}{2}z^2\right) dz \tag{4.28}$$

$$= \frac{1}{4}\cdot\sqrt{\frac{\gamma_{\mathrm{n}}\cdot\pi}{a}}\,. \tag{4.29}$$

Using the results Eq. (4.25) and Eq. (4.28) in Eq. (4.22), leads to the expression:

$$k_{\mathrm{b}}\vartheta = \frac{1}{4}\cdot\sqrt{\frac{\gamma_{\mathrm{n}}\cdot\pi}{a}}\,, \tag{4.30}$$

so, a can be given, as:

$$a = \gamma_{\mathrm{n}}\cdot\frac{\pi}{16\cdot(k_{\mathrm{b}}\vartheta)^2}\,. \tag{4.31}$$

For obtaining the coefficients b and c, the exponential parts of Eq. (4.18) and Eq. (4.19) are set equal at the two different prominent energy levels $\mathcal{E}_0$ and $E_{\mathrm{f,n}}$:

$$|\vec{E}(\mathcal{E})|\cdot T(\mathcal{E})\Big|_{\mathcal{E}=\mathcal{E}_0,E_{\mathrm{f,n}}} = b\cdot\exp(-c(\mathcal{E}_0-\mathcal{E}))\Big|_{\mathcal{E}=\mathcal{E}_0,E_{\mathrm{f,n}}}\,. \tag{4.32}$$

For $\mathcal{E}=\mathcal{E}_0$, Eq. (4.32) becomes:

$$|\vec{E}(\mathcal{E}_0)|\cdot T(\mathcal{E}_0) = b\cdot\exp(-c\cdot 0) = b\,. \tag{4.33}$$

By considering that $T(\mathcal{E}_0)$ is the tunneling probability directly at the top of the SB at $x=0$ (see: Fig. 4.2) where the barrier has a thickness of 0, $T(\mathcal{E}_0)$ must be 1. Therefore, the coefficient b can be expressed as:

$$b = E_{\mathrm{x}}(0)\cdot T(0) = E_{\mathrm{x}}(0)\,. \tag{4.34}$$

For the second auxiliary point $\mathcal{E}=E_{\mathrm{f,n}}$, Eq. (4.32) becomes:

$$|\vec{E}(E_{\mathrm{f,n}})|\cdot T(E_{\mathrm{f,n}}) = b\cdot\exp(-c(\mathcal{E}_0-E_{\mathrm{f,n}}))\,, \tag{4.35}$$

which can be rearranged into the final expression of c, as:

$$c = \ln\left(\frac{1}{b}\cdot E_{\mathrm{x}}(E_{\mathrm{f,n}})\cdot T(E_{\mathrm{f,n}})\right)\cdot\frac{1}{(E_{\mathrm{f,n}}-\mathcal{E}_0)}\,. \tag{4.36}$$

$E_{\mathrm{x}}(x)$ is the compact electric field in x-direction from Eq. (4.17) and $T(x)$ is the tunneling probability at position x. The fitting parameter γ_{n} for electrons (or γ_{p} for holes) is in the range of $0\ldots 1$ and shall compensate the error for low V'_{gs} caused by the Gaussian approximation from Eq. (4.19). The tunneling probability $T(x=0)$ must be 1, because $x=0$ is exactly the

top of the barrier where the tunneling thickness is zero. The tunneling probability at $x = x_\mathrm{f}$, which is at the peak of the Gaussian distribution (see Fig. 4.2), is calculated by a modified version of the WKB approximation for triangular tunneling barrier shapes from Eq. (2.65), that is given by:

$$T_\mathrm{WKB}(x_\mathrm{f}) = \exp\left(-\frac{4}{3}\cdot\frac{\sqrt{2qm^*}\cdot(\Delta\Phi(x_\mathrm{f}))^{3/2}}{\hbar\cdot|E_\mathrm{x}(0)|}\right). \tag{4.37}$$

Here, $\hbar$ is the reduced Planck's constant and m^* is either the electron $(m_\mathrm{n}\cdot m_0)$ or the hole $(m_\mathrm{p}\cdot m_0)$ tunneling mass, which are both used as fitting parameters in the compact model. The parameter $\Delta\Phi$ is the height of the barrier to be tunneled through by charge carriers, which is either given as the potential difference $\Delta\Phi(x_\mathrm{f}) = \varphi_\mathrm{ch}(x_\mathrm{f}) - \varphi_\mathrm{ch}(0)$, in case $\Delta\Phi(x_\mathrm{f})$ is bigger than $\Phi_\mathrm{B,n}$, or it is fixed to $\Phi_\mathrm{B,n}$ otherwise. Although, Eq. (4.37) is calculated at the position x_f, the electric field, that is used is $|E_\mathrm{x}(0)|$, directly at the Schottky junction. Since the approximated SB has a $1/x$ curvature and Eq. (4.37) is used for triangular energy barriers, some approximations have to be made. Using the electric field $|E_\mathrm{x}(x_\mathrm{f})|$ would be too small for a correct calculation. There are other possible methods, like an average electric field or an area equivalent method, as proposed in [84]. However, it has proven to be a good approximation to use the electric field $|E_\mathrm{x}(0)|$ in the WKB equation.

Finally, with the equations Eq. (4.31)-Eq. (4.37) the FE current density J_FE can be calculated. As it is demonstrated in [30], the integral of Eq. (4.19) can be solved to:

$$J_\mathrm{FE} \approx \frac{q\mu_\mathrm{tn}N_\mathrm{C}}{8k_\mathrm{b}\vartheta}\cdot\frac{b\sqrt{\pi}}{\sqrt{a}}\cdot\exp\left(c(E_\mathrm{f}-\mathcal{E}_0)+\frac{c^2}{4a}\right) \times\left[j_\mathrm{erfc}(\mathcal{E}_0) - j_\mathrm{erfc}(\mathcal{E}_\mathrm{min})\right], \tag{4.38}$$

with:

$$j_\mathrm{erfc}(\mathcal{E}) = \mathrm{erfc}\left(\frac{-2a(\mathcal{E}-E_\mathrm{f})+c}{2\sqrt{a}}\right), \tag{4.39}$$

where $\mathrm{erfc}(x)$ is the complementary error function. This equation for the FE current density is valid for electrons, tunneling through SBs at the conduction band. The FE current density for holes works similarly, but with the correspondent hole transport parameters.

4.2.2 Thermionic Emission Injection Current

The TE current consists of the charge carriers which overcome the energy barriers, instead of tunneling through them. In case of electrons, it is calculated according to Eq. (2.80) (in reverse direction), by:

$$J_\mathrm{TE} = A^*\vartheta^2\cdot\exp\left(-\frac{q\Phi_\mathrm{bar}}{k_\mathrm{b}\vartheta}\right)\cdot\left[1-\exp\left(-\frac{qV_\mathrm{ds}}{k_\mathrm{b}\vartheta}\right)\right], \tag{4.40}$$

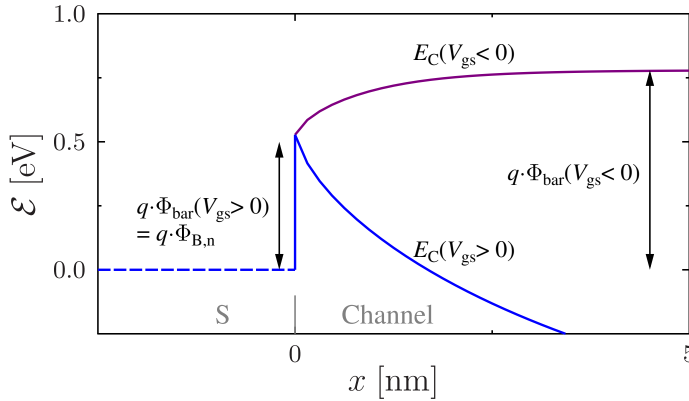


Figure 4.3: Energy barriers for the electron TE current at the source-side SB. The blue line shows the device in the on-state. In this state, Φ_{bar} is as high as the SB height. The purple line shows the device with negative gate bias. In this state Φ_{bar} equals the highest potential in the channel.

where A^* is the effective Richardson constant (see Eq. (2.79)) and Φ_{bar} is the calculated barrier height that charge carriers have to overcome. The gate voltage in Eq. (4.40) is considered in terms of the parameter Φ_{bar}, as demonstrated in Fig. 4.3. If a SB forms where the charge carriers can tunnel through, the barrier height Φ_{bar} will be given by $\Phi_{B,n}$ itself (see $q \cdot \Phi_{bar}(V_{gs} > 0)$ in Fig. 4.3). In case of a reversed electric field at the interface, it is given by the potential barrier in the channel (see $q \cdot \Phi_{bar}(V_{gs} < 0)$ in Fig. 4.3), which corresponds to the potential $\Phi_{cen,L/2}$ calculated with Eq. (4.7). For the TE current of holes an equation similar to Eq. (4.40) is defined.

4.3 Current Balancing Model

The so far described current components (FE and TE current) are both contributing to the total device current (I_{ds}). While the previous sections mainly focus on the FE and TE current calculations at the source junction, those currents also appear at the drain junction. In n-type operation mode there is an electron current at the source side and a hole current at the drain side of the device and vice versa for p-type operation mode. While the TE current, given by Eq. (4.40), depends on the drain-source voltage V_{ds}, the FE current according to Eq. (4.19) is independent of V_{ds}. This means that even for low V_{ds} high FE currents would be possible, in case of high gate voltages V_{gs}. In order to prevent this effect and bring a V_{ds} dependency into the expression for the FE current, a current balancing model is included at the drain side. In case that the drain potential is bigger than the potential in the middle of the channel (see Fig. 4.4(a)), both FE current contributions are included regularly into the total current. In case that the potential in the channel of the device is bigger than the drain potential, a virtual

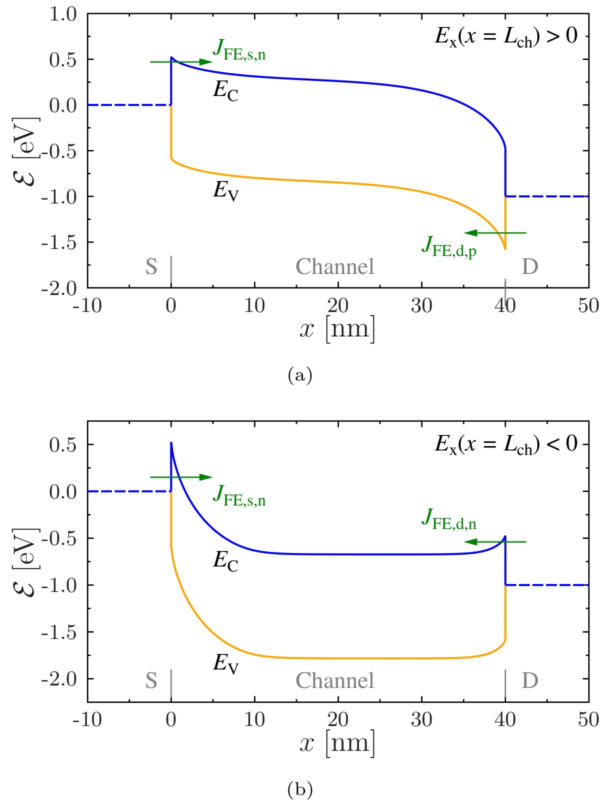


Figure 4.4: Example band diagrams at different bias conditions to demonstrate the total FE current calculation. (a) device state that allows an electron FE current ($J_{\mathrm{FE,s,n}}$) at the source side and a hole FE current ($J_{\mathrm{FE,d,p}}$) at the drain side. Both currents are contributing to the total FE current ($J_{\mathrm{FE,tot}}$). (b) device state with a SB for electrons on both sides. In the compact model, a virtual drain-side FE current ($J_{\mathrm{FE,d,n}}$) is calculated and subtracted from the source-side injection current ($J_{\mathrm{FE,s,n}}$), to calculate the total FE current ($J_{\mathrm{FE,tot}}$).

FE current is calculated which gets subtracted from the source current (see Fig. 4.4(b)). So, if $V_{\mathrm{ds}} = 0$ and a gate voltage was applied, the source FE current and the virtual drain FE current would be equally high and cancel out each other. For the total FE current density of the device this results in:

$$J_{\mathrm{FE,tot}} = \begin{cases} J_{\mathrm{FE,s,n}} - J_{\mathrm{FE,d,n}}, & E_{\mathrm{x}}(x = L_{\mathrm{ch}}) < 0 \\ J_{\mathrm{FE,s,n}}, & E_{\mathrm{x}}(x = L_{\mathrm{ch}}) = 0 \\ J_{\mathrm{FE,s,n}} + J_{\mathrm{FE,d,p}}, & E_{\mathrm{x}}(x = L_{\mathrm{ch}}) > 0 \end{cases}, \tag{4.41}$$

in the n-type operation mode and the on-state and similarly for other operation modes. $E_{\mathrm{x}}(x = L_{\mathrm{ch}})$ is the electric field in x-direction at the drain-channel junction.

The total TE current density is calculated with the TE current contributions from electrons

and holes, given by:

$$J_{\mathrm{TE,tot}} = J_{\mathrm{TE,n}} + J_{\mathrm{TE,p}} \,. \tag{4.42}$$

Considering both total current densities from Eq. (4.41) and Eq. (4.42) the total drain current of the DG SBFET is calculated by:

$$I_{\mathrm{ds,inj}} = W_{\mathrm{ch}} \cdot t_{\mathrm{ch}} (J_{\mathrm{FE,tot}} \cdot t_{\mathrm{eff,FE}} + J_{\mathrm{TE,tot}} \cdot t_{\mathrm{eff,TE}}) \,, \tag{4.43}$$

where W_{ch} is the channel width and t_{ch} is the channel thickness of the DG structure (see Fig. 3.2(a)). The channel width W_{ch} is needed, because the used potential model from Sec. 4.1 works with a 2D planar structure. Therefore, instead of calculating a nanowire structure, the model calculates the currents inside the planar structure from Fig. 3.2(a), which gets stretched in the third dimension by W_{ch}. To consider the fact that the FE current is the main on-current where the current flow is mostly located at the channel-oxide interface and the TE current flows mainly in the center of the device, two effective thicknesses ($t_{\mathrm{eff,FE}}$ and $t_{\mathrm{eff,TE}}$) are introduced in Eq. (4.43), each in the range of $0 \dots 1$. Equation (4.43) describes the total SB injection drain current which can be used to describe the SBFET characteristics as long as the channel of the transistor can be neglected.

4.4 Channel Resistance Model Addition

The channel resistance is modeled as a second-order effect of SBFETs. As an unwanted effect in those devices, this effect can get significant at higher biases and for devices with longer channel lengths and does not need to be considered for all devices. The approach in this model is to treat the channel of the SBFET as a regular MOSFET, which can accumulate negative charges and show an n-type behavior in case of a positive gate bias, and which can accumulate positive charges and show a p-type behavior in case of a negative gate bias. For the mathematical description of the channel MOSFET, a well-known charge-based model is used, that has been introduced in Sec. 2.2, given by:

$$I_{\mathrm{MOS}} = 2\mu_{\mathrm{n}} \frac{W_{\mathrm{ch}}}{L_{\mathrm{ch}}} \cdot \left[\frac{k_{\mathrm{b}}\vartheta}{q} \cdot \left(Q'_{\mathrm{s}} - Q'_{\mathrm{d}}\right) + \frac{{Q'}_{\mathrm{s}}^{2} - {Q'}_{\mathrm{d}}^{2}}{2 \cdot C'_{\mathrm{ox}}} \right] . \tag{4.44}$$

The coefficients of Eq. (4.44) are the carrier mobility of electrons μ_{n}, the device geometries W_{ch} and L_{ch} and the oxide capacity per gate area C'_{ox}. Both charge densities of Eq. (4.44) are defined as:

$$Q'_{\mathrm{s}} = \frac{S}{\ln(10)} \cdot C'_{\mathrm{ox}} \cdot W_0 \left(\exp\left(\frac{V_{\mathrm{gs,MOS}} - V_{\mathrm{T0}}}{S/\ln(10)} \right) \right) \tag{4.45}$$

and

$$Q'_{\mathrm{d}} = \frac{S}{\ln(10)} \cdot C'_{\mathrm{ox}} \cdot W_0 \left(\exp\left(\frac{V_{\mathrm{gd,MOS}} - V_{\mathrm{T0}}}{S/\ln(10)} \right) \right) , \tag{4.46}$$

with the gate-drain voltage $V_{\mathrm{gd,MOS}} = V_{\mathrm{gs,MOS}} - V_{\mathrm{ds}}$ of the channel MOSFET, the coefficients S which is the subthreshold swing and the threshold voltage V_{th} of the channel MOSFET model that can be used as fitting parameters. The function $W_0(z)$ used in Eq. (4.45) and Eq. (4.46) is the principal branch of the Lambert W function (See Eq. (2.42)).

The given Eq. (4.44) to Eq. (4.46) are valid for an n-type transistor, or rather in case that the channel of the SBFET is conductive for electrons. Since the injection model from Sec. 4.2 also supports an ambipolar and p-type mode, a p-type behavior also needs to be implemented. In this case, p-type transistor is calculated by using Eq. (4.44), but with the hole mobility μ_{p} instead of μ_{n} and with reversed voltages in the charge equations ($V_{\mathrm{gs,MOS}} \rightarrow V_{\mathrm{gd,MOS}}$ and $V_{\mathrm{gd,MOS}} \rightarrow V_{\mathrm{gs,MOS}}$). In case of the SBFET, the gate voltage for the channel MOSFET is set to $V_{\mathrm{gs,MOS}} = V_{\mathrm{gs}} - V_{\mathrm{fb}}$.

To combine the channel resistance model with the SB injection model, there are multiple options. The most accurate model would be implementing both models independently in a circuit simulator and use them together as a macro model, so the circuit simulator could find the best operating point between both model parts. However, this is not a closed-form compact solution and would require additional computation effort during runtime. Therefore, a compact approach has been chosen which is used to combine both models together. The idea is that the total current of both models is mainly dominated by the model that leads to the lower current. For an on-state n-type SBFET that would result in:

$$I_{\mathrm{ds}} = \begin{cases} I_{\mathrm{ds,inj}}, & I_{\mathrm{ds,inj}} \ll I_{\mathrm{MOS}} \\ I_{\mathrm{MOS}}, & I_{\mathrm{ds,inj}} \gg I_{\mathrm{MOS}} \end{cases}, \tag{4.47}$$

which however, is not steady or rather not even defined in a state where $I_{\mathrm{ds,inj}}$ and I_{MOS} are in the same order of magnitude. To keep the idea of using the smaller current and also have a steady, smooth, and adjustable transition between both models, the equation:

$$I_{\mathrm{ds}} = \frac{I_{\mathrm{MOS}}}{\sqrt[\gamma_{\mathrm{MOS}}]{1 + \left(\frac{I_{\mathrm{MOS}}}{I_{\mathrm{ds,inj}}}\right)^{\gamma_{\mathrm{MOS}}}}}, \tag{4.48}$$

is used. This equation combines both currents of Eq. (4.43) and Eq. (4.44) by emphasizing the lower of the two currents. The parameter γ_{MOS} is a fitting parameter which is used to smooth and fit the transition between both parts of the model.

4.5 Model Results

In this section, the results of the room temperature SBFET compact model are shown. These results are compared to TCAD simulations, in case of a short channel device in Sec. 4.5.1 and a longer channel device, including the channel resistance model, in Sec. 4.5.2. There are additional results compared to simulations and measurements for the room temperature model

which are RFET results and will be discussed in Chapter 6.

4.5.1 Model Results of the Injection Model

In this first result from [81] an ideal test case for the injection SBFET model is used, which provides a 2D DG structure and a very short channel length of $L_{\mathrm{ch}} = 40\,\mathrm{nm}$. The model results have been obtained by using the injection model only (Eq. (4.43)), while neglecting the channel resistance. For this calculation, the 2D potential model in combination with the effective gate-source voltage according to Eq. (4.1) is used. Figure 4.5 shows the model results compared to the 2D TCAD simulations of a SBFET with an intrinsic silicon channel. The S/D contacts are made of nickel silicide and the gate material is titanium, which leads to a flatband voltage of $V_{\mathrm{fb}} \approx 1\,\mathrm{V}$. The nickel silicide to silicon material junction leads to almost equally high SBs for electrons and holes and therefore, very symmetric characteristics. The geometry used in the simulation is a DG structure and L_{ch}, t_{ch} and t_{ox} are in a scale to match the model constraints well. The channel width W_{ch} of this DG structure is normalized to 1 µm, and the model's fitting parameters have been adapted manually in order to obtain the best agreement with the simulated data.

The distinctive property of the SBFET is the on-state and the ambipolar-state in the transfer characteristics which is clearly visible and covered by the compact model. The results of the model show a good agreement to the simulated current for all simulated bias conditions.

Table 4.1: Device parameters of the SBFET under investigation in Fig. 4.5

Parameter	TCAD SBFET
L_{ch} [nm]	40
W_{ch} [nm]	1000
t_{ch} [nm]	10
t_{ox} [nm]	2
$t_{\mathrm{eff,FE}}$ [-]	0.2
$t_{\mathrm{eff,TE}}$ [-]	0.8
$\varepsilon_{\mathrm{r,ox}}$ [-]	3.9
$\varepsilon_{\mathrm{r,SC}}$ [-]	11.7
E_{g} [eV]	1.155
$\Phi_{\mathrm{B,n}}$ [V]	0.660
$\Phi_{\mathrm{B,p}}$ [V]	0.495
m_{n} [-]	0.749
m_{p} [-]	0.288
μ_{tn} [$\mathrm{cm^2\,V^{-1}\,s^{-1}}$]	378
μ_{tp} [$\mathrm{cm^2\,V^{-1}\,s^{-1}}$]	20
γ_{n} [-]	1.0
γ_{p} [-]	1.0
α [-]	0.6
V_{fb} [V]	+1

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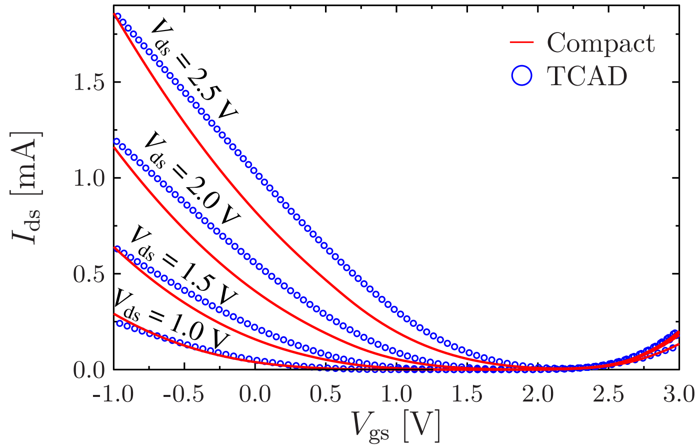
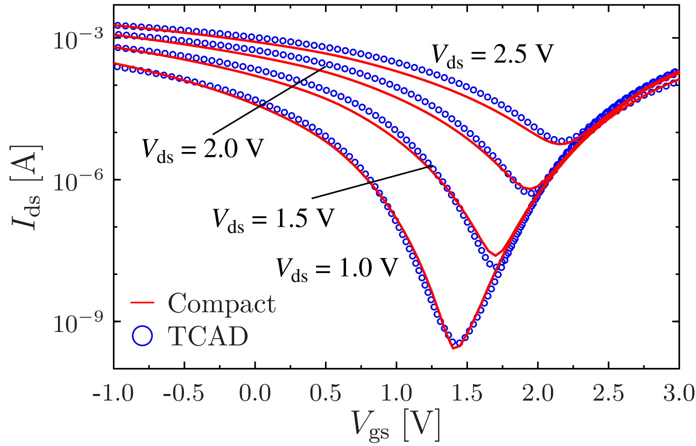
COMPACT MODELING OF SCHOTTKY BARRIER AND RECONFIGURABLE FIELD-EFFECT TRANSISTORS
Christian Römer



(a)



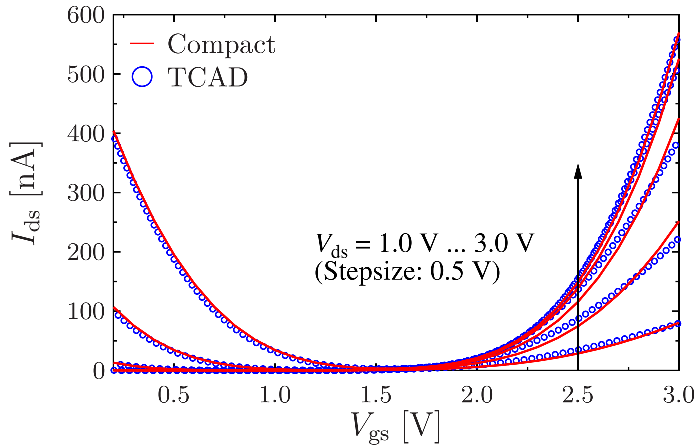
(b)

Figure 4.5: Model results compared to TCAD simulations. The blue dots represent the results of the TCAD simulations, and the red lines are the compact model results. The results are presented in (a) linear and (b) logarithmic scale. The used model parameters can be found in Tab. 4.1.

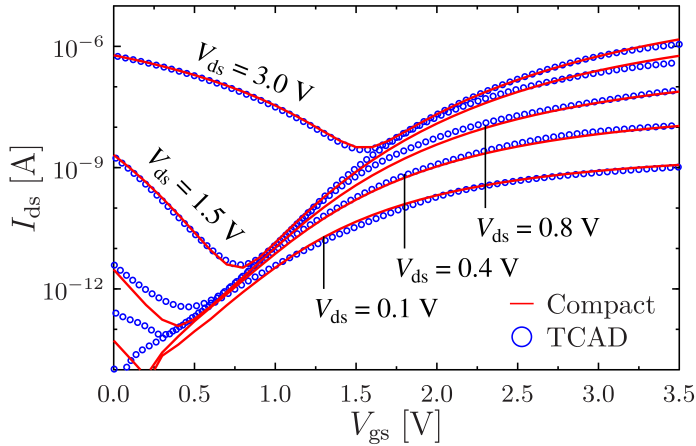
There are only slight deviations in the ambipolar region for higher drain voltages. The full set structural and model parameters that were used can be found in Tab. 4.1.

4.5.2 Model Results Including Channel Resistance

In this section, the model is applied to a long-channel SBFET device with a channel length of 5 µm which is also simulated with TCAD Sentaurus [83]. This TCAD simulation is performed as a 2D simulation of the device's cross-section combined with the cylindrical mode, in order to simulate a full nanowire gate-all-around structure [28]. The used material parameters of the TCAD simulation are equal to those from Sec. 3.1. The used geometric, material, and fitting parameters used for the compact model can be found in Tab. 4.2. For obtaining these model results the channel resistance model from Sec. 4.4 is used, together with the effective gate-source voltage calculation according to Eq. (4.3). The fitting parameters have been adapted manually to the simulated data. It shall be mentioned that the device geometries W_{ch} and t_{ch} have been chosen to approximately fit the circumference and diameter, respectively of the simulated device, which has a nanowire channel radius of $R_{\mathrm{NW}} = 15\,\mathrm{nm}$. However, these model parameters are still not completely comparable to the nanowire's radius but used to fit the calculated characteristics. Especially, the channel width W_{ch} is roughly about four times smaller than expected. An explanation for this reduced channel width, could be the different physical behavior between the simulated gate-all-around structure and the modeled 2D double gate structure, as well as the fact that the TCAD simulation uses a high-field saturation mobility model, that reduces the carrier mobility at high electric fields, which is impactful for MOSFETs at higher bias voltages [28]. This second effect using a dynamic mobility is not considered in the current implementation of the compact model, but can lead to the recognized deviation, compensated by the channel width. All other geometric parameters correspond to the simulation. The results are shown in Fig. 4.6, which consist of transfer characteristics in linear and logarithmic scale and Fig. 4.7 which are the corresponding output characteristics. The compact model results show a good agreement to the given TCAD simulations, besides a slight deviation in the output characteristics.



(a)



(b)

Figure 4.6: Device characteristics of the SBFET calculated from the compact model (solid red lines) and compared to TCAD simulations (blue dots). The geometries of the simulated device are $L_{ch} = 5.0\,\mu m$, $R_{NW} = 15\,nm$ and $t_{ox} = 6.5\,nm$. The compact model parameters can be found in Tab. 4.2. (a) shows the transfer characteristics for various positive drain voltages in linear scale and (b) shows similar results in logarithmic scale.

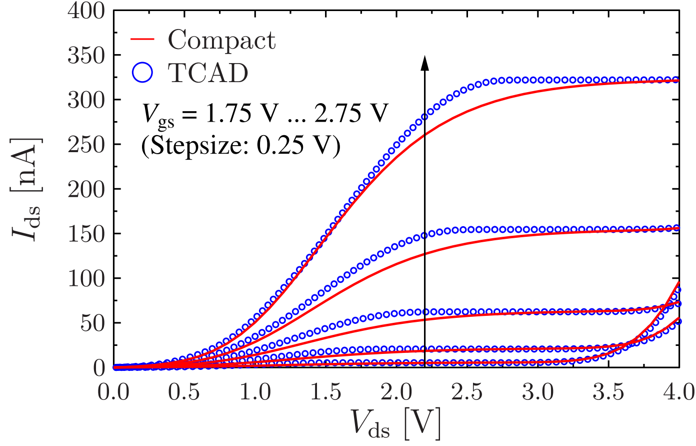


Figure 4.7: Device output characteristics of the SBFET calculated from the compact model (solid red line) and compared to TCAD simulations (blue dots). The geometries of the simulated device are $L_{ch} = 5.0\,\mu m$, $R_{NW} = 15\,nm$ and $t_{ox} = 6.5\,nm$. The compact model parameters can be found in Tab. 4.2.

Table 4.2: Device parameters of the SBFET under investigation in Fig. 4.6 and Fig. 4.7

Parameter	SBFET (TCAD)
L_{ch} [µm]	5.0
W_{ch} [nm]	13
t_{ch} [nm]	30
t_{ox} [nm]	6.5
$t_{eff,FE}$ [-]	0.2
$t_{eff,TE}$ [-]	0.8
$\varepsilon_{r,ox}$ [-]	3.9
$\varepsilon_{r,sc}$ [-]	11.7
E_g [eV]	1.1696
$\Phi_{B,n}$ [V]	0.5800
$\Phi_{B,p}$ [V]	0.5896
V_{limit} [V]	1.65
$\gamma_{Vg,eff}$ [-]	2.10
m_n [-]	0.26
m_p [-]	0.27
μ_{tn} [$cm^2\,V^{-1}\,s^{-1}$]	415.35
μ_{tp} [$cm^2\,V^{-1}\,s^{-1}$]	1352.00
γ_n [-]	0.20
γ_p [-]	0.20
V_{T0} [V]	1.11
S [mV/dec.]	150
γ_{MOS} [-]	0.5
μ_n [$cm^2\,V^{-1}\,s^{-1}$]	1440
μ_p [$cm^2\,V^{-1}\,s^{-1}$]	450
V_{fb} [V]	0

CHAPTER 5

Model Additions for Deep Cryogenic Temperatures

This chapter describes the model for SBFETs that is adjusted for a deep-cryogenic temperature environment of $\vartheta \approx 0\,\mathrm{K}$. This compact model has been published in [85, 86]. Although the SBFET compact model described in Chapter 4 has a temperature dependency in its equations, it is made for room temperature environment, specifically. This means that the room temperature model is not scalable to the temperature and needs to be re-fitted for different temperatures. It is also not capable of capturing certain physical effects occurring at deep cryogenic temperatures.

For this SBFET compact model at deep cryogenic temperatures, the equations are further developed and solved in this temperature environment. For an easier model derivation, a temperature of $\vartheta \to 0\,\mathrm{K}$ is estimated. The compact model for deep cryogenic temperatures uses a different approach to obtain the potential inside the transistors channel, compared to the room temperature model. This approach is described in Sec. 5.1. In case of a temperature of $\vartheta \to 0\,\mathrm{K}$, there is no TE current expected to be injected at the devices' SBs. Therefore, the main injection current is the FE current which is derived in Sec. 5.2. Section 5.3 describes the inclusion of second order effects that can be observed in measurements at the given temperature environment. Those are quantum oscillations, band tail effect and the channel resistance. In Sec. 5.4 the total drain current equation is given, which includes the FE current and the mentioned second order effects. Finally, Sec. 5.5 shows the model results compared to measurements of SBFETs that are measured at temperatures of about $5\,\mathrm{K}$. The cryogenic SBFET measurements have been provided by Forschungszentrum Jülich GmbH.

5.1 Potential Model Adjustments at Absolute Zero

For the cryogenic SBFET model the used potential model has been replaced, by the quasi 2D potential model introduced in Sec. 2.1.2. The replacement has two reasons. First, the quasi 2D model is temperature independent and the doping concentration used in this model can be

ignored, since the dopants are supposed to be frozen out. Second, at temperatures of $\vartheta \to 0\,\mathrm{K}$, there is no thermal energy and therefore, no TE current expected to be flowing. Without the TE current it is not necessary to calculate the potential in the center y-position of the device's channel. In this case, only the surface potential is of interest, which can be calculated with less effort by the quasi 2D potential model.

For a proper usage of the quasi 2D potential model, even at high bias voltages, a saturation model has to be included to counteract the neglect of accumulated charges in the potential model. Section 5.1.1 introduces a potential saturation model that is derived specifically for the case $\vartheta \to 0\,\mathrm{K}$ which calculates an effective gate-source voltage $V_{\mathrm{gs,eff}}$. The following Sec. 5.1.2 describes the usage of the basic potential model including the saturation model, and the reconstruction of important band diagram parameters with the potential model.

5.1.1 Saturation at High Gate Voltages

Since the potential model that is used for the cryogenic SBFET model is based on Poisson's equation, but neglects accumulated charges inside the channel, it is working fine for lower gate voltages, but overestimates the device's surface potential at higher gate voltages. In order to work around this problem, appearing at higher gate voltages, a surface potential saturation model applicable for temperatures of $\vartheta \to 0\,\mathrm{K}$ is introduced which calculates an effective gate voltage $V_{\mathrm{gs,eff}}$. The given derivation is done for accumulated electrons (positive gate voltages) but works similarly with holes. For the derivation of this model, the standard approach for the calculation of the electron density n inside a 3D semiconductor according to [2, 6] is used, given as:

$$n = \int_{E_{\mathrm{C}}}^{\infty} g_{\mathrm{C3D}}(\mathcal{E}) \cdot f_{\mathrm{n}}(\mathcal{E}) \cdot d\mathcal{E}\,, \tag{5.1}$$

where g_{C3D} is the semiconductor's density of states and f_{n} is the Fermi distribution function, both dependent on the energy level $\mathcal{E}$. In a temperature environment that is estimated to be $\vartheta \to 0\,\mathrm{K}$, the Fermi distribution function can be simplified to:

$$\begin{aligned} f_{\mathrm{n}}(\mathcal{E}) &= \lim_{\vartheta \to 0} \left[\frac{1}{1 + \exp\left(\frac{\mathcal{E} - E_{\mathrm{f,n}}}{k_{\mathrm{b}}\vartheta}\right)} \right] \\ &= \begin{cases} 0, & \mathcal{E} > E_{\mathrm{fn}} \\ 1, & \mathcal{E} < E_{\mathrm{fn}} \end{cases}\,, \end{aligned} \tag{5.2}$$

resulting in a piece-wise defined step function with a full occupation of states for energy levels lower than the quasi-Fermi energy level for electrons (E_{fn}) and no occupation for states on

energy levels higher than E_{fn}. Using Eq. (5.2) in Eq. (5.1), the integral can be simplified to:

$$n = \int_{E_\mathrm{C}}^{E_\mathrm{fn}} g_\mathrm{C3D}(\mathcal{E}) \cdot 1 \cdot d\mathcal{E} + \int_{E_\mathrm{fn}}^{\infty} g_\mathrm{C3D}(\mathcal{E}) \cdot 0 \cdot d\mathcal{E}\,, \tag{5.3}$$

with g_{C3D} as density of states, according to [2, 6], which can be written as:

$$n = v_\mathrm{n} \cdot \frac{(2m_\mathrm{n}^*)^{\frac{3}{2}}}{2\pi^2\hbar^3} \cdot \int_{E_\mathrm{C}}^{E_\mathrm{fn}} \sqrt{\mathcal{E} - E_\mathrm{C}} \cdot d\mathcal{E}\,. \tag{5.4}$$

This integral solves to:

$$n = v_\mathrm{n} \cdot \frac{(2m_\mathrm{n}^*)^{\frac{3}{2}}}{2\pi^2\hbar^3} \cdot \left[\frac{2}{3} \cdot (\mathcal{E} - E_\mathrm{C})^{\frac{3}{2}}\right]_{E_\mathrm{C}}^{E_\mathrm{fn}}\,, \tag{5.5}$$

which leads to an expression for the electrons in the conduction band, given as:

$$n = \frac{\sqrt{8} v_\mathrm{n} m_\mathrm{me}^{3/2}}{3\pi^2\hbar^3} (E_\mathrm{fn} - E_\mathrm{C})^{\frac{3}{2}}\,. \tag{5.6}$$

Equation (5.6) shows the relation of the electron density to the energy difference of E_{fn} and the conduction band energy E_{C}. The constants of Eq. (5.6) are the number of equivalent minima in the conduction band v_{n}, the density-of-state effective mass for electrons m_{me}, and the reduced Planck's constant $\hbar$ [2, 6]. Equation (5.6) shows that, in case of $\vartheta \rightarrow 0\,\mathrm{K}$, the quasi Fermi energy level for electrons $E_{\mathrm{f,n}}$ must be higher than the conduction band energy E_{C} in order to have existing free electrons that can contribute to the current flow.

The accumulated carriers (or rather the carrier density) at the device's channel surface also depends on the applied gate voltage. At high gate voltages, it is estimated that almost all accumulated carriers are close to the channel surface and the major voltage drop of the flatband voltage corrected gate-source voltage $V_{\mathrm{gs}}' = V_{\mathrm{gs}} - V_{\mathrm{fb}}$ is at the oxide. This is represented by:

$$V_\mathrm{gs}' = \frac{q_\mathrm{sur}}{C_\mathrm{ox}'} = \frac{n \cdot q \cdot t_\mathrm{sur}}{C_\mathrm{ox}'}\,, \tag{5.7}$$

with q_{sur} as the accumulated surface charge and C_{ox}' as oxide capacitance per gate area. In the second step of Eq. (5.7), q_{sur} is replaced by $n \cdot q \cdot t_{\mathrm{sur}}$, where t_{sur} is an average thickness that contains the accumulated electron concentration n and is estimated to be constant in this approach. Finally, using Eq. (5.6) in Eq. (5.7), leads to:

$$V_\mathrm{gs}' = \frac{\sqrt{8} q t_\mathrm{sur} v_\mathrm{n} m_\mathrm{me}^{3/2}}{3C_\mathrm{ox}'\pi^2\hbar^3} \cdot (E_\mathrm{fn} - E_\mathrm{C})^{\frac{3}{2}}\,. \tag{5.8}$$

This equation describes the dependency between V_{gs}' and $(E_{\mathrm{fn}} - E_{\mathrm{C}})$ in case of saturation of the channel potential. For a simplification and better usage in the algorithm, a constant K_{sat}

is introduced and defined as:

$$K_{\mathrm{sat}} = \frac{\sqrt{8} q t_{\mathrm{sur}} v_{\mathrm{n}} m_{\mathrm{me}}^{3/2}}{3 C'_{\mathrm{ox}} \pi^2 \hbar^3} \cdot q^{\frac{3}{2}} , \quad (5.9)$$

which replaces the constants in Eq. (5.8). In the next step, the energies are represented as potentials, with $\Phi_{\mathrm{sur,sat}} = -q^{-1} \cdot (E_{\mathrm{C}} - E_{\mathrm{g}}/2)$ as the saturated surface potential and $\Phi_{\mathrm{fn}} = E_{\mathrm{f,n}}/q$ as the quasi Fermi potential for electrons, which can only be in range of V_{s} to V_{d}. Using both potentials and Eq. (5.9) in Eq. (5.8) leads to the equation:

$$V'_{\mathrm{gs}} = K_{\mathrm{sat}} \cdot \left(\Phi_{\mathrm{sur,sat}} - \frac{E_{\mathrm{g}}}{2q} - \Phi_{\mathrm{fn}}\right)^{\frac{3}{2}} . \quad (5.10)$$

The energy-to-potential conversion term $q^{\frac{3}{2}}$ has been included in the constant K_{sat}. Equation (5.10) is the key equation for the upcoming calculations.

In order to incorporate the saturated channel potential from Eq. (5.10) into the used potential model with an effective gate-source voltage $V_{\mathrm{gs,eff}}$, an algorithm is used which is explained in the following steps.

Establish Boundary Condition

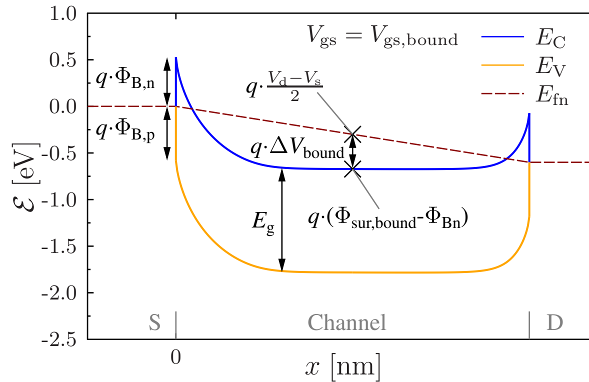
First, a boundary condition at which the saturation process starts, needs to be defined. The idea is to find a boundary surface potential $\Phi_{\mathrm{sur,bound}}$ and a corresponding boundary gate-source voltage $V_{\mathrm{gs,bound}}$, where $V'_{\mathrm{gs}} > V_{\mathrm{gs,bound}}$ leads to a saturation of the surface potential, due to accumulated charges in the channel. As Eq. (5.6) demonstrates, the electron accumulation happens as soon as the quasi-Fermi energy of electrons $E_{\mathrm{f,n}}$ is higher than the conduction band energy E_{C}. This state is shown in Fig. 5.1(a), which shows the band diagram of a SBFET reconstructed by the potential model of Eq. (2.15) (See Sec. 2.1.2). This condition is shown in Fig. 5.1(a) in the calculated band diagram. In case that the boundary condition is met or surpassed, it is assumed, that the quasi-Fermi energy for electrons drops linearly from source to drain. Therefore, the quasi-Fermi potential in the middle of the channel can be written as:

$$\Phi_{\mathrm{fn,L/2}} = \Phi_{\mathrm{fn}}\left(\frac{L_{\mathrm{ch}}}{2}\right) \approx \frac{V_{\mathrm{d}} - V_{\mathrm{s}}}{2} , \quad (5.11)$$

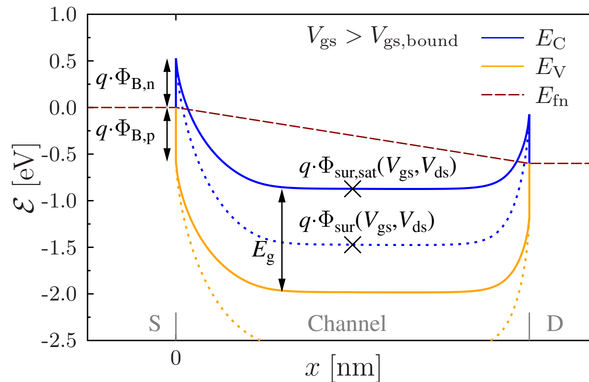
so the value of $\Phi_{\mathrm{fn,L/2}}$ is exactly in between of the source and drain potentials. A useful condition for switching over to the saturation model is at:

$$\Phi_{\mathrm{sur,bound}} = \frac{V_{\mathrm{d}} - V_{\mathrm{s}}}{2} + \Phi_{\mathrm{B,n}} + \Delta V_{\mathrm{bound}} , \quad (5.12)$$

which represents the boundary potential in the middle of the channel at which the conduction band hits the approximated value of $\Phi_{\mathrm{fn,L/2}}$, minus an additional voltage $\Delta V_{\mathrm{bound}}$, that serves as an adjustable fitting parameter (see Fig. 5.1(a)).



(a)



(b)

Figure 5.1: Band diagram of an arbitrary device, demonstrating the surface potential saturation model. The blue line is the conduction band energy, the orange line is the valence band energy, and the red dashed line is the estimated quasi-Fermi energy for electrons in the on-state. (a) shows the saturation condition, given by Eq. (5.12). (b) shows an example of a higher gate bias and the difference between a saturated (solid lines) and an unsaturated (dotted lines) surface potential. The unsaturated case leads to a huge difference between E_{fn} and E_C and therefore, to an unrealistically high number of accumulated electrons, according to Eq. (5.4).

After the boundary potential $\Phi_{\mathrm{sur,bound}}$ for the given drain voltage has been calculated, the needed gate-source voltage $V_{\mathrm{gs,bound}}$ for reaching that boundary state can be obtained, using the potential model Eq. (2.15) in reverse, as:

$$V_{\mathrm{gs,bound}} = \Phi_{\mathrm{sur,bound}} - \left[\frac{V_{\mathrm{b,s}} \cdot p(L_{\mathrm{ch}} - x) + V_{\mathrm{b,d}} \cdot p(x)}{p(L_{\mathrm{ch}})}\right]_{x=\frac{L_{\mathrm{ch}}}{2}} , \tag{5.13}$$

with $p(x)$ given as Eq. (2.16).

Determine the Saturation Constant

In a second step, it is assumed that for an applied gate-source voltage of $V'_{\mathrm{gs}} > V_{\mathrm{gs,bound}}$, the accumulated charges in the channel can no longer be neglected and therefore, the saturation equation Eq. (5.10) needs to be used in order to describe the dependency between gate-source voltage and surface potential. Using Eq. (5.10) at the saturation boundary, with $V'_{\mathrm{gs}} = V_{\mathrm{gs,bound}}$ and $\Phi_{\mathrm{sur,sat}} = \Phi_{\mathrm{sur,bound}}$, K_{sat} can be calculated as:

$$K_{\mathrm{sat}} = V_{\mathrm{gs,bound}} \cdot \left(\Phi_{\mathrm{sur,bound}} - \frac{E_{\mathrm{g}}}{2q} - \Phi_{\mathrm{fn,L/2}}\right)^{-\frac{3}{2}} , \tag{5.14}$$

which is estimated to be constant for all $V'_{\mathrm{gs}} > V_{\mathrm{gs,bound}}$.

Calculate the Saturated Potential and Gate-Source-Voltage

In the previous steps the boundary condition for the saturation and the saturation constant K_{sat} have been defined. Now, for gate-source voltages of $V'_{\mathrm{gs}} > V_{\mathrm{gs,bound}}$ the constant K_{sat} and $\Phi_{\mathrm{fn,L/2}}$ can be used in Eq. (5.10) again, in order to calculate the saturated surface potential $\Phi_{\mathrm{sur,sat}}$, as:

$$\Phi_{\mathrm{sur,sat}} = \left(\frac{V'_{\mathrm{gs}}}{K_{\mathrm{sat}}}\right)^{\frac{2}{3}} + \frac{E_{\mathrm{g}}}{2q} + \Phi_{\mathrm{fn,L/2}} . \tag{5.15}$$

Finally, Eq. (5.15) leads to an expression that could be used as saturated surface potential, but only at the position $x = L_{\mathrm{ch}}/2$. For a completed surface potential, the Laplace function based potential model adjusted in Eq. (5.13) can be used again, but this time to calculate from $\Phi_{\mathrm{sur,sat}}$ the corresponding saturated gate-source voltage $V_{\mathrm{gs,sat}}$, as:

$$V_{\mathrm{gs,sat}} = \Phi_{\mathrm{sur,sat}} - \left[\frac{V_{\mathrm{b,s}} \cdot p(L_{\mathrm{ch}} - x) + V_{\mathrm{b,d}} \cdot p(x)}{p(L_{\mathrm{ch}})}\right]_{x=\frac{L_{\mathrm{ch}}}{2}} . \tag{5.16}$$

This voltage, as replacement for V'_{gs} in the initial potential model of Eq. (2.15), results in the same surface potential $\Phi_{\mathrm{sur}}(L_{\mathrm{ch}}/2) = \Phi_{\mathrm{sur,sat}}$ as from the saturation model Eq. (5.10), which is necessary for the last step.

Expression for all Bias Regions

In the last step, a distinction needs to be made at which the applied (model input) gate-source voltages V'_{gs} the saturation model should be used or not. For this case an effective gate-source voltage $V_{\mathrm{gs,eff}}$ is introduced that replaces the actual input voltage V'_{gs}. The easiest way for this distinction would be conditional, as:

$$V_{\mathrm{gs,eff}} = \begin{cases} V'_{\mathrm{gs}}, & V'_{\mathrm{gs}} \leq V_{\mathrm{gs,sat}} \\ V_{\mathrm{gs,sat}}, & V'_{\mathrm{gs}} > V_{\mathrm{gs,sat}} \end{cases} , \tag{5.17}$$

which would be steady and considers both operation regions. For compact modeling it is preferable to have smooth functions that are differentiable for all input voltages V_{gs}'. For this smooth transition between the unsaturated and the saturated region, instead of using Eq. (5.17), a smoothing function is defined to calculate the effective gate-source voltage, as

$$V_{\mathrm{gs,eff}} = \left(\sqrt[\gamma_{\mathrm{sat}}]{V'^{-\gamma_{\mathrm{sat}}}_{\mathrm{gs}} + V^{-\gamma_{\mathrm{sat}}}_{\mathrm{gs,sat}}} \right)^{-1} , \tag{5.18}$$

where γ_{sat} is a fitting parameter to adjust the transition region between the saturated and the unsaturated model. Finally, the resulting effective gate voltage $V_{\mathrm{gs,eff}}$ from Eq. (5.18) can be used in the initial potential model Eq. (2.15) for calculating the surface potential for the entire gate-source voltage range.

Figure 5.1(b) demonstrates the differences between using $V_{\mathrm{gs,eff}}$ (solid lines), where the surface potential (and therefore, the conduction band) depends on the distance to the quasi Fermi potential Φ_{fn}, and using V'_{gs}, leading to an unbound surface potential (dashed lines) and an overestimated band bending. Even though the modeled band diagram does not show a linear voltage drop along the trace from source to drain as it is to be expected in a real device, the described saturation model prevents an over-bending of the bands. Figure 5.2 shows $V_{\mathrm{gs,eff}}$ calculated by Eq. (5.18) vs the applied V'_{gs} using the parameters from Fig. 5.11(b).

5.1.2 Basic Potential Model and Band Diagram Reconstruction

As discussed in the previous section, the used potential model for the cryogenic SBFET model is the 1D / quasi 2D potential model from [34], which has been introduced in Sec. 2.1.2. This model is used to calculate and give the dependency between the surface potential Φ_{sur} and the x-location along the semiconductor-oxide interface, from source ($x = 0$) to drain ($x = L_{\mathrm{ch}}$). Using the effective gate voltage form Eq. (5.18), for a proper saturation at all bias voltages, with Eq. (2.15), it is given as:

$$\Phi_{\mathrm{sur}}(x) = V_{\mathrm{gs,eff}} + \frac{V_{\mathrm{b,s}} \cdot p(L_{\mathrm{ch}} - x) + V_{\mathrm{b,d}} \cdot p(x)}{p(L_{\mathrm{ch}})} , \tag{5.19}$$

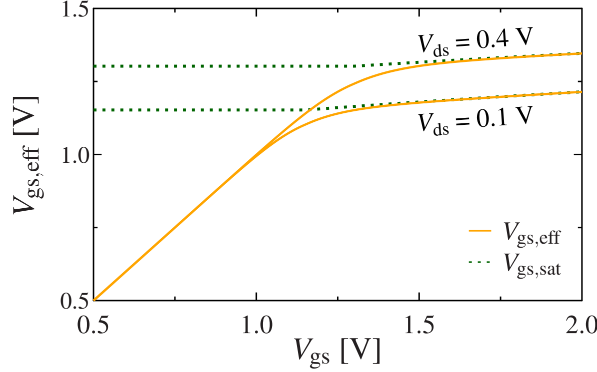


Figure 5.2: Plot that shows $V_{gs,eff}$ and $V_{gs,sat}$ vs V_{gs} calculated by the surface potential saturation model. The shown curves belong to the model verification shown in Fig. 5.11(b).

with

$$p(x') = \exp\left(\frac{x'}{\lambda}\right) - \exp\left(-\frac{x'}{\lambda}\right) . \tag{5.20}$$

$V_{b,s}$ and $V_{b,d}$ are the potential bendings at the source and drain side, respectively, which are calculated using the built-in potential $\Phi_{bi} = \Phi_{Bn} - E_g/(2q)$ as $V_{b,s/d} = \Phi_{bi} - V_{gs,eff} + V_{s/d}$, with the channel material's band gap E_g, the SB height for electrons Φ_{Bn}, and the source/drain potential $V_{s/d}$.

Similarly to the approach of Chapter 4, the potential model is used to reconstruct the band diagram and the SB thickness x_f at $\mathcal{E} = E_{f,m}$ (shown in Fig. 5.3). Unlike the 2D potential model used in the approach of Chapter 4, the model from Eq. (5.19) is already a closed-form and very simple equation, so there is no need for a further simplification. The band diagram energies can be calculated as:

$$E_C = -q \cdot \Phi_{sur}(x) + \frac{E_g}{2} , \tag{5.21}$$

and:

$$E_V = -q \cdot \Phi_{sur}(x) - \frac{E_g}{2} . \tag{5.22}$$

The parameter x_f can be calculated analytically by using Eq. (5.19) and Eq. (5.20) and rearranging the equations for $x = x_f$, which results in:

$$x_f = \lambda \cdot \ln\left[\frac{\frac{E_{f,m}}{q} \cdot p(L_{ch}) \pm \sqrt{d_{xf}}}{2 \cdot V_{b,d} - 2 \cdot V_{b,s} \cdot \exp\left(-\frac{L_{ch}}{\lambda}\right)}\right] , \tag{5.23}$$

with:

$$d_{xf} = \frac{E_{f,m}}{q}^2 \cdot p(L_{ch})^2 - 4 \cdot V_{b,s} \cdot V_{b,d} \cdot p(L_{ch}) - 4 \cdot V_{b,s}^2 - 4 \cdot V_{b,d}^2 . \tag{5.24}$$

Equation (5.23) is only solvable in case x_f exists, which means that E_C must be smaller as

$E_{\mathrm{f,m}}$ due to band bending (see Fig. 5.3).

5.2 Injection Current for SBFETs at Deep Cryogenic Temperatures

With the reconstructed band diagram at the SBs, the FE injection currents can be calculated. Although the approach is similar to Chapter 4, there are some changes in the derivation. In this section, the basic approaches for the tunneling equation and tunneling probability are shown (see Sec. 5.2.1), as well as the usage and simplification of the supply function (see Sec. 5.2.2).

5.2.1 Tunneling Equation and Tunneling Probability

The expression for the electron (similar for hole) FE current density is derived based on a modified version of the Tsu-Esaki formula, which has been introduced in Sec. 2.3.3.1, as:

$$J_{\mathrm{FE,n}} = \frac{q \cdot m^*}{2\pi^2 \hbar^3} \cdot B_{\mathrm{PAT}} \cdot \int\limits_{E_{\mathrm{C,min}}}^{E_{\mathrm{fs}}} T(\mathcal{E}) \cdot N(\mathcal{E}) \cdot d\mathcal{E}\,, \tag{5.25}$$

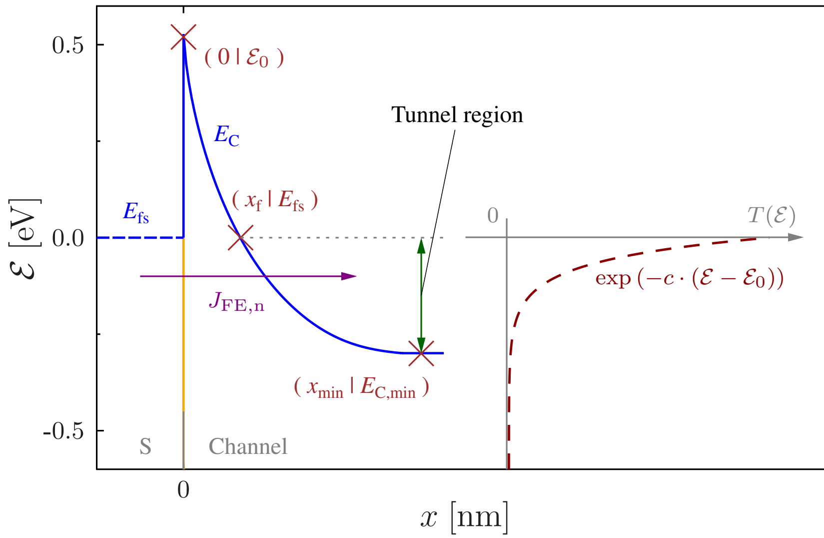


Figure 5.3: Band diagram at the source-side Schottky junction (left-hand side). The solid blue line is the conduction band of the channel, and the blue dashed line shows the metal's Fermi energy level. The right-hand side subplot shows the approximated tunneling probability, which is exponentially increasing with the energy, as dashed red line. The green arrow marks the tunneling region. In this energy region electrons are allowed to tunnel through the SB, due to Fermi statistics.

where q is the elementary charge, m^* is the charge carrier's effective tunneling mass ($m_\mathrm{n} \cdot m_0$ for electrons or $m_\mathrm{p} \cdot m_0$ for holes), used as fitting parameter, and $\hbar$ is the reduced Planck's constant. $T(\mathcal{E})$ and $N(\mathcal{E})$ denote the tunneling probability and supply function at the energy $\mathcal{E}$, respectively. In cryogenic environment it is estimated that the metal source and drain regions have all energy states completely filled which are lower than the metal's Fermi energy level (E_fs for the source and E_fd for the drain) and those states with higher energy levels than the metal's Fermi energy level are completely empty. This leads to the upper integration limit of Eq. (5.25) since there are no electrons available for tunneling at $\mathcal{E} > E_\mathrm{fs}$. The lower integration limit is the minimum energy level carriers can tunnel to, which is estimated to be the lowest conduction band energy value $E_\mathrm{C,min}$ in the channel. This is determined by using the value directly in the middle of the device's channel ($L_\mathrm{ch}/2$). Figure 5.3 illustrates the tunneling process at the source-side SB and shows the integration boundaries.

The tunneling probability in Eq. (5.25) assumes direct tunneling, i.e. tunneling charge carriers will keep their momentum, or rather $\vec{k}$ wave vector in x direction (coherent tunneling) [6]. Although, tunneling through a SB may require a change in momentum by phonon scattering (phonon-assisted tunneling, PAT) [6]. At room temperature, due to the presence of excited phonons, this effect is usually neglected in compact modeling. However, at deep cryogenic temperatures the phonon scattering events are massively reduced, so tunneling events can almost only occur, if both materials at the tunneling junction (the SB) have overlapping k-spaces [87]. In order to represent this in the compact model, we introduce the fitting parameter B_PAT in Eq. (5.25) with a value between 0 and 1 that is used to describe the reduced tunneling current density.

For the calculation of the tunneling probability, the same approximation is used as in the room temperature model from Sec. 4.2.1. Instead of using the WKB approximation for the tunneling probability T_WKB (from Eq. (2.65)) directly in Eq. (5.25) which would lead to an unsolvable integral, the tunneling probability is approximated by an exponential function, given as:

$$T_\mathrm{cryo,0}(\mathcal{E}) = \exp\left(-c \cdot (\mathcal{E}_0 - \mathcal{E})\right) . \tag{5.26}$$

In this approximation, c is obtained similarly as in Eq. (4.35) by using:

$$c = \frac{\ln\left(T_\mathrm{WKB}(x_\mathrm{f})\right)}{(E_\mathrm{fs} - \mathcal{E}_0)} . \tag{5.27}$$

$T_\mathrm{WKB}(x_\mathrm{f})$ is the tunneling probability calculated at position x_f by using the WKB method, as in Eq. (4.37). $\mathcal{E}_0$ is the conduction band energy E_C directly at the source-channel Schottky junction, marking the energy barrier height. The parameters x_f, E_fs and $\mathcal{E}_0$ are indicated in Fig. 5.3.

5.2.2 Supply Function Simplification

The supply function of the tunneling process from Eq. (2.72), is given by:

$$N(\mathcal{E}) = \int_0^\infty \left(f_\text{s}(\mathcal{E}_\text{tot}) - f_\text{d}(\mathcal{E}_\text{tot})\right) \cdot d\mathcal{E}_\rho \,, \tag{5.28}$$

$$N(\mathcal{E}) = k\vartheta \cdot \ln \left[\frac{1 + \exp\left(-\frac{\mathcal{E} - E_\text{fs}}{k\vartheta}\right)}{1 + \exp\left(-\frac{\mathcal{E} - E_\text{fd}}{k\vartheta}\right)} \right] \,, \tag{5.29}$$

with the source and drain side Fermi distribution functions f_s and f_d. The carrier's total energy $\mathcal{E}_\text{tot} = \mathcal{E} + \mathcal{E}_\rho$ is the sum of its longitudinal $\mathcal{E}$ and transversal $\mathcal{E}_\rho$ energy components [59]. The supply function depends on the temperature, as it can be seen in Eq. (5.28). At the deep cryogenic temperature environment ($\vartheta \to 0$), the equation Eq. (5.29) can be simplified to:

$$\lim_{\vartheta \to 0} N(\mathcal{E}) \approx \lim_{\vartheta \to 0} k\vartheta \cdot \ln \left[\frac{\exp\left(-\frac{\mathcal{E} - E_\text{fs}}{k\vartheta}\right)}{1} \right] \tag{5.30}$$

$$\approx E_\text{fs} - \mathcal{E} \,, \tag{5.31}$$

This simplification can be used in Eq. (5.25), to solve the integral.

5.3 Inclusion of Second Order Effects

There are some second order effects that are considered in the cryogenic SBFET model. First, in [8] oscillations in the curves have been found in the measured transfer characteristics. Section 5.3.1 presents an empirical modeling approach for the inclusion of quantum oscillations into the tunneling probability expression.

As a second included effect, it has been shown in [11] that some devices show a subthreshold swing that is shallower as it would be expected at $\vartheta \approx 0\,\text{K}$. The worse slope has been attributed to the existence of band tail states inside the semiconductors band gap region, which are notable at deep cryogenic temperatures [11]. Section 5.3.2 shows an approach to include a band tail current by assuming an exponential band tail states distribution into the semiconductor's band gap, that affect the SBFET's subthreshold swing.

Although the potential saturation model has been included and described in Sec. 5.1.1, this model part does not directly limit the current at high biases. As in room temperature environment, it can also happen at cryogenic temperatures that the channel resistance for longer channels at higher bias voltages can no longer be neglected. So, as a last included

effect the channel resistance model introduced in Sec. 4.5.2 is included into the model, which is described in Sec. 5.3.3.

5.3.1 Empirical Model for Quantum Oscillations

In some measured characteristics of SBFETs at deep cryogenic temperatures, it can be noticed that the measured current is oscillating while increasing the applied voltage. This phenomenon has been reported in [8] and can be seen in some measured characteristics that are presented in Sec. 5.5. Although, it cannot be stated for sure where this effect comes from, a possible answer can be given by the NEGF approach, described in Sec. 2.3.3.3. In [88] it is shown, by using a compact NEGF method from [88, 89], that this wave-based approach leads to local minima and maxima in the density of states along the energy axis at the source-side SB. The simulated local density of states using the compact NEGF approach for a 50 nm SBFET is illustrated in Fig. 5.4(a). The corresponding tunneling probability at the source-side SB is shown in Fig. 5.4(c), where the oscillating tunneling probability is notable. The NEGF approach-based results with the shown local density of states is only valid at temperatures of $\vartheta \approx 0\,\mathrm{K}$, since it neglects phonon scattering events inside the device. At higher temperatures the density of states would blur together, making the oscillations in the tunneling probability vanish.

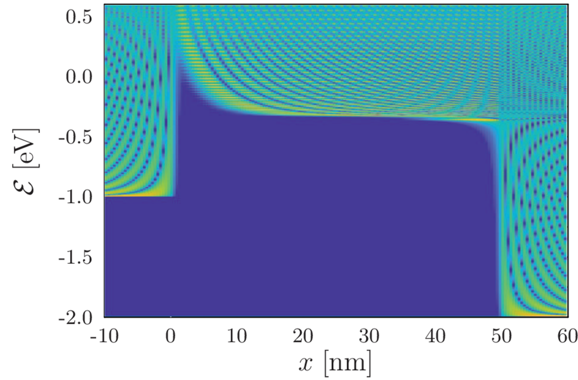
Since the NEGF method is a numerical approach, it cannot be used directly in a closed-form compact model. In order to mimic the behavior of the NEGF-based tunneling probability from Fig. 5.4(c), an empirical approach is chosen using a $\sin^2$-function. This term is incorporated into the expression of the tunneling probability from Eq. (5.26), leading to an adjusted tunneling probability T_{cryo}, which includes the oscillations:

$$\begin{aligned} T_{\mathrm{cryo}}(\mathcal{E}) &= T_{\mathrm{cryo},0}(\mathcal{E}) \cdot \sin^2\left(\omega_E \cdot \mathcal{E} + \varphi_0\right) && (5.32) \\ &= \exp\left(-c \cdot (\mathcal{E}_0 - \mathcal{E})\right) \cdot \sin^2\left(\omega_E \cdot \mathcal{E} + \varphi_0\right) \,. && (5.33) \end{aligned}$$

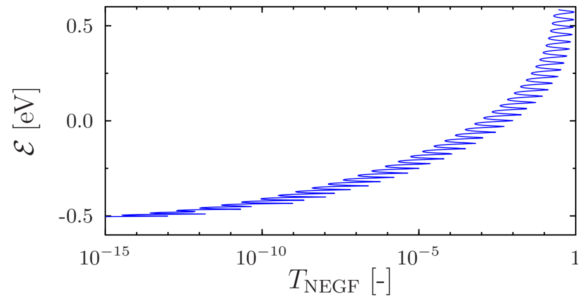
This empirical addition comes with the two fitting parameters ω_E and φ_0, used for adjusting the model's oscillation of the tunneling probability. They provide a possibility to change the oscillation's phase shift and frequency (i.e. the spacing between resonances with energy and therefore V_{gs}) and allow fitting to the measurement. Both parts of Eq. (5.32) are illustrated in Fig. 5.5.

Combining Eq. (5.25) with Eq. (5.32) for the tunneling probability and Eq. (5.28) for the supply function results in

$$\begin{aligned} J_{\mathrm{FE,n},0} = \frac{q \cdot m^* \cdot B_{\mathrm{PAT}}}{2\pi^2\hbar^3} \cdot \int\limits_{E_{\mathrm{C,min}}}^{E_{\mathrm{fs}}} & \exp\left(-c \cdot (\mathcal{E}_0 - \mathcal{E})\right) \\ & \times \sin^2\left(\omega_E \cdot \mathcal{E} + \varphi_0\right) \cdot (E_{\mathrm{fs}} - \mathcal{E}) \cdot d\mathcal{E} \,, \end{aligned} \tag{5.34}$$



(a)



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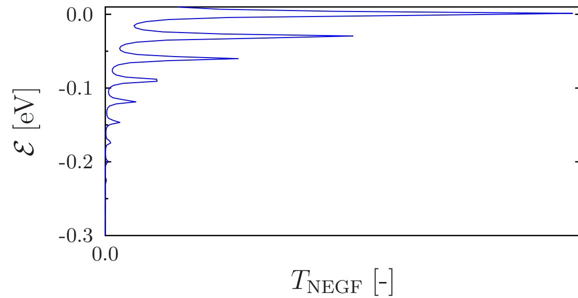


(c)

Figure 5.4: Compact NEGF simulation results performed on a 50 nm SBFET, which is described in Sec. 5.5.1. The results are taken from [88]. (a) qualitatively shows the calculated local density of states, along the channel (x-axis) and per energy (y-axis). The light blue to yellow regions indicate the presence of states. This figure is simulated at $V_{\mathrm{ds}} = 1\,\mathrm{V}$ and $V_{\mathrm{gs}} = 0.5\,\mathrm{V}$. (b) and (c) show the calculated tunneling probability per energy for the source-side SB in logarithmic (b) and linear scale (c), calculated at $\vartheta = 5.4\,\mathrm{K}$ and $V_{\mathrm{ds}} = V_{\mathrm{gs}} = 1\,\mathrm{V}$. The result in (c) shows the most important tunneling region directly below the metal's Fermi energy at 0 eV, where the oscillations show a nearly asymptotic behavior to an exponential function.

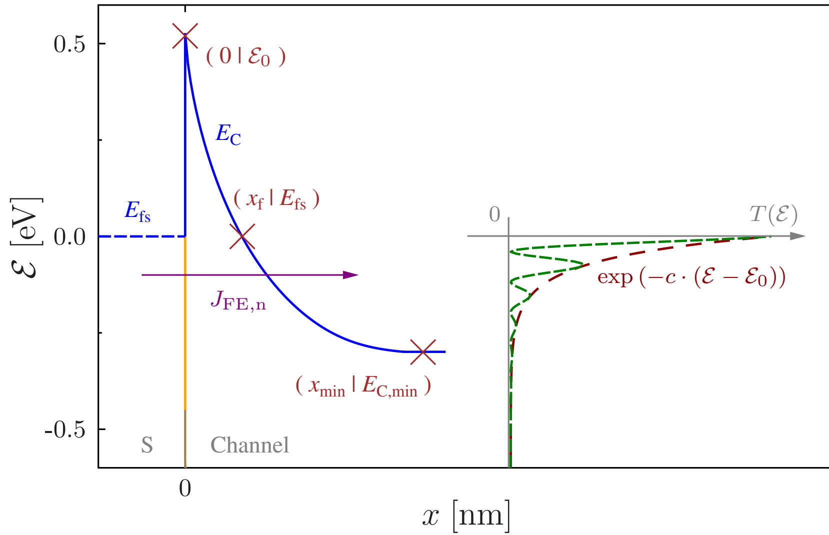


Figure 5.5: Band diagram at the source-side Schottky junction (left-hand side). The solid blue line is the conduction band of the channel, and the blue dashed line shows the metal's Fermi energy level. The right-hand side subplot shows the tunneling probability from Eq. (5.26), with the exponential part (red line) and the total probability, including the oscillations (green line).

as expression to calculate the electron FE current (the hole FE current works similarly). The integral of Eq. (5.34) can be solved in closed form, to:

$$J_{\mathrm{FE,n,0}} = \frac{q \cdot m^* \cdot B_{\mathrm{PAT}}}{2\pi^2\hbar^3} \cdot \left[j_{\mathrm{cryo}}(E_{\mathrm{fs}}) - j_{\mathrm{cryo}}(E_{\mathrm{C,min}})\right] , \tag{5.35}$$

with:

$$\begin{aligned} j_{\mathrm{cryo}}(\mathcal{E}) = \frac{\exp(-c(\mathcal{E}_0 - \mathcal{E}))}{2\left(c^3 + 4c\omega_{\mathrm{E}}^2\right)^2} \cdot \Big[& 2c^2\omega_{\mathrm{E}} \cdot (c^2(E_{\mathrm{fs}} - \mathcal{E}) + 4\omega_{\mathrm{E}}^2 \cdot (E_{\mathrm{fs}} - \mathcal{E}) + 2c) \\ \cdot \sin(-2\omega_{\mathrm{E}}\mathcal{E} + 2\varphi_0) + (c^2 + 4\omega_{\mathrm{E}}^2)^2 \cdot & (c(E_{\mathrm{fs}} - \mathcal{E}) + 1) - c^2(c^3(E_{\mathrm{fs}} - \mathcal{E}) \\ & + 4c\omega_{\mathrm{E}}^2 \cdot (E_{\mathrm{fs}} - \mathcal{E}) + c^2 - 4\omega_{\mathrm{E}}^2) \cdot \cos(-2\omega_{\mathrm{E}}\mathcal{E} + 2\varphi_0)\Big] . \end{aligned} \tag{5.36}$$

5.3.2 Modeling of Band Tail States

As an addition to the injection current from Eq. (5.34), in this model the band tail effect is added, which is a second order effect and supposed to enable carrier injection even into the band gap region, leading to a worse slope of the devices [11]. To consider the band tail effect in the equations, first, a distribution of the band tail states needs to be introduced. Since the compact model does not use any term of a density of states in its equations, the distribution used in this case is considered as a unit less factor between zero and one, where one means

that a full current density is possible, and zero means that no states are available for charge transport. This band tail states distribution g_{ts} is assumed to start at one, directly at the conduction band edge E_{C} and decreases exponentially inside the band gap region. It given by:

$$g_{\mathrm{ts}}(\mathcal{E}) = \exp\left(-\frac{E_{\mathrm{C,min}} - \mathcal{E}}{\mathcal{E}_{\mathrm{ts,fit}}}\right) , \tag{5.37}$$

with $\mathcal{E} < E_{\mathrm{C,min}}$. Here, $\mathcal{E}_{\mathrm{ts,fit}}$ is a fitting parameter for adjusting the argument of the exponential function and therefore, the subthreshold swing of the resulting device transfer characteristics. The band tail current density $J_{\mathrm{FE,n,ts}}$, which consists of carriers tunneling into the band tail states, is calculated with the approach of Eq. (5.25), including the tail states distribution Eq. (5.37) and changing the integration boundaries, as:

$$J_{\mathrm{FE,n,ts}} = \frac{q \cdot m^*}{2\pi^2\hbar^3} \cdot B_{\mathrm{PAT}} \cdot \int_{\mathcal{E}_{\mathrm{ts,min}}}^{E_{\mathrm{C,min}}} T(\mathcal{E}) \cdot (E_{\mathrm{fs}} - \mathcal{E}) \cdot g_{\mathrm{ts}}(\mathcal{E}) \cdot d\mathcal{E} \, . \tag{5.38}$$

The band tail states distribution, and its boundaries are visualized in Fig. 5.6. The lower integration boundary is given by $\mathcal{E}_{\mathrm{ts,min}} = E_{\mathrm{C,min}} - \alpha_{\mathrm{ts}} \cdot E_{\mathrm{g}}$, where α_{ts} is an adjustable fitting parameter in a range of zero to one and limits the tunneling depth inside the band gap.

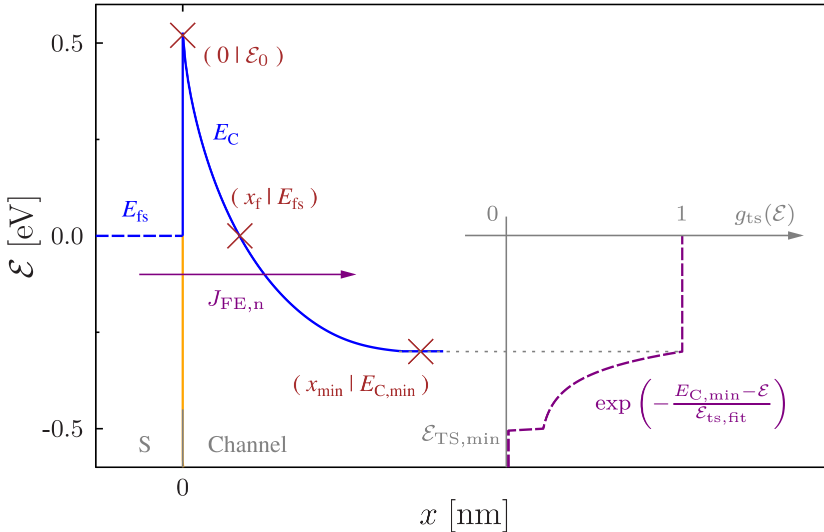


Figure 5.6: Band diagram at the source-side Schottky junction (left-hand side). The solid blue line is the conduction band of the channel, and the blue dashed line shows the metal's Fermi energy level. The right-hand side subplot shows the band tail states distribution, according to Eq. (5.37), which is used in the model. The tail states distribution is used at energy levels below $E_{\mathrm{C,min}}$ in the band gap. A constant value of one above $E_{\mathrm{C,min}}$ indicates, that there are no band tail states, but the full tunneling process happens instead.

Equation Eq. (5.38) can be solved with the existing model solutions by incorporating the tail states distribution Eq. (5.37) into the tunneling probability $T_{\mathrm{cryo}}(\mathcal{E})$, given as:

$$T_{\mathrm{ts}}(\mathcal{E}) = T_{\mathrm{cryo}}(\mathcal{E}) \cdot g_{\mathrm{ts}}(\mathcal{E}) = \exp\left(-c' \cdot (\mathcal{E}_0' - \mathcal{E})\right) , \tag{5.39}$$

with:

$$\begin{aligned}
T_{\mathrm{ts}}(\mathcal{E}) &= \exp\left(-c \cdot (\mathcal{E}_0 - \mathcal{E})\right) \cdot \exp\left(-\mathcal{E}_{\mathrm{ts,fit}}^{-1} \cdot (E_{\mathrm{C,min}} - \mathcal{E})\right) && (5.40)\\
&= \exp\left(-c \cdot \mathcal{E}_0 + c \cdot \mathcal{E} - \mathcal{E}_{\mathrm{ts,fit}}^{-1} \cdot E_{\mathrm{C,min}} + \mathcal{E}_{\mathrm{ts,fit}}^{-1} \cdot \mathcal{E}\right) && (5.41)\\
&= \exp\left(-c \cdot \mathcal{E}_0 - \mathcal{E}_{\mathrm{ts,fit}}^{-1} \cdot E_{\mathrm{C,min}} + (c + \mathcal{E}_{\mathrm{ts,fit}}^{-1}) \cdot \mathcal{E}\right) && (5.42)\\
&= \exp\left((c + \mathcal{E}_{\mathrm{ts,fit}}^{-1}) \cdot \left(\frac{c \cdot \mathcal{E}_0 + \mathcal{E}_{\mathrm{ts,fit}}^{-1} \cdot E_{\mathrm{C,min}}}{c + \mathcal{E}_{\mathrm{ts,fit}}^{-1}} - \mathcal{E}\right)\right) && (5.43)\\
&= \exp\left(-c' \cdot (\mathcal{E}_0' - \mathcal{E})\right) . && (5.44)
\end{aligned}$$

So, the rearranging leads to:

$$c' = c + \frac{1}{\mathcal{E}_{\mathrm{ts,fit}}} , \tag{5.45}$$

and:

$$\mathcal{E}_0' = \frac{c \cdot \mathcal{E}_0 + \dfrac{E_{\mathrm{C,min}}}{\mathcal{E}_{\mathrm{ts,fit}}}}{c + \dfrac{1}{\mathcal{E}_{\mathrm{ts,fit}}}} . \tag{5.46}$$

Since Eq. (5.39) has the same shape as the exponential part of Eq. (5.32), it can be used in the closed form solution Eq. (5.35), but with c' instead of c, $\mathcal{E}_0'$ instead of $\mathcal{E}_0$ and the adjusted boundaries ($\mathcal{E}_{\mathrm{ts,min}}$ instead of $E_{\mathrm{C,min}}$ and $E_{\mathrm{C,min}}$ instead of E_{fs}). With the inclusion of the tail states, the total injection current density can be expressed as

$$J_{\mathrm{FE,n}} = J_{\mathrm{FE,n,0}} + J_{\mathrm{FE,n,ts}} . \tag{5.47}$$

The result of the modeled band tail effect on the calculated characteristics can be seen in Fig. 5.11(a) from the results section. In this figure the solid red lines show the results including and the dotted red lines show the results excluding the modeled band tail effect.

5.3.3 Inclusion of Channel Resistance

In the SBFET model for room temperature environment, a channel MOSFET addition is added in Sec. 4.4 which leads to a drain current saturation at high bias voltages. For a validation of

measured output characteristics, this addition has been used for the cryogenic SBFET model with the adjusted equation from Eq. (4.44), as:

$$I_{\mathrm{MOS}} = 2\mu \frac{W_{\mathrm{ch}}}{L_{\mathrm{ch}}} \cdot \lim_{\vartheta \to 0} \left[\frac{k_{\mathrm{b}}\vartheta}{q} \cdot \left(Q'_{\mathrm{s}} - Q'_{\mathrm{d}} \right) + \frac{Q'^2_{\mathrm{s}} - Q'^2_{\mathrm{d}}}{2 \cdot C'_{\mathrm{ox},\check{}}} \right] \tag{5.48}$$

$$= 2\mu \frac{W_{\mathrm{ch}}}{L_{\mathrm{ch}}} \cdot \frac{Q'^2_{\mathrm{s}} - Q'^2_{\mathrm{d}}}{2 \cdot C'_{\mathrm{ox},\check{}}} , \tag{5.49}$$

which takes out the diffusion current component from the MOSFET equation. For the charges Q'_{s} and Q'_{d}, Eq. (4.45) and Eq. (4.46) are used.

5.4 Total Current of the Cryogenic SBFET

In order to calculate the total device current, not only the injection side (source side), but also the drain side is considered. For the calculation of the total current density, the method from Sec. 4.3 has been used which is given by:

$$J_{\mathrm{FE,tot}} = \begin{cases} J_{\mathrm{FE,s,n}} - J_{\mathrm{FE,d,n}}, & E_{\mathrm{x}}(x = L_{\mathrm{ch}}) < 0 \\ J_{\mathrm{FE,s,n}} + J_{\mathrm{FE,d,p}}, & E_{\mathrm{x}}(x = L_{\mathrm{ch}}) \geq 0 \end{cases} . \tag{5.50}$$

In this case the injection current density $J_{\mathrm{FE,s,n}}$ is calculated by Eq. (5.47) at the source side and $J_{\mathrm{FE,d,n/p}}$ is the injection current density at the drain side, consisting either of electrons for a permeable SB at the conduction band, or holes for a permeable SB at the valence band.

Finally, with the device geometries the total device's drain current I_{ds} is determined by:

$$I_{\mathrm{ds}} = W_{\mathrm{ch}} \cdot t_{\mathrm{ch}} \cdot t_{\mathrm{eff,FE}} \cdot J_{\mathrm{FE,tot}} , \tag{5.51}$$

for DG structures, with the channel width W_{ch} and thickness t_{ch}. For nanowire structures it is given as:

$$I_{\mathrm{ds}} = C_{\mathrm{NW}} \cdot R_{\mathrm{NW}} \cdot t_{\mathrm{eff,FE}} \cdot J_{\mathrm{FE,tot}}, \tag{5.52}$$

using the nanowire's circumference C_{NW} and the averaged radius R_{NW}. The parameter $t_{\mathrm{eff,FE}}$ is the effective thickness in which the on-current is supposed to be flowing.

5.5 Model Results

The compact model results from the cryogenic SBFET model are compared to measurements, in this section [85]. The results are separated into a model comparison to measurements of ultra-thin body and buried oxide SOI SBFETs from [85] in Sec. 5.5.1 and a comparison to measurements of nanowire SBFETs from [86] in Sec. 5.5.2. TCAD studies on devices at $\vartheta \approx 0\,\mathrm{K}$ are not presented here, because of convergence problems of the simulations in the given temperature environment.

5.5.1 Model Results Compared to SOI SBFETs

Figure 5.8 and Fig. 5.9 show the compact model compared to p-type measurements performed on ultra-thin body and buried oxide SOI SBFETs from [8], of which a schematic cross-section is presented in Fig. 5.7. The devices consist of source and drain regions made of nickel silicide and a lightly p-doped silicon channel ($N_\mathrm{A} = 1 \times 10^{15}\,\mathrm{cm}^{-3}$) [8]. The channel doping of the devices is neglected in the compact model at deep cryogenic temperatures because the dopants are expected to be frozen out. The gate oxide has a thickness of about $t_\mathrm{ox} = 5\,\mathrm{nm}$ made of $\mathrm{HfO_2}$, and the gate material is TiN [8]. All measured devices have a channel width of $W_\mathrm{ch} = 800\,\mathrm{nm}$, a channel thickness of $t_\mathrm{ch} = 12\,\mathrm{nm}$ and vary in their channel length L_ch.

The presented compact model is compared to measurements for devices with a channel length of $L_\mathrm{ch} = 30\,\mathrm{nm}$ (transfer characteristics, Fig. 5.8(a)), $L_\mathrm{ch} = 70\,\mathrm{nm}$ (transfer characteristics, Fig. 5.8(b)), and $L_\mathrm{ch} = 50\,\mathrm{nm}$ (transfer and output characteristic, Fig. 5.9(a), and Fig. 5.9(b)). The used model parameters (geometrical, material, and fitting parameters) are listed in Tab. 5.1. In this first modeling attempt for cryogenic SBFETs, originally presented in [85], the 2D potential model from Sec. 4.1 is used for the model, instead of the simplified potential model from Sec. 5.1. Additionally, the impact of the band tail states has been neglected. The fitting parameters have been adapted manually in order to obtain the best agreement with the measurement data. Since the measured devices have a single-gate structure and the compact model is made for DG devices, the compact model was calculated with twice the channel thickness and the resulting current was halved.

The results of the model for the three devices show a good agreement with the measurements. Only the curvature and slope in the subthreshold region of the characteristics show a slight deviation, where the model's slope is too steep, and the curvature is not exactly fitting to the measured data.

As it can be seen in Tab. 5.1, for the 50 nm device, the model parameter for the oxide thickness was slightly increased, which has the effect to reduce that steepness and fit the model's slope to the measurements, since the band tail effect is not included here. Additionally, the band gap (E_g) has been increased to provide a better fit between model and measurement

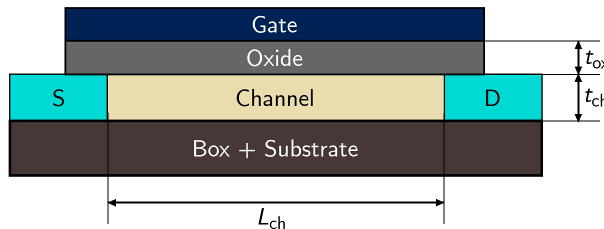


Figure 5.7: Schematic cross-section of the measured devices. The relevant geometrical parameters are shown. Values of the devices under investigation are presented in Tab. 5.1

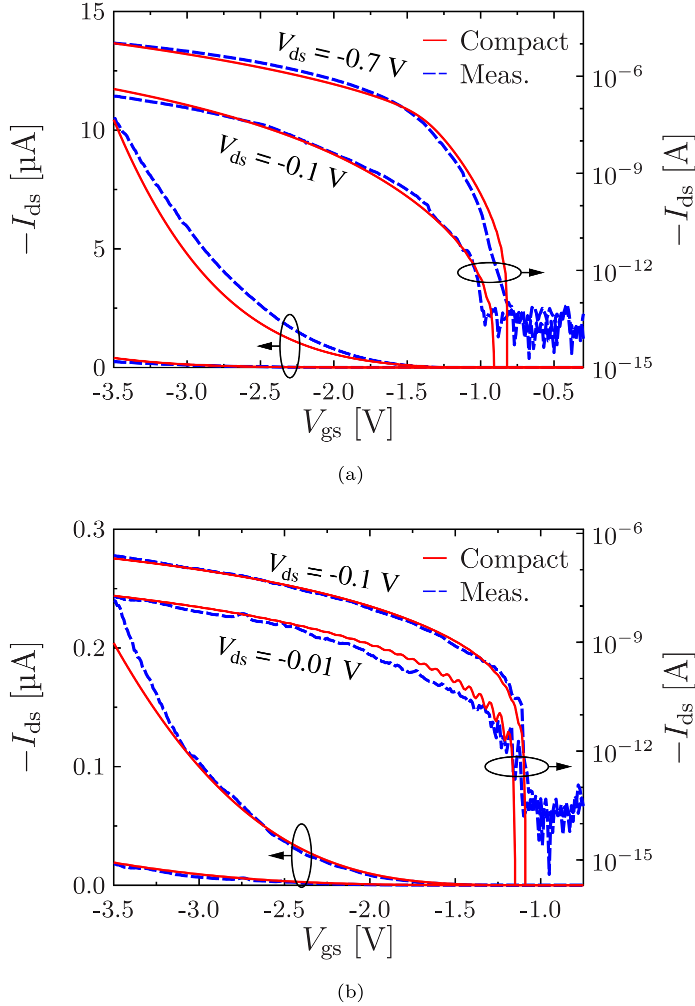
Table 5.1: Device parameters of the devices under investigation in Fig. 5.8 and Fig. 5.9

Parameter	30 nm Dev.	50 nm Dev.	70 nm Dev.
L_{ch} [nm]	36	50	70
W_{ch} [nm]	800	800	800
t_{ch} [nm]	12	12	12
t_{ox} [nm]	5.00	5.65	5.00
$t_{\mathrm{eff,FE}}$ [-]	0.2	0.2	0.2
$\varepsilon_{\mathrm{r,ox}}$ [-]	22.0	22.0	22.0
$\varepsilon_{\mathrm{r,sc}}$ [-]	11.7	11.7	11.7
E_{g} [eV]	1.1696	1.2281	1.1696
$\Phi_{\mathrm{B,n}}$ [V]	0.5800	0.6090	0.5800
$\Phi_{\mathrm{B,p}}$ [V]	0.5896	0.6191	0.5896
m_{p} [-]	0.900	0.810	0.900
B_{PAT} [-]	1.7×10^{-3}	5.0×10^{-4}	6.2×10^{-6}
V_{fb} [V]	-0.20	0.00	-0.47
$\omega_E/(2\pi)$ [eV^{-1}]	20	20	20
φ_0 [-]	0	0	0
α [-]	0.7	0.7	0.7

in the subthreshold region. An increasing band gap of silicon for cryogenic temperatures has also been reported in [9, 90]. It is also notable that the channel length for the 30 nm device was calculated by the model using 36 nm. A further reduction of the channel length leads to an impact on the used 2D potential model, as the potential profile of the drain-side's SB interacts with the source side. Additionally, the 2D potential model gets more inaccurate, the more the channel length approaches the channel thickness [29, 31, 82].

The resonance effect, caused by the $\sin^2$-addition in Eq. (5.26), is mostly pronounced at low drain voltages, as it can be seen in Fig. 5.8(b) at $V_{\mathrm{ds}} = -0.01\,\mathrm{V}$. The harmonic oscillation of the model does not entirely fit to the measured curves but is still a useful method to include quantum oscillations. However, it can also be observed that in certain cases (for example in the measurement of Fig. 5.9(a), $V_{\mathrm{ds}} = -0.1\,\mathrm{V}$ and $V_{\mathrm{gs}} \approx -2.0\,\mathrm{V}$) there are oscillations occurring at higher voltages, which are not covered by the model and might be attributed to other phenomena, which have not been included yet into the model.

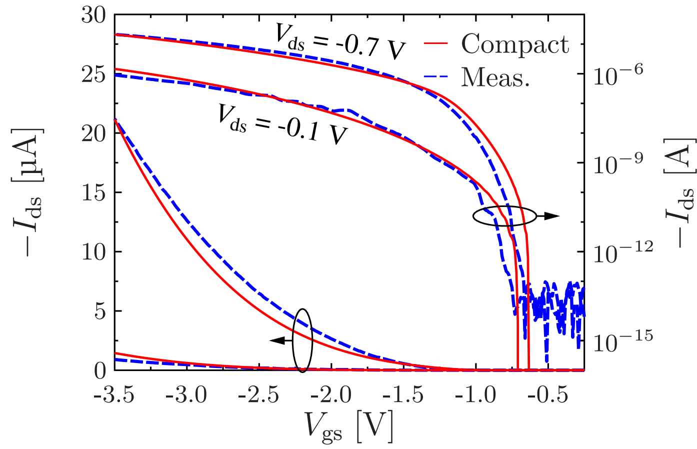
The output characteristics (Fig. 5.9(b)) in the given bias range also show a good agreement of the compact model compared to the measured curve. However, for this set of measurements only one output curve is available.



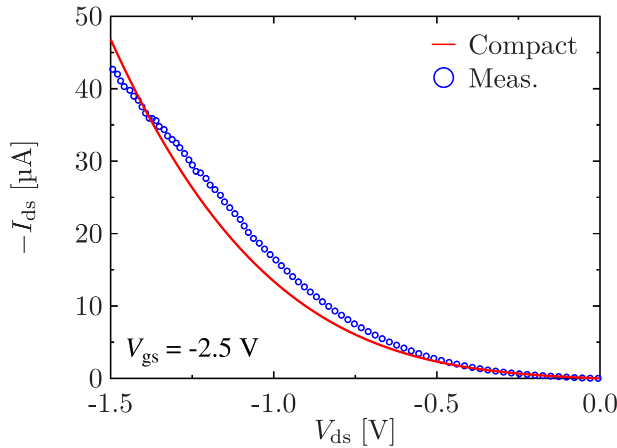
(a)

(b)

Figure 5.8: P-type device characteristics of SBFETs with various channel lengths and drain voltages calculated with the compact model (solid red lines) and compared to measurements (dashed blue lines) in linear and logarithmic scale. The devices' back gate voltage is $V_{bg} = 0\,V$ in the measurements. It is neglected in the compact model, which in agreement to [8] has a negligible influence on the device current for deep cryogenic temperatures. (a) SBFET transfer characteristics with a channel length of $L_{ch} = 30\,nm$, measured at $\vartheta = 5.3\,K$. (b) SBFET transfer characteristics with a channel length of $L_{ch} = 70\,nm$, measured at $\vartheta = 5.3\,K$.



(a)



(b)

Figure 5.9: P-type device characteristics of SBFETs with various channel lengths and drain voltages calculated with the compact model (solid red lines) and compared to measurements (dashed blue lines) in linear and logarithmic scale. The devices' back gate voltage is $V_{bg} = 0\,V$ in the measurements. It is neglected in the compact model, which in agreement to [8] has a negligible influence on the device current for deep cryogenic temperatures. (a) SBFET transfer and (b) output characteristics with a channel length of $L_{ch} = 50\,nm$, measured at $\vartheta = 5.6\,K$.

5.5.2 Model Results Compared to Nanowire SBFETs

In this section the compact model is compared to measurements of nanowire SBFETs [86]. The devices are lightly-doped silicon elliptical-shaped nanowire SBFETs with nickel silicide as source/drain materials and a HfO_2/SiO_2 oxide stack, followed up by a TiN gate [11]. The important device geometries and the used model parameters can be found in Tab. 5.2. The compact model results are obtained by using the potential model from Sec. 5.1 and all of the discussed second order effects form Sec. 5.3. The model's fitting parameters have been adapted manually for a good agreement with the measured data. A schematic slice of a nanowire SBFET is shown in Fig. 5.10. The channel doping of the devices is neglected in the compact model at deep cryogenic temperatures because the dopants are expected to be frozen out.

Fig. 5.11(a) shows the results of a p-type SBFET as transfer characteristics for $V_{\mathrm{ds}} = -0.1\,\mathrm{V}$ and $-0.4\,\mathrm{V}$. The total device current is normalized to the approximated nanowire circumference. As it can be seen in the results, the compact model results show a good agreement to the measurements. The subthreshold part of the characteristics is fitted using the band tail model from Sec. 5.3.2. The difference between the model with and without band tail addition is shown in Fig. 5.11(a) (solid vs dotted lines). The oscillations, that are provided by the model and that are especially notable in the linear characteristics, are not entirely in phase with the oscillating measurements. It can be seen that for $V_{\mathrm{ds}} = -0.1\,\mathrm{V}$ and $-1.1\,\mathrm{V} > V_{\mathrm{gs}} > -0.8\,\mathrm{V}$ the oscillations are in phase, while they are drifting apart for higher (negative) gate voltages. Also, at $V_{\mathrm{ds}} = -0.4\,\mathrm{V}$ the model's oscillations are overpronounced. This shows that the simplified oscillation model cannot capture the effects entirely, yet, but gives a good approximation to measured effects.

Figure 5.11(b) shows the result of the n-type SBFET as transfer and Fig. 5.12 as output characteristics at various bias conditions. Both characteristics also show a good agreement, in general. Since for this case there is not a huge number of oscillations (at least in the transfer curves), the model was fitted so it also barely shows oscillations. In the output characteristics of Fig. 5.12(a) slight deviations are visible for lower V_{ds}. This could indicate ohmic contact resistances which are not covered by the compact model, yet.

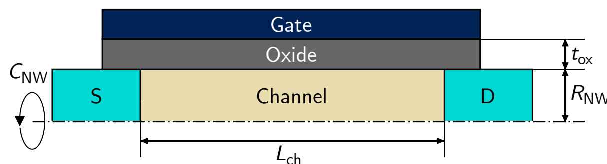


Figure 5.10: Schematic slice of one half of the nanowire SBFET which is used for compact modeling and is similar to the measured devices. The relevant geometric parameters are shown. C_{NW} corresponds to the nanowire channel's circumference. Values of the devices under investigation are shown in Tab. 5.2.

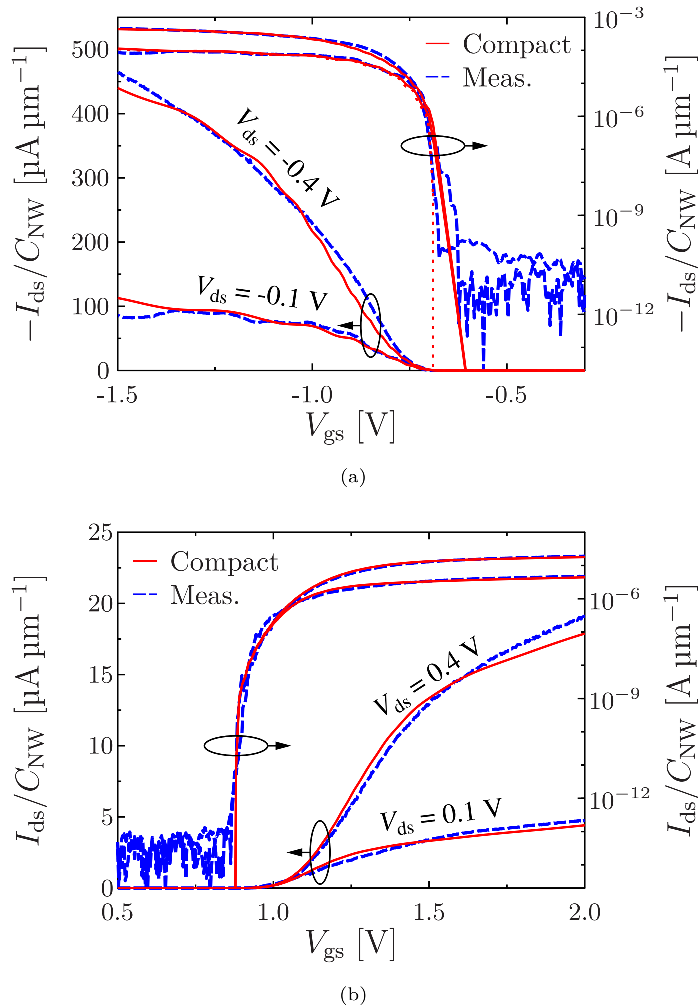


Figure 5.11: Compact model result (solid red lines) vs measurements (dashed blue lines) of nanowire SBFETs, performed at $\vartheta = 5.5\,\mathrm{K}$. The device geometries and model parameters can be found in Tab. 5.2. The shown transfer characteristics are presented in linear and logarithmic scale for the given drain voltages The current is normalized to the nanowire's circumference C_{NW}. (a) n-type transfer characteristics of the $L_{\mathrm{ch}} = 70\,\mathrm{nm}$ device (from [11]). (b) p-type transfer characteristics of the $L_{\mathrm{ch}} = 100\,\mathrm{nm}$ device

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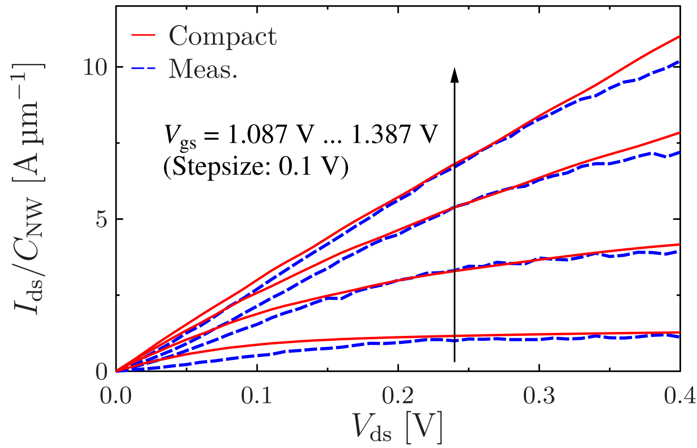
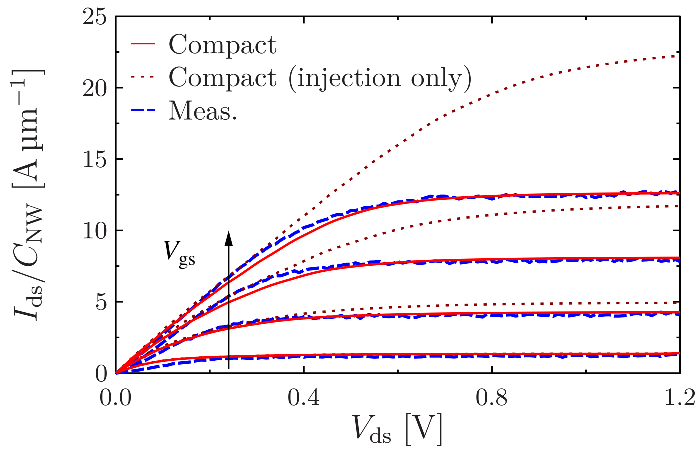


(a)



(b)

Figure 5.12: Compact model result (red solid lines) vs n-type measurement (blue dashed lines) of the $L_{ch} = 70\,\text{nm}$ n-type nanowire SBFET, performed at $\vartheta = 5.5\,\text{K}$. The device geometries and model parameters can be found in Tab. 5.2. The output characteristics are shown for the given gate voltages. The current is normalized to the nanowire's circumference C_{NW}. (a) presents a lower V_{ds} section of the characteristics which is calculated by the injection model only. (b) presents the full measured V_{ds} range using the same V_{gs} values as in (a). In this result the red dotted lines are calculated using the injection model only. The red solid lines show the results including the channel resistance addition from Sec. 5.3.3.

Finally, Fig. 5.12(b) shows the model results of the n-type nanowire measurement with an extended V_{ds} range up to 1.2 V. In this part the channel resistance model from Sec. 5.3.3 is included (solid red lines) and compared to using the injection model only (dotted red lines). The parameters for the channel resistance model are shown in the lower section of Tab. 5.2. As it can be seen in the results, using only the injection model is not sufficient to capture the entire V_{ds} range, because it overestimates the current. In contrast to this, the Channel MOSFET addition limits the calculated drain currents very well. Although, it has to be noticed that the electron mobility for the channel needed to be reduced in order to fit the characteristics. This reduction does not fit to the reported intrinsic semiconductor behavior [91], but it has been shown that the mobility for doped silicon close to absolute zero can get massively reduced, due to ionized impurity scattering [92]. So, reasons for the reduced electron mobility could be the ionized impurity scattering or quantum confinement effects, due to the small nanowire's diameter.

Table 5.2: Device parameters of the devices under investigation in Fig. 5.11 and Fig. 5.12

Parameter	P-type Dev.	N-type Dev.
L_{ch} [nm]	70	100
R_{NW} [nm]	2.6	2.3
C_{NW} [nm]	16.5	14.1
t_{ox} [nm]	5.5	5.5
$t_{eff,FE}$ [-]	0.2	0.2
$\varepsilon_{r,ox}$ [-]	17.1	17.1
$\varepsilon_{r,sc}$ [-]	11.7	11.7
E_g [eV]	1.1696	1.1696
$\Phi_{B,n}$ [V]	0.5800	0.5800
$\Phi_{B,p}$ [V]	0.5896	0.5896
λ [nm]	2.18	2.18
ΔV_{bound} [V]	0.1	0.1
γ_{sat} [-]	10	10
$m_{p/n}$ [-]	0.081	0.081
B_{PAT} [-]	7.43×10^{-3}	3.15×10^{-4}
V_{fb} [V]	-0.095	0.420
$\omega_E/(2\pi)$ [eV^{-1}]	18	20
φ_0 [-]	0	0
$\mathcal{E}_{ts,fit}$ [meV]	5.0	66.7
α_{ts} [-]	0.50	0.11
V_{T0} [V]	-	0.38
S [mV/dec.]	-	60
γ_{MOS} [-]	-	4
μ_n [cm^2 V^{-1} s^{-1}]	-	1.26

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CHAPTER 6

Compact Modeling of Reconfigurable Field-Effect Transistors

In this section the adaption of the room temperature compact model, introduced in Chapter 4, to a compact model covering RFETs is explained. The difficulty of modeling RFETs compared to SBFET is the introduction and inclusion of (at least) one additional gate electrode. Additional electrodes lead to an increased complexity of the model equation, since for all possible bias conditions the model needs to output a valid result, while fulfilling the basic rules for compact models.

Another point that needs to be considered is the type of RFET that shall be described by the model. As it is shown in Sec. 3.3.3, there are multiple different structures that are called RFET. All of these devices have a similar goal of using an additional gate as polarity gate, but they vary in the way this goal is achieved and can also vary in their characteristics. This means that a compact model that offers a very detailed physical description of a certain RFET type A, might be very inaccurate on another type B.

This chapter is split into two main sections. The first section (Sec. 6.1) focuses only on compact modeling of the dually-gated RFET variation, while keeping a constant polarity gate voltage [81–83]. The second part (Sec. 6.2) discusses some approaches for other device structures and more than one steady gate.

6.1 Compact Model for Fix-Programmed Dually-Gated RFETs

This section describes the adaption of the room temperature compact model to fix-programmed RFETs. The devices covered by this model addition are the dually-gated RFETs, which are introduced in Sec. 3.3.1. The contents and results of this section is published in [81–83].

The first step of the model adaption is to split up the one gate of the SBFET model into two gates of the dually-gated RFET - the source-side and the drain-side gate, and considering the impact on the potential model. This is described in Sec. 6.1.1.

In the next step, described in Sec. 6.1.2, the channel resistance addition from Sec. 4.4 is extended for the RFET, in order to consider the channel resistance of the ungated region in the covered devices.

Section 6.1.3 explains the calculation of the final device current, considering either a charge-carrier type suppression by the second gate, or the usage of the RFET as SBFET.

Finally, the model results compared to TCAD simulations and measurements are shown and discussed in Sec. 6.1.4. The RFET measurements have been provided by Technische Universität Dresden and NaMLab gGmbH.

6.1.1 Injection Model Extension for two Independent Gates

The dually-gated RFET variation, as described in Sec. 3.3, has a similar structure to a SBFET, but with the single gate split up into a source-side and a drain-side gate, which leads to an additional input voltage for the compact model. When running a RFET in the on-state, the injection side for the main charge-carrier type (either electrons or holes) is the source side of the device, where the source-side gate is considered to be the CG, with the applied V_{cg} voltage. The second gate (drain-side gate) with its applied PG voltage V_{pg} is used to suppress the other carrier type, when programmed to a fixed voltage of $V_{\mathrm{pg}} \gg 0$ for suppressing a hole current and $V_{\mathrm{pg}} \ll 0$ for suppressing an electron current.

For the implementation of both gates, the 2D potential model used in the model, which is introduced in Sec. 2.1.4 and used in Sec. 4.1, is adjusted for the second gate. In the potential model of Sec. 2.1.5, the gate voltage is considered as boundary condition in the source-related potential Eq. (2.35) and the drain related potential Eq. (2.36). In case of the RFET, the source and drain related cases are considered by using the corresponding gate voltage, so V_{cg} for $\phi_{\mathrm{2D,s}}(x,y)$ and V_{pg} for $\phi_{\mathrm{2D,d}}(x,y)$. In the 2D potential model for the SBFET the two calculated potentials are added together in the last step (Eq. (2.37)), which supports potential overlapping in short channel SBFETs. In case of the RFET, it is not expected to have a comparably short channel device, since both gate of the device need to have a certain distance from each other. Therefore, the step from Eq. (2.37) is left out in the RFET model and the next step, which are the auxiliary potentials from Eq. (4.8) to Eq. (4.15) are calculated using Eq. (2.35) for the source side or Eq. (2.36) for the drain side instead.

The current calculation for the RFET model works similar to the SBFET model. It needs to be considered that, due to the potential model adjustments, there is an unsteadiness in the channel potential at $L_{\mathrm{ch}}/2$, which leads to two solutions for the potentials $\Phi_{\mathrm{cen,L/2}}$ and $\Phi_{\mathrm{sur,L/2}}$ in the middle of the device. This needs to be considered in the TE current calculation, so Φ_{bar} of Eq. (4.40) considers the maximum of the source or drain-related case, now.

The current balancing model from Eq. (4.41) is also still used in the RFET model. However, it needs to be mentioned that this model only works properly in the programmed case with

$V_{\mathrm{ds}} \approx V_{\mathrm{pg}}$, or in the SBFET use case with $V_{\mathrm{cg}} = V_{\mathrm{pg}}$. In case of a different polarity of V_{cg} and V_{pg}, the addition of Sec. 6.1.3 needs to be considered. The current RFET model state does not fully support a steady variation of the PG.

6.1.2 Modeling of the Ungated Channel Impact

In Sec. 4.4, the channel resistance inclusion into the SBFET model is explained. This unwanted second-order effect is given by a resistance of the device's channel at high voltages and high channel length, so the injection model is not sufficient to describe the transistor's characteristics. For RFETs the channel resistance is supposed to be even more impactful, since they have ungated regions, between the CG and PG, given by the CG-to-PG distance L_{ung}. Within this ungated region the electrostatic coupling of the channel surface to the gates diminishes drastically, which leads to less accumulated charge carriers that can contribute to the transistor's current flow. This has been investigated in the TCAD simulation shown in Sec. 3.3.2.2. For the modeled RFET, the equations from Sec. 4.4 are adopted, but with some modifications. First, Eq. (4.44) is slightly adjusted, as:

$$I_{\mathrm{MOS}} = 2\mu \frac{W_{\mathrm{ch}}}{L_{\mathrm{ch}}} \cdot \left[\frac{k_{\mathrm{b}}\vartheta}{q} \cdot \left(Q'_{\mathrm{s}} - Q'_{\mathrm{d}}\right) + \frac{Q'^{2}_{\mathrm{s}} - Q'^{2}_{\mathrm{d}}}{2 \cdot C'_{\mathrm{ox},\kappa}} \right] , \tag{6.1}$$

where C'_{ox} is replaced by $C'_{\mathrm{ox},\kappa}$, defined as:

$$C'_{\mathrm{ox},\kappa} = \kappa_{\mathrm{ung}} \cdot \frac{\varepsilon_{\mathrm{ox}}}{t_{\mathrm{ox}}} . \tag{6.2}$$

The parameter κ_{ung} is a fitting parameter smaller or equal than one representing the missing gate coverage in RFET devices and therefore, the much higher ungated channel resistance. The reduced gate coupling in the ungated region is illustrated in Fig. 6.1.

In order to obtain an average gate voltage for a dually gated RFET, a replacing gate voltage for the modeled channel MOSFET is calculated by:

$$\tilde{V}_{\mathrm{gs,MOS}} = \frac{V_{\mathrm{cg}} + V_{\mathrm{pg}}}{2} . \tag{6.3}$$

Both charge densities of Eq. (6.1) are similarly defined as in Eq. (4.45) and Eq. (4.46), but including the average channel MOSFET gate voltage and $C'_{\mathrm{ox},\kappa}$, as:

$$Q'_{\mathrm{s}} = \frac{S}{\ln(10)} \cdot C'_{\mathrm{ox},\kappa} \cdot W_0 \left(\exp\left(\frac{\tilde{V}_{\mathrm{gs,MOS}} - V_{\mathrm{T0}}}{S/\ln(10)} \right) \right) , \tag{6.4}$$

and with $\tilde{V}_{\mathrm{gd,MOS}} = \tilde{V}_{\mathrm{gs,MOS}} - V_{\mathrm{ds}}$

$$Q'_{\mathrm{d}} = \frac{S}{\ln(10)} \cdot C'_{\mathrm{ox},\kappa} \cdot W_0 \left(\exp\left(\frac{\tilde{V}_{\mathrm{gd,MOS}} - V_{\mathrm{T0}}}{S/\ln(10)} \right) \right) . \tag{6.5}$$

With this channel resistance model adjustments, this second-order effect can be used for the RFET model. For the inclusion of this model addition, Eq. (4.48) is used, as for the SBFET model.

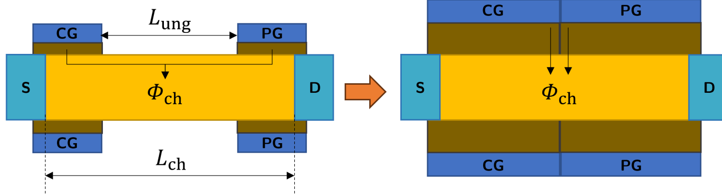


Figure 6.1: Electrostatic impact of the RFET's gates on the ungated channel. The left-hand side figure shows the electrostatic coupling of the gates on the ungated channel area, which is reduced due to the distance to the gates. The right-hand side figure is the compact model's used substitution. The reduced $C'_{\mathrm{ox},\kappa}$ is represented by an increased oxide thickness in the figure.

6.1.3 Program Gate Induced Carrier Suppression

One important step of the RFET model that needs to be discussed is the polarity reconfigurability. In order to make the model applicable to RFETs, that have been configured as n-type or p-type, one of the two charge-carrier types need to get suppressed in the FE current calculation, depending on the PG bias. This is done by using the total FE injection current Eq. (4.41), with a modification, as:

$$J_{\mathrm{FE,tot}} = \begin{cases} s_{\mathrm{n}} \cdot J_{\mathrm{FE,s,n}} - s_{\mathrm{n}} \cdot J_{\mathrm{FE,d,n}}, & E_{\mathrm{x}}(x = L_{\mathrm{ch}}) < 0 \\ s_{\mathrm{n}} \cdot J_{\mathrm{FE,s,n}}, & E_{\mathrm{x}}(x = L_{\mathrm{ch}}) = 0 \\ s_{\mathrm{n}} \cdot J_{\mathrm{FE,s,n}} + s_{\mathrm{p}} \cdot J_{\mathrm{FE,d,p}}, & E_{\mathrm{x}}(x = L_{\mathrm{ch}}) > 0 \end{cases} . \tag{6.6}$$

The introduced coefficients s_{n} and s_{p} represent the current programming status of the modeled device and can have the exact values of 0 or 1, where s_{n} activates or deactivates the electron current contributions and s_{p} activates or deactivates the hole current contributions. The system works similarly for holes as main injection current, in case $V_{\mathrm{ds}} < 0$.

There are three different operation modes for the current model implementation. In case of $V_{\mathrm{pg}} \gg 0$ the device is supposed to be in n-type operation mode which results in $s_{\mathrm{n}} = 1$ and $s_{\mathrm{p}} = 0$ in the compact model. In case of $V_{\mathrm{pg}} \ll 0$ the device is supposed to be in p-type operation mode which results in $s_{\mathrm{n}} = 0$ and $s_{\mathrm{p}} = 1$ in the compact model. The third valid option is setting $s_{\mathrm{n}} = s_{\mathrm{p}} = 1$, which results in using the RFET as a regular SBFET, as if $V_{\mathrm{pg}} = V_{\mathrm{cg}}$.

6.1.4 Model Results

The model verification is done by a combination of TCAD simulations and measurements [82]. Therefore, the measurement of the device from [66] is used. In order to obtain results for a SBFET including the symmetric device behavior, the TCAD simulation from [67] is used to simulate a device with various bias conditions. Tab. 6.1 shows the geometric, material, and fitting parameters that are used for the compact model. The model results have been obtained by using the injection model only, while neglecting the channel resistance. For this calculation, the 2D potential model in combination with the effective gate-source voltage according to Eq. (4.1) is used. The fitting of the compact model has been done by a manual parameter variation, as in the previous fits. While the real and the simulated structures are gate-all-around nanowire structures, the compact model calculates a double gate structure. Therefore, in the model a channel width W_{ch} is used which is in the same order of magnitude than the nanowire's diameter. The discrepancy between those two structures is compensated by the model's fitting parameters.

Figure 6.2 shows the device transfer characteristics with the actual measurement, the corresponding TCAD fit and the model fit, in linear and logarithmic scale. Figure 6.2(a) shows the p-configured version with a program gate voltage of $V_{\mathrm{pg}} = -2\,\mathrm{V}$ and a drain voltage of $V_{\mathrm{ds}} = -2\,\mathrm{V}$. Figure 6.2(b) shows the n-configured version with a program gate voltage of $V_{\mathrm{pg}} = 2\,\mathrm{V}$ and a drain voltage of $V_{\mathrm{ds}} = 2\,\mathrm{V}$. The model shows a good agreement compared to the TCAD simulation results. There are slight deviations in the p-type characteristics, because of the unsteadiness in the measured curve. Figure 6.3 to Fig. 6.4 depict various TCAD simulation scenarios compared to the model. They show the same transfer characteristics as Fig. 6.2, but with additional drain voltages. Figure 6.5 shows the results of the RFET used as SBFET model results. In these two simulations the PG was not fixed but biased similarly to the CG ($V_{\mathrm{pg}} = V_{\mathrm{cg}}$), which leads to a device behavior like a SBFET. Figure 6.6 shows one simulated output characteristics per operation mode (with a fixed PG voltage). Although the model shows some deviations in the curvature, which may be attributed to the neglected effect of current control by the channel conductivity, the overall behavior is well captured by the compact model.

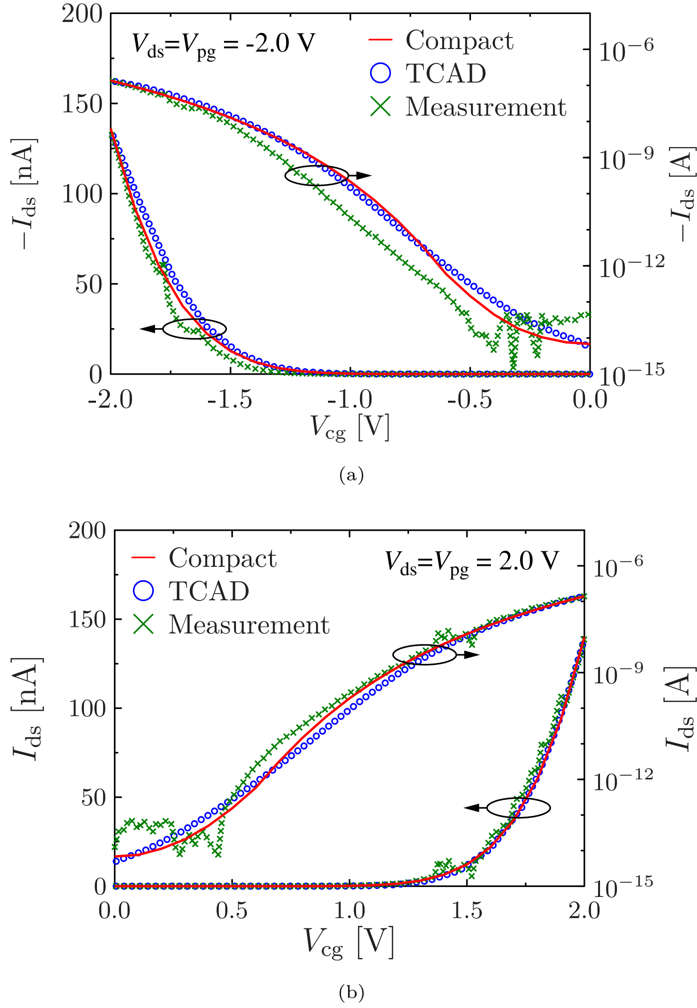
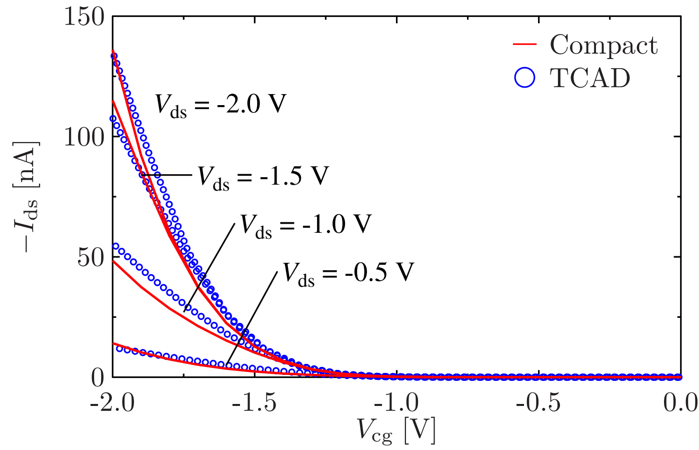
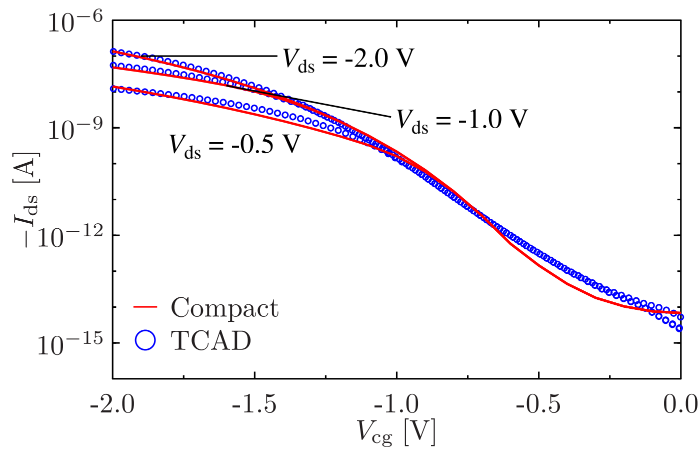


Figure 6.2: Transfer characteristics of a RFET device calculated from the compact model (solid red lines) compared to TCAD simulations (blue dots) and measurements (green crosses) from [66] in linear (left axis) and logarithmic (right axis) scale. (a) p-type operation mode ($V_{ds} = V_{pg} = -2\,V$). (b) n-type operation mode ($V_{ds} = V_{pg} = 2\,V$). The used model parameters can be found in Tab. 6.1.



(a)



(b)

Figure 6.3: Transfer characteristics calculated from the compact model (solid red lines) compared to TCAD simulations (blue dots). (a) p-type operation mode with $V_{pg} = -2\,V$ in linear and (b) logarithmic scale. The used model parameters can be found in Tab. 6.1.

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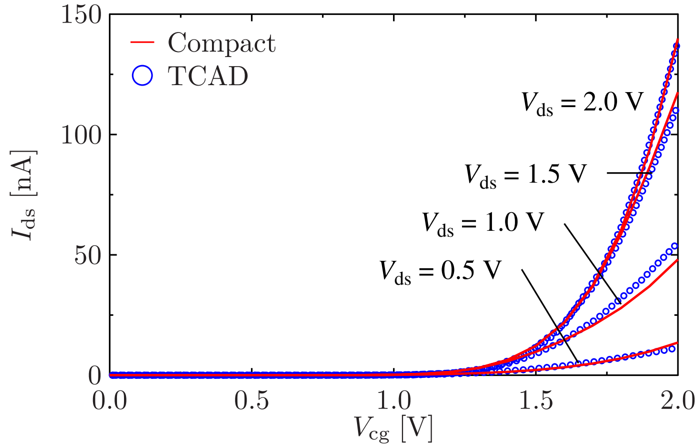
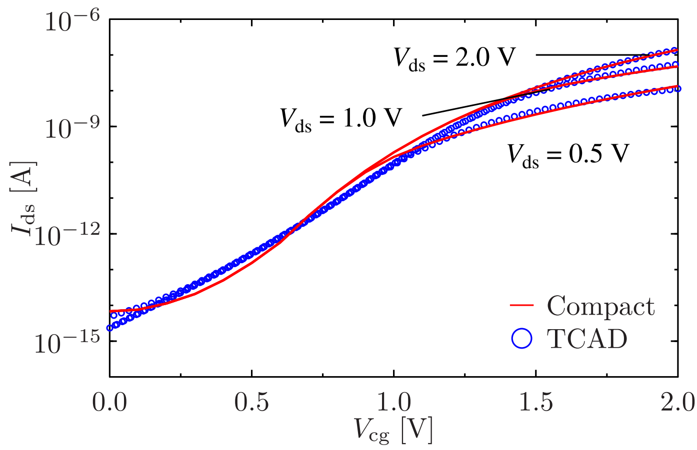
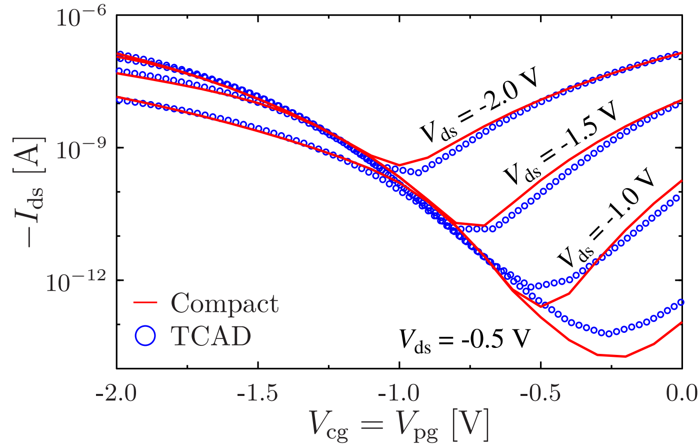


(a)

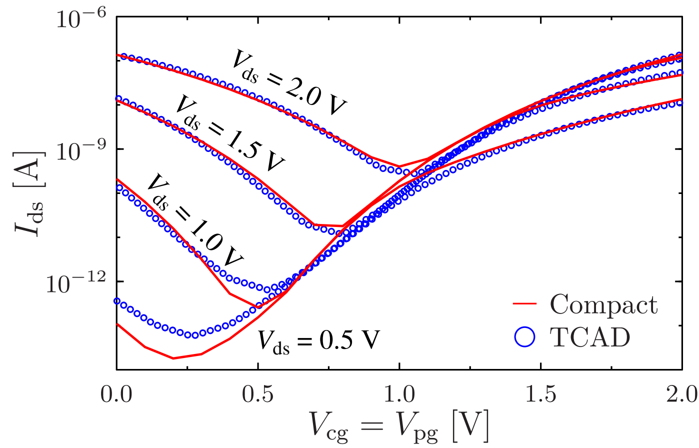


(b)

Figure 6.4: Transfer characteristics calculated from the compact model (solid red lines) compared to TCAD simulations (blue dots). (a) n-type operation mode with $V_{pg} = 2\,\text{V}$ in linear and (b) logarithmic scale. The used model parameters can be found in Tab. 6.1.

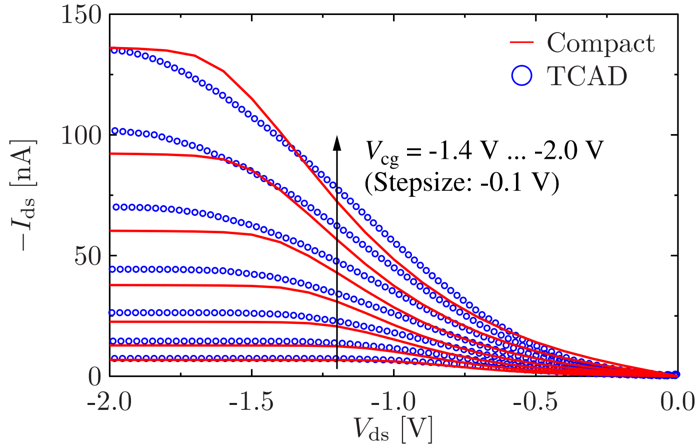


(a)

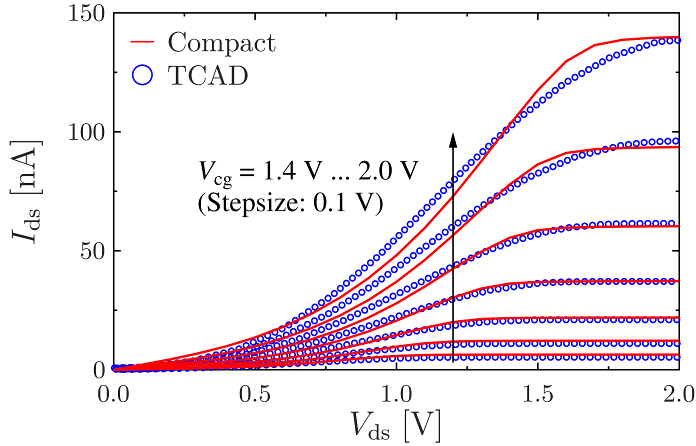


(b)

Figure 6.5: Transfer characteristics calculated from the compact model (solid red lines) compared to TCAD simulations (blue dots). (a) transfer characteristics for various negative drain voltages and (b) transfer characteristics for various positive drain voltages, while the device is used in SBFET mode ($V_{cg} = V_{pg}$), in logarithmic scale. The used model parameters can be found in Tab. 6.1.



(a)



(b)

Figure 6.6: Output characteristics calculated from the compact model (solid red lines) compared to TCAD simulations (blue dots). (a) p-type operation mode for various CG voltages with $V_{\mathrm{pg}} = -2\,\mathrm{V}$. (b) n-type operation mode for various CG voltages with $V_{\mathrm{pg}} = 2\,\mathrm{V}$. The used model parameters can be found in Tab. 6.1.

Table 6.1: Device parameters of the device under investigation in Fig. 6.2 to Fig. 6.6

Parameter	Value
L_{ch} [nm]	220
W_{ch} [nm]	12
t_{ch} [nm]	12
t_{ox} [nm]	8
$t_{\mathrm{eff,FE}}$ [-]	0.2
$t_{\mathrm{eff,TE}}$ [-]	0.8
$\varepsilon_{\mathrm{r,ox}}$ [-]	3.9
$\varepsilon_{\mathrm{r,sc}}$ [-]	11.7
E_{g} [eV]	1.1696
$\Phi_{\mathrm{B,n}}$ [V]	0.5800
$\Phi_{\mathrm{B,p}}$ [V]	0.5896
m_{n} [-]	0.10
m_{p} [-]	0.09
μ_{tn} [$\mathrm{cm^2\,V^{-1}\,s^{-1}}$]	59.78
μ_{tp} [$\mathrm{cm^2\,V^{-1}\,s^{-1}}$]	43.59
γ_{n} [-]	0.2
γ_{p} [-]	0.2
α [-]	0.5
V_{fb} [V]	0

The second model calculation (from [83]) is done on measurements of the RFET device from [93]. The used model parameters can be found in Tab. 6.2. The geometric parameters are selected to match the measured device as good as possible, so the values of W_{ch} and t_{ch} are chosen to approximately fit the nanowire's elliptical base area [93]. The length of the device's channel is estimated to be about $L_{\mathrm{ch,nw}} \approx 2.1\,\mathrm{\mu m}$, while the ungated channel of this device can be estimated to be about $L_{\mathrm{ung,nw}} \approx 0.7\,\mathrm{\mu m}$. For obtaining the model results, the channel resistance model from Sec. 6.1.2 is used, together with the effective gate-source voltage calculation according to Eq. (4.3). The results of this model comparison, shown in Fig. 6.7 and Fig. 6.8, contain calculated vs. measured transfer and output characteristics, while all of the presented cases show the device programmed in p-mode, using negative gate and drain voltages. In addition, Fig. 6.7(b) shows the compact model results obtained by just using the injection model (brown dotted lines), which shall demonstrate the necessity of the channel resistance model of Sec. 4.4 and Sec. 6.1.2. The results show a good agreement between measurements and the compact model. However, there are slight deviations in the subthreshold slope and the curve traces of the output characteristics. While observing the deviations in the output characteristics it is notable that the measurements have a stronger s-shape behavior, which could be attributed to non-idealities at the device's Schottky junctions and its simplification in the model. E.g. the Schottky barrier lowering is neglected.

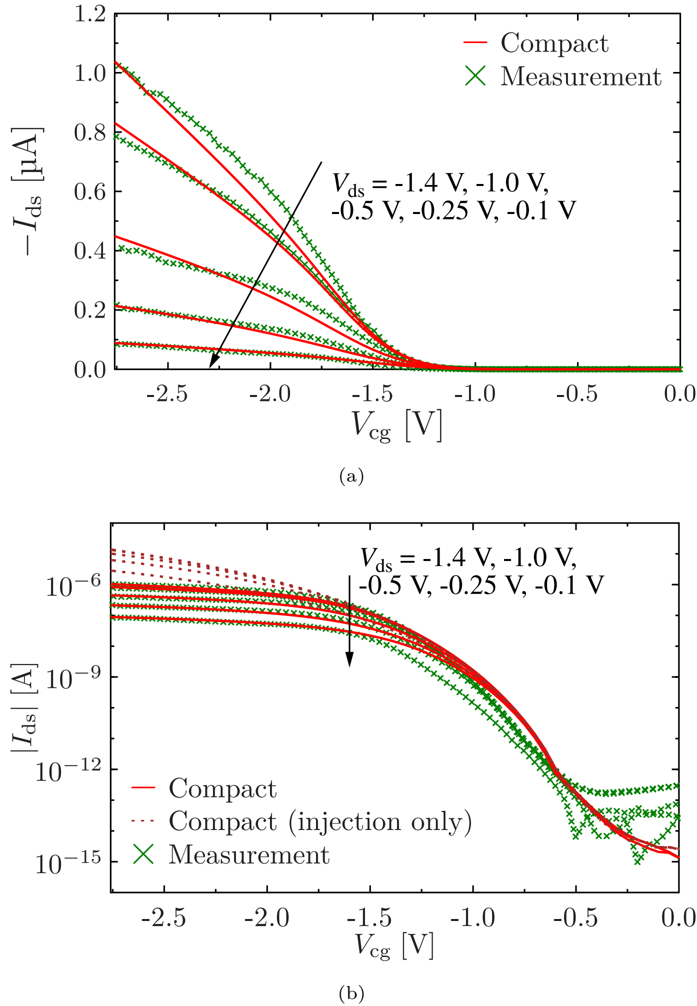


Figure 6.7: Device characteristics calculated from the compact model (solid red lines) and compared to measurements from [93] (green crosses). The geometries of the measured device are $L_{ch} \approx 2.1\,\mu m$, $L_{ung} \approx 0.7\,\mu m$, $R_{NW} = 3.5$ to $16\,nm$ (elliptical shape) and $t_{ox} \approx 6.5\,nm$. The compact model parameters can be found in Tab. 6.2. (a) shows the transfer characteristics for various negative drain voltages in linear scale and (b) shows the same results in logarithmic scale. Additionally, (b) shows the results from using the injection model only (brown dotted lines). During the transfer characteristics measurement, the PG was fixed to $V_{pg} = -2.8\,V$.

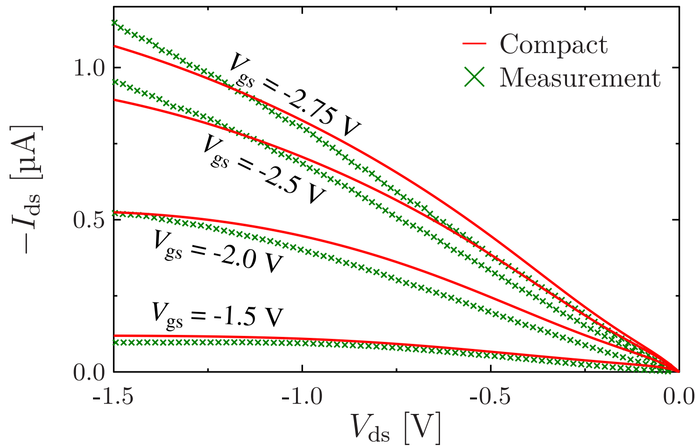


Figure 6.8: Output characteristics calculated from the compact model (solid red lines) and compared to measurements from [93] (green crosses) for various negative gate voltages. During these measurements the gate voltages are given as $V_{\mathrm{gs}} = V_{\mathrm{cg}} = V_{\mathrm{pg}}$. The geometries of the measured device are $L_{\mathrm{ch}} \approx 2.1\,\mu\mathrm{m}$, $L_{\mathrm{ung}} \approx 0.7\,\mu\mathrm{m}$, $R_{\mathrm{NW}} = 3.5$ to $16\,\mathrm{nm}$ (elliptical shape) and $t_{\mathrm{ox}} \approx 6.5\,\mathrm{nm}$. The compact model parameters can be found in Tab. 6.2.

Table 6.2: Device parameters of the device under investigation in Fig. 6.7 and Fig. 6.8

Parameter	RFET (Meas.)
L_{ch} [µm]	2.1
W_{ch} [nm]	16
t_{ch} [nm]	3.5
t_{ox} [nm]	6.5
$t_{\text{eff,FE}}$ [-]	0.2
$t_{\text{eff,TE}}$ [-]	0.8
$\varepsilon_{\text{r,ox}}$ [-]	3.9
$\varepsilon_{\text{r,sc}}$ [-]	11.7
E_{g} [eV]	1.1696
$\Phi_{\text{B,n}}$ [V]	0.5800
$\Phi_{\text{B,p}}$ [V]	0.5896
V_{limit} [V]	1.50
$\gamma_{\text{Vg,eff}}$ [-]	2.75
m_{n} [-]	0.26
m_{p} [-]	0.27
μ_{tn} [$\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$]	100.0
μ_{tp} [$\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$]	870.0
γ_{n} [-]	0.20
γ_{p} [-]	0.23
κ_{ung} [-]	0.13
V_{T0} [V]	0.38
S [mV/dec.]	60
γ_{MOS} [-]	2.0
μ_{n} [$\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$]	1440
μ_{p} [$\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$]	450
V_{fb} [V]	0

6.2 Approaches for Further Investigation

The RFET model which has been discussed in the previous sections is based on the SBFET injection model, while using a charge carrier suppression which depends on the PG voltage. In case of a transistor characterization with a fixed programming state and a main carrier injection over the source-side SB, the given compact model is sufficient. In case that a steady adjustment of the PG is needed for circuit simulation or the investigated device's CG has a different working principle (e.g. the TIG-RFET), further adjustments have to be done on the model.

In the following sections, some approaches are discussed for handling RFET structures which are not covered by the compact model, so far. The discussed methods have not been implemented or verified, yet.

6.2.1 Empirical Approach for two Steady Gates

The PG of the RFET is meant to be used for switching between the operation modes of the device and, in case the device is programmed, it is usually at $V_{\mathrm{pg}} \approx V_{\mathrm{ds}}$. Cases at which the PG voltage differs from this rule would be during switching processes.

In Eq. (6.6) it is shown how the RFET compact model suppresses charge carriers in a digital way, by setting the coefficients s_{n} or s_{p} to either 1 or 0. An empiric way of including a steady suppression dependent on the CG's and PG's bias voltages would be an expression inspired by the TE current (Eq. (4.40)), given as:

$$s_{\mathrm{n}} = \exp\left(-\frac{q \cdot (\Phi_{\mathrm{sur,L/2,s}} - \Phi_{\mathrm{sur,L/2,d}})}{k_{\mathrm{b}}\vartheta}\right), \tag{6.7}$$

with $\Phi_{\mathrm{sur,L/2,s}} \geq \Phi_{\mathrm{sur,L/2,d}}$, or with $s_{\mathrm{n}} = 1$ for $\Phi_{\mathrm{sur,L/2,s}} < \Phi_{\mathrm{sur,L/2,d}}$. This equation uses the potential barrier (in this case for electrons) between the two gates, to vary the factor s_{n} between 0 and 1. The two potentials $\Phi_{\mathrm{sur,L/2,s}}$ and $\Phi_{\mathrm{sur,L/2,d}}$ are the same potentials as Eq. (4.6), but calculated with the source- and drain-related potential model, as described in Sec. 6.1.1. A similar equation to Eq. (6.7), with reversed potentials, would be needed to calculate s_{p} for the hole suppression. The expression could be also extended with a fitting parameter in the exponent to adjust the rate of carrier suppression.

However, testing and fitting such an empirical approach would require several new simulation or measurement results, demonstrating the impact of a PG sweep, with various fixed drain and CG voltages, in order to have a proper verification. The approach from Eq. (6.7) would be only valid for the dually-gated RFET, since in other RFET structures the potential distribution is different.

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6.2.2 Macro Model Approach

Another approach for simulating RFETs, also covering more complex RFET structures, is by using a macro model. This could be done by combining the closed-form injection-based SBFET / RFET compact model of this work with other circuit elements that can mimic certain parts of the RFET (e.g. a second gate). Such a macro model could be used in a circuit simulator (e.g. SPICE) to be solved. However, the usage of a macro model comes with the disadvantage that it needs much more calculation effort, since it is solved numerically. In addition, it is likely harder to adjust the model's fitting parameters since each part of the model has its own parameters and needs separate adjustments.

Figure 6.9 shows some suggestions to construct a DC macro model for TIG-RFETs (see Fig. 3.19(b)) using the injection model. The first step (Fig. 6.9(a)) shows a simple version of a macro model, using the injection SBFET model for the source-side and drain-side gates. The MOSFET model which represents the CG in the middle of the channel must be a model which can be used for intrinsic semiconductors and uses accumulation of charge-carriers as conduction mechanism. This macro model would be able to calculate the RFET current through all three gates and, in case one gate is switched off, the corresponding part of the model would block the total current. However, this first suggestion has a design flaw since it does not distinguish the flowing charge-carrier type. If for example, the source-side injection model calculates an electron current and the CG transistor is negatively biased and calculated a hole current, the macro model will still conduct a total current, because after each model part the carrier type information is dropped, which is important for a real RFET. Therefore, the model of Fig. 6.9(a) can only be used for one carrier type (one operation mode).

An extension of the simple model is shown in Fig. 6.9(b). In this macro model the injection SBFET model parts have separate outputs for the electron and hole currents, which would require minor adjustments to the compact model. Additionally, the CG in the device's center is represented by two transistors, now. One transistor is p-type only and is located inside the hole injection connection and the other transistor is an n-type transistor in the n-type connection. With this macro model, there is a clear distinction between the carrier types inside the model and a total current can only flow in case that all model parts are conductive for the same type of charge carrier. The downside is, compared to the first suggestion, the complexity of the circuit and therefore the calculation effort has increased.

A further step of this model, which can be used to describe more complex RFET structures (for example the multi CG RFET, investigated in [71]), is shown in Fig. 6.9(c). This approach shall demonstrate that the macro model could also be used to model more than just one central gate, by adding one p- and n-type transistor combination per additional gate, for the cost of an increased circuit complexity.

It shall be mentioned that this macro modeling approach is not only a way of just being

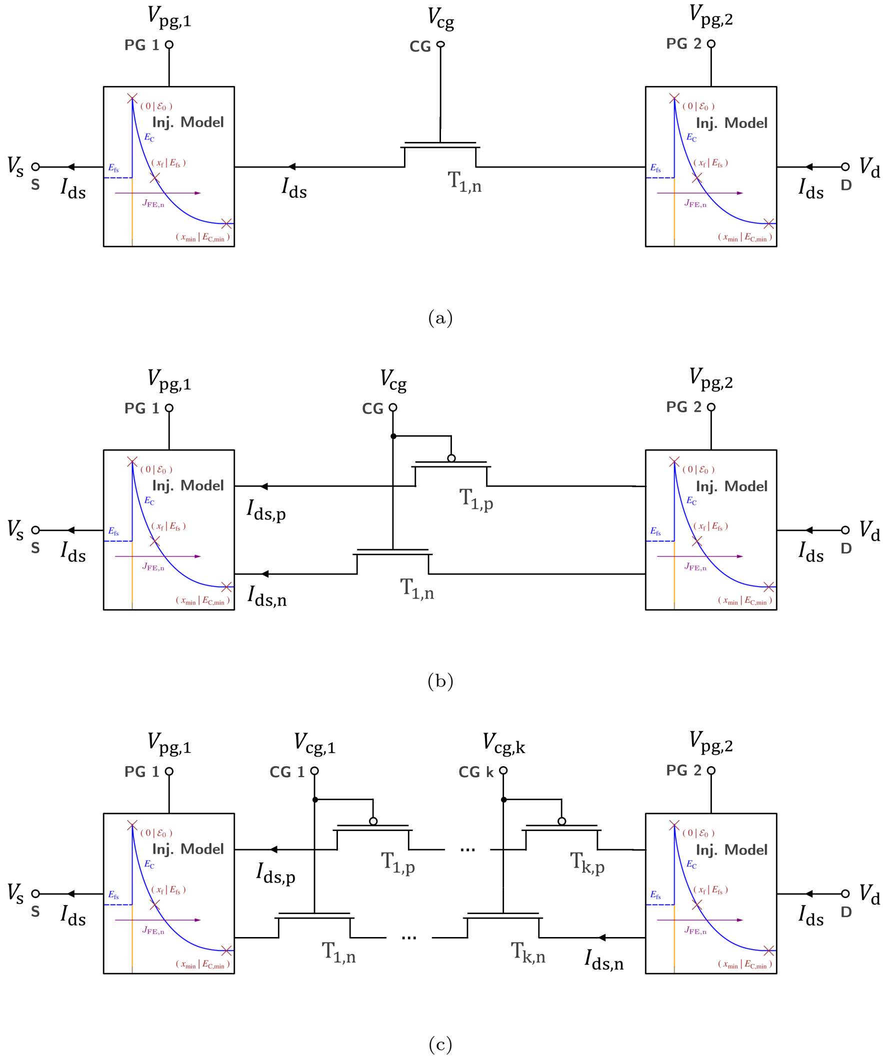

Figure 6.9: Macro model circuits for modeling TIG-RFETs by using a combination of the SBFET injection model and one or more FETs (T) as components. (a) shows a simplified approach with one channel FET. (b) uses two FETs (one p-type and one n-type) for the CG, with one FET for each carrier type. (c) is the extension of (b) for multiple CGs, using two FETs (one p-type and one n-type) per CG.

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able to simulate the given RFET structures. It could also help improving the understanding of the different device operation modes and also lead to some simplifications of the model. For example, it could be possible, by some adjustments of the CG voltages and device parameters to translate the structure from Fig. 6.9(c) to Fig. 6.9(b). Additionally, by characterizing the central gates, it could also be possible to find a way of extracting a compact expression for certain device structures, which could be finally included into the channel MOSFET addition of the compact model, in order to translate the macro model back into a compact model.

CHAPTER 7

Conclusion

In this work the derivation of a physics-based and closed-form DC compact model is presented which is applicable on several transistor types working on the principle of SB injection. More detailed, the model has been derived for SBFETs at room temperature and extended for SBFETs at deep cryogenic temperatures ($\vartheta \approx 0\,\mathrm{K}$), as well as for fix-programmed RFETs at room temperature. All three model parts are supplemented by the inclusion of second order effects coming to the fore in their operation environment. The verification of the compact model has been done on TCAD simulations and measurements, and all of the discussed model parts generally show a good agreement to the simulated and measured data, while only using a small number of fitting parameters.

The room temperature SBFET calculates the DC drain current of a SBFET by using expressions for the TE and FE current contribution. While the TE current, which acts as off-state or leakage current, already has some closed-form expressions from literature, the FE current expression is approximated in order to obtain a closed-form current equation. This approximation of the on-state FE current is done by a simplified tunneling equation using the WKB approach in order to calculate tunneling charge carriers through the transistor's SBs. This model is also extended by including channel resistance effects for long-channel devices, by using a charge-based MOSFET model for limiting the SBFET's total drain current.

The room temperature SBFET model is modified in a second step for the usage at deep cryogenic temperatures, and thereto the compact model is derived estimating a temperature of about $\vartheta \approx 0\,\mathrm{K}$. In this state the TE current is supposed to be non-existent. The FE current contribution, which is supposed to be the only injection current in this operation environment, is re-calculated using a simplified expression for the Fermi distribution function. This model variation also empirically includes second order effects that have been experimentally observed at these temperatures. The included effects are quantum oscillations which are oscillations of the drain current in the device characteristics, the band tail effect that flattens the SBFET's subthreshold swing, and the channel resistance model similar to the one from the room

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temperature approach.

The model variant for RFETs is also an extension of the SBFET room temperature model. In this part, the additional PG of the RFET is considered by suppressing one type of charge carrier, which negates the ambipolar device behavior. This part of the model is also extended by the channel resistance model as second order effect with the additional impact of the ungated transistor part. Although, the RFET model is specifically derived for fix-programmed dually-gated RFETs, there are suggestions made in this work how a steady PG and other RFET structures can be supported.

In this work, the functionality of the compact model and all of its extensions has been demonstrated. The model in its current state is implemented in MATLAB (MathWorks, Inc.) for programming and testing at a single device level. For a proper usage of the model in a circuit simulator, as a last step it needs to be translated to Verilog-A and tested in this environment, which has yet to be done. In addition to the transition into a SPICE environment, a studies and guidance for the model's fitting parameters has to be done. The fitting process in this work is performed by a manual variation of the parameters. Some of the model's fitting parameters are more dominant in certain voltage regions of the characteristics, and some parameters have overlapping effects on the model outputs. The different parameters need to be documented with their impact on the characteristics and reasonable limitations, in order to provide a functional compact model operation state and a good starting point for model fits.

Moreover, for the compact model there are additional effects that may be considered as future investigations. Although, there are several cases mentioned throughout the document which have been neglected in the model derivation, because they have not been relevant in the specific cases. Some other effects are included empirically. A few points shall be mentioned at this point which could be interesting to further investigate in the future, depending on the model's use case:

- The compact model in all of its extends has been derived and tested for nickel silicide to (almost intrinsic) silicon SBs, specifically. This junction leads to the symmetric device characteristics for electron and hole currents. However, the model has not been tested and verified on SBFETs with unsymmetrical characteristics (see Sec. 3.2.2.1) or other semiconductor materials like germanium, yet. The model supports several material parameter adjustments, like changing the semiconductors bandgap E_g, the source / drain metal work function by adjusting the SB heights $\Phi_\mathrm{B,n}$ and $\Phi_\mathrm{B,p}$, or the gate's work function by adjusting the flatband voltage V_fb. In the current implementation state, only semiconductor materials with the Fermi energy in the middle of the bandgap are supported, because some equations like the built-in potential are calculated by estimating that $E_\mathrm{C} - E_\mathrm{f} \approx E_\mathrm{f} - E_\mathrm{V} \approx E_\mathrm{g}/2$. This means that doped silicon cannot be used as channel material at the moment. In order to add the support for other (doped) semiconductor materials into the model, some of the equations need to replace the $E_\mathrm{g}/2$-expression by

accurate values for $E_\mathrm{C} - E_\mathrm{f}$ and $E_\mathrm{f} - E_\mathrm{V}$, respectively.

- The SBL effect, introduced in Sec. 2.4.3, has been neglected in this work. Although, this effect is supposed to impact the FE current, its impact on the TE current is higher, since the TE current is directly exponentially affected by the SB height, while the FE current has a stronger dependency on the SB thickness. In the model and simulation results, it can be observed that the TE current contribution can mostly be neglected (in case of SBFETs) or only describe the off-current (in case of programmed RFETs). By extending the model towards material combination with lower SB heights, the TE current might be more impactful again. In this case, adding the SBL effect at least in the TE equations might lead to improved results.
- The quantum confinement effects have been neglected so far, which is also debatable in the results of Sec. 5.5.2, since the nanowire diameters are smaller than 10 nm. Even though the model results show a good agreement to the measurements, the quantum confinement effects in this case might be just covered by other fitting parameters.
- Especially, in case of the deep cryogenic SBFET modeling, there is the need of additional studies and model fits. This would be useful for a better characterization of the included second order effects, as the quantum oscillation and the channel MOSFET addition at $\vartheta \to 0\,\mathrm{K}$. The model for quantum oscillations is inspired by the local density of states calculated with the compact NEGF approach, although the measured characteristics seems to include more oscillation effects. Those might be also caused by resonant tunneling effects inside the device or through the SB, which has not been clarified, yet, and also needs some additional experimental studies.

There are also possibilities for longer term investigations of using this work's compact model for other device's or extend the model for other use cases. Some possibilities shall be briefly discussed:

- The currently implemented compact model is for the DC current calculation only. For a fully operational compact model that can be used to simulate the switching behavior of circuits comprising SBFETs or RFETs, it is mandatory to also have a valid AC model describing the device behavior. For this case, modeling approaches like shown in [94, 95] could be used.
- The temperature dependency of the model is restricted to room temperature and deep cryogenic temperatures. Although, the room temperature SBFET model uses the temperature in its equations, due to the approximations done for the derivation, the temperature dependency is not supposed to be varied steadily and work for all temperatures. It might be helpful to have a single compact model that is able to describe the transistors' behavior for all temperatures, by just varying that single parameter. This, however, would need a more extensive temperature studies of the devices (with TCAD simulations and measurements) and the derivation of the equations including temperature dependencies,

which also means a unification of the used potential model and the injection equations.

- In terms of the model adaption towards different types of RFETs, in Sec. 6.2 there are already some suggestions on how to include a steady PG or a central gate into the model. Modeling specific types of RFETs close to the device's physics comes with the disadvantage that the resulting compact model would be more specialized towards that certain technology, and less open or flexible towards other type of RFETs. The currently implemented version of the RFET model, using the carrier type suppression, is applicable to all SB injection based RFETs. More specific modeling approaches might be just valid for a certain type of technology, so a further specialization of the model should be done on demand for it.
- Similarly, the model for SBFETs could be potentially adapted to other SB-based technologies. As example, the ferroelectric SBFET could be modeled by replacing the constant oxide permittivity $\varepsilon_{\mathrm{r,ox}}$ by a voltage and time-dependent expression, or it might be used for source-gated transistors by replacing the potential model.

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