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# *Novel nanoelectronic circuits and systems*

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# Novel Nanoelectronic Circuits and Systems

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# *Abstract*

Lately, in the rise of the era of 2D materials, Graphene is one of the materials that has been extensively investigated for its possible integration in computing devices and thus computing circuits. This is mainly attributed to its very wide set of appealing properties. The combination of its electronic properties with others, such as mechanical, optical or chemical properties, can extend the range of use of computing devices and lead to groundbreaking interdisciplinary applications. However, this integration of Graphene in switching and computing elements is not easy.

In this dissertation, the Non-Equilibrium Green's Function method (NEGF), along with the Tight Binding Hamiltonians, are fitted on experimental data from fabricated Graphene devices. Although as a computational method, NEGF is appropriate for the simulation of small-scale devices in the regime of nanometers, its ability to be efficiently expanded for the description of larger devices is presented.

The aforementioned electronic properties of the material are highly related to its shape and structure. Consequently, it requires a very precise fabrication method that can guarantee the minimum presence of defects on the Graphene grid. For that reason, the effect of defects is deeply investigated. The NEGF method is further enhanced in order to be able to incorporate lattice defects. The most common lattice defects are included, meaning the single and double vacancy. A framework has thus been created, so that for the first time the user can select areas of interest on the grid, in which the defects will be concentrated. Those concentrations can also be variable. Moreover, an extensive study is conducted on defective grids with different concentrations of single and double vacancies. The investigated grids are non-rectangular and have regions with different widths. The effect of those vacancies on the electronic properties of Graphene is investigated, and more specifically their effect on the conductance and the energy gap of the device, as well as the effect on circuit-centered characteristics such as the leakage current and ON/OFF current ratio. Having a functional, robust, versatile, and accurate model, the focus of this thesis is extended to the level of circuits. The model is imported into SPICE through Verilog-A. In this part, the thesis emphasizes on the investigation of the switching capabilities of L-shaped Graphene Nanoribbons (GNRs). These structures have been proven to be able to operate as switches, without the use of a back gate, and here, the properties that are dependent on their

dimensions are explored and optimized for the first time. The optimized structures are then used for the realization of a set of computing topologies. Initially, a novel area-optimized 2-branch comb-shaped topology is introduced for the realization of a universal computing set that consists of an `AND`, `OR`, `NOT` gate, and a `Buffer`. All these logic operations can be mapped on the same topology through appropriate biasing. Then, an extension of this, the 3-branch comb-shaped topology is proposed, which is able to operate as a `2-XOR`, `3-XOR` and `3-MAJ` gate. The circuit of a 1-bit full adder, is also presented. For the evaluation of the performance of the topologies, several related metrics are employed such as the area, delay, power dissipation and the power-delay product. The operation of these topologies relies of the principles of Pass Transistor Logic (PTL) and reconfigurable computing. Finally, in an attempt to go beyond the conventional Boolean logic, the compliance of Graphene with Multi-Valued Logic (MVL) circuits and applications is investigated. The ability of a Graphene Quantum Point Contact (G-QPC) device to encode the digits of the radix-4 numeral system is presented and as a proof of concept, the operation of an arbitrary radix-4 adder is explained.

# Περίληψη

Τελευταία, με την διάδοση των 2Δ υλικών, το Γραφένιο εμφανίζεται ώς ένα από τα υλικά που έχουν μελετηθεί εκτενώς για την πιθανή ενσωμάτωσή του σε υπολογιστικές διατάξεις και κατ΄ επέκταση σε υπολογιστικά κυκλώματα. Αυτό οφείλεται κυρίως στο πολύ ευρύ σύνολο ελκυστικών ιδιοτήτων που διαθέτει. Ο συνδυασμός των ηλεκτρονικών του ιδιοτήτων με άλλες, όπως μηχανικές, οπτικές ή χημικές, μπορεί να επεκτείνει το φάσμα χρήσης των υπολογιστικών συσκευών και να οδηγήσει σε πρωτοποριακές διεπιστημονικές εφαρμογές. Ωστόσο, η ενσωμάτωση του Γραφενίου σε διακοπτικές και υπολογιστικές διατάξεις είναι εύκολη. Στην παρούσα διατριβή, η μεθόδος Non Equilibrium Green's Function (NEGF) σε συνδυασμό με τις Χαμιλτονιανές Ισχυρού Δεσμού βαθμονομείται σε πειραματικά δεδομένα από κατασκευασμένες διατάξεις Γραφενίου. Αν και ως υπολογιστική μέθοδος, η NEGF είναι κατάλληλη για την προσομοίωση συσκευών μικρής κλίμακας τις τάξης των νανομέτρων, η ικανότητά της να επεκταθεί αποτελεσματικά για την περιγραφή μεγαλύτερων συσκευών επεκτείνεται. Οι προαναφερθείσες ηλεκτρονικές ιδιότητες του υλικού συνδέονται άμεσα με το σχήμα και τη δομή του. Συνεπώς, η μέθοδος κατασκευής του πρέπει να είναι τόσο ακριβής ώστε να μπορεί να εγγυηθεί την ελάχιστη δυνατή συγκέντρωση ατελειών στο πλέγμα. Για αυτό το λόγο, η επίδραση των πλεγματικών σφαλμάτων ερευνάται σε βάθος. Η μέθοδος NEGF ενισχύεται περαιτέρω ώστε να μπορεί να ενσωματώσει στις προσομοιώσεις πλεγματικά σφάλματα. Τα πιο κοινά πλεγματικά σφάλματα συμπεριλαμβάνονται, δηλαδή το σφάλμα μονής κενής θέσης και το σφάλμα διπλής κενής θέσης. Έχει επομένως δημιουργηθεί ένα υπολογιστικό πλαίσιο, ώστε για πρώτη φορά ο χρήστης να μπορεί να επιλέξει περιοχές ενδιαφέροντος στο πλέγμα, στις οποίες θα εμφανίζονται οι επιλεγμένες συγκεντρώσεις και οι επιλεγμένοι τύποι σφαλμάτων. πραγματοποιείται μια αναλυτική μελέτη σε πλέγματα που περιέχουν σφάλματα μονής και διπλής θέσης σε διάφορες συγκεντρώσεις. Για πρώτη φορά, τα εξεταζόμενα πλέγματα δεν έχουν απλό πραλληλόγραμο σχήμα, αλλά περιέχουν περιοχές διαφορετικού πλάτους. Επομένως, μελετάται η επίδραση της ύπαρξης αυτών των κενών θέσεων στις ηλεκτρικές ιδιότητες του γραφενίου και πιο συγκεκριμένα στην αγωγιμότητα του και στο ενεργειακό του χάσμα. Γίνεται επίσης μελέτη ώς προς την επίδραση των σφαμλμάτων αυτών σε κάποιες άλλες ποσότητες, πιο σχετικές με την κατασκευή κυκλωμάτων, όπως ειναι το ρεύμα διαρροής και ο λόγος των ρευμάτων αγωγής και διαρροής, $I_{ON}/I_{OFF}$. Διαθέτοντας λοιπόν πλέον ένα πλήρες, στιβαρό και ακριβές μοντέλο, η έμφαση αυτής της διατριβής επεκτείνεται στο επίπεδο των κυκλωμάτων. Το μοντέλο

εισάγεται στο SPICE μέσω Verilog-A. Στο κομμάτι αυτό, η διατριβή επικεντρώνεται κυρίως στην μελέτη των διακοπτικών ικανοτήτων των Νανοταινιών Γραφενίου (GNRs) σχήματος $L$. Αυτές οι δομές έχουν αποδειχθεί ότι είναι ικανές να λειτουργούν ως διακόπτες, χωρίς τη χρήση πίσω πύλης, και εδώ, οι ιδιότητες που εξαρτώνται από τις διαστάσεις τους εξερευνώνται και βελτιστοποιούνται για πρώτη φορά. Οι βελτιστοποιημένες δομές χρησιμοποιούνται στη συνέχεια για την υλοποίηση ενός συνόλου υπολογιστικών τοπολογιών. Αρχικά, παρουσιάζεται μια νέα βελτιστοποιημένη ως προς το μέγεθος τοπολογία κομβικού 2-κλάδων για την υλοποίηση ενός συνόλου καθολογικού υπολογισμού που αποτελείται από τις πύλες `AND, OR, NOT` και έναν `Buffer`. Όλες αυτές οι λογικές λειτουργίες μπορούν να αντιστοιχιστούν στην ίδια τοπολογία μέσω κατάλληλης πόλωσης. Στη συνέχεια, προτείνεται μια επέκταση αυτού, η τοπολογία 3-κλάδων, η οποία είναι ικανή να λειτουργήσει ως πύλη `2-XOR, 3-XOR` και 3-MAJ. Παρουσιάζεται επίσης το κύκλωμα ενός πλήρους αθροιστή 1-bit. Για την αξιολόγηση της απόδοσης των τοπολογιών, χρησιμοποιούνται διάφορες σχετικές μετρικές όπως το μέγεθος, η καθυστέρηση, η κατανάλωση ισχύος και το γινόμενο ισχύος-καθυστέρησης. Η λειτουργία αυτών των τοπολογιών βασίζεται στις αρχές της κλασσικής μεθοδολογίας Pass Transistor Logic (PTL) ενώ παράλληλα ανοίγει τον δρόμο για νέες υλοποιήσεις στο πεδίο της επαναπρογραμματιζόμενης λογικής. Τέλος, σε μια προσπάθεια να ξεπεραστεί η συμβατική λογική Bool, ερευνάται η συμβατότητα του Γραφενίου με τα κυκλώματα και τις εφαρμογές της Multi-Valued Logic (MVL). Η ικανότητα συκεκριμένων διατάξεων γραφενίου να κωδικοποιήσουν τα ψηφία ενός αριθμητικού συστήματος με βάση το 4 παρουσιάζεται και αναλύεται η λειτουργία ενός πρωτόλυου αθροιστή του τετραδικού συστήματος.

# *Resumen*

Últimamente, en el auge de la era de los materiales bidimensionales, el grafeno es uno de los materiales que ha sido ampliamente investigado por su posible integración en dispositivos de cómputo y en circuitos informáticos. Esto se debe principalmente a su muy amplio conjunto de propiedades atractivas. La combinación de sus propiedades electrónicas con otras, como las mecánicas, ópticas o químicas, puede extender el rango de uso de los dispositivos de cómputo y llevar a aplicaciones interdisciplinarias revolucionarias. Sin embargo, esta integración del grafeno en elementos de conmutación y cómputo no es fácil. En esta disertación, el método de la Función de Green Fuera del Equilibrio (NEGF), junto con los Hamiltonianos de Unión Apretada, se ajustan a datos experimentales de dispositivos de grafeno fabricados. Aunque NEGF es apropiado para la simulación de dispositivos a pequeña escala en el régimen de nanómetros, su capacidad para ser expandido eficientemente para la descripción de dispositivos más grandes se presenta. Las propiedades electrónicas mencionadas del material están altamente relacionadas con su forma y estructura. Por consiguiente, requiere un método de fabricación muy preciso que pueda garantizar la mínima presencia de defectos en la rejilla de grafeno. Por esa razón, el efecto de los defectos se investiga profundamente. El método NEGF se mejora aún más para poder incorporar defectos en la red. Se incluyen la vacante simple y doble. De esta manera, se ha creado un marco, para que el usuario pueda seleccionar áreas de interés en la rejilla, en las cuales se concentrarán los defectos. Esas concentraciones pueden ser variables. Además, se lleva a cabo un estudio extenso en rejillas defectuosas con diferentes concentraciones de vacantes simples y dobles. Las rejillas investigadas son no rectangulares y tienen regiones con diferentes anchuras. Se investiga el efecto de esas vacantes en las propiedades electrónicas del grafeno, y más específicamente su efecto en la conductancia y la brecha de energía del dispositivo, así como el efecto en características centradas en el circuito como la corriente de fuga y la relación de corriente ON/OFF. Teniendo un modelo robusto y versátil, el enfoque de esta tesis se extiende al nivel de circuitos. El modelo se importa a SPICE a través de Verilog-A. En esta parte, la tesis enfatiza en la investigación de las capacidades de conmutación de las Nanocintas de Grafeno (GNRs) en forma de L. Estas estructuras han demostrado ser capaces de operar como interruptores, sin el uso de una puerta trasera, y aquí, las propiedades que dependen de sus dimensiones

se exploran y optimizan. Las estructuras optimizadas se utilizan entonces para la realización de un conjunto de topologías de cómputo. Inicialmente, se introduce una topología en forma de peine de 2-ramas optimizada en área para la realización de un conjunto de cómputo universal que consiste en una puerta AND, OR, NOT y un Buffer. Todas estas operaciones lógicas se pueden mapear en la misma topología a través de un sesgo apropiado. Luego, se propone una extensión de esta, la topología en forma de peine de 3-ramas, que es capaz de operar como una puerta 2-XOR, 3-XOR y 3-MAJ. También se presenta el circuito de un sumador completo de 1-bit. Para la evaluación del rendimiento de las topologías, se emplean varias métricas como el área, el retraso, la disipación de potencia y el producto potencia-retraso. El funcionamiento de estas topologías se basa en los principios de la Lógica de Transistor de Paso (PTL) y la computación reconfigurable. Finalmente, en un intento de ir más allá de la lógica Booleana convencional, se investiga la conformidad del grafeno con circuitos y aplicaciones de Lógica de Múltiples Valores (MVL). Se presenta la capacidad de un dispositivo de Contacto Cuántico Puntual de Grafeno para codificar los dígitos del sistema numérico de base-4 y como prueba de concepto, se explica el funcionamiento de un sumador de base-4 arbitrario.

# *Resum*

En definitiva, a l'altura de l'era dels materials bidimensionals, el grafè és un dels materials que s'ha investigat àmpliament per la seva possible integració en dispositius informàtics i circuits informàtics. Això es deu principalment al seu conjunt molt gran de propietats atractives. La combinació de les seves propietats electròniques amb altres, com ara mecàniques, òptiques o químiques, pot ampliar el ventall d'ús dels dispositius informàtics i aportar aplicacions interdisciplinàries revolucionàries. Sense embargo, aquesta integració del grapheno en elements de commutació i còmput no és fàcil. En aquesta tesi, el mètode Non-Equilibrium Green's Function (NEGF), juntament amb els Tight Binding Hamiltonians, s'ajusten a les dades experimentals dels dispositius de grafè fabricats. Tot i que NEGF és adequat per a la simulació de dispositius a petita escala en règim de nanòmetres, es presenta la seva capacitat d'ampliar-se de manera eficient per a la descripció de dispositius més grans. Les propietats electròniques esmentades en el material estan molt relacionades amb la seva forma i estructura. Per tant, requereix un mètode de fabricació molt precís que pugui garantir la mínima presència de defectes a la graella de grafè. Per aquesta raó, l'efecte dels errors s'investiga profundament. El mètode NEGF es millora encara més per poder incorporar defectes a la xarxa. Inclouen vacants individuals i dobles. D'aquesta manera, s'ha creat un marc perquè l'usuari pugui seleccionar zones d'interès de la quadrícula, en les quals es concentraran els defectes. Aquestes concentracions poden ser variables. A més, es porta a la tesi es realitza un extens estudio en reixes defectes amb diferents concentracions de singles i dobles vacancies. Les quadrícules investigades no són rectangulars i tenen regions amb diferents amplades. S'investiga l'efecte d'aquestes vacants sobre les propietats electròniques del grafè i, més concretament, el seu efecte sobre la conductància i el gap of energy del dispositiu, així com l'efecte sobre característiques centrades en el circuit com ara el corrent de fuga i la relació de corrent ON/OFF. Tenint un model robust i versàtil, el focus d'aquesta tesi s'estén al nivell de circuits. El model s'importa a SPICE mitjançant Verilog-A. En aquesta part, la tesi posa èmfasi en la investigació de les capacitats de commutació dels nanoribbons de grafè (GNR) en forma de L. S'ha demostrat que aquestes estructures poden funcionar com a interruptors, sense l'ús de porta posterior, i aquí, las propietats que depenen de les seves dimensions es explorar i optimitzar. Les estructures optimitzades s'utilitzen llavors per a la realització d'un conjunt

de topologies d'ordinador. Inicialment, s'introdueix una topologia en forma de quadrícula de 2 branques optimitzada en àrea per a la realització d'un conjunt de computació universal que consta d'una porta AND, OR, NOT i un buffer. Totes aquestes operacions lògiques es poden mapejar a la mateixa topologia mitjançant un biaix adequat. Aleshores, es proposa una extensió d'aquesta, la topologia en forma d'arbre de 3 branques, que és capaç d'operar com a porta 2-XOR, 3-XOR i 3-MAJ. També es presenta el circuit d'un sumador complet d'1 bit. Per a l'avaluació del rendiment de les topologies s'utilitzen diverses mètriques com ara l'àrea, el retard, la dissipació de potència i el producte de retard de potència. El funcionament d'aquestes topologies es basa en els principis de Pass Transistor Logic (PTL) i informàtica reconfigurable. Finalment, en un intent d'anar més enllà de la lògica booleana convencional, s'investiga la conformitat del grafè amb els circuits i aplicacions de la lògica de valors múltiples (MVL). Es presenta la capacitat d'un dispositiu de contacte quàntic puntual de grafè per codificar els dígits del sistema numèric de base-4 i com a prova de concepte, s'explica el funcionament d'un sumador arbitrari de base-4.

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# Chapter 1

# Introduction

Since its inception and successful production in 1947, the Transistor, particularly the Field Effect Transistor (FET), has been at the forefront of the electronics industry, propelling its remarkable and rapid advancement throughout the subsequent years. This device quickly displaced the previously prevailing switching device, the vacuum tube, and resulted in significant miniaturization of electronic devices. The very first functional transistor device, designed as a point contact transistor, was manufactured utilizing Germanium as the semiconductor material (Bardeen & Brattain, 1948). This breakthrough prompted an increased scientific interest in the field of semiconductors. In the early 1950s, Germanium utilization was quickly restricted and replaced by Silicon due to its superior thermal stability, improved electronic properties, and abundant availability in nature. These characteristics made Silicon a suitable material for the mass fabrication of transistors. Several alternative materials, including Silicon-Germanium Alloys (SiGe), Gallium Arsenide (GaAs), Indium-Phospide (InP), and Gallium-Nitride (GaN), have been extensively studied and successfully employed in the development of Transistors. Several of these components have been utilized over time for specific purposes such as Radio Frequency (RF) systems requiring high-speed capabilities, Power systems necessitating more power handling capacity, or Optical systems aiming to exploit various optical features.

Nevertheless, Silicon quickly became the prevailing material for manufacturing transistors specifically designed for use in computing circuits. The first Integrated Circuit (IC), which incorporated many silicon transistors on a single chip, had already been developed in the early 1960s. This marked the initial phase of the following microprocessor revolution. Subsequently, there has been a continuous rise in the quantity of transistors incorporated within integrated circuits (ICs), resulting in a significant growth

in microelectronics and serving as a catalyst for the computer manufacturing sector. Those advancements of IC technology, combined with the successful development of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) in the early 1960s (Kahng, 1960), played a crucial role in the development of the Microprocessors we use today.

MOSFETs provide a bunch of intriguing characteristics. These devices are energy efficient due to their low static power consumption resulting from their operational principle. Additionally, they offer high input impedance and can be fabricated at a relatively low cost. They also provide design flexibility, as they can be utilized in various digital and analog applications. Most importantly, they are highly scalable and robust, which is crucial for the ongoing miniaturization of integrated circuits.

The continual reduction in size of the MOSFET has resulted in integrated circuits (ICs) with higher density, increased speed, and lower power consumption which can be directly translated to overall better performance in every factor. The correlation between the physical dimensions of a transistor and the performance of a microprocessor led to the formulation of two empirical laws that have been essential in driving the continuous improvement of computing chips over the years. First, there is Moore's Law, a well-known principle that asserts the number of transistors on a chip will double every 2 years (Moore, 1965), Additionally, there is Dennard's Scaling Law, an extension of Moore's Law, which states that the chip's performance per unit of power will double every 18 months (Dennard et al., 1974).

Those laws governed the evolution of CPU technology and performance and were followed by the industry up until recently, as the shrinking of transistor provided chips with higher density while simultaneously reducing their power consumption, which contributed to the maintenance of their heating dissipation at manageable levels. This reduction in size also resulted in a substantial increase in memory density, so increasing the capacity of available memories while simultaneously reducing the cost per megabyte (MB).

Unfortunately, this convenient trend recently ceased. In the mid-2000s, Dennard's law, which mostly focused on the energy aspect of chips, was violated as a result of the higher leakage currents of transistors at decreasing dimensions (Bohr, 2007). After some time, in 2010, the Moore's Law was also violated, as the costs of doubling the number of transistors per chip by shrinking started to increase exponentially (Eeckhout, 2017; Theis & Wong, 2017; Williams, 2017).

In general, this ongoing minimization trend has also given rise to some significant issues. Transistors reached their physical scaling limits. In the nanometer regime, quantum effects begin to govern their operation, affecting their performance. Furthermore, it should be noted that the fabrication techniques of silicon transistors become extremely challenging and the fabrication equipment costs increase exponentially, while also variability issues emerge and significantly diminish the fabrications yields. The high density of the chips poses a substantial challenge in dissipating heat, which can ultimately impact the speed performance of the chips, raise failure rates, and lower their lifespan (Hamdioui et al., 2017; Ratnesh et al., 2021).

To address the challenges arising from ongoing miniaturization, researchers are pursuing two distinct approaches. The first involves tackling these issues at the architectural level. This research path not only aims to enhance the efficiency of traditional computing architectures but also places a strong emphasis on exploring "Beyond von Neumann" architectures. This strategy signifies an active effort to develop and adjust computing systems in response to emerging technological constraints.

There are two main conventional architectures for computing systems, the von Neumann architecture (Von Neumann, 1993) and the Harvard architecture (Pawson, 2022). The first one, describes a system with a processing unit and a shared memory both for instructions and data, while the second one describes a system with a processing unit and two separate memory units, one dedicated to instructions and the other to data. In both of those architectures, the processing units are separated from the memory. Although those ideas are fundamental to contemporary computers, they have notable constraints. One of the most significant is the von Neumann bottleneck. This separation of the central processing unit (CPU) from the memory, which is responsible for data and instruction storage, serves as a barrier in data flow as data needs to be sent back and forth between these components. As CPUs become faster, the relatively slow movement of data from and to the memory has emerged as a more prominent constraint (Backus, 1978). The continuous transfer of data between memory and CPUs also results in increased power consumption, which is in conflict with the prevailing trends of low-power systems and portability.

Therefore, numerous computing architectures are being continuously studied to address the aforementioned issues, some designed for general-purpose computing while others dedicated to specific applications. A representative example is in-memory computing, which offers the potential to

combine processing and memory capacities, enabling operations to be performed within the memory array (Sebastian et al., 2020). This feature leads to decreased data movement, which is highly advantageous for large data applications. In addition, Neuromorphic computing represents an alternative approach to von Neumann architectures that is utilized in artificial intelligence (AI) and machine learning (ML) systems (Marković et al., 2020; Roy et al., 2019). In this case, the system draws direct inspiration from the human brain and its neurons, effectively carrying out tasks such as pattern recognition. Additional methodologies can be considered Quantum Computing (QC) which provides the potential for solving complex problems much faster than classical computers (Ladd et al., 2010; Shor, 1999), High Radix computing for reduced interconnect complexity and increased computing density (Miller & Thornton, 2022), and Reconfigurable computing akin to the case of Field-Programmable Gate Arrays (FPGAs), which offer post-manufacturing reconfigurability, thereby yielding certain performance and efficiency advantages in specific applications (Almomany et al., 2023; Compton & Hauck, 2002; Thakare & Bhandari, 2023).

However, research on the circuit and architecture level often coincides with parallel research in the field of devices. This represents the second main path of research pursued to address the problems that occurred due to the ongoing reduction in the size of transistors. Research at the device level is closely linked to the study of integrating new materials into computing devices, which is a key step towards the future of computing beyond silicon (Gutiérrez, 2020; Iacopi & Ferrari, 2024; Liu, Chen, et al., 2020; Zhang et al., 2023).

## 1.1 Beyond Silicon Electronics

Research on alternative materials for device manufacturing has been ongoing since the early years of Transistor, as mentioned above. Various categories of semiconductors have undergone thorough examination, resulting in the successful incorporation of several of them into transistors and switching devices in general. These advancements have led to improved performance in specific applications, like the conventional and unconventional computing paradigms that were described above. The intensity of this study has increased significantly in recent times, as the challenges associated with Silicon have become more severe (Courtland, 2016). As a result, the idea of transitioning to a post-silicon era is being considered not

only as a potential but also as an inevitable step in the evolution of electronics (Yuan et al., 2023).

The advancement of material science, fabrication techniques and machinery, has generated considerable interest in novel materials. Carbon, together with its numerous allotropic forms, is widely regarded as a highly promising material to lead the future of computing electronics after silicon, as it entails a set of compelling properties and features, many of which surpass those of Silicon (Guisinger & Arnold, 2010; Lin et al., 2023).

Carbon Nanotubes (CNTs) have been one of the most mature Carbon-related technologies that have been effectively utilized in the fabrication of switching devices, specifically Carbon Nanotube Field Effect Transistors (CNT FETs) (Martel et al., 1998). This technology has already achieved a significant milestone, as researchers from MIT in collaboration with Analog Devices, have managed to develop the first-ever working and fully functional 16-bit Microprocessor completely based on CNT devices, leveraging also the well-known and open source RISC-V architecture (Hills et al., 2019). This chip, fabricated in 2019, contained a total number of 14000 CNT Transistors, which is a substantial advancement compared to Stanford's earlier MIPS-based chip of only 142 Transistors (Shulaker et al., 2013).

During the early 2000s, 2D materials emerged and started also to attract significant attention. In that field, Carbon was also the leader, as one of its allotropes, Graphene, was the first thermodynamically stable 2D-Material to be effectively isolated in 2004 (Novoselov et al., 2004) and it quickly acquired tremendous adoption by both the academia and the industry. The material's remarkable features, especially its electronic and thermal properties, were initially considered ideal for applications in electronics. As the field of 2D-Materials started to flourish, other competitors emerged, such as Transition Metal Dichalcogenides (TMDs) (Manzeli et al., 2017), Hexagonal Boron Nitride (h-BN) (Zhang et al., 2017), Black Phosphorus (Phosphorene) (Carvalho et al., 2016) and others. Each of these options possesses unique advantages that could be exploited in different types of applications in electronics, as well as their drawbacks (Fiori et al., 2014; Kaushal & Khanna, 2022). Research in that field is now vigorous and Graphene has been at the forefront due to its extraordinary properties, wide range of applications and relative ease of fabrication, particularly when compared to other 2D materials. Also the hybrid approach of combining different 2D materials, such as Graphene with h-BN or TMDs, is an emerging field of study. Such combinations can leverage the strengths of each material to

create devices with optimized properties (Dean et al., 2012; Lee et al., 2023).

Graphene is a term used to describe a single layer of carbon atoms that covers a wide area and is only one atom thick. However, as the dimensions of the material scale down to a few nanometers, the properties of the material change. Those narrow strips of Graphene are called Graphene Nanoribbons (GNRs) and are the most important emerging Graphene structures for nanoelectronic and sensor applications (Celis et al., 2016). Originally, plane large area Graphene proved to be a zero-bandgap material, meaning that it exhibited a metallic behavior and could not in any way stop the flow of electrons through it. This feature posed a significant obstacle to the incorporation of the material in switching devices. Graphene Nanoribbons on the other hand, whose operation is now governed by quantum phenomena, can have a bandgap induced. For this bandgap to be properly tuned, many different methods have been proposed. Among those methods is the application of external electric bias (Jiang et al., 2019b) or magnetic bias (Moysidis et al., 2020), the stacking and twisting of Graphene (Nimbalkar & Kim, 2020), as well the Graphene shape modulation (Jiang et al., 2018c; Karafyllidis, 2014a). While each approach has its advantages and disadvantages, the question remains: what is the most effective way to modulate the conductance of a GNR device, induce a bandgap, and preserve its properties for usage in diverse applications?

Prior investigations have already been carried out to explore the application of single layer Graphene sheets of relatively small dimensions for the development of Graphene Field Effect Transistors (GFETs) and GFETs and comparable devices have already been presented both in theoretical and experimental forms (Bennett et al., 2013; Schwierz, 2010). From their initial iterations, these devices effortlessly demonstrated the capability to operate inside the GHz range, suggesting their suitability for high-speed electronic systems and computing circuits. In addition to the electronic and thermal properties that may be utilized in conventional CMOS computing systems, Graphene's other attributes can be harnessed to drive the advancement of future electronics and broaden the scope of electronic applications by delving into new scientific domains. It's optical and some mechanical properties are very attractive, particularly when combined with the previously mentioned electronic properties, for realizing electronic devices with enhanced features, that will empower electronics for special applications. The transparency of Single-Layer Graphene (SLG), absorbing

only 2.3% of light in the visible spectrum, is ideal for light sensing applications (Shi et al., 2009), as well as for transparent electronics (Georgiou et al., 2013). The high Young's modulus of Graphene can also be exploited not only for sensors, but in general, for flexible electronics, electronics applied on flexible substrates fabrics and other special materials (Jang et al., 2016). Another key characteristic of Graphene that is very appealing to the research community and can possibly enable bringing together biology with electronics, is its biocompatibility (Bullock & Bussy, 2019; Syama & Mohanan, 2016). Graphene, albeit the existence of some contradictory results considering its cyto- toxicity, in general, is considered to be a biocompatible material, in specific forms and with a high correlation to its fabrication method. This biocompatibility feature can really come in handy for the realization of biosensors, bioimaging applications as well as tissue engineering (Bei et al., 2019).

Despite its remarkable features and broad range of applications, GNR (graphene nanoribbon) is a relatively new material that necessitates substantial research efforts in several aspects. This is crucial for its establishment in the highly competitive sector of electronic devices and electronics in general. From its fabrication and modeling to the identification of the optimal method for its utilization in nanoelectronic circuits and systems, there exists a diverse range of challenges that have to be confronted.

## 1.2 Challenges of Graphene-based Computing

One of the most significant challenges considering Graphene, Graphene nanoribbons and their incorporation into computing devices and circuits, is their effective, accurate and efficient in terms of resources, modeling. Switching devices that consist of larger area Graphene sheets, behave in a way similar to that of conventional silicon transistors, and can be accurately modeled with compact models suitable for SPICE simulations (Jimenez, 2011; Mukherjee et al., 2015; Tye et al., 2022; Umoh et al., 2013). However, as the devices, and thus the Graphene lattice itself, are miniaturized to the nanoscale following the current trends, and moving from graphene to graphene nanoribbons of just a few nanometers in size, new quantum mechanical phenomena begin to govern their operation. The modeling of such devices becomes a far more complex task that requires complicated and computationally heavy simulation methods. Those methods are very challenging, due to their complexity, to be incorporated in

SPICE simulators for easy and fast large-scale circuit simulations. Thus, the quest for a robust, unified, adaptable, and versatile simulation tool that can be accurate for a set of devices of a wide variety of dimensions and shapes remains ongoing.

As getting down to scale, apart from the modeling, Graphene nanoribbon-based devices are becoming even harder to fabricate. Their optimal properties are heavily based on the shape and condition of their nanoribbon, the width, the edge roughness and the possible presence of impurities vacancies or any other kinds of defects. Any disturbance on the pristinity of the lattice of a graphene nanoribbon can significantly affect its functionality (Lherbier et al., 2012). Thus, it becomes a challenge of high importance for the viability of GNR as material exploited in computing devices and circuits, to be able to simulate its operation and predict its behavior under the influence of defects.

Apart, from that, another significant challenge is bandgap engineering. Typically, Graphene is characterized as a zero bandgap material, a property that significantly restricts its applicability in the field of electronics. For that reason, creating a bandgap in graphene nanoribbons in order to enable them to be used in switching devices is of vital significance. Several methods have been already proposed, but the scientific community consistently seeks novel and optimized approaches.

Finally, one more significant challenge is the use of graphene nanoribbons and graphene nanoribbon-based devices in computing circuits, as well as their seamless integration with existing computing circuits and architectures. CMOS circuits with the use of MOSFETs or other typical transistors, are a very mature technology. Therefore, simply substituting conventional transistors with their GNR-based counterparts may not be the optimal way to exploit this novel material. In that manner, it is of great importance to discover a way to incorporate GNRs in electronics, through which they will provide a not marginal but substantial performance boost.

It is also challenging but significant to explore methods of combining the electronic properties of GNRs, with some of their other attributes (i.e. mechanical, optical). This will broaden the variety of applications for GNR circuits, unlock the material's complete potential, and offer answers to interdisciplinary challenges. Finding applications in fields beyond the scope of CMOS technology, will guarantee the viability of GNR technology. Finally, as mentioned above, it is of greater importance for any proposed circuit and architecture based on GNR devices, to be able to be integrated

with existing silicon-based conventional CMOS technologies. The compatibility between silicon and CMOS with GNR technology poses challenges not only during the fabrication process but also at the circuit level. This includes the requirement for matching operating voltages or an interface to connect the two distinct technologies. That way the unique properties of GNRs can be fully exploited to enhance and expand the capabilities of existing and far more mature computing infrastructures.

## 1.3 Objectives

*This Doctoral Thesis deals with some of the challenges of Graphene and Graphene nanoribbon research as presented above. It mainly focuses on the investigation of the electronic properties of Graphene through modeling and simulation, its ability to be incorporated in switching devices and its possible use in computing circuits with enhanced properties.*

In a summarized manner, the main objectives are:

1. to explore the possibility of tuning and fitting the mathematical modeling tools to in-house fabricated large-scale devices by NCSR Dimokritos.

2. to investigate and improve the state-of-the-art computational modeling methods, enhancing them with new features that will lead to the realization of more complete, robust, versatile and accurate frameworks. Such a feature is the ability to extend their abilities and make them capable of simulating even large-scale devices and many device systems.

3. to further enhance the modeling tools by providing them the significant ability of easy incorporation of different kinds of lattice defects in variable concentrations to the simulation process.

4. to thoroughly explore the effect of different kinds of lattice defects in different regions and in different concentrations on the electronic properties of Graphene-based devices.

5. to extend the use of computational models in SPICE simulations for easy many-device large-scale simulations of circuits constituted by Graphene-based devices.

6. to study the ability to harness the properties of graphene nanoribbon-based devices to design basic computing circuits with enhanced and competitive properties, for the realization of boolean logic functions.

7. to inspect the possibility of graphene nanoribbon-based devices to be used in Multi-Valued Logic circuits.

## 1.4 Contributions

After the successful experimental isolation of Graphene and the verification and study of its very appealing electronic properties, several modeling methodologies have been investigated for the simulation of its behavior. Not only for large sheet Graphene, but also for some of its allotropes such as Graphene Oxide (GO) and Graphene Nanoribbons (GNRs). The latter is considered to be one of the most promising forms of Graphene to be used in electronics. GNRs are very small-area graphene sheets, whose operation is mainly governed by quantum mechanical phenomena. The simulation of their behavior is based on complex mathematical models and methods that are used for the calculation of the electron transfer and transport in mesoscopic systems. The most common, among others, are the Density Function Theory (DFT) (Polini et al., 2008) and Non-Equilibrium Green's Function method (NEGF) (Pourfath, 2014).

The NEGF method can capture and describe the behavior of the under-investigation GNR-based device. While it is considered to be highly accurate as it describes the interconnectivity and relation between the atoms of the material's grid and their interactions with electrons flowing through it, it is computationally heavy, demanding significant resources even for small-scale devices. This makes NEGF unsuitable for large-scale, many-device simulations, where a compact model would be ideal, due to its reduced complexity.

Currently, in bibliography, the simulation of larger-scale Graphene-based devices is achieved through alternative compact models similar to those used in conventional transistors (Chen et al., 2015; Gholipour et al., 2015). The approach of this dissertation is different. In the attempt to fit a model to the experimental data of a fabricated device provided by NCSR Demokritos, the NEGF method along with the Tight Binding Hamiltonians (TBH) have been used. This choice is rooted in NEGF's ability to handle non-equilibrium conditions, its scalability, and focus on transport properties, combined with its capability for device engineering. All these make it

more suitable for graphene simulations targeted to electronic applications. The data obtained using NEGF for small-scale devices of a few nanometers, are transformed through the aid of a mathematical interface in order to effectively describe the behavior of larger-scale devices. By utilizing this mathematically enhanced model, the data extracted from simulations for very small devices, were fitted to the experimental data extracted from the much larger fabricated devices. This not only resulted in a satisfactory level of accuracy but also significantly reduced the computational time required compared to using the pure NEGF method for the actual device's dimensions. For comparison, a simple but accurate curve-fitting model as well as a circuit-equivalent model have been implemented (Vasileiadis et al., 2024). This piratically enhances the NEGF model enabling it to simulate even larger size devices, targeting towards the development of a versatile tool capable of precisely simulating both small-scale devices, measuring in nanometers, and larger-scale devices, spanning up to micrometers in size.

The computational non-equilibrium Green's function (NEGF) method was further extended to incorporate and model not only Graphene nanoribbon (GNR) grids of varying geometries, as previously demonstrated in the bibliography, but also Graphene grids with lattice imperfections. Different kinds of defects can be present on the grid of a GNR. The defects can be clustered in two main categories, corrugations and lattice defects. The first refers to disturbances of the GNR lattice as a whole, such as wrinkles, folds etc (Yang et al., 2018). Lattice defects refer to changes that happen inside the grid, such as vacancies, changes in the inter-atomic connections, adsorpsions, absorpsions etc (Banhart et al., 2011). This dissertation focuses on the simulation of the most common lattice defects which are the vacancy, specifically the single and double vacancy. With the enhanced method, users have the ability to select which of the implemented defects they want to include in the grid. They can also determine the concentration of a specific type of defect, and finally choose a region of the Graphene grid in which those defects will be placed.

The aforementioned defects, are consistently present on Graphene and GNR grids and they arise as a result of the fabrication process. As previously stated, the pristinity and symmetry of GNR grid have a substantial impact on its electronic properties, particularly its bandgap and conductance. As the dimensions of those grids are getting smaller, even small numbers of defects may significantly affect the operation of a GNR-based

device. Therefore, utilizing the enhanced NEGF method that enables precise simulation of graphene grids, in the context of this thesis, an extensive analysis of the impact of lattice defects was conducted, focusing on the effects on the electronic properties and of GNRs. More specifically, as it is known that GNR shape affects its electric behavior and operation, butterfly-shaped GNRs were simulated instead of rectangular. Those lattices were separated in regions of interest, where defects were separately accumulated. The defects that have been investigated were the two most common, which are also interconnected, the single and the double vacancy. The simulated defective grids were of variable defect concentration, spanning from 0% up to $\sim$ 15%. Initially, the investigated variables were analyzed through energy dispersion to conductance diagrams, that showed an overview of the effects of the defects. In addition, the dependence of defects on the maximum conductance was investigated, as well as the effect on the size of the energy gap. The results were consistent with prior relevant literature and revealed which parts of a variable shape graphene grid are more sensitive to defects (Rallis, Dimitrakis, et al., 2021; Rallis et al., 2019). In addition to that, further investigation has been conducted on some other parameters. As those devices are intended to be used as switches, for the first time some switching-related factors were examined. Selecting as an operating voltage a common value of $0.5Volts$, the current density with respect to the defect density was calculated, as well as a factor very significant for the realization of computing architectures, the $I_{ON}/I_{OFF}$ ratio (Rallis, Dimitrakis, Sirakoulis, et al., 2022).

This dissertation, apart from its contribution on the fields of GNR device modeling and defect evaluation, also focused on the field of electronics. However, being a computational simulation tool, the aforementioned enhanced NEGF method becomes unable to be employed for many device circuit simulations. For this problem to be surpassed, a hybrid method is pursued in an attempt to merge the gap of computational and compact modeling. An equivalent Verilog - A model is developed, utilizing the NEGF approach to calculate conductance for GNR-based devices of determined shape and structure. In this manner, the model is able to be utilized in SPICE simulations while maintaining a high level of accuracy and all the added features (i.e. defect incorporation) (Rallis, Dimitrakopoulos, et al., 2023).

One of the major problems in creating switching devices with GNRs, is the fact that graphene is a zero bandgap material. Since its discovery, there have been many approaches for the effective solution of this problem, such

as the use of magnetic contacts, external electric bias, specific graphene shaping and stacking and many more. Recently, in bibliography, the L-shaped, Z-shaped and T-shaped GNRs were investigated and proved to be able to solve the zero bandgap problem and operate effectively as switches (Moysidis & Karafyllidis, 2018). They are able to operate without the use of a back gate, facilitating their application on non-traditional substrates. On top of that, their use as the basic cells for the realization of comb-shaped topologies that are able to operate as `AND`, `OR`, and `NOT` gates, as well as, as a majority gate was demonstrated (Moysidis et al., 2018). In this thesis, for the first time, a design space exploration on the L-shaped GNRs was conducted, and the effect of their dimensions, top gate layout, and applied electric bias on their operation as switches was investigated, leading to the reasonable and appropriate selection of values for significant parameters. Furthermore, the existing set of gates was expanded, adding also the ability of comb-shaped topologies to operate as a 2-input and 3-input `XOR` gate as well as as an area-optimized `Majority` gate. Those gates were imported in SPICE using the NEGF-based model that had previously been implemented and were used for the simulation of a Full-Adder cell (Rallis, Sirakoulis, Karafyllidis, Rubio, & Dimitrakis, 2022). The proposed topologies and circuits were compared in terms of performance to other GNR-based as well as $7nm$ CMOS counterparts, where they performed similarly and even better in some of the metrics (Rallis, Fyrigos, et al., 2023). In search of further optimization on the field of electronics, reduced size, non backgated, 2-branch reconfigurable comb-shaped topologies were designed, that function based on the principles of Pass Transistor Logic (PTL), and constitute a universal set of gates (Rallis, Dimitrakopoulos, et al., 2023).

Finally, in pursuit of utilizing Graphene in beyond CMOS computing circuits, the ability of a single butterfly-shaped GNR-based device to provide an effective multi-level operation was for the first time investigated at a fundamental level. As a proof of concept, a radix-4 adder using those devices was proposed (Rallis et al., 2018b).

## 1.5 Thesis Organization

In the rest of this thesis, firstly a detailed introduction to Graphene as a material, its fabrication methods, properties and applications, is elaborated in *Chapter 2*. Then, the modeling methodology of graphene is described in *Chapter 3*, where my contribution to the enhancement of the computational

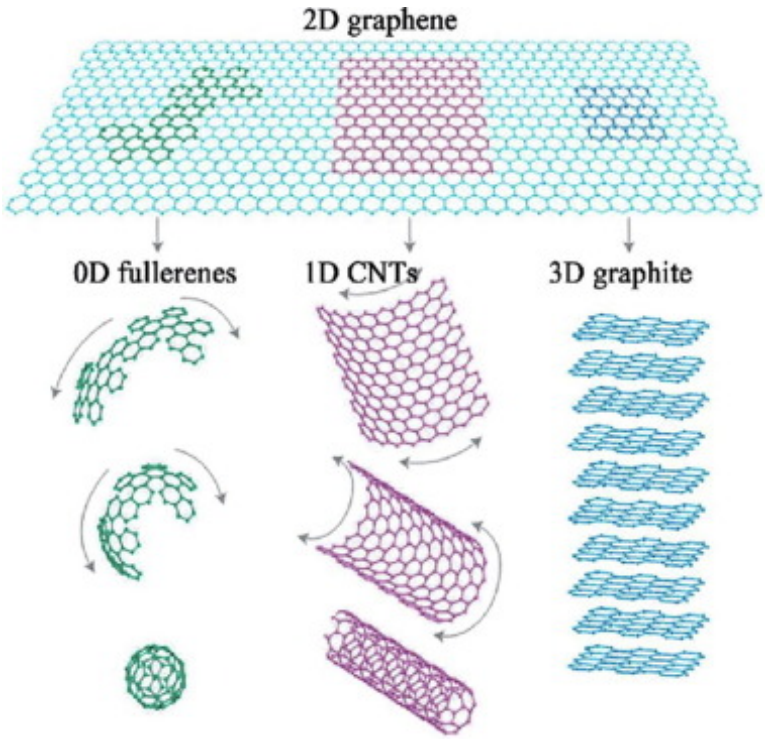
modeling and simulation tools is shown and a fitting of the tuned model to experimental data is attempted. *Chapter 4* is dedicated to the description of the categories of defects that are present in a Graphene lattice, as well as the study of their impact on the electronic properties of the material through an enhanced NEGF-based framework. The use of GNR-based devices for the design of computing topologies is elaborated in *Chapter 5*. Finally, the conclusions and scientific contributions of this Doctoral Thesis are detailed in *Chapter 6*.

# Chapter 2

# Graphene

## 2.1 The material

The term Graphene refers to a flat monolayer of carbon atoms tightly packed into a two-dimensional (2D) hexagonal lattice. It can be considered as the basic building block for a set of graphite-related materials of different shapes, dimensions and structures. It can be wrapped up into fullerenes, rolled into 1D-nanotubes or stacked into 3D graphite, as shown in Fig. 2.1. Additionally, it can be utilized in its oxidised form as Graphene Oxide (GO). All those types of materials can be referred to as the allotropes of Graphene. The material has undergone theoretical investigation for more than 70 years. However, although known as an integral part of 3D materials, graphene was considered to be unable to exist in the free state, and was believed to be thermodynamically unstable, as stated by Landau and Peierls (Geim & Novoselov, 2007). Nevertheless, the initial toy-model came to life, when graphene was successfully isolated in the form of thermodynamically stable sheets back in 2004, by the research group of Gheim and Novoselov at the University of Manchester (Novoselov et al., 2004). The simplicity and ingenuity of the experiment that led to this discovery are remarkable. The employed technique is referred to as the "Scotch Tape" approach, which entailed the utilization of a strip of adhesive tape and graphite (the material that pencils are made of). The adhesive tape was applied on the graphite and then peeled off. Repeated iterations of this technique resulted in progressively thinner coatings of graphite adhering to the tape. It was such a significant discovery that it earned the group a Nobel Prize in 2010. Since then, it has attracted a great amount of interest and research effort both in academia and industry, finding applications in a wide variety of areas. It essentially pioneered the field of 2D-materials, which has been continuously expanding since then.



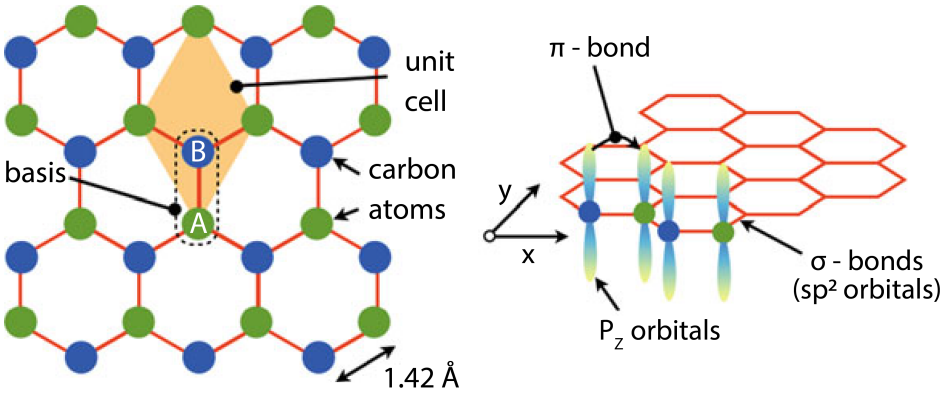

(a)

Figure 2.1: Foundation of all graphitic formations. Graphene is a 2D building material for carbon materials of all other dimensionalities. It can be wrapped up into 0D Bucky balls, rolled into 1D nanotubes or stacked into 3D graphite.

### 2.1.1 Structure of Graphene

As mentioned above, Graphene is practically a 2D Material. It is a one-atom-thick layer of carbon atoms tightly connected together with very strong covalent bonds. The fundamental hexagonal cell that comprises a bigger Graphene sheet, can be seen in Fig. 2.2a. This honeycomb structure is composed of a triangular Bravais lattice with a basis of two atoms, labeled A and B (Zhang, 2022). The distance between two neighboring atoms, meaning practically the length of a covalent bond is equal to $0.142nm$

The tightness and rigidity of its shape, its geometry, and consequently




(a) (b)

Figure 2.2: a) The basic structure of Graphene grid. The yellow rhombus represents the primitive unit cell. A and B are the two different types of atoms that shape the two different sublattices. The C-C bond length is 1.42Å. b) The chemical bonds of Graphene. Shows the $\sigma - bonds$ and $\pi - bonds$, along with their orbitals. [Adopted from (Bhushan, 2012)]

a vast amount of its properties that will be later analyzed, are a direct outcome of those strong bonds and in general, are based on the chemical composition of the material. Those strong covalent bonds that each carbon atom makes with three of its carbon neighbors, are also called $\sigma$-bonds and are achieved through $sp^2$ hybridization. Those hybrid orbitals are formed by combining one $s$ orbital with two out of the three available $p$ orbitals. They are placed on top of the plane of Graphene at an angle separation of 120 deg. Each $sp^2$ hybrid orbital of a carbon atom is connected with another corresponding orbital that originates from an adjacent carbon atom, forming the aforementioned very strong bond. The 3rd p-orbital, which is not involved in the realization of an $sp^2$ hybrid orbital, does not contribute to the formation of $\sigma$-bonds. Its direction is perpendicular to the graphene sheet and therefore perpendicular to the $sp^2$ orbitals, as seen in Fig. 2.2b. Adjacent carbon atoms exhibit overlapping p-orbitals, resulting in the formation of $\pi$-bonds. This network of $\pi$-bonds is delocalized on top of the graphene sheet and is responsible for its unusual electronic properties (Castro Neto et al., 2009). It is a half-filled system, as the vertical p-orbitals have only a single electron instead of two that would be required for them to be fully occupied. The presence of partially filled p-orbitals practically creates a conductive route for electrons to pass through them, especially

when there is the appropriate external perturbation (Peres, 2009).

## 2.2 Properties

As mentioned above, the remarkable properties of Graphene are attributed to its lattice structure. As can be derived from the analysis of the chemical bonds that are present in the material in Section 2.1.1, the $\sigma$-bonds determine its mechanical properties, while the $\pi$-bonds determine its peculiar electronic properties (Peres, 2009). In general, Graphene concentrates a set of interesting properties in a variety of fields, leading researchers to characterize it as a "wonder" material.

### 2.2.1 Mechanical Properties

Graphene is renowned for its exceptional mechanical properties. It is widely regarded to be the strongest material ever measured. The stiffness of the material has been theoretically calculated through simulations and also experimentally verified via measurements of its Young's modulus, which was determined to be $E = 1.0 \pm TPa$. This value was based on the calculation of the second-order elastic stiffness, which was found to be equal to $E^{2D} = 340 \pm 50 Nm^{-1}$ (Papageorgiou et al., 2017). The intrinsic strength of the material in the form of a pristine, defect-free monolayer grid has been calculated to be equal to $42 Nm^{-1}$ or $130 GPa$ (Lee et al., 2008). This ranks it as far stronger compared to the well known Kevlar, whose intrinsic strength has been calculated to be equal to $\sim 3 MPa$. These values however can be significantly affected and reduced by specific types of lattice defects, such as single and double vacancy, or other vacancy-type defects (Zandiatashbar et al., 2014). The fracture stress of flat graphene was also measured to be $97.5 GPa$, higher compared to that of a graphene sheet affected by wrinkles, with a fracture stress of around $60 GPa$. Finally, critical for many applications, the fracture toughness of Graphene was found to be equal to around $4.0 \pm 0.6 MPa$ (Zhang et al., 2014). Despite its strength and stiffness, Graphene also exhibits remarkable levels of elasticity and flexibility. It can stretch up to 20% of its initial strength without breaking while also maintaining its original size after strain. In fact, it can sustain repeated stretch and stress cycles without significant degradation of its mechanical properties. Graphene is one of the thinnest materials, as it is a one-atom thick 2D material, with an effective thickness of just $0.345 nm$ (Shearer et al., 2016). Additionally, it is regarded as one of the most lightweight materials

on earth, weighing just $0.77mgr/m^2$. For scale purposes, $1m^2$ of regular paper is 1000 times heavier than Graphene. Graphene is also practically transparent, as it absorbs only as low as 2.3% of white light, which is noteworthy, taking into consideration its atomic thickness. Adding another layer of graphene increases the amount of white light absorbed by approximately the same value (2.3%). Graphene's opacity of $\pi\alpha \approx 2.3\%$ equates to a universal dynamic conductivity value of $G = e^2/4\hbar(\pm 2 - 3\%)$ over the visible frequency range.

### 2.2.2 Electronic properties

Adding to that, Graphene possesses a set of remarkable and very appealing electronic properties, which make it stand out as a highly promising material for a variety of applications. Extensive research on the material has experimentally shown that its electronic mobility can reach levels higher than $15000cm^2/Vs$, This is a lot lower compared to the theoretical limit of $200000cm^2/(Vs)$, due to scattering effects (Bolotin et al., 2008). Even the experimentally reported value is considerably higher compared to that of silicon, which is equal to $1350cm^2/(Vs)$. Those values are attributed to the ballistic transport phenomenon which control´s Graphene's operation and enables charge carriers to travel without dispersion at distances up to $2\mu m$ (Tombros et al., 2007). It is also notable that Graphene is a zero-band gap material, as it does not have an energy gap between its conduction and valence bands. However, adding other elements or compounds can adjust some of its electronic characteristics, such as conductivity and band-gap, tailoring it for specific applications (Schwierz, 2010). It also displays the Quantum Hall effect even at room temperatures, which is very uncommon given that it has previously been observed only at liquid-helium temperatures. This effect involves the conductance quantization phenomenon that appears in Graphene, which can be exploited in different types of electronics (Novoselov et al., 2007a).

### 2.2.3 Other properties of Graphene

Apart from all those aforementioned mechanical and electronic properties that Graphene is well-known for, there is a set of supplementary properties which in combination with the previous, allow the material to be used in a broad range of applications. Graphene exhibits excellent thermal conductivity, with a value of $5300W/(mK)$. This feature, in combination with the

electrical conductivity, makes it highly suitable for applications related to electronics (Balandin et al., 2008).

It is also mostly bio-compatible. The bio-compatibility of graphene is dependent on its various forms, including graphene oxide (GO), reduced graphene oxide (rGO), and graphene nanoplatelets. Each of these forms possesses unique characteristics affecting its interaction with biological systems. Jointly with its lipophilic nature, it can easily interact with living cells and thus contribute to the field of biomedical engineering (Wang, Ruan, et al., 2011). Studies have shown that graphene can exhibit cytotoxicity, particularly at higher concentrations or with prolonged exposure. The cytotoxic effects include oxidative stress, membrane damage, and inflammatory responses among others. Nevertheless, the cytotoxicity is heavily influenced by the physical and chemical properties of the graphene allotrope in use (Bullock & Bussy, 2019).

All in all, graphene is notable for its exceptional strength, flexibility, and high electrical conductivity, making it promising for electronics and composites. Its thermal and optical properties further broaden its applications. However, its bio-compatibility varies, requiring careful consideration for biomedical uses. Graphene's versatility is enhanced by its tunability, offering tailored solutions across multiple technological areas. Nevertheless, all those properties are heavily based on the quality of the Graphene grid. It has to be in pristine condition to operate properly. The presence of defects or any other anomalies can severely impact its special characteristics. Therefore, its behavior and performance are highly related to the reliability of the fabrication method flow that will be employed.

## 2.3 Fabrication

The production methods of Graphene can be broadly classified into two primary categories: the top-down methods and the bottom-up methods. The top-down processes involve the utilization of a bulk material, such as bulk graphite, which undergoes exfoliation to generate thinner graphene sheets. On the contrary, the bottom-up processes entail the assembly of graphene from smaller molecules or atoms. The synthesis of graphene is achieved from the ground up and can provide better control over the structure and thus the properties of the resulting material.

### 2.3.1 Top-down Methods

#### Mechanical Exfoliation

This technique, which was developed in the initial stages of Graphene investigations, involves manually separating graphene layers from graphite using adhesive tape. The principle behind this technique is harnessing the weak van der Waals forces that bind graphite layers together. Those layers have a distance of $0.33nm$ and the energy of their bonds is equal to $2eV/nm^2$. Apart from the scotch tape, other means can be used for mechanical exfoliation, such as the application of electric field (Liang et al., 2009) and ultrasonication (Ci et al., 2009). Despite being a labor-intensive process with low yield, mechanical exfoliation produces graphene of exceptional quality with minimal defects, ideal for high-precision electronic devices and any other field of research where the quality of graphene is paramount. However, the method's impracticality for large-scale production limits its use in laboratory-scale experiments and niche applications.

#### Chemical Exfoliation

Chemical exfoliation is another common top-down method for obtaining single-layer Graphene. It provides a more scalable approach, suitable for industrial production. This process involves introducing chemicals like alkali metals into graphite solutions, which will lead to the reduction of the interlayer van der Waals forces, and to the formation of graphene-intercalated compounds (GICs). Those compounds are then dispersed in a liquid medium, in order to finally form monolayer graphene through an exothermic reaction (Viculis et al., 2005). Potassium is a frequently utilized alkali metal in this manufacturing procedure. Other alkali metals have also been employed, such as Cesium (Cs) and also $NaK_2$ alloy (Viculis et al., 2003). The primary benefit of alkali metals lies in their comparatively small atomic size. This size is smaller than the spacing between layers in graphite, allowing them to easily fit within these interlayer spaces. The versatility of this method enables the production of various graphene derivatives, crucial for applications in batteries, supercapacitors, and composite materials. Despite being scalable and operated at relatively low temperatures, the resulting graphene often contains more defects than mechanically exfoliated graphene, potentially limiting its use in applications where electrical and structural integrity are crucial (Adetayo, Runsewe, et al., 2019).

### Chemical Synthesis

Chemical synthesis, particularly the reduction of Graphite Oxide (GO), is a widely used method for producing graphene on a large scale. There are three main variations of Chemical Syntehsis, the Brodie method (Das et al., 2015), the Staudenmaier method (Adetayo, Runsewe, et al., 2019) and the Hummers method (Hummers Jr & Offeman, 1958). They are mentioned in chronological order and each one of those is practically an extension of the previous. Hummers method is the most common among the others, and it is still widely used today. This process starts with the oxidation of graphite through mixing with sodium nitrite ($NaNO3$), concentrated $H_2SO4$ and potassium permanganate ($KMnO4$). Modifications of the Hummers method have also been proposed, targeting to higher oxidation efficiency and to better quality of the final product (Graphene) (Marcano et al., 2010). This oxidation process leads to increased interlayer distances, which is further enhanced through ultrasonication, finally creating individual layer suspensions (Adetayo, Runsewe, et al., 2019). Then, the newly formed GO is reduced back to Graphene or reduced graphene oxide (rGO). This reduction is achieved mainly using hydrazine or dimethyl hydrazine in the presence of a polymer. Reduction can be also achieved with the exploitation of other chemicals as reducing agents such as sodium borohydride ($NaBH4$), hydrxylamine, hydroquinone, ascorbic acid and many more. Apart from those reducing agents, there are several other common methods for reduction such as thermal reduction (Wong et al., 2012), electrochemical reduction (Shao et al., 2010), photochemical reduction (Stroyuk et al., 2012), hydrothermal reduction (Krishnamoorthy et al., 2012) and reduction through microwave radiation (Dai et al., 2013). The resulting material is versatile and can be used in a range of applications, including sensors, coatings, and energy storage devices. However, the presence of residual functional groups and defects from the oxidation process can affect its electronic properties, making it less suitable for applications requiring high electrical conductivity. Those remaining functional groups on Graphene and rGO can however be exploited and utilized to precisely adjust the materials' electronic and chemical properties, according to the desired application.

#### Unzipping of Carbon Nanotubes (CNTs)

A novel approach to the synthesis of graphene entails the methodical unzipping of carbon nanotubes (CNTs) to produce graphene nanoribbons (GNRs) with specific dimensions. This technique utilizes multiwall carbon nanotubes (MWCNTs) which are unzipped through a variety of experimental procedures, including the application of acid mixtures (Li et al., 2016), catalytic cutting techniques (Wang, Ma, et al., 2011), electrical unzipping (Zheng et al., 2020), and hydrogen-induced unzipping (Tsetseris & Pantelides, 2011), among others. In the catalytic cutting process, CNTs are the precursor material. During this process, the carbon atoms within the CNTs migrate onto metal nanoparticles at approximately 900 deg $C$ in an argon-hydrogen atmosphere. As these particles reach a point of saturation, they undergo a reaction with $H_2$. The orientation of the cut, which can lead to either armchair or zigzag edges, is influenced by the size of these nanoparticles. It has also been documented that the use of Nickel (Ni) or Cobalt (Co) facilitates the longitudinal incision of MWCNTs to form graphitic nanoribbons, with lengths typically ranging from $100 - 500$ nm and widths between $15 - 40$ nm (Elías et al., 2010). Similarly, oxidative splitting has been proposed in (Wang, Wang, et al., 2020) for the synthesis of GNRs. This method involves the use of $(NH_4)_2S_20_8$ in ahydrous acidic media. However, the produced GNRs are enriched with oxygen functionalities, which can change their properties. This problem can be effectively hindered through irradiating MWCNTs with a low energy laser pulse of $\sim 300mJ$ (Kumar et al., 2011).

### 2.3.2 Bottom-up methods

#### Pyrolysis

Pyrolysis is a cost-effective and simple method to produce graphene. It can be described as solvothermal as it involves decomposing organic precursors under high temperatures in a controlled environment (Bhuyan et al., 2016). This controlled environment concsists of a closed vessel under high pressure with a 1:1 ratio of ethanol and sodium. The sheets of graphene can be produced by the pyrolysis of sodium ethoxide with the assistance of external sound energy application (sonication). The quality of graphene produced through pyrolysis varies significantly based on the precursor used and the process conditions, such as the temperature. While this method has the capability to generate large quantities of graphene, controlling the

layer thickness and minimizing defects remain challenging. Applications that pyrolysis generated Graphene can be used include bulk composites, where high conductivity is not a primary requirement.

### Epitaxial Growth on SiC Surface

Epitaxial growth on single-crystalline silicon carbide ($SiC$) surfaces is one of the most well-known and sophisticated methods for producing high-quality graphene with well-defined layers. Being a bottom-up method, it allows the growth, the deposition of an epitaxial film (single-cyrstalline) on a substrate. This process of epitaxial growth on $SiC$ substrates, results in the formation of heteroepitaxial graphene, as the epitaxial film and the substrate consist of distinct materials. The process involves heating $SiC$ under ultra-high vacuum conditions, causing the silicon atoms to sublime and leaving behind a layer of graphene. The early versions of the method produced Graphene, which however could not be transferred to other substrates (De Heer et al., 2007). A modification of the method, which uses $SiC$ substrate coated with Ni catalyst, provided the ability to produce graphene that could be easily transferred to other substrates (Juang et al., 2009). The epitaxial graphene produced is of very high quality, highly crystalline and suitable for advanced electronic applications, such as high-frequency transistors and sensors. However, the high cost due to high-energy demand and expensive equipment, as well as the complexity of the process and the general difficulty in transferring the graphene to other substrates, limit its widespread use.

### Chemical Vapor Deposition (CVD)

CVD is a prominent method for producing high-quality, large-area graphene films. It involves the decomposition of hydrocarbon gases on a heated metal substrate under controlled conditions. The quality of graphene produced by CVD is suitable for electronic applications, transparent conductive films, and flexible electronics. However, the process requires precise control of parameters like temperature, pressure, and gas flow rates. Additionally, it is prone to generate defects during the process of transferring Graphene from the initial metal substrate to a targeted alternative one.

- **Thermal Chemical Vapor Deposition:** The production of graphene through this method involves the introduction of precursor gases like

methane, hydrogen, and argon in specific proportions into a quartz tube. This tube contains a substrate, for example, copper, and is heated to high temperatures in a furnace. Over time, graphene deposits onto the substrate, forming single, bi, or multilayers, depending on various preset factors such as the rate of gas flow, reaction duration, pressure, and temperature. The Chemical Vapor Deposition (CVD) process, widely utilized for producing Graphene of superior quality, utilizes various transition-metal substrates like Ni (Guo et al., 2010), Pd (Choucair et al., 2009), Ru (Sutter et al., 2008), Ir (Coraux et al., 2008), and Cu (Reina et al., 2009), which function as catalysts. These substrates are combined with different hydrocarbons including methane, benzene, acetylene, and ethylene (Reina et al., 2009). When these transition metals are subjected to hydrocarbon gas at elevated temperatures, carbon accumulates on the substrate, eventually forming a thin carbon film upon cooling. Among those, the growth of Graphene on Cu substrate (Cu foil) has been extensively explored and optimized towards better material quality (Lee et al., 2015). After the shaping of graphene on the Cu foil substrate, follows the transfer of this material to an appropriate substrate. A common substrate, especially for electronics applications is $SiO_2/Si$. For this process, initially, the Graphene layer is covered with polymethyl methacrylate (PMMA) for protection, while the Cu foil is etched away with the help of $Fe(NO_3)_3$ or a similar solution. The remaining PMMA/Graphene heterostructure is then cleaned from any remaining etching solution and added to the same di-ionized water solution with the substrate. The two are joined by van der Waals bonds, and the PMMA is then removed, using an appropriate solvent, such as acetone or isopropyl alcohol (Lee et al., 2015).

Overall, the growth of graphene using the CVD technique has predominantly been conducted on Cu and Ni substrates (Reina et al., 2009; Wei et al., 2009). The challenge with employing Ni substrates is the lengthy, non-self-limiting growth process, alongside the formation of numerous wrinkles and folds. In contrast, copper substrates have shown more promising results for graphene growth through CVD (Li et al., 2009).

- **Plasma Enhanced Chemical Vapor Deposition:** The synthesis of

Graphene with this technique entails a sequence of chemical reactions of gases in a vacuum chamber in the presence of plasma, leading to the formation of a thin film on the substrate's surface. This technique is known as plasma-enhanced chemical vapor deposition (PECVD). The plasma in PECVD can be generated through various sources, including radio frequency (RF), microwave, and inductive coupling (which involves electrical currents created by electromagnetic induction). The PECVD process for synthesizing graphene is carried out at lower temperatures and requires shorter deposition times compared to other CVD methods, making it better suited for large-scale industrial applications. By adjusting the process parameters, it's possible to grow graphene even without a catalyst (Shang et al., 2008). RF plasma-enhanced chemical vapor deposition has been successfully used with substrates like Ti, $SiO_2$, Si, $Al_2O_3$, Mo, Hf, Zr, Nb, Cr, W, Ta, and 304 stainless steel (Das et al., 2015). This approach not only reduces energy consumption but also minimizes the creation of undesirable byproducts or amorphous carbon (Zhu et al., 2007).

The Plasma Enhanced Chemical Vapor Deposition (PECVD) technique has been established as a method for producing high-crystallinity, high-purity graphene. Nevertheless, there is ongoing extensive research focused on achieving uniform, large-scale production of single-layer graphene using this method.

## 2.4 Characterization

### 2.4.1 Optical Microscopy

Optical microscopy is a valuable method for analyzing Graphene, despite its single-atom layer thickness. In fact, the first observation of graphene was achieved using a standard optical microscope (Folorunso et al., 2022). The visibility of the material under such a microscope depends on various factors. When placed on a $Si/SiO_2$ substrate, its visibility is influenced by the number of layers and the thickness of the $SiO_2$ layer. On a clean silicon substrate, graphene is invisible, but the oxide layer's thickness is crucial for imaging (Subramaniam et al., 2023). The distinct colors and contrasts seen are due to diffraction and interference effects. This method is also applicable to other substrates like $Si_3N_4$ or polymethyl methacrylate, provided they are of suitable thickness (Blake et al., 2007). Techniques like thermal

annealing are used to visually distinguish graphene on metallic substrates, where heat treatments highlight differences in multilayer graphene stacks on substrates like Copper (Cu), Nickel (Ni) and others (Jia et al., 2012). This approach is excellent due to its simplicity and speedy results, although it has limitations in resolution.

### 2.4.2 Scanning Probe Microscopy (SPM)

Scanning probe microscopy (SPM), a widely utilized method for analyzing the surface details of nanomaterials like Graphene, operates by sweeping a probe across the sample. Atomic force microscopy (AFM) and scanning tunneling microscopy (STM) are two commonly used SPM techniques for the examination of Graphene. AFM operates by either contact or non-contact tapping of the probe tip, where the cantilever probe's deflection, responding to Graphene's surface chnages, provides 2D and 3D images (Adetayo, Runsewe, et al., 2019). STM, on the other hand, produces images of the sample's surface pattern based on the tunneling current established between the SPM probe and the graphene (Luican et al., 2009).

### 2.4.3 Scanning Electron Microscopy (SEM)

Scanning Electron Microscopy (SEM) is employed to acquire detailed images of the surface morphology of Graphene. This technique offers benefits like detecting impurities, folds, and synthesis-related discontinuities in Graphene. However, its resolution is limited for ultra-thin graphene layers. It involves scanning a focused beam of electrons over the sample. The electrons interact with the atoms of the Graphene grid, producing various signals, such as secondary electrons, backscattered electrons and X-rays, that can be detected and converted into high-resolution images (Subramaniam et al., 2023). SEM is higly-effective in examining the layering and surface features of graphene flakes but fails to quantify the thickness of Graphene sheets. Additionally, it necessitates the application of a conductive coating on samples that are non-conductive.

### 2.4.4 Transmission Electron Microscopy (TEM)

Transmission Electron Microscopy (TEM) is a highly effective technique employed in the field of Graphene research and development. TEM operates by projecting a high-energy electron beam onto a sample. The interactions of these electrons with the sample's atoms yield data that can

be used to determine numerous features, such as layer thickness, crystal structure, dislocations, and grain boundaries (Seekaew et al., 2014). Due to the electrons' small wavelength, TEM offers very high resolution, enabling efficient analysis of the shape and size of nanomaterials. TEM is particularly useful for investigating the growth of layers, identifying defects in crystal structures, and has been extensively used in examining Graphene and its nanocomposites (Subramaniam et al., 2023).

### 2.4.5 Raman Spectroscopy

Raman Spectroscopy is one of the most common non-destructive key techniques for analyzing the layers and structural integrity of graphene (Vandenabeele, 2013).Due to its sensitivity to variations in the electrical environment, it serves as a valuable instrument for evaluating the quality of graphene, determining the number of layers, analyzing strain effects (Li et al., 2010), and detecting the presence of defects. This method uses monochromatic radiation that interacts with graphene's molecular vibrations, causing a shift in radiation due to scattering (Graves & Gardiner, 1989). Three primary peaks, namely D, G, and 2D peaks, are observed in Graphene's Raman spectrum. The D-peak, appearing at $1350cm^{-1}$, indicates $sp^2$ hybridization disorder (Eklund et al., 1995). The G-peak, at $1580cm^{-1}$, reflects lattice vibrations, while the 2D-peak at $2700cm^{-1}$ arises from second-order Raman scattering at the Dirac point (Wang et al., 2008). The intensity ratio of the D and G peaks ($I_D / I_G$) changes in relation to the level of disorder in Graphene, increasing with more defects but decreasing as the structure becomes more amorphous (Mbayachi et al., 2021).

Each of these characterization methodologies offers unique insights into the properties of Graphene, aiding researchers in understanding this material's potential for diverse applications like electronics, energy storage, and material science. Different applications may prioritize different properties. Commonly analyzed Key characteristics include the Graphene sheets' disorder level, stacking arrangement, lateral size, and functional groups. By combining these methods, a comprehensive understanding of graphene's physical and chemical properties can be achieved.

## 2.5 Applications

Graphene has indeed receive tremendous adaptation from both academia and industry. Due to its spectacular properties it has find application in

many fields. It has been succesfully used in composite materials. Due to its strength and light weight, Graphene is incorporated into various materials, including plastics, metals, and concrete, to enhance their mechanical properties and electrical conductivity. It has also been utilized in the field of coatings and paints due to its exceptional barrier capabilities, protecting surfaces from corrosion, UV light, and providing electrical conductivity. Its mechanical properties have found applications in the automotive and aerospace sectors where Graphene is used to develop lighter and stronger materials, that contribute to fuel efficiency and overall performance.

Most of the above uses primarily rely on the mechanical capabilities of the material, rather than its electronic properties. Nevertheless, the material encapsulates a set of fantastic properties that make it appropriate for a wide variety of applications in the field of electronics. In par with the contents of this dissertation, Graphene's applications in electronics will be analyzed more.

### 2.5.1 Energy Storage and Power Delivery applications

Graphene's extensive surface area makes it a valuable material for energy storage applications, including batteries and supercapacitors (Mbayachi et al., 2021). In the realm of Li-ion batteries, graphene serves as an effective anode material, boasting a capacity of approximately $1000 mAhg^{-1}$, which is three times higher than that of conventional graphite electrodes. This enhancement not only allows for batteries with extended durability, but also enables them to recharge much quicker, often within seconds, and can possibly provide them with special characteristics, such as tolerance in low temperatures (Selinis & Farmakis, 2022). Additionally, graphene's inherent flexibility has led to its use in solid-state supercapacitors integrated into textiles, paving the way for innovative wearable electronics (Abdelkader et al., 2017).

### 2.5.2 Computing with Graphene

#### Graphene in Digital Computing

Graphene is considered a promising alternative to Silicon in electronics applications and thus is considered one of the most prominent candidates to drive the post-silicon era. Its most well-known application in Computing is the successful fabrication of a complete Carbon Nanotube FET based Microproccesor, as mentioned in Chapter 1 (Hills et al., 2019). Apart

from that, Graphene in its other forms, especially as single layer Graphene Nanoribbon, has been employed in the development of various types of switching devices, with a structure similar to that of a Field Effect Transistor (FET). These devices possess entail intriguing features, such as low power consumption and high-speed operation (Schwierz, 2010). In fact, various iterations of a Graphene-based transistor have been proposed, including the more common MOS GNR FET, the Schottky barrier GNR FET (Chuan et al., 2023), the side-gate transistor (Di Bartolomeo et al., 2016), the GNR tunneling transistor (Zhao et al., 2013), the vertical transistor (Liu, Liu, & Duan, 2020) and many more. Each iteration offers distinct advantages and disadvantages. This enabled their compatibility with a variety of applications, including ultra-fast terahertz communication applications (Boubanga-Tombet et al., 2021; Gayduchenko et al., 2021), microwave applications (Saeed et al., 2022) and many more. Following the development of the initial Graphene-based switching devices, further research has been carried out around the field of digital circuits that leverage their unique properties. Recently, Jiang et al. investigated the ability of Graphene Nanoribbon (GNR) based devices to constitute digital circuits in a manner similar to CMOS. In fact, he effectively utilized the capacity of GNRs to modify their characteristics by altering the configuration of their lattice and managed to map all the basic logic gates to single devices with variable shape (Jiang et al., 2018c). These devices were subsequently employed to construct complementary circuits with enhanced performance (Jiang et al., 2018d). Apart from that, Moysidis et al. managed to effectively design non-back gated GNR-based topologies that implement all the standard Boolean logic gates, enabling them to be used in special applications (Moysidis et al., 2018). Recently, in the field of spintronics, Graphene's efficient spin transmission has been exploited for the realization of a topology that in combination with nanomagnets is able to transmit, write, and read information. The innovation allows for a multistate spin-majority logic function, which can be adapted to perform various Boolean operations including (N)AND, (N)OR, and XNOR (Khokhriakov et al., 2022).

#### Graphene for Neural/Neuromorphic Computing

Graphene as one of the novel 2D materials to be used in future electronics is extensively explored for its Neural and Neuromorphic computing capabilities. In that direction, several devices have been fabricated and examined in the literature, demonstrating a favorable performance. Hence,

the integration of Graphene with other materials has demonstrated the capability to create devices exhibiting non-volatile resistive switching behavior (Das et al., 2023). The combination of Graphene with $Al_2O_3$ in a structure similar to that of a GFET (Schranghamer et al., 2020), the $Graphene \setminus WSe_{2-x}O_y \setminus Graphene$ memristor (He et al., 2020) and the more common Graphene Oxide Memristor (Hui et al., 2017) are some of those devices. Graphene has been employed as either an electrode or an intermediate layer in those applications (Das et al., 2023). In fact Graphene-based devices exhibiting memristive behavior have been employed in the field of neuromorphic computing, serving as either an artificial neuron or a synapse (Abunahla et al., 2020; Kireev et al., 2022). In the work of Wang et al., both synapses (Wang, Laurenciu, Jiang, & Cotofana, 2021) and neurons (Wang, Laurenciu, Jiang, & Cotofana, 2020) have been succesfully realized using Graphene, and a fully functional spiking neural network with learning capabilities has been presented (Wang, Laurenciu, & Cotofana, 2021).

### 2.5.3 Graphene in sensors

Graphene's remarkable properties have resulted in its incorporation into a diverse range of sensor technologies, showcasing its versatility and potential across various fields. In the realm of electronic sensors, graphene is utilized to create tactile pressure sensors employing mechanisms like piezoelectricity (He et al., 2023), piezoresistivity (Zheng et al., 2020), capacitance (Šiškins et al., 2020), and field-effect transistors (FETs) (Shin et al., 2017), tailored for applications in healthcare and health monitoring (Lou et al., 2016). These sensors, characterized by their flexibility, high sensitivity, and durability, are utilized in medical diagnostics, robotics, and automatic electronics. The material's adaptability is further highlighted in the development of wearable electronics, where graphene's integration onto textile fibers enables the fabrication of flexible, transparent, and durable LEDs and touch sensors (Torres Alonso et al., 2018). With the same material, optical waveguide tactile sensors have been fabricated (Kim et al., 2018), as well as transparent and flexible UV sensors, which provide high optical transparency and electric reliability (Pyo et al., 2019). A very interesting application is the monolithic integration of Graphene with conventional CMOS circuits for the realization of a circuit operating as a high mobility phototransistor with image sensing capabilities at the visible and infrared light spectrum (Goossens et al., 2017). In addition, Graphene's

application extends into the domain of biomolecule sensors, where its capabilities are harnessed to develop electrochemical sensor arrays for cell sensing. These arrays have the ability to accurately classify different cell types with nearly 100% accuracy, which is a crucial advancement for cancer diagnosis and treatment purposes (Wu, Ji, et al., 2017). Furthermore, it plays a pivotal role in the noninvasive monitoring of a set of other electroactive materials in human body fluids (Wang et al., 2017), as well as in the identification of DNA sequences, underpinning the advancement in clinical diagnostics, systems biology, and personalized medicine (Sang et al., 2019). The development of graphene-based glucose monitoring systems that are noninvasive, transdermal, and capable of continuous blood sugar recording exemplifies the strides being made towards improving patient care and managing conditions such as diabetes (Lipani et al., 2018). In the field of gas molecule sensors, Graphene enhances the detection of hazardous gases, offering exceptional sensitivity, selectivity, fast response, and good reversibility, crucial for environmental monitoring and protecting human health. Its integration into sensors for detecting $NO_2$, hydrogen ($H_2$), and other gases demonstrates improved performance metrics. These include enhanced sensitivity and quicker response/recovery times, indicating Graphene's significant impact on the development of efficient and reliable gas sensors (Guo et al., 2018; Wu, Tao, et al., 2017). Furthermore, the integration of graphene-based sensors with conventional CMOS circuits has been utilized in various technologies such as cloud computing and the Internet of Things (IoT), enabling innovative real-time, long-distance monitoring of gas concentrations. This highlights Graphene's transformative potential in sensor technology (Mortazavi Zanjani et al., 2017). Graphene, in the form of various of its allotropes, can be utilized in various temperature sensors with enhanced properties, including transparency and stretchability (Nag et al., 2022). Additionally it can be for printable sensors through inkjet-printed technology (Soni et al., 2020; Vuorinen et al., 2016). In general, graphene-based temperature sensors pose remarkable sensitivity to temperature variations, making them well-suited for fast and sensitive applications. Similar sensors can also be utilized for humidity sensing (Lv et al., 2019). The integration of these two elements enables the development of more advanced applications such as electronic skins (E-skins) for human-machine interfaces (Sang et al., 2019; Zhou et al., 2021). Graphene, in its different forms, can be utilized as an active material to provide a wider range of sensors. Multiple unique properties of Graphene are often integrated in most technologies to create a device with novel and

improved characteristics.

### 2.5.4 Biomedical applications

Graphene's biocompatible nature, along with its electronic and mechanical capabilities, make it a suitable material for biomedical applications. In addition to its biomolecule sensing applications described above, Graphene is favored for its ability to promote cell adhesion and proliferation, along with its ability to deliver electrical stimulation. Its optical transparency is particularly beneficial for neural network studies and examination of cortical features, complementing techniques such as optogenetics and calcium imaging (Hébert et al., 2018). The transparency of the material enables the development of revolutionary devices for direct brain interfacing, such as flexible electrodes and graphene field-effect transistors (GFETs) for neural signal recording in brain-computer interfaces. These devices can conform to the brain's surface for stable signal recording and are used for neuro-stimulation in treating diseases like Parkinson's and epilepsy. Implantable neural electrodes using graphene encapsulated on copper microwires, demonstrating reduced toxicity to brain tissues and high MRI compatibility have been developed. This opens new avenues for studying brain activity and clinical applications that require continuous MRI and electrophysiological recordings (Zhao et al., 2016). Graphene electrodes also enable multimodal neural recording and stimulation, supporting artifact-free MRI studies, simultaneous in vivo calcium imaging, and electrocorticography (ECoG) recording (Bakhshaee Babaroud et al., 2022). Furthermore, GFETs based on CVD graphene offer an intrinsic amplification effect, leading to a higher signal-to-noise ratio (SNR) than traditional electrodes (Lu et al., 2018). Such devices have demonstrated high-fidelity in vivo recording of cortical signals at very low frequencies (Masvidal-Codina et al., 2019) and have simplified the technical complexity of multiplexed neural probes by allowing for in situ amplitude modulation of neural signals (Garcia-Cortadella et al., 2020). Another field that Graphene finds broad application is drug delivery systems. Graphene oxide (GO), with its extensive surface area and exposed functional groups (epoxy, hydroxyl, carboxylic, carbonyl, etc.), provides numerous binding sites for organic/inorganic molecules. This property makes it an ideal candidate for efficiently attaching and transporting different drugs and biomolecules (Muñoz et al., 2019).

### 2.5.5 Graphene Flexible Electronics

Several of the previously stated applications encapsulate the property of flexibility. With the help of Graphene, either alone or in combination with other 2D materials, many flexible and also printable electronic devices have been realized. Computing devices, such as flexible resistive switches and transistors for different applications have been developed. Additionally, there are flexible sensors of different kinds available, including piezoelectric, temperature, humidity, chemical or biological, and many more. As mentioned above, flexible supercapacitors have also been presented. Combining this property with the optical properties of graphene, flexible solar cells are under investigation. In general, flexibility is one of the key features of graphene. It is often related to printable and wearable electronics, which can be fabricated on fabrics. Generally, the flexibility attribute of Graphene is utilized in conjunction with its other characteristics in every possible application.

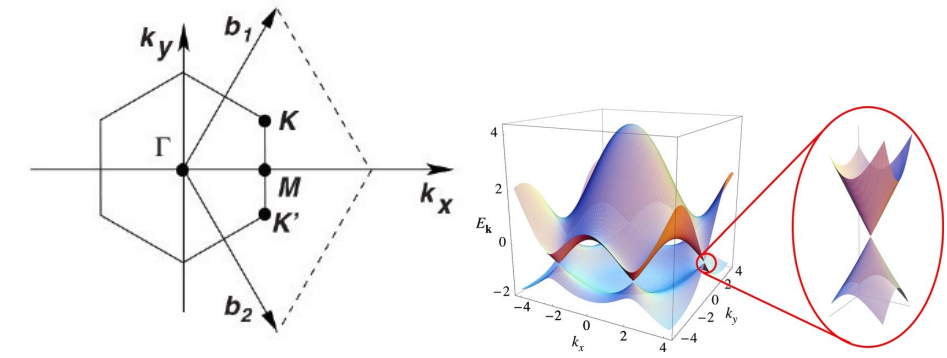
## 2.6 Electronic band structure of Graphene

The electronic band structure of Graphene is quite interesting and special as it is responsible for most of its extraordinary electronic and physical properties. It can be accurately derived through the tight binding approximation model. Due to the symmetry of the graphene grid, this investigation can be conducted on the first first Brillouin zone of Graphene, as shown in Fig. 2.3a. The points at the edges of the presented hexagon correspond to the location of the carbon atoms and are called the Dirac points. The first Brillouin zone of graphene contains 6 Dirac points.

As presented initially by Wallace, based on the structure of the Graphene lattice and utilizing the tight binding approximation model that takes only the nearest neighbor interactions into consideration, the energy bands are shaped following Eq. 2.1 (Wallace, 1947):

$$E_{\pm} = \pm t\sqrt{3 + 2cos(\sqrt{3}k_y a) + 4cos(\frac{\sqrt{3}}{2}k_y a)cos(\frac{3}{2}k_x a)} \tag{2.1}$$

, where $t$ is the is the nearest-neighbor hopping energy (hopping between different sublattices) and the two different signs ($\pm$) correspond to the upper and lower bands, respectively. Based again on Fig. 2.2a, the coordinates of the two marked Dirac points in the momentum space are the




(a) (b)

Figure 2.3: a) The First Brillouin Zone of Graphene. K and K′ are the Dirac points, the location of the Dirac cones. Vectors b1 and b2 shape the unit cell. b) The complete band structure of Graphene. Focus on the Dirac points, where the Dirac cones appear, and the conduction and valence bands intersect. [Adopted from (Castro Neto et al., 2009)]

following (Castro Neto et al., 2009):

$$K = \left(\frac{2\pi}{3a}, \frac{2\pi}{2\sqrt{(3)}a}\right), K' = \left(\frac{2\pi}{3a}, -\frac{2\pi}{2\sqrt{3}a}\right) \tag{2.2}$$

Through the combination of Eq. 2.1 and Eq. 2.2, it occurs that there is a touching of the two regions, of the upper and lower band at the Dirac points. This phenomenon is illustrated in the focused part of Fig. 2.2b, where the upper and lower halves of the Dirac cone make contact with one another. Those two halves of the Dirac cone that intersect are practically the conduction and the valence bands. This signifies the metallic behavior of the material and thus the absence of bandgap (Castro Neto et al., 2009). Analyzing the band structure very close to the K (or K′) vector, at a position $k$ where $k = K + q$ and $|q| \ll |K|$, it occurs that there is a linear dispersion both for the upper and lower part of the cone, in all 6 edges (Dirac points) of the first Brillouin zone as seen in Fig. 2.2a. This indicates that the electron's energy $E$ and momentum $k$ are linearly dependent (Castro Neto et al., 2009), similar to a photon with zero mass in vacuum. This practically indicates that the effective mass of the electron has become zero. Graphene lattice atoms do not impede to the movement of electrons,

instead, the electrons can be transported smoothly at a very high speed. Their speed at those places is as high as $c/300$, where $c$ represents the speed of light. This behavior exhibits similarities to Dirac fermions. The movement of electrons now obeys the modified Dirac equation, which takes into account the 2D nature of graphene and the effective "speed of light" within the material (Zhang, 2022).

## 2.7 From Graphene to Graphene Nanoribbons

As mentioned above, one of the allotropes of Graphene, in its 1D configuration is the Graphene Nanoribbon (GNR). GNRs are one of the most prominent forms of graphene to be used in electronics. In particular, GNRs are very narrow sheets of SLG, having a width smaller than $100nm$. Their small dimensions make them appropriate to be used in switching devices that will follow the sizing trend of the state of the art silicon based electronics. In fact, Graphene Nanoribbons inherit many excellent properties of graphene, such as high electrical conductivity and high thermal conductivity. Now in such a small size, the quantum phenomena that govern the operation of Graphene, particularly ballistic transport, become dominant. This characteristic enables the rapid transmission of electrons through a GNR channel, as now the electrons practically encounter minimal obstructions. The edge states play a significant role in this operation. For instance, the zig-zag edges possess localized states, which increase the Density of States (DoS) at Fermi Energy level and significantly affect the electronic and magnetic properties of the GNRs (Castro Neto et al., 2009; Dutta & Pati, 2010).Hence, GNRs can be characterized and classified based on the morphology of their boundaries. The two varieties distinguished by this criterion are the zig-zag edged GNRs (zGNRs) and armchair-edged GNRs (aGNRs).

In Fig. 2.4a, a zGNR is illustrated, as well as its corresponding band structure in Fig. 2.4c, calculated using the tight binding approximation model.According to the band structure diagram, it is evident that a pristine zGNR does not possess an energy gap. This is because there are regions, namely on the left and right sides of Fig. 2.4c, where the conduction and valence bands are in direct contact. This also highlights one of the most significant obstacles for the incorporation of zig-zag Graphene Nanoribbons in electronic devices: A zGNR is a zero-band-gap material and exhibits metallic characteristics (Castro Neto et al., 2009). On the other hand, in Fig.

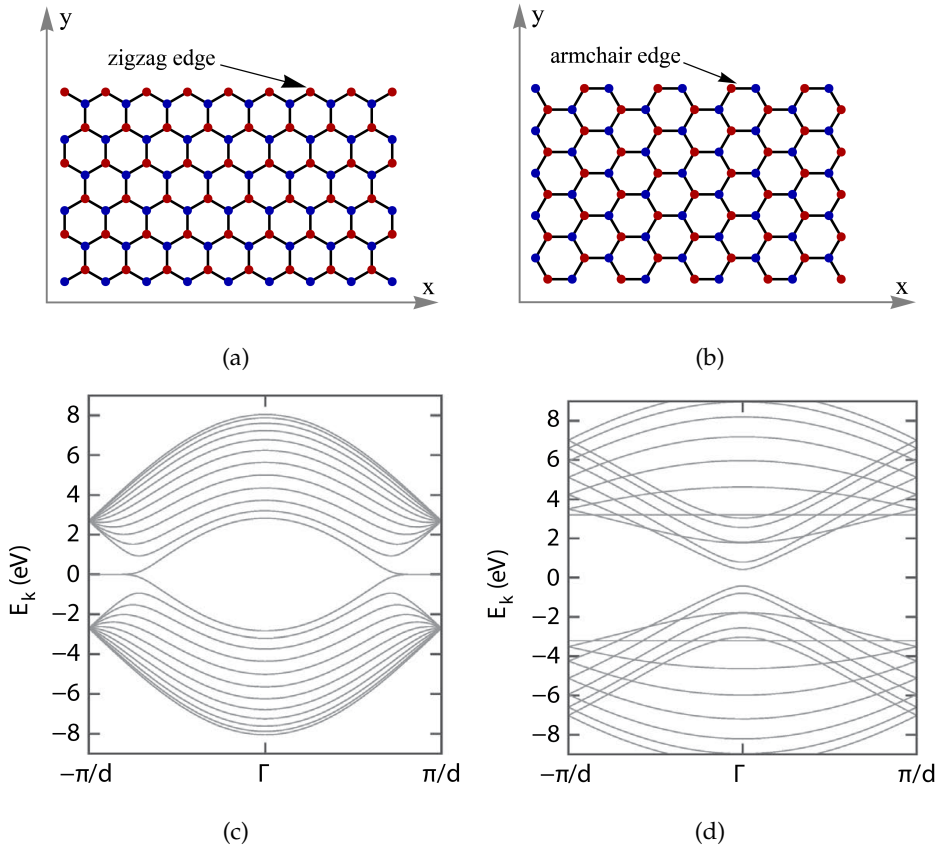



Figure 2.4: a) Zigzag graphene nanoribbon (ZGNR). (b) Armchair graphene nanoribbon (AGNR). Red and Blue atoms describe sublattice A and B. (c) Band structure for ZGNR and (d) for AGNR, calculated from tight-binding model.[Adopted by (Huang et al., 2016)]

2.4b, an aGNR is depicted alongside its corresponding band structure in Fig. 2.4c. As it comes out, the distinguishing factor between the two GNRs is the configuration of their edges alongside the same axis (here axis x). This is the axis that runs parallel to the flow of electrons. Here, the band structure of the aGNR exhibits a notable difference from that of the zGNR. There is no overlap between the conduction and valence bands, indicating the existence of a bandgap (Castro Neto et al., 2009). Studies indicate that this bandgap is also related to the width of the nanoribbon. More specifically, with the increase of the zGNR width, the band-gap diminishes. For

that reason aGNRs can be characterized either as metallic or semiconducting, depending on their width (Zhang, 2022).

Zigzag graphene nanoribbons (zGNRs) can be considered favored over armchair graphene nanoribbons (aGNRs) in the context of switching devices due to their unique electronic properties that can be utilized for high-speed and efficient switching. One of those properties is the existence of localized edge states. These states contribute to the metallic behavior of the GNRs, allowing for efficient electron transport, which is advantageous for switching applications where fast and reliable switching is crucial (Kunstmann et al., 2011). Another one is the spin polarization of zGNRs along with their magnetic properties. Those features can be harnessed in spintronic devices, which employ the manipulation of spin instead of charge for information processing. This enables the development of switches that operate with reduced energy consumption and generate less heat compared to traditional charge-based devices (Shiraishi et al., 2009). An additional notable characteristic is the ability to easily tune the operation of a zGNR through band-gap engineering. zGNRs allow band-gap engineering through various methods, such as chemical doping (Liu et al., 2011), grid shape change (Jiang et al., 2018c), the application of external electric (Jiang et al., 2018c) or magnetic field (Moysidis et al., 2020) and others. These characteristics, in combination with the aforementioned high carrier mobility, make them particularly attractive for fast-switching applications with tailored electronic properties and high on/off ratios.

All these attributes make GNRs a promising alternative to traditional copper wiring in integrated circuit interconnections and pave the way for their use in creating advanced electronic components like field-effect transistors, lasers, and amplifiers.

# Chapter 3

# Modeling of Graphene Nanoribbons

## 3.1 Introduction to GNR modeling

Graphene, apart from its other properties that have been previously analyzed, has attracted a lot of interest in the field of simulation, especially when considering its application in switching and computing devices and, in general, electronics. Many methods have been utilized for its simulation and no specific standard has been established either in the scientific community or in the industry. Different types of methods are utilized for the calculation of different parameters.

In the realm of computational models, the use of the Density Functional Theory (DFT) is very common for the calculation of the energy band structure of Graphene (Nakada & Ishii, 2011). It has been also be incorporated in very well-known professional tools such as Quantum ESPRESSO (Giannozzi et al., 2017) and ABINIT (Gonze et al., 2020). The Tight Binding model is also a more simplified approach for the calculation of the electronic band structure of Graphene, providing computational efficiency, easier scalability, customization and flexibility (Bena & Montambaux, 2009). It can be found implemented in QuantumATK (Smidstrup et al., 2019). Those two are commonly combined with the Non-Equilibrium Green's function method, for very accurate quantum transport calculations. This computational method is essential for studying the conductance and electronic transport properties of nanoconductors such as Graphene (Camsari et al., 2022), and can be found also implemented in NanoTCAD ViDES (Marian et al., 2023) and QuantumATK (Smidstrup et al., 2019). Monte Carlo simulations are also commonly used to model the

transport properties of Graphene, their defect dynamics, and other phenomena where statistical variations are significant (Armour et al., 2011). Targeting different properties, the Finite Element Method (FEM), is commonly utilized for the study of bending and buckling of Graphene, as well as to investigate its vibration modes (Chandra et al., 2020). This method, as well as other continuum models, can be found in physics simulation tools such as COMSOL Multiphysics (Inc., 2024). Finally, Ab-Initio calculations can be used for the investigation of dynamic processes in GNRs, such as diffusion and chemical reactions (Mattausch & Pankratov, 2007).

Especially for the field of electronics, apart from the aforementioned computational models, there have been attempts for the realization of Compact Models. In bibliography, several types of compact models have been proposed, mainly concentrated on the estimation of the $I - V$ characteristics of Graphene FETs and Graphene Nanoribbon FETs in their different formations (Lu et al., 2017). Compact physics-based models as well as models in the form of circuit equivalents have been proposed and evaluated. The circuit approach of Umoh for dual gate Graphene FETs (Umoh et al., 2013) and the physics based approach of Jimenez (Jimenez, 2011) are two common representative models. There are also compact models targeted mainly for graphene interconnects applications such as the one proposed by Naeemi et al. and others (Naeemi & Meindl, 2009).

Compact Models are considered to be ideal for larger-scale simulations related to computing devices of higher dimensions. They are also perfect for circuit simulations, as circuits are comprised of many devices that are investigated all together in the same system. Thus, compact models through analytical equations or through equivalent circuits, can be easily imported into SPICE simulators and other standard Electronic Design Automation (EDA) tools. They offer computational efficiency, significant for the simulation of systems within a reasonable time frame. They can also sometimes be easier to parametrize, in order to represent devices of different geometries or under various operational conditions, without requiring significant interaction with the model. On the other hand, even though they fit perfectly to circuit design and system-level analysis, they do have some limitations. Usually, they cannot capture all the complex nuances of device behavior under extreme conditions or at very small scales, where quantum effects dominate, practically leading to a lack of simulation accuracy.

This is where computational models practically have the upper hand. They provide analytic atomistic and quantum mechanical insights into

GNR devices. Apart from allowing the prediction of the material´s properties, they also accurately capture quantum mechanical effects, which are essential for designing and understanding devices at the nanoscale. Additionally, they allow for easy experimentation with various geometries and materials, from bulk to atomically thin, such as Graphene. They are also capable of interpreting experimental results and matching them with corresponding phenomena, as well as for predictive modeling. All this comes with a significant cost in complexity and computational efficiency.

For that reason, in the need for accuracy, a computational method is mainly utilized in the context of this dissertation. Targeting solely to the electronic characteristics of the devices, the combination of The Tight Binding Hamiltonian (TBH), for the calculation of the band structure, with the Non Equilibrium Green's Function method (NEGF) for the calculation of the transport properties, is considered to be the most appropriate. It has been proven already to be a state-of-the-art atomistic level simulation framework that is ideal for the description of Graphene based devices (Datta, 2012). This method is going to be analytically described in the following section.

Although it is a complex computational method, appropriate for small-scale device simulations, a hybrid approach is attempted, in order for it to be able to describe the operation of larger devices. This hybrid NEGF method for larger-scale devices is fitted on experimental data through a simple mathematical interface. The fitting and comparison of the hybrid NEGF model with other common compact approaches is also presented in this chapter.

## 3.2 Atomistic Level Modeling

In general, in materials such as Graphene, it is almost impossible to analytically calculate their band structure, especially in the case where their dimensions, their length $L$ and width $W$ are considered to be infinite. However, it is possible to numerically calculate the aforementioned band structure in the case of Graphene Nanoribbon (GNR), whose length $L$ is a lot bigger compared to its width $W$, by employing the semi-empirical Tight Binding Hamiltonian method, as mentioned also in Chapter 2. After determining the energy band structure of a GNR or nanoconductor in general, the Non-Equilibrium Green's function method (NEGF) will be employed for the calculation of its conductance (Datta, 2005).

### 3.2.1 The Tight-binding model

A short qualitative analysis of the tight-binding model has been presented in Chapter 2, where its ability to describe the band structure of Graphene and predict its metallic behavior through the touching of the conduction and valence bands in the Dirac points was described. It also indicated the linear dispersion of energy near the Dirac points. Here, a more quantitative analysis will be attempted.

Graphene is a crystalline material, which exhibits periodicity in its structure. The periodically spatially arranged atoms in the crystal exert a force on the electrons, which will also be periodic and affect the behavior and especially the movement of the electrons within the solid.

This effect can be described by the Kronig-Penney model (McQuarrie, 1996), according to which the lattice atoms are described by unit impulses (Dirac delta functions). The model provides a simple quantum mechanical approach to understanding how electrons move through a periodic potential, which is a representation of the repeating atomic structure in a crystal lattice.

The essence of the Kronig-Peney model hides in its treatment of the potential energy of electrons in a crystal as a series of square potential wells, reflecting the periodic nature of the atomic arrangement. By applying the Schrödinger equation to this periodic potential, the model predicts the existence of allowed and forbidden energy bands for the electrons. These bands explain key properties of solids, such as electrical conductivity and band gaps.

We will analyze this model for a one-dimensional periodic lattice, of total length $L$, in order to make the mathematical treatment more tractable while capturing the essential physics of band formation. However, the model easily generalizes to two-dimensional lattices, such as the lattice of Graphene. (Bena & Montambaux, 2009; Karafyllidis, 2014b; Marsiglio & Pavelich, 2017; Reich et al., 2002).

Eq. 3.1 represents the fundamental one-dimensional time-independent Schrödinger equation:

$$\frac{d^2y}{dx^2} + \frac{2m}{h^2}(E - U(x))\psi \tag{3.1}$$

where, $\psi$ represents the wave function of a particle, which provides information about the quantum state of the particle, including its position, momentum, and energy, $x$ is the spatial coordinate, $m$ is the mass of the

particle (here the mass of electron), $\hbar$ is the reduced Planck's constant, $E$ is the energy of the particle and $U(x)$ is the potential energy of the particle (electron) with respect to its position.

This common second-order linear differential equation has one known solution in the form of the following wave function, presented in Eq. 3.2:

$$\psi(x) = u(x)e^{ikx} \tag{3.2}$$

where $u(x)$ s a function that has the same periodicity as the lattice and is normalized within a unit cell: $u(x) = u(x + a)$, with $a$ being the lattice constant. Also, $e^{ikx}$ represents the plane wave component, with $k$ being the wave vector that is associated with the particle's momentum.

According to Bloch's theorem, the wave function will also be periodic along the grid of a crystalline solid, e.g. $\psi(0) = \psi(L)$.

Thus, applying the aforementioned condition to the wave function of Eq. 3.2 occurs that:

$$\begin{aligned} e^{ikL} &= e^{0} \\ e^{ikL} &= 1 \\ k &= \frac{2\pi}{L}n \end{aligned} \tag{3.3}$$

where $n$ is a positive integer. The determination of the function $u(x)$ will be done within a unit cell of the graphene lattice when $U(x) = 0$. Thus, the equation 3.1, Schrödinger's equation, will conclude in the following form:

$$\frac{d^2\psi}{dx^2} + \gamma^2\psi = 0 \tag{3.4}$$

where:

$$\gamma^2 = \frac{2mE}{\hbar^2}$$

So now, by combining the Bloch wave function ( Eq. 3.2) with Eq. 3.4 the following equation (Eq. 3.5) can be derived:

$$\frac{d^2u}{dx^2} + 2ik\frac{du}{dx} + (\gamma^2 - k^2)u = 0 \tag{3.5}$$

The above equation (Eq. 3.5) is a second-order differential equation, also well-known in the field of electromagnetism, where it can describe

the behavior of electromagnetic waves as they interact with periodic structures, such as photonic crystals, distributed feedback (DFB) structures, or Bragg gratings. Here, the solution of Eq. 3.5, can have the form presented in Eq. 3.6:

$$u(x) = (A\cos(\gamma x) + B\sin(\gamma x))e^{ikx} \tag{3.6}$$

However, here, careful consideration is required. This equation is required to obey to a periodic boundary condition, in order to verify the perquisites of continuity, as well as of continuity of its first derivative. A boundary condition of that type can be described in a generic form as follows in Eq. 3.7:

$$u(0) = u(\alpha) \tag{3.7}$$

Nevertheless, in order to select the appropriate boundary condition, Schrödinger's equation needs to be integrated in a range of $[-\epsilon, \epsilon]$. This range is practically a small interval around a point where the potential is represented by a Delta function. Supposing that $x = 0$, the equation, after the integration in the aforementioned interval, will take the following form:

$$-\frac{\hbar^2}{2m}\int_{-\varepsilon}^{+\varepsilon}\frac{d^2\psi}{dx^2}dx + \int_{-\varepsilon}^{+\varepsilon} C\delta(x)\psi dx = E\int_{-\varepsilon}^{+\varepsilon}\psi dx \tag{3.8}$$

where the first term represents the kinetic energy, the second term represents the potential energy and the third term on the right-hand side represents the total energy. Integrating over a very small interval with a range of $2\epsilon$, allows for the safe assumption that the right-hand side of Eq. 3.8 remains constant and equal to $\psi(0)$. Taking this under consideration, Eq. 3.8, takes the following form:

$$\psi'(\varepsilon^+) - \psi'(\varepsilon^-) - \frac{2m}{\hbar^2}C\psi(0) = 2\varepsilon E\psi(0) \tag{3.9}$$

Nevertheless, when $\varepsilon$ has a very small value such that $\varepsilon \to 0$, then, as Eq. 3.9 implies, $2\varepsilon E\psi(0) \to 0$. Thus, Eq 3.9 will have the following form:

$$\psi'(\varepsilon^+) - \psi'(\varepsilon^-) = \frac{2mC}{\hbar^2}\psi(0) \tag{3.10}$$

This is a direct consequence of the presence of a delta function potential at $x = 0$, which induces a "jump" in the derivative of the wave function

proportional to the strength $C$ of the delta potential. The combination of Eq. 3.9 with the previously mentioned Eq. 3.6, ultimately leads to the following expression (Eq. 3.11):

$$u'(\varepsilon^+) - u'(\varepsilon^-) + ik(u(\varepsilon^-)) = \frac{2mC}{\hbar^2}u(0) \tag{3.11}$$

Thus, exploiting the periodicity mentioned above, the following substitutions can be performed: $\varepsilon^+ = 0$ and $\varepsilon^- = \alpha \sin(c\epsilon u(x))$, which finally lead to Eq. 3.12:

$$u'(0) = u'(\alpha) + \frac{2mC}{\hbar^2}u(0) \tag{3.12}$$

After all those assumptions, the combination of Eq. 3.6, Eq. 3.7 and Eq. 3.12 leads to a system of 2 equations which is comprised by Eq. 3.13:

$$A(1 - e^{ik\alpha}\cos(\gamma\alpha)) = Be^{ik\alpha}\sin(\gamma\alpha) \tag{3.13}$$

and Eq. 3.14 below:

$$\begin{aligned} &A(ike^{-ik\alpha}\cos(\gamma\alpha) + \gamma e^{-ik\alpha}\sin(\gamma\alpha) - ik - \frac{2mC}{\hbar^2}) = \\ &B(\gamma e^{ik\alpha}\cos(\gamma\alpha) - ike^{-ika}\sin(\gamma\alpha) - \gamma) \end{aligned} \tag{3.14}$$

Solving this equation system, the following results are derived, as presented in Eq. 3.15:

$$\cos k\alpha = \cos\gamma\alpha + P\frac{\sin\gamma\alpha}{\gamma\alpha} \tag{3.15}$$

where

$$P = \frac{maC}{\hbar^2}$$

The solution to the equation can be calculated numerically, or estimated through a graphical solution. In the extreme case where $P = 0$, meaning that the potential energy is equal to zero, the solution is similar to the case of a free electron inside a finite solid.

In the other extreme solution where $P \to \infty$, we have solutions of the equation 3.15, only for the cases where

$$\gamma\alpha = n\pi$$

Therefore now, the dispersion will be calculated as:

$$E = \frac{\hbar^2 k^2}{2m} = \frac{\hbar^2 \pi^2}{2m\alpha^2} n^2 \tag{3.16}$$

where $n$ is an integer number. This equation describes the energy levels of a particle in a one-dimensional quantum well or a particle confined in a "box" of width $\alpha$.

In the tight-binding model, which is used to describe electrons in a solid moving through a periodic lattice of atoms, the energy of an electron is typically expressed in terms of its ability to "hop" from one atomic site to another. The model emphasizes the discrete nature of the lattice and the localized states at each atomic site. Electrons do not move freely, rather inside a restricted space $\alpha$. Thus, it can only jump to its neighboring atoms, approximating the behavior of a nearly free electron. It can be assumed that the electron is trapped within the walls of a potential well.

### 3.2.2 Schrödinger's Equation

According to the well-known laws of the conservation of energy, the total energy of an electron can be described as follows, in Eq. 3.17:

$$E_{TOT} = E_{KIN} + E_{POT} \Rightarrow E_{TOT} = \frac{1}{2}mv^2 + V(x,t) \Rightarrow E_{TOT} = \frac{p^2}{2m} + V(x,t) \Rightarrow \tag{3.17}$$

where $E_{KIN}$ is electron's kinetic energy and $E_{POT}$ is electron's potential energy. Also, $p$ is the momentum of the electron and $m$ is its mass.

Employing Schrödinger's equation, along with the aforementioned Eq. 3.17 leads directly to the following (simplified) formulation (Eq. 3.18):

$$E\psi(x,t) = \frac{p^2}{2m}\psi(x,t) + V\psi(x,t) \tag{3.18}$$

E new, operator $H$ is then defined, which is used to describe the total energy of the under-investigation system. This operator is therefore equal to:

$$H = \frac{p^2}{2m} + V \tag{3.19}$$

Employing this new operator $H$, the Schrödinger equation can be reformed, for the special occasion of an 1-dimensional system, as presented

in Eq. 3.20:

$$i\hbar\frac{d}{dt}\psi(x,t) = -\frac{\hbar^2}{2m}\frac{d^2}{dx^2}\psi(x,t) + V(x,t)\psi(x,t) \tag{3.20}$$

From this wavefunction it can be derived that

$$H = -\frac{\hbar^2}{2m}\frac{d^2}{dx^2} + V(x,t) \tag{3.21}$$

And thus, a rewriting of the equation leads to the following:

$$i\hbar\frac{d}{dt}\psi(x,t) = H\psi(x,t) \tag{3.22}$$

Now suppose that the potential energy, $V(x)$, is time-independent, and that the temporal and spatial variation of the solution can be separated. This practically means that the initial term $\psi(x,t)$ of Eq. 3.20, can be rewritten as $\psi(x,t) = \psi(x)\zeta(t)$. Then Schrödinger's equation will be written as in Eq. 3.23:

$$\begin{aligned} i\hbar\psi(x)\frac{d}{dt}\zeta(t) &= -\frac{\hbar^2}{2m}\zeta(t)\frac{d^2}{dx^2}\psi(x) + V(x)\psi(x)\zeta(t) \Rightarrow \\ i\hbar\frac{1}{\zeta(t)}\frac{d}{dt}\zeta(t) &= -\frac{\hbar^2}{2m}\frac{1}{\psi(x)}\frac{d^2}{dx^2}\psi(x) + V(x) \end{aligned} \tag{3.23}$$

In Eq. 3.23, after the division, it can be concluded that the spatial and temporal variations have been separated. In the left-hand side of the equation, there is only temporal dependence while in the right-hand side, there is only spatial dependence. This separation allows for a focused analysis of how the electrons' spatial distribution within the graphene lattice determines its unique properties. It also simplifies the original time-dependent Schrödinger equation into components that are easier to solve. Thus, focusing only on the spatial part, it can be derived that:

$$E\psi(\chi) = \left(-\frac{\hbar^2}{2m}\frac{\theta^2}{\theta\chi^2} + V(\chi)\right)\psi(\chi) \tag{3.24}$$

Here, the new variable $\chi$ is introduced instead of the initial $x$ variable in order to denote the potential expansion to more dimensions. For example $\frac{\theta^2}{\theta\chi^2}$ can be analyzed as $\frac{\theta^2}{\theta x^2} + \frac{\theta^2}{\theta y^2}$.

Equally, Eq. 3.24 can be rewritten as:

$$E\psi(\chi) = H\psi(\chi) \tag{3.25}$$

Schrödinger equation can be rewritten in a matrix form. The resulting $H$ matrix is the Hamiltonian Matrix. Employing the tight-binding model described above to calculate the Hamiltonian, the so-called Tight-Binding Hamiltonian matrix can be obtained, which describes the energy band structure of crystalline materials, and in this specific dissertation, of a Graphene-related material.

### 3.2.3 Tight Binding Hamiltonian Matrix

Combining what is mentioned above for the tight binding model, and the Hamiltonian matrix derived from the time-independent wave function, the Tight Binding Hamiltonian can be formed. The Tight Binding Hamiltonian matrix that will be derived, is practically an analytic description, in terms of energy, of the structure of the nanoconductor that is going to be investigated. Below the formation of a Hamiltonian matrix that corresponds to an arbitrary square-shaped 2D-nanoconductor, as illustrated in Fig. 3.1, is presented.

The atoms that constitute a 2D-nanoconductor, such as the one presented in Fig. 3.1, are equidistant from each other in both the $x$ and $y$ axes, with a distance equal to $\alpha$. In the case of Graphene, $\alpha$ is the length of the strong covalent ($\sigma$) bond between carbon atoms, as mentioned in Chapter 2. Taking under consideration, for the sake of simplicity and without losing any significant accuracy, only nearest neighbor interactions, electrons can either be located at the lattice site of an atom, or jump to one of its neighboring carbon atoms. The retention energy of an electron to a lattice site is represented by $E_0$, while the hopping energy from a lattice site to a neighboring lattice site is equal to $t_0$. Due to all the atoms of the grid being the same, as well as due to the lack of any external perturbations, the hopping energy is the same for all the neighboring lattice sites. Those energies can be mapped to the potential and kinetic energy of an electron, respectively.

Suppose that the under-investigation nanoconductor consists of $p$ number of atoms in total, then the corresponding Hamiltonian matrix that will describe its structure will be a $p \times p$ square matrix. In essence, in this matrix, each one of the rows as well as each one of the columns corresponds to an atom of the nanoconductor and the values of this matrix indicate how

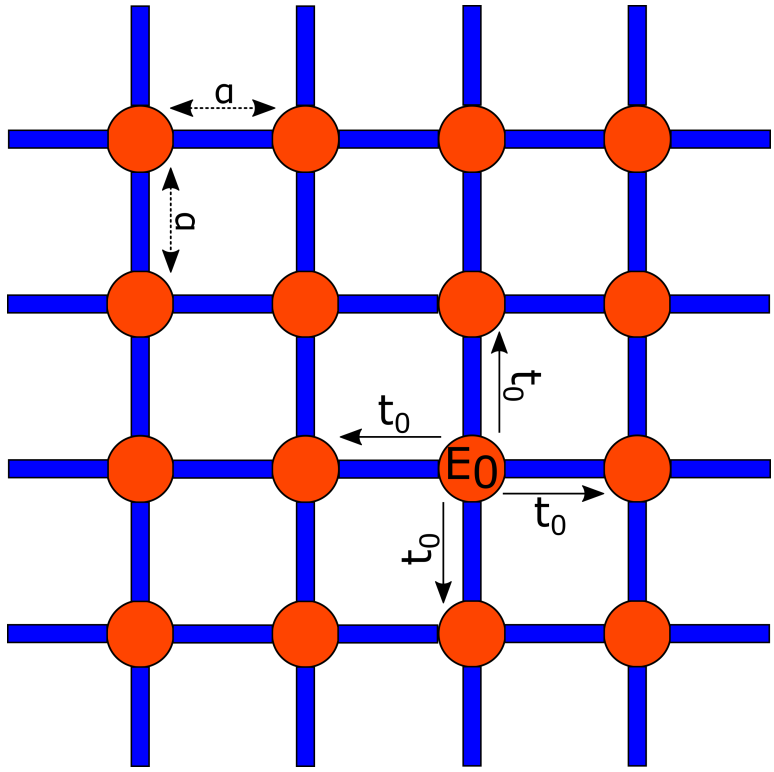
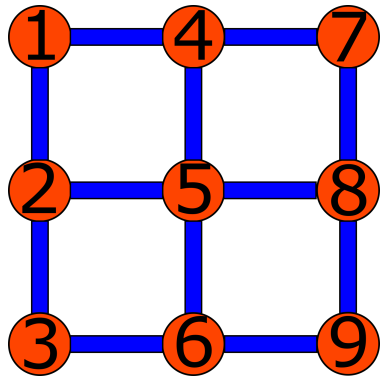



Figure 3.1: The graphene lattice in matrix form. The dots represent the atoms and the blue lines connecting the atoms represent the bonds. The length of the bond is denoted by $\alpha$. $E_0$ is the retention energy of the electron located in the specific atom site. $(t_0)$ is the transition (hopping) energy of the electron to one of the neighboring atoms

the lattice atoms are energetically related to each other. Therefore, the values in the main diagonal correspond to the retention energy, while the rest of the values of the non-diagonal elements correspond to the hopping energies from one lattice site to the other. This is the reason why there are non-zero values only in the rows and columns that correspond to neighboring atoms. This can be derived from the matrix and grid of Figure 3.2, where for example, in the first row of the matrix, the element of the main diagonal, with coordinates $[1, 1]$ has the value of the retention energy, while the hopping energy values can be seen only at positions with coordinates $[1, 2]$ and $[1, 4]$. This is verified through the structure itself, in the numbered




(a)

$$H = \begin{bmatrix} E_0 & t_0 & 0 & t_0 & 0 & 0 & 0 & 0 & 0 \\ t_0 & E_0 & t_0 & 0 & t_0 & 0 & 0 & 0 & 0 \\ 0 & t_0 & E_0 & t_0 & 0 & t_0 & 0 & 0 & 0 \\ t_0 & 0 & t_0 & E_0 & t_0 & 0 & t_0 & 0 & 0 \\ 0 & t_0 & 0 & t_0 & E_0 & t_0 & 0 & t_0 & 0 \\ 0 & 0 & t_0 & 0 & t_0 & E_0 & t_0 & 0 & t_0 \\ 0 & 0 & 0 & t_0 & 0 & t_0 & E_0 & t_0 & 0 \\ 0 & 0 & 0 & 0 & t_0 & 0 & t_0 & E_0 & t_0 \\ 0 & 0 & 0 & 0 & 0 & t_0 & 0 & t_0 & E_0 \end{bmatrix}$$

(b)

Figure 3.2: a)The numbered grid of an arbitrary nanoconductor. The numbers refer to the corresponding row and column of the Hamiltonian matrix. b) The Hamiltonian matrix that represents the structure of the nonconductor in a)

grid of Fig. 3.2a where the atom numbered as 1 ($[1,1]$ in the H matrix) is only connected to atoms 2 ($[1,2]$ and $[2,1]$ in the H matrix) and 4 ($[1,4]$ and $[4,1]$ in the H matrix), just as it can be observed in the Hamiltonian matrix of Fig. 3.3b. Only the aforementioned elements of the matrix have a value equal to the hopping energy $t_0$. The other elements have zero values, indicating no interaction. The Hamiltonian matrix is a Hermitian matrix and loosely reminds an adjacency matrix, in terms of representing connections or interactions between sites in a system.

A closer look in the Hamiltonian matrix of Fig. 3.2b, can easily lead to the deduction that it consists of two main submatrices, the submatrix A and the submatrix B, as they are presented in Fig. 3.3. Those submatrices

$$A = \begin{bmatrix} E_0 & t_0 & 0 \\ t_0 & E_0 & t_0 \\ 0 & t_0 & E_0 \end{bmatrix} \qquad B = \begin{bmatrix} t_0 & 0 & 0 \\ 0 & t_0 & 0 \\ 0 & 0 & t_0 \end{bmatrix}$$

(a) (b)

Figure 3.3: a) Submatrix $A$, which entails the description of a single column of a nanoconductor. b) Submatrix $B$ that describes the connection between two neighboring columns in the lattice of 2D-nanoconductor, like the numbered arbitrary nanoconductor illustrated in Fig. 3.2

are repeated inside the bigger Hamiltonian matrix. Practically, submatrix $A$, corresponds to a single column of the nanoconductor, while matrix $B$ expresses the hopping energy that is required to move from one column of the nanoconductor to the next. Here the term column practically resembles a one-dimensional nanoconductor. In the numbered grid of Fig. 3.2a for example there are 3 columns, comprised by the following sets of atoms: $(1,2,3), (4,5,6), (7,8,9)$.

The Hamiltonian can also be described by the following formula in Eq. 3.26 below:

$$H = -\tau \sum_{i,j} \hat{c}_i \hat{c}_j^{\dagger}, \tag{3.26}$$

where $\hat{c}_i$, $\hat{c}_j^{\dagger}$ are the annihilation and creation operators respectively, and $\tau$ is the overlap integral that has been computed to be equal to about $-3eV$ (Chico et al., 1996). The overlap integral ($\tau$) represents the interaction strength between neighboring atomic orbitals, crucial for electron hopping processes. The annihilation ($\hat{c}_i$) and creation ($\hat{c}_j^{\dagger}$) operators are fundamental quantum mechanical operators that describe the removal and addition of electrons at lattice sites, respectively. Thus, Eq. 3.26 describes the hopping process between nearest-neighbor sites in a lattice (Bena & Montambaux, 2009).

Having therefore determined the Hamiltonian matrix, the dispersion relation can be expressed as follows:

$$E(k) = E_0 + 2t_0[\cos(k_x\alpha) + \cos(k_y\alpha)] \tag{3.27}$$

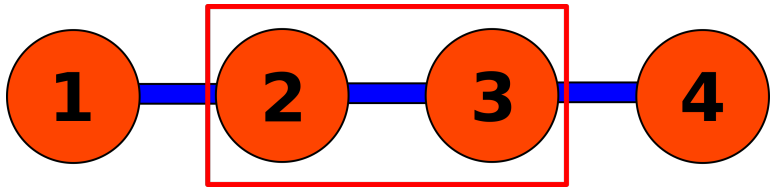
where $E_0$ and $t_0$ are the values in the matrix and are always used with their signs.

Through the TBH matrix, it is possible to move forward from the simulation of simple rectangular shape nanoconductors (in the case of this dissertation GNRs), and simulate structures of different shapes. This can be easily achieved by removing from the TBH of a rectangular nanoconductor the appropriate set of atoms that will finally give it the targeted shape.

**External electric field incorporation**

As has been explained above, the TBH matrix is responsible for providing a description of the lattice structure of the investigated material. It practically does so by providing the calculations of its energy band structure. Apart from that, the TBH matrix can be utilized for the introduction of external electric field application to the system. For example, in the simulation of a Graphene-based transistor-like device, the influence of any available top-gates or back gates will be incorporated through the TBH matrix.

Technically this will affect the main diagonal elements of the Hamiltonian matrix by changing the value of the corresponding retention energy.




(a)

$$H = \begin{bmatrix} E_0 & t & 0 & 0 \\ t & E_0 & t & 0 \\ 0 & t & E_0 & t \\ 0 & 0 & t & E_0 \end{bmatrix}$$

(b)

$$H = \begin{bmatrix} E_0 & t & 0 & 0 \\ t & E_0 + E & t & 0 \\ 0 & t & E_0 + E & t \\ 0 & 0 & t & E_0 \end{bmatrix}$$

(c)

Figure 3.4: a) A simple 1D nanoconductor that consists of only 4 atoms. b) The Hamiltonian matrix of the nanoconductor before the application of external electric field in atoms 2 and 3. c) The Hamiltonian matrix of the same nanoconductor after the application of external electric field in atoms 2 and 3.

As seen in Fig. 3.4a, supposed that there is an external electric field applied on the two marked atoms of the 1D conceptual nanoconductor. Then, the initial table of Fig. 3.4b, which corresponds to a nanoconductor with no external electric field applied, is transformed to the table of Fig. 3.4c after the application of the external electric field. This value is practically the

energy, equal to $E = qV$, where q is the charge of the electron in Coulomb and V the value of the applied voltage

### 3.2.4 The Non-Equilibrium Green's Function method

Following the calculation of the energy band structure of Graphene by employing the Tight-Binding Hamiltonian method, the calculation of the conductance of the corresponding nanoconductor is required, as well as the current density that flows through it. That will enable its use for the realization of circuits. This calculation of conductance can be achieved through the Non-Equilibrium Green's Function method (NEGF) and requires the values of the following four main parameters (Datta, 2000, 2005, 2012):

1. Green's Function
2. Density of Electrons
3. Density of States
4. Current/Conductance of the nanoconductor.

These steps will be separately and shortly described below. Using Eq. 3.18, the Schrödinger's equation can be re-written as:

$$[E - H]\psi(x,t) = 0 \tag{3.28}$$

in the case that the investigated nanoconductor is not connected to any external power source. Nevertheless, it will take the following form of Eq. 3.29:

$$[E - H]\psi(x,t) = S(x,t) \tag{3.29}$$

in the case that it is connected to some external source of power. Assuming that this external source supplies power in the form of a delta function, then Eq. 3.29 will be reshaped as follows:

$$[E - H]G(x,t_z,y,t_y) = \delta(x-y)\delta(t_x - t_y) \tag{3.30}$$

Eq. 3.30 can also be transcribed in the following matrix formation:

$$[E - H]G = I \tag{3.31}$$

where $H$ is the Hamiltonian matrix that has been described above and corresponds to the total energy of the system, including both kinetic and potential energies. $E$ is a diagonal matrix that represents the energy variable in the system and adjusts the equation for a specific energy level being considered in the analysis, and $I$ is the identity matrix.

Matrix $G$, represents Green's function of the system. It is used to describe the propagation of electrons through the system. It technically is the probability amplitude of an electron that is located in position $x$ at time $t_x$, to be trans-located to position $y$ at time $t_y$. The Green's function effectively captures the response of the system to external perturbations, such as the injection of electrons or the application of a voltage.

Solving the Eq. 3.31 above, in terms of $G$, will lead to the following Eq. 3.32:

$$G = \frac{I}{E - H \pm i\delta} \tag{3.32}$$

The term $i\delta$ is added to the equation to ensure the mathematical and physical consistency of the propagation. It solves the problems that appear in the case of $E = H$. This happens at the Dirac points, where Green's function goes to infinity. Thus, $\delta$ is selected to be a very small value that ensures the well-posedness of the Green's function. Also the sign of this term ($\pm$) determines whether the Green's function is retarded ($+i\delta$) or advanced ($-i\delta$) (Low et al., 2009; Schomerus, 2007). The Green's function is called Retarded and symbolized with $G^R$, when $t_x > t_y$ and thus the electron moves from the point $y$ to the point $x$ (the states propagate forward in time). On the other hand, Green's function is called Advanced and symbolized with $G^A$, when $t_y > t_x$ and thus the electron moves from the point $x$ to the point $y$ (the states propagate backward in time).

#### $1^{st}$ Step of the NEGF method: Calculating Green's Function

A key aspect of the NEGF approach is the conceptual partitioning of the system under study into three distinct parts: Contact 1 (or Lead 1): This refers to one of the two electrodes that are linked to the nanoconductor (or the transport region). It functions as a provider of carriers and is distinguished by its unique electronic characteristics. The contact introduces carriers into the central region under the influence of an applied voltage or other external sources (Datta, 2000, 2005).

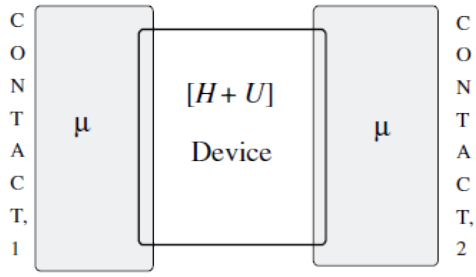



Figure 3.5: The configuration of the system which is separated into 3 individual parts: Contact 1, Main Conductor and Contact 2. [Adopted from (Datta, 2000)]

Main Conductor (or Central Region): It contains the nanostructured material or device under investigation, in the case of this dissertation, Graphene. The central region is where the potential landscape is significantly altered by external biases. It is also the area where the carriers' transmission through the device is critically determined.

Contact 2 (or Lead 2): This is the second electrode and serves as the drain for the electrons or carriers. Similar to Contact 1, it has its specific electronic properties. Carriers exit the central region into this contact, completing the transport process. This configuration is also illustrated in Fig. 3.3.

The aforementioned system is described by 3 different Hamiltonian sub-matrices, the matrix $H_1$, $H_D$, $H_2$. Those matrices correspond to Contact 1, Main Conductor and Contact 2 respectively. There are practically 3 different sub-systems, each one described by its own Hamiltonian matrix. For the transition of electrons (carriers) from one subsystem to the other, a specific amount of hoping energy $\tau$ is required. Thus, Eq. 3.32 for all three subsystems can be analytically rewritten as:

$$\begin{bmatrix} E-H_1 & -\tau_1 & 0 \\ -\tau_1^* & E-H_D & -\tau_2^* \\ 0 & -\tau_2 & E-H_2 \end{bmatrix} \begin{bmatrix} G_1 & G_{1D} & G_{12} \\ G_{D1} & G_D & G_{D2} \\ G_{21} & G_{2D} & G_2 \end{bmatrix} = \begin{bmatrix} I & 0 & 0 \\ 0 & I & 0 \\ 0 & 0 & I \end{bmatrix} \tag{3.33}$$

From all the parameters in the aforementioned description of Eq. 3.33, $G_D$ is the one that needs to be determined. This is the Green's function that describes the Main Conductor. Thus, from the notation above it is derived that (Eq. 3.34):

$$(E - H_1)G_{1D} - \tau_1 G_D = 0 \tag{3.34}$$

$$-\tau_1^* G_{1D} + (E - H_D)G_D - \tau_2^* G_{2D} = I \tag{3.35}$$

$$-\tau_2 G_D + (E - H_2)G_{2D} = 0 \tag{3.36}$$

Solving Eq. 3.34 and Eq. 3.35 with respect to $G_1D$ and $G_2D$ respectively, leads to the following, as seen in Eq. 3.37 and Eq. 3.38:

$$G_{1D} = \frac{\tau_1 G_D}{E - H_1} \tag{3.37}$$

$$G_{2D} = \frac{\tau_2 G_D}{E - H_2} \tag{3.38}$$

The employment of the two aforementioned mathematical expressions (Eq. 3.37 and Eq. 3.38) in Eq. 3.36 leads to the following result of Eq. 3.39:

$$\frac{\tau_1^* \tau_1}{E - H_1} G_D + (E - H_D)G_D - \frac{\tau_2^* \tau_2}{E - H_2} G_D = I \tag{3.39}$$

As previously mentioned, the $\tau$ terms correspond to the hopping energy from Contact 1 to Main Conductor and from the Main Conductor to Contact 2. Additionally, the terms $(E - H_1)^{-1}$ and $(E - H_2)^{-1}$, are the Green's function of the two contacts, as it can easily be derived from Eq. 3.31

For ease of notation, the two fractional terms of Eq. 3.39 can be replaced with two new variables as follows: $\Sigma_1 = \frac{\tau_1^* \tau_1}{E - H_1}$ and $\Sigma_2 = \frac{\tau_2^* \tau_2}{E - H_2}$. By replacing those two equations with the aforementioned Eq. 3.39, the final form of the equation that is used for the calculation of the Green's function will be derived as follows (Eq. 3.40):

$$G_D = [E - H_D - \Sigma_1 - \Sigma_2]^{-1} \tag{3.40}$$

The two newly created variables that are symbolized with $\Sigma$, are also called Self Energies. Each self-energy is related to a corresponding contact of the system ($\Sigma_1$ with Contact 1 and $\Sigma_2$ with Contact 2). They effectively modify the Hamiltonian of the Main Conductor region ($H_D$), to account for the coupling to the Contacts. In general, they are crucial for capturing the open boundary conditions of the system, reflecting the inflow and outflow of particles and energy due to the contacts. Through Eq. 3.40 presented above, both the retarded and the advanced Green's function can be derived as follows:

$$G^R = [E + i\eta - H - \Sigma_1 - \Sigma_2]^{-1} \tag{3.41}$$

$$G^A = [E - i\eta - H - \Sigma_1 - \Sigma_2]^{-1} \tag{3.42}$$

It is a common practice to initially calculate the retarded Green's function and then derive the advanced Green's function through the following conjugacy relation, as presented in Eq. 3.43:

$$G^{R*} = G^A \tag{3.43}$$

**$2^{nd}$ Step of the NEGF method: Calculating the Density of Electrons**

Motivated by the retarded Green's equation as shown above (Eq. 3.41) it can be written that:

$$[E - H - \Sigma_1 - \Sigma_2] = I \tag{3.44}$$

This is the response of the under-investigation system, in the case of this dissertation the Graphene Nanoribbon, to an external perturbation, a source that behaves as a Delta function. Supposed that there is another source of perturbation, source $S$, then Eq. 3.44 will be rewritten as follows:

$$[E - H - \Sigma_1 - \Sigma_2]\Psi = S \tag{3.45}$$

Which leads to the reasonable conclusion that:

$$\Psi = G^R S \tag{3.46}$$

And the conjugate of the above response at input $S$ can be described via Eq. 3.47 as:

$$\Psi^* = S^* G^{R*} \Rightarrow \Psi^* = S^* G^A \tag{3.47}$$

Having all that information, the Density of Electrons can be derived through the following calculations, as presented in Eq. 3.48:

$$\Psi\Psi^* = G^R S S^* G^A \tag{3.48}$$

In Eq. 3.48 above, this two replacements can take place: $\Psi\Psi^* = G^n$ and $SS^* = \Sigma^{in}$. Term $G^n$ resembles the Density of Electrons and is called Non-Equilibrium Green's function. Additionally, the term $\Sigma^{in}$ resembles the total power of the external sources that are applied to the system.

Ultimately, the Density of Electrons can be calculated using Eq. 3.49 below:

$$G^n = G^R \Sigma^{in} G^A \tag{3.49}$$

### $3^{rd}$ Step of the NEGF method: Calculating the Density of States (DoS)

Initially, the factors that describe this hopping of carriers from the contacts to the main conductor and vice versa have to be determined. They are called the broadening factors and symbolized by the letter $\Gamma$. Each contact has its own broadening factor. Those factors can be described by the following equations, Eq. 3.50 for the broadening factor of Contact 1 and Eq. 3.51 for the broadening factor of Contact 2:

$$\Gamma_1 = i[\Sigma_1 - \Sigma_1^*] \tag{3.50}$$

$$\Gamma_2 = i[\Sigma_2 - \Sigma_2^*] \tag{3.51}$$

Overall, the following Eq. 3.52 can be written:

$$\Gamma = \Gamma_1 + \Gamma_2 \tag{3.52}$$

Considering that an external source is applied to the 2 contacts of the investigated nanoconductor, in this case the nanoribbon, the term $\Sigma^{in}$ which reflects the total power of the applied external source can be further analyzed as below in Eq. 3.53.

$$\begin{aligned} \Sigma^{in} &= S_1 S_1^* + S_2 S_2^* \Rightarrow \\ \Sigma^{in} &= f_1 \Gamma_1 + f_2 \Gamma_2 \end{aligned} \tag{3.53}$$

where terms $f_1$ and $f_2$ represent the expressions of Fermi level in Contact 1 and Contact 2 respectively (Datta, 2000)

Having calculated all the quantities above, the density of energy states can be easily derived. In the extreme case where every legal energy state is occupied by electrons, it can be safely and reasonably assumed that the density of states is equal to the density of electrons that was previously calculated. Due to the equilibrium of the energy Fermi of the contacts with that of the nanoconductor, it can be also assumed that at the contacts, all the available legal energy states will be fully occupied by electrons too.

Based on those assumptions, and using $A$ as the symbol for the density of states, the following equity of Eq. 3.54 will be valid:

$$A = G^n \tag{3.54}$$

where $G^n$ was mentioned before as the Density of Electrons.
Due to the fact that the energy bands of the two contacts are both considered to be full of electrons, the following equity is valid:

$$f_1 = f_2 = 1 \tag{3.55}$$

The combination of the aforementioned equations (Eq. 3.49, Eq. 3.52, Eq. 3.53, Eq. 3.54 and Eq. 3.55) leads to the expression of Eq. 3.56:

$$\begin{aligned} &A = G^R(\Gamma_1 + \Gamma_2)G^A \Rightarrow \\ &A = G^R \Gamma G^A \end{aligned} \tag{3.56}$$

Finally, it can be derived that:

$$\begin{aligned} &A = G^R \Sigma^{in} G^A \Rightarrow \\ &A = G^A \Sigma G^R \Rightarrow \\ &A = i[G^R - G^A] \end{aligned} \tag{3.57}$$

#### $4^{th}$ Step of the NEGF method: Calculating the Current

The calculation of current can be approached as the calculation of the changes of the electron density $G^n$ with respect to time. For that reason, the generalized form of the time-dependent Schrödinger equation will be utilized.

$$i\hbar \frac{\theta}{\theta t}\Psi = [H + \Sigma_1 + \Sigma_2]\Psi + S \tag{3.58}$$

The employment of $\Sigma = \Sigma_1 + \Sigma_2$ leads to the following expression:

$$i\hbar \frac{\theta}{\theta t}\Psi = [H + \Sigma]\Psi + S \tag{3.59}$$

Similarly, for the conjugate response and taking under consideration that the Hamiltonian is Hermitian matrix ($H = H^*$), Eq. 3.60 can be derived:

$$-i\hbar\frac{\theta}{\theta t}\Psi^* = \Psi^*[H+\Sigma^*] + S^* \tag{3.60}$$

Now, the time derivative of the Density of Electrons $G^n$ can be calculated as follows:

$$\begin{aligned}\frac{\theta}{\theta t}G^n &= i\hbar\frac{\theta}{\theta t}(\Psi\Psi^*) = \left(i\hbar\frac{d}{dt}\Psi\right)\Psi^* + \Psi\left(i\hbar\frac{d}{dt}\Psi^*\right) = \\ &= ([H+\Sigma]\Psi + S)\Psi^* - \Psi(\Psi^*[H+\Sigma] + S^*) = \\ &= [(H+\Sigma)\Psi\Psi^* - \Psi\Psi^*(H+\Sigma^*)] + [S\Psi^* - \Psi S^*]\end{aligned} \tag{3.61}$$

Utilizing Eq. 3.49, Eq. 3.50 as well as Eq. 3.61 and also the equations $\Psi\Psi^* = G^n$ and $SS^* = \Sigma^{in}$, leads to the reformed version of Eq. 3.61 that follows:

$$\begin{aligned}&\frac{\theta}{\theta t}G^n = [H+\Sigma)G^n - G^n(H+\Sigma^*)] + [\Sigma^{in}G^A - G^R\Sigma^{in}] \Rightarrow \\ &i\hbar\frac{\theta}{\theta t}(\Psi\Psi^*) = [HG^n - G^nH] + [\Sigma G^n - G^n\Sigma^*] + [\Sigma^{in}G^A - G^R\Sigma^{in}]\end{aligned} \tag{3.62}$$

Nevertheless, for the computation of the current that flows through the conductor, only some part of $G^n$ is required. More specifically, the total electron density is a real number and can be calculated as the sum of all the elements of the main diagonal of the $G^n$ matrix. The values on the other non-diagonal elements are complex numbers that describe phase correlation. Thus, the equation of the derivative of electron density will take the following form:

$$\begin{aligned}&i\hbar\frac{\theta}{\theta t}(Trace(\Psi\Psi^*)) = Trace[HG^n - G^nH] + Trace[\Sigma G^n - G^n\Sigma^*] \\ &+ Trace[\Sigma^{in}G^A - G^R\Sigma^{in}]\end{aligned} \tag{3.63}$$

However, the term $Trace[HG^n - G^nH] = 0$ is valid because $Trace(HG^n) = Trace(G^nH)$. Thus, Eq. 3.63 can be re-written as:

$$\begin{aligned} i\hbar\frac{\theta}{\theta t} &= Trace([(\Sigma-\Sigma^*)G^n-(G^R-G^A)\Sigma^{in}]) \Rightarrow \\ \frac{\theta}{\theta t}(Trace(\Psi\Psi^*)) &= \frac{1}{\hbar}Trace[i(G^R-G^A)\Sigma in - i(\Sigma-\Sigma^*)G^n] \end{aligned} \tag{3.64}$$

However, it has already been previously reported that $A = (G^R - G^A)$ and also that $\Gamma = (\Sigma - \Sigma^*)$. Those relations, combined with Eq. 3.64 can lead to Eq. 3.65 that follows:

$$\begin{aligned} \frac{\theta}{\theta t}(Trace(\Psi\Psi^*)) &= \frac{1}{\hbar}Trace[\Sigma^{in}A-\Gamma G^n] \Rightarrow \\ I &= \frac{q}{\hbar}Trace[\Sigma^{in}A-\Gamma G^n] \end{aligned} \tag{3.65}$$

Eq. 3.65 above calculates the current per unit of energy only for a single contact. A more generalized version of this for $n$ contacts is presented below (Eq. 3.66)

$$I_k(E) = \frac{q}{\hbar}Trace[\Sigma_k^{in}A-\Gamma_k G^n] \tag{3.66}$$

where $k$ is a positive integer number: $k = 1, 2, 3, ...$

### 3.2.5 Calculating the conductance

As indicated above, Eq. 3.66 describes the current just for a single contact. Nevertheless, in a nanoconductor with contacts, the current that enters from one contact will be equal to the current that will exit from the other contact. Thus, the calculation of the current in just a single contact is sufficient. Utilizing the $2^{nd}$ and $3^{rd}$ NEGF equations, as well as the formula that connects the total energy of the system with the broadening factors and the fermi energies: $\Sigma^{in} = \Sigma_1^{in} + \Sigma_2^{in} = f_1\Gamma_1 + f_2\Gamma_2$, it can be derived that:

$$
\begin{aligned}
I_1(E) &= \frac{q}{\hbar} Trace[f_1\Gamma_1(G^R(\Gamma_1+\Gamma_2)G^A) - \Gamma_1(G^R(f_1\Gamma_1+f_2\Gamma_2)G^A)] \Rightarrow \\
I_1(E) &= \frac{q}{\hbar} Trace[f_1\Gamma_1 G^R\Gamma_1 G^A + f_1\Gamma_1 G^R\Gamma_2 G^A - \Gamma_1 G^R f_1\Gamma_1 G^A - \Gamma_1 G^R f_2\Gamma_2 G^A] \Rightarrow \\
I_1(E) &= \frac{q}{\hbar} Trace[f_1\Gamma_1 G^R\Gamma_2 G^A - f_2\Gamma_1 G^R\Gamma_2 G^A] \Rightarrow \\
I(E) &= \frac{q}{\hbar} Trace[\Gamma_1 G^R\Gamma_2 G^A](f_1 - f_2)
\end{aligned}
\tag{3.67}
$$

This is the current per unit of energy of the transported electrons, as mentioned above. Thus, for the calculation of the total current, the integration around the total complete energy range of operation, as follows:

$$
I = \frac{q}{\hbar}\int_{+\infty}^{-\infty} Trace[\Gamma_1 G^R\Gamma_2 G^A](f_1(E) - f_2(E))\, dE \tag{3.68}
$$

In fact, it is known that the electronic properties of a system are determined by the nature of the spectrum close to the last filled states, the energy of which defines the Fermi level. Therefore, the physics of graphene is determined by the nature of the energy spectrum close to the top of the valence band and to the bottom of the conduction band. It practically means, that for the calculation of current, the integration has to be at a small energy range around the Energy Fermi.

The formula in Eq. 3.68, is a practical implementation of the Landauer formula, which is used for the calculation of current and conductance in mesoscopic systems (Datta, 2005). The Landauer formula can be seen in Eq. 3.69 below:

$$
I = \frac{q}{h}\int_{+\infty}^{-\infty} G(E)(f_L(E) - f_R(E))\frac{h}{q^2}\, dE \tag{3.69}
$$

By comparing Eq. 3.68 with the Landauer formalism in Eq. 3.69, in can be derived that:

$$
G(E) = \frac{q^2}{\hbar} Trace[\Gamma_1 G^R\Gamma_2 G^A] \tag{3.70}
$$

where $G(E)$ is the conductance of the nanoconductor.

The normalized conductance is called Transmission, is symbolized with T, and can be derived from Eq. 3.70 as follows:

$$T(E) = \frac{G(E)}{q^2/\hbar} = Trace[\Gamma_1 G^R \Gamma_2 G^A] \tag{3.71}$$

### 3.2.6 Summary of the simulation framework

All in all, in the context of this dissertation, two methods are utilized for the description of the electronic properties of Graphene: the Tight Binding Hamiltonian method (TBH), which is elaborated for the calculation of the electronic band structure of the material, and the Non-Equilibrium Green's Function method (NEGF), which is used for the calculation of its transport properties.

In its matrix form, the TBH is given by:

$$H = -\tau \sum_{i,j} \hat{c}_i \hat{c}_j^\dagger, \tag{3.72}$$

where $\hat{c}_i$, $\hat{c}_j^\dagger$ are the annihilation and creation operators respectively, and $\tau$ is the overlap integral that has been computed to be equal to about $-3eV$ Chico et al., 1996. In our approach, we are taking into consideration only the first nearest neighbor interactions, meaning that we neglect every other interaction between non-direct neighboring carbon atoms. Increasing the range of atoms' effective neighborhood significantly increases computational complexity, while offering only an insignificant increase to the method's precision.

After the introduction of the GNR geometry through the TBH and electron hopping between atoms, we use the NEGF method to calculate its conductance. Briefly, NEGF method consists of 4 main equations. The $1^{st}$ step is the computation of the retarded Green's function using Eq. 3.73:

$$G^R = [EI - H - \Sigma_L - \Sigma_R]^{-1}, \tag{3.73}$$

where $E$ stands for the energy of the electrons transported through the nanoribbon and $I$ is the identity matrix, which shares the same dimensions with the tight-binding Hamiltonian $H$ (Eq. 3.72). Even though NEGF can be used for simulating devices with any number of contacts Moysidis and Karafyllidis, 2018, in this case, only two contacts are utilized. So, $\Sigma_L$ and $\Sigma_R$ are the self-energies of the left and the right contact respectively. Taking into consideration the above formulations, the advanced Green's function can be computed as: $G^A = (G^R)^\dagger$.

The $2^{nd}$ equation of the NEGF method is:

$$G^n = G^R \Sigma^{in} G^A, \tag{3.74}$$

where $G^n$ physically represents the density of electrons at a specific energy level $E$. The term $\Sigma^{in}$ practically reflects the total power of an external source (i.e. the applied potential difference between the left and right ohmic contact of a device) and is calculated by the following equation:

$$\Sigma^{in} = f_L \Gamma_L + f_R \Gamma_R. \tag{3.75}$$

Here, $f_L$ and $f_R$ denote the Fermi energy of the left and right contact, respectively. $\Gamma_L$ and $\Gamma_R$ are the broadening factors of left and right contact respectively, which are calculated as a function of the aforementioned self-energies $\Sigma_L$ and $\Sigma_R$. The broadening factors physically describe the hopping of electrons from the ohmic contacts to the main conductor.

The $3^{rd}$ equation of the NEGF method derives from Eq. 3.73 and calculates the Density of States (DoS) as follows:

$$A = i(G^R - G^A). \tag{3.76}$$

Finally, the $4^{th}$ and last equation of the method is used to compute the conductance of the system, as a function of electron energy, between the two contacts:

$$G(E) = \frac{2q^2}{h} Trace[\Gamma_L G^R \Gamma_R G^A]. \tag{3.77}$$

Which, by changing the constant variables with their values, will be reformed as:

$$G(E) = 7.7463 \cdot 10^{-5} \cdot Trace[\Gamma_L G^R \Gamma_R G^A] \tag{3.78}$$

where $7.7463 \cdot 10^{-5}$ is the conductance quantum in Siemens.

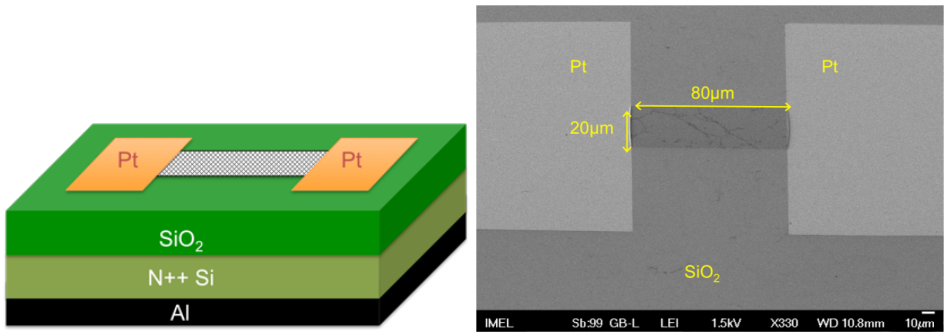
## 3.3 NEGF-based model fitting on experimental data

As presented in the previous section the use of Tight Binding Hamiltonians (TBH), for the calculation of the electronic band structure of Graphene and Graphene Nanoribbons, as well as the utilization of Non-Equilibrium Green's function method (NEGF) for the calculation of its conductance, is a very effective way for simulating GNRs and studying their electronic

properties. In fact, it has found broad adoption as a methodology by both academia and industry, as it applies not only to Graphene but also to other solid-state materials with similar properties, whose operation is governed by similar phenomena. As an atomistic-level simulation framework, NEGF provides high levels of accuracy (Datta, 2005).

Nevertheless, it is not a simple method to operate. It is a complex computational model that can become extremely resource-intensive in terms of computing resources. It is very convenient for the accurate analysis of small-scale systems, in the context of this dissertation small-scale GNRs. It can however scale up badly. For larger size GNRs, even still below the regime of hundreds of nanometers, the execution times become harsh. For a point of reference, the computational complexity of the NEGF method can commonly scale as $O(N^3)$. This can be considered as the worst case, as it can be reduced depending on the problem itself, the sparsity of its matrices and the application of several computational techniques (Zeng et al., 2013). Its complex nature distinguishes NEGF from compact models, which are designed to be simpler, faster to compute, and more suitable for integration into larger simulations where computational efficiency is a critical concern.

In the context of this dissertation, a novel hybrid approach is attempted, for NEGF-based simulations of larger devices. In that essence, simulated data for small-size GNR-based devices have been produced, which are then modified through a mathematical interface in order to resemble the behavior of larger-scale devices. This is a step towards bridging the gap between compact and computational models, leading towards the realization of a robust and flexible framework for the simulation of a wide variety of Graphene-based devices, in terms of shapes and dimensions, from the range of a few nanometers, up to the range of micrometers. For verification of the usefulness of the proposed approach, the data produced from the modified NEGF model, in terms of I-V characteristic, were fitted to experimental data from fabricated Graphene devices in collaboration with NCSR Demokritos. Those devices were in the form of bottom gate Graphene field effect transitors. A straight comparison with other types of models has been conducted.




(a) (b)

Figure 3.6: (a) Schematic of the fabricated FET device, and (b) the SEM plan view microimage of a real $80 \times 20\ \mu m^2$ FET.

### 3.3.1 Device Fabrication

A bottom gate field effect transistor was fabricated (Fig.3.6). For this purpose, a heavily doped $100mm$ (100) n-type Si wafer with a resistivity $0.003\Omega cm$ was cleaned by RCA and a $10nm$ $SiO_2$ thin layer was thermally grown on the polished front-side following a dry oxidation process in a conventional atmospheric pressure furnace. Next, a $500nm$ thick Aluminium layer was deposited by standard electron gun evaporation on the backside of the wafer, forming the future gate metal electrode. Following, a CVD single-layer of Graphene (SLG) was transferred from a Cu foil on the oxidized wafer. Details on the Graphene material and the optimized transfer method will be given in the next paragraph. In order to define the Graphene ribbons (GR), acting as channel of the FETs, we used e-beam lithography (EBL). More specifically, the wafer was spin-coated using a 7% dilution of the negative tone electron sensitive resist $ARN7520$ (ALLRESIST, 2023) and then baked the substrate at $85^{\circ}C$ in order to form a $160nm$ thick resist layer over Graphene. EBL was performed on a Vistec EBPG 5000+ tool. After development, the substrate is subjected to oxygen plasma in RIE tool so that Graphene exposed to the plasma is removed. The resist thickness of the mask suffices to protect the underlying Graphene during the etching process. Resist stripping is performed in a warm acetone bath without the use of ultrasonic agitation. Following, source/drain Pt electrodes were deposited and formed by lift-off, using polymethyl methacrylate/methyl methacrylate (PMMA/MMA) and

EBL, at the edges of Graphene stripes. This method has displayed consistency, good precision and control over the resulting critical dimensions of the ribbons, for a range of widths, from $100\mu m$ down to $20nm$. Here, we present the results from two different Graphene devices where the Graphene stripes have dimensions (width/length, W/L) 80/20 $\mu m^2$ and $110/40\mu m^2$. The final devices are shown in Fig.3.6.

### 3.3.2 Model fitting for the bottom gate Graphene FET

#### Curve Fitting

As a first approach to fitting and replicating the produced experimental data, a pure mathematical fitting/model was implemented. This is a simple, yet effective first step, in the modeling of the investigated devices. The experimental data, seem to follow an almost, but not completely, linear tendency. For that reason, the use of 2nd order polynomials of the form $f(x) = \alpha x^2 + \beta x + \gamma$, seems to be sufficient enough to describe the operation of the device and fit the provided experimental data. In the equation above, $f(x)$ is the current flowing through the device ($I_{DS}$), $x$ is the voltage ($V_{DS}$) applied on the device and $\alpha, \beta, \gamma$ are fitting parameters. In this case, the curve fitting tool of Matlab has been used for the estimation of the aforementioned fitting parameters however the use of any other fitting tool or manual fitting is possible.

For this specific case of the in-house fabricated Graphene-based devices, 7 different equations were exploited for the description of the operation of the devices under the influence of different applied back-gate potential, within a range of 0 to $-3$ Volts, as seen in Fig. 3.8a. For the cases where a different back gate voltage is applied, within the range mentioned above, linear interpolation is used for the approximation of the intermediate values.

The verification of the hypothesis that the behavior of the experimental devices may be adequately described by $2^{nd}$ order equations is presented in Table 3.1. It can be observed that the Normalized Root Mean Square Error (NRMSE), calculated as shown in (Umoh et al., 2013), remains below 0.52% for all analyzed cases. This is also visually verified through the curves of Fig. 3.8b, where the experimental values (symbols) and the simulated values (dashed lines) appear to have a nearly perfect match.

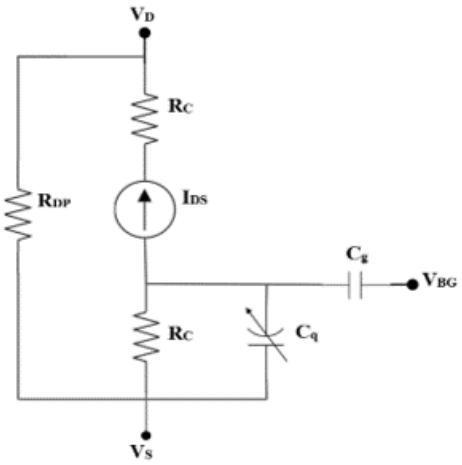



Figure 3.7: Equivalent circuit of bottom gate Graphene field effect transistor.

### Circuit Equivalent

A circuit equivalent model was also developed for single bottom gate Graphene FETs, based on the work of Umoh et al. (Umoh et al., 2013) for dual gate devices. In Umoh's work, the model simulations showed a very good agreement with published experimental data (Meric et al., 2008) and so the general idea of its proposed equivalent dual-gate circuit was kept. In order to use this model for the devices investigated here, some adjustments are necessary because of the single back gate covering the whole substrate and the uncovered layer of Graphene on the top side.

In Fig. 3.7, the equivalent circuit for our model is presented. Contact resistances $R_C$ are equal and represent the resistances of the metal contacts on the source and drain respectively. $R_{DP}$ represents the device's resistance at the Dirac Point which is attributed to residual carrier concentration. The quantum capacitance $C_q$ acts as a measure of the energy required to pump in carriers from the source into the channel, because of the different surface carrier concentration of the 2D Graphene sheet and gate, and $C_g$ represents the geometrical capacitance $C_{ox}$ between the channel and the gate. The current source $I_{DS}$ represents the current of the device, which changes depending on the applied gate and drain voltages for each region (triode, saturation, second linear regime) of the $I_{DS} - V_{DS}$ characteristics as mentioned previously

The comparison between the experimental $I_{DS} - V_{DS}$ characteristics

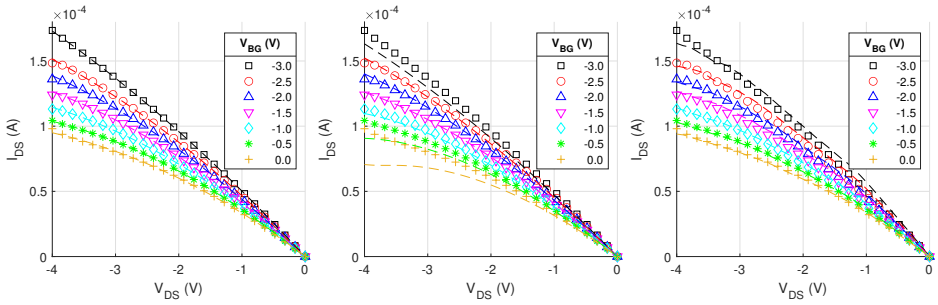



Figure 3.8: Comparison of output characteristics between simulation and experimental data. The symbols represent the experimental data and dashed lines represent the data of the model. a) Fitting of SPICE model of Section 3.3.2 to experimental data. b) Fitting of polynomial based model of Section 3.3.2 to experimental data. c) Fitting of mathematically enhanced NEGF based model of Section 3.3.2

and the modified circuit equivalent model is presented in Fig. 3.8b. The symbols represent the experimental data for the various back-gate voltages $V_{BG}$ and the dashed curves are the related output of the model. The two curves have similar behavior at linear region, but lose their agreement as they go into saturation region. This lack of agreement is observed due to the short saturation regime of the experimental devices, which is reported in most experiments (Reddy et al., 2011). This behavior cannot be represented accurately with the current models, as a constant current value is used for the saturation regime (Reddy et al., 2011; Umoh et al., 2013). Further improvement in modeling variables, mainly in the part of contact resistances, is needed in order to simulate every distinct behavior of experimental devices. Even so, as Table 3.1 clearly shows, there is a maximum NRMSE of 4.78% for all the investigated cases, except for the case where $V_{BG} = 0$. In this case the NRMSE spikes at 10.89%, something which is expected after the inspection of Fig. 3.8b. Apart from that, there seems to be a decent fit between the simulated and experimental data.

### NEGF-based Model

Another approach to device modeling and simulation, is the use of more advanced and thus complicated mathematical tools. A common tool used for nano-device simulation is the Non-Equilibrium Green's Function method (NEGF), in combination with Tight Binding Hamiltonians (TBH)

(Bena & Montambaux, 2009; Datta, 2000). It is a theoretical framework for the modeling of devices at an atomic level, especially suitable for devices whose operation is governed by quantum phenomena. The method has been extensively used in bibliography for the modeling and simulation of electron transport through Graphene-based devices, providing accurate results. It also provides flexibility in the incorporation of different features like the application of external electric and magnetic fields (Moysidis et al., 2020), the effect of the presence of different kinds of lattice defects (Rallis, Dimitrakis, et al., 2021), the effect of shape variation in Graphene grid (Jiang et al., 2018d; Rallis, Fyrigos, et al., 2023), and many others. However, a major drawback of such a numerical method is the high computational cost, which is exponentially increased with the increase of the dimensions of the investigated devices, making it very hard to be encapsulated in large-scale device simulations, or circuit simulations with many components.

A common and effective approach to merge the gap between numerical device modeling and circuit simulation is the use of hybrid NEGF-SPICE simulations (Jiang et al., 2018b; Rallis, Dimitrakopoulos, et al., 2023). The TBH-NEGF part takes into consideration the geometry and the structure of the device and calculates the conductance at several points inside the operation range. The data produced are stored in the form of a library file which is then used by a SPICE simulator. It is clear that each time there is the need for investigation of a device with new dimensions, a new library file must be created, with the use of new NEGF based simulations. This process can become extremely time and resource consuming, especially for larger-scale devices that exceed the size of a few nanometers.

Here, for the first time, a different approach on the NEGF based simulations for large scale devices is followed. The in-house fabricated devices have a width of $20nm$ and a length of $80nm$, making NEGF calculations unfeasible. For that reason, the behavior of a much smaller and easier-to-handle device with dimensions of $\sim 3.7nm \times 1nm$ was simulated. The conductance of this device was calculated under the influence of different applied potentials on its available gate, as well as on its Source and Drain contacts, within the range of operation. The values that occurred were fitted with the help of a mathematical interface that tunes their scale appropriately, in order to match the experimental device, that is of much greater size.

More specifically, as mentioned above, the values of its conductance are obtained from the NEGF calculations of the smaller device, which are later used for the calculation of the output current as follows:

| $V_{BG}$ (V) | NEGF based (%) | Circuit Equivalent (%) | Curve Fitting (%) |
|---|---|---|---|
| 0.0 | 0.95 | 10.89 | 0.52 |
| −0.5 | 0.90 | 4.92 | 0.18 |
| −1.0 | 1.09 | 1.50 | 0.30 |
| −1.5 | 2.70 | 0.20 | 0.34 |
| −2.0 | 2.04 | 0.53 | 0.31 |
| −2.5 | 2.43 | 0.67 | 0.26 |
| −3.0 | 2.72 | 3.30 | 0.05 |

Table 3.1: Normalized Root Mean Square Error (NRMSE) for all-3 investigated models, calculated for 7 different back gate applied potentials.

$$I_{DS} = V_{DS} \times \frac{G_{SM}(V_{BG_0})}{SF} \tag{3.79}$$

where $I_{DS}$ is the drain-source current, $V_{DS}$ is the drain-source voltage, $G_{SM}$ is the conductance value of the small device. The value of this conductance is selected through $V_{BG_0}$ and scaled through $SF$, which are the two fitting parameters used for adjusting the results extracted from NEGF. Those fitting parameters are calculated for the specific experimental devices through linear equations. Thus, $V_{GB_0}$ is calculated as follows:

$$V_{BG_0} = -1.064 \times V_{BG} + 1.882 \tag{3.80}$$

Also, the second fitting parameter, namely $SF$, is calculated as follows:

$$SF = 3.286 \times V_{BG} + 19.57 \tag{3.81}$$

where in both Eq. 3.80 and Eq. 3.81, $V_{BG}$ is the potential applied on the back gate of the device.

After the appropriate tuning of the NEGF method, the same comparison was conducted with the experimental values, as previously done with the use of the circuit equivalent model and the curve fitting model. As Fig. 3.8c shows, there is a very good matching of the experimental values with the simulated values, also for lower values of the applied back gate potential, where the previously presented circuit equivalent model did have mismatches. In order to provide a more clear insight on the accuracy of the mathematical NEGF-based model, the NRMSE for each separate set of curves, which correspond to a different back gate voltage ($V_{BG}$) was calculated again.

Table 3.1, clearly verifies the accurate fitting of the NEGF-based model to the experimental data. The NRMSE does not surpass the value of 3%, for none of the tested curves. As mentioned above, each approach for the modeling of the investigated devices has its pros and cons. However, by enabling NEGF to be used for the description of large-scale devices, there is now a complete, versatile modeling tool, that is able to be used for a wide range of device geometries and dimensions. For smaller-sized devices, pure TBH-NEGF atomistic level computations can be conducted providing very accurate results, while for larger devices, mathematically aided NEGF computations can provide accurate enough results while significantly reducing computational cost and time.

## 3.4 Concluding Remarks

The simulation of Graphene and Graphene Nanoribbons is not a trivial and standardized task. Several different kinds of models exist and are constantly investigated, each one owning its advantages and disadvantages and finding better match in different types of applications. For the calculation of transport properties, the Non-Equilibrium Green's Function method, which is analyzed in this chapter, in combination with Tight Binding Hamiltonians for the estimation of the band structure, is definitely one of the most frequent selections. Even though the method itself is very accurate and provides all the required insights for electronic device simulations (i.e. conductance, current), it has some serious limitations. Due to its increased complexity, it cannot be applied to larger-scale devices, as the computation time becomes very high. In this work, for the first time, a hybrid approach is attempted for the utilization of NEGF in the simulation of large-scale Graphene-based devices. Conduction data that are produced for small-scale GNR devices are adjusted in order to describe the behavior of a larger-scale device, with the aid of a mathematical interface. This model was fitted to the experimental data of a back-gate Graphene transistor, fabricated by NCSR Demokritos. The accuracy of the fitting of this model is compared with two other approaches. A fitted circuit-based equivalent, based on the work of Umoh et al. (Umoh et al., 2013) and modified for back-gated transistors, and also a simple curve fitting model that utilized 2$nd$ order polynomials. The mathematically enhanced NEGF-based model performed relatively good, with a mean NRMSE value

of 1.83% for all the investigated cases. All in all, this expansion to larger device sizes allows the use of NEGF-based simulations as a flexible and versatile tool, capable of handling a wide variety of device shapes and sizes.

# Chapter 4

# Graphene Nanoribbons with Defects

## 4.1 Introduction

Graphene, as analyzed in Chapter 2, can be fabricated with a set of different methods. The selection of the appropriate method depends on the specific allotrope of Graphene that needs to be fabricated, as well as on the targeted application. Single Layer Graphene (SLG) is formed at large areas by CVD method on Cu foils. The fabrication method makes unavoidable the presence of structural defects (Banhart et al., 2011). These are mainly attributed to the process conditions such as the growth rate (Chin et al., 2018), and the imperfections of the metallic foils (Zhang, Zhang, et al., 2016). In addition, the harsh process of the Graphene during the transfer on the desired substrate and/or device fabrication induces lattice defects (Liu et al., 2015). The SLG defects are distinguished to intrinsic and extrinsic (Tian et al., 2017), where the first term refers to structural imperfections of the honeycomb lattice, while the last one to defects due to non-carbon atoms or chemical groups attached on the SLG lattice. Experimentally, the SLG defects were investigated by Raman spectoscopy (Cançado et al., 2011) and transmission electron microscopy (TEM) (Meyer et al., 2008) regarding their structural properties and by Hall and conductivity measurements regarding their transport properties. Profound theoretical works and reviews (Lherbier et al., 2012; Liu et al., 2015) have been published on the effect of lattice defects on the transport properties of graphene, where tight-binding(Zhang, Lu, et al., 2016), ab initio and combined methods have been examined (Lherbier et al., 2012). Among the various predicted characteristics of a defective graphene lattice, which have been found experimentally and modeled successfully, is conductivity

engineering of graphene sheets by controlling the structural defects (Jafri et al., 2010). Although it is well-known that lattice defects always reduce the mobility – and hence the conductivity of graphene due to scattering effects – it has been demonstrated that defects can also improve the conductivity through the generation of carriers. In the same direction, it has been proven that the metal/graphene contact resistance is remarkably decreased when extended defects are introduced in the graphene lattice underneath the metal electrodes (Na et al., 2017; Song et al., 2014).

Obviously, defects are expected to affect severely the properties of graphene sheets as their size (mainly the width $W$) decreases and becomes the so-called graphene nanoribbon (GNR), which is the most emerging structure for graphene low power electronic devices and sensors (Chen, Sangai, et al., 2013; Harada et al., 2016). The attractive properties of GNRs arise from quantum confinement and the edge form (zigzag or armchair) of the GNR lattice. The spatial confinement leads to momentum and consequently to discrete energy bands ($\Delta E \sim 2eV/W(nm)$) and conductance quantization, while the armchair GNR can be either metallic or semiconducting depending on the size $W$ of the GNR. It has been theoretically predicted and experimentally proven that when a GNR is below $10nm$ shows semiconducting properties despite the metallic one in bulk (Li et al., 2008). Several theoretical studies on GNR defects have been published (Backes et al., 2020; Li & Lu, 2008; Mucciolo et al., 2009; Rallis et al., 2019). Recently, theoretical investigations have demonstrated that GNRs can be used to form `p-n` junctions (Nikiforidis et al., 2018), and complementary logic gates (Jiang et al., 2019a) with superior delay time compared to CMOS (Jiang et al., 2018a), as well as Multi Value Logic circuits(Rallis et al., 2018a). Furthermore, it has been predicted by simulation that depending on the shape of the GNR it is possible to create energy pseudo-gaps where conductivity is zero and thus to create a full set of logic gates by engineering the GNR shape (Moysidis et al., 2018; Moysidis et al., 2019b).

This Chapter focuses on the exploration of the effect of the most common lattice defects on the conductivity of a GNR, combining Tight-Binding Hamiltonian (TBH) with the Non-Equilibrium Green's Function (NEGF) method and the Landauer formalism for the conductivity calculation in terms of the defect location and concentration. This effective method has been analyzed in Chapter 3. The cases of the simplest possible defects, namely the single and double vacancy have been analytically examined. Those vacancies were tested in different regions and concentrations on the GNR nanodevice, like edges, main body, contacts and narrow region. The

corresponding results are presented in the form of energy dispersion diagrams, maximum conductance to number of lattice defects diagrams, as well as change of energy gap to defect density diagrams, indicating the varying defect tolerance of the butterfly shaped GNR devices. This study further investigates these lattice effects aiming to aid the design of real nanoelectronic circuits in which defects will always be present. It also provides insights into the previously unexplored field of defects on butterfly shaped devices, and generally variable shape devices, which is crucial for their viability as devices of computational circuits. The aforementioned analysis, with the addition of defect locality as a parameter, comprises a tool for a rough estimation of defect density and locality in real devices, which is obtained by only measuring the conductance of the device. The rest of this Chapter is structured as follows. In Section 4.2, the modeling methodology and the theoretical aspects of the proposed simulation are described. In Section 4.3 to 4.4.4, the simulation results on the effect on the conductivity of the defects in various regions of the GNR are presented and thoroughly discussed. Additionally, in Section 4.5 the effects of defects on some current characteristics of defective devices are also investigated. Finally, Section 4.6 summarizes the results and draws the main conclusions.

## 4.2 Modelling and Method

The calculation of conductance of a GNR was achieved, as described in Chapter 3 by combining the Tight-Binding Hamiltonian (TBH) method (Bena & Montambaux, 2009; Reich et al., 2002) and the Non-Equilibrium Green's Function (NEGF) method (Datta, 2000, 2012), which is considered to be the state of the art modeling method for atomic level modeling of nanoscale devices, and, in particular, carrier transport, which are governed by quantum mechanical effects. The combination of the two aforementioned methods allows the simulation of any possible nanoribbon shape. This Chapter investigates explicitly the butterfly shape GNR(quantum-point contact) (Karafyllidis, 2014a), that is a GNR comprising a graphene nanostripe, called hereby channel, ending at both sides to large trapezoid graphene regions, called hereby contacts, as shown in Fig. 4.1. In terms of dimensions, the device under investigation has a total length of $6.026nm$ ($30\sqrt{2}\alpha$). The width on the short region is equal to $1.562nm$ ($11\alpha$), while the maximum width of the large region is equal to $5.822nm$ ($41\alpha$), where $\alpha$ is the lattice constant equal to $0.142nm$, but the results are similar also

for higher dimension devices. The edges of the GNR were selected to have zigzag configuration. The calculations were focused on the dependence of the conductance of the described GNR structure with the presence of defects. More specifically, the conductance modification for the following cases are examined: (a) defect distribution in the channel, (b) defect distribution in the contacts, and (c) the concentration of defects in each GNR region.

The simulation method and all its steps are analytically presented in Chapter 3. Here a very short description of the main equations that comprise the simulation framework is given as a reminder. The TBH that describes the GNR structure and takes under consideration only the nearest neighbor interactions is given by:

$$H = -\tau \sum_{i,j} \hat{c}_i \hat{c}_j^{\dagger}, \tag{4.1}$$

where $\hat{c}_i$, $\hat{c}_j^{\dagger}$ are the annihilation and creation operators respectively and $\tau$ is the overlap integral that has been computed to be equal to about $-3eV$ (Chico et al., 1996).

Then, the NEGF method is employed for the calculation of the conductance. Concisely, NEGF method consists of 4 equations. The $1^{st}$ step is the computation of the retarded Green's function using Eq. 4.2:

$$G^R = [EI - H - \Sigma_L - \Sigma_R]^{-1}, \tag{4.2}$$

where $E$ stands for the energy of the electrons transported through the nanoribbon and $I$ is the identity matrix, which shares the same dimensions with the tight-binding Hamiltonian $H$ (Eq. 4.1). $\Sigma_L$ and $\Sigma_R$ are the self-energies of the left and the right contact respectively. The $2^{nd}$ equation of the NEGF method is:

$$G^n = G^R \Sigma^{in} G^A, \tag{4.3}$$

where $G^n$ represents the density of electrons and $\Sigma^{in}$ reflects the total power of an external power source.

The $3^{rd}$ equation of the NEGF method derives from Eq. 4.2 and calculates the density of states (DoS) as follows:

$$A = i(G^R - G^A). \tag{4.4}$$

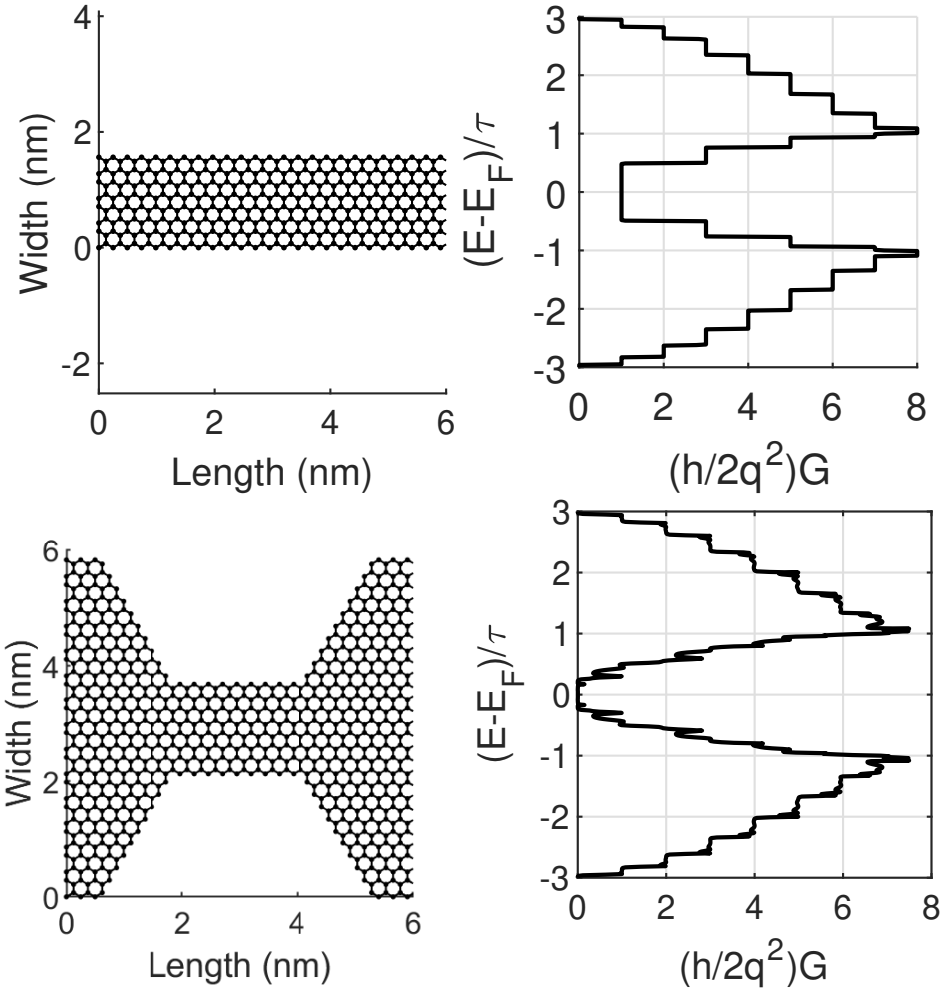



Figure 4.1: *Top row*: The lattice of a graphene nanoribbon and its conductance dispersion diagram shown on the right side of the top row. The absence of band gap is evident. *Bottom row*: A butterfly shaped GNR, the geometry of which results in a small band gap around the Fermi energy level (zero in the y-axis)

Lastly, the $4^{th}$ and final equation of the method, Eq. 4.5 is employed to calculate the system's conductance as a function of electron energy between the two contacts.

$$G(E) = \frac{2q^2}{h} Trace[\Gamma_L G^R \Gamma_R G^A]. \tag{4.5}$$

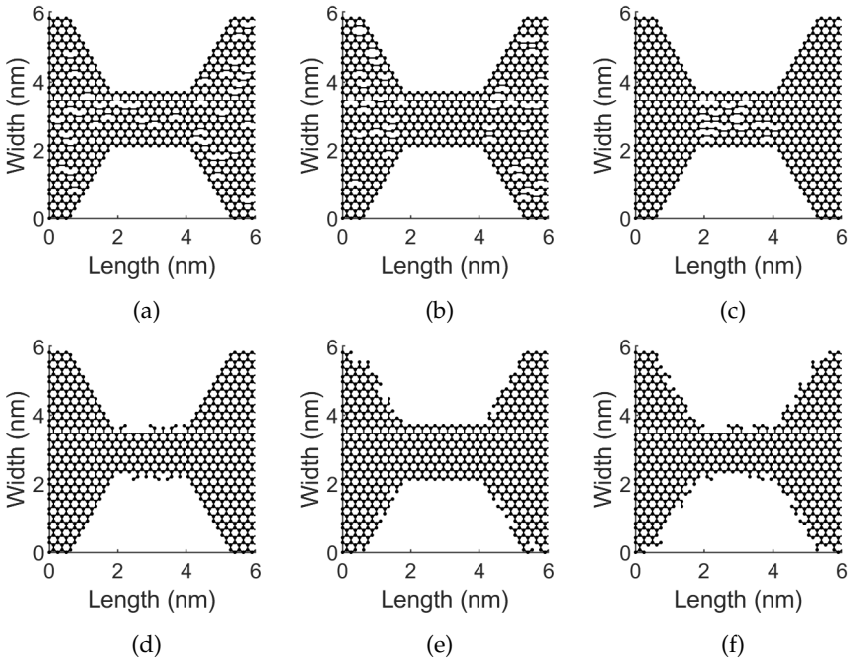



Figure 4.2: Graphene lattice with (a) Bulk defects at channel and contact regions, (b) Bulk defects only at the contact region, (c) Bulk defects only at the channel region, (d) Edge defects only at the channel region, (e) Edge defects only at the contact region, (f) Edge defects at the channel and contact region.

As mentioned before, GNRs with zigzag edge configuration have been proven to have a semi-metallic behavior instead of a much desired semi-conducting one (Nakada et al., 1996). The zero band-gap problem is therefore a great obstacle in the use of graphene nanoribbons for the realizations of new graphene based switching devices. There is a lot of research going on around the zero band-gap problem, and several solutions have been proposed, like the vertical stacking of graphene layers for the realization of bi- and multi-layer graphene (Castro Neto et al., 2009) and the growth of graphene on specific substrates(Zhou et al., 2007). Additionally, the narrowing of one of GNR's dimensions has been proposed as an effective way for realizing band-gap. Recent research has exploited that exact property for the realization of GFET like devices with the use of butterfly shaped GNRs (Karafyllidis, 2014a).

This geometry of graphene, that enables band gap engineering of GNR

based devices, has been expanded with the utilization of devices with different shaped GNRs. The proposed devices when combined together can lead to computing architectures similar to that of CMOS, but with much better performance in terms of delay (Jiang et al., 2019a). This makes such devices a very promising alternative to silicon based structures. However, the reliability, viability and practical exploitation of those, cannot be validated without an extensive analysis on their behavior when under the effect of lattice defects (Fig. 4.2).

## 4.3 Defects in GNRs

As mentioned before, defects are always present in smaller or larger Graphene lattices, as they are an inevitable outcome of the fabrication process. As stated in Chapter 2, some processes are more prone to produce defective Graphene grids, while others can produce Graphene grids with fewer defects. Based on the application requirements in terms of Graphene lattice condition, the appropriate fabrication is selected. The types of defects can be initially separated into two different categories, corrugations and structural defects. Corrugations in Graphene refer to the rippling, buckling or wrinkling of the graphene sheet. These are not necessarily defects but rather physical deformations that can occur due to various reasons. They can however affect the electronic properties of Graphene by inducing local variations in the electronic structure, potentially leading to changes in its conductivity as well as in its mechanical properties (Deng & Berry, 2016; Geringer et al., 2009; Preobrajenski et al., 2008).

Structural defects in Graphene, on the other hand, refer to imperfections in the crystalline structure of the lattice. These defects can be intrinsic (arising from the material itself) or extrinsic (caused due to the presence of foreign atoms). Extrinsic defects are also referred to as impurities (Banhart et al., 2011).

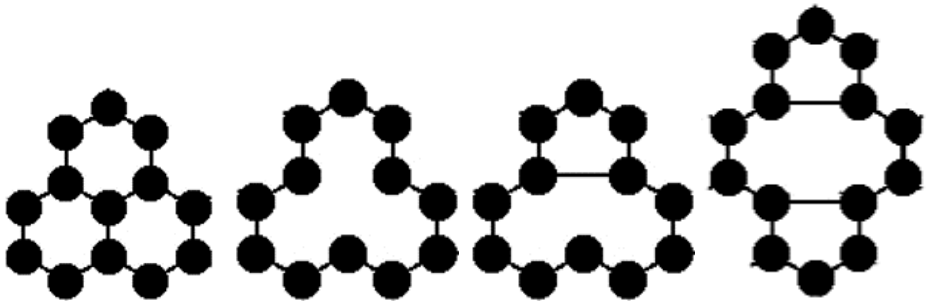
In general, there are several types of intrinsic defects, each one affecting the properties of Graphene in a different way. Among these defects, the Stone-Wales (SW) defect is distinguished by its pure reconstruction mechanism, involving neither addition or removal of atoms. This defect entails rotating a carbon-carbon bond by 90°, transforming four hexagons into two pentagons and two heptagons, which alters the lattice structure without affecting the total number of atoms or creating dangling bonds. The SW defect has a high production energy of approximately $5eV$, suggesting that

it is uncommon under normal conditions but stable when created in non-equilibrium conditions (Ma et al., 2009). Single vacancies (SV) are an essential type of defect, occurring when a lattice atom is removed, and resulting in a combination of five-membered and nine-membered rings with a formation energy of $7.5eV$ (Banhart et al., 2011). Double vacancies (DV) result from the merging of two single vacancies (SVs) or the direct elimination of two neighboring atoms. This process creates a reconstructed lattice with two pentagons and one octagon. Double vacancies have formation energies similar to single vacancies but are more thermodynamically stable due to the reduced energy per missing atom (Banhart et al., 2011). The presence of carbon adatoms is also considered to be a type of intrinsic defect (Ataca et al., 2011). The energetically prefer to be at a bridge configuration, altering local hybridization. They are highly mobile and can interact with other defects, such as vacancies, leading either to recombination or to the formation of other more complex defects, such as the inverse Stone-Wales (Lusk & Carr, 2008).

The extrinsic defects are more straightforward. They can either be foreign adatoms or substitutional impurities. As foreign adatoms are considered non-carbon atoms that are connected weakly with graphene through physisorption. They can also be connected with stronger, covalent bonds. This phenomenon is called chemisorption (Banhart, 2009). For such defects, configurations such as on top of the carbon atom, on top of the center of a hexagon, or the aforementioned bridge position are preferred. As substitutional impuritites are considered the defects that involve the replacement of one or two carbon atoms with an impurity atom. Boron and Nitrogen are two common impurity atoms, that also serve as dopants, due to their lack of one or more electrons (Lazar et al., 2014). They also have almost the same atomic radius as Carbon and do not significantly stand out from the Graphene grid. They are however located slightly off the lattice as their bonds with carbon are in general bigger compared to the carbon-carbon bonds (Krasheninnikov et al., 2009).

## 4.4 Investigated GNR defect formations

In this Section, the types of defects considered in the GNR lattice as shown in Fig. 4.3a are presented. In particular, the single vacancy (SV) in different configurations is shown, and, in more details, the standard single vacancy



(a) (b) (c) (d)

Figure 4.3: Graphene lattice with (a) no defect, (b) a single vacancy (SV), (c) a single vacancy with two available carbon atoms bonded $V1$(5-9) and (d) a double vacancy $V2$(5-8-5).

in Fig. 4.3b and, the case where a bond between two of the three available carbon atoms is formed, the corresponding single vacancy (Fig. 4.3c). These defects are described in the literature as a single vacancy $V1$(5-9) due to the appearance of two different grid structures, where one of them (the top defined in the image above) consists of 5 atoms, while the other consists of 9 atoms (Banhart et al., 2011), respectively. The formation and the migration energies of this defect are $7.4eV$ and $1.7eV$, respectively (Li et al., 2017). While the length of the normal bond between two carbon atoms is about $0.142nm$ long, the new bond that is formed between two carbon atoms after the vacancy, has a length of $r = (0.142 \times \sqrt{(3)})nm$. This different bond is introduced in the model through the tight binding overlap parameter. For the original bond of $0.142nm$, the overlap parameter has been experimentally determined to be about $-3eV$. The new overlap integral $\tau$ can be calculated by:

$$\tau_0 = -3 \times \frac{1.42}{r^2}. \tag{4.6}$$

Moreover, the expansion of this phenomenon can lead to the creation of the so-called in literature, double vacancy $V2$(5-8-5), as shown in Fig. 4.3d. This is the most thermodynamic stable configuration and the migration energy of $V2$ is $7eV$, denoting that $V2$ is almost stationary. In addition, in case of $V1$ there is always a dangling bond while in case of $V2$ there is no dangling bond, meaning that $V1$ is chemically reactive while $V2$ is not.

In this section, the investigations begin by simulating the case where

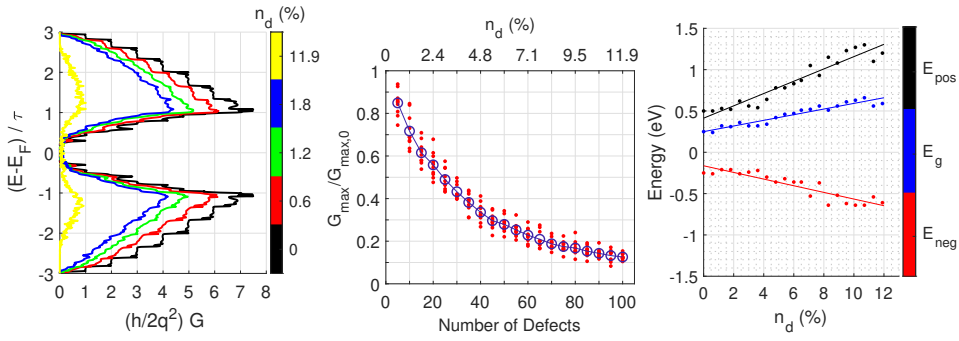



Figure 4.4: (a) Energy dispersion diagrams of the conductance calculated for different number of defects in GNR lattices shown in Fig. 4.2a. (b) The dependence of the maximum conductance of a GNR on the number of lattice defects. The average values of $G$ for each $n_d$ are varying smoothly (solid line). (c) The change of maximum energy of valence band, minimum energy of conduction band, and energy gap with the increase of bulk defect density on both contact and channel region, while straight lines are the fitting lines for every variable.

the whole GNR lattice contains defects, except for the edges. The number of defects is varied in the range of 5 to 100. The calculations were executed in an additive way, meaning that 5 more vacancies were added in a random way to the previously existing formation. This process was repeated (for 10 times) and the final results were averaged. This procedure was followed in all simulations presented in this chapter, unless otherwise specified. Such typical defective GNR lattice is shown in Fig. 4.2a.

Fig. 4.4a presents the effect of defect number on the electronic properties of the GNR utilizing conductance energy dispersion diagrams. The calculated conductance $G$ is expressed in quantum conductance units, $\frac{2q^2}{h}$ where $q$ is the elementary charge and $h$ is the Planck's constant. As previously mentioned, each diagram is an average of 10 different simulations for the same number of defects in the GNR lattice. Considering that the total number of carbon atoms in the simulated GNR are 840, then the number of defects from 5 to 100 correspond to a concentration $n_d$ in the range $0.6 - 12\%$. Obviously, the results in Fig. 4.4b reveal that $G$ is lowering as the $n_d$ increases. Moreover, the $G(E)$ curves are not symmetric with respect to the Fermi level $E_F$ (or the neutrality point) and this asymmetry becomes more evident for energies higher than the energy where maximum conductance $G_{max}$ is observed. This finding suggests that the GNR conductance is

affected in a different manner for electrons and holes. Nevertheless, the energy gap $E_g$ around the neutrality point remains constant for all examined values of $n_d$. The latter result is mainly attributed to the fact that the bulk disorder in a GNR with perfect edges does not affect the carrier transport taking place mainly from the edges. It should be here emphasized that the energy gap $E_g$ is not the same with that extracted by transport measurements, the transport gap, beyond which the conductivity of the GNR increases very fast, i.e. the change from the OFF state to the ON state. In most cases transport gap is larger due to several GNR device imperfections (Murali, 2012). Furthermore, the conductance quantization is fading and practically disappears for $n_d > 1.2\%$.

In order to investigate further the conductance degradation as a function of the defect number, the variation of $G_{max}$ at positive energies, e.g. $G_{max} = 6.1$ at $\frac{E-E_F}{\tau} = 1.1$ is examined. For the sake of comparison, $G_{max}$ is divided with $G_{max,0}$ that is the maximum conductance of the perfect GNR (see Fig. 4.1). Hereafter, the $G_{max}$ and the normalized $\frac{G_{max}}{G_{max,0}}$ will be used without any difference. In Fig. 4.4b, the dependence of $\frac{G_{max}}{G_{max,0}}$ on $n_d$ is shown. Evidently, $G_{max}$ decreases rapidly for $n_d < 3.6\%$ and more slowly for higher concentrations.

Another significant parameter that can be potentially of great importance, is the effect of lattice defects on the size of the energy gap ($E_g$). For the general case of defects on the whole bulk region of the device, including both the channel and contact regions, Fig. 4.4c shows the change of the $E_g$ with the increase of defect concentration on the grid. This figure also presents the change of $E_{pos}$ and $E_{neg}$ which correspond to the lowest energy of the conduction band and the highest energy of the valence band, respectively. Those energies are connected with the $E_g$, which can be calculated as $E_g = \left|E_{pos} - E_{neg}\right|$.

Fig. 4.4c indicates that $E_g$ broadens, while $E_{pos}$ rises and $E_{neg}$ decreases. They can be fitted finely on least squares lines whilst those straight lines have different slopes. In particular, the line that describes $E_{pos}$ has the highest slope, namely $a_{pos} = 0.0744$, the slope of $E_g$ follows a value of $a_g = 0.0342$, while $E_{neg}$ changes the least with a slope of $a_{neg} = -0.0403$. It is also obvious that $E_F$ does not have an equal distance from $E_{pos}$ and $E_{neg}$, but, in this case, it is located closer to $E_{neg}$. The presented asymmetry is visible on the energy dispersion diagrams of Fig. 4.4a. The $E_g$ increase can be reasonably explained by the symmetry breaking that creates electron scattering on the graphene surface.

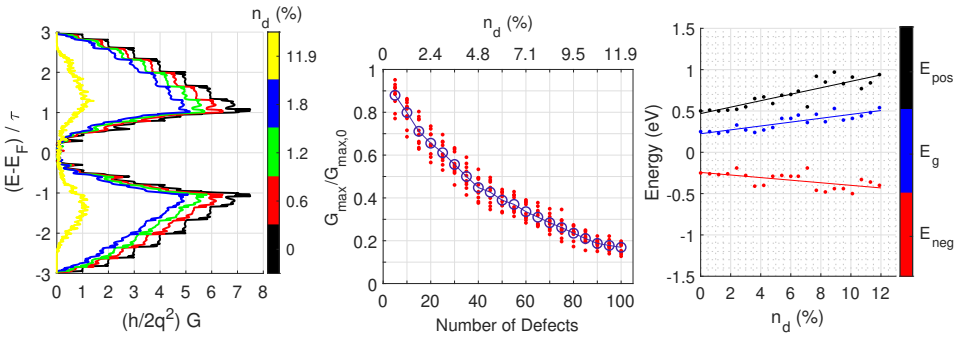



Figure 4.5: (a) Energy dispersion diagrams of the conductance calculated for different numbers of defects in GNR lattices shown in Fig. 4.2b. (b) The dependence of the maximum conductance of a GNR on the number of lattice defects on contact region. (c) The change of maximum energy of valence band, minimum energy of conduction band, and energy gap with the increase of bulk defect density on contact region, while straight lines are the fitting lines for every variable.

### 4.4.1 Defects in the wide regions

In order to separate the effect of the defects in the contacts from the defects in channel regions, further simulations were performed. More specifically, lattices were investigated where defects were located only in the contact regions and, in particular, only in the bulk region of the GNR, without affecting the edges. Such lattices, used in simulations, are shown in Fig. 4.2b.

The conductance dispersion diagrams are shown in Fig. 4.5a. In this case, those diagrams indicate a slightly different behavior of the device, in comparison with the previous general case of defects covering both channel and contact regions. Even though the conductance $G$ is always lowering as the $n_d$ increases, the ratio of this decrease is smaller. This result is in harmony with the property of GNRs maximum conductance to be affected mainly by the shortest dimension of the grid. Again, the symmetry around $E_f$ is not preserved especially for a high number of defects. A very interesting finding is that the effect on the level quantization phenomenon is far inferior in this case. Especially for energies higher than $E_f$, conductance quantization is almost perfectly preserved for $n_d \leq 1.2\%$, and also very well preserved for $n_d = 1.8\%$, and even higher defect densities.

In Fig. 4.5c, the diagram of the $E_g$ change provides similar results with

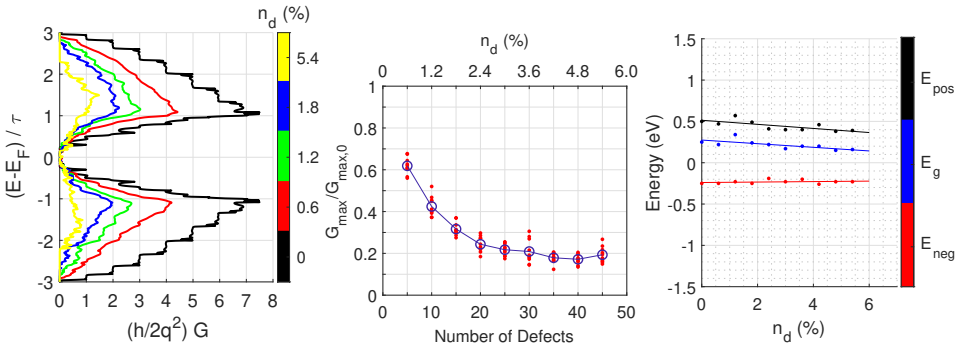



Figure 4.6: (a) Energy dispersion diagrams of the conductance calculated for different number of defects in GNR lattices shown in Fig. 4.2c. (b) The dependence of the maximum conductance of a GNR on the number of lattice defects on channel region. (c) The change of maximum energy of valence band, minimum energy of conduction band, and energy gap with the increase of bulk defect density on channel region, while straight lines are the fitting lines for every variable.

the previous case. $E_{pos}$ and $E_g$ are again increasing, while $E_{neg}$ is decreasing. $E_{pos}$ increases with a slope of $a_{pos} = 0.4684$, $E_{neg}$ decreases with a slope of $a_{neg} = -0.2437$ and $E_g$ is the variable that changes with the lowest slope of the three, $a_g = 0.2246$, but very close in terms of absolute value to the slope of $E_{pos}$.

### 4.4.2 Defects in the channel region

According to the results of the previous section, it is apparent that the defects in the channel should govern the conductance lowering in the under study GNR structure. For the purpose of deeper understanding, the effect of defects in GNR lattice only in the channel region was investigated according to Fig. 4.2c.

The related energy dispersion of the conductance is shown in Fig. 4.6a and the dependence of the maximum conductance on the increase of the defects is presented in Fig. 4.6b. The total number of defects in the channel region that was examined, was up to 5.4% of the total number of atoms in the device. Such a concentration of defects, restricted in the channel region is destructive for the device. Thus, further increase of the defect densities surely does not give any significant results.

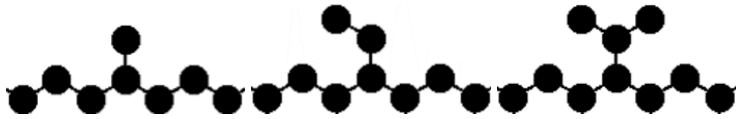



Figure 4.7: Graphene lattice with zigzag edge with three different type of defects: (a) single C atom, (b) two C atoms and (c) three C atoms.

Fig. 4.6c describes the change of $E_{pos}$, $E_g$ and $E_{neg}$ with the increase of defect densities at the edges of the device channel regions. For the first time here, an increase on the defect density leads to the decrease of the $E_{pos}$. This is accompanied by a very small increase of the $E_{neg}$ and both lead to a decrease of $E_g$, meaning practically to a smaller energy gap. In particular, the slope of $E_{pos}$ decrease is equal to $a_{pos} = -0.0247$, which is very close the slope of $E_g$ decrease, i.e. $a_g = -0.219$. The rate by which $E_{neg}$ increases is very small and equal to $a_{neg} = 0.0028$. This practically means that the line that describes the change of $E_{neg}$ is almost straight. It is also the reason why the change rates of $E_{pos}$ and $E_g$ are almost the same.

In the following Sections, the simulation results regarding the influence of the edge defects in a GNR with no bulk disorder on the conductance are presented.

### 4.4.3 Defects at the channel edges

The channel region has proven to be the most significant one, in terms of affecting the electronic properties, and, most importantly, the conductance of GNR based devices. This phenomenon is attributed to the dominant role of the smallest dimension of a nanoribbon sheet on the device's operation. The same phenomenon applies when dealing with defects concentrations only at the edges. The effect of the channel edge defects on the conductance are examined. Typical configurations of edge defects considered in our simulations are demonstrated in Fig. 4.7. Obviously, the presence of edge defects lead to a local shortening of the channel region width.

Lattices with a range of 1 to 36 defects were tested with the incremental step of the number of vacancies being 1. The selected step is smaller than the previous one because the number of atoms comprising the edges, is by far smaller. Also, due to the significant effect of the edges on electron transport properties, a more early and abrupt change on the conductance of the device is expected.

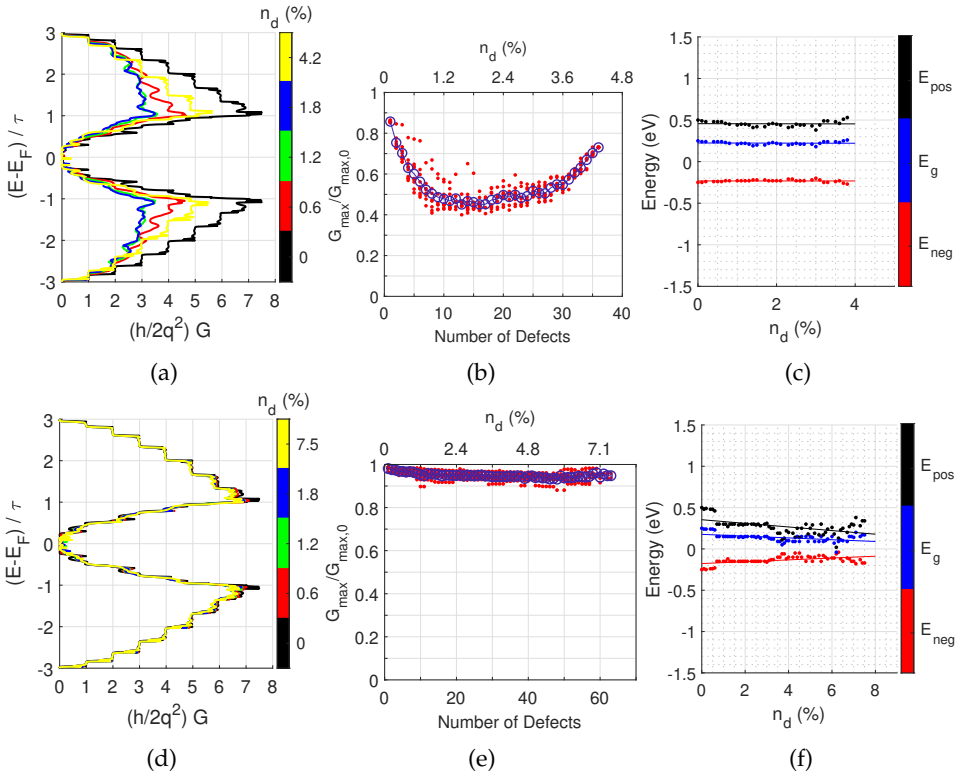



Figure 4.8: (a), (d) Energy dispersion diagrams of the conductance calculated for different number of defects in GNR lattices shown in Fig. 4.2d and Fig. 4.2e, respectively. (b), (e) The dependence of the maximum conductance of a GNR on the number of lattice defects for edge defects only at the channel region and contact region, respectively. (c), (f) The change of maximum energy of valence band, minimum energy of conduction band, and energy gap with the increase of edge defect density on channel region and contact region, respectively, while straight lines are the fitting lines for every variable.

In Fig. 4.2d, a typical grid with defective channel edges is presented. The extreme case of the two whole rows of atoms missing, one from the top and one from the bottom, is of great interest. This leads to a grid which preserves its symmetry and zig-zag shape, but has a smaller channel width, which is reduced by $(2+\sqrt{2})a$.

Fig. 4.8a shows the calculated dispersion diagram indicating the effect of defective grids on the device's operation for various numbers of defects.

It is clear that after a certain number of defects, the conductance on the device starts to increase again, in accordance with relevant results in the field (Poljak et al., 2012), until the extreme case of 36 defects was considered, where perfect shaped quantised levels reappear. This time the number of levels is smaller, due to the smaller width of the channel region, which directly affects the quantization.

The maximum conductance for the different number of defects, is presented in Fig. 4.8b, where the red dots are the values for each iteration, while the blue line and the blue circles represent the mean value of conductance for each number of defects. From the Fig. 4.8b, it is obvious that after about 18 edge defects, about half the number of defects resulting to the extreme case previously described, the maximum normalized conductance starts to increase again. So, when the zigzag edges regain their dominance, the performance of the device increases.

Fig. 4.8c presents the changes of $E_{pos}$, $E_g$ and $E_{neg}$ with the increase of defect concentration, respectively. In this case, the fitting lines are almost totally straight, and parallel with each other. More specifically, the slope for each line is $a_{pos} = -0.0007$, $a_g = -0.0008$, $a_{neg} = -0.0001$ for $E_{pos}$, $E_g$ and $E_{neg}$ in accordance. There seems to be very small connection between the energy gap and the number of defects of the channel edges of butterfly shaped GNR.

### 4.4.4 Defects at the contacts' edges

In the following simulations, only the defects on the edges of the wide regions were considered, while no new bonds after each vacancy were formed. In Fig. 4.2e, a typical case of a defective GNR lattice with defects at the contacts' edges is presented. Lattices with a range of 1 to 63 defects were tested with the incremental step of the number of vacancies being equal to 1. 10 sets of those simulation were performed. The transition from one step to another, in each set, was made in an additive way, meaning that 1 more vacancy was added to the previously existent formation.

In this case, both dispersion diagrams of Fig 4.8d and maximum conductance diagram of Fig 4.8e lead to the same conclusions. It is obvious that the edges of the contact region of the GNR play an inconsiderable role on affecting its conductance. Fig 4.8e shows that even for relatively high defect densities on the edges, namely for densities up to $n_d = 7.3\%$, the dispersion diagrams are only slightly affected, and even the quantization

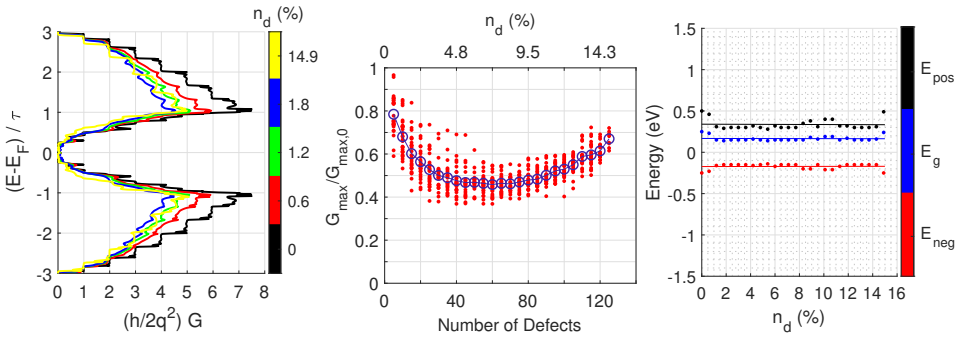



Figure 4.9: (a) Energy dispersion diagrams of the conductance calculated for different number of defects in GNR lattices shown in Fig. 4.2f. (b) The dependence of the maximum conductance of a GNR on the number of lattice defects on both channel and contact regions. (c) The change of maximum energy of valence band, minimum energy of conduction band, and energy gap with the increase of edge defect density on both channel and contact regions, while straight lines are the fitting lines for every variable.

levels remain almost totally unspoiled. Also, Fig 4.8d shows with a better resolution that the performance of the device in terms of maximum conductance practically remains intact. The maximum conductance of a defective GNR drops only by 6.81% in comparison with the ideal GNR.

Fig. 4.8f describes the correlation between the values of $E_{pos}$, $E_g$ and $E_{neg}$ and the number of defects on edges of the contacts of a butterfly shaped GNR. In this case, there is a strong tendency of the $E_{pos}$ and $E_g$ to decrease. On the other hand, $E_{neg}$ increases. The fitting lines for $E_{pos}$, $E_g$ and $E_{neg}$ change with a slope of $a_{pos} = -0.0219$, $a_g = -0.0108$ and $a_{neg} = 0.0111$ respectively. Here it can be observed that although for defect densities lower than 3%, the fitting lines seem to be in accordance with the change of the values, for $n_d > 3$ the fitting is not so accurate. However, it is clear, that $E_g$ is getting smaller with the increase of defect densities.

### 4.4.5 Defects at the GNR edges

As a final test case, devices that have defects on their edges, both on the wide contact and also on the short channel region were simulated, in order to examine the effect of edge defects on the device properties as a whole.

In Fig. 4.2f an instance of the defective grid is presented; it is basically a combination of the grids shown in Fig 4.2d and Fig 4.2e.

This time grids with a range of 5 to 125 defects were examined. Each time the number of defects was increased by at least 5 more. In Fig. 4.9a, like in the previous cases, the initial energy dispersion diagrams can be observed.

In Fig. 4.9c the effect of edge defects on both the channel and the contact region together on the values of $E_{pos}$, $E_g$ and $E_{neg}$ is tested. Except from a small number of outliers, the values of the energies with the increase of defect densities seem to fit very well on almost straight lines. More precise, the values change with a slope of $a_{pos} = -0.0004$ $a_g = -0.0002$ and $a_{neg} = -0.0002$ for $E_{pos}$, $E_g$ and $E_{neg}$ respectively. For up to $n_d = 15\%$ defective grid, where the defects are located only on the edges of a butterfly based device, the energy gap seems to be unaffected.

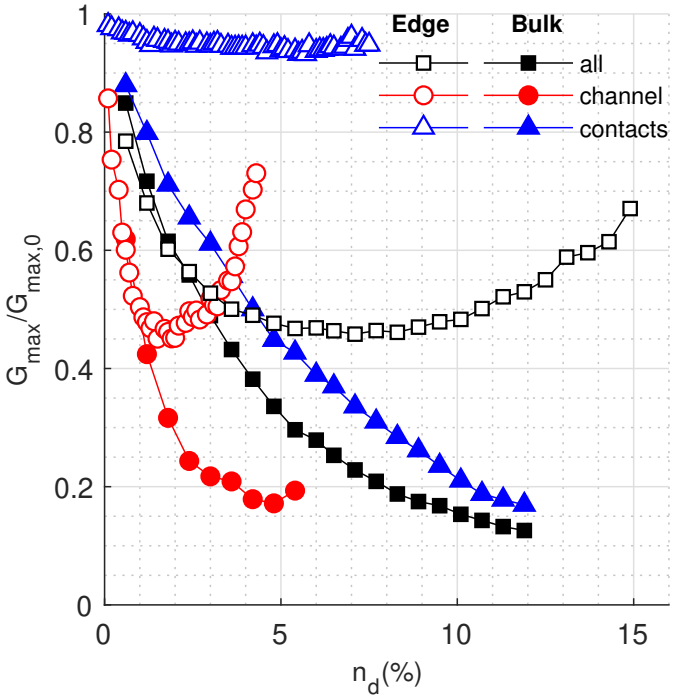



Figure 4.10: Overall comparison of the change of conductance with the increase of defect density, for every case described above.

Fig. 4.10 is a general comparison of the maximum conductance of a defective device, for every case that has been already presented in this Chapter. The first observation that can be made is that there is a very similar behavior between the cases of bulk channel defects and the bulk defects on the whole area of the device. This showcases the impact of the contacts as the dominant, which is mainly credited to the higher number of atoms that is included in the contact regions, in comparison with the amount of atoms at the channel. The maximum difference between those cases in terms of maximum conductance can be seen for defect concentrations of defects around $n_d = 5.5\%$, which is the same value where a device with bulk channel-only defects reaches its minimum value. Even though bulk channel defects lead rapidly the device to a minimum value of maximum conductance, all the cases of bulk defects end up almost to the same value of conductance, which is about 80% smaller than the initial of the perfect device.

In the cases of edge defects, the results are different. More specific, in the case of edge contact defects, the impact on the devices' maximum conductance is insignificant. This is the only case where defects do not affect significantly the operation of the device. The devices with channel edge defects as well as those combining both contact and channel edge defects develop a behavior that was not present before. The minimum value of maximum conductance is obtained when half of the targeted edge atoms are missing. This value is considerably higher in comparison with the values that occur at the cases of bulk defects, but is achieved for very low defect concentrations, namely about $n_d = 2 - 4\%$. This time the performance is reduced only by 55%. A further increase of the defects leads to an improved performance which reaches up to 68% and 74% of the initial performance, for edge defects on both channel and contacts, and only on the channel region, respectively. This maximum value after removing two layers of edge atoms is mainly determined by the new width of the channel region.

## 4.5 Current Characteristics of Graphene Nanoribbons

As an extension to the aforementioned investigation, for the same set of defective devices, their performance is evaluated using metrics that are related more to their operation as circuit components. Of course, the results produced here are correlated with the results of the previous sections, as

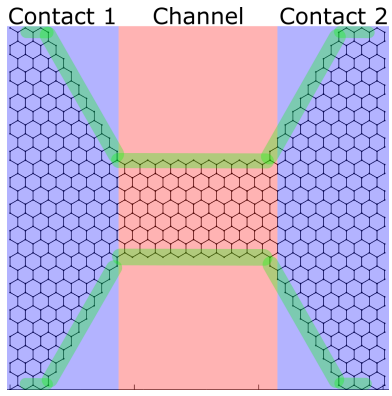



Figure 4.11: GQPC grid's with marked regions. Blue color marks the contacts region, red color marks the channel region and green color marks the edges.

most of the measured quantities are loosely or strongly related For every separate simulation case, three (3) different metrics are examined, and thus three (3) corresponding but different graphs are produced. The first is the current density to the number of defects. The current density that is calculated here practically is the current flowing through the device at $0.5V$, divided by the number of defects, thus, its unit of measurement is $A$ / $N_o$ of defects ($J$). The second is the leakage current; more specifically, as the examined device is a simple volatile current switch, the leakage current is considered to be the current that flows through it when it is set at Low Conductance mode. The operation voltage which is selected for the device and thus for the calculation of the leakage current is $0.5Volts$. This value is selected based on the operating voltage of GNR gates on Moysidis et al., 2018. Finally, another significant parameter taken under consideration, decisive for the successful operation of a switch, is the $I_{ON}/I_{OFF}$ ratio. The $I_{OFF}$ is considered to be the aforementioned leakage current, and the $I_{ON}$ the current flowing at $0.5V$, when the device is set to High Conductance mode.

### 4.5.1 Bulk Defects at GNRs

Initially, the investigation concentrated on the simulation of defects that were induced only in the bulk area of a GNR. In particular, the term bulk, again, refers to all those atoms of the GNR that do not belong to the edge,

i.e. to the outer (top or bottom) row of the GNR's atoms, or as clearly previewed in Fig. 4.11, the green color marked area.

Following the area device separation that has been thoroughly presented in Section 4.4, as a first step defects of different densities in the two trapezoidal regions, namely the contacts, are applied (see Fig. 4.11. The produced results are presented in Fig. 4.12a, 4.12b, and 4.12c, respectively. The leakage current in Fig. 4.12b seems to be randomly affected by the defects and to not follow a specific tendency. Notwithstanding, due to the fact that the leakage current seems to have a mean value of around $2.5 \times 10^{-6} A$, the current density in Fig. 4.12a seems to be minimized after almost thirty five $(35)$ defects to just $0.5 \times 10^{-7} A/defect$. This is a clear statement that leakage current remains practically intact to the increase of defects for up to $n_d = 12\%$ concentration. The $I_{ON}/I_{OFF}$ ratio, has an almost linear tendency and decreases from 120 to 10. Considering that the leakage current has a steady mean value, this means that the maximum conductance of device is almost linearly decreasing with the increase of defects, especially after the first fifteen $(15)$ vacancies $n_d = 1.2\%$.

After the examination of the contacts region, the next step is the introduction of increased defect densities at the bulk of the channel area of a butterfly-shaped GNR device (as seen in Fig. 4.11). In this area, there are also some similarities with the previous one. Fig. 4.12d shows an abrupt decrease of the current density, which caps to the lowest value of $2 \times 10^{-8}$ $A$ for only fifteen $(15)$ defects (around $n_d = 1.8\%$). This is almost identical to the previously reported behavior, indicating, however, that the channel drastically affects the operation of the device. The leakage current is again variable and seems to have a median value of around $1 \times 10^{-6} A$. Like the contacts' case, this time again the `ON/OFF` ratio of the device linearly decreases with the increase of defects, implying a linear decrease of the maximum conductance of the device.

The last case of examining the defects in the bulk of a GNR device, involves the simultaneous appearance of defect concentrations both at the contacts and at the channel. This case as shown in graphs seems to be a superposition of the previous two. At around twenty five $(25)$ to thirty $(30)$ defects, the current density reaches a minimum value, while the leakage current seems to have a mean value of $2 \times 10^{-6} A$. Again the `ON/OFF` ratio decreases linearly, in a very similar manner with that of the first case shown in Fig. 4.12c.

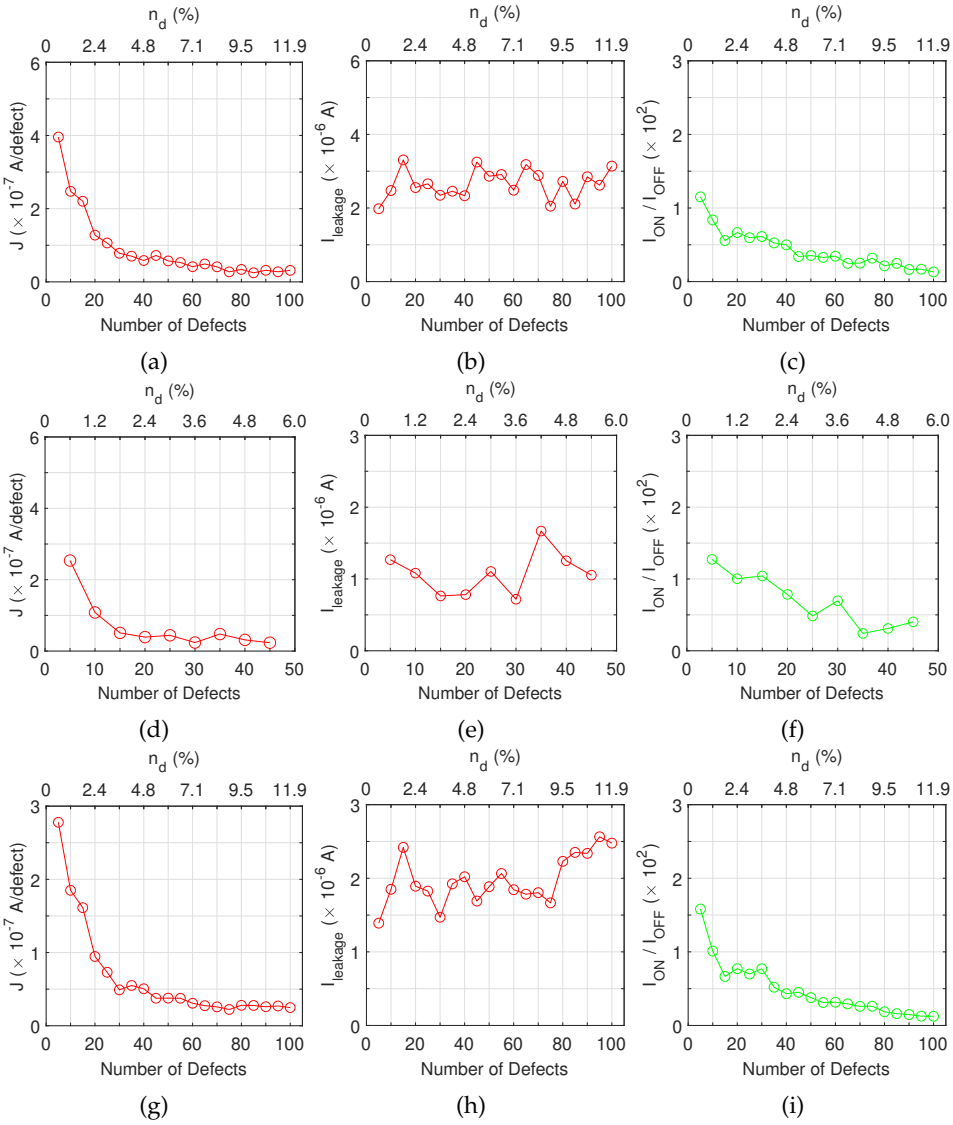



Figure 4.12: (a), (d), (g) Current density diagrams at $0.5V$ (leakage current) calculated for different defect concentrations in the bulk of contacts, channel and both channel and contact, respectively. (b), (e) (h) The change of leakage current (at $0.5V$) on the number of lattice defects in the bulk of contacts, channel and both channel and contacts, respectively. (c), (f), (i) $I_{ON}/I_{OFF}$ ratio to the number of defects in the bulk of contacts, channel and both channel and contacts regions, respectively.

### 4.5.2 Edge Defects at GNRs

In this Section, the simulations of defects are concentrated on the edges of the GNR devices. Only the outer rows on the top side and the bottom side are affected by vacancies, while the bulk of the device remains intact. Referring to Fig. 4.11, the edges are marked with green color. In the same manner with the previous simulations, initially, the effect of edge defects at the contacts region is examined. This time, the behavior of the device is more interesting. The leakage current which is presented in Fig. 4.13b slightly increases, with a small ratio until a vacancy concentration of $n_d =$ 3.6%. After that threshold, it remains practically steady, and as the defect density increases up to $n_d = 7\%$, it starts to reduce, until reaching its initial value. This is also reflected on the current density graph of Fig. 4.13a. The ON/OFF ratio of Fig. 4.13c also develops a local minimum at a $n_d =$ 3.6% defective grid and after hitting a plateau, abruptly increases to almost initial values.

Similar behavior also is depicted in the second row of Fig. 4.13, which corresponds to devices with defective edges of their channel. In this case, however, the mean value of leakage current remains almost constant, and reaches levels of almost an order of magnitude lower than at the case of edge defective contacts. The ON/OFF ratio also increases slowly and abruptly spikes up to an order of magnitude higher value, at a defect density of $n_d = 4.2\%$.

Finally, the last case refers to defects distributed in the edges of both contacts and channel with rather similar behavior. The analysis of defective edge behavior verifies the significance of edge states and symmetry to the behavior of GNRs. This peculiar performance boost after a specific value of defect concentration is attributed to the fact that the outer rows are severely damaged, and the rows just below them begin to act as the new edges. Thus, the behavior of the device is gradually led to the behavior of a pristine Graphene butterfly-shaped Device device with a narrower width.

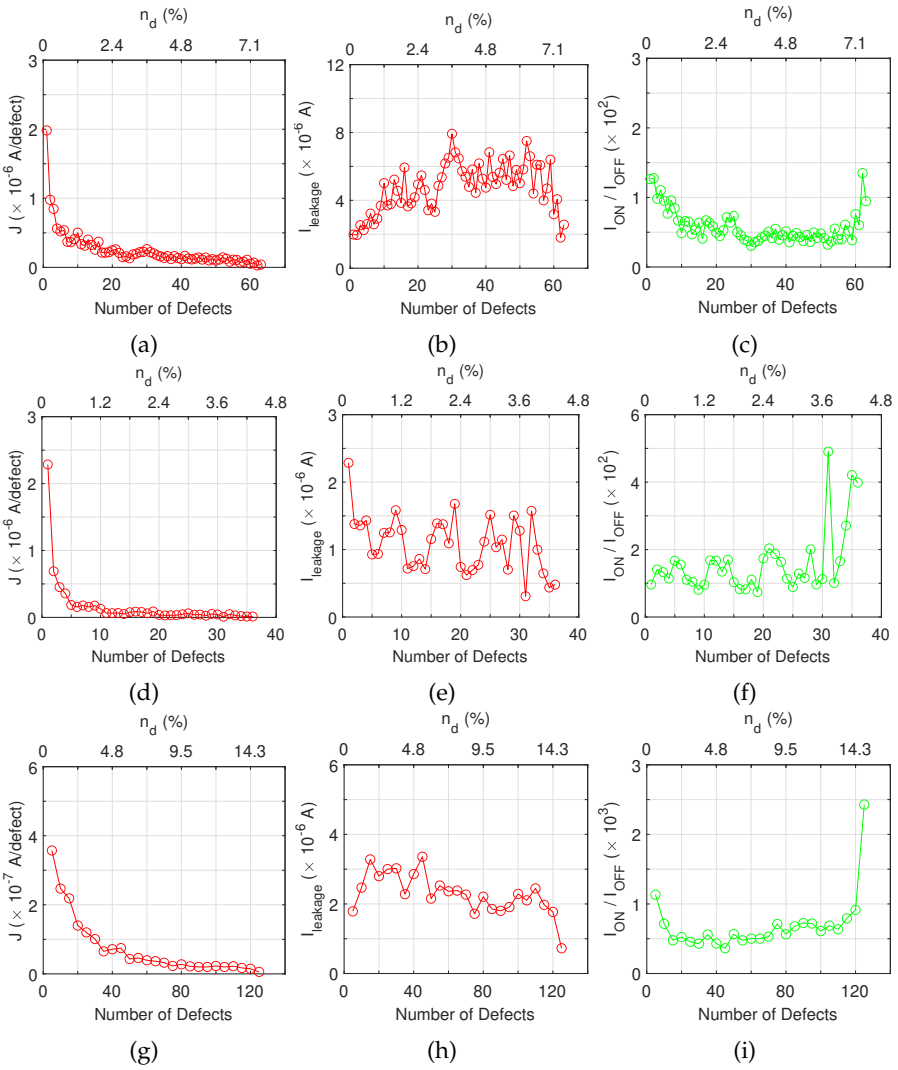



Figure 4.13: (a), (d), (g) Current density diagrams at $0.5V$ (leakage current) calculated for different defect concentrations in the edges of contacts, channel and both channel and contact, respectively. (b), (e) (h) The change of leakage current (at $0.5V$) on the number of lattice defects in the edges of contacts, channel and both channel and contacts, respectively. (c), (f), (i) $I_{ON}/I_{OFF}$ ratio to the number of defects in the edges of contacts, channel and both channel and contacts regions respectively.

## 4.6 Conclusions

In this chapter, the operation of butterfly-shaped, GNR based devices, under non-ideal conditions has been investigated. In particular, the effect of defects on the electronic properties of the devices was examined. Defects on specific parts of the device were considered for each different simulation, in order to find out which part of the device is more defect-tolerant. Investigation was also conducted on whether different parts of the device affect its properties in different ways. For the simulations presented, the very accurate NEGF combined with TBH was used, which was expanded and enhanced with the capability of including different kinds of defects. The most significant variables that define the device switching capabilities were tested, namely the maximum conductance, the energy gap and also the conductance of the device at different energies.

The presented results indicate that lattice defects affect significantly the electronic properties of the devices. In general, the channel region appears to be more severely affected by defects than the contact region. Both edge and bulk channel defects reduce the maximum conductance to very low values. The shape and symmetry of the edges play a very significant role in this phenomenon. In the cases where channel edge defects are included, the maximum conductance increases, when perfect zig-zag becomes dominant again. The energy quantization property that is present on an ideal defect-free grid, vanishes for very small defect concentrations, in almost every sub-location of the device, except from the edge defects on the contacts. Another significant variable, the energy gap, changes with the increase of defects. Bulk defects at the contacts induce an increase in the device's energy gap, while edge and channel defects either decrease the gap, creating problems on device's operation, or do not affect it at all.

Finally, further simulations revealed that the leakage current and the ON/OFF current ratio are modulated by defect concentration. More specifically, the edge defects contribute significantly to the leakage current increase nearly on order of magnitude. On the contrary, the channel defects do not cause a remarkable increase in leakage current. Also, as a figure-of-merit, the current per defect is introduced.

# Chapter 5

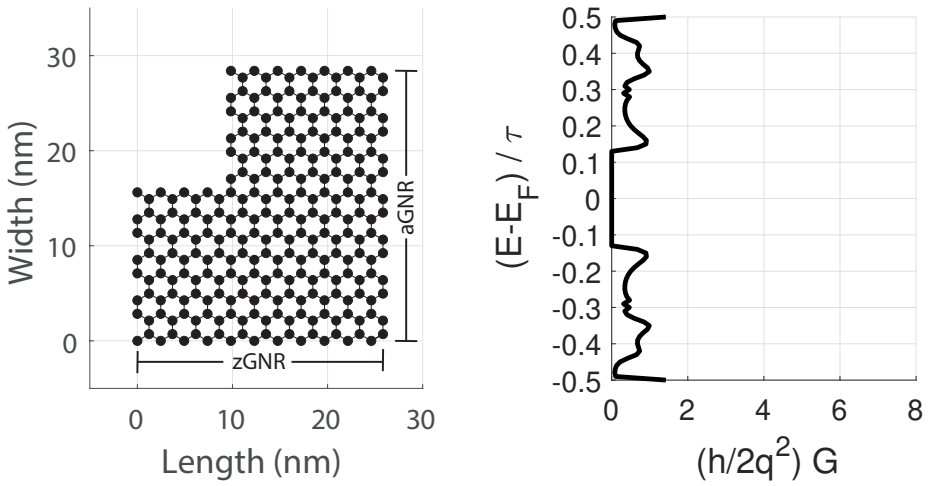
# Graphene Nanoribbon based Circuits

## 5.1 Introduction

In extension of the prior work on the field of Graphene Nanoribbon based devices and the effect of their defects on their electronic properties presented in Chapter 4, the focus of this dissertation shifts to the field of electronic circuits.

In fact, the field of electronics is one of the areas in which Graphene is considered to be able to stand out and play a significant role. As analyzed in Chapter 2, this is due to a set of very attractive properties that it entails. Briefly, the combination of its spectacular electronic properties, such as its high electrical conductivity and ballistic transport, with other properties such as its thermal conductivity, optical conductivity, flexibility, and even biocompatibility, among others, make it an ideal candidate to drive the field of future conventional and unconventional electronics, with broad applications in a wide set of scientific fields.

Especially in the form of Graphene Nanoribbons, which apart from inheriting the special properties of Graphene, are also very convenient due to their very small size in the regime of nanometers, Graphene has been utilized in several types of switching devices that are suitable for the realization of computing circuits. Several different types of Graphene Field-Effect Transistors (GFETs) and similar to them devices, have been already presented both in theoretical and experimental forms (Schwierz, 2010). Also, GNR-based devices have been proposed for the implementation of devices with hysteresis, that can be used in Neural Network (NN) accelerators, in the form of synapses or neurons. (Wang, Laurenciu, & Cotofana, 2021; Wang, Laurenciu, Jiang, & Cotofana, 2021; Wang et al., 2019).




(a) (b)

Figure 5.1: (a) The lattice of an L-shaped GNR and (b) its energy dispersion to the normalized conductance diagram. The realization of a band gap is evident.

All of the aforementioned examples of GNR-based devices, that can effectively operate as switches, have managed to overcome the basic obstacle in the incorporation of Graphene and also Graphene Nanoribbons in electronics. This problem is the well-known absence of bandgap, which is a straight outcome of the energy band structure of the material as described in Chapter 2. However, in order for this problem to be surpassed and induce bandgap to Graphene, many different methods have been employed. Among those methods, some of the most well-known and widely used are: the application of external electric bias (Jiang et al., 2019b) or magnetic bias (Moysidis et al., 2020), the stacking and twisting of Graphene (Nimbalkar & Kim, 2020), as well the Graphene shape modulation (Jiang et al., 2018c; Karafyllidis, 2014a). This last method specifically, can be simply referred to as the topology awareness of Graphene and has been exploited in many different ways. While each approach has its advantages and disadvantages, the question remains: what is the most effective way to modulate the conductance of a GNR device, induce a bandgap, and preserve its properties for usage in different applications?

In this chapter, the aforementioned property, the topology awareness of Graphene is leveraged in order to create a device that is able to operate as a switch, without the demand of a back-gate terminal. This switch

is then used as a basic cell for the composition of a single topology that owns the property of re-programmability, in an attempt to expand the use of Graphene, especially GNRs, in the field of re-configurable computing, in a different way compared to what has been previously proposed (Moura et al., 2018; Nakaharai et al., 2014; Ramos-Silva et al., 2021). More specifically, the L-shaped GNRs are used as the basic building blocks, as they have been proven to be able to operate satisfactorily enough as switches (Moysidis & Karafyllidis, 2018). In Section 5.2, for the first time, a design space exploration on the devices is conducted and the effects of their geometrical and structural characteristics on their electronic characteristics are investigated. The simulation method for the investigated devices is briefly exposed in Section 5.3. Section 5.4 presents two novel re-programmable comb-shaped devices. With effective programming through biasing the first of them can operate as an `AND` gate, an `OR` gate, an `NOT` gate or a `Buffer`, while the second can operate as 2-input `XOR`, 3-input `XOR` or `Majority` gate. In this same section, the first circuit consisting purely of comb-shaped topologies is presented. It is a full adder unit, which is comprised of a `XOR` gate and a `Majority` gate and whose operation is verified through SPICE simulations, again, for the first time for that type of devices. In addition to the presentation of the topologies, the investigations are extended by including some significant metrics considering computing devices, which are the area, delay, and power, in comparison with state-of-the-art CMOS circuits, as well as another state-of-the-art low-power complementary GFET-based architecture (Jiang et al., 2019b) in Section 5.4.3. Section 5.5 presents a butterfly-shaped Graphene Quantum Point Contact device (G-QPC) that can encode the digits of the radix-4 numeral system. Using this device as a building block, the circuit of a radix-4 adder is presented, opening the way for its employment in Multi Valued Logic applications. Finally, in Section 5.6, the conclusions of the chapter are drawn.

## 5.2 L-Shaped Graphene Nanoribbons

As mentioned again in Chapter 2, GNRs can be boldly clustered into two main categories based on the orientation of their edges, the zig-zag edged GNRs (zGNRs) and the armchair GNRs (aGNRs) (Nakada et al., 1996) which plays a very significant role in their electronic behavior. In their simplest zig-zag-edged form, they reportedly present no bandgap, which is a prohibitive feature for nano switches. In this approach, the

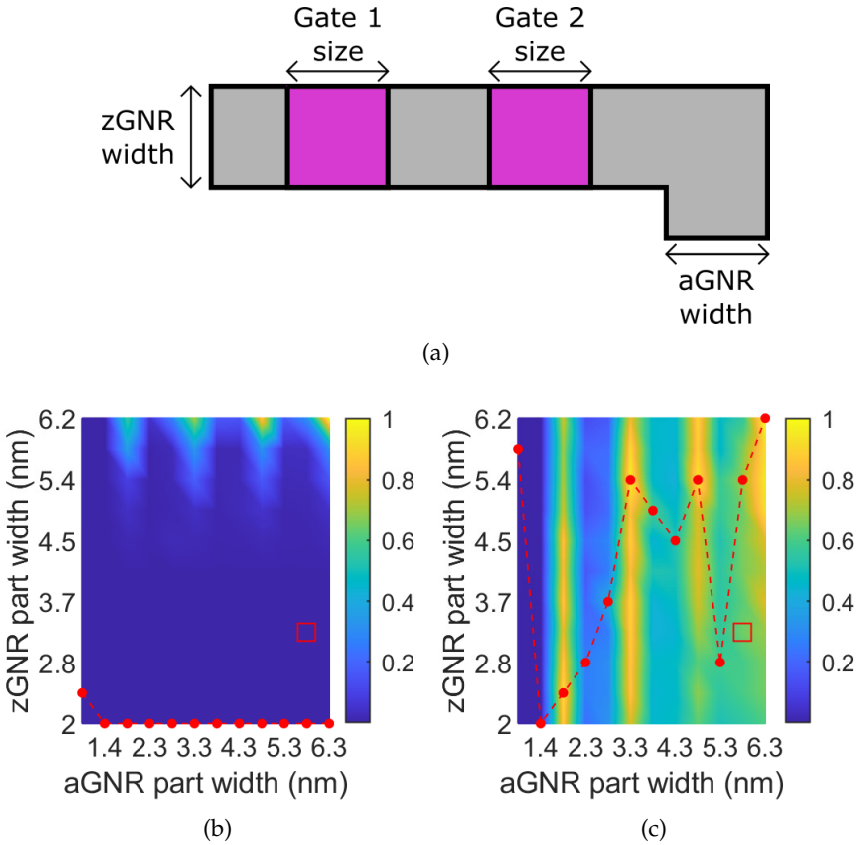



Figure 5.2: a) The L-shaped GNR top view, marked with the under investigation dimensions. b) The dependency of the (normalized) device conductance value (colorbar) on the width of the horizontal ($Y$ axis) and vertical ($X$ axis) part of an L-shaped GNR. $X$ and $Y$ axes refer to the size of vertical and horizontal part respectively. It corresponds to a switched-off device with low conductance (lower is better). The red dots refer to the lowest value in every column. The normalization value is $9.8455 \times 10^{-6}$ Siemens. c) It corresponds to a switched-on device with high conductance (higher is better). The red dots refer to the highest value in every column. The normalization value is $2.7676 \times 10^{-5}$ Siemens. The red square indicates the selected dimensions. The conductance calculations were made using the simulation method of Section 5.3.

Graphene Nanoribbons are expanded from their simplest straight form to an L-shaped form. As previewed in Fig. 5.1a, an L-shaped GNR is in fact a combination of the two aforementioned different types of GNRs, the zGNR, and the aGNR. This combination seems to be capable of creating a small bandgap in the GNRs' band structure, which is clearly visible

in the energy dispersion to conductance diagram of Fig. 5.1b, calculated using the state-of-the-art atomistic level modeling tool, that is described analytically in Chapter 3 and briefly in this chapter, in Section 5.3. This gap realization has been attributed to the scattering phenomena that are introduced through this edge direction change from zGNR to aGNR (Moysidis & Karafyllidis, 2018). In addition, L-shaped GNRs allow for easy conductance tuning through the application of external electric bias in the form of top gates. In contrast to common GFETs, additional electric biasing through any form of back gate terminal is not required. This feature provides another level of freedom, as it does not require Graphene to be placed on top of a thick insulating layer. The proposed devices can thus be placed on top of every compatible substrate, elastic, fabric, organic etc. Exploiting the biocompatibility feature, they can also bring logic to places such as on top of or near to human tissue and even on living cells.

### 5.2.1 L-shaped GNR sizing

The sizing of the proposed topology is crucial not only in order to compete with the state-of-the-art scaling trends, but also because it proves to affect its operation and performance. A very significant parameter is the ratio between the width of the zGNR and the aGNR part of the device. As presented in Fig. 5.2, this ratio significantly affects both the high conductance value (`OFF`-state) and low conductance value (`ON`-state) of the branches.The red line marks the lowest conductance value (Fig. 5.2b) and the highest conductance value (Fig. 5.2c) for a set of different width aGNR-zGNR combinations. Choosing a set of bigger sized branches, more to the right top corner of the graphs, will provide a switch with a higher high-conductance value as seen in Fig. 5.2c, but also with a poor low conductance value as seen in Fig. 5.2b. On the other hand, choosing very low GNR widths for both the horizontal and vertical part of the branch, will lead to a device with a very small low-conductance value but a very poor high-conductance value. Thus, the dimensions of the device have to be chosen carefully keeping in mind to maintain as good as possible both high and low conductance values. Fig. 5.2 also presents a phenomenon of periodicity that connects the dimension ratio of the device with its conductance. The aGNR size is dominant, as for specific values of aGNR width, the device generally has higher conductance and is not strongly affected by the

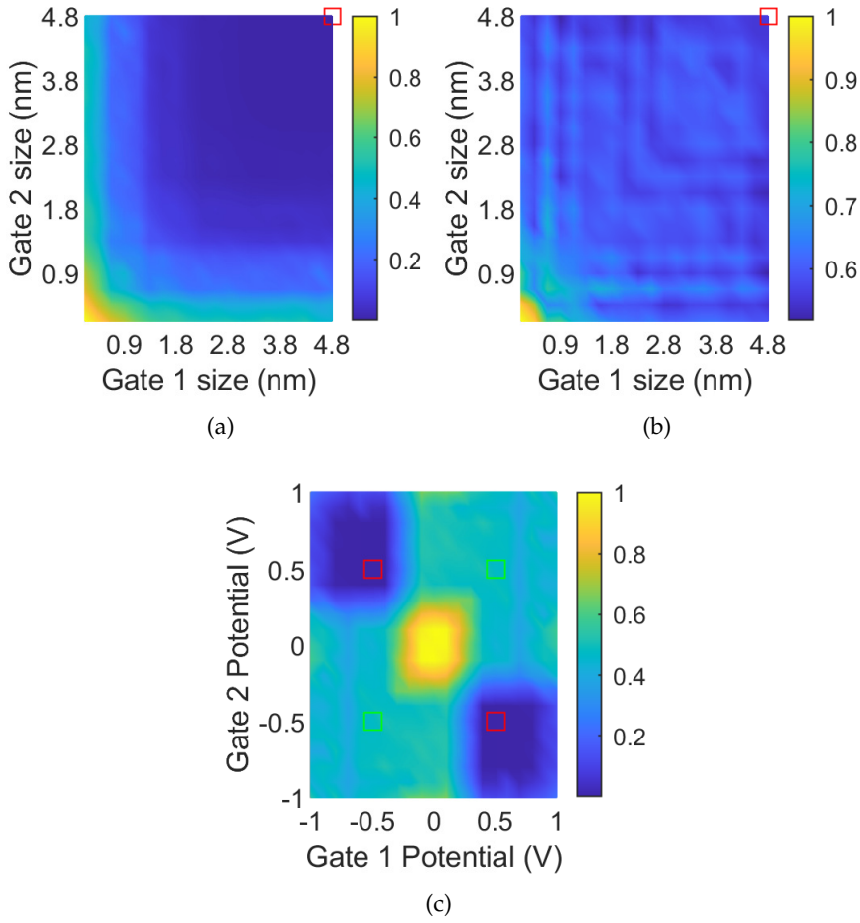



Figure 5.3: a) The dependency of the (normalized) conductance value (colorbar) of the OFF state (low conductance) on the size (length) of the gates ($X$ and $Y$ axes). The normalization value is $3.1175 \times 10^{-5}$ Siemens. b) The dependency of the conductance value of the ON state (high conductance) on the size (length) of the gates. The normalization value is $3.5498 \times 10^{-5}$ Siemens. c) The dependency of the conductance value of the topology on the applied potential on the two top gates. The normalization value is $4.2078 \times 10^{-5}$ Siemens. The green squares mark the ON-state operating point and the red square the OFF-state operating point. The conductance calculations were made using the simulation method of Section 5.3.

zGNR. This phenomenon of dependency of the conductance on the dimensions is probably due to the overlapping of the energy bands of zGNRs and aGNRs with specific dimensions.

For the simulations in this work, the dimensions of the branches are selected with the strategy to maintain an ON/OFF ratio of around $10^4$. Thus the selected dimensions are $3.266nm$ for the width of the horizontal part and $5.78nm$ for the width of the vertical part, as shown in Fig. 5.2a, keeping in mind that such small-sized branches are not so easy to be fabricated with the current fabrication technology. However, several experimental reports have proposed fabrication techniques that can provide GNRs of dimensions similar to the ones that are proposed here, in the following sections (Yagmurcukardes et al., 2016). In any case, the designer can make his own decision depending on his needs, based on Fig. 5.2. This decision will also be finally reflected in the performance of the device.

### 5.2.2 Top Gate Sizing

The gate size is also a significant aspect that must be carefully examined during the design of the device, as it affects its performance. The total gate area is the determinant factor of the device´s parasitic capacitance as described in Section 5.3.1, which will then affect the total delay of the device. Apart from that, as it has been proven both theoretically and experimentally, the length of the Graphene nanosheet does not significantly affect the total resistance of the device, mainly due to the ballistic transport, making the impact of the size (the length, as depicted in Fig. 5.2a) of the top gates as the main variable, which will determine the total length of the L-shaped GNR. As depicted in Fig. 5.3, the size of the top gates indeed has a significant effect on the conductance of the GNR. Fig. 5.3a presents the effect of different gate sizes on the conductance of a switched-off L-shaped GNR, while Fig. 5.3b presents the same effect on a switched-on L-shaped GNR. As those figures indicate, the effect on the OFF-state of the GNR is far more intense compared to the effect on the ON-state. In Fig. 5.3a, the maximum value is $6 \cdot 10^3\times$ bigger than the minimum, while in Fig. 5.3b, the maximum value is only $2\times$ bigger than the minimum. The maximum value of normalized conductance in both cases is encountered for a device with very small gates, which is reasonable, as applied electrical potential influences only a very small amount of carbon atoms. The increase in gate size, leads to a decrease in conductance. Also, both Figs. 5.3a and 5.3b show an antisymmetric relation, implying that the location of the different-sized gates is not significant. For the design of the presented topology, due to the severity of the effect described above, the size (length) of both gates has been selected to be equal to $\sim 4.8nm$, as marked with the red square in

the figures. This is the only operation point from those explored, that can provide the desirable ON/OFF ratio of the device, which is equal to $\sim 10^4$. Top gates of bigger length, may, probably, lead to even better results, leading however to a device with a bigger active area footprint. However, the results of the simulations indicate that gate-to-gate distance primarily impacts the device's area footprint, rather than its functional performance.

### 5.2.3 Top Gate Biasing

In Fig. 5.3c, the operation of an L-shaped GNR with 2 top-gates is investigated, under the influence of different potential values, in order to reasonably select the operating voltage of the proposed topology. It is clear that the operation of the device can be separated in 3 different generalized categories. The 1*st* category refers to the case where both top gates are connected to the ground, in which the device is tuned to the highest possible conductance, depending on its dimensions. The 2*nd* category refers to the case where the top gates are biased with voltage of different polarity. This is practically depicted by the two blue regions of Fig. 5.3c, where the device is tuned towards very low conductance values. The 3*rd* category refers to the case where the top gates are biased with a voltage of the same polarity. For this case, the values of the normalized conductance span in a very small range from $\sim 0.4$ up to $\sim 0.7$ regardless of the absolute value or the sign of the applied voltages. Having said that, it is obvious that the operation of each top gate is similar to the operation of a mechanical valve in a pipe line (i.e., graphene branch). As Fig. 5.3c implies, when all the applied biases have the same polarity, the flow of electrons and thus current, is allowed, setting the GNR to the ON-state, while when there are different polarity biases, the corresponding branch is not conductive, tuned to the OFF-state. A GNR that utilizes 3 top gates, like those employed in Section 5.4.1, operates based on the same principle: When all the top gates are biased with the same polarity potentials, then the GNR is tuned to the ON-state. On the contrary, when one of the top gates is biased with opposite polarity potential compared to the others, then the GNR is tuned to the OFF-state.

From Fig. 5.3c becomes obvious that the device needs potentials with different polarity on its inputs and top-gates in order to operate and provide an acceptable ON/OFF ratio. Thus, it is required to use a negative value for the logic level 0 that will provide easier device cascadability, and a positive value for the logic level 1. Also, Fig. 5.3c clearly shows

that the minimum conductance value is encountered when the top gate biases have the value pair of $-0.5$ *Volts* and 0.5 *Volts*. This is practically the top-gate bias combination that sets the L-shaped GNR to the OFF-state. In summary, for the effective switching operation of the L-shaped GNRs, 0.5 *Volts* for the logic 1, and $-0.5$ *Volts* for logic 0 were selected as the operation voltage values. The high conductance operating point (ON-state) at $(V_{TG1}, V_{TG2}) = (-0.5\ Volts, -0.5\ Volts)$ or $(+0.5\ Volts, +0.5\ Volts)$, provides a device with a conductance only $2.3\times$ smaller than the highest possible conductance at $(V_{TG1}, V_{TG2}) = (0\ Volts, 0\ Volts)$, which is depicted with yellow color in Fig. 5.3c. The value of ground (0 *Volts*) has also been used for the programming of the topology, as it is presented in the following Sections 5.4.2 and 5.4.2. Grounding a top-gate practically eliminates its participation in the tuning of the conductance of the GNR, which is now determined by the rest of the top-gate potentials.

## 5.3 Computational Method

The investigation of the use of Graphene as a material that comprises computing devices requires a simulation method that is able to take under consideration all the phenomena that play a decisive role in determining its electronic behavior. There have already been proposed a couple of different compact models for GNR-based Field-Effect Transistors (GNRFETs), that practically lead to parametrized equivalent circuits, allowing for easy and fast SPICE simulations, in an attempt to ease the GNRFET-based circuit design process (Chen, Rogachev, et al., 2013; Frégonèse et al., 2015; Henry & Das, 2012). However, the most accurate GNR device simulation is achieved through atomistic simulations. The state-of-the-art numerical tool that is used for computing the energy band structure of Graphene and thus its conduction consists of the combination of the Tight-Binding Hamiltonian (TBH) model (Bena & Montambaux, 2009; Reich et al., 2002), with the Non-Equilibrium Green's Function method (NEGF)(Datta, 2000, 2012). This method has been analytically described in Chapter 3. Here, its basic equations will be briefly presented as a reminder.

In this work, the topology awareness of Graphene is exploited through the use of L-shaped devices, which will be included in the simulation through the TBH; a square matrix given by equation 5.1:

$$H = -\tau \sum_{i,j} \hat{c}_i \hat{c}_j^{\dagger}, \tag{5.1}$$

with $\hat{c}_j^{\dagger}$, $\hat{c}_i$ being the creation and annihilation operators respectively and $\tau$ being the hopping integral that has been computed through the atomic orbitals of the interconnected atoms to be equal to about $-3eV$ (Chico et al., 1996).

Then, the investigated geometry is passed as a square Hamiltonian matrix, to the NEGF method for the calculation of the tranport properties. The method can be separated into 4 discrete steps, each one represented by one main equation. The $1^{st}$ step computes the retarded Green's function, as described by Eq. 5.2:

$$G^R = [EI - H - \Sigma_1 - \Sigma_2 - ... - \Sigma_N]^{-1}, \tag{5.2}$$

In that generalized form of equation 5.2, the retarded Green's function ($G^R$) is calculated for any given number of contacts of the device (Moysidis & Karafyllidis, 2018). Those contacts are introduced into the system by the self-energy factors, $\Sigma_{1...N}$. Also $E$, represents the energy level of the carriers.

The $2^{nd}$ step of the NEGF method is the calculation of $G^n$:

$$G^n = G^R \Sigma^{in} G^A, \tag{5.3}$$

$G^n$ represents the density of carriers at a specific energy level, $E$. $G^A$ is the advanced Green's function and $\Sigma^{in}$ describes the effects of all the externally applied power sources to the investigated system.

The $3^{rd}$ step of the NEGF method is to calculate the density of states (DoS) of the carriers in the nanodevice. This calculation requires the $G^R$ and $G^A$ from Eq. 5.2 and can be produced as follows:

$$A = i(G^R - G^A). \tag{5.4}$$

The DoS is the number of legal energy states in a system of a specific volume, in a specific energy range.

Finally, the $4^{th}$ step of this method leads to the calculation of the conductance of the investigated nanodevice, in a range of energies. This calculation directly leads to the realization of the energy dispersion diagrams.

$$G(E) = \frac{2q^2}{h} Trace[\Gamma_L G^R \Gamma_R G^A]. \tag{5.5}$$

This complex simulation method provides very accurate results for the electronic properties and in this case for the conductance (and thus the

resistance) of the GNR, based on its shape, dimensions and grid condition, and applied potentials.

In order to be able to make SPICE simulations feasible, in realistic time and with accurate results, the aforementioned NEGF method is combined with a Verilog-A model, in a way similar to Jiang et al., 2018b. After selecting all the appropriate technology characteristics of the device, that critically affect its operation, like the geometry, the materials, the number, location and size of the top gates, and also the operation voltage range, NEGF method is used to calculate the conductance. The conductance is calculated for various operating points in the operation voltage range and the granularity (the number of calculated operating points) can be selected depending on the demand, in terms of accuracy. Finally, the calculated conductance of every operating point is stored in a file which is then used by the Verilog-A model, for SPICE simulations, in this case using Cadence Virtuoso®.

Apart from the conductance, the calculation of further parameters is necessary for a better investigation of GNR-based devices, including their performance as circuit components.

### 5.3.1 Parasitic Capacitance

Parasitic capacitances play a significant role in determining operating dynamic characteristics of gated computing devices, mainly the propagation delay $t_{pd}$ and the dynamic power dissipation. Especially carbon-based gated devices like CNT FETs and GFETS, constitute a special case. Apart from the ordinary parallel plate capacitance of the top-gates ($C_{ox}$), they also display another form of capacitance, the quantum capacitance ($C_q$). The $C_{ox}$ is based on the geometrical characteristics of the top-gate and is calculated by the following well-known formula

$$C_{ox} = k\epsilon_0 \frac{A}{d}, \tag{5.6}$$

where $k$, and $d$ are the dielectric constant and the thickness of the gate dielectric respectively, $\epsilon_0$ is the permittivity of empty space, $A$ is the area of the top-gate.

Plenty of research has been conducted considering the determination of the quantum capacitance of Graphene. For the calculation in this chapter, the analytical formula presented in (Xia et al., 2009) has been leveraged, the results of which have been in also in accordance with experimental results

(Chen & Appenzeller, 2008; Xu et al., 2019; Yang et al., 2015). The formula is:

$$C_q = \frac{2q^2 k_B T}{\pi(\hbar v_F)^2} ln[2(1 + cosh\frac{qV_g}{k_B T})], \tag{5.7}$$

where $\hbar$ is the Planck constant, $q$ is the electron charge, $k_B$ is the Boltzmann constant, $v_F \simeq c/300$ is the Fermi velocity of the Dirac electron, c is the speed of light in vacuum and $V_g$ is the voltage of the Graphene channel. $Cq$ shows a clear dependence on the voltage applied on Graphene and thus the DOS. The two capacitances are practically connected in series, meaning that the total capacitance of a gate can be calculated as in (5.8):

$$C_{tot} = \frac{C_q \times C_{ox}}{C_q + C_{ox}} \tag{5.8}$$

### 5.3.2 Delay Estimation

The delay induced by the proposed topology is estimated through the Elmore delay model. In this estimation, apart from the resistance of the Graphene channel, the resistances of the contacts are taken into consideration. The Elmore delay model for the proposed topology can be previewed in (5.9) :

$$t_{pd} = (R_{GNR} \times C_{tot}) + (R_{C,L} + R_{C,R}) \times C_{min} \tag{5.9}$$

where $R_{GNR}$ is the resistance of the Graphene nanoribbon, $R_{C,L}$ and $R_{C,R}$ are the resistances of the left and right contacts of the device, respectively and $C_{tot}$ is the total parasitic capacitance as calculated in (5.8). $C_{min}$ is the conductance between the input and output contacts, which is equal to quantum capacitance $C_q$. Due to its very low value, (5.9) can be approximately rewritten as $t_{pd} = (R_{GNR} + R_{C,L} + R_{C,R}) \times C_{tot}$. The values of the contact resistances are considered to be the same and were based on various experimental results. Common values for contact resistances on GNR-based devices have been reported in the bibliography to span at a range from as low as $30\Omega \cdot \mu m$, up to almost $1K\Omega \cdot \mu m$, for contacts of various different metals (Cusati et al., 2017; Russo et al., 2010; Smith et al., 2013). For the provided calculations, a value of $R_{C,L} = R_{C,R} = 200\Omega \cdot \mu m$ was selected, as it is very common for the vast majority of the contact materials, and also used as the contact resistance value in (Jiang et al., 2018d).

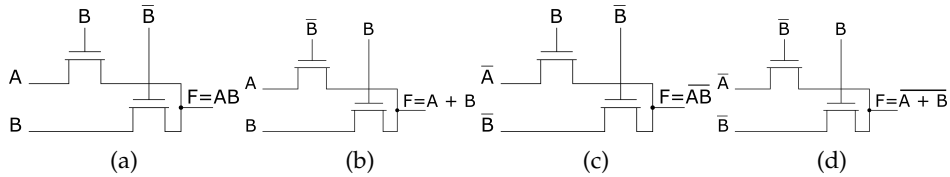



Figure 5.4: a) Circuit of a conventional PTL `AND` gate. b) Circuit of a conventional PTL `OR` gate. c) Circuit of a conventional PTL `NAND` gate. d) Circuit of a conventional PTL `NOR` gate.

### 5.3.3 Power Dissipation

For the estimations of the power dissipation of the proposed topology, both the static power ($P_{static}$) and the dynamic power ($P_{dynamic}$) have been included. For those calculations, a simple DC-equivalent has been designed and SPICE simulations have been conducted in order to calculate the total static power dissipation of comb-shaped topology. The SPICE simulations are conducted with the use of the NEGF method for the calculation of the conductance at various operating points in the operation voltage range. Every different steady state of the circuit was examined separately (the 2 different states of the `NOT` gate and the `Buffer`, the 4 different states of the `AND`, `OR`, and 2-input `XOR` gate, and the 8 different states of the 3-input `XOR` gate and the `Majority` gate, each one representing 1 row of the corresponding truth table), and only the worst case for each gate was included in Table 5.5. The portion of the dynamic power was also included, calculated by the formula:

$$P_{dynamic} = C_{tot} V_{dd} f, \tag{5.10}$$

where $C_{tot}$, is the total capacitance of the capacitors being charged and discharged during the operation of the topology, $V_{dd}$ is the operating voltage and $f$ is the operating frequency. Thus, the total power dissipated by the topology during its operation is calculated as $P_{tot} = P_{static} + P_{dynamic}$.

## 5.4 Graphene Nanoribbon based Pass Transistor Logic

Pass transistor logic is not a new idea and practically refers to a set of logic families that are used in the design of integrated circuits (ICs). This methodology for IC design is based on the use of transistors, or any other switching devices, as switches that pass logic values to the different nodes

of a logic circuit, in comparison to the conventional CMOS design methodology, in which the switching elements connect either the supply voltage or the ground voltage, directly to the output (Pal, 2014).

In general, such a design methodology promises to provide circuits with reduced transistor count and power dissipation that are also faster compared to their CMOS counterparts. However, some significant drawbacks and problems that the designers have to face when designing PTL circuits, manage to restrict their final performance. The most significant of those problems is the degradation of signal in long PTL combinational circuit chains, as well as the increase of series resistance (Al-Assadi et al., 1991). Those problems demand hardware overhead in order to be resolved, eliminating that way the main advantage of PTL circuits (Zimmermann & Fichtner, 1997).

Fig. 5.4, shows the basic boolean gates, designed using a PTL configuration. In those circuits, the switching element is depicted as a single NMOS transistor, however, transmission gates can also be utilized. Those 2 basic gates, the `AND` gate of Fig. 5.4a and `OR` gate of Fig. 5.4b, in combination with an Inverter compose a universal computing set. The circuit of a buffer is also needed to operate as a signal level restorer, in order for the major problem of signal degradation to be tackled. Also, those same circuits can be easily re-tuned to operate as a `NAND` and `NOR` gate respectively, as shown in Fig. 5.4c and Fig. 5.4d.

Pass Transistor Logic has been used in the past for area-saving reasons and it also found wide application in the design of multiplexers, however for most of the part of the digital circuit design, it has been abandoned, mainly due to the limitations it introduces in long combinational paths, especially with the tendency of reduction of the power supply voltage levels of the state of the art low power circuits. Nevertheless, the compliance of PTL design styles with new technologies like Carbon Nanotubes or novel 2D materials, is constantly investigated (Baidya et al., 2022; Ding et al., 2012; Wang et al., 2022).

In this work, all the interesting properties of Graphene and Graphene Nanoribbons, as reported in the previous sections, are aimed to be leveraged in order to revisit the old idea of Pass Transistor Logic, with the goal of developing circuits that can compete with the latest advancements in the field.

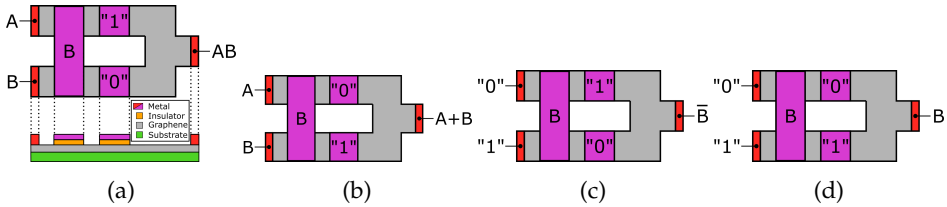



Figure 5.5: a) Top and side view of the proposed two-branch GNR-based topology, operating as an AND gate. b) Top view of the proposed GNR-based OR gate. c) Top view of the proposed GNR-based inverter (NOT gate). d) Top view of the proposed GNR-based buffer

### 5.4.1 GNR 2-branch comb-shaped topology

The proposed topology practically consists of two L-shaped GNR branches that are connected together, as seen in Fig. 5.5a. Each branch consists of two top gates, one that is common for both branches and one that belongs only to a single branch. The applied potential on those top gates determines the state of each branch, which operates based on the valve principle as described in Section 5.2.3. Due to the demand of potentials with different signs for the L-shaped GNR to operate, the proposed topologies will use $0.5Volts$ as logic level 1, and $-0.5Volts$ as logic level 0, exactly as described again in Section 5.2.3. Fig. 5.5a presents also a cross-section of the proposed topology. The metallic (ohmic) contacts that operate similarly to the Source/Drain contacts of conventional transistors and are responsible for injecting carriers in Graphene are marked with red color. The purple-colored metallic contacts act as the top gates and are responsible only for potential application. They are separated from the Graphene lattice (grey color) with an insulator (orange color). The substrate is marked with green color and it can be any graphene-compatible material, as the topology does not require a back gate terminal. Through the count of top gates, a re-programmable topology can be achieved, which operates accordingly under the influence of different combinations of top-gate and input voltages.

#### GNR based PTL Logic Gates

Concequently, this two-branch topology for the implementation of the basic logic gates in a PTL configuration is proposed. Fig. 5.5a, depicts the top view of this topology biased properly in order to operate as an AND

gate. Based on the aforementioned valve-like operation, its behavior can be analyzed as follows. When input B is at logic level 0, then only the bottom branch is switched ON, passing the value of B to the output, thus the output will be set to logic 0. In the case where B is at logic level 1, only the top branch will be switched ON, and the output will be set to the logic value of A. The description above can be written using boolean algebra as $OUT = \overline{B}B + AB = AB$

Fig. 5.5b, depicts the same topology tuned properly in order to operate as an OR gate. The only difference with the AND gate is the change of the values of the two single-branch top gates. Now, when B is set to logic level 0, only the top branch is switched ON, passing the logic value of A to the output and when B is set to logic value 1, only the bottom branch is switched ON, passing the value of B to the output. The description above can be written using boolean algebra as $OUT = A\overline{B} + BB = A\overline{B} + B = A + B$ (using the absorption law).

In Fig. 5.5c the topology of an inverter (NOT gate) is presented. It is practically the same topology as the two presented previously, however, now the inputs of the branches have constant values. This specific topology inverts input B. When B has the value of logic level 0, the bottom branch is conductive, setting the output to logic level 1. When B has the value of logic level 1, the top branch is conductive, passing logic level 0 to the output.

Finally, in order to avoid the need for conventional CMOS buffers for signal level restoration, the design of a buffer using this exact same technology is proposed. As seen in Fig. 5.5d the proposed buffer is similar to the inverter, with a small difference in top gate biasing. For this specific buffer of the aforementioned figure, when B is at logic level 0, the top branch is conductive, setting the output to logic level 0, and when B is at logic level 1, the bottom branch is conductive, setting the output to logic level 1. That way this topology manages to successfully buffer the input signal B.

The functionality of the aforementioned topologies is also verified through SPICE simulations, as shown in Fig. 5.6. All the investigated topologies behave as expected. In the cases of the AND and OR gates, there are some spikes at the output voltage levels. Those spikes appear when there is a transition at the input signals, and are bigger when two transitions happen simultaneously. Those events are attributed to the fact that during the transition, the two branches have similar conductance values for a very short period of time.

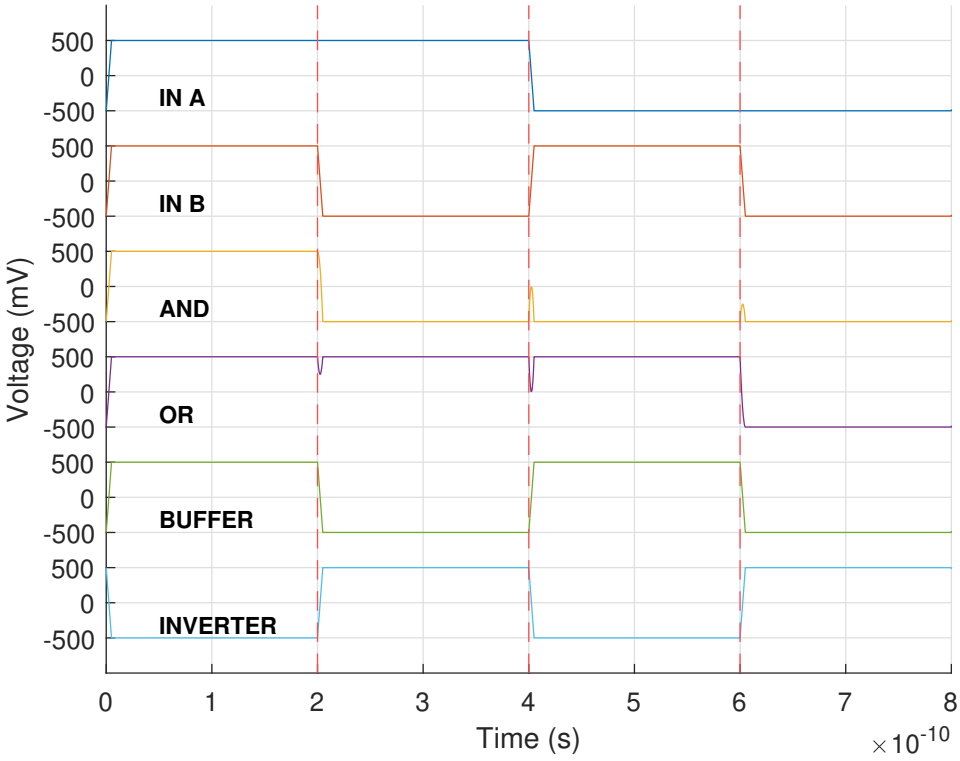



Figure 5.6: SPICE simulations of the proposed GNR based PTL logic gates.

With this universal set of gates, combinational logic circuits can be successfully designed in a PTL manner.

### 5.4.2 GNR 3-branch comb-shaped topology

As an extension of the aforementioned 2-branch comb-shaped topology, presented in the previous section, a 3-branch comb-shaped topology is also proposed, as seen in Fig.5.7a. This new topology has almost the same structure as the previous one. Apart from the substrate, it consists now of 4 ohmic contacts, 3 on the left acting as inputs of carriers and 1 on the right acting as an output. Here, there are also 5 top-gates for external electric bias application. Again, the top gates comprise metallic electrodes that are separated from the Graphene channel through an insulator (i.e. $Al_2O_3$). In this case, two out of five top gates are shared by two branches, while the remaining three belong solely to one branch. This topology is also reprogrammable and operates accordingly under the influence of different

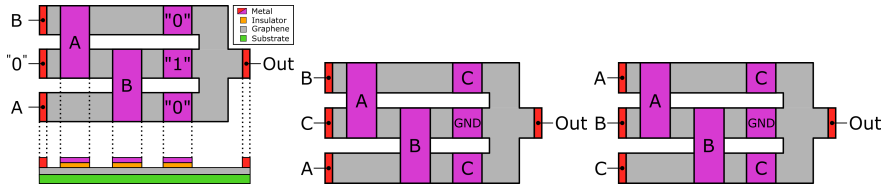



Figure 5.7: a) Top and side view of the proposed comb-shaped GNR-based 2-input XOR gate. The substrate is presented with green color, the Graphene sheet with black, insulator layers with orange, ohmic metallic contacts in direct contact with Graphene are presented with red color, and metallic contacts of the top gates with purple. b) Top view of the proposed comb shaped GNR-based 3-input XOR gate. c) Top view of the proposed comb shaped GNR-based 3-input MAJ gate.

biasing and input combinations, extending the set of Logic Gates that can be mapped in the 2-branch comb-shaped topology.

### GNR 2 Input XOR Gate

The proposed re-programmable comb-shaped topology can be tuned to operate as a 2-input XOR gate, by setting its top-gate biases and inputs to the appropriate signals, as shown by Fig. 5.7a. The way that the device operates is inspired by the architecture of the universal set of logic gates that have already been presented (Moysidis et al., 2018). However, there is a major difference, in this approach that is presented here, input signals are applied not only on the top gates, but also in the input terminals, passing through the device itself, and thus operating in a way that reminds the operation of pass transistor logic circuits (PTL).

Fig. 5.7a shows the proper biasing of the comb-shaped topology for the operation of the 2-input XOR gate. The single-branch top gates have fixed biases, logic 0 for the top and bottom branches, and logic 1 for the middle branch. Logic level 1 is equal to 0.5 Volts and the logic level 0 is equal to $-0.5$ Volts. Also in the input terminals, the proper values must be applied in order the topology to produce the output of $A \oplus B$. In the top branch, the value of signal B is applied, in the bottom branch the value of signal A, while the middle branch value is constant and equal to the value of logic 0.

The valid operation of the proposed topology with the appropriate programming can be verified through the validation of a 2-input XOR gate truth table, such as Table 5.1. The validation of this operation will be conducted through the examination of the state of each different branch of the device

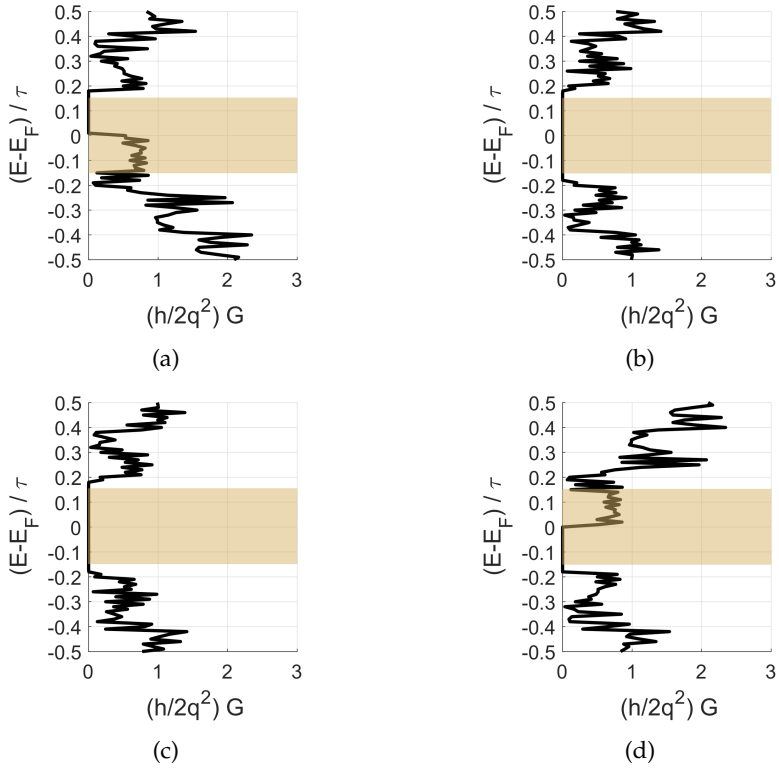



Figure 5.8: Energy dispersion of conductance diagrams for the GNR branches that comprise the presented topologies. a) Dispersion diagram of an L-shaped branch when both top gates are at logic 0. b) Dispersion diagram of an L-shaped branch when the leftmost top-gate is at logic 0 and rightmost at logic 1. c) Dispersion diagram of an L-shaped branch when the leftmost top gate is at logic 1 and rightmost at logic 0. d) Dispersion diagram of an L-shaped branch when both top gates are at logic 1.

(namely the top middle and bottom branches), under all four different input combinations.

For the case of both inputs `A` and `B` being at the logic 0, from Fig. 5.8 occurs that the top and bottom branches which are both described by Fig. 5.8a are switched `ON`, while the middle branch is switched `OFF`, as described in Fig. 5.8b. Thus, both the logic values of `A` and `B`, which are equal to logic 0, are delivered to the output. Similar is the operation of the device with an input of `A` and `B` being equal to logic 1. Now the top and bottom branches' conductance is described by Fig. 5.8b, while only the middle branch is switched `ON` (Fig. 5.8a, passing the value of logic 0 to the output.

Table 5.1: Truth table of 2-input XOR gate

| A **Input** | B **Input** | OUT |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

There are also two cases where the two inputs, A and B, do not have the same logic value. In both those cases the middle branch is switched OFF, as described by Fig. 5.8. When A is equal to logic 1 and B to 0, the value of A passes to the output from the bottom branch, which is switched ON. Similarly, when A is equal to logic 0 and B is equal to logic 1, the value of B passes through the top branch to the output.

### GNR 3-input XOR gate

As an extension to the aforementioned 2-input XOR gate, a topology that implements a 3-input XOR gate has been proposed. The topology presented in Fig. 5.7b, is practically the same re-programmable topology of Fig. 5.7a, with different applied signals. The extension from a 2-input to a 3-input XOR gate demands an increase of the input signals maintaining, however, the same occupied area.

The proposed topology of Fig. 5.7b, has the top-gates of the top and bottom branch biased with the value of input C and the value of the top-gate of the middle branch grounded (0 *Volts*). The only difference in the input signals is that now in the middle branch, the value of input C is applied.

As proof of the valid operation of the proposed topology, the accordance with the truth table of the 3-input XOR gate as proposed in the $4^{th}$ column of Table 5.2 will be analytically investigated. The operation of this topology can be examined in 3 separate categories.

The first category refers to the cases where only A and B inputs have the same logic value. In those cases, only the middle branch is switched ON, with a conductance tuned as in Fig. 5.8a, when both the top-gate biases are positive, or tuned as in Fig. 5.8a when both the top gate biases are negative. In those cases, the value of input C passes to the output, verifying the $2^{nd}$ and $7^{th}$ rows of the truth table.

Table 5.2: Truth tables of the 3-input XOR gate, the Majority gate and the 1-bit FULL ADDER cell

| A Input | B Input | C Input | 3XOR | MAJ | FULL ADDER | |
|---|---|---|---|---|---|---|
| | | | | | SUM | CARRY |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 |

The second category is the one where A and B have different logic values. In all those cases, the middle branch is switched OFF. The switched ON branch is every time one, either the top or the bottom, and more specifically each time the one that has top-gate biases of the same value. All those cases cover from the $3^{rd}$ up to the $6^{th}$ row of the truth table.

Finally, the third category covers the extreme cases where all the input signals have the same value. In those cases all three branches are switched ON, passing the same value to the output, either logic 0, covering the $1^{st}$ row of the truth table, or logic 1, covering the $8^{th}$ row of the truth table.

### GNR Majority Gate

The technology of re-programmable comb-shaped devices allows for the realization of a Majority gate, which in combination with the XOR gates presented in Sections 5.4.2 and 5.4.2, enables the creation of a half adder and a 1-bit full adder cell. Therefore, it is crucial to achieve the realization of the Majority gate. A first approach of a comb-shaped GNR-based Majority gate has already been presented (Moysidis et al., 2019a), however, our proposed topology operates differently, by passing the input signals through the devices, more similar to the PTL circuits operation, allowing for the realization of a re-programmable topology and performance optimizations.

The operation of the majority gate can thus be replicated by the aforementioned 3 branch comb shaped topology. In fact, the only differences

now, in comparison to the previously described 2-input and 3-input XOR logic gates, are the different locations of the externally applied signals (inputs A, B, C that pass through the device).

The proposed device utilizes shared input gates that retain the initial signal values of inputs A and B. Additionally, the 3 single-branch top-gates also retain their values during the 3-input XOR gate operation. The only alteration occurs at the inputs of the device, where the applied signals from top to bottom branch are A, B, and C, respectively. This topology can be observed as being appropriately biased in Fig. 5.7c.

Similar to Section 5.4.2, the operation of the proposed device to confirm its effectiveness as a majority gate through the MAJ column of Table 5.2 will be analytically examined. The operation of this majority gate topology can be divided into three distinct categories.

The first category represents the cases where only A and B have matching logic values. In these cases, the middle branch is the only one switched ON and is described by the energy dispersion diagram of Fig. 5.8a when A and B are equal to logic level 0 and Fig. 5.8d when A and B are equal to logic level 1. As a result, only the logic value of B is passed to the output, being either 0 for the $2^{nd}$ or 1 for the $7^{th}$ row of the truth Table (5.2).

The second category encompasses cases where A and B possess different logic values. Those where A and C have the same value, set the top branch to a switch ON state, and pass the value of input A to the output, as outlined in rows 3 and 6 of Table 5.2. Similarly, those where B and C have the same value, set the bottom branch to a switch ON state and pass the value of C to the output, successfully verifying rows 4 and 5 of Table 5.2.

The third category entails extreme cases where all three inputs have the same value. In both those cases, all three branches are set to a switch ON state, visible in Fig. 5.8a, when the input value is equal to logic 0 and in Fig. 5.8d when the input value is equal to logic 1. Those cases cover also the $1^{st}$ and $8^{th}$ row of Table 5.2.

### GNR based Full-Adder

As a first proof of the usefulness of the aforementioned presented topology, it has been utilized as building block of a basic 1-bit Full Adder (FA) cell. The realization of a full adder is a natural outcome of the presented XOR and MAJ gates. In fact, the direct equivalent of a Full Adder cell is a combination of a 3-input XOR gate for the calculation of the SUM part and a 3-input Majority gate for the calculation of the CARRY part, as presented

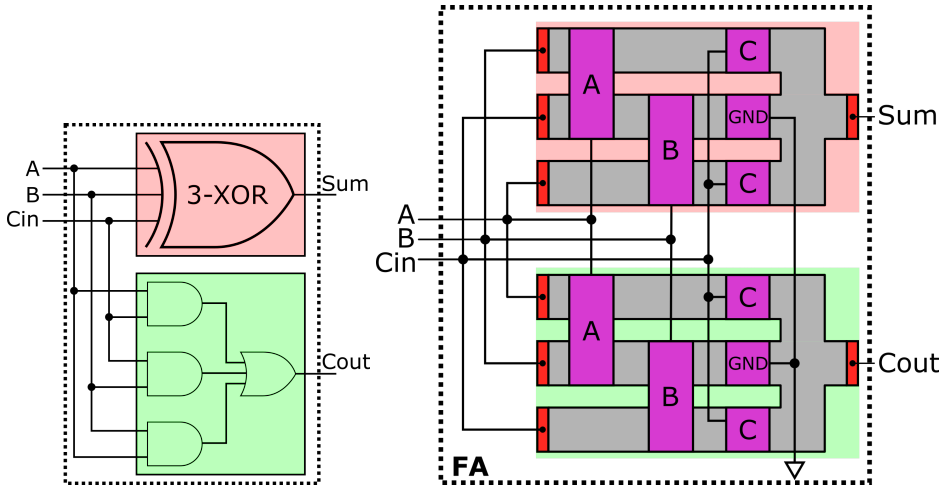



Figure 5.9: a) Basic 1-bit FA cell at logic level consisted by a 3-input XOR gate and a Majority gate. b) Equivalent 1-bit FA cell structure, consisting by 2 comb shaped re-programmable gates.

in Fig. 5.9a, along with its truth table (Table 5.2). In the latter, it becomes obvious that the truth table of SUM, indeed matches that of a 3-input XOR gate and the truth table of the CARRY, matches that of a 3-input Majority gate.

Thus, for the implementation of a 1-bit Full-Adder cell, two appropriately programmed comb-shaped topologies have been used, as in Fig. 5.9b. The top with the red background is programmed to operate as a 3-input XOR gate, and the bottom is programmed to operate as a 3-input Majority gate. Our proposed cell demands only two comb-shaped GNR devices, maintaining a very low device count, in comparison with the conventional 28T CMOS FA cell. The interconnects of such devices can be implemented through either metal or Graphene wires (Hazra & Basu, 2018; Stan et al., 2009) and this is going to be part of future research upon devices fabrication.

For the verification of its valid operation, the results of SPICE simulations are presented in Fig. 5.10. The operation of the circuits was examined with an operating period of $400ps$, in order to provide a fair comparison with the other presented architectures, as described in (Jiang et al., 2019b). The results show an accurate operation that perfectly validates both the

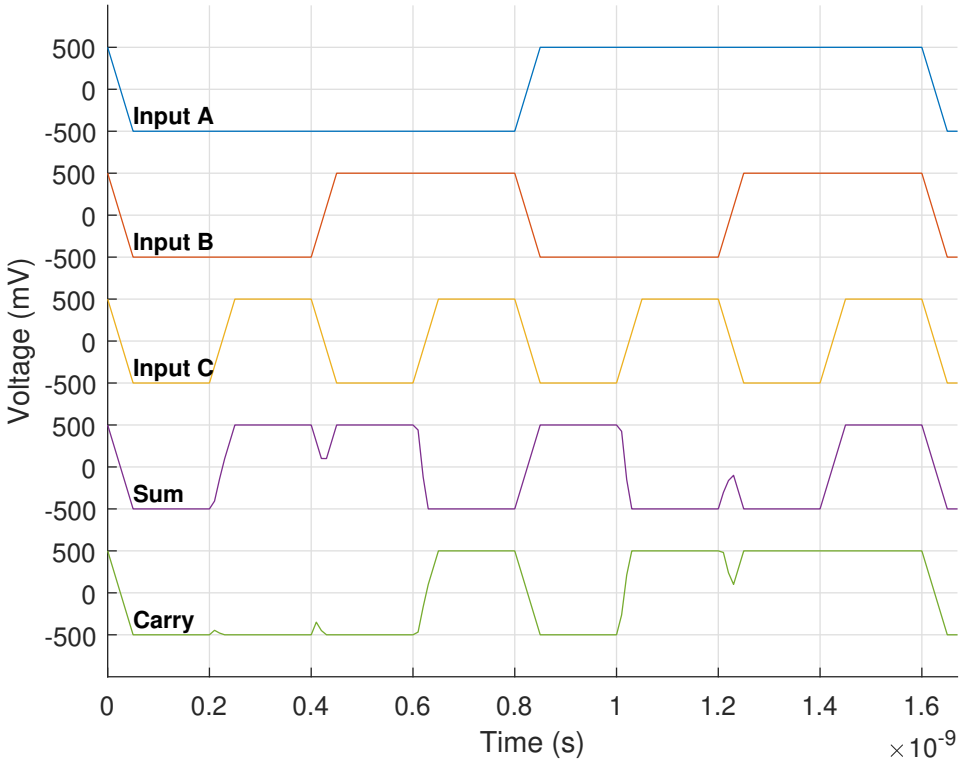



Figure 5.10: SPICE simulations of 1-bit FA cell based on GNR comb-shaped reprogrammable topologies.

truth tables of `SUM` and `Carry`. Some spikes appear at both the output signals, at around $0.4ps$ and $1.2ps$. Those spikes coincide with the simultaneous transition of two different inputs (inputs `B` and `C` for both cases), which momentarily tunes two different branches of a single comb-shaped topology to similar resistance values, affecting the output voltage. However, this change in the output voltage, does not have an amplitude big enough to affect the operation of the device (it is not bigger than the 50% of total voltage range). Also, the circuit manages to overcome this instability in a very small amount of time and as it will operate always between two clocked flip-flops, those small intermediate signal variations, will not affect the final output.

Table 5.3: Area footprint comparison

| | AREA ($nm^2$) | | |
|---|---|---|---|
| | Comb-Shaped GNR | CMOS | Complementary GNR |
| `AND` | $1.384 \times 10^2$ | $1.452 \times 10^3$ | $4.272 \times 10^1$ |
| `OR` | $1.384 \times 10^2$ | – | – |
| `NOT` | $1.384 \times 10^2$ | $4.840 \times 10^2$ | $5.431 \times 10^1$ |
| `Buffer` | $1.384 \times 10^2$ | $9.680 \times 10^2$ | $3.283 \times 10^1$ |
| `XOR-2` | $2.532 \times 10^2$ | $2.420 \times 10^3$ | $4.038 \times 10^1$ |
| `XOR-3` | $2.532 \times 10^2$ | $4.840 \times 10^3$ | $5.179 \times 10^1$ |
| `Majority-3` | $2.532 \times 10^2$ | $2.180 \times 10^4$ | $5.078 \times 10^1$ |
| `1-bit FA` | $5.265 \times 10^2$ | $3.004 \times 10^4$ | $1.538 \times 10^2$ |

### 5.4.3 Results and Discussion

Apart from the operation evaluation that has been carried out, it is also crucial for the topology to be tested in terms of performance. As mentioned in Section 5.3, and is presented in Tables 5.3, 5.4, 5.5, the performance of the proposed topologies has been examined through measuring their area, delay and power and comparing it with state-of-the-art complementary GFET (Jiang et al., 2019b) and 7nm FinFET CMOS architectures (Jiang et al., 2019b; Arizona State University, n.d.).

#### Area Footprint

For the case of the area, as a first observation comes that all four implemented gates with the 2 branch topology have the exact same area footprint, as well as that all three implemented logic gates implemented with the 3 branch topology have also the same area footprint. This is a straight outcome to the fact that both those topologies are re-configurable and do not require any shape or dimension changes, just a re-arrangement of the applied signals. For the case of the gates implemented with the 2 branch topology (`AND`, `OR`, `NOT`, `Buffer`), and in terms of absolute numbers, the area covered is $1.383 \times 10^2$. Compared to its CMOS counterparts its $\sim 10\times$, $\sim 3.5\times$ and $\sim 7\times$ smaller for the cases of `AND` gate, `NOT` gate and `Buffer`

respectively. However, compared with the complementary GFET counterparts, the case is different. The proposed topology is bigger by a factor of $\sim 3\times$, $\sim 2.5\times$ and $\sim 4\times$ for the `AND`, `NOT` and `Buffer` cases, as mentioned above.

As for the 3 branch topology, in terms of absolute numbers, the area covered by the implemented gates is $2.532 \times 10^2 nm^2$. Compared to its CMOS counterparts it is $\sim 9.5\times$, $\sim 19\times$ and $\sim 86\times$ better for the cases of 2-input `XOR` gate, 3-input `XOR` gate and 3-input `Majority` gate, respectively. In comparison with its state-of-the-art complementary GFET counterparts, it is very close, being only $\sim 6\times$ bigger for the case of 2 input `XOR` gate and $5\times$ bigger for the cases of 3-input `XOR` and `Majority` gates. Also in the case of the Majority gate, it is 50% smaller than the previous approach on comb-shaped majority gate (Moysidis et al., 2019a), considering that it uses the exact same dimensions at its Graphene branches. In this case and in the search for optimization, in a manner more similar to the PTL circuits, a Majority gate using only the half size of the previously presented one has been implemented. The topology has been practically condensed from a 6-branch device to a 3-branch device, bringing it down to the same dimensions with the 2-input and 3-input `XOR` gates. The examined circuit, the FA cell, consists of 2 GNR comb-shaped re-configurable topologies, thus its size is calculated to be a bit higher than 2 times the area of a single comb-shaped topology. In absolute numbers, as shown in Table 5.5, the total area of the FA is calculated to be $5.265 \times 10^2 nm^2$, which is $\sim 57\times$ smaller, and $\sim 3\times$ bigger than its CMOS and complementary GFET counterparts, respectively.

**Delay Performance**

For the estimations of the transition delay, the Elmore delay model was leveraged, as described in Section 5.3.2. The computed delay here the same for all-seven investigated cases, both for those based on the 2 branch topology and those based on the 3 branch topology. This result is also based on the fact that the device is the same for each implemented gate, with the only difference being the different signal locations. In other words, it does not depend either on the transistor count changes, as in conventional CMOS, or the gate size, as happens in complementary GFET. A fixed delay of $\sim 0.02054 ps$ has been calculated for all the investigated cases. Beginning from the gates that are based on the 2 branch topology, this is translated as $\sim 465\times$, $\sim 54\times$ and $\sim 99\times$ better performance than the corresponding

Table 5.4: Propagation delay comparison

| | DELAY ($ps$) | | |
|---|---|---|---|
| | Comb-Shaped GNR | CMOS | Complementary GNR |
| AND | $2.054 \times 10^{-2}$ | 9.618 | 1.38 |
| OR | $2.054 \times 10^{-2}$ | – | – |
| NOT | $2.054 \times 10^{-2}$ | 1.110 | 0.27 |
| Buffer | $2.054 \times 10^{-2}$ | 2.040 | 0.42 |
| XOR-2 | $2.054 \times 10^{-2}$ | 9.168 | 7.48 |
| XOR-3 | $2.054 \times 10^{-2}$ | $1.373 \times 10^{1}$ | 1.583 |
| Majority-3 | $2.054 \times 10^{-2}$ | $1.099 \times 10^{1}$ | 0.109 |
| 1-bit FA | $2.054 \times 10^{-2}$ | 11.863 | 1.910 |

CMOS counterparts, for the cases of the AND gate, the NOT gate and Buffer respectively. It also denotes better performance compared to the complementary GNR counterparts by a factor of $\sim 67\times$, $\sim 13\times$ and $\sim 20\times$ for the AND, NOT and Buffer cases.

For the logic gates related with the 3 branch topology, this value of $\sim 0.02054ps$ implies a performance which is $\sim 446\times$, $\sim 668\times$ and $\sim 535\times$ better than its CMOS counterparts for the cases of 2-input XOR, 3-input XOR and 3-input Majority gates, respectively. The proposed comb-shaped topology has also similar and slightly better performance in comparison with the complementary GFET architecture. It is $\sim 364\times$, $\sim 77\times$ and $\sim 5\times$ faster for the cases of 2-input XOR, 3-input XOR and 3-input Majority gates, respectively. For those calculations, all possible input combinations that can lead to an output transition have been examined. From all those input to output transitions, only the worst-case scenario was kept. Due to the symmetry of the device, where all top gates have the exact same size, and all branches have the same dimensions, the worst case produces always the same delay. Our 1-bit FA implementation consists of a single 3-input XOR gate for the SUM part, and a single 3-input Majority gate for the Carry part of the circuits. Thus, the total delay of the circuit is equal to the delay of the worst part of the circuit. In this case, as the two gates are practically designed with the exact same GNR comb-shaped topology but with different programming, the total delay is equal to the delay of the 3-input XOR and Majority gate, calculated to be equal to $2.052 \times 10^{-2} ps$. This is $578\times$

Table 5.5: Power dissipation comparison

| | POWER ($nW$) | | | | |
|---|---|---|---|---|---|
| | Comb-Shaped GNR | | | CMOS [1] ($\times 10^3$) | Complementary GNR |
| | Static | Dynamic | Total | Total | Total |
| AND | 4.269 | 0.5013 | 4.7703 | 0.5886 | 4.628 |
| OR | 4.269 | 0.5013 | 4.7703 | – | – |
| NOT | 4.269 | 0.5013 | 4.7703 | 0.4621 | 0.947 |
| Buffer | 4.269 | 0.5013 | 4.7703 | 0.4704 | 0.937 |
| XOR-2 | 8.534 | 1.003 | 9.536 | 0.5923 | 1.734 |
| XOR-3 | 8.534 | 1.675 | 10.204 | 1.768 | 1.654 |
| Majority-3 | 8.534 | 1.675 | 10.204 | 3.482 | 3.388 |
| 1-bit FA | 17.068 | 3.745 | 20.408 | 7.915 | 6.188 |

and 93× smaller than its CMOS and complementary GFET counterparts, respectively.

**Power Performance**

Finally, for the power dissipated, the worst case for each one of the examined logic gates is presented. The static part of the total power dissipation was calculated with the help of a simple DC-equivalent circuit for each topology, simulated through SPICE, as mentioned in Section 5.3.3. For the dynamic part, the equation 5.10 was leveraged. For the sake of comparison, the selected device clock period was $400ps$, equal to the period of the GFET and CMOS gates implementations (Jiang et al., 2019b). The power dissipated for all the gates based on the 2 branch topology is the same, and generally lower compared to the power dissipated by the gates based on the 3 branch topology, due to the reduced number of capacitances that have switching activity. However, the power dissipated is slightly lower in the case of the 2-input XOR gate, than in the cases of the 3-input XOR and Majority gates. This is an outcome of the fact that the 3 single-branch top-gates in the case of 2-XOR, have fixed potential (Fig. 5.7(a)), while for the 3-XOR and MAJ, 2 out of 3 single-branch top-gates are biased by the C-input signal, which is not constant (Fig. 5.7(b) and Fig. 5.7(c)). Thus, even though the static power is equal for the three cases as the topology remains the

Table 5.6: Power - Delay product comparison

| POWER × DELAY ($nW \cdot ps$) | | | |
|---|---|---|---|
| | Comb-Shaped GNR | CMOS | Complementary GNR |
| AND | 0.0980 | $5.66 \times 10^3$ | 6.3866 |
| OR | 0.0980 | – | – |
| NOT | 0.0980 | $0.51 \times 10^3$ | 0.2557 |
| Buffer | 0.0980 | $0.96 \times 10^3$ | 0.3935 |
| XOR-2 | 0.1958 | $5.43 \times 10^3$ | 12.970 |
| XOR-3 | 0.2095 | $2.43 \times 10^4$ | 2.618 |
| Majority-3 | 0.2095 | $3.83 \times 10^4$ | 0.3692 |
| 1-bit FA | 0.4293 | $9.37 \times 10^4$ | 11.819 |

same, the dynamic power dissipation is higher at the 3-input gates causing this small difference.

In absolute numbers, the total power dissipated by the AND, OR, NOT gates the Buffer is equal to $4.7703nW$. This makes the proposed topologies $\sim 20\times$, $\sim 95\times$ and $\sim 98\times$ more power efficient than its CMOS counterparts for the cases of the AND gate, the NOT gate and the Buffer respectively. On the other hand, the proposed 2 branch topology dissipated more power compared to the complementary GFET architecture. For the case of the AND gate the dissipation is almost equal, however for the cases of the NOT gate and the Buffer, the complementary GFET counterparts are $\sim 5\times$ and also $\sim 5\times$ more power efficient.

For the case of the 3 branch topology, in absolute numbers the total power dissipated by the 2-XOR gate is as low as $9.536nW$ and by both the 3-input gates, it is $10.204nW$. This makes the proposed topologies $\sim 62\times$, $\sim 173\times$ and $\sim 341\times$ more power efficient than its CMOS counterparts for the cases of 2-input XOR gate, 3-input XOR and Majority gates respectively. Its performance in terms of power is a lot closer to that of the complementary GFET architecture. By comparing them, our proposed comb-shaped topology is only $\sim 6\times$, $\sim 6\times$ and $\sim 3\times$ worst in terms of power dissipation for the cases of 2-input XOR,3-input XOR and Majority gates respectively. As estimated, the total power dissipated by the 1-bit FA cell, is calculated to be equal to the power of its components, which is $20.408nW$. This is $\sim 388\times$ more power efficient than its CMOS alternative and $\sim 3\times$

more power consuming than its complementary GFET counterparts.

The figure of merit of this work, goes beyond the re-programmability of the proposed topology, which introduces Graphene in the field of reconfigurable computing, and the ability to functionally operate without the use of a back gate contact which allows for easier combination with alternative substrate materials. In terms of performance, the proposed comb-shaped topology manages to provide favorable results. It is implied through Tables 5.4 and 5.5, as well as stated in Table 5.6, that the proposed topology performs ideally, also when other approaches are considered, in terms of the Power-Delay factor, which describes the efficiency of the device, and practically represents the energy that each logic gate consumes in order to complete an operation. The results compared to the CMOS architecture are anticipated, as comb-shaped GNRs are performing better in terms of power and delay. The comparison with the complementary GFET results in a slightly superior power-delay product for the proposed topology, mainly owing to the lower delay of the comb-shaped topology that manages to overcome the worst power performance when compared with complementary GFET. More specifically, for the cases of the 2-input `XOR`, 3-input `XOR`, the Majority gate, and also the proposed FA cell, the comb-shaped topology manages to provide a power delay product $66\times$, $12.5\times$, $1.5\times$ and $28\times$ lower compared to its complementary GFET topologies. Additionally, for the cases of the `AND` gate, the not `NOT` gate and the `Buffer`, the power-delay product is measured to be respectively $\sim 65\times$, $\sim 2.5\times$ and $\sim 4\times$ lower compared to its GFET counterparts.

## 5.5 Multi-Valued-Logic in Graphene

In Chapter 4 the butterfly-shaped Graphene Quantum Point Contact (G-QPC) device is analytically investigated in terms of its electronic properties. In fact, the effect of lattice defects on its electronic properties is examined. Through this examination, and specifically through the energy dispersion diagrams, the conductance quantization effect becomes evident. This is due to the quantum hall effect, which, unlike most other materials, exists even in room temperature (Novoselov et al., 2007b). Those plateaus that appear in the conductance for a specific range of energy make it easier to create Multi-Valued-Logic circuits and use them with higher radix numeral systems.

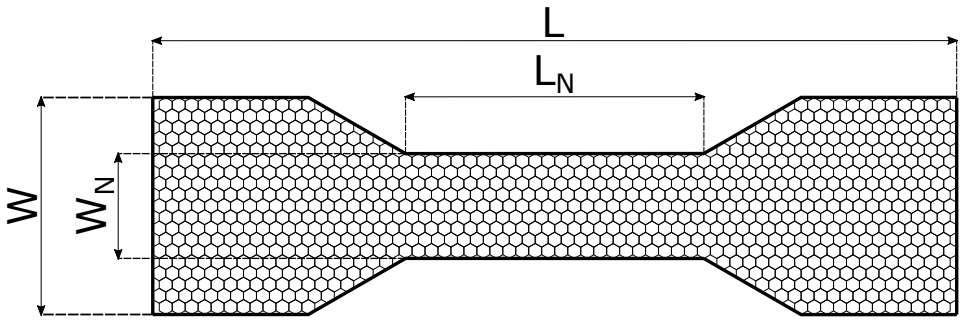



Figure 5.11: The G-QPC layer of the device used for the radix-4 arithmetic system. The dimensions are $L = 25a$, $L_N = 9a, W = 14a, W_N = 4a$, where $L$ is the total length of the device, $L_N$ is the length of the shortened area, $W$ is the total width and $W_N$ is the width of the shortened area, respectively.

For that reason, here, this ability is further investigated. Through appropriate selection of the geometric structure of the device, and especially the width of the shortened area of the G-QPC, the number of the quantized conductance levels is determined, as well as the range of energies that each one covers and consequanetly the radix of the numeral system that is the most appropriate. As a proof of concept, a two digit adder is designed using Graphene and the simulation results show the efficacy of the proposed circuit.

### 5.5.1 Graphene Quantum Point Contact device for MVL

In the proposed implementation, the employed device has fixed specific dimensions that are critical for its behavior under the influence of different back gate voltages. Those dimensions are shown in Fig. 5.11.

The G-QPC comprises a narrow Graphene nanoribbon connected to two wider nanoribbons on its right and left. The G-QPC has its zigzag edge along the length L. The zigzag-edged Graphene nanoribbons maintain the highest electron mobility. The G-QPC grid is placed on a silicon dioxide substrate about $300nm$ thick. A metallic contact on a heavily doped n-Si substrate acts as the back gate. The source and drain contacts are also placed on the dielectric. In particular, the corresponding G-QPC device with the proposed dimensions has 6 different quantized conductance levels, 5 of which are broad enough to be actually usable. Those levels are sufficient enough for designing circuits for MVL logic and, more specifically, Radix-4 (Quaternary) arithmetics, because they can encode all the

four necessary digits. In fact, half of those levels can be bypassed, so that the selected levels are even farther from one another, and the results can be easier to separate by appropriate selection. Moreover, the device has also one top gate and one back gate. The top gate is separated from the Graphene nanoribbon by a silicon dioxide layer, so that no electrons can enter the device from either the top or back gates. The length of the top gate is $5a$, where $a \simeq 0.246nm$ is the lattice constant of graphene, while the back gate covers the whole device. In the proposed design, the back gate voltage represents the input of the device, while the top gate voltage is constant and used only for minimizing small overshoots that may appear at the conductance levels.

In the proposed design, the device conductance changes by applying the appropriate voltage at the back gate of the device. The calculation of this conductance will be done using the Non-Equilibrium Green's function method (NEGF) along with Tight Binding Hamiltonians Datta, 2000; Reich et al., 2002, as analytically described in Chapter 3. Briefly, the conductance of the G-QPC device, as a function of energy is calculated as follows:

$$G_{value}(E) = \frac{2q^2}{h} Trace[\Gamma_L G^R \Gamma_R G^A] \tag{5.11}$$

where $\Gamma_L$ and $\Gamma_R$, are the broadening factors, $G^R$ is the retarded Green's function, $G^A$ is the advanced Green's function, $q = 1.6 \cdot 10^{-19} Coulomb$ is the electron charge and $h = 1.06 \cdot 10^{-34} J \cdot s$ the Planck constant. Taking all these into account, Eq. 5.11 as found above can be rewritten:

$$G_{value}(E) = 7.7463 \cdot 10^{-5} \cdot Trace[\Gamma_L G^R \Gamma_R G^A] \tag{5.12}$$

As a result, in the aforementioned Eq. 5.12 only $Trace[\Gamma_L G^R \Gamma_R G^A]$ depends on energy and, for specific energy values, the conductance of the device can be computed.

Even though conductance can be calculated for every energy value, only electrons with energies near Fermi Energy level, take part in current flow. Thus, the conductance of only a small region of energies, a few $kT$ above and below energy Fermi, should be taken into consideration. Therefore, the total conductance that a G-QPC device displays, can be calculated as the mean value of conductance for this energy region of interest. In fact, back gate voltage moves the Fermi energy level up or down, and so changes the conductance that the device displays.

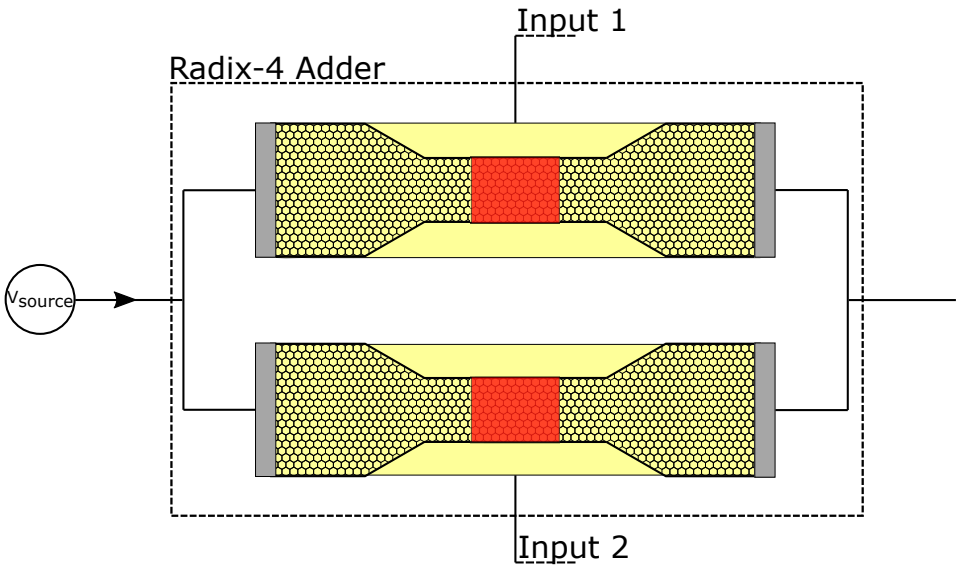



Figure 5.12: The circuit of the two digit adder. Inputs 1 and 2 represent the terminals for the back gate voltages.

### 5.5.2 The Radix-4 Numerical System

A radix-4 numeral system, consists of a set of numbers from $-3$ to 3, including 0. A conversion to the more common decimal system can be achieved with the following equation (Parhami, 1999)

$$D = \sum_{i}^{n} x_i \cdot 4^i \tag{5.13}$$

where $x_i$ represents a number from the set described above. In this case, an unsigned number representation is used, so the digits that will be taken under consideration are $[0, 1, 2, 3]$. Such a system is very convenient to use, because the radix proposed, is a power of 2, and the conversion from and to the binary system is straightforward and efficient. Thus, devices using a radix 4 system, could be easily designed along with today's very mature binary logic circuits, even as interconnects, with the advantage of optimizing the connection wiring between binary subsystems (Smith, 1988). The operation of addition in such a numeral system is described in (KS & Gurumurthy, 2009).

Table 5.7: Correlation between the Quaternary system digits and back gate voltages used for tuning properly the G-QPC device

| Quaternary Digit | Back Gate Voltage(Volts) |
|---|---|
| 0 | 0.13 |
| 1 | −2.7 |
| 2 | −2.15 |
| 3 | −1.45 |

### 5.5.3 High Radix G-QPC Circuit

By using the G-QPC device that exploits the unique characteristics of Graphene, and the quantization of conductance that is displayed, a radix 4 adder is proposed. For the creation of a two Quaternary-digit adder, two G-QPCs are connected together in parallel, as shown in Fig. 5.12. In this figure, the yellow background represents the silicon dioxide layer below of which the back gate is placed, while the two grey regions on the left and right depict the source and drain contacts, respectively. Moreover, the red region in the middle is the top gate. As mentioned before, with the application of the appropriate voltage at each back gate, the tuning of the devices at a specific conductance level is achieved. Thus, the output current will differ, for different combinations of inputs. $V_{SOURCE}$ can be set at any value that will not damage the device, and fortunately, Graphene can sustain high current densities and therefore high source voltages. Nevertheless, it would be more convenient to use voltages similar to those already used on the back or top gates. The current that will run through the device, will be measured at the output and will determine the result of the addition.

The devices shown in Fig. 5.12 are tuned separately, but the total conductance that will arise will determine the result of the addition being executed. The total conductance of a circuit with devices in parallel connection can be easily calculated by:

$$G_{TOTAL} = G_1 + G_2 \tag{5.14}$$

The potentials applied to the back gates are specific, and each one represents one digit out of the four that make up a Quaternary numeral system. Those correlations between back gate voltages and Quaternary digits can be seen in the following Tab. 5.7.

The specific back gate voltages mentioned above, were chosen so that

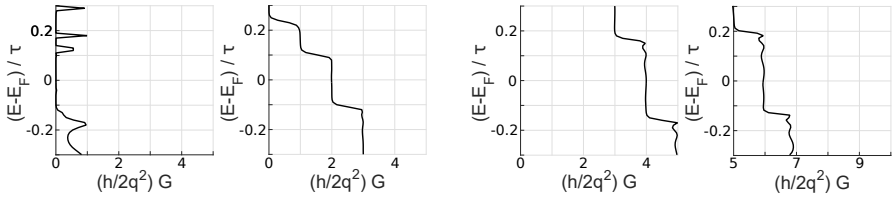



Figure 5.13: Conductance of a single G-QPC device. In (a), the two subfigures, from left to right, demonstrate the conductance of the device for input digit 0 ($-0.13V$) and input digit 1 ($-2.7V$) respectively. In (b), the two subfigures, from left to right, demonstrate the conductance of the device for input digit 2 ($-2.15V$) and input digit 3($-1.45V$) respectively

each digit, is represented by only one predefined conductance value. Moreover, changing the back gate voltage of one device, so as to move from one digit to the next or the previous one (i.e. from 2 to 3 or 1), corresponds to an equal change in conductance, as shown in Figure 5.13. This last property of the selected conductance levels eliminates the danger of error in case of additions with same result but different added digits, and makes the circuit scalable by allowing the simultaneous addition of n-bits. That can be achieved with the use of n G-QPC devices connected in parallel.

At this point, an advantage of using G-QPC devices for radix 4 addition is that, the parallel combination of such devices, creates more conductance levels than those available at a single device. More specifically, through the parallel connection of two G-QPC devices, results higher than 3 (the highest digit that a radix 4 numeral system can depict), can be encoded and represented, without further circuitry. Carry does not necessarily need special manipulation.

### 5.5.4 Simulation Results

In this section, numerical simulations of the G-QPC devices forming the Radix-4 adder circuit as discussed before are presented. The simulation results are expected to be in accordance with quaternary addition described in (KS & Gurumurthy, 2009) and show that the proposed circuit maps correctly an addition in a higher radix (4) numeral system.

As described above, the region of interest in those diagrams is a few $kT$ above and below $E = 0$, which corresponds to Fermi energy. In Fig. 5.13 conductance is depicted for a wide range of energies, from $E = -0.5$ to

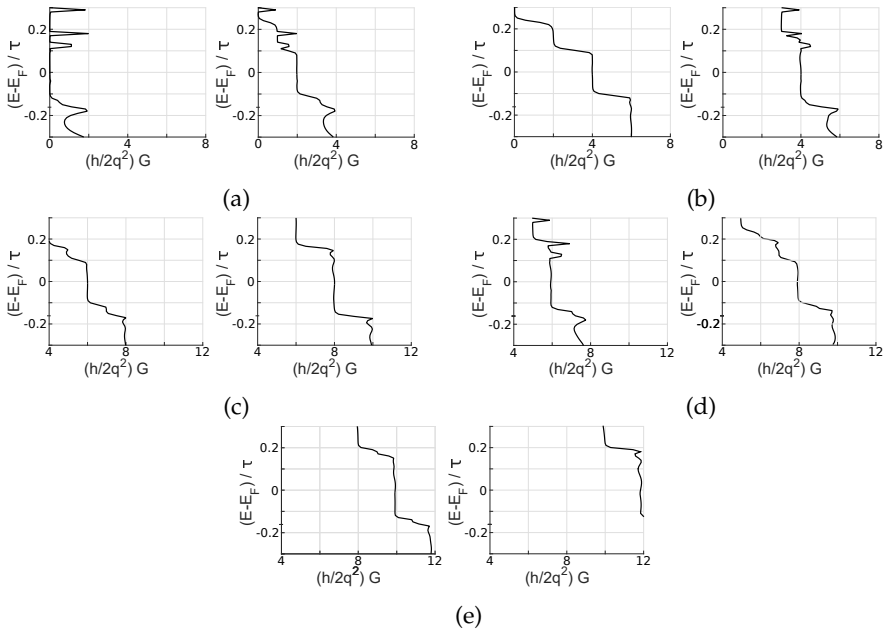



Figure 5.14: Conductance of the proposed circuit for every possible input combination for 2-digit addition. More specifically, from left to right are presented: In (a), operation $0+0$ and $0+1$. In (b), operation $1+1$ and $2+0$. In (c), operation $2+1$ and $2+2$. In (d), operation $3+0$ and $3+1$, and finally in (e), operation $3+2$ and $3+3$

$E = 0.5$ in units of $((E-E_F)/\tau)$, where $\tau = -2.7eV$ is the overlap integral for atoms that are nearest neighbors (Reich et al., 2002). However, the mean value of conductance and therefore the mean value of resistance, presented in Tab. 5.8, are calculated using values for a range of energies from $E = -0.1$ to $E = 0.1$ in units of $((E-E_F)/\tau)$. Also, in those figures, conductance ($x$-axis) is normalized. More precisely, $x$-axis corresponds to $Trace[\Gamma_L G^R \Gamma_R G^A]$.

In Fig. 5.14 the results of the proposed Radix-4 adder circuit are presented. The nature of the circuit implies that changing input 1 with input 2, and input 2 with input 1, would not bring any difference to the result, so only one of those calculations is depicted. For example, $0+1$ and $1+0$ have the same result, $1+2$ and $2+1$ have the same result, and so on. In all the subfigures presented in Fig. 5.14, the top gate voltage does not change, it is constant and its value is $V_{TG} = 0.07Volts$. The variable is back gate potential which determines the inputs, as mentioned above.

Table 5.8: The results of the simulations in numbers

| Calculations | Result | $R_{MEAN}$(Ohm) | Current(Ampere) |
|---|---|---|---|
| 0+0 | 0 | $2.6798 \cdot 10^{7}$ | $3.7316 \cdot 10^{-8}$ |
| 1+0 | 1 | $6.5291 \cdot 10^{3}$ | $1.5316 \cdot 10^{-4}$ |
| 1+1 | 2 | $3.2719 \cdot 10^{3}$ | $3.0564 \cdot 10^{-4}$ |
| 2+0 | 2 | $3.2443 \cdot 10^{3}$ | $3.0823 \cdot 10^{-4}$ |
| 2+1 | 3 | $2.1686 \cdot 10^{3}$ | $4.6112 \cdot 10^{-4}$ |
| 2+2 | 0 | $1.6238 \cdot 10^{3}$ | $6.1585 \cdot 10^{-4}$ |
| 3+0 | 3 | $2.1787 \cdot 10^{3}$ | $4.5900 \cdot 10^{-4}$ |
| 3+1 | 0 | $1.6343 \cdot 10^{3}$ | $6.1188 \cdot 10^{-4}$ |
| 3+2 | 1 | $1.3044 \cdot 10^{3}$ | $7.6662 \cdot 10^{-4}$ |
| 3+3 | 2 | $1.0901 \cdot 10^{3}$ | $9.1738 \cdot 10^{-4}$ |

Based on Tab. 5.7 for the inputs of the devices, the results are as expected, and show that the proposed circuit indeed maps a Radix-4 addition. It can be easily distinguished that the devices, in additions with the same result, irrespective of the inputs, are tuned so that the total conductance of the circuit is the same, and thus the current that will run through it, will also be the same.

The mean value of the adder's resistance for the energy region of interest has also been calculated, as mentioned above. This mean value is calculated for every possible 2 digit addition in a Radix-4 system, and is presented in Tab. 5.8. A source potential of $1Volt$ was applied for the calculation of the current that runs through the device. The current was calculated using the corresponding Ohm's law:

$$I = \frac{V_{SOURCE}}{R_{MEAN}} \tag{5.15}$$

Tab. 5.8 is an other view of the results shown in Fig. 5.14. The visualization of the table (Fig. 5.15) leads to the result that operations with the same result, indeed conduct the same amount of current through the device, while the current difference between consecutive results (i.e. between 1 and 2, 2 and 3 etc.) is almost the same. It is also obvious that the higher the result of the operation, the higher the current running through the device.

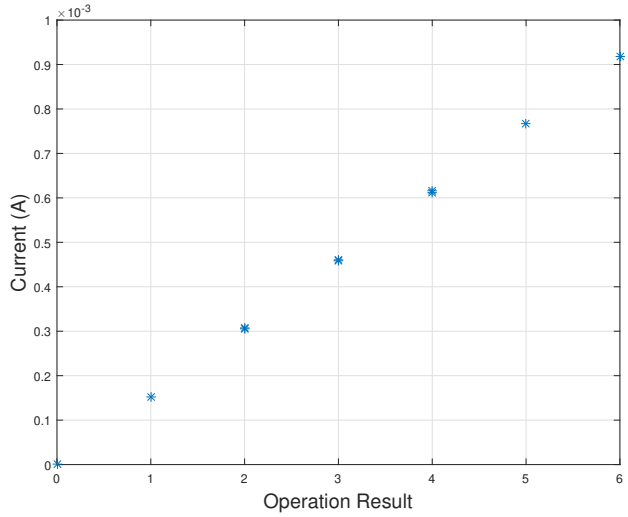



Figure 5.15: Visualization of Table 3.1. Shows the correlation between the current running through an adder, and the result of the computation

## 5.6 Conclusions

In this work, the special electronic properties of Graphene were leveraged, in order to present a set of re-configurable computing topologies. In this manner, two different but similar re-programmable comb-shaped GNR-based topologies were proposed. The first consists of 2 branches and is able to operate as an `AND`, an `OR`, a `NOT` and a `Buffer`, while the second consists of 3 branches and is able to operate as a 2-input `XOR` gate, a 3-input `XOR` gate, and a 3-input `Majority` gate, with appropriate biasing. As a proof of concept, a 1-bit full adder cell, based on the aforementioned 3 branch topology was also presented. Both proposed topologies work in a way similar to that of PTL circuits and, moreover, do not require back gate biasing in order to operate, allowing for a wider variety of applications. The effect of different dimensions of the topologies on their electronic properties was investigated and their dimensions and geometry were specified based on the results. The simulation method was enriched with capacitance calculations, that enable the analysis of the parasitics of the proposed device. Then, the operation of both the topologies as re-programmable logic gates was analytically exposed and the 7 in total different operation modes were explained, presenting as well a basic circuit element as a proof of concept. The operation of the 4 different logic gates based on the 2 branch topology

was verified through the gate biasing heatmaps, while the operation of the 3 different gates based on the 3 branch topology was evaluated using the energy dispersion to conductance diagrams in order to verify the conductance of each branch in every possible input combination and, thus, verify the truth table of every different gate. Finally, through the added features in the simulation, some key characteristics of the topology were estimated. The area footprint with a universal value of $1.384 \times 10^2 nm^2$ for the 2 branch topology and $2.532 \times 10^2 nm^2$ for the 3 branch topology, the propagation delay with a value of $2.054 \times 10^-2 ps$ for both topologies and the power dissipation at $10.204 nW$ in the worst case. The corresponding results were compared with metrics for complementary CMOS and state-of-the-art complementary GFET counterparts and showcased very competitive outcome and quite encouraging perspectives. This part of the work clearly indicates that GNR devices can be used as computing blocks with favorable characteristics and find application in PTL and re-configurable computing. Extending to that, the ability of GNR-based devices, and specifically of Graphene Quantum Point Conctact devices (G-QPCs) to be used in Multi-Valued Logic (MVL) applications was investigated. The ability of such devices to be tuned in different conductance levels through the application of back gate bias is showcased. Also, the correlation of the number of available conductance levels of the device with its dimensions is explained. Finally, as a proof of concept, a G-QPC device of specific dimensions is used to encode the digits of the radix 4 numeric system, and two of them are connected together to expose the possible operation of an arbitrary radix-4 adder.

# Chapter 6

# Conclusions and Future Work

## 6.1 Conclusions

In general, this dissertation deals with a wide spectrum of the challenges that appear in the incorporation of Graphene in electronics, ranging from the low level of device modeling and simulation, up to the high level of circuits and systems. It begins with a deep investigation of the models and methodologies for the simulation of Graphene and Graphene Nanoribbon sheets, in search for appropriate fitting on data from fabricated devices. Two types of models are available in the bibliography, the compact models, and the computational models. The compact models are capable of effectively describing the operation of devices that are based on larger-area Graphene sheets. Computational models are very accurate for smaller-size devices, in the regime of nanometers, where quantum phenomena become dominant and are very convenient for device engineering. However the latter, are computationally intensive and become challenging to be used for bigger size devices. For that reason, a hybrid methodology for expanding computational models, and specifically Non-Equilibrium Green's Function (NEGF), for the simulation of bigger-size devices has been proposed. Conductance values for small-scale devices are generated using the (NEGF) method and are employed to simulate the behavior of larger-scale devices. This scale adjustment is achieved here for the first time through a simple mathematical interface. That way, a complete robust and versatile tool for the simulation of GNR-based devices of a wide variety of dimensions is provided, where pure NEGF simulations can be employed for small-size devices and mathematically enhanced NEGF simulations for larger ones, in an attempt to bridge the gap between computational and compact models. The model accurately predicts the behavior of larger devices and this is demonstrated by fitting it to the experimental data of a back-gate Graphene

transistor developed by NCSR Demokritos. Its precision is proved to be remarkable with a mean Normalized Root Mean Square Error (NRMSE) of 1.83% across various cases. This approach actually outperformed the common circuit equivalent adapted from Umoh et al. (Umoh et al., 2013).

The analysis and corresponding results of this study are presented in the following work, which is under submission:

**(Vasileiadis et al., 2024)** Vasileiadis, N., **Rallis, K.**, Tselios, K., Samara, G., Papageorgiou, G., Kalaitzakis, F., Katsiaounis, S., Parthenios, J., Papagelis, K., Ioannou-Sougleridis, V., Normand, P., Karafyllidis, I., Rubio, A., Sirakoulis, G. C., & Dimitrakis, P. (2024). Graphene monolayer treated with UV irradiation for large area Graphene field-effect transistors by electron beam lithography. *Under Submission*.

Graphene's electronic properties are heavily based on the condition of its grid. In this dissertation, the NEGF-based simulation method is enhanced. The flexibility provided by Tight Binding Hamiltonians (TBHs) is exploited, and the method is now enabled to simulate Graphene grids that contain anomalies. Using this ability, an in-depth analysis is performed to examine the influence of structural defects on the functionality of Graphene. The investigation is concentrated specifically on its electronic properties by evaluating correlated metrics. For the first time, such evaluation is conducted on devices of variable shape, where defects can be found in different regions and at different concentrations. The results highlight that defects significantly impact the electronic behavior of devices, with the channel region being more adversely affected than the contact region. Both types of channel defects —edge and bulk— drastically lower the devices' maximum conductance. The configuration and symmetry of the edge defects are crucial, as conductance improves when edges are predominantly perfect zig-zag. Defects also disrupt the energy quantization seen in ideal, defect-free structures, except at edge defects on contacts. The presence of defects alters the energy gap; bulk defects at contacts widen the gap, whereas edge and channel defects may reduce it or leave it unchanged, potentially impairing device performance. Further analysis shows that defect density influences leakage current and the ON/OFF current ratio. Edge defects notably increase leakage current, while channel defects have a minimal impact. A new metric, current per defect, was introduced to evaluate this effect.

The analysis and the results of this study on the effect of defects on the electronic properties of Graphene, have been presented in the following publications:

**(Rallis et al., 2019)** **Rallis, K.**, Dimitrakis, P., Sirakoulis, G. C., Karafyllidis, I., & Rubio, A. (2019). Effect of lattice defects on the transport properties of graphene nanoribbon. *2019 IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, 1-2.

**(Rallis, Dimitrakis, et al., 2021)** **Rallis, K.**, Dimitrakis, P., Karafyllidis, I., Rubio, A., & Sirakoulis, G. C., (2021). Electronic properties of graphene nanoribbons with defects. *IEEE Transactions on Nanotechnology*, 20, 151–160.

**(Rallis, Dimitrakis, Sirakoulis, et al., 2022)** **Rallis, K.**, Dimitrakis, P., Sirakoulis, G. C., Rubio, A., & Karafyllidis, I. (2022). Current Characteristics of Defective GNR Nanoelectronic Devices. *Proceedings of the 17th ACM International Symposium on Nanoscale Architectures*, 1-6.

Having all that prior knowledge, the thesis shifted its focus to the circuit/system level. For this transition, the NEGF-based model has been imported into a SPICE simulator through look-up tables and Verilog-A. Closer to conventional computing circuits, a set of GNR-based comb-shaped topologies has been presented. These topologies exploit the capability of L-shaped GNRs to effectively operate as switches with the help of external application of electric bias through a combination of top gates and without the need for back gate biasing, broadening their application scope. The first, reduced size proposed topology, consists of 2 GNR branches and with appropriate biasing on its top gates, can operate as an `AND`, `OR`, and `NOT` gate, as well as as a `Buffer`. Its operation resembles that of Pass Transistor Logic, as the signals, apart from biasing its gates, also pass through the Graphene channels. It also leans on the principles of reconfigurable computing, as the same topology can encode the operation of all 4 aforementioned boolean gates, with an appropriate change of bias. The extension of this topology is a topology with 3 GNR branches, which can also operate as a 2-input and 3-input `XOR` gate and as a 3-input `Majority` gate. For the first time, the design and operation of a 1-bit full adder cell is presented, as a practical application of the aforementioned topology. The study through a design space exploration process, delves into the impact of topology dimensions on electronic properties, specifying dimensions and

geometry based on simulation results that include capacitance calculations for analyzing parasitics. The operational viability of these topologies as logic gates is confirmed through gate biasing heatmaps and energy dispersion to conductance diagrams, supporting their functionality. For the first time, key performance metrics are introduced, such as area footprint, propagation delay, and power dissipation are evaluated, showing competitive advantages over CMOS and other relevant complementary GFET technologies. The 2 GNR branch topology manages to achieve a constant area footprint of $1.384 \times 10^2$ while dissipating only $4.77nW$ for a single operation, with a delay as low as $2.054 \times 10^{-2}$ which leads to a significantly low energy-delay product (energy). The same goes for the 3 GNR branch topology, which covers a total area of $2.532 \times 10^2$ while dissipating only $10.204nW$ in the worst case, with a delay of $2.054 \times 10^{-2}$. Overall, the significant potential of graphene-based devices in advancing the field of re-configurable computing and logic gate design is underscored. As a proof of concept that GNR-based devices can be exploited in unconventional computation and mainly in beyond CMOS applications, the potential of butterfly-shaped Graphene Quantum Point Contact devices (G-QPCs) in Multi-Valued Logic (MVL) applications is explored, demonstrating the ability of a single device to be tuned to different conductance levels and encode digits for a radix-4 numeric system. The feasibility and operation of a radix-4 adder circuit employing two or more of these devices is reported.

All these results can be found in the following papers:

**(Rallis et al., 2018b)** **Rallis, K.**, Sirakoulis, G. C., Karafyllidis I., & Rubio, A. (2018). Multi-valued logic circuits on graphene quantum point contact devices. *Proceedings of the 14th IEEE/ACM International Symposium on Nanoscale Architectures*, 44–48.

**(Rallis, Sirakoulis, Karafyllidis, Rubio, & Dimitrakis, 2022)** **Rallis, K.**, Sirakoulis, G. C., Karafyllidis I., Rubio, A., & Dimitrakis, P. (2022). A Novel Graphene Nanoribbon XOR Gate Design. *2022 IEEE 22nd International Conference on Nanotechnology (NANO)*, 265–268.

**(Rallis, Dimitrakopoulos, et al., 2023)** **Rallis, K.**, Dimitrakopoulos, G., Dimitrakis, P., Rubio, A., Cotofana, S., Karafyllidis, I., & Sirakoulis, G. C. (2023). Novel Circuit Design Methodology with Graphene Nanoribbon Based Devices. *2023 IEEE 23rd International Conference on Nanotechnology (NANO)*, 708–712.

**(Rallis, Fyrigos, et al., 2023)** **Rallis, K.**, Fyrigos, I. -A., Dimitrakis, P., Dimitrakopoulos, G., Karafyllidis, I., Rubio, A., & Sirakoulis, G. C. (2023). A Reprogrammable Graphene Nanoribbon-Based Logic Gate. *IEEE Transactions on Nanotechnology*.

During the evolution of this thesis, there was involvement in several other publications, all relevant to Nanotechnology circuits and systems. The most relevant to the thesis, highly related to Graphene are the following:

**(Moysidis et al., 2020)** **Moysidis, S.**, Rallis, K., & Karafyllidis, I. (2020). Conductance parametric analysis of graphene nanoribbons with magnetic contacts. *IEEE Transactions on Nanotechnology 19*, 778–783.

**(Rallis, Moysidis, & Karafyllidis, 2021)** **Rallis, K.**, Moysidis, S., & Karafyllidis, I. (2021). Implementation of cellular automata using graphene nanoribbons with magnetic contacts *Cellular Automata: 14th International Conference on Cellular Automata for Research and Industry, ACRI 2020, Lodz, Poland, December 2–4, 2020, Proceedings 14*, 169-176.

Others, related to the field of Memristive devices and circuits can be seen below:

**(Tsipas et al., 2022a)** Tsipas, E., Chatzinikolaou T. P., Tsakalos K. -A., **Rallis, K.**, Karamani, R. -E., Fyrigos, I. -A., Kitsios, S., Bousoulas, P., Tsoukalas, D., & Sirakoulis, G. C. (2022). Unconventional Computing With Memristive Nanocircuits. *IEEE Nanotechnology Magazine*, 22–33.

**(Tsipas et al., 2022b)** Tsipas, E., Chatzinikolaou T. P., Tsakalos K. -A., **Rallis, K.**, Karamani, R. -E., Fyrigos, I. -A., Kitsios, S., Bousoulas, P., Tsoukalas, D., & Sirakoulis, G. C. (2022). Unconventional memristive nanodevices. *IEEE Nanotechnology Magazine*, 34–45.

**(Tsipas et al., 2023b)** Tsipas, E., Stavroulakis, E., Chatzipaschalis, I. K., **Rallis, K.**, Vasileiadis, N., Dimitrakis, P., Kostopoulos, A., Konstantinidis, G., & Sirakoulis, G. Ch. (2023). Modeling of memristor-based RF switches. *2023 12th International Conference on Modern Circuits and Systems Technologies (MOCAST)*, 1–4.

**(Tsipas et al., 2023a)** Tsipas, E., Stavroulakis, E., Chatzipaschalis, I. K., **Rallis, K.**, Vasileiadis, N., Dimitrakis, P., Kostopoulos, A., Konstantinidis, G., & Sirakoulis, G. Ch. (2023). Case study of a differential single-pole double-throw RF switch using memristors. *2023 IEEE 23rd International Conference on Nanotechnology (NANO)*, 703–707.

**(Stavroulakis et al., 2023)** Stavroulakis, E., Vasileiadis, N., Mavropoulis, A., Chatzipaschalis, I. K., Tsipas, E., **Rallis, K.**, Vourkas, I., Dimitrakis, P., & Sirakoulis, G. C. (2023). A TCAD model for silicon nitride based memristive devices. *2023 IEEE 23rd International Conference on Nanotechnology (NANO)*, 571–575.

**(Tsipas et al., 2023c)** Tsipas, E., Stavroulakis, E., Chatzipaschalis, I. K., **Rallis, K.**, Vasileiadis, N., Dimitrakis, P., Kostopoulos, A., Konstantinidis, G., & Sirakoulis, G. Ch. (2023). Novel materials and methods for fabricating memristors for use in RF applications. *2023 IEEE Nanotechnology Materials and Devices Conference (NMDC)*, 779–784.

## 6.2 Future Work

Graphene is a relatively new material and as it became clear during this dissertation, there is plenty of available space for further research considering many aspects, spanning from as low as the level of material and fabrication, up to the level of circuits, systems, and architecture with the use of GNR based devices.

First of all, in the field of modeling and simulation, there is plenty of room for further research related to the fabrication of Graphene in relation to the creation of defects and their effects. More specifically, the proposed framework for simulating defective GNRs can be further enhanced. In its current form, it can simulate 3 types of defects, single vacancy, double vacancy, and the change of carbon atoms within a graphene grid, with different types of atoms. However, those are not the only defects that can be present in a defective graphene grid. Different types of common structural defects are the Stoke Wales defect, as well as the grain boundary defect, which can be incorporated in the simulation framework to further expand its capabilities. Also, another significant part is the incorporation of corrugations in the NEGF simulation tool, which is already an active area of research (Bishnoi et al., 2022).

Apart from that and in the same path, the framework can be used as a moving force for the improvement of the fabrication process. The results of the simulation of defective grids can be compared with experimental measurements from fabricated devices, and through that comparison, there will be an estimation of the type, concentration, or location of defects that exist. Their correlation to specific fabrication processes can provide very useful insights on which of the processes causes specific damage to the structure of Graphene, help on providing a guideline on what needs to be fixed, and boost the area of GNR device fabrication.

Transitioning from the domain of fabrication and manufacturing to the field of circuits presents ample opportunities for additional research. As described in the previous chapters, defects are always present on a Graphene grid or a Graphene Nanoribbon, in varying quantities and qualities. Thus, Graphene-based devices have inherent stochasticity, which can be exploited for the implementation of security-related systems, such as Physically Unclonable Functions (PUFs) and True Random Number Generators (TRNGs), which are lately highly discussed subjects.

It is also obvious that the field of conventional and unconventional computing constitutes a fertile ground for additional exploration in the domain of Graphene-based devices and circuits. In this dissertation a complete set of Boolean gates has been proposed, that is able to implement every logic function. Therefore, this proposed architecture has the ability to constitute combinational logic circuits. In order to extend the capabilities of the proposed technology and transform it to a fully capable computing architecture, it is imperative to make some advancements in the field of memories. The goal of developing GNR-based non non-back-gated flip-flops will enable our proposed circuits to additionally implement sequential circuits. With the presence of all those fundamental cells, the focus can be expanded to the field of other basic blocks of computing circuits. The capability of the proposed computing topologies to adjust their behavior with a set of multiple top gates could be effectively exploited and lead to optimized designs of circuits such as Multiplexers (MUX). The same topologies also presented the ability to reconfigure their operation. In order to expand in a fully featured way on the field of reconfigurable computing, a systematic methodology of reprogramming must be investigated, that will enable a set of reconfigurable topologies to be programmed properly depending on the logic function that they need to replicate. Also, as mentioned before, the ability of GNR-based circuits to be CMOS compatible, either at a fabrication level or at a circuit level, is of existential significance and demands

comprehensive and analytical investigation.

To enable the design of circuits and finally production of monolithic chips on a broad scale, beyond a limited number of devices, further advancements in electronic design automation (EDA) are necessary. So there is room for research on the development of an EDA tool that will be able to effectively and optimally handle the technology mapping as well as other significant parts of the design flow, such as routing and placement. Significant know-how can be derived from EDA tools that have already been developed for conventional technologies, however, it is critical for those tools to be optimized based on the properties and unique characteristics of the new technology they are intended for.

Moving away from pure boolean logic, the use of GNR-based devices in other applications can be also investigated. As seen from conductance to energy dispersion diagrams throughout this dissertation, GNRs showcase a conductance quantization property. This property could be useful in the realization of mixed-signal circuits, such as Digital to Analog (DACs) or Analog to Digital converters (ADCs). The investigation of employing Graphene in those applications and the exploration of the properties of the resulting circuits can possibly expand the ability of GNR circuits to communicate with their environment. Combined with the biocompatible nature of Graphene, DACs and ADCs could enable near-cell logic through easy conversion of neural signals from the analog to the digital domain, or specific cell stimulation through conversion of digital signals to the analog domain.

Last but not least comes the investigation of the compatibility of GNR-based devices with unconventional computing applications. The ability of GQPC devices to operate in a multi-state manner was presented. In that essence, further investigation of their ability to be exploited in Multi-Valued Logic (MVL) circuits can be proven productive. Taken as an example the relatively known Quaternary Logic, a set of circuits and their operation can be evaluated, such as the Quaternary AND (QAND) and Quaternary OR (QOR) gates, a standard quaternary inverter (SQI) and many more. In the area of unconventional computing, GNR-based devices have been investigated as possible candidates for the realization of artificial neurons and synapses. This is a relatively new topic, that follows the current trends and shows significant potential.

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