UNIVERSITAT DE BARCELONA

On the use of multilayer hexagonal boron nitride as dielectric in micro/nano-electronic devices

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PhD thesis dissertation

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To my family,

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Abstract

Electronic devices are becoming increasingly essential for our work and life. The downscaling process of electronic devices, as well as the development of new devices for artificial intelligence and internet of things, are boosting the demand of advanced electronic devices. In this context, dielectric materials are essential building blocks of many electronic devices, as they enable key functionalities like capacitance and memristive effect.

Currently, the dielectric materials most employed by the semiconductor industry (such as high-k materials) face performance and reliability challenges that endanger the correct development of future memory and computing devices. For this reason, a new generation of dielectric materials is desired to overcome the current demands. Two-dimensional (2D) materials are considered promising candidates for next-generation electronic devices. In particular, hexagonal boron nitride (h-BN) is a 2D layered material with one of the largest band gaps (5.9 eV), which enables its use as gate insulator of a transistor or a resistive switching layer in memristors.

In this work, we study the dielectric performance of multilayer mechanically exfoliated h-BN stacks in several types of devices. First, we explore the performance of defect-free mechanically exfoliated multilayer h-BN as gate dielectric material. Second, we explore the performance of defect-rich multilayer h-BN stacks, produced via chemical vapor deposition (CVD), as resistive switching layer in memristors with vertical metal-insulator-metal (MIM) structure. And third, we have explored the performance of one-transistor-one-memristor (1T1M) cells – the building block of memristive circuits for information storage and computation – fabricated by connecting a molybdenum disulfide (MoS_2) transistor to a h-BN memristor.

In this doctoral thesis, we present valuable data to understand the properties of h-BN, as well as its potential for applications in the field of micro/nano-electronics. The data contained in this document may be of great help of other researchers and engineers devoted to the development of post-silicon electronics, and they should contribute to a faster development of such technologies for the benefit of mankind.

Abstract in the official language

Els dispositius electrònics són cada cop més essencials per a la nostra feina i la nostra vida. El procés de miniaturització dels dispositius electrònics, així com el desenvolupament de nous dispositius per a la intel·ligència artificial i l'internet de les coses, estan augmentant la demanda de dispositius electrònics avançats. En aquest context, els materials dielèctrics són components essencials de molts dispositius electrònics, ja que permeten funcionalitats clau com la capacitat i l'efecte memristiu.

Actualment, els materials dielèctrics més utilitzats per la indústria dels semiconductors (com els materials d'alta permitivitat) s'enfronten a reptes de rendiment i fiabilitat que posen en perill el desenvolupament correcte de futurs dispositius de memòria i informàtica. Per aquest motiu, es necessita una nova generació de materials dielèctrics per superar les exigències actuals. Els materials bidimensionals (2D) es consideren candidats prometedors per a dispositius electrònics de nova generació. En particular, el nitrur de bor hexagonal (h-BN) és un material en capes 2D amb una de les bandes prohibides més grans (5,9 eV), que permet el seu ús com a aïllant de porta d'un transistor o una capa de aïllant resistiva en memristors.

En aquest treball, estudio el rendiment dielèctric de multicapes de h-BN exfoliades mecànicament en diversos tipus de dispositius. En primer lloc, explorem el rendiment del h-BN multicapa exfoliat mecànicament sense defectes com a material dielèctric de la porta. En segon lloc, explorem el rendiment de les piles h-BN multicapa riques en defectes, produïdes mitjançant deposició química de vapor (CVD), com a capa de commutació resistent en memristors amb estructura vertical metall-aïllant-metall (MIM). I en tercer lloc, hem explorat el rendiment de les cèl·lules d'un transistor-un-memristor (1T1M), el bloc més empleat per a la construcció dels circuits memristius per a l'emmagatzematge i la computació d'informació de dades, fabricades connectant un transistor molibden disulfur (MoS_2) a un memristor h-BN. En aquesta tesi doctoral presentem dades valuoses per entendre les propietats de l'h-BN, així com el seu potencial d'aplicacions en el camp de la micro/nanoelectrònica.

Les dades contingudes en aquest document poden ser de gran ajuda per a altres investigadors i enginyers dedicats al desenvolupament de l'electrònica post-silici, i haurien de contribuir a un desenvolupament més ràpid d'aquestes tecnologies en benefici de la humanitat.

Chapter 1: General introduction

1.1. Introduction

1.1.1. Introduction of dielectric materials

Materials are categorized into conductors, semiconductors, and insulators based on their electrical conductivity characteristics. A dielectric material is a specific type of insulator that, while non-conductive, becomes polarized when exposed to an external electric field [1]. The attributes of dielectric materials encompass electric susceptibility, dielectric polarization, electric dipole moment, electronic polarization, relaxation time, dielectric dispersion, and dielectric breakdown [1]. When selecting an appropriate dielectric, several parameters should be taken into account, such as a favorable dielectric constant, high dielectric strength, a low loss factor, stability at elevated temperatures, long-term storage stability, responsive frequency characteristics, and compatibility with industrial manufacturing processes [2].

Dielectric materials can be broadly classified into three categories based on their physical states: solid, liquid, and gaseous dielectrics. Regardless of their form, each type of dielectric material possesses distinct applications and properties. For instance, glass, a solid dielectric, was utilized in the creation of the Leyden jar, which is considered the first capacitor [3]. This pioneering development spurred further exploration and discovery of new dielectric materials and their potential uses. Solid dielectric materials, such as mica [4,5], various polymers [6,7], and oxides including perovskite oxides, silicon dioxide (SiO_2), aluminum oxide (Al_2O_3), and hafnium dioxide (HfO_2), are integral components in the construction of transistors, capacitors, and dielectric layers within a wide array of electronic devices [8-11]. Liquid dielectric materials, including mineral oils and deionized water, are valued for their insulating capabilities and are commonly employed in high-voltage electrical equipment [12-14]. Dry air, a fundamental gaseous dielectric, serves as a dielectric medium in capacitors [15]. The versatility of dielectric materials in their solid, liquid, and gaseous forms underscores their indispensable role across various technological applications, highlighting the significance of ongoing research and innovation in this field.

Among the dielectric properties, dielectric constant and dielectric strength are the most used parameters to evaluate the materials' dielectric property. Dielectric constant reflects the ability of materials to store charges and also can express the ability to hold electric flux in it. The dielectric constant formula is:

$$K = \varepsilon/\varepsilon_0$$

K is the dielectric constant; ε is the permittivity of substance; ε_0 is the permittivity of free space [16].

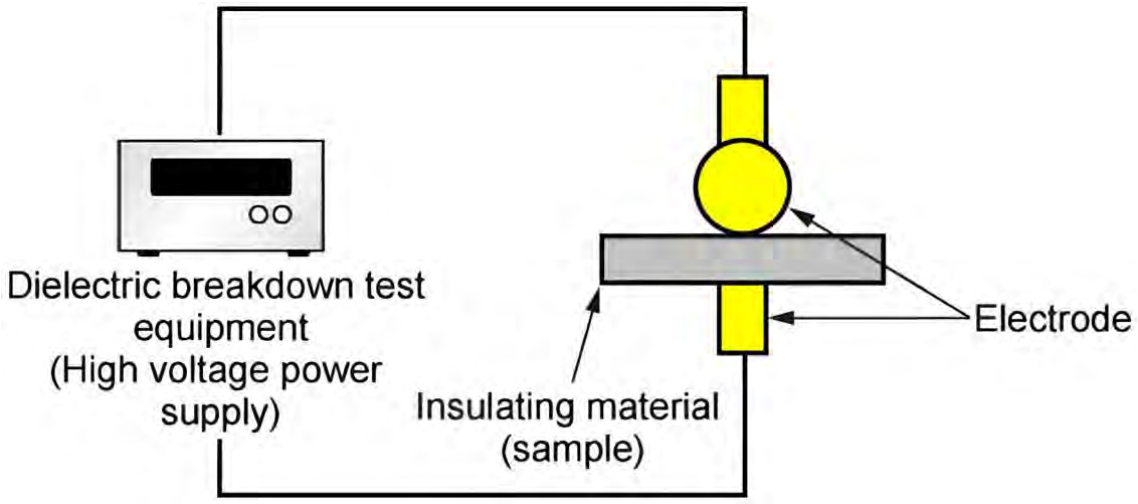

Figure 1.1 Dielectric strength measurement illustration [17].

Dielectric strength refers to the maximum voltage that a dielectric material can withstand before experiencing dielectric breakdown. The assessment of this property is conducted through a specific testing procedure where the dielectric material is positioned between two electrodes in an ambient air environment, as depicted in Figure 1.1. The process involves the incremental application of voltage across the electrodes. The voltage applied gradual increase continues until a point is reached where there is a sudden and significant surge in current flow. The precise voltage level at which this dramatic current increase occurs is designated as the breakdown voltage. This critical threshold is a crucial metric in evaluating the performance and reliability of dielectric materials in electrical insulation applications. The dielectric strength is calculated via the following equation:

$$D = E/d$$

D is the dielectric strength; E is the breakdown voltage; d is the thickness of dielectric materials [17].

Dielectric materials, renowned for their distinctive electrical properties, are extensively utilized across a multitude of industries. They are frequently employed in electronic devices, notably as components of capacitors [18-20], and in the construction of radio frequency transmission lines [21]. Mineral oils, a type of dielectric material, serve dual purposes as insulators and cooling agents within transformers [22] and data centers [23]. Additionally, dielectric materials find applications in resonators [24], tunable microwave devices [25, 26], and liquid crystal displays [27], showcasing their versatility and significance in modern technology.

1.1.2. Application of dielectric materials in electronic devices

Dielectric materials play a crucial role in the construction and functionality of a variety of electronic devices. Polymers [28-30], inorganic substances [31-33], hybrid composites [34,35], and a range of other dielectric materials are harnessed to fabricate these technological components. Among their many applications, dielectrics are particularly crucial in capacitors, and transistors. These uses underscore the indispensable nature of dielectric materials in the realm of electronics, highlighting their contribution to the performance and reliability of modern electronic devices.

A dielectric capacitor consists of two conductive metal electrodes that are insulated from each other by a dielectric layer. Charging occurs when an external voltage induces polarization within the dielectric layer, causing dipoles to align with the electric field and leading to charge accumulation on the electrode surfaces. The energy storage capacity of these capacitors is determined by the polarization and capacitance of the dielectric material, as well as the magnitude of the applied electric field, with these factors collectively impacting the capacitor's performance and energy-storing efficiency [36].

Dielectric capacitors are renowned for their exceptional high-power density, which can reach up to the megawatt range, and their swift response times, typically less than 100 microseconds. This performance is attributed to their unique method of energy storage, which involves the creation and utilization of electrostatic fields through the processes of dielectric polarization and depolarization [37-42]. In addition to their impressive power capabilities, dielectric capacitors also offer several other distinct advantages. These include a straightforward design, the ability to operate at high voltages exceeding thousands of volts, a broad operating temperature range, an all-

solid-state construction, enhanced safety features, and an extended cycle life. These attributes have positioned dielectric capacitors as a versatile solution across a variety of sectors and applications. Notably, they are increasingly being utilized in smart power transmission systems, pulsed electronics, emerging energy technologies, hybrid electric vehicles, and advanced military equipment, meeting a diverse array of requirements in these fields [43-52].

The transistor exemplifies a prevalent application for dielectric materials, particularly in the form of a gate dielectric. SiO_2 has been a foundational dielectric in silicon-based electronic devices from the early stages [53], favored for its exceptional attributes such as seamless integration with silicon, straightforward manufacturing processes, and affordability [54]. Nonetheless, the relatively low dielectric constant of SiO_2 poses limitations in its use within transistors. For instance, at the 90 nm node of transistor technology, a SiO_2 layer as thin as 1.2 nm is employed as the dielectric [55]. The trend toward device miniaturization necessitates even thinner dielectric layers, which, in turn, can lead to an increase in leakage current [55].

To address this challenge without compromising the miniaturization of transistors, the industry has turned to novel dielectric materials with a dielectric constant exceeding that of SiO_2 ($k \approx 3.9$). These advanced materials, known as high-k materials, encompass a variety of compositions such as metal oxides [56,57], nitrides [58], perovskites [59], and organic dielectrics [60]. Figure 1.2 illustrates the ideal characteristics for high-k materials, with a selection of prominent oxides charted according to their dielectric constant and energy bandgap, offering a visual representation of their properties for comparison and selection in transistor design.

Among the array of high-k materials, HfO_2 emerged as the choice for the first generation of complementary metal oxide semiconductor (CMOS) technology [62], favored for its elevated dielectric constant ($k \approx 19$) and its capacity to mitigate leakage current [63]. Despite these advantages, the transition from SiO_2 to high-k materials still has some challenges [64,65]. Key issues include: i) An increase in material defects during the metal oxide deposition process, which can compromise the stability of device performance; ii) The potential for reaction with the silicon substrate, leading to the formation of an additional SiO_2 layer; iii) A reduction in carrier mobility due to phonon scattering in the channel region; iv) The risk of poly crystallization, which can degrade homogeneity and increase variability.

As CMOS technology continues to evolve, there is a growing demand for dielectric materials that can surpass the performance limitations of even high-k materials, offering enhanced stability, reduced defects, and improved compatibility with existing semiconductor processes.

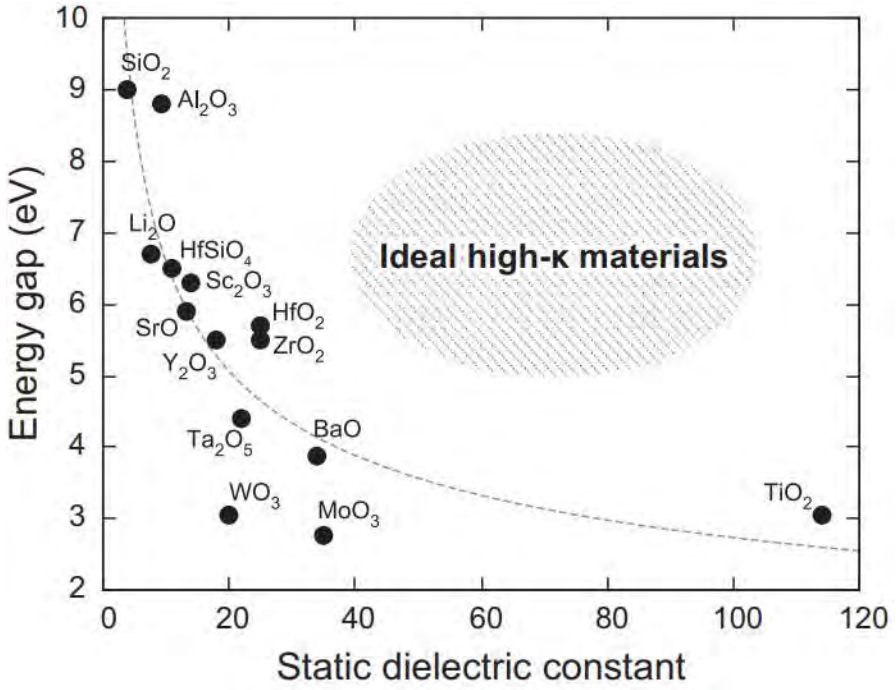

Figure 1.2 Experimental dielectric constant and bandgap for well-known oxides [61].

Dielectric materials play an important role in the construction of capacitors within memory devices, particularly in dynamic random-access memory (DRAM) [66]. In emerging memory devices, dielectric materials can also be used as a switching medium layer in two-terminal memory devices called memristors [67,68]. For example, the typical high-k materials, HfO_2, can work as a switching layer in memory devices [69-71] with impressive performance.

1.1.3. 2D materials for next-generation electronic devices

The development of the semiconductor industry and increasing demand for high-performance hardware for emerging data-based industries (such as deep learning, the Internet of Things (IoT), and in-memory computing [72,73]), requires Si-based CMOS technology enhanced performance, which are often related to device miniaturization. This generates challenges like short channel effects, leakage current increasing, high-power consumption, and high contact resistance [74,75]. When the thickness of the

semiconductor decreases to 5 nm due to the surface dangling bonds and high roughness, the scattering of internal charges increases, leading to a sharp decrease in mobility (μ) [76,77]. In memory devices, defects will be uncontrolled when the metal oxide dielectrics thickness is reduced to 3 nm [78]. Novel materials and devices are required when the Si-based integrated circuit (IC) industry reaches its physical limitation [79].

After the discovery of graphene in 2004 [80], a new kind of material called 2D) materials attract interest for their application in the electronic region due to their unique structure, physical and electric properties. For example, 2D materials are layered structures connected via the weak van der Waals force, indicating that 2D materials can approach single atomic thin sheets in the application of vertical and planner electronic devices [81]. This characteristic aligns perfectly with the demand for the progressive miniaturization of next-generation electronic devices, particularly in terms of their thickness dimensions [82]. Other unique properties such as dangling free of the atomically flat surface, easy stacking on other materials, high transparency [83], and excellent electric performance [84-87] make 2D materials a promising candidate for the application of next-generation electronic devices.

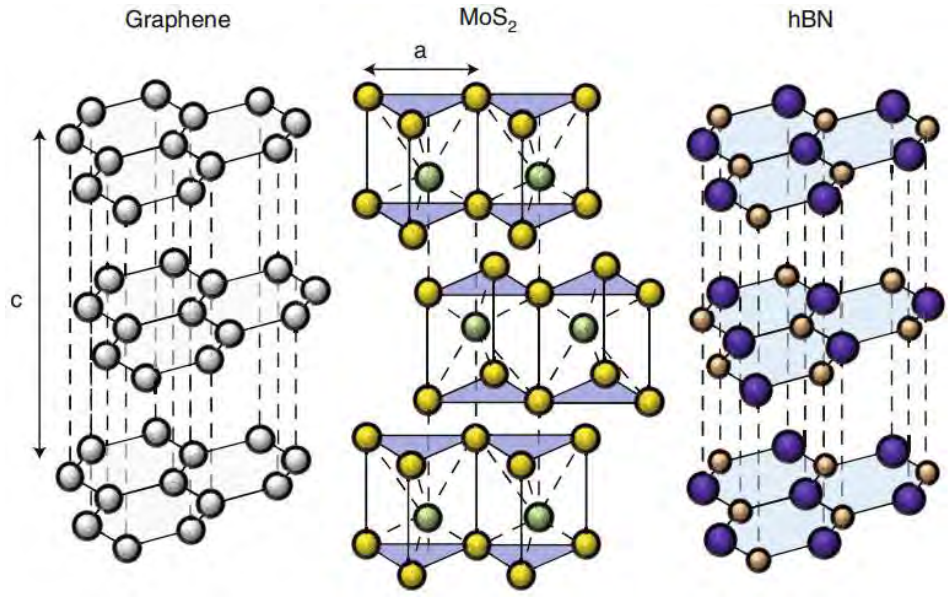

Figure 1.3 Example of metallic, semiconducting, and insulating 2D materials from left to right [88].

2D materials exhibit a spectrum of conductive properties, which can be neatly divided into three categories: conductors, semiconductors, and insulators. This classification is visually represented in Figure 1.3, progressing from left to right.

Graphene stands out as a quintessential example of a conductive 2D material, characterized by its lack of a bandgap [89]. This unique trait positions graphene as an ideal candidate for conductive electrodes, offering a compelling alternative to traditional metal electrodes [90]. The exploration of 2D materials extends to metallic transition metal dichalcogenides (TMDs), which display intriguing metallic properties. For instance, Zhao et al. employed the CVD technique to grow 2D niobium disulfide (NbS_2) on a h-BN substrate, revealing that NbS_2 retains its metallic nature even when reduced to just three layers [91]. A comprehensive review delves into a broader range of 2D metallic TMDs and their metallic characteristics, shedding light on their potential applications and properties [92].

Semiconductor 2D materials include most TMDs materials, such as MoS_2 [93,94], tungsten disulfide (WS_2) [95], and tungsten diselenide (WSe_2) [96], etc. TMDs materials present a unique combination of properties, including atomic-scale thickness, direct bandgap, and electronic features that make them attractive to the field of electronic devices [97]. The most widely studied application of semiconductor TMDs in the electronics region is their use in transistors as channel materials due to their suitable bandgap [98]. MoS_2 is the most studied TMD material due to its robustness and the availability of raw materials in nature [97]. For example, a MoS_2-based transistor with a 1 nm wide gate electrode displays a sub-threshold swing (SS) of approximately 65 mV/decade and a large current on/off ratio of approximately 10^6 [99]. Tian et al. fabricated a side-wall transistor where the thickness of the monolayer MoS_2 serves as the channel length. These transistors, with an atomic scale channel length, exhibit a current on/off ratio of about 1.02×10^5 and a subthreshold swing of around 117 mV/dec [100].

Ultimately, h-BN stands out as the most extensively studied insulating material within the realm of 2D materials. Recognized for its role as a stable dielectric, coupled with its atomically flat surface and lack of dangling bonds, h-BN is exceptionally well-suited for use as either a substrate or a protective layer in electronic devices that incorporate other 2D materials. The combination of its insulating nature and its ability to provide an atomically smooth surface ensures compatibility and enhances the performance when paired with other 2D materials.

For instance, employing h-BN as a substrate in graphene-based electronics significantly boosts electron mobility, increasing from 10,000 cm^2/Vs when on SiO_2substrates [101] to an impressive 60,000 cm^2/Vs [102]. This enhancement, along

with the observed improvement in carrier inhomogeneities [103], underscores the material's potential to refine electronic properties. Further encapsulation of CVD-grown graphene between h-BN layers—a technique that sandwiches the graphene between two h-BN flakes—yields even more remarkable results, with electron mobility soaring to 350,000 cm^2/Vs [104] and an astounding 500,000 cm^2/Vs [105]. These advancements not only showcase the effectiveness of this optimization approach but also highlight the reliability of h-BN as an encapsulating material.

Similar improvements in device performance are mirrored in the case of encapsulated MoS_2 transistors. Here, the mobility of the transistors is observed to increase to 34,000 cm^2/Vs at low temperatures [106], with a concurrent enhancement in performance stability [107]. These findings underscore the broad applicability of h-BN as a means to optimize and stabilize the performance of various 2D material-based electronic devices

h-BN can also work as a functional material, such as switching layer in memristors to enhance storage density [108], or construct oscillatory neural network to solve optimization problems [109].

In addition to h-BN, some novel insulating 2D materials, such as calcium fluoride (CaF_2), strontium titanate ($SrTiO_3$), and bismuth selenite (Bi_2SeO_5) are studied and display inspired dielectric performance. CaF_2 is used as gate dielectric in MoS_2 field effect transistor (FET) and the FET exhibits low leakage current, low subthreshold swing (90 mV/dec), high on/off ratio (10^7), and small hysteresis [110]. $SrTiO_3$ as a well-known perovskite oxide material with good insulation and high dielectric constant is used as the gate dielectric in tin dioxide (SnO_2) thin film transistors presenting low operation voltage [111]. Encapsulation with Bi_2SeO_5 significantly improve the Hall mobility of bismuth oxyselenide (Bi_2O_2Se) nanosheets device from 43,000 $cm^2\ V^{-1}\ s^{-1}$ to 470,000 $cm^2\ V^{-1}\ s^{-1}$ at 1.8 K [112].

All thin-film transistors utilizing 2D materials have been masterfully demonstrated by Das and colleagues. In their construction, they employed monolayer graphene for metal electrodes, 3-4 layered h-BN as the dielectric material, and bilayer WSe_2 as the channel material. This all-2D-based transistor showcases a remarkably high on/off ratio of 10^7 and an impressively low subthreshold swing of 90 mV/dec [113]. This all 2D-based transistor demonstrates that 2D materials have vast potential in electronic devices.

Aside from the electric properties of 2D materials, the physical property such as high mechanical strength, flexible and transparent features make 2D materials

promising in flexile and wearable electronic devices. For example, monolayer MoS_2 is used to fabricate flexible transistors with low channel length (~60 nm) and exhibits high ~470 μA/μm at low source/drain voltage (1 V) [114]. Wearable electronic devices based on 2D materials such as energy harvesting and biomedical sensors are discussed in [115] and [116], respectively.

2D materials can act as any role in the IC industry, including conductors, semiconductors and insulators and their impressive performance in traditional and novel electronic devices indicates that 2D materials are promising candidates to fabricate next-generation electronic devices.

1.1.4. Introduction of h-BN

The h-BN structure is shown in Figure 1.3, and its experimental annular dark-field (ADF) phase images are presented in Figure 1.4 with high resolution. The ADF image exhibits the different intensities of boron (B) and nitrogen (N) atoms (bright points are N atoms, dark points are B atoms), and the phase image displays the hexagonal structure of the monolayer h-BN. In this structure, the hexagons consisting of boron and nitrogen atoms are clearly exhibited. This hexagonal structure is similar to that of graphene. The lattice mismatch between graphene and h-BN is low, at approximately 1.7% [118], indicating that h-BN can be an excellent substrate for graphene. Each layer of h-BN is composed of boron and nitrogen atoms, which are interconnected through robust covalent bonds. Despite this strong intralayer bonding, the interlayer forces in h-BN are comparatively weak, which allows for the existence of h-BN in the form of individual layers that are only atomically thin. The thickness of each layer of h-BN is around 0.33 nm, which is beneficial for minimizing the size of electronic devices in the vertical direction.

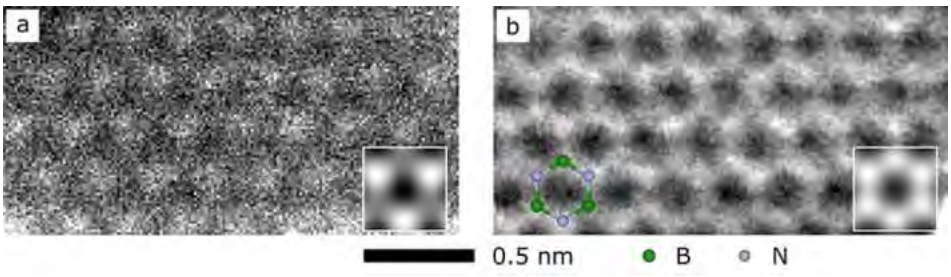

Figure 1.4 Experimental ADF and phase images of monolayer h-BN [117].

Among 2D materials, h-BN is recognized as an insulating material with an extensive bandgap of approximately 5.9 eV [119,120]. The dielectric constant of h-BN is around 3, which varies depending on the direction (in-plane or out-of-plane) and the number of layers [121]. In terms of dielectric breakdown strength, CVD-grown h-BN and exfoliated h-BN exhibit values of 1.5 MV/cm [122] and 12 MV/cm [123], respectively. Owing to h-BN's distinctive attributes, including its wide bandgap, atomically flat surfaces, and the absence of dangling bonds, h-BN layers are well-suited to serve as substrates in electronic devices and/or as encapsulating layers [124,125] for devices based on 2D materials.

Additional physical properties of 2D h-BN, such as its mechanical strength [126], high thermal conductivity [127], temperature stability [128], flexibility [129,130], and high transparency [131], further expand its potential applications in functional coatings, composite materials [132], and wearable electronic devices [133]. h-BN also finds use as a reinforcing agent [134] or as a gas barrier filler [135] in polymer composites. Its utility in electronic devices is further highlighted by its role as a dielectric material in capacitors [136], a gate dielectric in planar graphene-based photodetectors [137], an insulator in memristors [138-140], and as a medium layer in resistive switching devices [141]. With its unique features, 2D layered h-BN holds substantial promise for a variety of innovative applications.

1.1.5. h-BN production

Due to its exceptional performance in electronic devices, the production of h-BN is a critical aspect of its practical application. Traditionally, the fabrication of 2D materials can be achieved through either a top-down or bottom-up approach. The process of extracting 2D materials from bulk precursors is referred to as the top-down method. This methodology encompasses techniques such as mechanical exfoliation (ME), liquid-phase exfoliation (LPE), and chemical etching, among others. In contrast, the bottom-up method involves the synthesis of 2D materials by assembling them from atomic or molecular building blocks into layered structures. Common bottom-up techniques include CVD, physical vapor deposition (PVD), and molecular beam epitaxy (MBE).

Initially, we will discuss the top-down approach, detailing various strategies for procuring h-BN materials. This involves the exfoliation of h-BN flakes or nanosheets

from bulk boron nitride materials, leveraging methods that allow for the transition from a three-dimensional bulk material to a two-dimensional material with desirable electronic properties.

The first top-down method we will introduce is mechanical exfoliation, which is the method that found graphene and initiated 2D materials research. As Figure 1.5a shows, the material is peeled off through the tape, and ultimately, a few or single layers of h-BN will be obtained on the tape [142]. The drawback is that there is no standard way to achieve accurate thickness with low yields, time-consuming processes, and small-area h-BN (several nanometer thicknesses and hundreds of micrometers in size) [143]. However, the h-BN exfoliated has the best quality with fewer native defects [144] than that of h-BN obtained from other methods. The mechanically exfoliated h-BN flakes can be transferred to a precise location via a dry transfer.

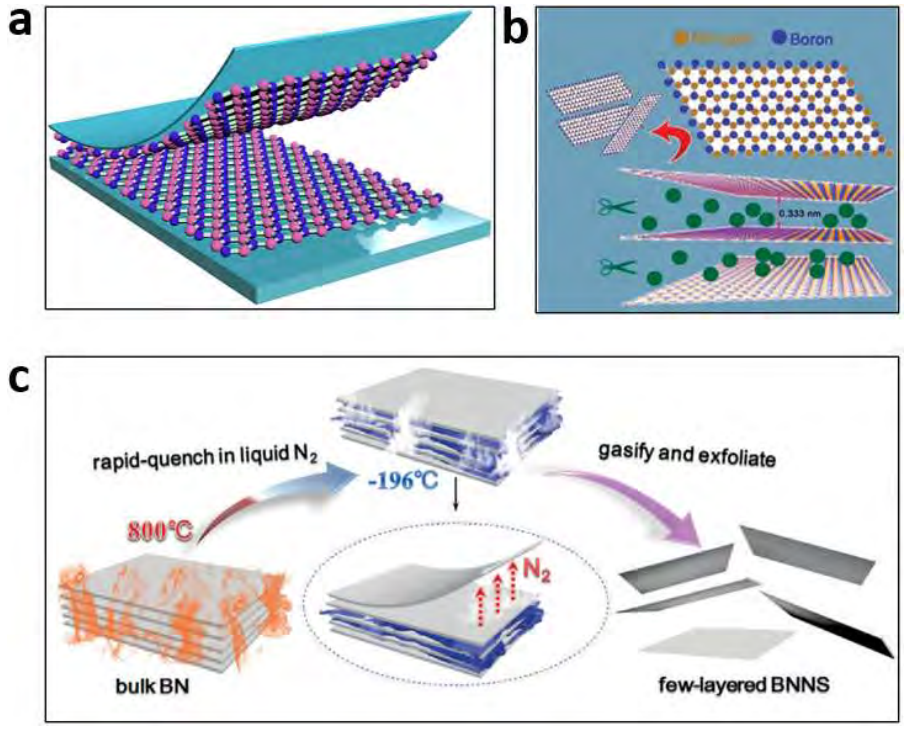

Figure 1.5 Exfoliation of h-BN from bulk to layers (a) Mechanical exfoliation with tape [142]. (b) Liquid-phase exfoliation using sonication and centrifugation in IPA (green spheres) [146]. (c) Gas exfoliation method [148].

Liquid-phase exfoliation is another extensively utilized technique for the production of 2D nanosheets. This method offers greater efficiency compared to mechanical exfoliation [145], and the process is depicted in Figure 1.5b. Bulk h-BN

crystals are transformed into 2D nanosheets through a combination of sonication and centrifugation within isopropanol (IPA) [146]. Zhu et al. have illustrated that h-BN layers exfoliated through liquid-phase processes exhibit high capacitance and minimal current leakage. These characteristics enable the achievement of an impressive mobility of 7,100 cm^2/Vs in graphene transistors that employ h-BN as a gate insulator [147]. Furthermore, Zhu et al. have also employed a gas exfoliation method to produce thin h-BN flakes, as showcased in Figure 1.5c. This approach primarily yields 1-5 layered nanosheets with lateral dimensions ranging from 50 to 500 nm [148].

Following a bottom-up approach, we can also synthesize h-BN films via CVD. Copper (Cu) foil [149-153] is the mostly used substrate in CVD-grown of h-BN because of its catalyst, feasible surfaces, low cost and available for mass production, although other metal substrates are also being investigated, such as nickel (Ni) [154-156], platinum (Pt) [157,158], and iron (Fe) [159]. The CVD process is illustrated in Figure 1.6. Ammonia borane (NH_3BH_3) is used as the precursor and decomposes by heating it at 55-120 °C. Then, the decomposed precursor flows into the chamber with a mixed hydrogen/argon (H_2/Ar) gas and reacts on the Cu foil, previously heated at 1000 °C, to form a h-BN layer [160]. However, the metal-assisted CVD growth can potentially limit the thickness of h-BN due to the catalytic metal being isolated from the first or few layers of h-BN [161]. Some publications describe the synthesis of h-BN directly on a dielectric substrate, like amorphous quartz [162], sapphire [163], and silicon carbide (SiC) [164], without the assist of metal. Other growth methods, such as metal-organic chemical vapor deposition (MOCVD) [165,166] and MBE [167-169] are also under study, but their high costs make them currently less effective for practical applications. More efforts are needed to explore the synthesis of h-BN via the CVD method to achieve large scale production with uniform and controllable quality.

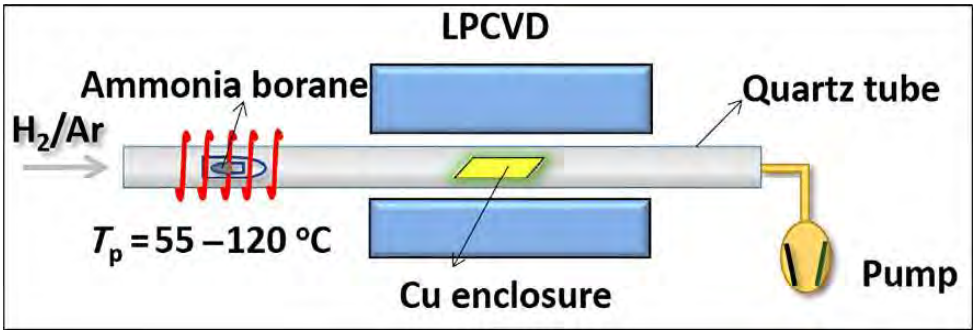

Figure 1.6 CVD synthesis of h-BN on Cu foil [160].

PVD is an additional method employed for the growth of h-BN. Techniques such as magnetron sputtering [170] and ion beam sputtering [171,172] are typical PVD approaches to fabricate h-BN films. The operational principle of the sputtering process is illustrated in Figure 1.7. Initially, a high-vacuum environment is essential to prevent contamination during the deposition process. Ar is introduced into the chamber as the sputtering gas and is ionized by an electric field to generate plasma. N_2 is also introduced into the chamber as a reactive gas, facilitating the formation of the h-BN film. The argon ions are accelerated towards a negatively biased boron target. These energetic argon ions impact the boron target, transferring momentum through collisions and dislodging atoms from the surface. Prior to reaching the substrate, the sputtered boron atoms react with nitrogen, yielding a boron nitride film on the substrate's surface. This process, which includes the reaction between boron and nitrogen, is known as reactive magnetron sputtering.

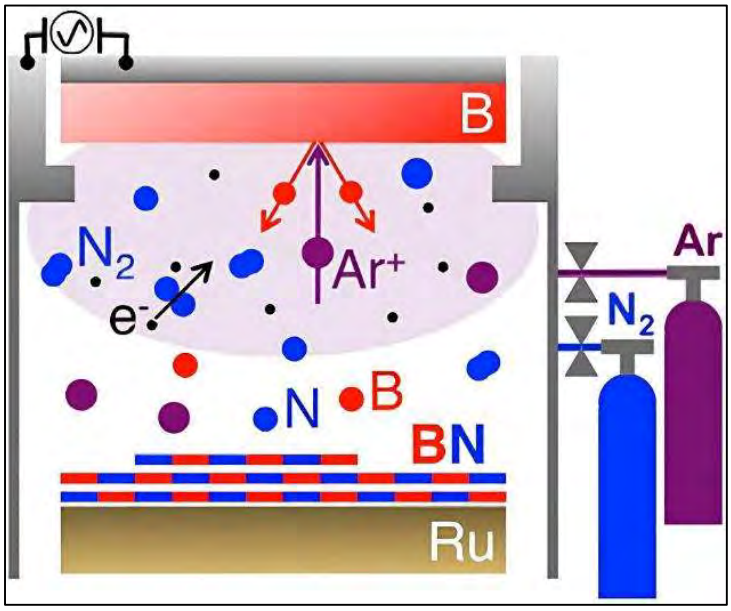

Figure 1.7 PVD method to fabricate h-BN films [170].

1.1.6. h-BN application in electronic devices

The dielectric property of h-BN is studied via a conductive atomic force microscope (CAFM) and at the device level, demonstrating its reliability as a dielectric material without issues such as charge trapping and de-trapping, stress-induced leakage current, and premature dielectric breakdown [173]. h-BN can be used as a gate dielectric in transistors. As shown in Figure 1.8, Zou et al. used h-BN as both the gate

dielectric and encapsulation layer in MoS_2 transistors, and the devices can survive at a much higher temperature (550°C) than ever reported [174]. In a h-BN/graphene/h-BN heterostructure field-effect transistor, the h-BN also serves as an encapsulation layer and gate dielectric, with the charge carrier mobility in the range of 30,000 to 36,000 cm^2/Vs at room temperature [175]. Since the carrier mobility is enhanced when a 2D semiconductor is placed on an h-BN layer, Liao et al. designed a hybrid top gate dielectric, an h-BN/HfO_2 stack, for a MoS_2 transistor [176]. The fabricated devices with this hybrid dielectric exhibit enhanced mobility and superior gate control. The carrier scattering induced by the underlying substrate is also suppressed by the h-BN/HfO_2 dielectric.

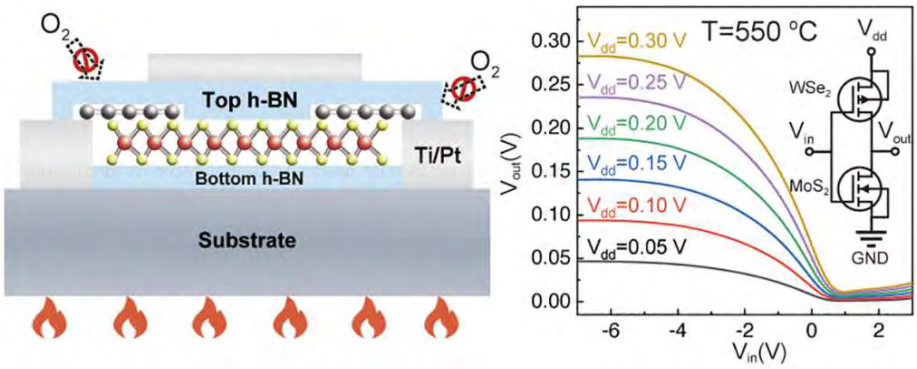

Figure 1.8 h-BN as gate dielectric and encapsulation layer in MoS_2 transistor [174].

In addition, h-BN can also be used in some emerging electric applications, such as resistive switching (RS) devices [177], random telegraph noise (RTN) devices [178-181], heterostructure devices [182-185], and so on.

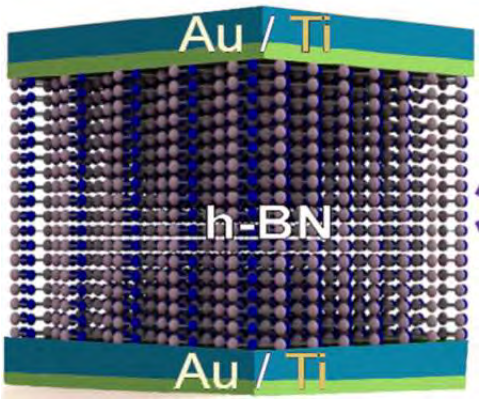

Figure 1.9 Schematic of typical resistive switching devices based on multilayer h-BN. Materials from top to bottom are Au/Ti/h-BN/Ti/Au [186].

RS devices typically exhibit a MIM structure, wherein insulating materials serve as the switching layer sandwiched between two conductive electrodes (as depicted in Figure 1.9 [186]). These devices have garnered significant interest due to their potential application as memristors [187]. Within RS devices, the resistance can be modulated reversibly between a high resistance state (HRS) and a low resistance state (LRS), contingent upon the application of an appropriate bias [188]. The HRS and LRS are analogous to digital 0 and 1, respectively, suggesting that RS devices are well-suited for information storage [189] and for utilization in in-memory computing devices [190].

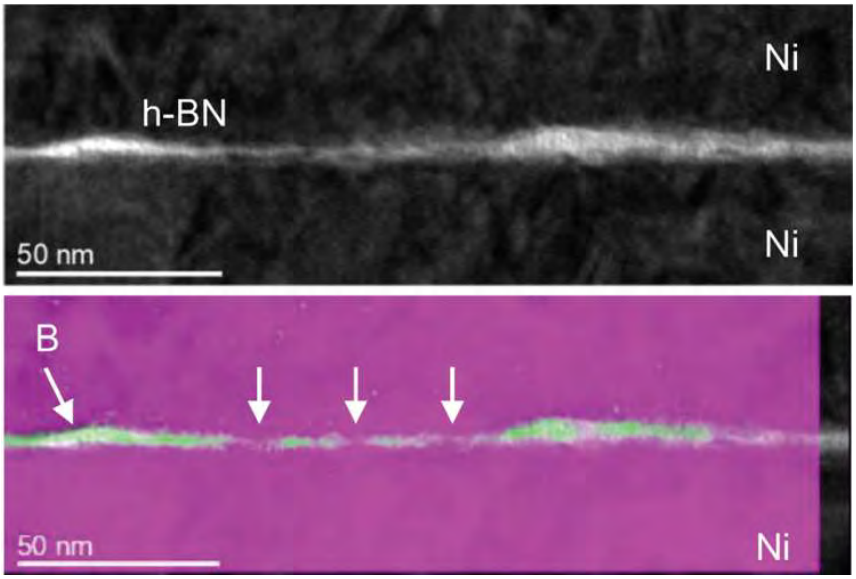

Figure 1.10 TEM image of a Ni/h-BN/Ni memristor in a permanent LRS state. The top display the Ni/h-BN/Ni structure. The bottom is the EFTEM image of the top TEM image. Purple and green represent Ni and B element, respectively. The arrows indicate the contacted top and bottom Ni by diffusion [194].

Filament formation and rupture are posited as reliable mechanisms underlying resistive switching in metal oxide-based RS devices [191,192], as well as in h-BN-based RS devices [193,194]. Pan et al. discovered the concurrent presence of bipolar and threshold RS behaviors in metal/h-BN/metal structures. This coexistence is attributed to the formation of conductive filaments at grain boundaries and the facilitation of RS by metal ions migrating through the h-BN [193]. Figure 1.10 displays a transmission electron microscope (TEM) image extracted from a Ni/h-BN/Ni memristor in the LRS state. The underlying energy-filtered transmission electron microscopy (EFTEM) image illustrates the diffusion of Ni. The researchers hypothesize

that both Ni ion diffusion and conductive filament formation occur predominantly at grain boundaries [194], aligning with the findings reported in [193]. Moreover, defects within h-BN are identified as playing a pivotal role in h-BN-based RS mechanisms [144,194]. Given the significance of the conductive filament mechanism in RS devices, h-BN, particularly when grown using the CVD method, emerges as an apt choice for the resistive layer. The presence of defects and grain boundaries in the h-BN layer facilitates the formation of conductive filaments, thereby enhancing the device's RS performance [195].

h-BN serves as a versatile material for the construction of both volatile and non-volatile memory devices in RS technology. For instance, Akinwande et al. have successfully demonstrated bipolar and unipolar non-volatile RS characteristics in a monolayer h-BN-based memristor. This device exhibits an exceptionally high on/off ratio of 10^7, rapid switching times of 15 ns, and eliminates the need for a forming process [196]. Furthermore, Shi et al. have crafted an electronic synapse utilizing a metal/h-BN/metal cell, which intriguingly displays both volatile and non-volatile RS behaviors. The power consumption of this synapse is remarkably low, with values as low as 0.1 fW in standby mode and 600 pW per transition in the volatile regime [197].

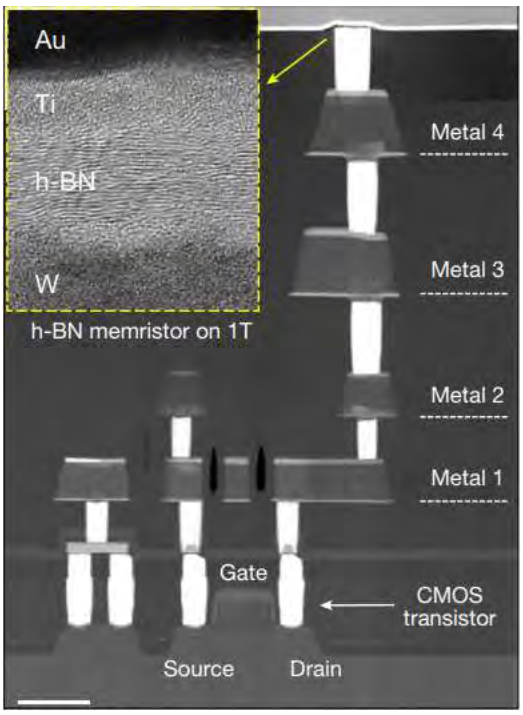

Figure 1.11 High-angle annular dark-field (HAADF) cross-sectional scanning transmission electron microscope (STEM) image of a 1T1M cell in the crossbar array. The inset shows the Au/Ti/h-BN/W memristor on the via [198].

Moreover, devices based on h-BN can be integrated with commercial electronic components to realize enhanced performance. Zhu et al. discovered that integrating an h-BN-based memristor with a conventional CMOS transistor to form a 1T1M cell can yield exceptional endurance, surpassing 2.5 million cycles. Figure 1.11 presents a TEM image of the 1T1M cell, with the Au/Ti/h-BN/W memristor distinctly visible at the top-left corner [198]. Collectively, these studies underscore the viability of h-BN as a 2D material for electronic device applications and suggest its potential for future expanded utilization.

1.2. Main contribution of the thesis

1.2.1. Objectives of the Thesis

The main goal of this thesis is to study the metal-insulator-metal structure electronic devices based on dielectric multilayer h-BN and explore their electric performance. The task can be divided into the following sections:

1) The dielectric performance of mechanical exfoliated multilayer h-BN has been investigated. The leakage current and dielectric breakdown field is explored. These types of devices contain very few atomic defects and they are very useful to understand the limit of the material in terms of electronic performance, despite their usability in real applications is poor due to the non-scalable fabrication process.

2) Nano-scale memristors based on h-BN are fabricated using only industry-compatible methods. The goal is to understand their potential for real memory and in-memory computing applications. The h-BN is synthesized via CVD. The device size is quite competitive in some cases, it approaches to 120 nm × 250 nm, as they are fabricated using electron beam lithography (EBL). The role played by the type of top electrode (Ag, Ti and Au) is also investigated.

3) We further improve the endurance of the CVD-grown nanomemristor by connecting a transistor in series (leading to 1T1M cells). This is done to avoid current overshoots during memristors set process. The type of transistor used is also made of a 2D material, which is semiconducting MoS_2. This allows us to observe an enhanced performance at the nanoscale memristors.

1.2.2. Key findings

In this work, we focused on studying one insulating 2D dielectric material named h-BN, and its application in micro- and nano-scale electronic devices with MIM structure. We obtained the following results.

First, we present the micro-scale electronic devices based on mechanically exfoliated h-BN layers. The mechanically exfoliated h-BN flakes with MIM structure have been fabricated to study the dielectric breakdown behavior of h-BN. In addition, each h-BN flake is characterized by optical techniques and atomic force microscope (AFM) to ensure their quality. Pt/h-BN/Pt devices show a uniform hard breakdown phenomenon at a ramp voltage stress from 0 to 30 V with a current limitation of 10^{-2} A, resulting a dielectric breakdown strength around 12 MV/cm. Au/h-BN/Au devices show nonlinear relationship between the breakdown voltage and h-BN thickness, leading to a median value of the dielectric breakdown strength of 10 MV/cm. Ti/h-BN/Au devices melt during the breakdown process and the median value of the dielectric breakdown strength is 9 MV/cm. The electrode diffusion ability affects the dielectric breakdown strength measured in h-BN. The excellent insulating properties of mechanically exfoliated h-BN are demonstrated, and the dielectric breakdown strength obtained from Pt/h-BN/Pt devices corresponds to previous work demonstrating a stable insulate quality of h-BN flakes.

Then, we fabricated memristors based on monolayer and multilayer h-BN grown by the CVD method, which has the potential for large-scale devices fabrication. The nano-scale size of these memristors can be down to 120 nm × 250 nm, which is the limitation of the resolution of the EBL in the lab. These memristors present non-volatile or volatile resistive switching behavior depending on the top metal electrodes utilized. Memristors with Ag electrodes present stable threshold resistive switching, and Ti and Au based memristors present non-volatile resistive switching. CVD growth h-BN is more suitable for memristors because the existence of native defects (mainly lattice distortions in the h-BN crystalline structure) can reduce the energy to form conductive filaments, allowing them to be later partially disrupted to produce the resistive switching effect.

We also do some work to modify the threshold resistive switching in Au/Ag/h-BN/Au memristors with a back-gate transistor based on mechanical exfoliated MoS_2. The on-state current of the MoS_2 transistor is around 10^{-7} A, which is an appropriate

current limitation for the Au/Ag/h-BN/Au memristors. More than 1000 cycles are achieved in the 1T1M cell, in which the memristor size is 500 nm × 600 nm.

1.2.3. Thesis Outline

This thesis consists of five parts: Chapter 1 presents the dissertation outline and introduction of the thesis. Chapter 2 presents the device fabrication method used in the thesis. Chapter 3 investigates the dielectric performance of mechanically exfoliated h-BN flakes with different metal electrodes. Chapter 4 studies the resistive switching behavior in the nano-scale memristors made of chemical vapor deposition grown h-BN. In Chapter 5, we investigate the one-transistor-one-memristor cells based on MoS_2 transistors and nano-scale h-BN memristors and characterize the threshold resistive switching in the cell. Finally, we summarize the thesis and perspective in Chapter 6.

1.3. List of publications

Only the publications included below shall be considered for the evaluation of this PhD Dissertation. A reproduction of each publication can be accessed by the information indicated below. A complete list of the author's publications (updated on May 29th, 2024) is included in the scientific curriculum vitae (Appendix A).

Article 1: **Bin Yuan**, Kaichen Zhu, Tingting Han, Sebastian Pazos, Mario Lanza*, "All-2D materials-based 1T1M cells with threshold switching for electronic neurons," ***Microelectronic Engineering***, revised.

** The author's contribution: methodology, investigation, writing draft, visualization.*

Article S1: Mario Lanza*, Felix Palumbo*, Yuanyuan Shi, Fernando Aguirre, Santiago Boyeras, **Bin Yuan**, Eilam Yalon, Enrique Moreno, Tianru Wu, Juan B. Roldan, "Temperature of Conductive Nanofilaments in Hexagonal Boron Nitride Based Memristors Showing Threshold Resistive Switching," ***Advanced Electronic Materials***, 2100580, 2021.

** The author's contribution: perform parts of the experiments.*

Article S2: Tingting Han, Fernando Aguirre, Kaichen Zhu, **Bin Yuan**, Sebastian Pazos, Sui-Dong Wang, Shaojuan Li, Mario Lanza*, "Fully two-dimensional materials-based resistive switching circuits for advanced data encryption," under review.

** The author's contribution: review and suggestion.*

Article S3: Wenwen Zheng, **Bin Yuan**, Kaichen Zhu, Sebastian Pazos, Yaqing Shen, Yue Yuan, Yue Ping, Chen Liu, Xiaowen Zhang, Xixiang Zhang, Mario Lanza*, "Ultralow defect density metal evaporation on 2D materials," under review.

** The author's contribution: perform parts of the experiments.*

Chapter 2: Device fabrication methods

This research employs various fabrication techniques to create micro/nano-scale electronic devices, utilizing h-BN as an insulating material. In this chapter, we elucidate the specific fabrication methods, parameters, and processes employed in our study.

2.1. Mechanical exfoliation method

Following the discovery of graphene in 2004 [80], the ME method saw extensive application. Over the years, with substantial development by researchers in the field of 2D materials, the ME method has undergone numerous modifications and enhancements. For instance, the original Scotch tape used in [80] was found to be excessively adhesive, resulting in polymer residues on the substrate after transfer. In our study, we opted for a different tape, SPV 224 from Nitto, which has a weaker adhesive force. This choice is motivated by the tape's reduced tendency to leave polymer residues on the substrate during the mechanical exfoliation process.

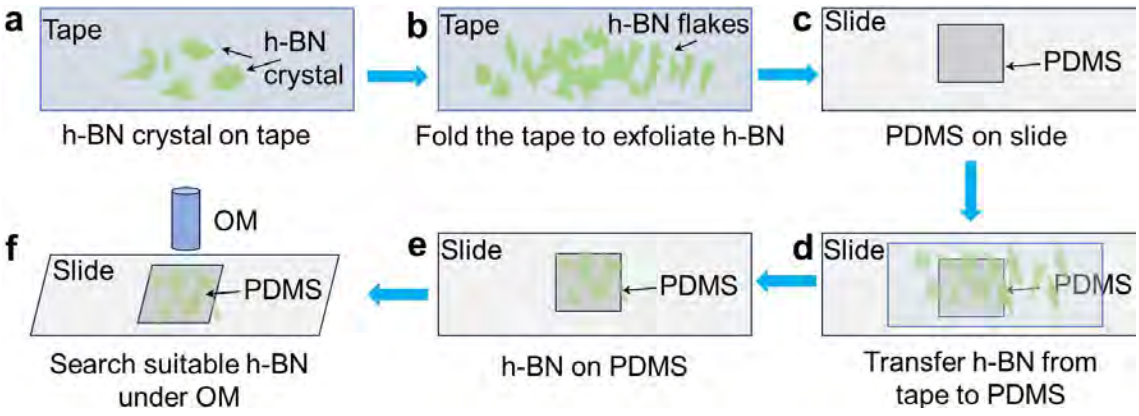

Figure 2.1 Mechanical exfoliation process of h-BN. (a) Crystal h-BN on tape. (b) h-BN flakes on tape after exfoliating several times. (c) A suitable piece of PDMS on a slide. (d) Soft press the tape to transfer the h-BN flakes to PMDS on the slide. (e) PDMS with h-BN flakes. (f) Search for thin h-BN flakes under an optical microscope.

In Figure 2.1, we illustrate the mechanical exfoliation process of h-BN. High-purity single-crystal h-BN is grown under high-temperature and high-pressure conditions [199]. Initially, we fix the tape (model SPV 224 from Nitto) onto the table and place

some h-BN particles on the tape (Figure 2.1a). We then use a new tape to exfoliate the h-BN particles on the fixed tape, repeating this step several times to obtain smaller h-BN flakes, as depicted in Figure 2.1b.

In some literature, the flakes are commonly transferred from the tape to a substrate, such as a SiO_2/Si wafer [200,201]. However, we opt for the dry transfer method to move the 2D materials to our desired location. To facilitate this, we cut a piece of polydimethylsiloxane (PDMS, 6 mil thick from Gel-pak) to cover the flakes and place it on a clean slide (see Figure 2.1c). During this placement, it is crucial to avoid bubbles between the slide and PDMS, as they make it difficult to focus under an optical microscope and can affect the subsequent dry transfer process.

Once we have confirmed that the PDMS is flat on the slide, we place the tape with h-BN flakes on top of the PDMS and gently press the tape using a cotton bud to transfer as many h-BN flakes as possible to the PDMS (Figure 2.1d). After slowly lifting the tape from the PDMS, we are left with some h-BN flakes on the PDMS, as shown in Figure 2.1e. Subsequently, we employ an optical microscope (OM, model LV 100N POL from Nikon) in reflection mode to locate the transferred h-BN flakes on the PDMS (Figure 2.1f). We might need to repeat the steps from Figure 2.1c to Figure 2.1f several times to identify the desired exfoliated flakes.

Furthermore, we have mechanically exfoliated h-BN flakes by following the same procedure outlined in Figure 2.1. After identifying the location of the flakes on the PDMS and capturing optical images for documentation, we store the slide in a protective case. This allows for the dry transfer process to be conducted at a later time when required.

2.2. Dry transfer of 2D materials

For mechanically exfoliated 2D materials, a precision transfer method is essential in the device fabrication process. Since the exfoliated materials typically have small dimensions—ranging from several micrometers to hundreds of micrometers, depending on the thickness and material—we require accurate transfer to the designated locations for the devices. A transfer stage and the dry transfer method are widely utilized for mechanically exfoliated 2D materials to achieve this objective

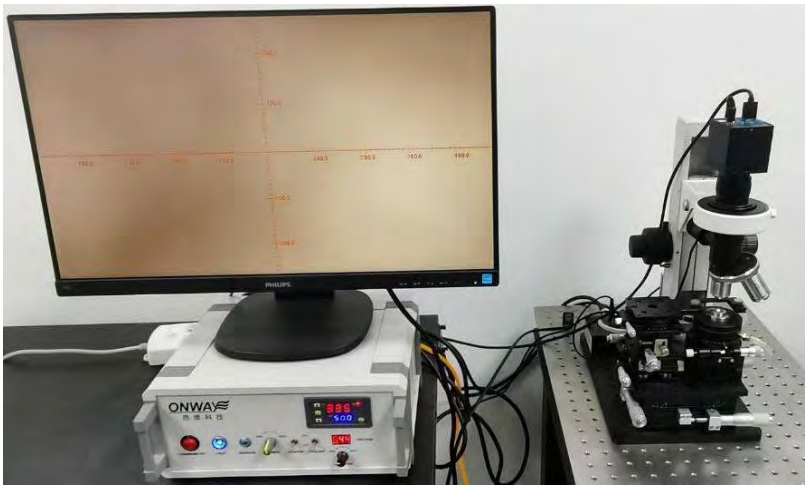

Figure 2.2 Transfer stage for the dry transfer of mechanically exfoliated 2D materials.

Figure 2.2 illustrates the transfer stage utilized in this research. Originating from Shanghai Onway Technology, the stage comprises an optical microscope, a removable stage for 2D materials, a heating mode, and a screen. Typically, the stage is mounted on an anti-vibration platform to minimize vibrations during the transfer process. On the screen, coordinate axes (as shown in Figure 2.2) serve as a reference for aligning the 2D materials with the target substrate.

The transfer process is depicted in Figure 2.3.

i) First, we prepare the 2D materials for transfer. Here, we use h-BN obtained through mechanical exfoliation, as shown in Figure 2.1.

ii) Based on the size of the h-BN on the PDMS, we use a scalpel to cut the PDMS as small as possible (Figure 2.3b) without damaging the h-BN. A smaller PDMS piece will facilitate more precise placement of the h-BN at the selected location during the dry transfer process.

iii) Then, we adjust the transfer stage to correctly align the slide with the 2D materials and the target substrate, as shown in Figure 2.3c. Using the optical microscope, it is possible to locate the 2D material and fine-tune the position until the material overlaps with the target on the substrate (Figure 2.3d).

iv) Finally, we slowly lower the slide until the h-BN on the PDMS touches the substrate (Figure 2.3e). This process must be very gradual. As the slide and substrate approach each other closely, we need to precisely adjust the position of the 2D material to ensure a correct transfer. Typically, we heat the sample plate to 50°C for 3 to 5 min (for h-BN, these parameters can be

optimized depending on the material used). Since the PDMS is a thermal release tape, heating reduces the adhesion between the 2D materials and PDMS, promoting transfer from the PDMS to the target substrate.

v) Carefully lift the slide to release the PDMS from the target substrate. This step is very delicate and should be executed with caution. If the material remains on the PDMS, it indicates that the force between the material and PDMS is greater than the van der Waals force between the substrate and 2D materials. Additional heating time may be required to weaken the adhesion force on the PDMS.

Lastly, the h-BN flake is successfully transferred to the bottom electrode on the substrate, and an optical microscope image is shown in Figure 2.3f.

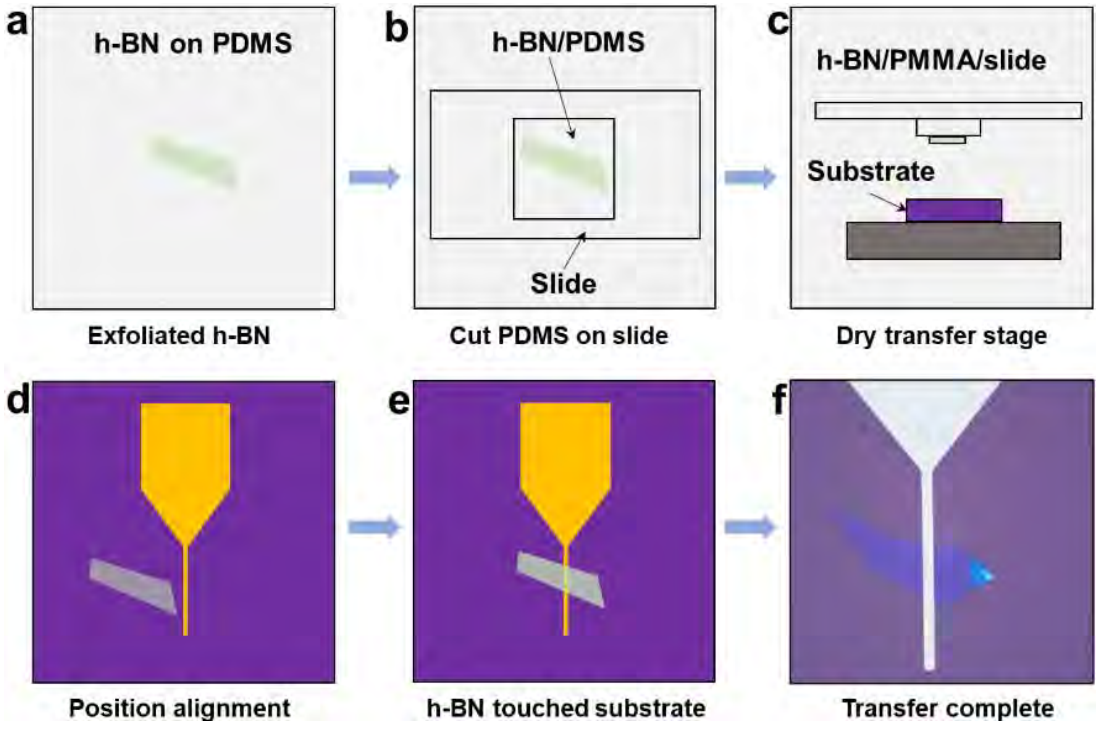

Figure 2.3 Dry transfer process. (a) h-BN flake is prepared to transfer. (b) Cut the PDMS smaller. (c) Fix the slide and substrate on the transfer stage. (d) Modify the position of the h-BN to the top of the bottom electrode on the substrate. (e) PDMS touches the substrate. (f) Image of real sample after transfer.

The process outlined above represents the standard dry transfer operation for the 2D materials utilized in this thesis. Following the transfer, the 2D material underwent characterization using an optical microscope and an AFM to verify its integrity and

confirm that it remained undamaged and intact. The transfer stage and the employed dry transfer methodology have proven to be sufficiently adept for meeting our device fabrication specifications.

2.3. Wet transfer method for CVD-grown 2D materials

CVD-grown 2D materials are typically synthesized on metal foils, as these metals can facilitate the decomposition of precursors due to their lower energy barriers and catalytic activity [202]. Graphene, for instance, is commonly grown on Cu foil [203] or Pt substrates [204]. While it is possible to synthesize some 2D materials directly on the target substrate [205], challenges remain inherent to this approach.

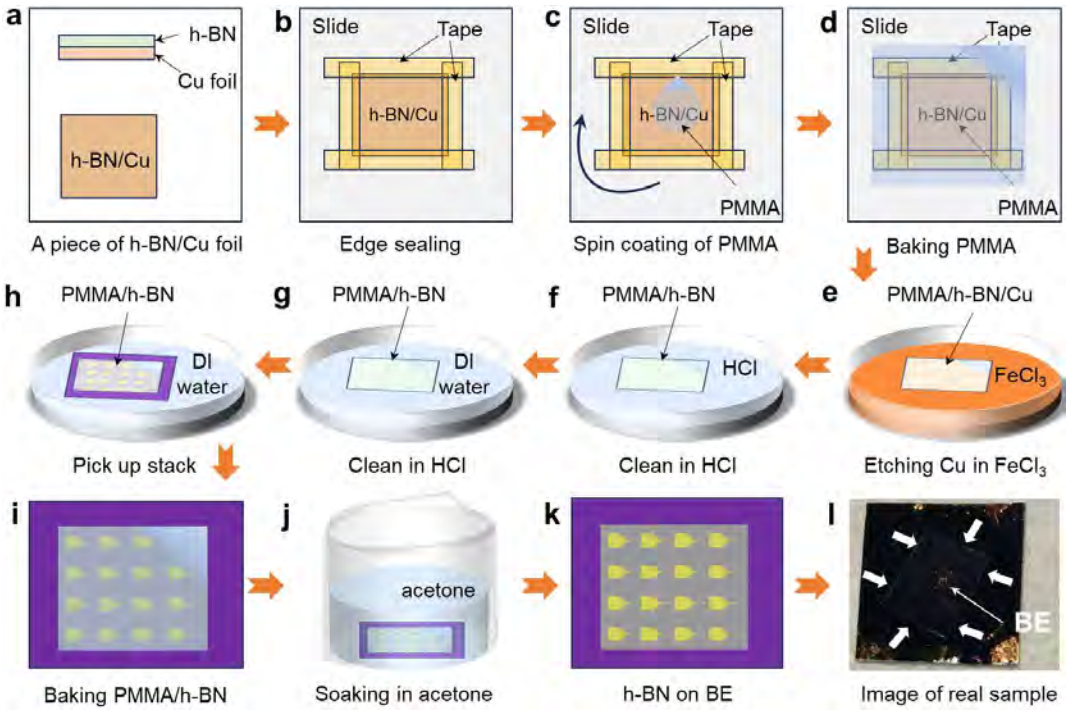

Figure 2.4 Wet transfer process (a) A piece of Cu foil with h-BN grown by CVD. (b) h-BN/Cu foil piece sealed and fixed on a slide by tape. (c) Spin coating of PMMA on the surface of h-BN. (d) Soft baking on a hot plate to remove liquid in PMMA. (e) PMMA/h-BN/Cu foil in saturation $FeCl_3$ solution. (f) PMMA/h-BN stack in 2wt% HCl solution. (g) PMMA/h-BN stack in DI water. (h) Transfer the PMMA/h-BN stack onto the target substrate. (i) Baking the water in the devices. (j) Soaking the sample in acetone to remove PMMA. (k) h-BN transferred on substrate with BE. (i) Image of a real h-BN transferred sample.

For the h-BN used in this thesis, we purchased it from Graphene Supermarket Co., where the h-BN is synthesized on a Cu foil. We employed a widely recognized wet transfer method [197] to facilitate the transfer of h-BN onto our desired substrate.

The wet transfer process steps are presented in Figure 2.4.

i) First, we cut a piece of Cu foil with h-BN on the surface (Figure 2.4a), which is large enough to cover the bottom electrode on the target substrate. Since both sides of the Cu foil have h-BN, the supplier marks the side with better quality. We always use this side to achieve the best performance.

ii) Then, we need to flatten the h-BN on a slide with another slide using clean paper to protect the h-BN piece. Tape is used to secure the h-BN onto the slide and seal all edges (Figure 2.4b) to prevent the polymethyl methacrylate (PMMA) from seeping into the back side during the spin coating process. If not sealed properly, it will be difficult to etch the Cu foil in the following steps.

iii) Next, spin coating of PMMA (950 K, A4, from Kayaku) on the surface of the h-BN. The parameters are set to 500 rpm for 6s and 3,500 rpm for 30 s, respectively (Figure 2.4c).

iv) We then bake the sample with PMMA at 100 ^{o}C for 3 min on a hot plate to form a stable PMMA layer to support the h-BN layers in the next steps.

v) After removing the tape around the edges, we re-flattened the foil and put the h-BN foil covered by the PMMA into saturated ferric chloride ($FeCl_3$) solution to etch the Cu foil, as shown in Figure 2.4e. The side of the substrate devoid of PMMA should be immersed face-down in the $FeCl_3$ solution. This process will take several hours (more than 8 hours in our research) until the PMMA/h-BN stack becomes transparent.

vi) Once the Cu foil is etched, we transfer the PMMA/h-BN stack to 2 wt% hydrochloric acid (HCl) solution for 2 min to clean the stack (Figure 2.4f).

vii) Subsequently, we move the PMMA/h-BN stack to deionized (DI) water for 20 min for cleaning (Figure 2.4g).

viii) Then we transfer the PMMA/h-BN stack to the substrate with the bottom electrode, as presented in Figure 2.4h, and bake the sample at 50 ^{o}C for 5 min to remove water and achieve better van der Waals contact between the h-BN and substrate (Figure 2.4i).

ix) We then soak the PMMA/h-BN/substrate in acetone for 12 hours to remove the PMMA (Figure 2.4j).

x) Finally, after annealing at 50 ^{o}C for 30 min, the h-BN is successfully transferred to the substrate. as shown in Figure 2.4k. A real transfer completed sample image is presented in Figure 2.4l we can observe that the bottom electrode (BE) is covered by the h-BN (area pointed by the wide white arrows) by naked eyes.

2.4. Device electrode fabrication

The conductive electrode is an important part of electrical characterization during the device fabrication process. In this research, we fabricate the metal electrode in two ways for micro and nano-scale devices, respectively. For micro-scale devices, we use photolithography to transfer the pattern to the substrate, and for nano-devices, we use electron beam lithography to conduct the pattern transfer work.

2.4.1. Photolithography for micro-scale device electrode

Photolithography stands as an exceedingly mature fabrication technique within the pattern transfer process, widely recognized and utilized in both academia and industry. Mask aligners are categorized based on the wavelength of ultraviolet (UV) light they employ, which includes ultraviolet (UV), deep ultraviolet (DUV), and extreme ultraviolet (EUV) [206]. It is well known that DUV and EUV technologies are predominantly utilized in the industry for the production of high-resolution chips, ranging from tens of nanometers down to a few nanometers. In contrast, UV photolithography is more prevalent in laboratory research settings.

In our research, we employ a UV mask aligner, the model MJB4 from SUSS Micro Tec. This equipment is capable of achieving a highest resolution of 2 μm, although this level of precision has become challenging to attain due to the age of the machine. For the electrodes in our devices, we have opted for a resolution of 5 μm, considering the optimal balance between stable quality and yield.

We utilize the bilayer method, which involves two distinct layers of photoresist, to achieve an undercut structure as illustrated in Figure 2.5 (step 4). An undercut structure is created when the etching process removes material from the sides of the photoresist

pattern, resulting in an angled sidewall that is wider at the bottom than at the top. This structure allows us to fabricate electrodes with flat edges, which is particularly beneficial for subsequent AFM characterization.

Initially, we design the photomask using Tanner software, a tool for pattern design, which is then manufactured by Suzhou Photomask Company. The photomask is typically made from soda glass, measuring 3 inches in diameter. One side of the mask is coated with chromium (Cr), except for the pattern areas, while the other side remains uncoated. This type of photomask is known as a positive mask, where the pattern region allows light transmission. The positive mask is used in conjunction with a positive photoresist; light passes through the transparent pattern region and reacts with the photoresist to break the molecular bonds within it. Subsequently, during the development process, the exposed and reacted regions (the pattern) are removed with specialized chemicals known as developers, leaving the desired pattern intact on the substrate. This selective removal means that we can add films or perform etching only in the patterned areas, as the other areas remain protected by the photoresist.

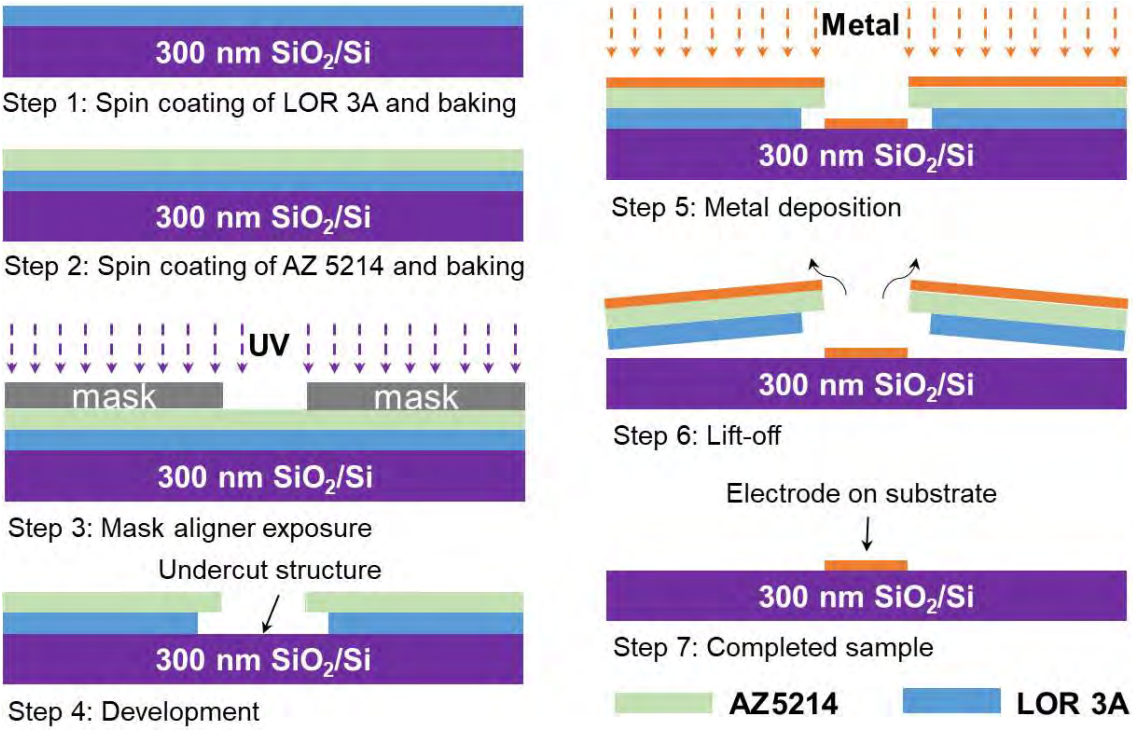

Figure 2.5 Photolithography process using bilayer method.

The photolithography process, as outlined in Figure 2.5, is detailed in the following steps:

Step 1: Initially, we apply a layer of LOR 3A (a non-light-sensitive resist from Micro Chem) as the bottom layer of our bilayer lift-off technique on a substrate (300 nm SiO_2/Si). The application is performed using a spin coater set at 6,000 rpm for 30 s, followed by a soft bake at 150°C for 3 min. The LOR 3A resist, though not sensitive to light, dissolves more rapidly in a special developer than the subsequent layer of photoresist (AZ5214).

Step 2: Subsequently, we spin coat a second layer of positive-tone photoresist (model AZ5214 from Micro Chem) with the following parameters: 4,000 rpm for 30 s, and a soft bake at 95°C for 90 s.

Step 3: We then secure the photomask onto the mask aligner in contact with the substrate bearing the photoresist layers. Employing a soft contact mode ensures that the mask gently touches the sample. Exposure is followed by UV light passing through the transparent patterned areas of the mask, initiating a reaction with the photoresist that alters its structure, thereby facilitating its removal during development.

Step 4: The sample is immersed in a developer solution, tetramethylammonium hydroxide (TMAH) at 2.38% concentration, for 45 s, then rinsed in DI water. During this phase, the LOR 3A dissolves more quickly than the AZ5214 that has been exposed, resulting in an undercut structure of the pattern sidewalls as illustrated in step 4 of Figure 2.5.

Step 5: Subsequently, metal deposition is carried out on the sample, as indicated in Figure 2.5. The metal in the patterned area does not make contact with the metal in other areas.

Step 6: The subsequent phase involves the lift-off process, which removes the unwanted metal from the substrate, preserving only the patterned region. This is accomplished by immersing the sample in a specialized remover. For our bilayer lift-off process, we utilize n-methylpyrrolidone (NMP) as the remover. The sample is placed in a beaker filled with NMP and both are immersed in a water bath at 60°C for a duration exceeding 90 min.

Step 7: Ultimately, the electrode is successfully fabricated on the substrate, as represented in the figure.

The AFM topography map presented in Figure 2.6 illustrates the bottom electrode fabricated using the bilayer lift-off technique. This electrode has a thickness of 40 nm.

The left-hand image clearly demonstrates that the surface of the bottom electrode is smooth and free of contaminants. Upon examining the three-dimensional (3D) view depicted in the right-hand figure, only a minimal number of particles are discernible, which are likely to be dust particles. The sharply defined edge of the bottom electrode suggests that the transferred h-BN can adhere precisely to the electrode's surface. This characteristic will prove particularly advantageous during the subsequent characterization of the h-BN's thickness after transfer.

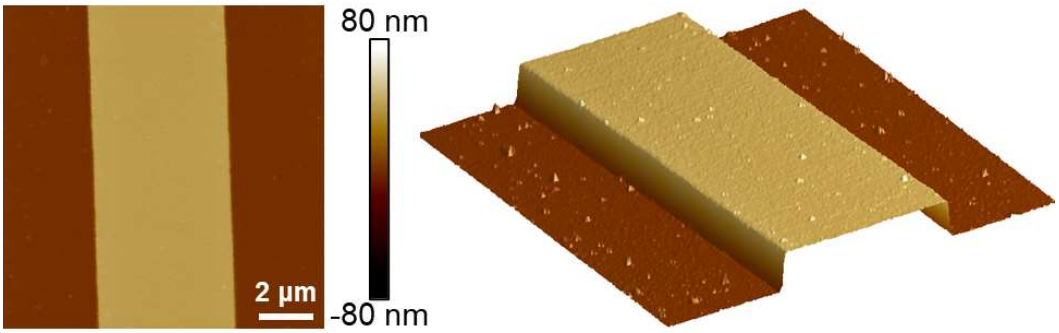

Figure 2.6 AFM topography map of electrode for micro-scale devices. The electrode has a sharp edge which is friendly to 2D materials transfer and characterization.

2.4.2. Electron beam lithography for nano-scale device electrode

In laboratory research, EBL is the predominant method for fabricating devices at the nano-scale. Within the EBL system, the electron beam is directed by a pattern generator to inscribe the desired pattern directly onto a substrate coated with PMMA, which serves as a photoresist in the EBL process. The sample, once written, is immersed in a developer and then stoper solution to dissolve the PMMA exposed by the electron beam, thereby leaving the pattern onto the substrate for following operations.

The advantages of EBL are manifold: i) It eliminates the need for physical masks, enabling the testing of numerous patterns without the associated mask fabrication costs and time investment. ii) EBL is capable of producing nano-scale features that are challenging for other fabrication techniques to achieve. iii) It does not necessitate the use of a yellow room or a cleanroom environment for the fabrication process.

However, a key limitation of EBL stems from its operational principles, resulting in a relatively low yield.

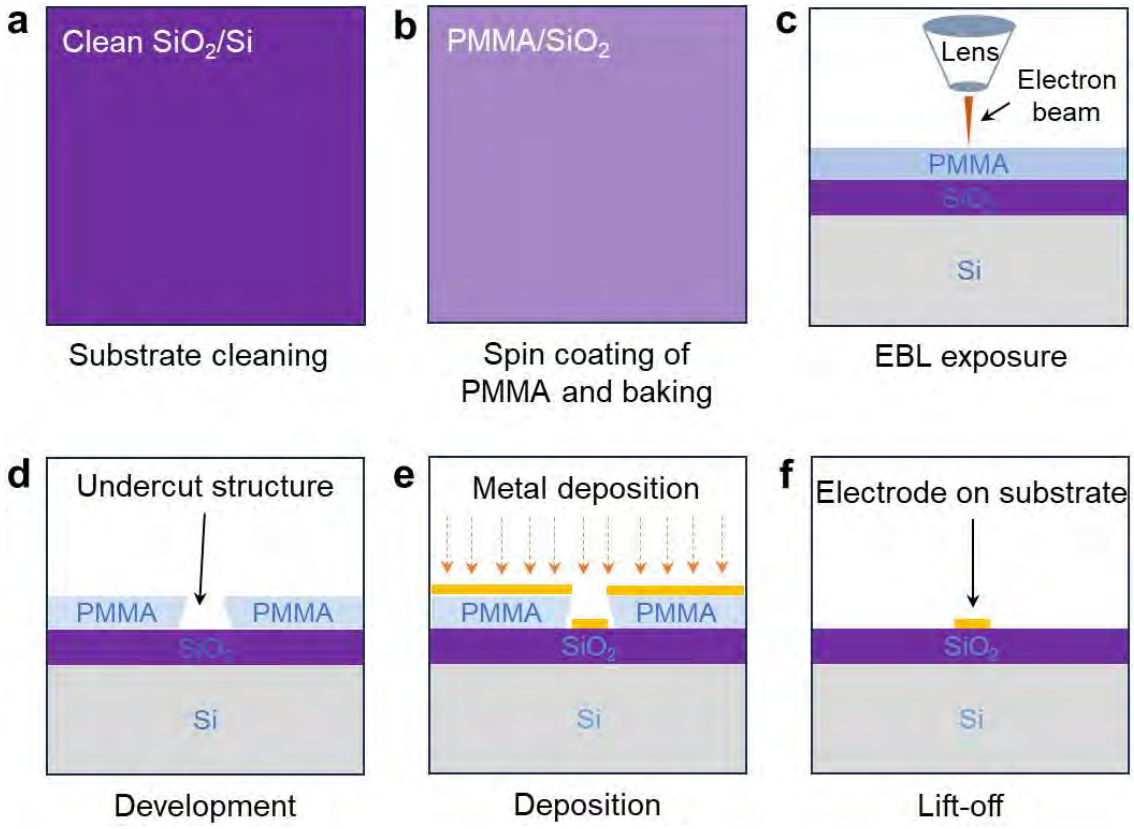

Figure 2.7 Fabrication of bottom electrode using EBL.

The EBL system we utilized consists of a pattern generator from Raith (model Elphy VII from Raith) in conjunction with a scanning electron microscope (model Quanta 200 FEG from FEI). The entire EBL process can be divided into the following steps, as presented in Figure 2.7:

a) The substrate is cleaned using ultrasonic cleaner with acetone, ethanol, and DI water.

b) Spin coating PMMA (950K, A4, from Kayaku) on the substrate. The parameters are 3,500 rpm for 60 s, then baking at 180 ℃ for 90 s.

c) Subsequently, the exposure is conducted in a vacuum chamber (< 2×10^{-3} Torr). The pre-designed pattern is directly written onto the PMMA layer at 20 kV and with suitable parameters.

d) After the patterning of the electrodes, the development process is carried out in a solution (isopropanol: methyl isobutyl ketone = 3:1) for 2 min, then soaked in a stopper (IPA) for 30 s. After development, we typically use an optical microscope to verify that the correct pattern has been produced by the EBL. Additionally, due to electron scattering at the base of the PMMA, an undercut structure is formed, as shown in Figure

2.7d. This undercut structure facilitates the lift-off process, resulting in a sharp edge of the pattern, as mentioned in the bilayer lift-off section.

e) Following development, metal is deposited onto the sample, and an illustration is presented in Figure 2.7e. Owing to the undercut structure, the deposited metal will not form a continuous film from the PMMA surface to the pattern. Such samples will be easier to process for the removal of unwanted metal during the lift-off step.

f) Finally, the fabrication of the bottom electrode via EBL, metal deposition, and lift-off is completed.

2.4.3. Metal deposition for electrode

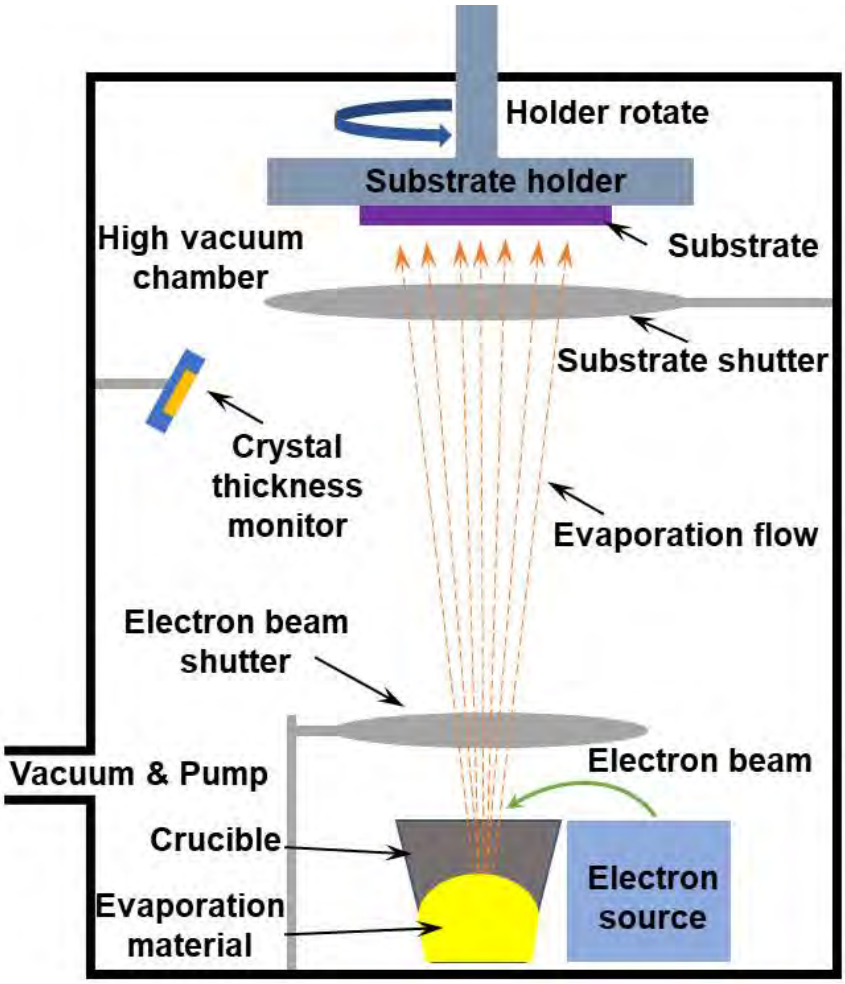

Figure 2.8 Schematic of electron beam evaporation.

The electrode patterns for the devices can be fabricated using either photolithography or the EBL method. In terms of metal deposition, we exclusively utilize electron beam evaporation. This is because the evaporation temperature is lower

than that of thermal evaporation, which is advantageous during the lift-off step for removing the photoresist in photolithography or the PMMA in EBL fabricated devices. High temperatures during the metal deposition process would cause the photoresist or PMMA to solidify, thereby making them difficult to remove during the lift-off process.

Magnetron sputtering can deposit metals without temperature concerns. However, the sputtered atoms possess higher energy compared to evaporated atoms, and these high-energy atoms could potentially damage the layered materials.

The schematic representation of the electron beam evaporation process is depicted in Figure 2.8. Samples are secured to the sample plate using heat-resistant tape. A high-energy electron beam, generated by the electron gun, is directed onto the material contained within the crucible. This beam heats and vaporizes the material. Subsequently, the metals, now in a gaseous state, traverse the chamber and undergo condensation upon contact with the substrate. The substrate is equipped with a rotational mechanism that operates at an adjustable speed, ensuring the formation of a uniformly thick film. An electron beam shutter is employed to meticulously control the precise thickness and to maintain a consistent film quality, alongside a stable deposition rate. The electron beam shutter remains closed until the evaporation rate stabilizes. The substrate shutter is activated post the opening of the electron beam shutter, allowing the vaporized metal to condense on the substrate.

The thickness of the deposited film is monitored in real-time using a crystal thickness monitor. Once the measured thickness reaches the predetermined value, the substrate shutter is closed to conclude the evaporation process

The model of the electron beam evaporation system we use is the PVD 75 from Kurt J. Lesker Company. The chamber vacuum can achieve 10^{-5} Torr after pumping. The machine is equipped with four distinct sources that facilitate the sequential deposition of various metals, all without the need to vent the chamber or replace the crucibles.

2.5. Summary

This chapter provides an overview of the primary techniques employed for device fabrication in this research endeavor. It delves into the working principles and procedural intricacies of mechanical exfoliation, dry transfer, wet transfer,

photolithography, EBL, and electron beam evaporation. Additionally, it enumerates the specific parameters utilized throughout the fabrication process.

In summary, this chapter compiles the majority of the data and pertinent details concerning device fabrication, thereby eliminating the need to reiterate certain fabrication specifics in subsequent chapters. It is designed to enhance the reader's comprehension of the entire thesis, particularly the segment dedicated to device fabrication.

Chapter 3: Dielectric breakdown of exfoliated h-BN in micro-scale devices

3.1. Introduction

h-BN is a 2D material with a honeycomb structure, similar to that of graphene. Unlike graphene, which is highly conductive, h-BN has a wide bandgap of approximately 5.9 eV [119,120], a property that is rarely observed in 2D materials. This unique dielectric characteristic of h-BN makes it suitable for use in electronic devices such as dielectrics and gate dielectrics in transistors [174]. Dielectric breakdown (BD) is an important phenomenon in dielectric materials, as it can transform insulating materials into a conductive state. When an adequate electric field is applied to the dielectric, the voltage exceeds the dielectric and generates a high current, which is referred to as BD. This event often results in the failure or damage of dielectric materials. Research into the BD of dielectrics/insulators is beneficial for understanding the electrical limitations of materials and selecting appropriate dielectric materials for device fabrication.

Because of these benefits, some studies have focused on BD in mechanically exfoliated h-BN using a CAFM [207] and/or probe station [208]. Hattori et al. measured the anisotropic dielectric breakdown strength (EBD) of mechanically exfoliated h-BN. The E_{BD} measured in the direction perpendicular to the layers of h-BN was approximately 12 MV/cm (million volts/centimeter). This value can serve as a benchmark for assessing the quality of h-BN layers grown via CVD [208]. The BD of h-BN synthesized via CVD has also been investigated. Jiang et al. characterized monolayer and multilayer h-BN grown by CVD at the nano-scale and device level and revealed that the superior thermal conductivity of h-BN is beneficial for improving the reliability of h-BN devices by increasing the local thermal heat dissipation rate, decreasing avalanche currents, and slowing down electromigration. [209]. For CAFM characterization, although the contact size can be 1 nm^2 to 50 nm^2 [210,211], the voltage bias that can be applied to the tip is normally limited to ±10 V, while some researchers connect a semiconductor parameter to lift the bias limitation [212], which requires annoying and complex operations. The smallest size of the devices based on h-

BN with metal/h-BN/metal structure for the probe station characterization in literature can be found is 6.25 μm^2 [213]. However, data from previous reports are scarce. In addition, AFM topography characterization of only a few h-BN flake devices has been presented in the literature. To study the BD properties of h-BN, it is better to use mechanically exfoliated h-BN to fabricate devices, as h-BN synthesized via CVD may contain defects or lattice distortion inside, which could affect the BD performance.

Due to the scarcity of previous research on the investigation of h-BN BD properties, such as limited data availability and large device size, we are currently developing a new study plan to examine the BD behavior of h-BN. Our plan involves using mechanically exfoliated h-BN as the dielectric layer and constructing MIM devices with a cross-point structure to regulate the device size. Specifically, we have opted for a device size of 5 μm × 5 μm, which ensures that the exfoliated h-BN flakes are sufficiently large for device fabrication. Additionally, photolithography enables us to efficiently produce a sufficient number of devices for measurement and future data analysis.

This chapter delves into the analysis of MIM devices, focusing on their breakdown behavior across varying h-BN dielectric thicknesses. The study employs different electrode materials and mechanically exfoliated h-BN in the fabrication process. By applying a ramped voltage stress (RVS) of up to 30 V, the micro-scale devices' breakdown characteristics were extensively examined.

3.2. Experiments

3.2.1. Cross-point micro-scale device fabrication process

Although there are two types of BD in h-BN layers, one is the BD that occurs in the perpendicular direction of the h-BN layers, and the other BD occurs in the direction parallel to the h-BN layers [208]. However, the dielectric breakdown strength is lower in the parallel direction, and it is less meaningful to study the breakdown in this direction. Therefore, we will only investigate BD in the perpendicular or out-of-plane directions.

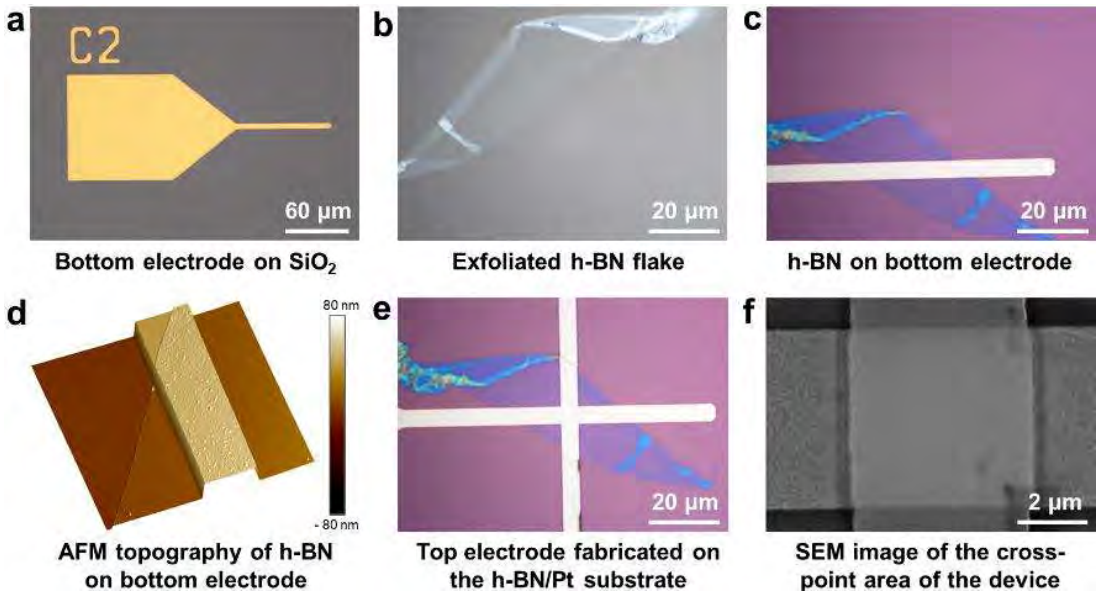

Figure 3.1 Metal/ME h-BN/Metal fabrication process. (a) The bottom electrode was prepared using photolithography, e-beam evaporation, and lift-off. (b) Optical microscope image of mechanically exfoliated h-BN flake on PDMS. (c) Dry transfer h-BN onto the bottom electrode. (d) 3D AFM topography map of the h-BN on bottom electrode. (e) Completed Pt/ME h-BN/Pt device. (f) SEM image of the cross-point area.

To assess the BD property of h-BN obtained by ME, a cross-point device structure was employed, which involves a metal/ME h-BN/metal sandwich configuration. This method allowed for a systematic examination of the dielectric strength of h-BN in the perpendicular direction to the device structure.

The cross-point structure is commonly utilized in evaluating dielectric breakdown, as the dimensions of the characterized h-BN can be defined by adjusting the size of the bottom and top electrodes. In this study, a device with dimensions of 5 μm × 5 μm was fabricated.

The metal/ME h-BN/metal sandwich structure served as a controlled environment for dielectric breakdown testing. It comprised a thin layer of ME h-BN positioned between two metal electrodes, which were utilized to apply a voltage across the h-BN layer. By progressively increasing the voltage and monitoring the current flow through the device, the point of electrical breakdown in the h-BN layer could be identified.

The metal/ME h-BN/metal device fabrication process is shown in Figure 3.1. i) First, we prepared a substrate with a bottom electrode, as shown in Figure 3.1a. The bottom electrode was fabricated via photolithography, electron beam (e-beam) evaporation, and lift-off. The large pad size was ~100 μm × 100 μm, and the tail size

was 90 μm × 5 μm. The width of the tail (5 μm) determines the size of the cross-point device. ii) The ME h-BN flakes were prepared as shown in Figure 3.1b. This OM image was captured when the h-BN flake was on PDMS. The mechanical exfoliation process is described in section 2. iii) Next, we used the dry transfer method to move the h-BN flakes to the bottom electrode using a transfer stage to obtain the h-BN/Au electrode (Figure 3.1 c). In this step, we can evaluate the quality of the h-BN flakes using an optical microscope and determine whether to proceed with the next fabrication step. iv) To confirm the thickness and film quality of the ME h-BN flake on the substrate, we used an AFM in tapping mode (the AFM tip does not contact the sample to cause possible damage) to characterize the thickness, and the 3D topography map is presented in Figure 3.1d, showing the clear existence of the transferred h-BN. From the AFM results, we can confirm not only the thickness and quality of h-BN but also the cover area and position on the bottom electrode. For example, according to the AFM image, we can determine whether the covered area is sufficient to fabricate the top electrode and the position with the best quality h-BN (uniform thickness, low roughness, without wrinkles, contaminations, or cracks) to place the top electrode. Therefore, AFM is an essential characterization method in the device fabrication process and should be conducted for every device in this research. v) After ensuring the correct h-BN thickness and position, we used photolithography, e-beam evaporation, and lift-off to fabricate the top electrode and finally obtain the device, as shown in Figure 3.1e. vi) The final confirmation of the device was conducted using a scanning electron microscope (SEM); the SEM image of the cross-point area of the device is presented in Figure 3.1f. According the SEM image, we can read out that the cross-point size is ~5 μm × 5 μm, and the surface of the device is clean. The h-BN flakes were uniform in the SEM image, and no wrinkles or cracks were detected.

3.2.2. Characterization of materials and devices

Various techniques were implemented in this research for device fabrication. In the fabrication process, OM (model LV 100N POL from Nikon) was utilized for the mechanical exfoliation of h-BN flakes and to assess the quality and size of the bottom electrodes. Following the transfer of h-BN to the bottom electrode, an AFM (model Multimode V from Bruker) operating in tapping mode with tips (model NCH from Nano World) was employed to characterize the topography and thickness of h-BN. OM

was subsequently used to determine the placement of the top electrode for alignment in the second photolithography process. After the devices were completed, OM and SEM (model Gemini 500 from Carl Zeiss) were used to evaluate the topography and size of the finished device. Electrical characterization was carried out using a probe station (model M150 from Cascade) connected to a semiconductor parameter analyzer (SPA, model 4200 from Keithley).

3.3. Result and discussion

3.3.1. Electrical characterization of Pt/ME h-BN/Pt devices

Prior to presenting the electrical characterization data, it is essential to provide additional information about the device, including the h-BN thickness, which serves as a crucial parameter in BD.

Previously, we mentioned the utilization of an AFM in tapping mode to assess the h-BN thickness without causing harm to the thin films. Figure 3.2 showcases AFM topography images of 30 h-BN flakes on 5 um width Pt bottom electrodes. The height scale bar in the AFM images ranges from -80 nm to 80 nm is suitable, considering the 40 nm Pt bottom electrode thickness. These AFM images reveal that the h-BN flakes covering the Pt electrodes are uniform and level. Any non-ideal h-BN flakes or samples will be discarded, as the yield is high at approximately 90%. This is due to the h-BN flake having sufficient area, as indicated by the scale bar, to cover the partial bottom electrode tail (tail width of 5 μm). The quality of the h-BN is also satisfactory. As a result, we are presenting 30 Pt/ME h-BN/devices here. All electrodes exhibit sharp edges due to the bilayer lift-off technique employed in the bottom electrode fabrication process outlined in Chapter 2. In some AFM images, white spots represent thick h-BN bulk, which is a common occurrence in mechanically exfoliated materials and difficult to avoid entirely. However, these spots are clear in the AFM images, and we will avoid using regions with contamination to fabricate top electrodes. The majority of the h-BN flakes in Figure 3.2 are clean, free from cracks or wrinkles in the area where the top electrode will be fabricated later. Only a few devices have clusters of thicker h-BN spots, but the ratio is minimal compared to the number of clean h-BN flakes. The impact of these imperfect devices on our study and data analysis will be negligible.

However, we will pay attention to the data generated by these devices during the subsequent electrical characterization.

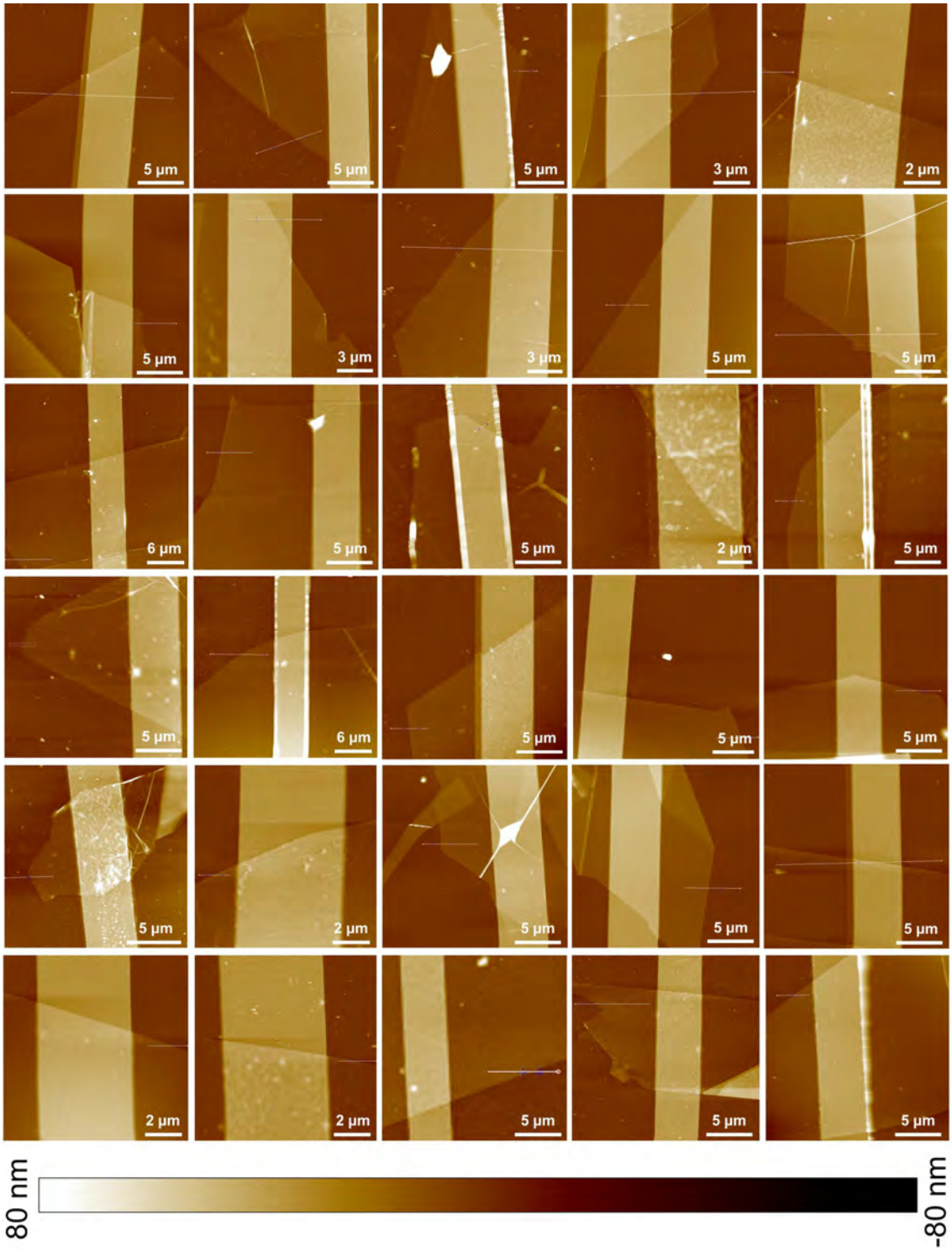

Figure 3.2 AFM topography map of thirty h-BN flakes on Pt bottom electrodes obtained using tapping mode.

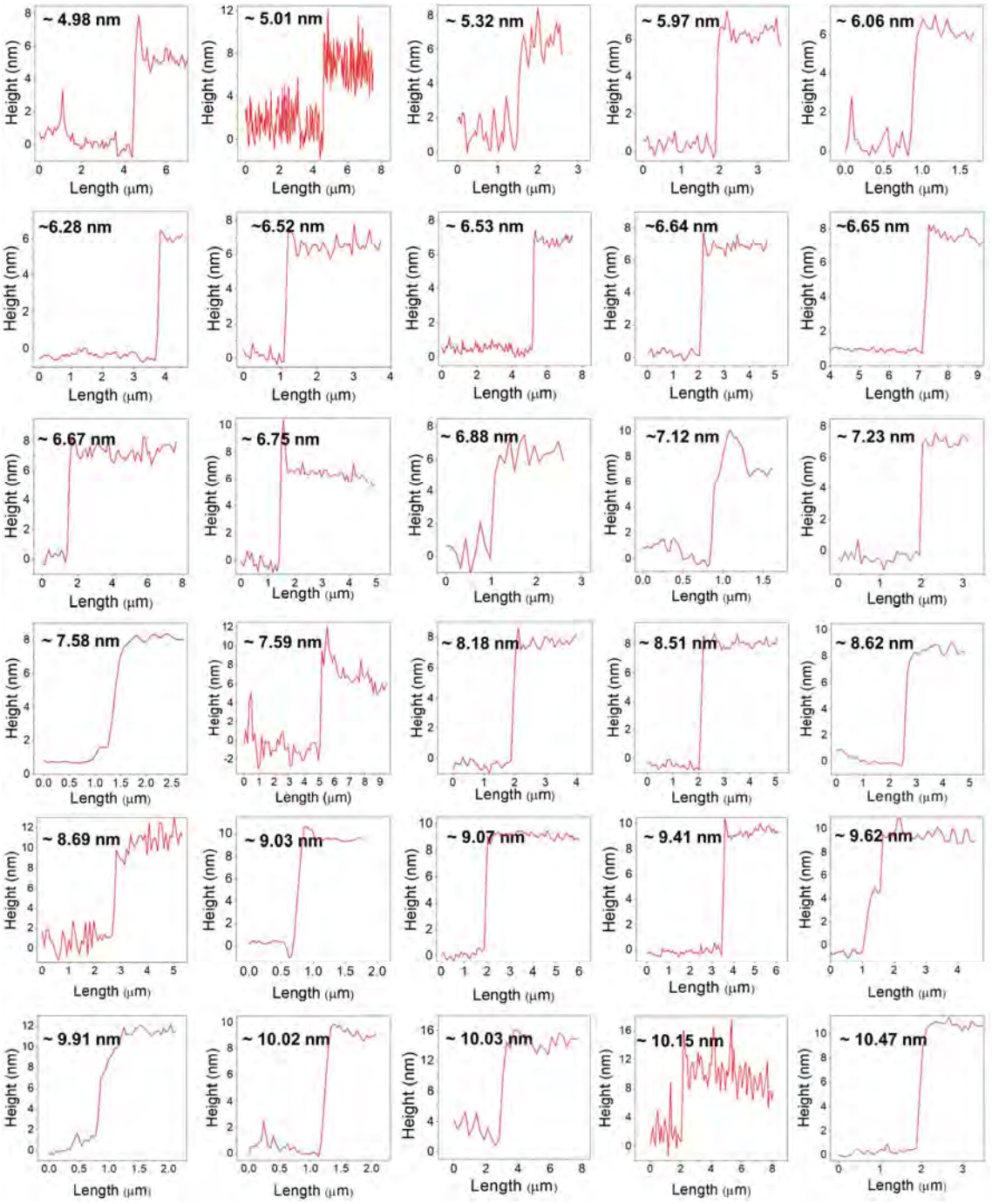

Figure 3.3 Thickness of the h-BN on Pt bottom electrodes measured by AFM. The plots range is in the same order to the devices in Figure 3.2.

Characterization of h-BN and bottom electrodes using AFM is crucial for several reasons. One of the primary objectives is to ascertain the thickness of h-BN. Utilizing the section function in NanoScope Analysis, the thickness of h-BN can be readily extracted. Figure 3.3 displays the corresponding h-BN thickness data. The thickness of h-BN is indicated in the top-left corner of each height versus length plot. The plots in

Figure 3.3 correspond to the range of devices depicted in Figure 3.2. Analysis of the h-BN thickness data in Figure 3.3 reveals that the thickness of the 30 h-BN flakes varies from 4.98 nm to 10.47 nm. Variability in the thickness of h-BN is inherent due to the mechanism of mechanical exfoliation. The thickness of individual h-BN flakes is random and can only be assessed within a range based on the transparency of the h-BN under an optical microscope. However, the progressive increase in the thickness of h-BN offers valuable insights into the relationship between thickness and electrical performance, which is crucial for this research.

Furthermore, due to the high transparency of h-BN, obtaining thinner h-BN, particularly less than 5 nm, is extremely challenging. To acquire sufficient data for future analysis of the behavior of BD in mechanically exfoliated h-BN, we suggest that a thickness of around 10 nm is acceptable. This thickness of h-BN is commonly observed and reported in previous studies [207,214].

Among all the metals that can be deposited using an electron beam evaporator, we have selected Pt as the bottom and top electrode. This is because Pt is an inert metal that is highly stable in ambient conditions and does not have native oxide defects [123]. Furthermore, Pt is unlikely to diffuse into the h-BN layers unless a sufficient bias is applied [215]. This makes Pt an ideal candidate for studying the breakdown of ME h-BN, with minimal interference from conductive electrodes. Additionally, a Pt wire tip was used as the top electrode in a study by Ref. [216] to investigate breakdown in h-BN. To study the BD in the ME h-BN layers, it is necessary to apply an external bias on the top electrode and ground the bottom electrode in the Pt/ME h-BN/Pt device. Figure 3.4 illustrates the details of the Pt/ME h-BN/Pt device structure and electrical measurement strategy. Specifically, Figure 3.4a depicts the thickness of each layer in the Pt/ME h-BN/Pt device. The substrate is a 300 nm SiO_2/500 μm Si wafer, which provides a high flat surface to ensure the smooth surface of the bottom electrode on the substrate. A flat bottom electrode is essential as the van der Waals force between the h-BN flake and bottom electrode requires a clean and flat interface. A 10 nm titanium (Ti) layer is used as an adhesion layer because Pt is challenging to attach to the wafer surface. Additionally, 30 nm and 40 nm Pt are deposited via e-beam evaporation as the bottom and top electrodes, respectively. Figure 3.4b is an optical microscope image of the Pt/ME h-BN/Pt device after fabrication, with the device compositions, including the top electrode, bottom electrode, and h-BN flake, marked in the image. During the electrical

measurement step, a positive RVS from 0 to 30 V will be applied to the top electrode, and the bottom electrode will be connected to the ground.

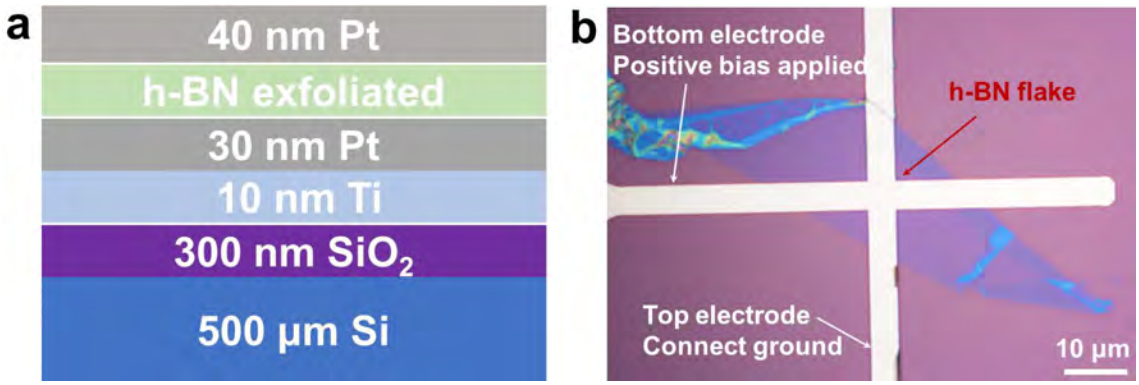

Figure 3.4 Pt/ME h-BN/Pt device schematic diagram. (a) Side view of the device and the layer information. (b) Optical microscope image of the devices after fabrication.

The electrical measurements of the Pt/ME h-BN/Pt devices were conducted, and the current-voltage (I-V) curves of all devices were collected in Figure 3.5. In the characterization strategy, the voltage was applied to the top electrode from 0 V to 30 V to provide an electric field, and the current limitation was set to 10^{-2} A by the SPA. This high voltage ensured adequate bias for the breakdown process. Figure 3.5a indicates that the BD occurs in all devices, and the sudden increased currents reach the limitation of 10^{-2} A. The trend of the I-V curves shows a high degree of homogeneity, although there are still some differences between these curves. First, the current before BD increases faster depending on the h-BN thickness. Thinner h-BN devices have a high current at low bias and their breakdown voltages are also lower than thick ones. This phenomenon indicates that the breakdown voltage has a close relationship with the thickness of h-BN flakes used in the Pt/ME h-BN/Pt device. In addition, the leakage current in the Pt/ME h-BN/Pt device depends on the thickness of h-BN. Thicker h-BN has less leakage current than thinner ones. After the BD was observed, a small voltage bias of 1 V was applied to the device again, and it was found that the device was conductive without high resistance. This means that the BD in Pt/ME h-BN/Pt is hard BD, i.e., the device will remain in a low resistance state, and the h-BN insulator property is permanently damaged. Figure 3.5b presents the current density of the Pt/ME h-BN/Pt devices based on the I-V curves in Figure 3.5a.

The calculation of current density is based on the following equation:

$$J = I/S$$

Here, J represents current density in amperes per square meter (A/m^2), I is the current flowing through the conductor in amperes (A), and S is the cross-sectional area in square meters (m^2). However, in our current density plot, we used the unit of A/cm^2 as our devices are small.

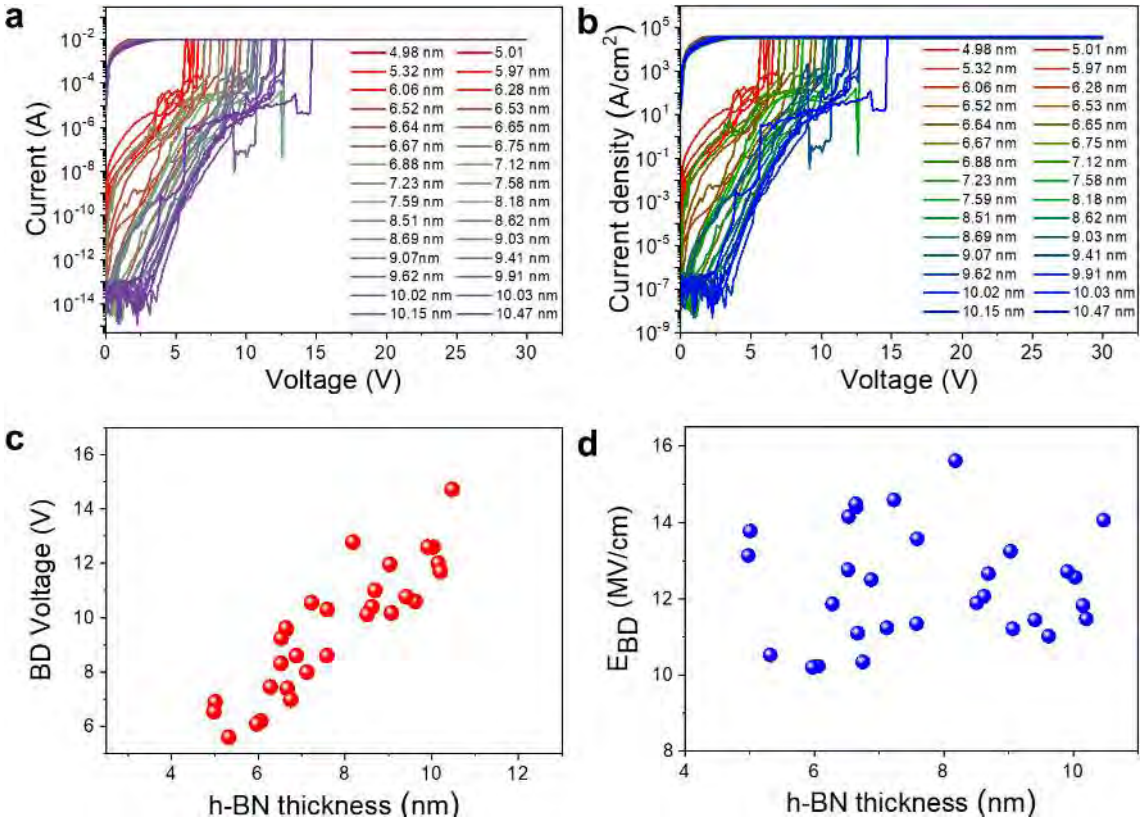

Figure 3.5 Electrical characterization of Pt/ME h-BN/Pt devices. (a) I-V curves of all Pt/h-BN/Pt devices. (b) Current density plot of all devices according to the I-V plot on left. (c) Breakdown voltage versus h-BN thickness plot. (d) Dielectric breakdown strength of the h-BN in Pt/ME h-BN/Pt devices.

In our MIM devices, the cross-sectional area is equal to the cross-point area. As we employ the same size of top and bottom electrodes, the cross-sectional area is approximately 25 μm^2. While there may be small variation in the areas, the current density plot is similar to the I-V plot. The current density of devices is approximately 10^3 A/cm^2 before the hard breakdown occurs. After extracting the breakdown voltage from the I-V curves, we create a BD voltage versus h-BN thickness plot, as depicted in Figure 3.5c. The BD voltages in Pt/ME h-BN/Pt devices range from 5.6 V to 14.72 V and exhibit a clear linear relationship with the h-BN thickness. This phenomenon is reasonable, as the thicker h-BN device requires a higher voltage to form a stronger

electrical field capable of breaking down the h-BN. For future analysis of the BD behavior, we calculate the E_{BD} and display the data in Figure 3.5d. The dielectric breakdown strength is determined using the equation:

$$E_{BD} = V_{BD}/T_{h\text{-}BN}$$

In this equation, E_{BD} represents the dielectric breakdown strength, V_{BD} signifies the breakdown voltage, and $T_{h\text{-}BN}$ is the thickness of the h-BN layer.

The unit of dielectric breakdown stress we utilize is million volts per centimeter (MV/cm). For the Pt/ME h-BN/Pt devices, the EBD value ranges from 10 MV/cm to 14 MV/cm, with a median value of approximately 12 MV/cm. This value is consistent with previously published data displayed in Figure 3.6. This indicates the consistent quality of the ME h-BN stacks used in the Pt/ME h-BN/Pt devices.

The electrical resistance of the devices can be observed in Figure 3.5a, which is dependent on the voltage and current. Typically, the thin h-BN devices exhibit a lower resistance of approximately 10^7 Ω to 10^9 Ω, while the thick h-BN devices exhibit a higher resistance of around 10^{12} Ω to 10^{15} Ω. This is reasonable, as the thicker h-BN stack has better dielectric properties and a higher dielectric constant. When the resistance reaches 10^5 Ω, it suddenly drops to a low level, indicating that a high out-of-plane current is flowing through the devices at that moment. The resistance in the low resistance state is around 10^3 Ω, due to the current limitation set by the SPA (10^{-2} A).

To compare the BD voltages with previous studies, we have collected the BD voltages and h-BN thickness data from relevant literature [207, 208, 213, 123, 216-218]. This data is plotted in Figure 3.6. The h-BN used in these publications was mechanically exfoliated from h-BN crystals. The literature can be categorized into two groups based on the measurement method used: one group used CAFM, while the other used SPA and probe station. There are more CAFM data points in the plot. The contact size between the tip and h-BN layers in the CAFM group was reduced to the nanos-cale, while the device working area in the SPA group could be up to 1300 μm^2. Despite this difference, the BD data from both groups shows a uniform linear trend between the BD voltage and exfoliated h-BN thickness, which is similar to the trend in Figure 3.5c. After calculations, the EBD was found to be around 13 MV/cm, which falls within the range of the EBD value obtained from Pt/h-BN/Pt devices in Figure 3.5d. Our Pt/ME h-BN/Pt devices exhibit similar dielectric breakdown behavior to previous studies using CAFM and SPA methods with devices of varying sizes. This result suggests that mechanically exfoliated h-BN displays stable dielectric performance under different

conditions, and the dielectric breakdown strength of ME h-BN is stable in various devices of different sizes using different measurement tools.

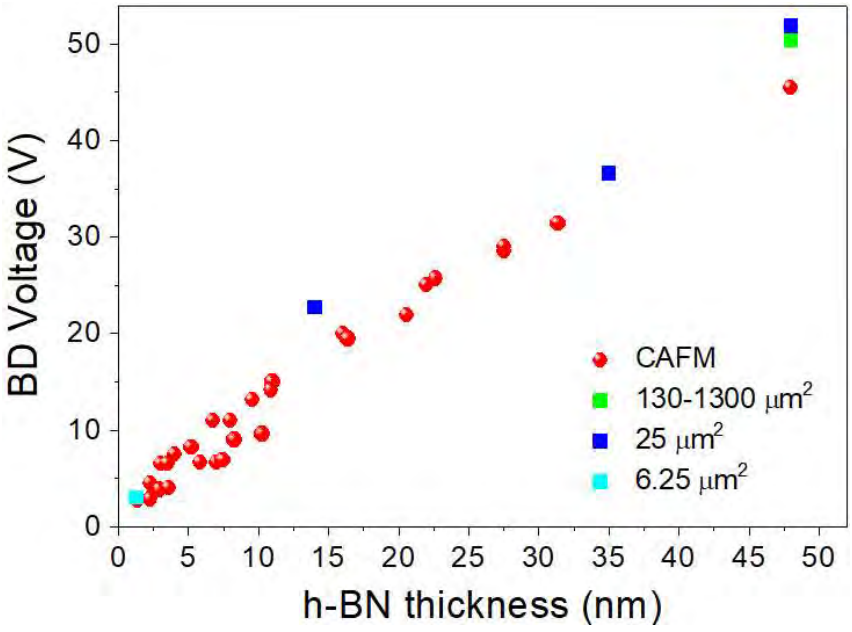

Figure 3.6 Mechanically exfoliated h-BN dielectric breakdown in previous literature [207,208,213,123,216-218].

We utilized a scanning electron microscope (SEM) to analyze the configuration of the Pt/ME h-BN/Pt devices following electrical evaluation. The SEM images of all devices are compiled and presented in Figure 3.7, featuring a 1 μm scale bar. The SEM images reveal that some of the devices exhibit damage resulting from dielectric breakdown during the electrical measurement. The high current observed in Figure 3.5 suggests the formation of conductive filaments between the top and bottom Pt electrodes. The melting of electrodes is probably caused by Joule heating induced by the current through the devices [219]. Additionally, small bright spots can be seen on the top electrodes, possibly indicating melted Pt balls due to the high temperature generated by the current flowing perpendicularly. Out of the 13 Pt/ME h-BN/Pt devices with h-BN thicknesses greater than 8 nm, around 61% of them exhibited melted top electrodes. We propose that thicker h-BN layers may possess greater resistance, resulting in increased heating within the device and ultimately leading to the destruction of the electrodes.

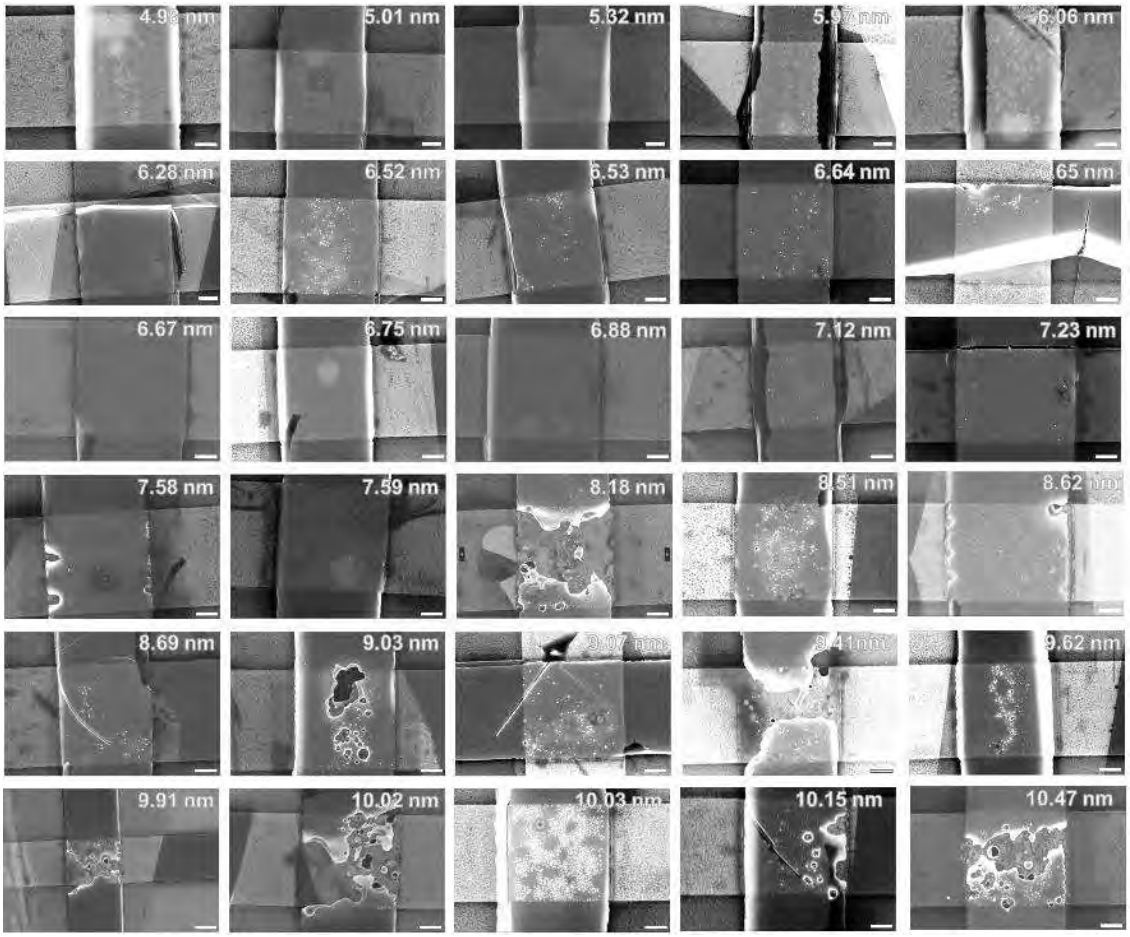

Figure 3.7 SEM images of all Pt/ME h-BN/Pt devices after electric characterization. Scale bar is 1 μm. The thickness of the h-BN flake is marked at the top-right corner in each SEM image.

To compare the topography of Pt devices before and after electrical characterization, we fabricated new devices and obtained SEM images before and after the measurement. SEM images of a typical Pt/ME h-BN/Pt device fabricated with a 6.64 nm thick h-BN flake are presented in Figure 3.8 to illustrate the change in topography before and after the electrical characterization. In Figure 3.8a, the fresh Pt/ME h-BN/Pt device exhibits a clean surface morphology and an undamaged cross-point area, indicating the successful fabrication of the device. After the electrical measurement, some small spots appear on the top electrode as shown in Figure 3.8b. This suggests that the appearance of metal spots is a result of the electrical characterization. The breakdown I-V curve of this device is also included in Figure 3.5a without significant differences compared to other devices' curves. We believe that the small spots are melted Pt, and their formation is

attributed to the intense Joule heating that occurs due to the high current passing through the device, which raises the temperature sufficiently to melt the Pt electrode.

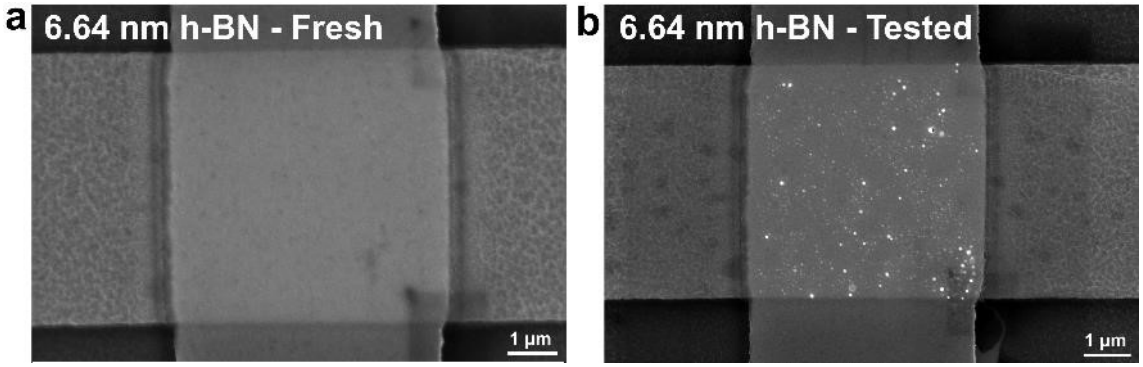

Figure 3.8 Pt/ME h-BN/Pt with thinner h-BN comparison before and after electric characterization. (a) Fresh device shows clean top electrode. (b) Some bright spots appear after electric testing.

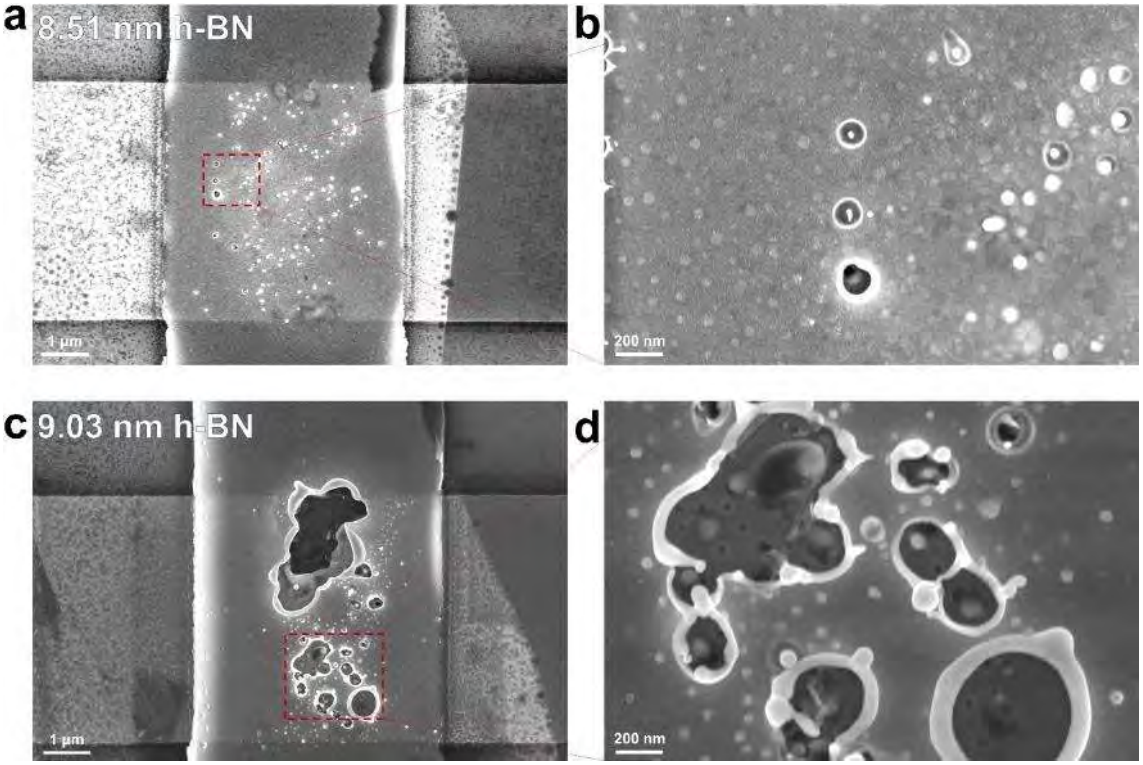

Figure 3.9 Melting of the top electrode of Pt/ME h-BN/Pt devices during the electric measurement. (a) SEM image of a Pt/ME h-BN/Pt device after the electric measurement. (b) Zoom in SEM image of the red square (dash line) in a. (c) SEM topography map of a Pt/ME h-BN/Pt device. (d) Zoom in SEM image of the red square (red dash line) in c.

We also conducted an analysis of two relatively thick Pt/ME h-BN/Pt devices, with their SEM images displayed in Figure 3.9. In the device with an 8.51 nm h-BN layer, only a few light spots are observable on the top electrode. Upon zooming in on the cross-point area of this device, as shown in Figure 3.9b, a hole is visible in the bottom center area, resulting from the melting of the Pt electrode. There are multiple small holes present in the formation step, which could evolve into actual holes if the device continues to generate heat. Moreover, since the top electrode comprises solely of a Pt film without an adhesion layer, the light spots are metallic balls composed of Pt.

In Figure 3.9d, severe damage to the top electrode in the device is evident. The zoomed-in image reveals that the top electrode has melted, creating several large holes. It can be observed that the h-BN layer beneath the top electrode has sustained partial damage during the electrical measurement. Referring to Figure 3.7, it appears that thicker h-BN devices possess superior dielectric properties; however, they are more prone to damaging the top electrode and/or other layers if subjected to a strong enough electric field.

3.3.2. Electrical characterization of Au/ME h-BN/Au devices

In this work, we have fabricated Au/ME h-BN/Au devices to compare the dielectric breakdown with the Pt/ME h-BN/Pt devices. Figure 3.10 displays the AFM topography map of 12 h-BN flakes on the Au bottom electrodes, which were obtained using the tapping mode.

Figure 3.11 illustrates the h-BN thickness obtained from the AFM images presented in Figure 3.10. We utilize the same fabrication and characterization method for the Au/ME h-BN/Au devices as for the Pt/ME h-BN/Pt devices to ensure their quality. The thicknesses of the h-BN flakes in the 12 Au/ME h-BN/Au devices range from 4.33 nm to 10.14 nm, which is similar to the range observed in the Pt/ME h-BN/Pt devices. Additionally, the uniformity of the h-BN quality is comparable to that of the Pt samples, as we employ the same method to exfoliate the h-BN flakes. All devices depicted in Figure 3.10 meet the requirements for proceeding with the Au/ME h-BN/Au device fabrication process. The thickness range of h-BN in the Au devices ensures that a reliable and feasible comparison with the Pt devices can be made. Although the sample size is smaller for the Au devices compared to the Pt devices, further Au devices will be presented in subsequent sections.

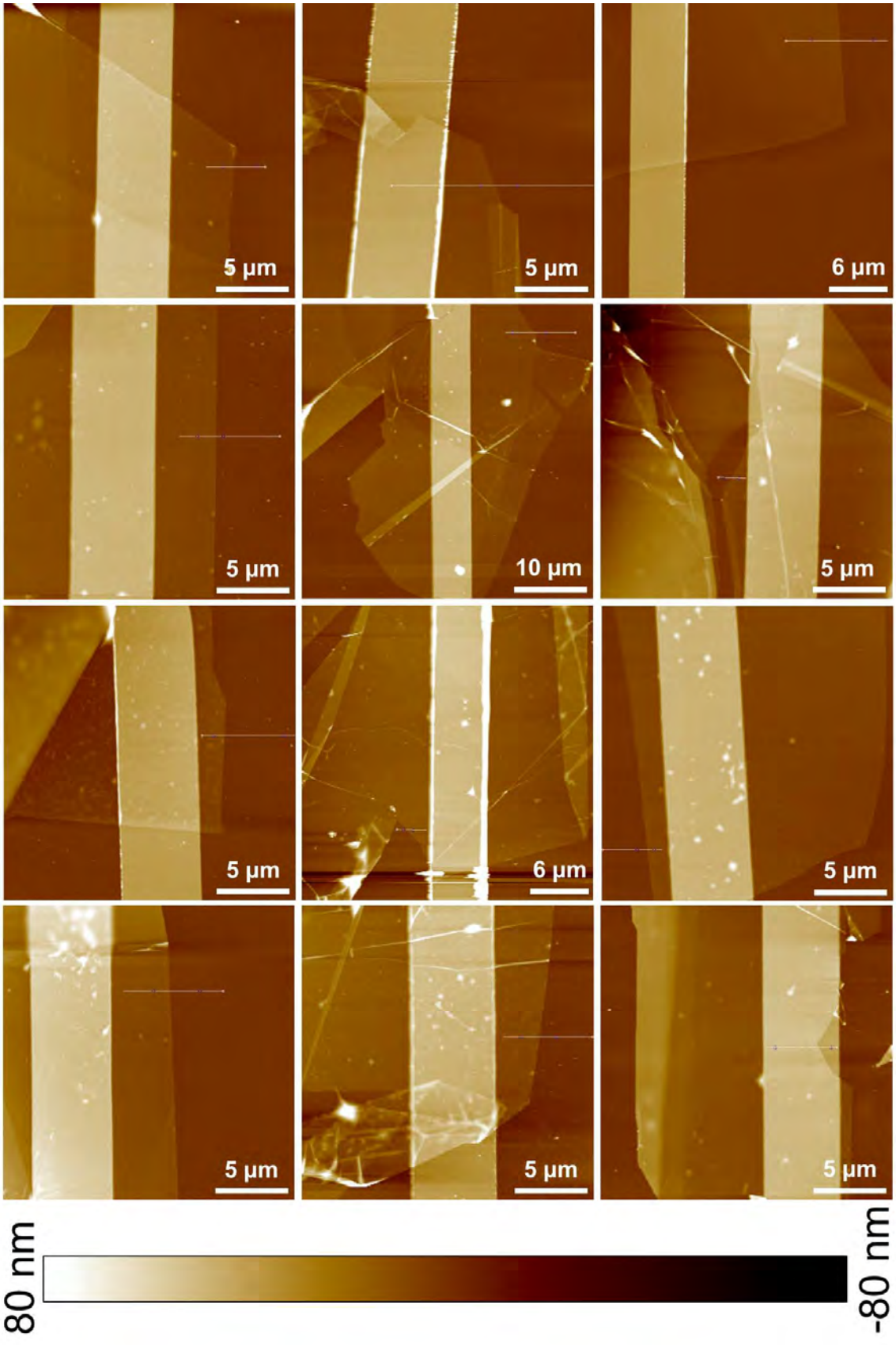

Figure 3.10 AFM topography map of 12 exfoliated h-BN on Au electrodes obtained via tapping mode.

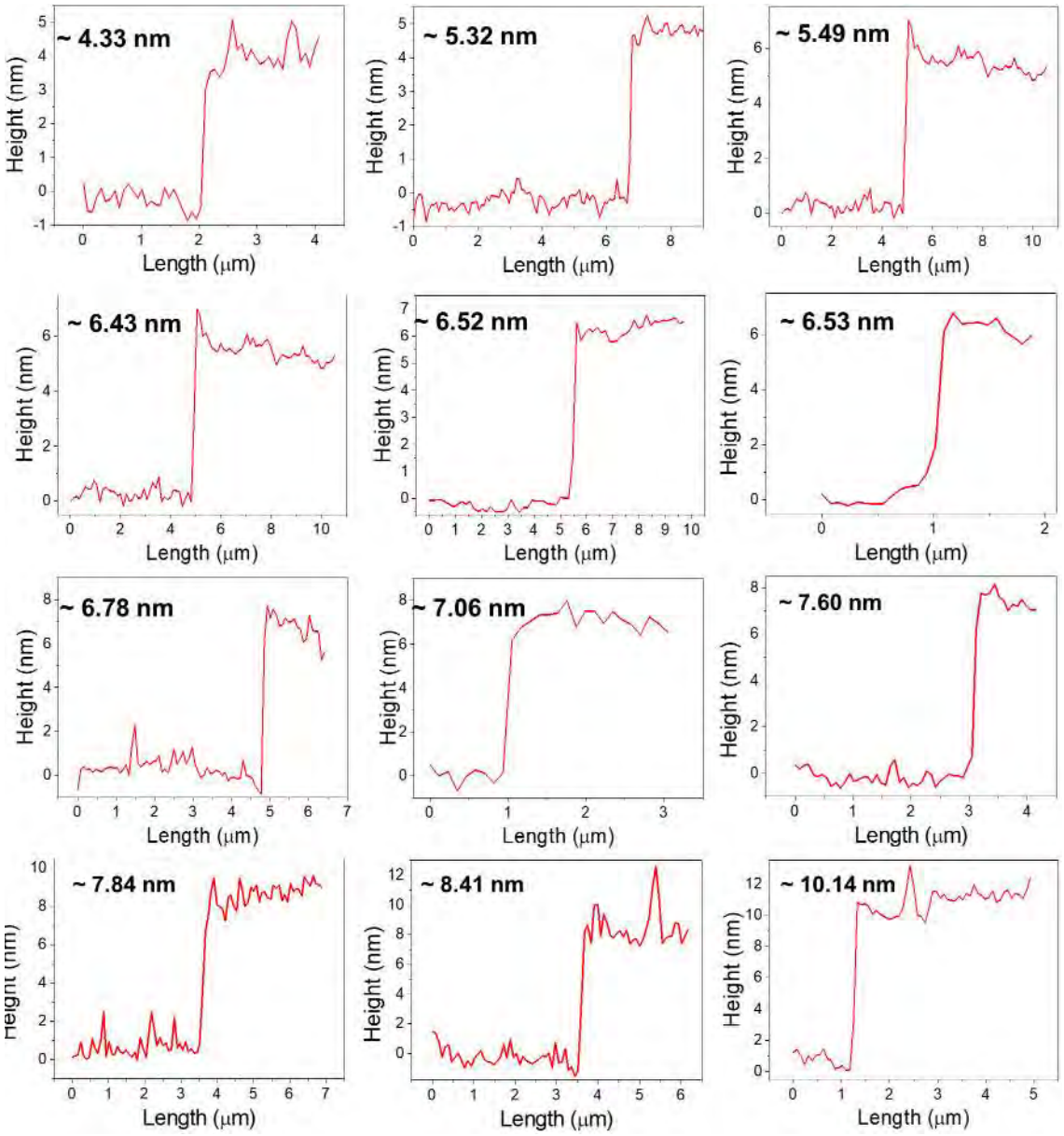

Figure 3.11 Height analysis of the cross-section in 12 exfoliated h-BN flakes on Au bottom electrodes and h-BN thickness.

The same electrical characterization strategy employed in studying Pt/ME h-BN/Pt devices was utilized to assess the Au/ME h-BN/Au devices, and the data obtained is summarized in Figure 3.12. The I-V curves of the 12 Au/ME h-BN/Au devices are displayed in Figure 3.12a. All devices were successful in reaching breakdown under the applied stress. Although two devices (5.49 nm and 7.06 nm) possessed lower current limitations (10^{-3} A), this did not impact the conclusion. The current density of the devices was calculated and presented in Figure 3.12b. The breakdown behavior of h-BN

in Au/ME h-BN/Au devices was similar to that in Pt/ME h-BN/Pt devices, as Au is also an inert metal. However, the breakdown voltages of the Au devices were different from those of the Pt devices, as demonstrated in Figure 3.12c. The BD voltages of Au/ME h-BN/Au devices showed a lower range from 5 V to 9 V compared to the BD voltages in Pt devices, and the BD voltages of Au devices did not exhibit a linear relationship with the h-BN thickness. The median dielectric breakdown strength of Au/ME h-BN/Au, calculated in Figure 3.12d, was approximately 10 MV/cm, which was lower than the EBD in Pt devices. To investigate whether the BD was influenced by the top electrode thickness, the results for 40 nm and 100 nm Au layers as top electrodes were compared. Unfortunately, the findings presented in Figure 3.12c and Figure 3.12d indicated that there was no significant difference between the Au devices with 40 nm and 100 nm thick top electrodes. This suggests that the top electrode thickness had no significant impact on the dielectric BD performance in Au devices.

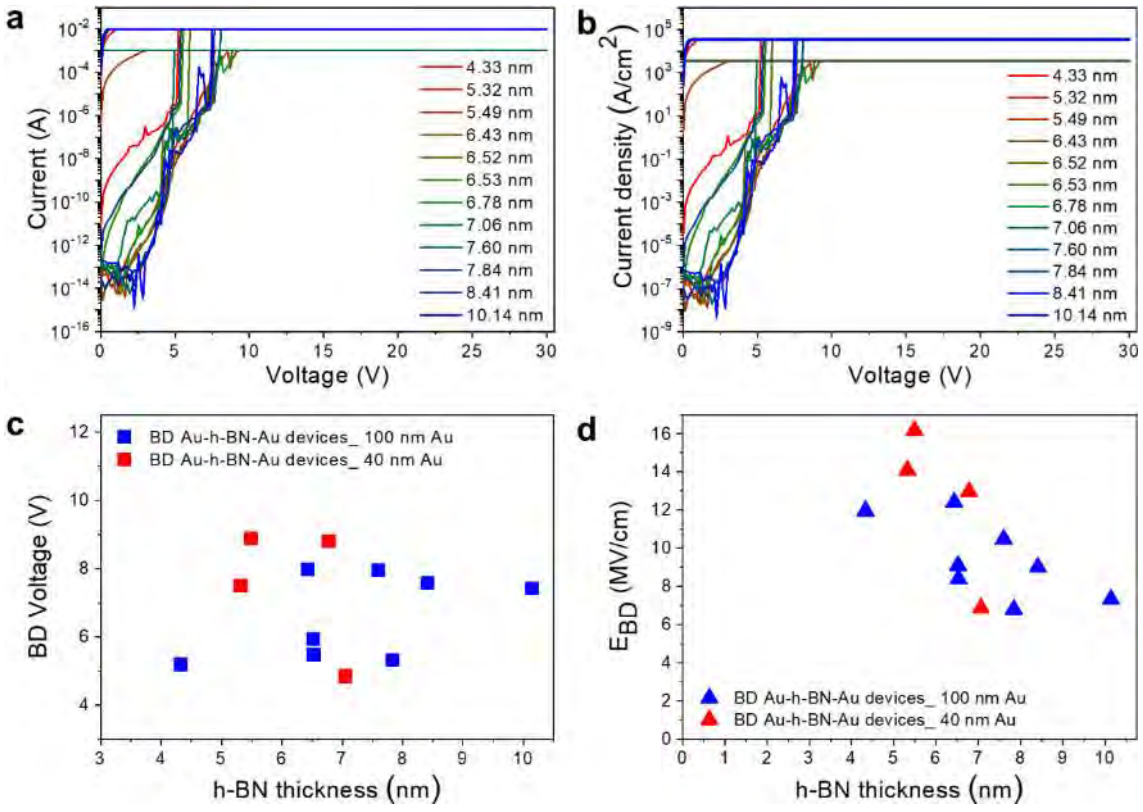

Figure 3.12 Electrical characterization of Au/ME h-BN/Au devices. (a) BD curves of all Au/h-BN/Au devices. (b) Current density plot based on the data in a and device size. (c) BD voltage versus h-BN thickness. (d) E_{BD} of the h-BN in Au/ME h-BN/Au devices.

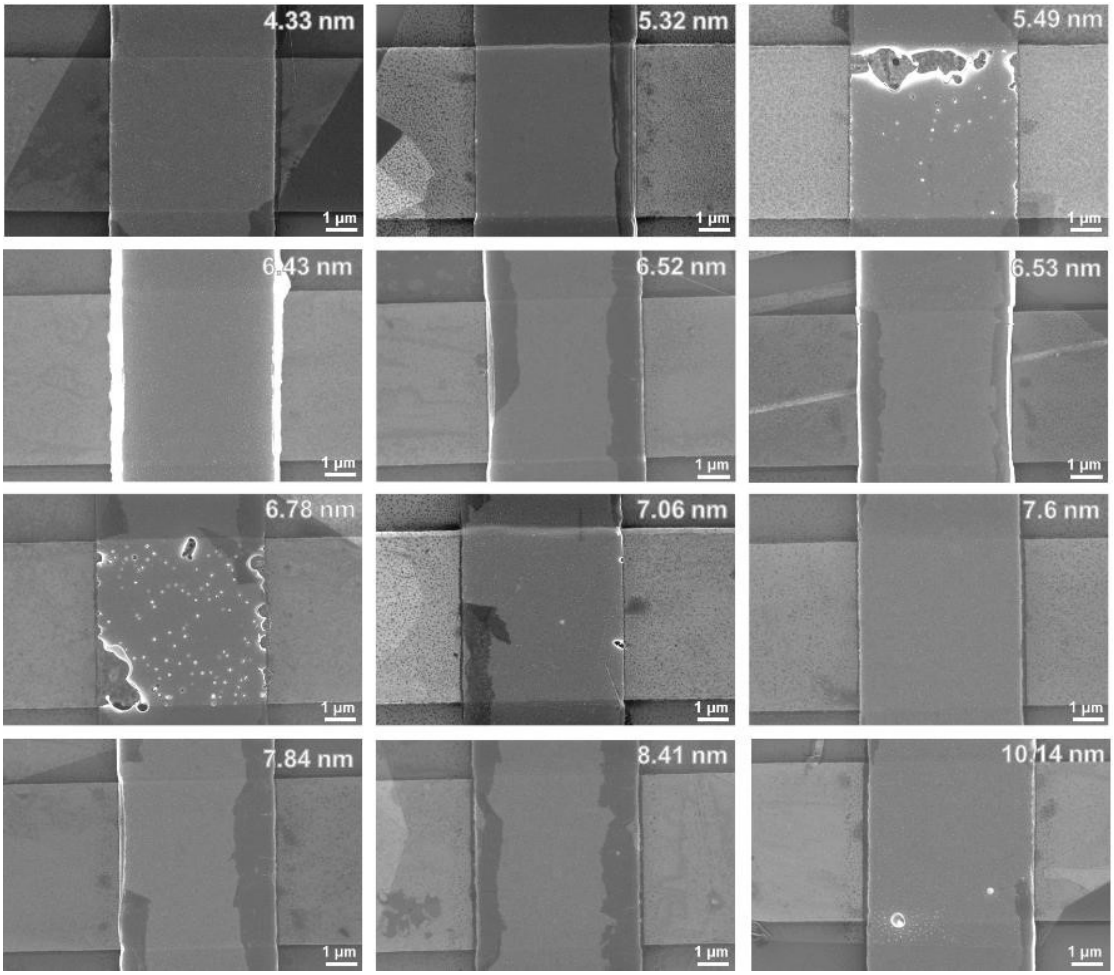

Figure 3.13 SEM images of 12 breakdown Au/ME-h-BN/Au devices after stressing.

In order to determine the cause of the varying E_{BD} between Pt and Au devices, we captured SEM images of both types of devices after undergoing electrical characterization. By analyzing these images, as shown in Figure 3.13, it appears that Au/ME h-BN/Au devices are susceptible to damage even when a thin h-BN layer is present (5.49 nm and 6.78 nm), whereas Pt devices show less susceptibility to damage. The most likely explanation for this difference is that there are higher resistance levels in the damaged devices, such as contact resistance, which generates a considerable amount of Joule heat during the BD process. This heat can ultimately result in the destruction of the top Au electrode.

We acquired ten Au/ME h-BN/Au devices that exhibited melting behavior during the electrical measurement process without displaying BD behavior. Among these devices, half of them had a 100 nm Au layer as the top electrode, while the others had a 40 nm Au layer. Although the differences in electrode thicknesses may seem significant,

our results indicate that it does not impact the devices' electrical performance, as demonstrated in Figure 3.12c.

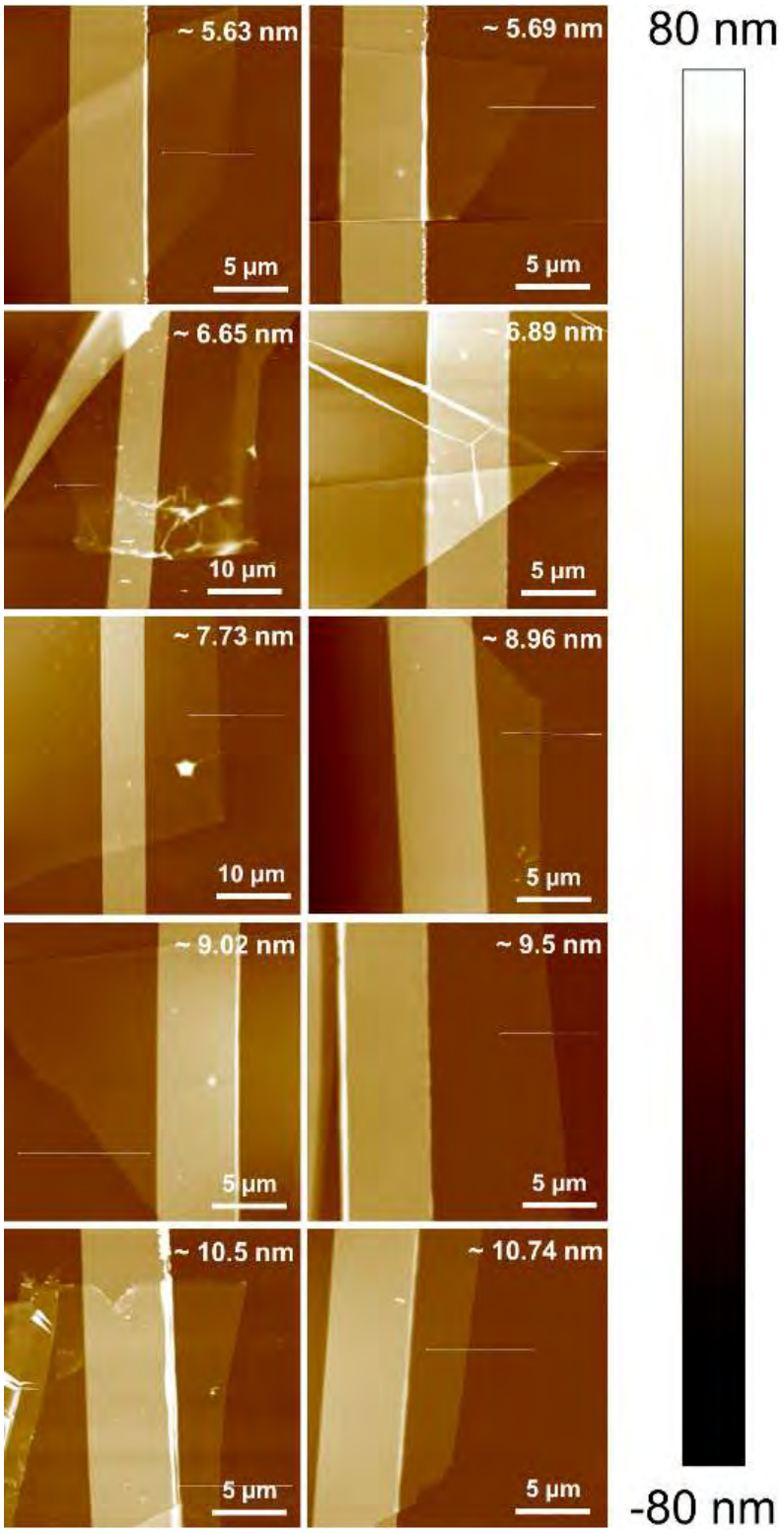

Figure 3.14 AFM topography map of 10 exfoliated h-BN on Au electrodes obtained via tapping mode. The thickness of the h-BN is displayed at the top-right corner.

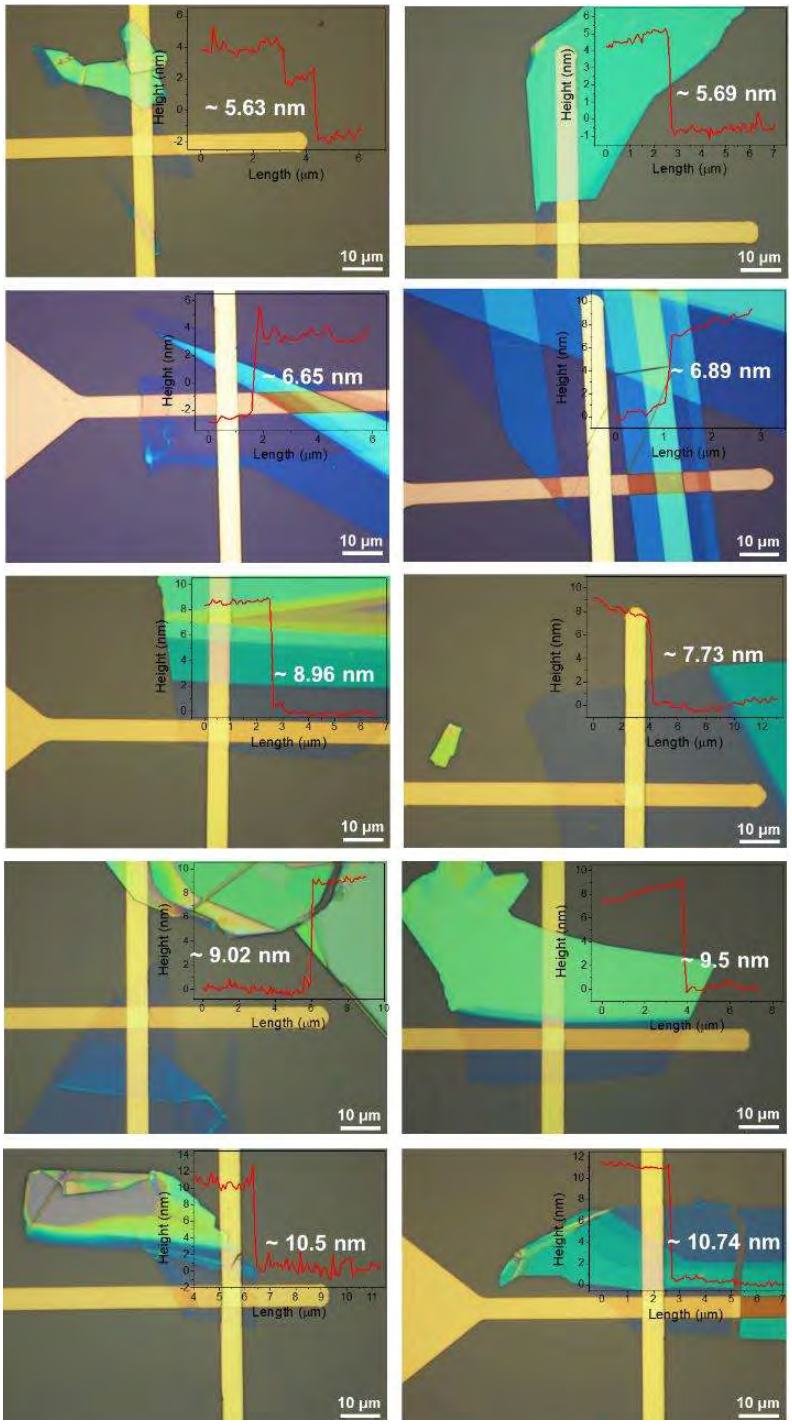

Figure 3.15 Optical images of 10 fresh Au/ME-h-BN/Au devices before applying stress. These devices all melted after the electric characterization. The inset plot at the top-right corner indicates the thickness of h-BN in the device.

We collected AFM topography maps of all ten devices when h-BN was transferred onto the bottom electrode, as shown in Figure 3.14. The optical images of these devices before electrical testing are presented in Figure 3.15. From these images, it is evident that there is no significant difference between the melted devices and the 12 breakdown

devices. The thickness of the h-BN stack measured by AFM is presented in the inset plots in each image (top-right corner). The thickness of the h-BN flakes ranged from 5.63 nm to 10.74 nm, which is similar to that of the successful BD Au/ME h-BN/Au devices.

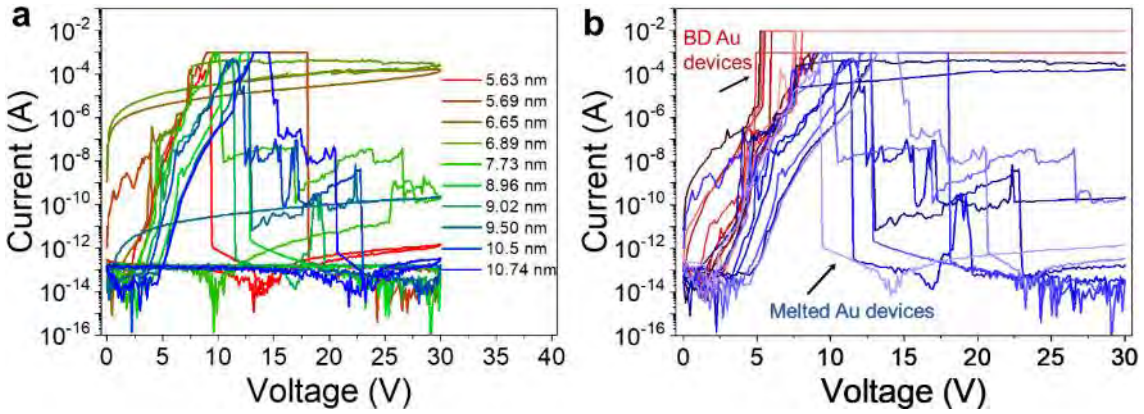

Figure 3.16 I-V curves of Au/ME h-BN/Au devices. (a) I-V curves of melted Au/ME h-BN/Au devices. (b) Forward curves of melted and BD Au/ME h-BN/Au devices. The red group presents BD Au devices, and the blue group presents melted Au devices.

The outcome exhibited in Figure 3.16 was obtained using the same electrical measurement technique and the identical parameters employed for the Pt and Au devices presented earlier. As demonstrated in Figure 3.16a, the majority of the I-V curves fail before reaching the current restriction (10^{-2} A). Subsequently, we isolate the forward portion of the I-V curves from the melted and BD Au devices and depict them in Figure 3.16b. The red line group represents the forward I-V curves of the BD Au devices, while the blue line group represents the forward I-V curves of the melted Au devices. It is evident that the melted Au devices exhibit a similar current increasing trend as the BD Au devices, but the current decreases when it reaches 10^{-3} A, which is lower than the current limitation (10^{-2} A) for both types of Au devices. This melting phenomenon occurs regardless of the thickness of h-BN and electrodes used indicating a more complex mechanism not discovered.

The distinct shape of the I-V curves observed between the BD and melted Au devices in devices with same fabrication process can be attributed to the fact that some devices experience current overshoot during the I-V curve and others don't. Current overshoot takes place when a device drives currents higher than the current limitation imposed. For the BD Au devices (red group in Figure 3.6b) there is no current

overshoot, as when they break, they just stay at the current level imposed during the I-V curve. However, for the melted Au devices (blue group in Figure 3.6b) there is current overshoot, which results in melting of the Au wires and a sharp current reduction. However, this current overshoot is not visible during the I-V curve because the measurement is very slow—this is normal in wide current dynamic range measurements—and this is a phenomenon that takes place very fast. The current overshoot takes place because the BD event (for some devices) is much faster than the time needed by the SPA to active the current limitation (typically 70 μs) [220]. The reason why current overshoot happens in some devices and not others is the different BD time of each device, which is related to the atomic structure of the device and hence cannot be carefully controlled. In any population of MIM cells like the ones studies in this PhD thesis, there is a stochastic variability in the BD time, which is unpredictable. Therefore, if one establishes a threshold time (the 70 μs needed to activate the current limitation of the SPA), some devices would break after and some others would break earlier, leading to devices that do not show and do show overshoot (respectively). However, the investigation into the origins of atomic structural variability is beyond the scope of this study.

The SEM images of the 10 melted Au/ME h-BN/Au devices are presented in Figure 3.17. All devices' electrodes are melted after electric characterization. The melting in the devices is caused by the current overshoot which has been described in the last paragraph. The unlimited high current produced exceed Joule heat that the electrodes can withstand. In the total 22 Au/ME h-BN/Au devices (12 BD and 10 melted), 12 of the Au/ME h-BN/Au devices melted their Au electrode regardless of the h-BN thickness during the electric characterization. In addition, the melting of electrodes also occurred in Pt/ME h-BN/Pt, although the probability is lower than that in Au devices. The melting of Pt electrodes proves that the current overshoot will occur randomly in devices whatever the metal used in the devices.

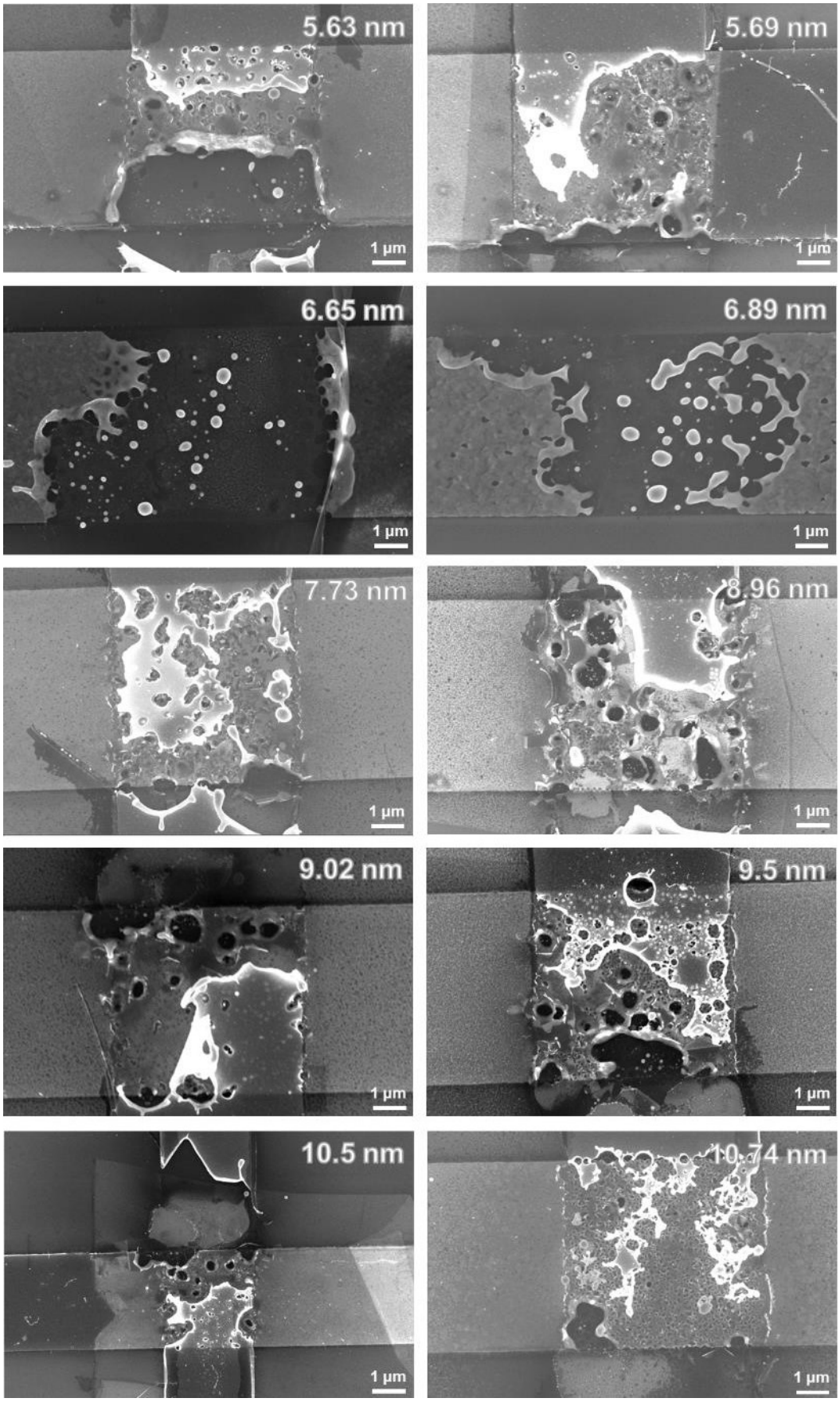

Figure 3.17 SEM images of melted Au/ME-h-BN/Au devices after stress.

3.3.3. Transfer Au/ME h-BN/Au devices

To study the impact of the top electrode deposition technique on metal/h-BN/metal devices, we employ an electrode transfer method instead of electron beam evaporation in order to avoid potential harm to the h-BN flakes during the deposition process.

The method of metal transfer that we utilized is similar to the strategy described in previous literature [221]. With respect to the adhesion force between the wafer and the metal electrode, we believe that Au is a suitable choice as a transfer electrode. Pt, on the other hand, is challenging to attach to the wafer without an adhesion layer. However, if we add an adhesion layer, such as a Ti layer, it will be impossible to peel off the Ti/Pt due to the strong adhesion force between the Ti and the wafer. Additionally, the presence of an adhesion layer will impact the breakdown performance, as the adhesion layer will participate in the BD process. For these reasons, we have selected Au as the electrode for transfer.

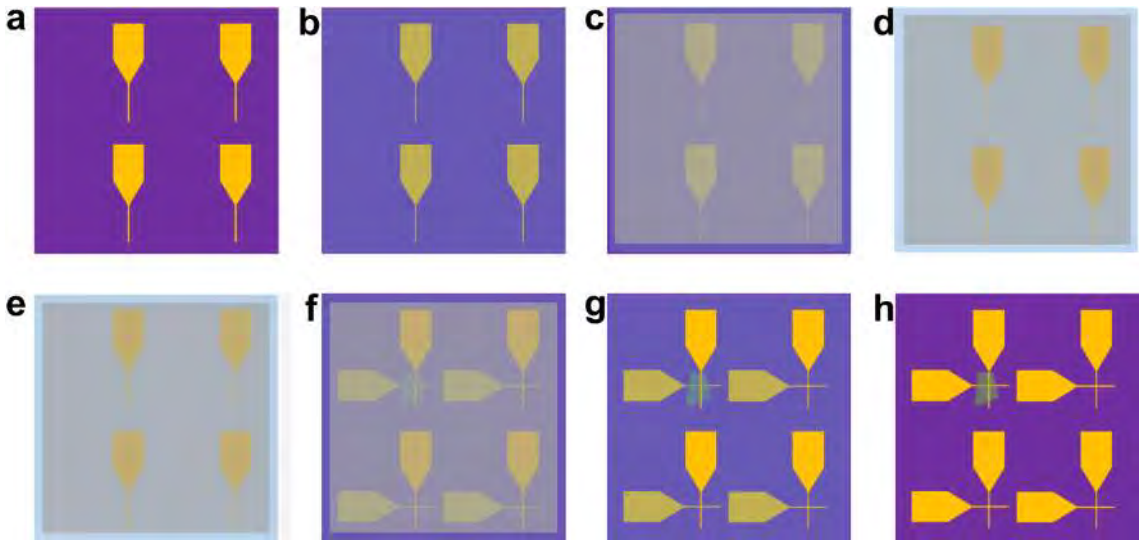

Figure 3.18 Fabrication process of transfer Au/ME h-BN/Au devices. (a) Prepare the top electrode for transfer via photolithography, electron beam evaporation, and lift-off. (b) Spin coating of 1.5% PLA on the top electrode and bake at 100°C for 5 min. (c) Cover PDMS on the PLA/Au/SiO_2/Si stack. (d) Put the PDMS/PLA/Au/SiO_2/Si stack in DI water and use an ultrasonic cleaner to peel off the top electrode from the wafer. (e) Pick the PDMS/PLA/Au stack to a slide. (f) Use the transfer stage to transfer the PDMS/PLA/Au stack on the h-BN/Au substrate. (g) Release the PDMS and get PLA/Au/h-BN/Au/SiO_2/Si. (h) Sink the stack into CH_2Cl_2 to remove the PLA film and clean it in ethanol.

The illustration of the transfer Au/ME h-BN/Au device fabrication process is presented in Figure 3.18.

i) Firstly, the Au electrodes are prepared using photolithography, electron beam evaporation, and lift-off. Only the Au layer is deposited on the substrate, enabling it to be easily removed from the substrate due to the suitably low adhesion force between the Au and the wafer. Additionally, the substrate is prepared with bottom electrodes, and the ME h-BN is transferred to the bottom electrode via a dry transfer method.

ii) Secondly, a 1.5% polylactic acid (PLA) solution is spin-coated onto the Au/SiO2/Si wafer, and then baked at 100 ℃ for 5 min to remove any excess liquid in PLA. Finally, the Au electrodes are secured in place by the PLA film, as shown in Figure 3.18b.

iii) Thirdly, we then cut a piece of PDMS sufficient to span all electrodes, thereby creating a PDMS/PLA/Au/SiO_2/Si layered stack from top to bottom, as illustrated in Figure 3.18c.

iv) Fourthly, the Au electrodes array is peeled off the substrate using an ultrasonic cleaner. The sample is immersed in DI water and cleaned until the PDMS/PLA/Au stack is separated from the substrate (Figure 3.18d).

v) Fifthly, a slide is used to pick up the PDMS/PLA/Au stack and dry it for the next step (Figure 3.18e).

vi) Sixthly, the Au electrodes array is then transferred to the substrate with h-BN and a bottom Au electrode. During the transfer process, the top electrode and h-BN are aligned on the bottom electrode, as shown in Figure 3.18f.

vii) Seventhly, the PDMS is then thermally released from the stack by heating at 90 ℃ for 2 min, leaving the PLA/Au on the substrate (Figure 3.18g).

viii) Finally, the PLA/Au/h-BN/Au/SiO_2/Si is immersed in CH_2Cl_2 solution for 10 min to remove the PLA film and clean the sample in ethanol (Figure 3.18h).

Similar to the previous devices presented, the h-BN flakes transferred onto the bottom electrodes were characterized using AFM in tapping mode, and the results are presented in Figure 3.19. The thickness of each h-BN is inset at the top-right corner, and all thicknesses are less than 10 nm, with sufficient size for the top electrodes.

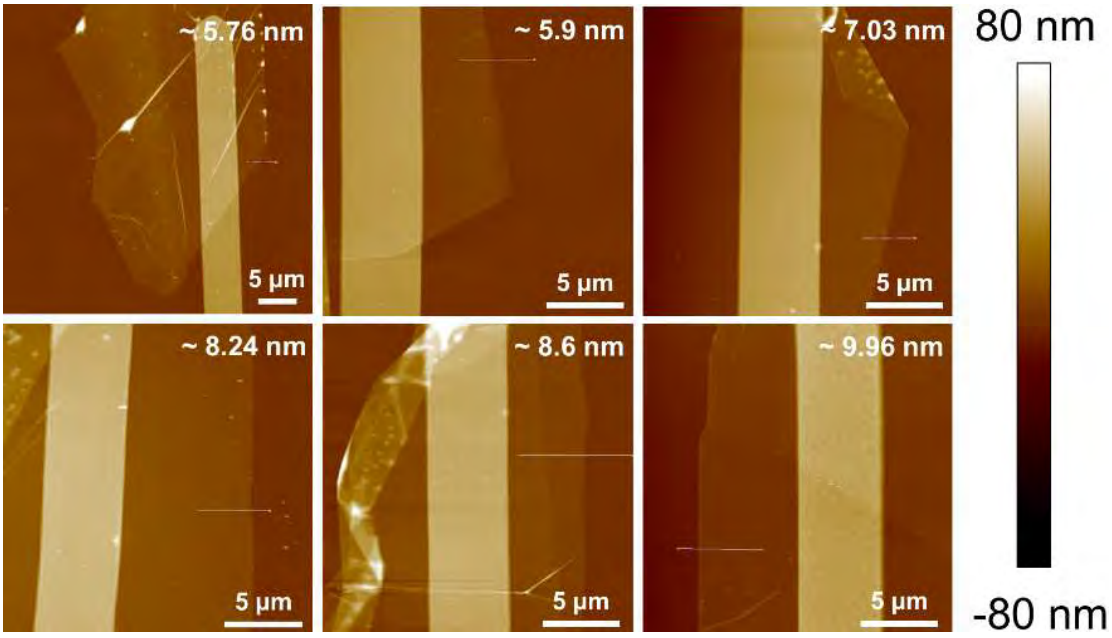

Figure 3.19 AFM topography map of mechanically exfoliated h-BN on Au electrodes for transfer Au/h-BN/Au devices. The thickness of h-BN is inset at the top-right corner.

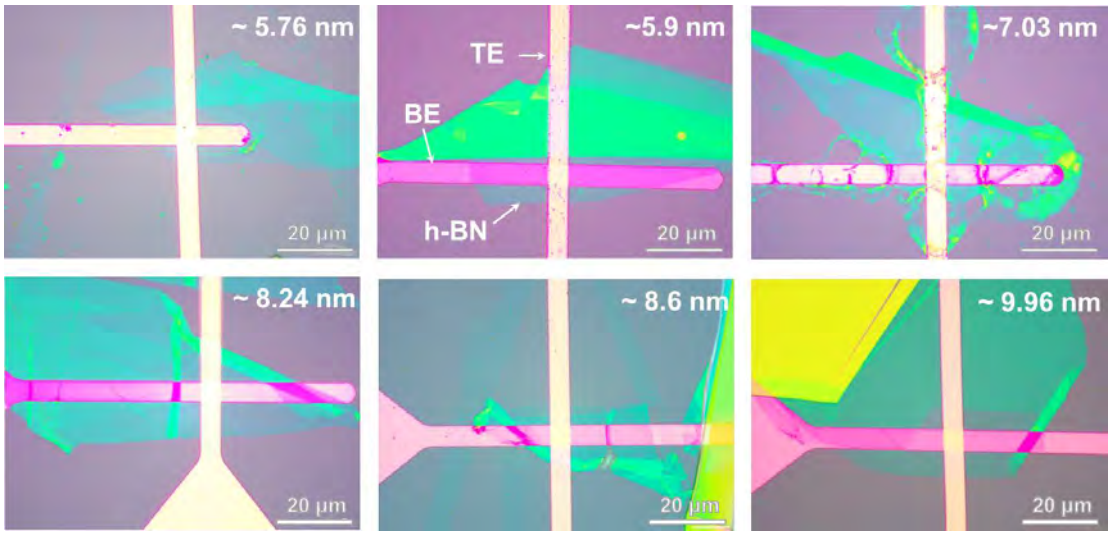

Figure 3.20 Optical microscope images of transferred Au/ME h-BN/Au devices.

The optical microscope images of the fabricated transfer Au/ME h-BN/Au devices are displayed in Figure 3.20. The majority of the devices exhibit a clean appearance post-fabrication within these images. Nonetheless, minor residue is observed in some devices, as exemplified by those with thicknesses of 5.76 nm, 7.03 nm, and 8.6 nm. We postulate that these residues are remnants of PLA that did not completely dissolve in CH_2Cl_2. However, such residues are not expected to impact the BD, given that the

electrical current will not traverse the residual areas. In any case, we have successfully crafted the Au/ME h-BN/Au devices employing the Au electrode transfer technique.

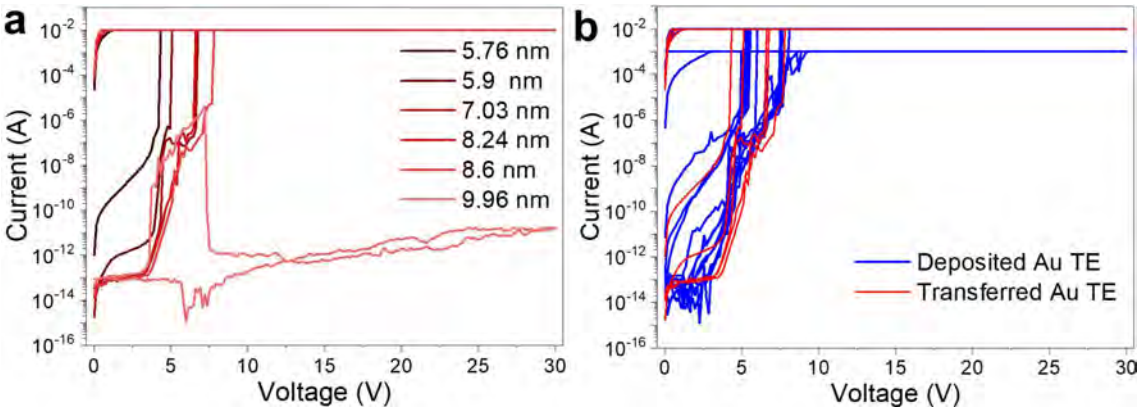

Figure 3.21 Electrical measurement result of transfer Au/ME h-BN/Au devices. (a) I-V curves of transfer Au/ME h-BN/Au devices. (b) Comparison of BD curves in devices using transfer Au and deposition Au as top electrode. Bule lines are the I-V curves of devices with deposited Au top electrode. Red lines are the I-V curves of the devices with transferred Au top electrode.

Using the same electrical measurement procedure for the Pt and Au devices previously mentioned, an RVS ranging from 0 to 30 V was applied to the top electrode of the transfer Au/ME h-BN/Au devices. The I-V curves of the transferred Au/h-BN/Au devices are illustrated in Figure 3.21a. Similar to the Au/ME h-BN/Au devices with a deposited top electrode (TE), certain devices exhibited breakdown behavior, while others melted during the testing process. In total, six Au/ME h-BN/Au devices with transferred TE were examined, five of which demonstrated dielectric breakdown, and only one device (h-BN thickness ~9.96 nm) experienced melting during the stressing. The breakdown voltage followed the trend that thicker h-BN requires a higher breakdown voltage, as the breakdown in h-BN occurs layer-by-layer [123]. The residuals on the devices did not affect the basic BD behavior, as the I-V curves of the devices with transferred Au TE were normal compared to the curves obtained from the device with deposited Au TE. It appears that the ratio of successfully BD devices with transferred Au TE is higher than that of devices with deposited Au TE, as half of the deposited Au/ME h-BN/Au devices melted during the electric characterization step.

We have collected all the BD curves for the Au/ME h-BN/Au devices, which feature both deposited and transferred top electrodes, and have charted these findings, as displayed in Figure 3.21b. Our analysis reveals that the I-V curves for all devices exhibited a high degree of similarity, irrespective of the technique employed for the top electrode's fabrication.

The I-V plot in Figure 3.21b indicates that employing electron beam evaporation to deposit Au as the top electrode does not appear to have a significant effect on the BD characteristics of the h-BN layer within the Au/ME h-BN/Au devices. The BD curves for the devices with transferred Au top electrodes closely mirrored those of the devices with deposited Au top electrodes. It is our proposition that these two methodologies are equally viable for the construction of Au/ME h-BN/Au devices intended for investigating the dielectric breakdown properties of ME h-BN materials.

The comparison of the Au/ME h-BN/Au devices before and after electric measurement in topography obtained via SEM can be observed in Figure 3.22. It is important to note that two thick h-BN devices were destroyed due to melting of the electrodes. However, other devices show negligible changes after electrical characterization.

The device using ~8.6 nm h-BN displays some light spots that are likely to be Au particles, which is also observed in Pt devices. These SEM images after stress testing confirm that the transfer Au method is interchangeable with electron beam evaporation deposited Au as a top electrode in the Au/ME h-BN/Au devices. The devices with transferred Au as top electrode show identical structure and accurate dimensions of the devices compared to the devices using deposited Au as top electrode. It is worth noting that the performance and failure of the devices are similar in the Au/ME h-BN/Au devices with transferred Au top electrode and deposited Au top electrode.

While the method of transferring Au electrodes yields a higher incidence of BD curves, it is accompanied by a more intricate fabrication process, which in turn results in a reduced device yield. Additionally, the constraint to a specific type of electrode may present limitations in broadening the method's applicability.

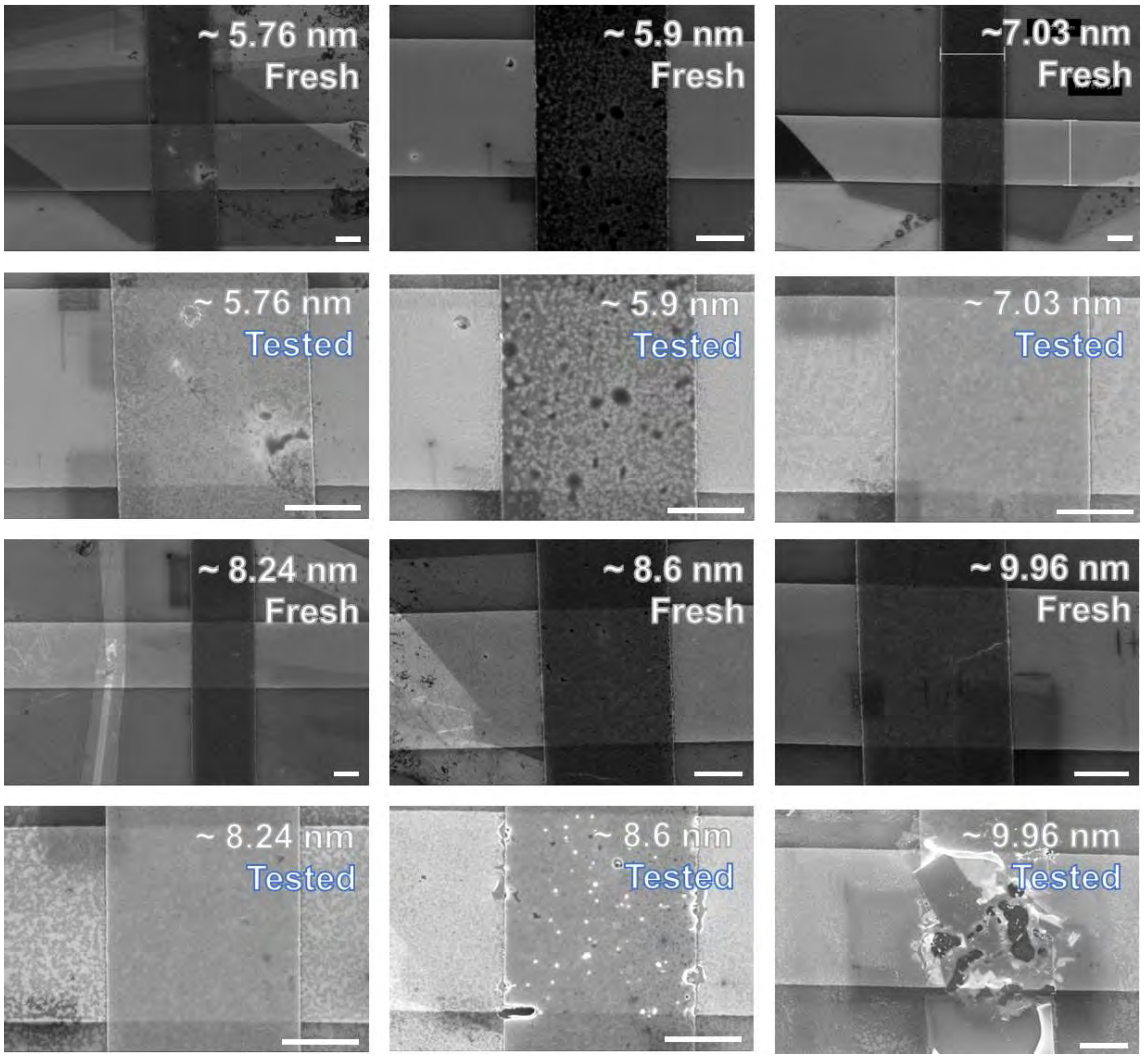

Figure 3.22 SEM images of 6 Au/ME h-BN/Au devices with transferred Au TE before and after electrical characterization. Scale bar is 2 μm.

3.3.4. Electric characterization of Au/Ti/ME h-BN/Au devices

To compare the dielectric BD in the devices with different top electrodes, we used Pt, Au, and transferred Au as the top electrodes to fabricate metal/ME h-BN/metal devices. Pt and Au are both inert metals, and to widen the research scope, we chose Ti as the top electrode to observe the BD behavior in devices with active metals.

The fabrication process for the Au/Ti/ME h-BN/Au (from top to bottom) devices is identical to that of the Pt and Au devices previously described. All metal layers are fabricated using photolithography, electron beam evaporation, and lift-off techniques. Following the formation of the Ti layer via electron beam evaporation, the top layer of

Au is deposited without releasing the vacuum state in the chamber, serving as a protective layer to prevent oxidation of the Ti layer in the air.

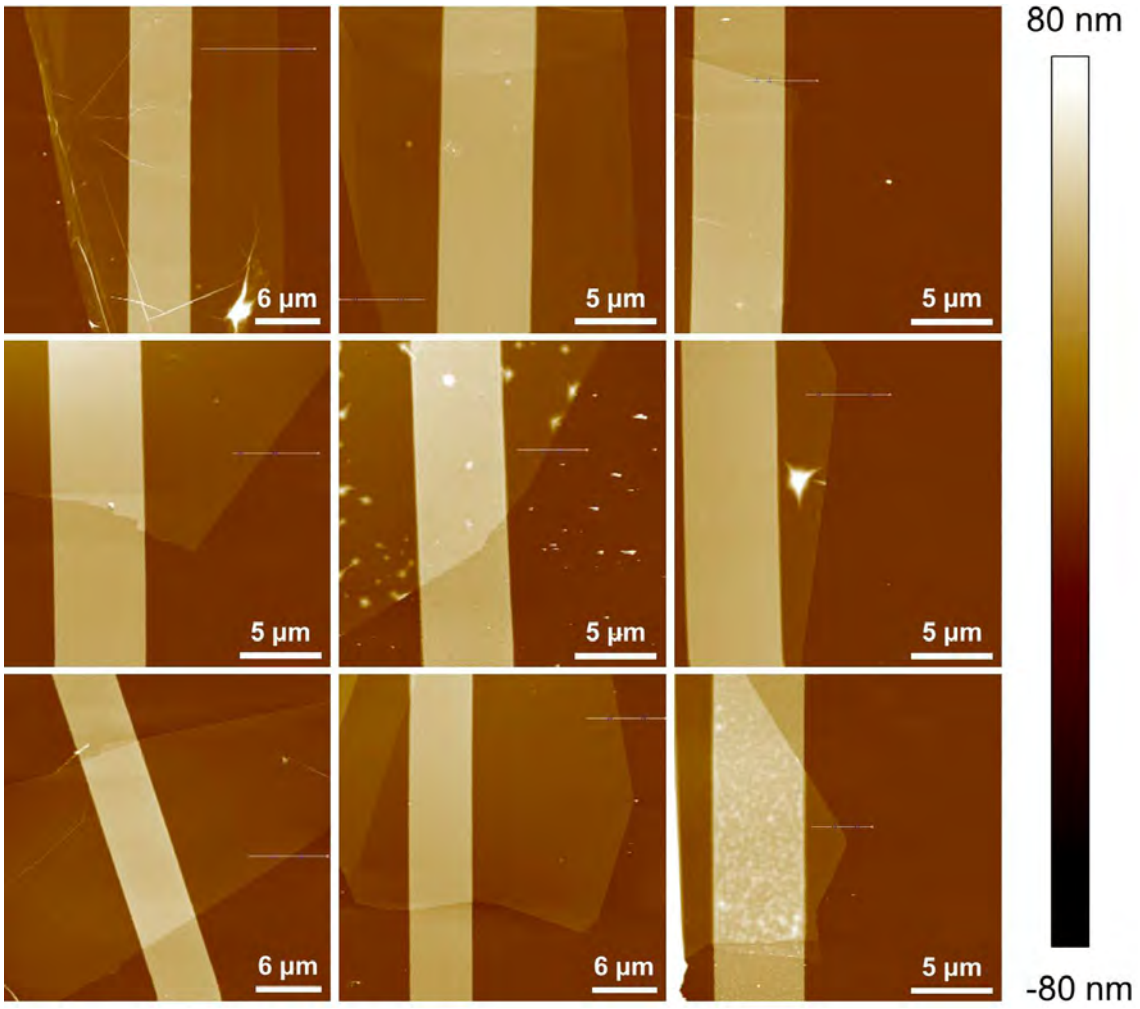

Figure 3.23 AFM topography map of 9 exfoliated h-BN on Au electrodes for Ti device.

We have fabricated nine Au/Ti/ME h-BN/Au devices and collected electrical data from them. In Figure 3.23, the AFM topography map of the h-BN flakes on the bottom Au electrodes is displayed, and Figure 3.24 shows the corresponding thickness of h-BN flakes in each device. From Figure 3.23, it is evident that all h-BN stacks have been transferred onto the bottom electrode accurately, and both the h-BN and bottom electrode are clean and flat. The thicknesses of the nine h-BN flakes range from 5.34 nm to 9.44 nm, as depicted in Figure 3.24. The thickness of h-BN is controlled within a similar range as the h-BN utilized in Pt and Au devices characterized previously to facilitate better comparison.

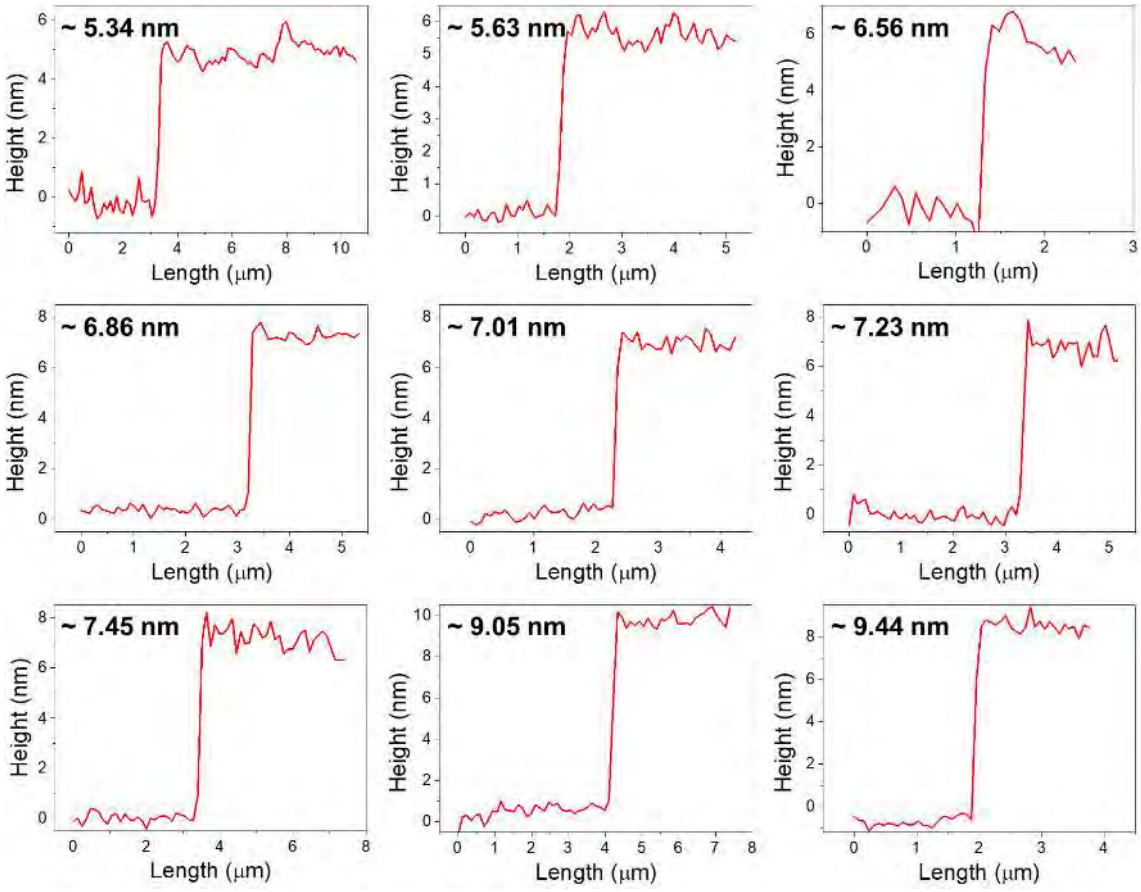

Figure 3.24 Thickness of 9 exfoliated h-BN flakes in Figure 3.23.

After the successful fabrication of the Au/Ti layer serving as both the top electrode and the passivation layer, we employed a SEM to scrutinize the topography of the complete Au/Ti/ME h-BN/Au devices. This examination verified the proper construction of the devices, ensuring accuracy in structural integrity, dimensions, and the positioning of the top electrodes. The SEM images presented in Figure 3.25 offer an enlarged perspective on the novel cross-point junctions. They demonstrate that the cross-point regions of each top electrode are exceptionally clean, whereas the bottom electrodes seem to be obscured, likely due to the h-BN layer adhering to their surfaces. The central SEM image at the base of Figure 3.25 shows a minor Au/Ti layer residue, an artifact from the lift-off process, which is deemed to have no bearing on the forthcoming electrical measurements. These SEM images confirm the successful fabrication of the nine devices, permitting us to advance to the subsequent phase of electrical characterization.

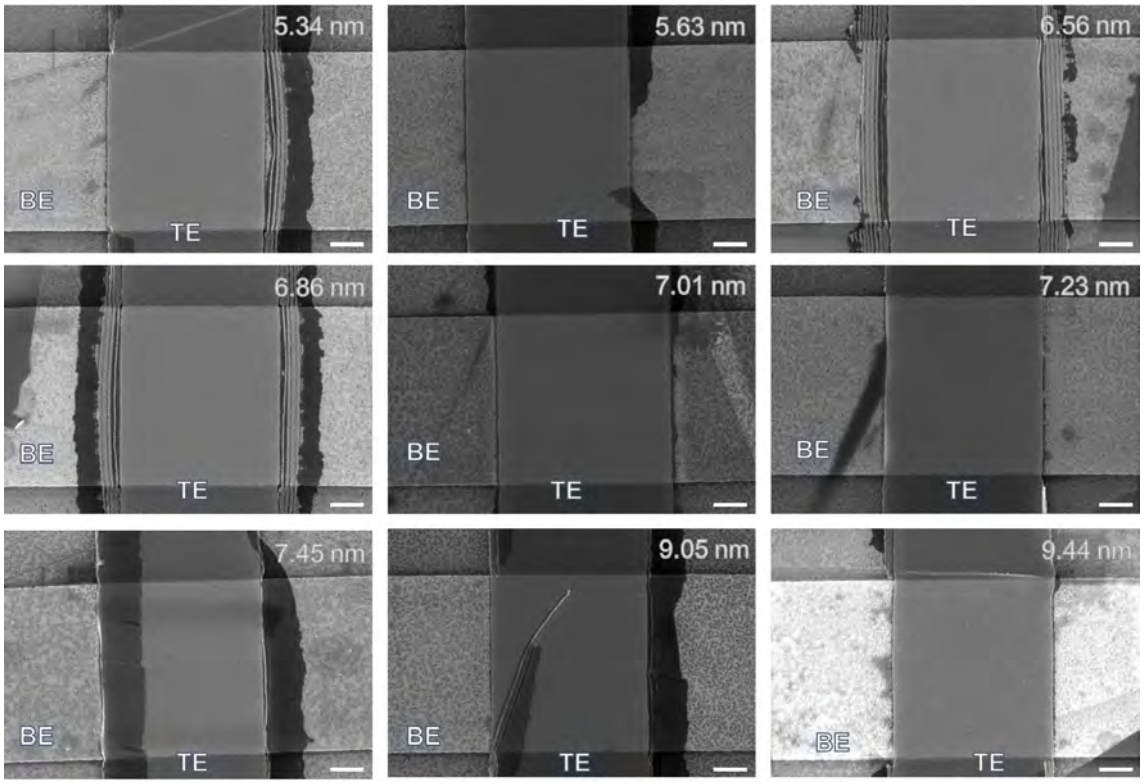

Figure 3.25 SEM images of 9 fresh Au/Ti/ME h-BN/Au devices. Scale bar is 1 μm.

For the Au/Ti/ME h-BN/Au devices, we shall employ the identical setup parameters for electrical characterization as those previously utilized for the Pt and Au devices. As previously delineated, a RVS ranging from 0 V to 30 V is imposed on the top electrode, with the bottom electrode being connected to ground.

The I-V curves for the nine Au/Ti/ME h-BN/Au devices are displayed in Figure 3.26a. Given that all Ti devices exhibited a melting trend during the testing procedure, the reverse I-V curves lack analytical value and may even obscure the clarity of the forward curves. For this reason, we have excluded the reverse I-V curves for the Ti devices and are presenting only the forward curves in Figure 3.26a. The thickness of the h-BN in each device is indicated in the legend. Employing the same electrical characterization settings as those used for Pt and Au devices, we have set the current limit to 10^{-2} A. However, the breakdown currents for all Au/Ti/ME h-BN/Au devices begin to diminish prior to reaching this current limit, akin to the behavior noted in the melted Au devices. It indicates that all Ti devices show a current overshoot before during the electric characterization.

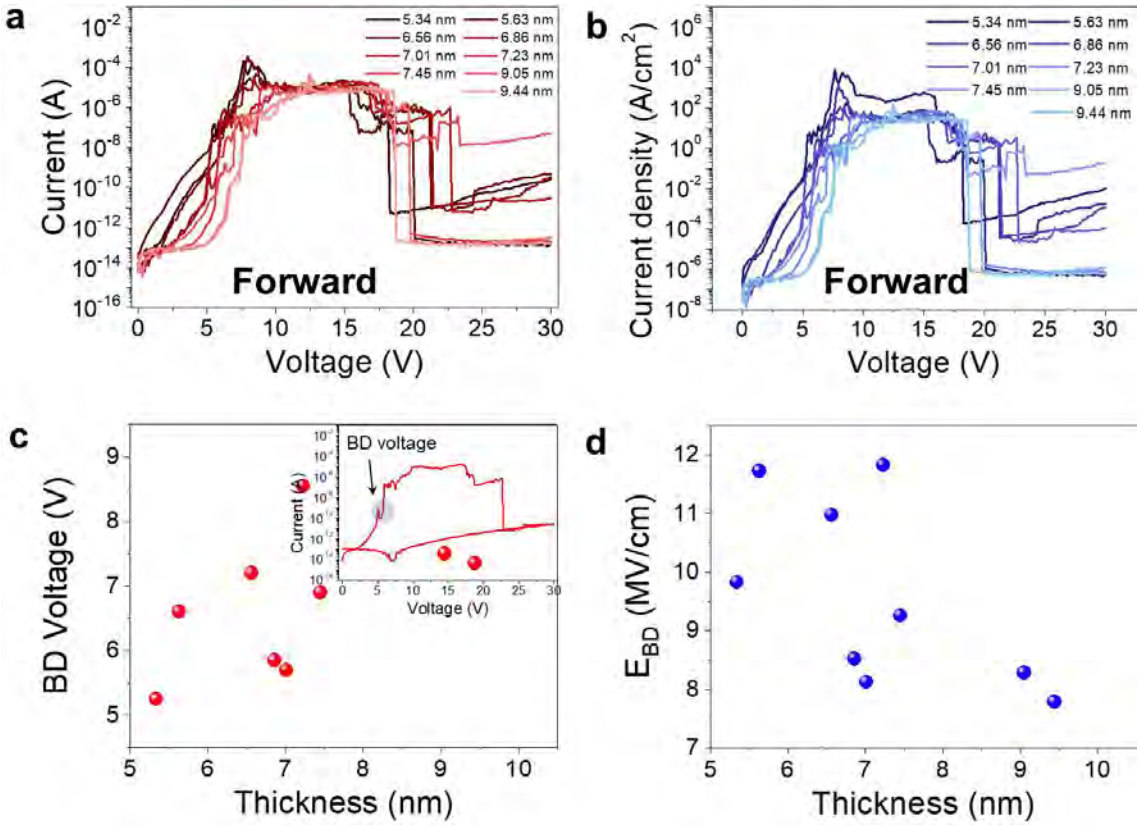

Figure 3.26 Data analysis of breakdown behavior in Au/Ti/ME h-BN/Au devices. (a) Forward part of I-V curves. (b) Current density based on the forward I-V curves. (c) BD voltage versus h-BN thickness. The inset plot indicates the BD voltage we take from the I-V curves. (d) E_{BD} versus h-BN thickness.

Figure 3.26b illustrates the current density, calculated based on the forward currents depicted in Figure 3.26a. The maximum current density in the majority of the Ti devices is approximately 10^2 A/cm^2, which is lower than the value observed for Pt and Au devices (10^3 A/cm^2). The breakdown voltage is derived from the I-V curves, as shown in the inset figure in Figure 3.26c. A plot of breakdown voltage versus h-BN thickness is presented in Figure 3.26c. The breakdown voltage does not exhibit a linear increase with h-BN thickness. After calculation, the dielectric breakdown strength is depicted in Figure 3.26d. The range of E_{BD} for h-BN in Ti devices is from 8 MV/cm to 12 MV/cm, with a median value of approximately 9 MV/cm. This dielectric breakdown value is lower than those recorded in Pt and Au devices.

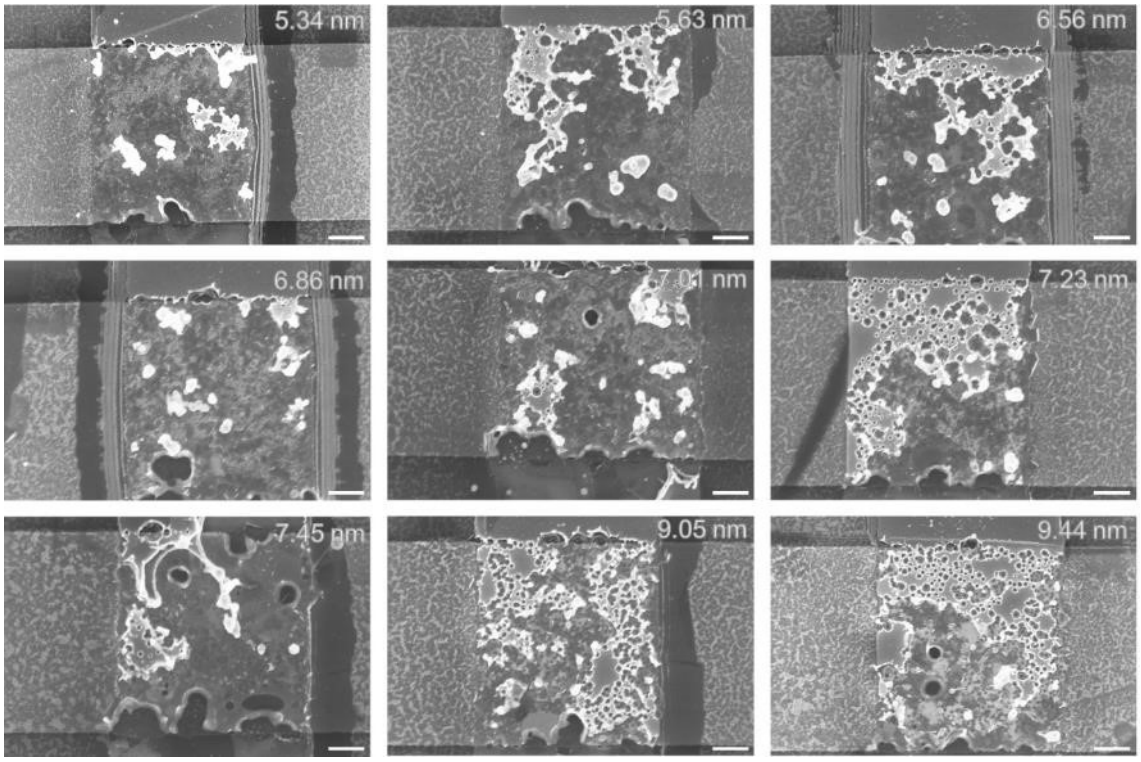

Figure 3.27 SEM images of 9 Au/Ti/ME h-BN/Au devices after electric characterization. Scale bar is 1 μm.

The damaged cross-point areas of the Au/Ti/ME h-BN/Au devices were examined using SEM, with the resulting images shown in Figure 3.27. Characterization of all nine Au/Ti/ME h-BN/Au devices via SEM reveals that the top electrodes have undergone melting. The mechanism of the melting is also current overshoot which has been discussed in Au device section. In contrast to the Au devices, the melting behavior observed in the Ti devices is characterized by uniformity. This uniform melting of the Au/Ti electrodes suggests that Ti is unable to endure the Joule heat generated during the BD process. The unsuitable nature of Ti as an electrode material in the study of the BD performance of ME h-BN is likely attributed to the high reactivity or diffusion properties of Ti, particularly when compared to Pt.

3.4. Conclusion

In this chapter, we employ ME h-BN flakes with thicknesses ranging from 4 nm to 10 nm to construct metal/ME h-BN/metal devices, each approximately 25 μm² in area (5 μm × 5 μm). The purpose of these devices is to investigate the dielectric breakdown induced by external bias on the top electrodes and to conduct subsequent analysis of the

electrical data and the condition of the devices post-electrical measurement. A variety of top electrode materials are utilized in this study, including inert metals such as Pt, Au, and an active metal like Ti. The fabrication of these devices is achieved through photolithography, electron beam evaporation, and a lift-off process at the micro-scale. Additionally, a transferred Au electrode serves as the top electrode in the fabrication of Au/ME h-BN/Au devices.

The principal findings of this study can be encapsulated as follows: i) The dielectric breakdown strength of h-BN, when utilizing Pt electrodes, is approximately 12 MV/cm, which exceeds that of devices employing Au and Ti electrodes. The dielectric breakdown strength of ME h-BN, as measured with different electrode materials, varies. ii) There is no significant difference in the dielectric breakdown performance between transferred Au and deposited Au as top electrodes in Au/h-BN/Au devices. iii) The electrodes melting behavior related to the current overshoot which induced by the shortage of the current limitation in measurement tool.

Chapter 4: Dielectric breakdown of CVD h-BN in nano-scale devices

4.1. Introduction

Dielectric breakdown refers to the phenomenon that occurs in dielectric materials when an external voltage is applied to the material. This behavior is characterized by the dielectric breakdown strength, which serves as an important metric for assessing the insulating properties of dielectric materials used in electronic devices.

Dielectric breakdown can be classified into two categories: hard breakdown and soft breakdown [222]. In the case of hard breakdown, the dielectric material is ruptured, resulting in the formation of a permanent conductive path within the material. In contrast, during soft breakdown, the conductive filament is reversible after appropriate operation. This mechanism of soft breakdown can be harnessed in the use of dielectric materials in memristors, which are regarded as the next generation of electronic devices with applications in memory storage, in-memory computing, artificial neural networks, and other fields.

Many studies have demonstrated memristors based on oxides in MIM structures. For example, Ta/TaOx/Pt memristors exhibit a high endurance of up to 10^{10} cycles [223], and Pt/Ta/TaOx/Pt/Ti memristors exhibit a high switching speed of 105 ps for set and 120 ps for reset [224]. Wang et al. reported a retention of up to 10 years in an $Al_2O_3/HfO_2/Al_2O_3$ memristor using an extrapolation method [225]. In addition, some other dielectric materials, such as organic materials [226], also exhibit their potential in applications as switching layers in memristors.

2D materials have numerous applications in memristors, as evidenced by the research of Xiong et al., who demonstrated that p-type doped mechanically exfoliated MoS_2 via H_2O_2 can be utilized in the TiN/O-MoS_2 planner memristor and the memristor exhibited bipolar RS behavior, making it a promising candidate for synapse and artificial neural network applications [227]. Furthermore, Hui et al. utilized Janus-graphene oxides as the RS medium to create Ag/Janus-graphene oxide/Au memristors, which displayed a low leakage current of 10^{-12} A and 1,200 cycles [228].

However, MoS_2 and graphene are not the initial candidates for memristor in 2D materials as they lack dielectric properties. Although they can potentially function as RS layers after optimization, as demonstrated in [227,228], h-BN emerges as a superior dielectric material in the 2D family, attracting considerable attention in memristor research. Chen et al. fabricated high-density Au/h-BN/Au memristors on a wafer scale, achieving a high yield of 98% and low variability in cycle (1.53%) and device (5.74%) levels. This work suggests that h-BN-based memristors hold potential for spiking neuromorphic hardware due to their stable relaxation process and multi-type threshold RS with ultra-low energy consumption [194]. Further investigation into the dielectric breakdown of h-BN could enhance understanding of its dielectric and electric performance and uncover additional applications for h-BN.

In the previous chapter, we explored the behavior of mechanically exfoliated h-BN under BD conditions. The remarkable insulating properties of mechanically exfoliated h-BN make it a promising material for electronic devices, particularly as encapsulation layer in the devices based on 2D materials.

However, once breakdown occurs in ME h-BN, the conductive path cannot recover, resulting in hard breakdown. This renders ME h-BN unsuitable as a resistive switching medium in memristors. Nevertheless, h-BN grown by CVD contains defects, mainly lattice distortions, that form during the growth process. As a result, CVD-grown h-BN is a more suitable material for use as a resistive switching layer in memristors due to its inherent defects and potential for mass production.

In this chapter, we will discuss the research conducted on memristors that utilize CVD-grown h-BN as an active layer. Monolayer/few layers and multilayer h-BN grown by CVD will be utilized in the study for performance comparison. The MIM device structure, a classic configuration, will be used to fabricate these memristors. We will explore the performance of various conductive electrodes in conjunction with the h-BN layer.

Our investigation will focus on nano-scale devices, and we will employ the EBL method to achieve this. The findings demonstrate that CVD-grown h-BN exhibits reversible RS behavior, and the crossbar structure helps to reduce device-to-device variability by minimizing the area of h-BN utilized.

4.2. Experiments

4.2.1. Fabrication of nano-scale devices based on CVD-grown h-BN

The fabrication of nano-scale devices involves the use of EBL, electron beam evaporation, lift-off, and wet transfer. In this process, the EBL technology, as described in Chapter 2, is utilized to image the device pattern onto the substrate with PMMA. process. Next, metal is deposited on the substrate after developing, and then lift-off is performed to obtain the bottom electrode. Subsequently, the CVD-grown h-BN is transferred to the bottom electrode using the wet transfer method, as described in Chapter 2. Afterward, the top electrode is constructed using EBL, electron beam evaporation, and lift-off. Ultimately, a MIM device based on two-dimensional h-BN is completed, with the two electrodes sandwiching the h-BN layer.

4.2.2. Characterization of CVD-grown h-BN after wet transfer

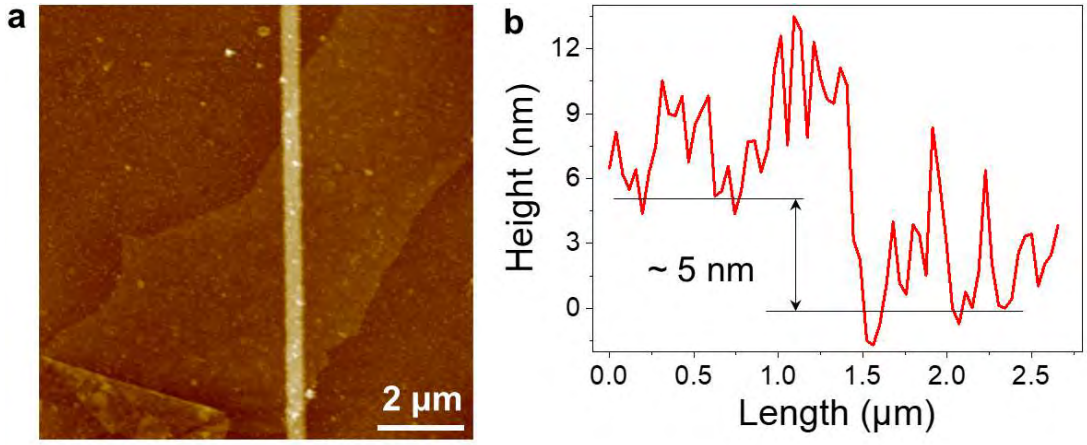

Figure 4.1 AFM characterization of the multilayer h-BN transferred on the substrate. (a) AFM topography map of the multilayer h-BN on the bottom electrode. (b) Thickness of the multilayer h-BN is around 5 nm.

The high-quality h-BN material used in this study was obtained from Graphene Supermarket, a company that synthesizes h-BN on Cu foil. The thickness and number of layers were verified using AFM, as shown in Figure 4.1b, which indicates that the transferred multilayer h-BN has a thickness of approximately 5 nm (equivalent to around 15 layers). The thickness of the multilayer h-BN was sufficient for the growth

process to include native defects, enabling easy observation of current through the layers. In Figure 4.1a, the transferred multilayer h-BN can be seen covering the bottom electrode, demonstrating a successful wet transfer. As the device is small, the h-BN covered area is sufficient for the fabrication of the top electrode.

4.3. Results and discussion

4.3.1. Topography characterization of Au/Ag/monolayer h-BN/Au

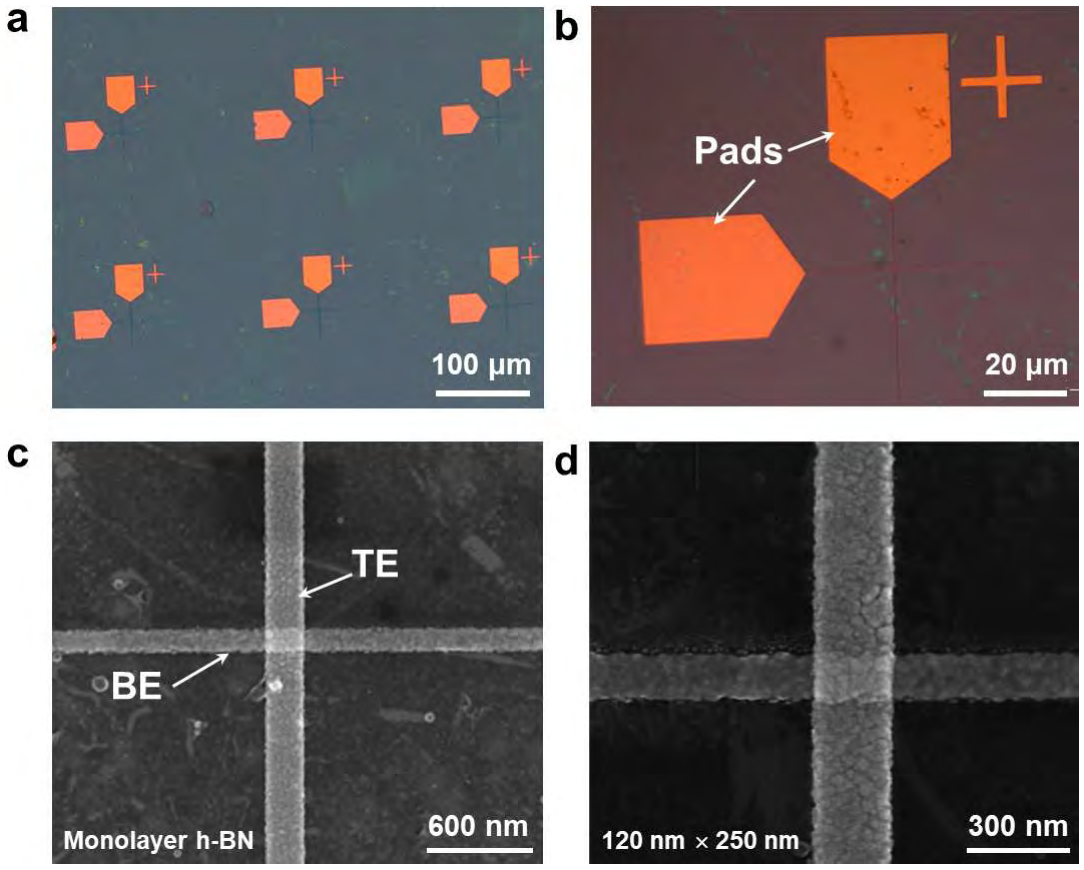

Figure 4.2 Topographic characterization of fabricated Au/Ag/monolayer h-BN/Au devices. (a) Portion of an array of the Au/Ag/monolayer h-BN/Au devices under an optical microscope. (b) Optical microscope image of a single device. (c) SEM image of the cross-point area. (d) Zoom-in SEM image and the practical size of the device.

Using monolayer h-BN, we fabricated memristors with Ag as the top electrode, and an external Au layer was added following the Ag layer to serve as the passivating function. We characterized the topography of the fabricated Au/Ag/monolayer h-BN/Au (in order from top to bottom) memristors using OM and SEM.

Figure 4.2a depicts a portion of an array of Au/Ag/monolayer h-BN/Au devices. Figure 4.2b illustrates an individual device from the array, showcasing its complete structure, including probe contact pads and real device electrodes. The presence of the monolayer h-BN is evident in the SEM view depicted in Figure 4.2c. The BE and TE are labeled in the image. The cross-point area measures approximately 120 nm by 250 nm, as illustrated in Figure 4.2d, making it a definitive nano-scale memristor. The size disparity between the top and bottom electrodes is attributed to the inconsistent conditions of the laboratory instrument. Nonetheless, from a topographical perspective, the fabrication of nano-scale devices was successful.

4.3.2. Electrical characterization of Au/Ag/monolayer h-BN/Au

To begin with, we conducted an electrical characterization of the Au (30 nm)/Ag (10 nm)/monolayer h-BN/Au (40 nm) devices, and the resulting I-V curves and related data analysis are presented in Figure 4.3. These devices are referred to as RS devices, as they can switch between a HRS and a LRS by applying an external bias. Furthermore, if the current returns to its original level (HRS) when the bias is removed, this type of RS is known as threshold RS, which is commonly observed in MIM devices when Ag serves as the electrode. The Au/Ag/monolayer h-BN/Au devices exhibit typical threshold RS behavior that is non-volatile.

The three plots in Figure 4.3a-c illustrate the typical threshold RS in Au/Ag/monolayer h-BN/Au devices. The initial current at HRS for all devices is approximately 10^{-14} A, which indicates the high uniformity of the CVD-grown h-BN utilized in these devices. The current at LRS is limited to 10^{-6} A due to the SPA tool used. These Au/Ag/monolayer h-BN/Au devices exhibit similar set voltages, which are less than 0.5 V. To assess the cycle-to-cycle variability of the device, we extracted the set voltages from Figure 4.3c as there are the most cycles (238 cycles) among the three I-V plots. The count versus set voltage plot is presented in Figure 4.3d. The set voltage is less than 0.5 V, and most of the values are around 0.25 V, indicating low variability in cycle-to-cycle. We then read the current in Figure 4.3c at 0.09 V in HRS and LRS, respectively, and plotted the obtained current data in Figure 4.3e. The on/off current ratio in this device is approximately 10^7, which is high and consistent with other reports [196, 229]. Figure 4.3f displays the HRS and LRS resistance calculated using the data in

Figure 4.3e. The high resistance (10^{13} Ω) indicates that the CVD-grown h-BN material still possesses excellent insulating properties despite some defects in the layer.

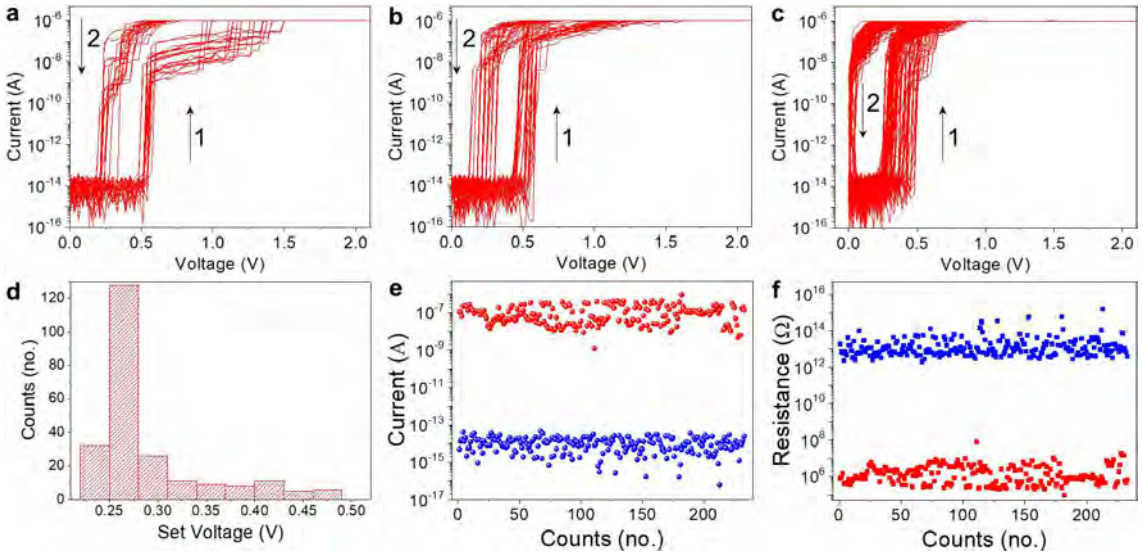

Figure 4.3 Electrical characterization of Au/Ag/Monolayer h-BN/Au memristors. (a)-(c), Three different devices present similar threshold switching behavior. (d) Set voltages of the I-V curves in the c plot. (e) The current read in c plot at 0.09 V in the set and reset process, respectively. (f) Resistance at HRS and LRS for the device in c.

Previous studies in literature [230] have suggested that the threshold resistive switching in h-BN occurs through the formation and rupture of conductive filaments caused by the migration of Ag ions. When a bias is applied to the device, an electric field is formed in the h-BN, leading to the migration of Ag ions towards the Au electrode side and the reduction of Ag atoms. The accumulation of Ag atoms on the Au side eventually establishes a conductive filament composed of Ag atoms that connects the top and bottom electrodes [230]. However, due to the active and mobile nature of Ag ions, the absence of a strong electric field can result in the movement of Ag ions to other locations, causing the breakage of conductive filaments in the h-BN.

4.3.3. Electrical characterization of Au/Ti/monolayer h-BN/Au

Besides utilizing the Ag electrode, we have also fabricated devices with Ti as the top electrode instead. The construction of these devices from top to bottom consists of Au (30 nm)/Ti (10 nm)/monolayer h-BN/Au (40 nm). The top Au layer serves as a protective layer since Ti is prone to oxidation in air. Figure 4.4a illustrates the proper

cross-point structure of the Au/Ti/monolayer h-BN/Au devices, which measure approximately 220 nm x 250 nm in size. While the device size may vary between different batches of samples, the discrepancy is acceptable for prototype research. Upon examining the SEM image, it becomes evident that the h-BN thickness is not uniform. Dark regions indicate the presence of thicker h-BN layers that formed during synthesis. Figure 4.4b displays the first I-V curves of five distinct Au/Ti/monolayer h-BN/Au devices, which are also referred to as forming curves. The Au/Ti/monolayer h-BN/Au devices exhibit distinct RS behavior relative to the threshold RS in Ag devices. These devices can switch from the HRS to the LRS at a positive bias around 3 V to 6 V and maintain the LRS for a considerable duration. Following the application of an opposing bias on the Ti devices, they switch from the LRS to the HRS. This reversible RS phenomenon is referred to as bipolar RS behavior. The process of switching from the HRS to the LRS is known as the set process, while the transition from the LRS to the HRS is referred to as the reset process.

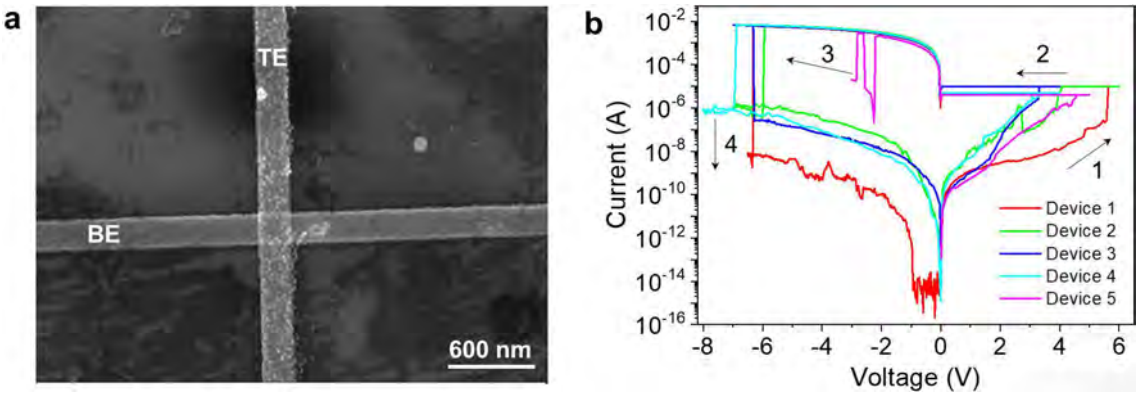

Figure 4.4 Characterization of Au/Ti/monolayer h-BN/Au devices. (a) SEM image of the fresh device. (b) Forming process of 5 Au/Ti/monolayer h-BN/Au devices.

Figure 4.4b demonstrates that all devices have reached their current limitation of 10-5 A, and the set voltage ranges from 3 V to 6 V. The set voltage in Ti devices is higher than that in Ag devices. We propose that Ti is less mobile in the h-BN than Ag. It is also worth mentioning that a similar set voltage is observed for the Ti/h-BN composition in [108].

The mechanism of the RS in Au/Ti/monolayer h-BN/Au has been discussed in [193]. According to the research, the migration of Ti ions through the grain boundaries

of h-BN, where there are more B vacancies, helps facilitate the migration or diffusion of Ti ions through the dielectric layer to form conductive filaments [193].

4.3.4. Au/Ag/multilayer h-BN/Au devices characterization

The fabrication of memristors with monolayer h-BN presents several challenges due to the difficulties in obtaining uniform properties and the presence of cracks caused by the wet transfer process. In contrast, multilayer h-BN has the ability to maintain better quality and stability during the device fabrication process. Additionally, the presence of native defects and a higher defect density in multilayer h-BN layers makes it more suitable for forming conductive channels in the perpendicular direction. For these reasons, we utilized multilayer h-BN to fabricate memristors using a MIM device structure.

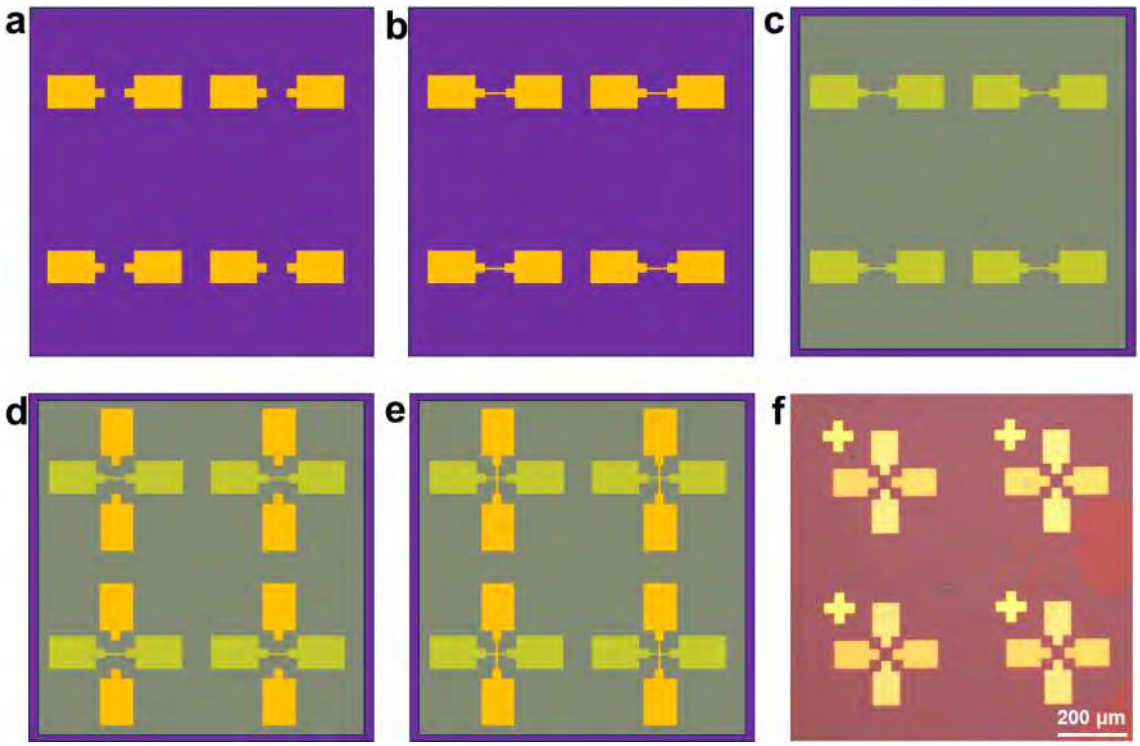

Figure 4.5 Fabrication process of metal/multilayer h-BN/metal devices. (a) Fabricate the testing pads with photolithography. (b) Fabricate the nano-scale electrode using EBL. (c) Transfer multilayer h-BN on the bottom electrode. (d) Fabricate the top testing pads using photolithography. (e) Fabricate nano-scale top electrodes with EBL. (f) Optical microscope image of fabricated Au/Ag/multilayer h-BN/Au devices.

The fabrication process of metal/multilayer h-BN/metal devices is depicted in Figure 4.5 and differs from the process used for monolayer h-BN memristors. The low efficiency of monolayer h-BN memristor fabrication is attributed to the prolonged time required by the EBL process to expose the entire electrode structure, including the large pads (several hundred μm^2) used for probe contact in electric measurement. To enhance the yield of multilayer h-BN devices, we incorporated photolithography and EBL into the fabrication process.

We first fabricated the large pads for probe station measurement using photolithography, electron beam evaporation, and lift-off. The pad size was 50 μm × 60 μm, which was easily achievable with the mask aligner (model MJB4 from SUSS Micro Tec) used in our process, and the size of the pad was sufficient for the conductive probes (radius 5 μm, model: 73CT-CMIA/50 from American Probe & Technologies) employed in the probe station.

We then used EBL to fabricate the nano-scale bottom electrode, as shown in Figure 4.5b. Now, we only use EBL to fabricate very small patterns; the time cost of EBL is reduced, and the efficiency improves. When the bottom electrode was completed, multilayer h-BN was transferred onto the bottom electrode using the standard wet transfer method (Figure 2.4) described in Chapter 2. We then repeated the electrode fabrication process for the top electrodes (Figure 4.5d and 4.5e). Finally, an optical image of the completed device is presented in Figure 4.5f. Although there are some cracks in h-BN after fabrication, the device area is still wholly covered by h-BN, indicating the successful fabrication of devices using the modified method. This method can save many sources of EBL and improve the efficiency of the device fabrication process, which is useful for prototype research.

Following the fabrication of Au/Ag/multilayer h-BN/Au devices, we conducted electrical characterization using a SPA connected with a probe station. Figure 4.6a presents a plot with over 400 threshold RS cycles, a significant increase compared to the Au/Ag/monolayer h-BN/Au devices. The set voltage range in the I-V curves, which ranges from 0.2 V to 0.4 V, is also very low. We measured the current at 0.2 V in both HRS and LRS, as shown in Figure 4.6b. The current on/off ratio is approximately 100, lower than that of monolayer h-BN-based memristors but still sufficient to distinguish between HRS and LRS states. The current versus counts plot in Figure 4.6b demonstrates acceptable cycle-to-cycle variability in this device. The resistance at HRS is approximately 10^5 Ω, which is lower than that of monolayer h-BN, indicating better

conductivity likely due to increased defects within the material. These defects may also contribute to the formation of conductive filaments and enhance the endurance of Au/Ag/multilayer h-BN/Au devices.

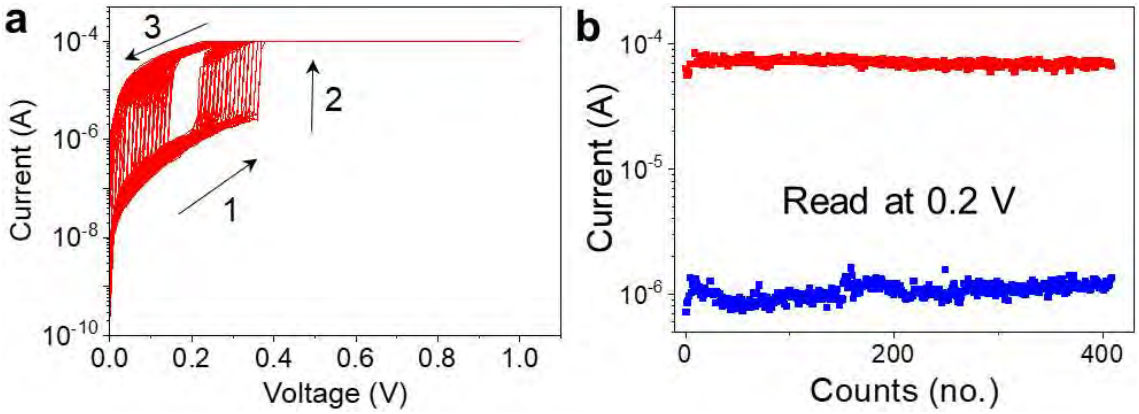

Figure 4.6 Electrical characterization of Au/Ag/multilayer h-BN/Au devices. (a) More than 400 threshold resistive switching cycles. (b) Current read at 0.2 V indicates an on/off ratio of 100 and a low cycle-to-cycle variability.

We conducted an analysis of the variability in Au/Ag/multilayer h-BN/Au devices. Figure 4.7 presents the I-V response of two different devices, revealing that all Au/Ag/h-BN/Au devices exhibit threshold RS behavior, regardless of the thickness of h-BN used in the devices (compare to monolayer h-BN devices).

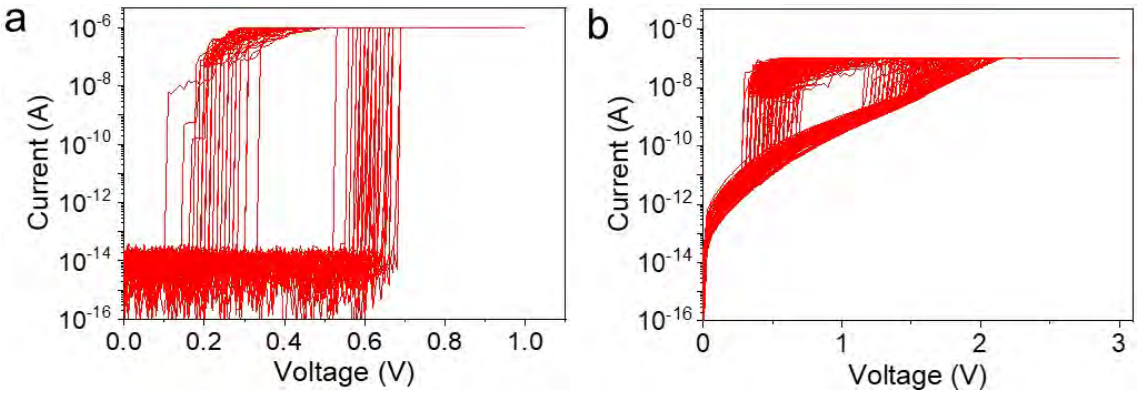

Figure 4.7 I-V curves of two Au/Ag/multilayer h-BN/Au devices.

In Figure 4.7a, the set voltage is significantly lower than in Figure 4.7b. Although both devices begin at 10^{-14} A, the left device demonstrates superior h-BN insulating properties, maintaining high resistance until breakdown. Conversely, the device on the right requires a higher applied bias of ~1.5 V to build conductive filaments.

Additionally, the current on/off ratios between the devices differ, with the left device exhibiting a high on/off ratio of up to 10^8, while the right device's on/off ratio is lower, at around 10^4. These results indicate that Au/Ag/multilayer h-BN/Au devices display device-to-device variability, and the quality of the h-BN can affect the device's performance, even when fabricated using the same parameters and process. It is worth noting that the uniform quality of CVD-grown h-BN remains challenging due to limitations in CVD synthesis technology for 2D materials.

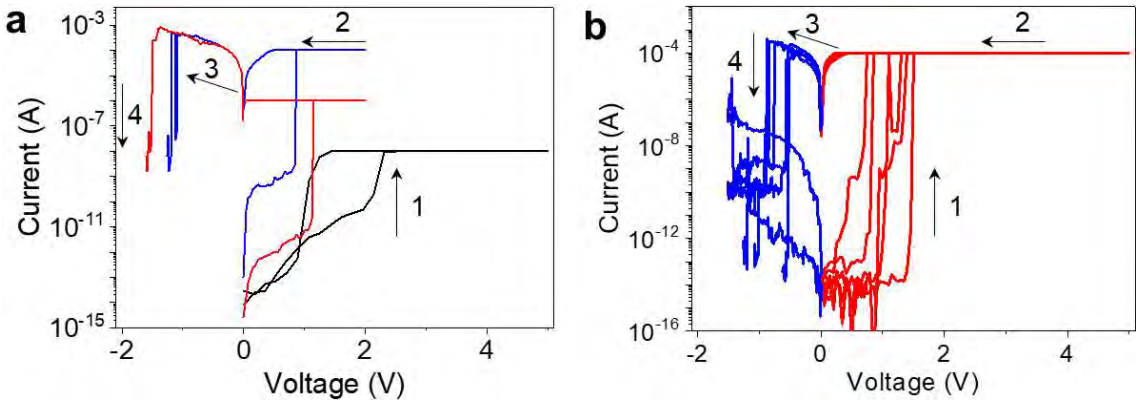

Figure 4.8 Unstable non-volatile resistive switching behavior in Au/Ag/multilayer h-BN/Au devices. (a) Memristor shows threshold RS at low current limitation while non-volatile RS at a higher current limitation. (b) Non-volatile RS in another Au/Ag/multilayer h-BN/Au memristor.

Most Ag/h-BN compositions display threshold-type resistive switching because the conductive filaments contain unstable Ag atoms. Nonetheless, Au/Ag/multilayer h-BN/Au devices have also been observed to exhibit non-volatile RS. In Figure 4.8, two examples of Au/Ag/multilayer h-BN/Au devices with non-volatile RS are illustrated. Figure 4.8a demonstrates that as the current limitation increases from 10^{-8} A to 10^{-6} A, the RS becomes non-volatile. The plots in Figure 4.8b indicate that a higher current limitation of 10^{-4} A in the Au/Ag/multilayer h-BN/Au devices can transform the RS from threshold to bipolar in this device. The reason might be the width of the conductive filament increased under high current limitation.

However, the conductive path is still not available to show a stable non-volatile RS. In Figure 4.9, the Au/Ag/multilayer h-BN/Au device shows a threshold and bipolar RS under the same current limitation of 10^{-5} A. The conductive filaments were not stale in the devices and ruptured quickly.

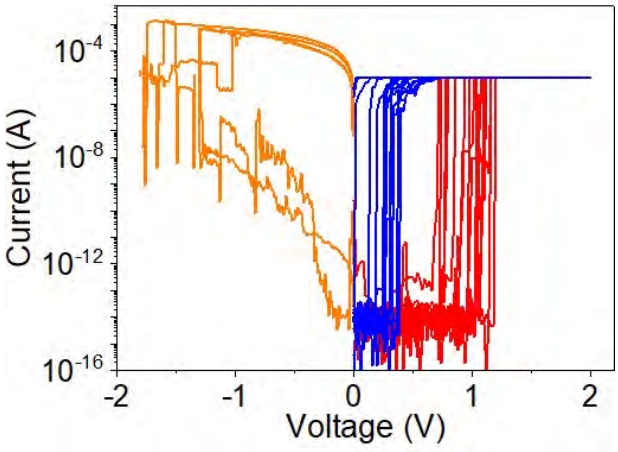

Figure 4.9 Threshold and bipolar coexistence under the same current limitation,

The current-time (I-t) test was conducted on Au/Ag/multilayer h-BN/Au device after it was switched to LRS. A constant voltage of 0.1 V was applied to the top electrode, and the resulting I-t plots are displayed in Figure 4.10. Initially, the current in LRS was approximately 10^{-6} A and decreased to 10^{-9} A in 250 s, which is a relatively short retention time for bipolar RS devices. Subsequently, a constant voltage of 0.1 V was reapplied to the top electrode, and the resulting data is shown in the right I-t plot. The current between the top and bottom electrodes continued to decrease until it reached the high-resistance state (HRS). The I-t plots indicate that the bipolar resistive switching in Au/Ag/multilayer h-BN/Au devices is not stable, and the conductive filaments will rupture within a short time.

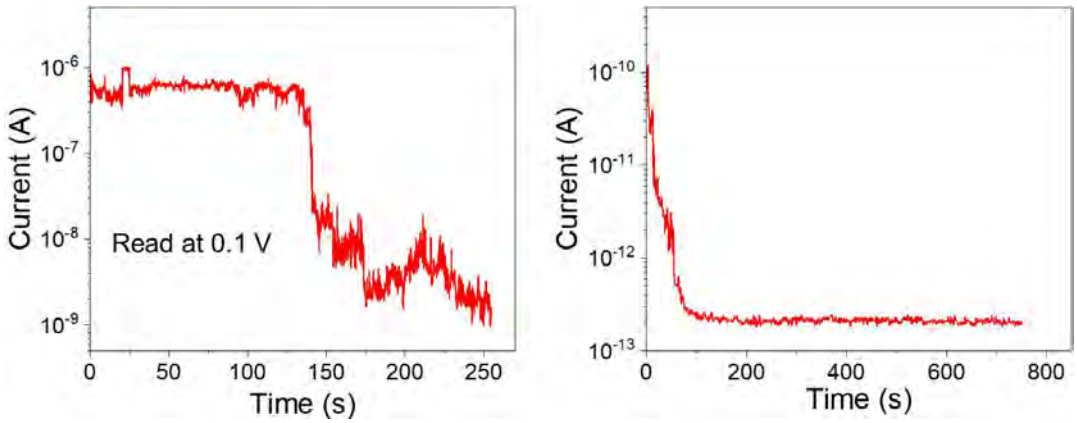

Figure 4.10 I-t plot for the Au/Ag/multilayer h-BN/Au devices showing bipolar RS.

Figure 4.11a and 4.11d presents the threshold RS curves obtained using positive and negative bias in the same Au/Ag/multilayer h-BN/Au device. These I-V cycles

exhibit similar set voltage and reset voltage regardless of the bias's polarity. In Figure 4.11b, the set voltage on the positive side is approximately 2 V, with a median value of 2.1 V. For the reset voltage in Figure 4.11c, the values range from 1 V to 1.5 V, with a median value of 1.4 V. The set and reset voltages extracted from I-V curves under negative bias are presented in Figure 4.11e and Figure 4.11f. The median value of the set voltage is -1.7 V, and the reset voltage is -1 V. Notably, the set and reset voltages in positive and negative threshold RS cycles are very close. The migration of Ag ions to the Au electrode side makes the RS in opposite electric field to be possible.

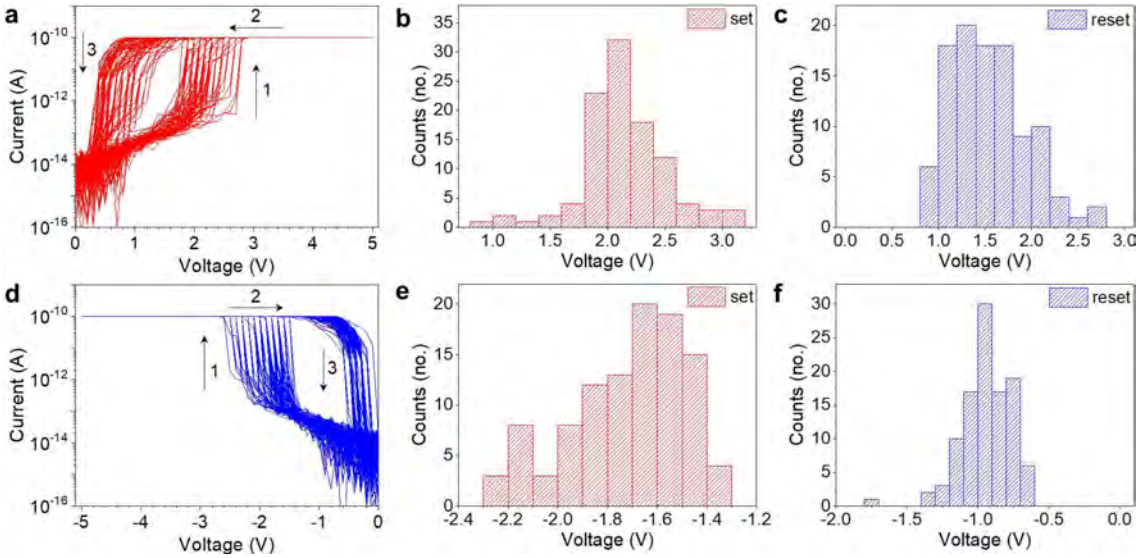

Figure 4.11 Threshold RS in Au/Ag/multilayer h-BN/Au devices under positive and negative bias. (a) I-V curves of threshold RS under positive bias. (b) Set voltage analysis of the I-V curves under positive bias. (c) Reset voltage distribution of the I-V curves under positive bias. (d) I-V curves under negative bias. (e) Set voltage distribution of I-V curves under negative bias. (f) Reset voltage distribution analysis of I-V curves under negative bias.

4.3.5. Crossbar array of Au/Ag/multilayer h-BN/Au devices

The Au/Ag/multilayer h-BN/Au devices display threshold RS with variability observed in different devices. We propose that the primary cause of this variability is the non-uniform quality of the multilayer h-BN used, despite consistent fabrication and characterization parameters. Discrepancies arise within areas of the same h-BN piece,

attributable to the limitations of current CVD growth technology, resulting in inhomogeneous h-BN quality.

To test this hypothesis, we have created a crossbar structure for the Au/Ag/multilayer h-BN/Au devices, simultaneously examining the potential for a high-density memristor array. In this crossbar arrangement, multiple memristors, arranged in a 10 × 10 grid, would utilize the same h-BN stack area, likely ensuring that the h-BN layers in these devices exhibit comparable performance characteristics. To minimize deviations caused by h-BN quality, the crossbar structure is designed at the nano-scale, and EBL is employed in the device fabrication process.

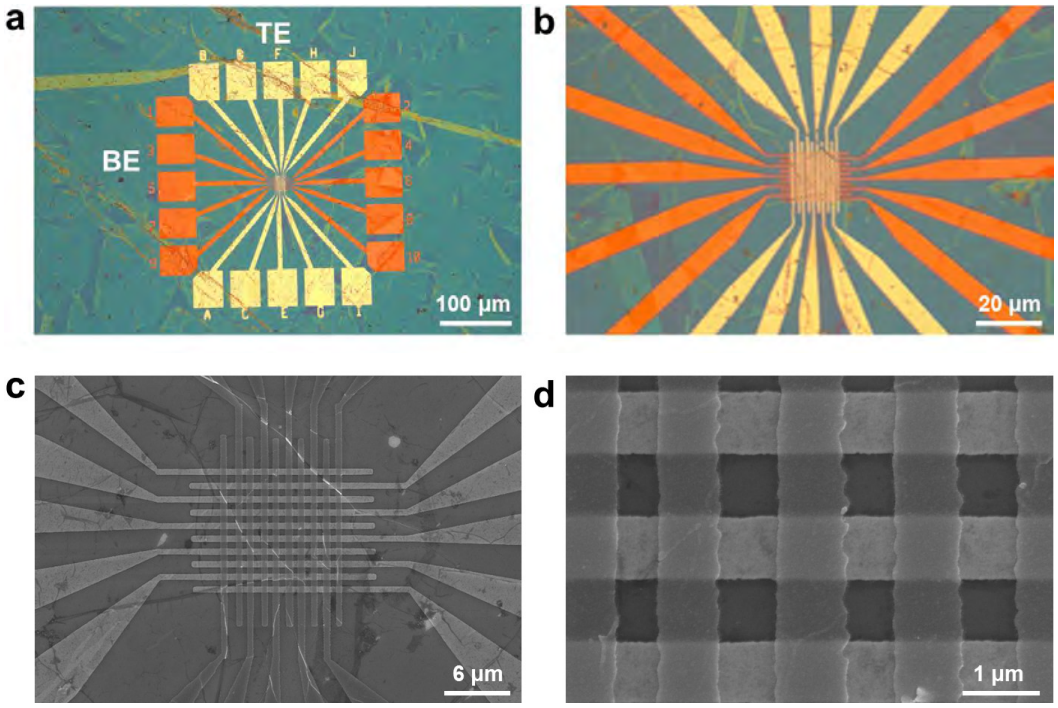

Figure 4.12 Topography map of the crossbar array of Au/Ag/multilayer h-BN/Au devices. (a) Optical microscope image of the crossbar array. (b) Zoom in the center area. (c) SEM image of the crossbar part and some wrinkles of h-BN is observed. (d) Dimensions of the top and bottom electrodes are both around 800 nm.

The topographical features of the Au/Ag/multilayer h-BN/Au devices integrated with a crossbar structure are depicted in Figure 4.12. The crossbar array is meticulously fabricated using a combination of techniques, including EBL, wet transfer, electron beam evaporation, and a lift-off process. Figure 4.12a presents an optical microscope image of the entire crossbar array, which is composed of a 10 by 10 grid, yielding a total of 100 Au/Ag/multilayer h-BN/Au devices available for characterization post-

fabrication. A 30 nm thick layer of Au is deposited over the Ag layer, serving as a protective shield against oxygen in the atmosphere. The orange-colored electrodes are the bottom ones, as the light absorption by the h-BN layer covering on bottom electrodes induces this color, while the yellow-colored electrodes are the top ones.

The magnified image of the central region, as depicted in Figure 4.12b, clearly demonstrates that the crossbar array is encased in a uniformly distributed h-BN layer, which is presumed to possess consistent thickness and quality. However, the SEM image featured in Figure 4.12c reveals the presence of several wrinkles across the crossbar array, potentially impacting device performance and augmenting device-to-device variability. The dimensions of the electrodes, as characterized in Figure 4.12d, measure approximately 800 nm × 800 nm.

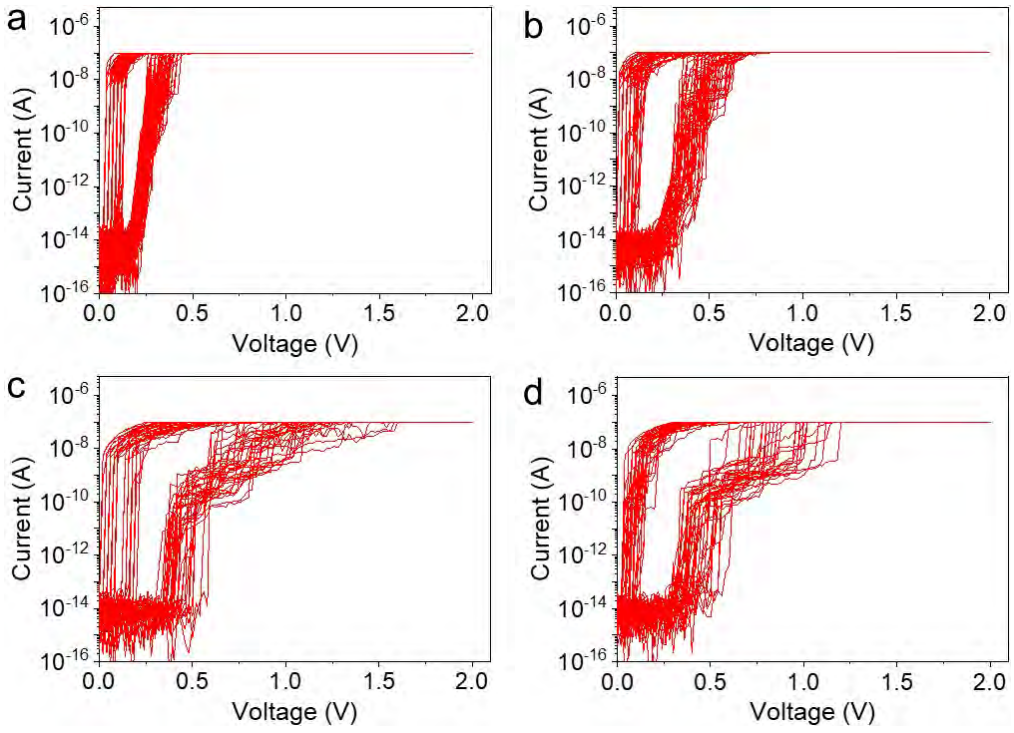

Figure 4.13 I-V curves of four Au/Ag/multilayer h-BN/Au devices from the same crossbar array.

Figure 4.13 presents the I-V curves for four devices from the same Au/Ag/multilayer h-BN/Au crossbar array. A consistent set of voltage and current limitations were applied during the I-V characterization of these devices. The data in Figure 4.13 reveals that the threshold RS performance among the four devices is generally consistent. However, a slight deviation is observed in the device depicted in

Figure 4.13a, which has a lower set voltage of approximately 0.2 V compared to the other devices, which show a set voltage of around 0.5 V. Despite this deviation, it is considered acceptable.

The crossbar array devices exhibit a substantially greater degree of homogeneity in threshold RS performance when compared to the cross-point structure devices. This superior performance can be attributed to the utilization of a uniform h-BN stack at the core of the crossbar array. The operational area within the crossbar array measures approximately 11 μm by 11 μm at the crossbar center, which is a relatively small area where the quality of the multilayer h-BN stack may be more consistently maintained.

In contrast, the cross-point array in Figure 4.5f demonstrates a substantial span of up to 500 μm between devices. Due to this extended distance, variability in the h-BN stack quality may arise, leading to noticeable device-to-device variability. Given the limitations in synthesis technology, achieving precise uniformity in h-BN through CVD is challenging. Therefore, it is understandable that the crossbar array devices do not exhibit completely consistent performance.

The existence of wrinkles in a 11 μm by 11 μm area may have an impact on device performance and contribute to differences between devices. In the future, advancements in the quality and uniformity of h-BN or decreases in device dimensions may lead to a reduction in device-to-device variability.

4.3.6. Au/Ti/multilayer h-BN/Au devices

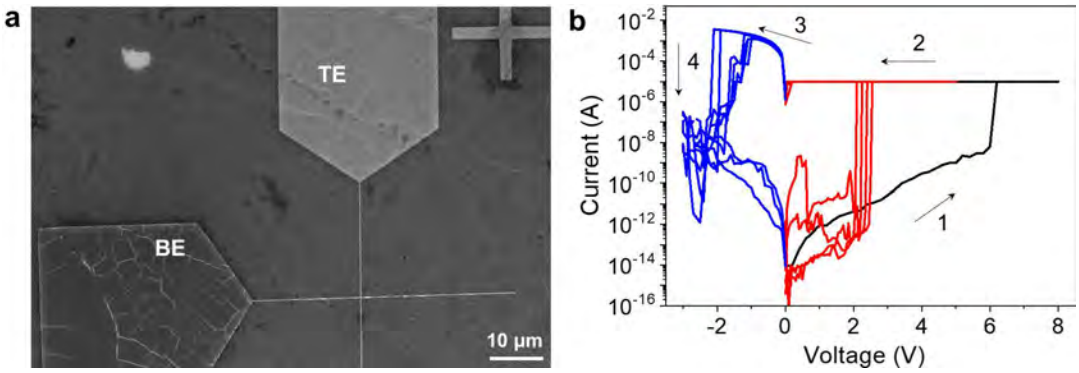

Figure 4.14 Topography and electric characterization of Au/Ti/h-BN/Au device. (a) SEM image of a Au/Ti/h-BN/Au device. (b) I-V curves show a typical bipolar resistive switching behavior.

Ti is commonly utilized as an electrode material in memristors that incorporate h-BN [172]. In our study, we employed Ti as the top electrode with an additional protective layer of Au in cross-point structure devices and observed non-volatile RS behavior within the Au/Ti/multilayer h-BN/Au devices. The structure of the device consists of layers, from top to bottom, of Au (30 nm)/Ti (10 nm)/multilayer h-BN/Au (40 nm). The topographical representation of the device is illustrated in Figure 4.14a, where the BE and TE intersect to form the cross-point area where RS occurs.

The high-quality surface coverage of the h-BN is evident in the presence of distinct h-BN wrinkles. The I-V characteristics, presented in Figure 4.14b, show a characteristic bipolar resistive switching behavior. An initial forming process is observed in the I-V curves, which is also evident in the Ti/monolayer h-BN/Au devices (refer to Figure 4.4b). After the forming curve, subsequent I-V cycles exhibit minimal cycle-to-cycle variability. The set voltage is maintained at 2.5 V, while the reset voltage fluctuates between -1 V and -2 V. However, the device does not demonstrate an impressive endurance.

4.3.7. Au/multilayer h-BN/Au devices

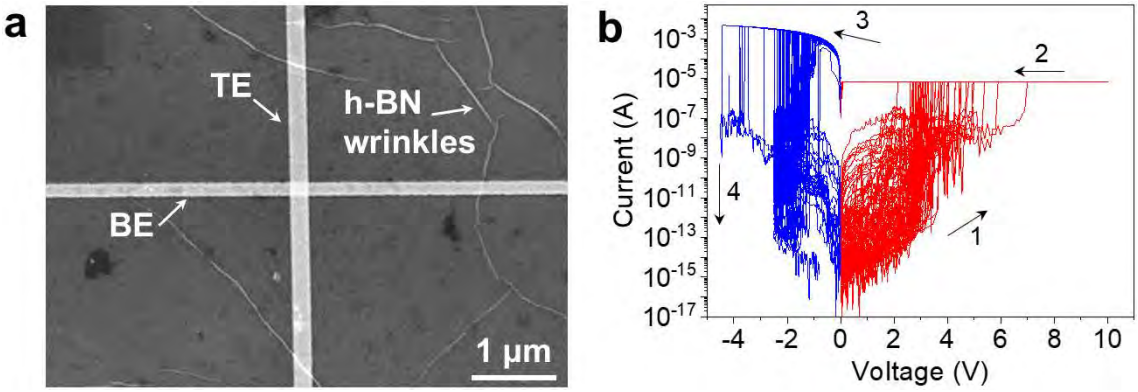

Figure 4.15 Au/h-BN/Au device. (a) SEM image of the cross-point area. (b) Au/h-BN/Au device shows non-volatile resistive switching.

Au enjoys a reputation for its exceptional conductivity and chemical stability, features that enable it to resist oxidation more effectively than many other metals. As a result, Au is frequently utilized in electrical devices as electrodes or conductive pathways. We have previously mentioned that Au is also employed in devices that incorporate Ag and Ti, serving as both the bottom electrodes and a protective layer. In

order to further investigate their electrical properties, we have fabricated Au (40 nm)/multilayer hexagonal boron nitride (h-BN)/Au (40 nm) devices and evaluated their performance as memristors.

The fabrication process for the devices under consideration follows the same procedure as that for Au/Ag/multilayer h-BN/Au devices. Figure 4.15a displays a SEM image of the cross-point structure, which reveals the layered nature of the h-BN stack through the presence of visible wrinkles. The memristor dimensions are 160 nm (BE) by 230 nm (TE). Unlike devices incorporating Ag, the Au/multilayer h-BN/Au device demonstrates classic bipolar RS behavior. The set voltage for these devices falls within the range of 2 V to 7 V, while the reset voltage varies between -1 V and -4 V. As compared to memristors that incorporate Ag and Ti, the Au/multilayer h-BN/Au device exhibits slightly greater cycle-to-cycle variability.

Au/h-BN/Au memristors have been the subject of several studies [144, 231], where the bipolar RS phenomenon has also been reported. The conductive filament formation in the Au/h-BN/Au memristor is attributed to the metal's migration from the electrodes and the creation of boron vacancies [231].

4.4. Conclusion

In this chapter, we fabricate both monolayer and multilayer CVD-grown h-BN-based memristors at nano-scale, and the RS performance using different top electrodes (Ag, Ti, Au) are analyzed. The cross-point structure is used in the h-BN memristors with Ag, Ti and Au top electrodes, and the crossbar device structure is used for Au/Ag/multilayer h-BN/Au devices. We obtained some conclusions: i) Memristors based on h-BN with the sizes of 120 nm × 250 nm in cross-point and 800 nm × 800 nm in crossbar structure are achieved by EBL. ii) The RS behavior type in the h-BN-based memristors depends on the top electrode metal used in the device. Memristors with Ag electrode show threshold RS in both monolayer and multilayer h-BN devices. However, the memristors using Ti and Au show non-volatile RS behavior. Our work provides useful information about RS in memristors based on CVD-grown h-BN and offers a feasible optimization method to modify the variability in device-to-device.

Chapter 5: Limited breakdown in one-transistor-one-memristor cell

5.1. Introduction

2D materials are considered promising candidates for the fabrication of all kinds of electronic devices and circuits, owing to their superior physical, chemical, electrical, mechanical, and thermal properties. Among the 2D materials family, h-BN is especially important because it has one of the widest bandgaps known (5.9 eV) [120], and hence it is one of the few 2D materials that can be used as dielectric in different devices. Mechanically exfoliated h-BN holds a very low number of local atomic defects [144]; when exposed to an electrical field, this can minimize the leakage current and maximize the capacitance effect, enabling its use as dielectric in transistors [232,233] and capacitors [234]. However, when fabricating real devices at the wafer level, h-BN (and most other 2D materials) contain a much higher number of local defects because i) the synthesis methods, such as CVD, result in lattice distortions, especially in multilayers [197] – note that in electronic devices h-BN is usually multilayer, as the thickness of a monolayer is 0.33 nm and that is not enough to block tunnelling current [235]. And ii) the evaporation of metal on the h-BN stack produces defects by metallic ions penetration in the uppermost layers [236]. For these reasons, and due to its low dielectric constant (~3), it is believed that h-BN is not a good gate dielectric for transistors.

CVD-grown h-BN can be also used to fabricate memristors, exhibiting non-volatile bipolar RS [108, 139], and/or volatile unipolar RS [230] – often referred to as threshold-type RS. The observation of one RS regime or another depends on the shape of the conductive filament formed across the h-BN stack when voltage is applied, which can be controlled using different types of electrode materials and/or current limitations [237] – this is necessary to control the energy delivered during the dielectric breakdown of the h-BN stack, which reduces the width of the conductive filament and enables it to be reset. In most exploratory studies the current limitation is applied using a semiconductor

parameter analyzer. However, in real circuits, such a setup is not available, and this is typically done using a transistor connected in series to the memristor.

Very few studies have successfully fabricated 1T1M cells using 2D materials [238, 240-242], but none of them measured threshold-type RS. Moreover, the size of the devices was normally very large (>10 μm^2), and the amount of data presented was scarce. In this article, we present the first all-2D materials-based 1T1M cells exhibiting threshold-type RS. We use transistors with a 4 μm^2 MoS_2 channel as the current limitation element and 0.3 μm^2 h-BN memristors that exhibit reliable threshold-type RS over thousands of cycles. This behavior is consistently observed in multiple devices, although there is an inherent device-to-device variability, which we also quantify—something never done before for 1T1M cells.

5.2. Transistor and memristor candidate for 1T1M cell

Prior to initiating the 1T1M project, it is imperative to carefully consider the appropriate transistor and memristor components. In Chapters 3 and 4, we conducted a study on memristors based on mechanically exfoliated h-BN and those grown via CVD. Our findings indicate that the CVD-grown h-BN-based memristors exhibit reversible RS, making them a prospective and promising candidate for the RS layer in memristor fabrication.

Regarding transistors, we have selected mechanically exfoliated MoS_2 as the channel material. Extensive research has been conducted on transistors utilizing mechanically exfoliated MoS_2 [243-245], and the efficacy of MoS_2 as a transistor channel has been well-established.

5.2.1. Fabrication of MoS_2 transistor

We chose ME MoS_2 as the channel material for constructing transistors in order to assess its electrical performance. The MoS_2 crystals were sourced from the Moly Hill mine in Quebec, Canada, and were obtained through the mechanical exfoliation method discussed in Chapter 2.

To begin, we utilized a confocal Raman imaging system (with a wavelength of 532nm and model Alpha300R from Wi Tec) to examine the exfoliated MoS_2 flake on the substrate. The Raman spectrum, depicted in Figure 5.1, shows peaks that align well with previously reported MoS_2 Raman profiles [246], thereby verifying the authenticity of the acquired MoS_2 flakes. However, the data alone is insufficient to determine the layer count within the MoS_2 flake. Therefore, we will proceed to use an AFM to accurately measure the thickness of the MoS_2 at a later step.

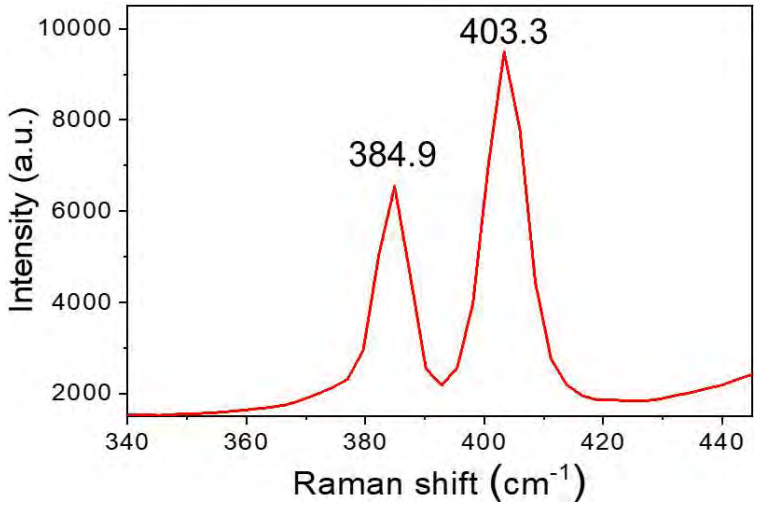

Figure 5.1 Raman data of the exfoliated MoS_2 flake on substrate.

We fabricate MoS_2 transistors using a conventional configuration, in which the source and drain contacts are placed on top of the MoS_2 flake. To tackle the alignment difficulties encountered during the photolithography process, we use the Au electrode transfer technique outlined in Figure 3.18 to accurately position the source and drain on the surface of the ME MoS_2. A visual representation of the device, along with a schematic illustration of its structure, is shown in Figure 5.2. The transistor channel measures approximately 4 μm in length and has variable width due to the non-uniform geometry of the ME MoS_2 flake.

Detailed structural specifications of the transistor are depicted in Figure 5.2b. For the back-gate transistor, a 300 nm thick SiO_2 layer serves as the gate dielectric, and a 40 nm thick Au film, which acts as the source and drain electrodes, is transferred onto the MoS_2 flake.

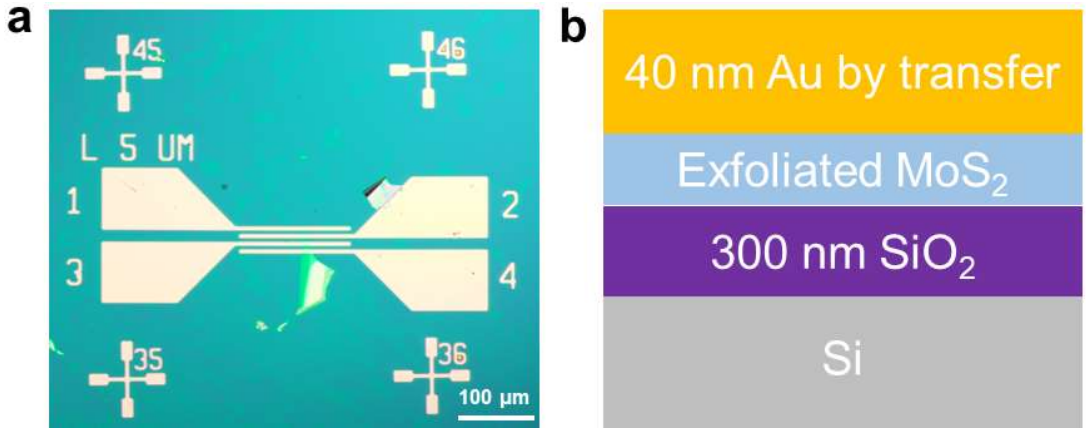

Figure 5.2 MoS_2 transistor fabricated using transferred Au as source and drain. (a) Optical microscope image of a MoS_2 transistor. (b) Structure illustration of the MoS_2-based back-gate transistor.

Additionally, we utilize EBL to fabricate conventional back-gate transistors. The complete structure and optical images are displayed in Figure 5.3. The image on the left illustrates the transistor's top view, while the image on the right provides a magnified optical microscope image of the fabricated transistor. Following the transfer of the ME MoS_2 onto a pre-marked SiO_2/Si wafer, EBL overlay patterning is employed to delineate the source and drain patterns onto the ME MoS_2. Subsequently, a 40 nm layer of Au is deposited, which is then lifted off to finalize the transistor fabrication process. The larger pads are designated for probe contact areas.

In Figure 5.3b, the metal pad on the left serves as a reference mark for the overlay patterning. Given the sufficient length of the MoS_2 flake in Figure 5.3b, we have fabricated two transistors using the identical MoS_2 flake.

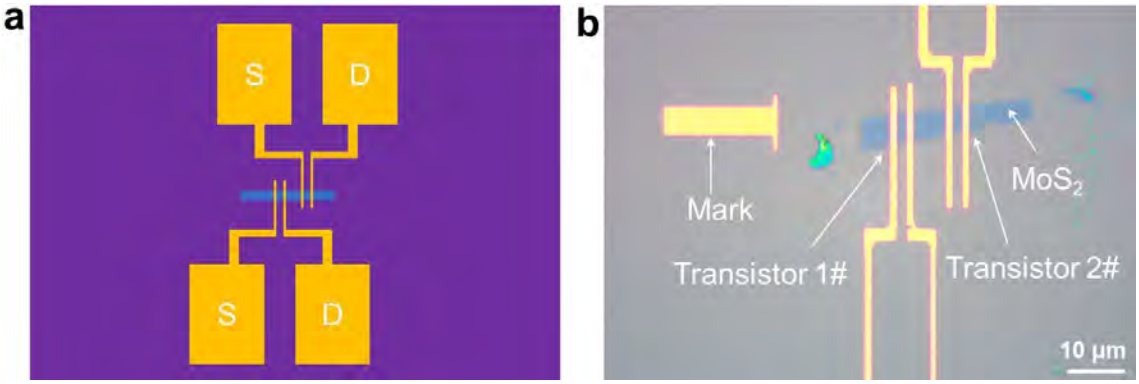

Figure 5.3 Back-gate transistor based on ME MoS_2. (a) Top view of the MoS_2 transistor. (b) Optical microscope image of part of the transistors.

5.2.2. Materials and devices characterization

The characterization of mechanically exfoliated MoS_2 flakes is initiated with an OM (model LV100N POL from Nikon). The source/drain and mark are created using either photolithography (model MJB4 from SUSS) or EBL (pattern system from Raith combined with Quantan 200 FEG from FEI), electron beam evaporation (model PVD 75 from Kurt J. Lesker), and lift-off. The quality of these electrodes is assessed through OM. Following the completion of MoS_2 transfer, the MoS_2 flakes on the substrate are analyzed with an AFM (model Multimode V from Bruker) in tapping mode, utilizing tips (NCH) from Nano World.

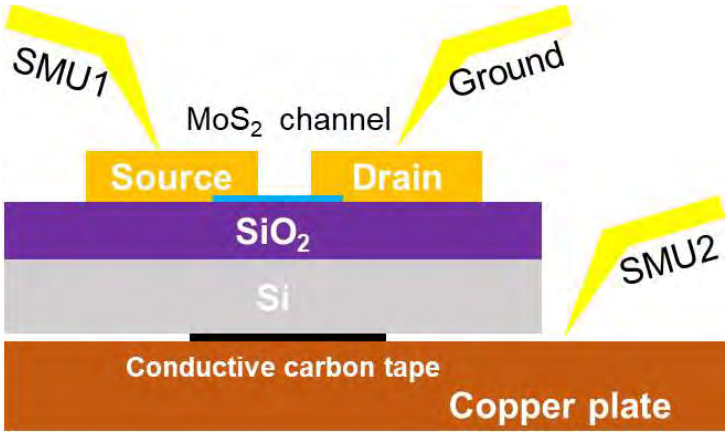

Figure 5.4 Illustration of transistor electrical characterization.

The back-gate transistor is a three-terminal device that necessitates gate bias in the electrical characterization process. In our devices, we employ n-doped Si (0.002-0.004 Ω.cm) as a back-gate to apply the gate bias during testing. To apply the bias on the Si, we affix the transistor to a polished Cu plate using conductive carbon tape (from NEM), which has a good conductivity (< 5 Ω/mm^2).

Then, the probes of the probe station (M150 from Cascade) connected to a semiconductor parameter analyzer (model 4200 from Keithley) are placed on the transistor, as illustrated in Figure 5.4. The source-measure unit (SMU) 1 connects the source, and SMU2 connects the bottom Cu plate. The ground (GND) probe is placed on the drain to form a conductive channel with SMU1. The bias can be applied to the transistor via SMU1 and SMU2.

5.2.3. Characterization of the transistor with transferred source/drain

We successfully fabricated the transistor using the Au transfer method, which eliminates the need for complex alignment processes in photolithography. The ME MoS_2 flake was characterized using AFM, with the topography map presented in Figure 5.5a and the thickness of the MoS_2 flake measuring approximately 5.29 nm, as shown in Figure 5.5b. Following the inspection of the MoS_2 flake, the Au pattern was transferred onto it to form the transistor channel, as depicted in Figure 5.5c, with a channel length of 4 μm.

After successfully fabricating the transistor, we conducted an analysis of its output performance. The output results are displayed in Figure 5.5d, which shows that the source-drain voltage (V_{ds}) varies from 0 V to 1 V while the gate voltage (V_g) is incremented from 0 V to 10 V in steps of 2 V, maintaining a constant value throughout. The I-V curves exhibit a desirable current saturation in the output characteristics. In addition, the current within the MoS_2 plane can be modulated by adjusting the V_g.

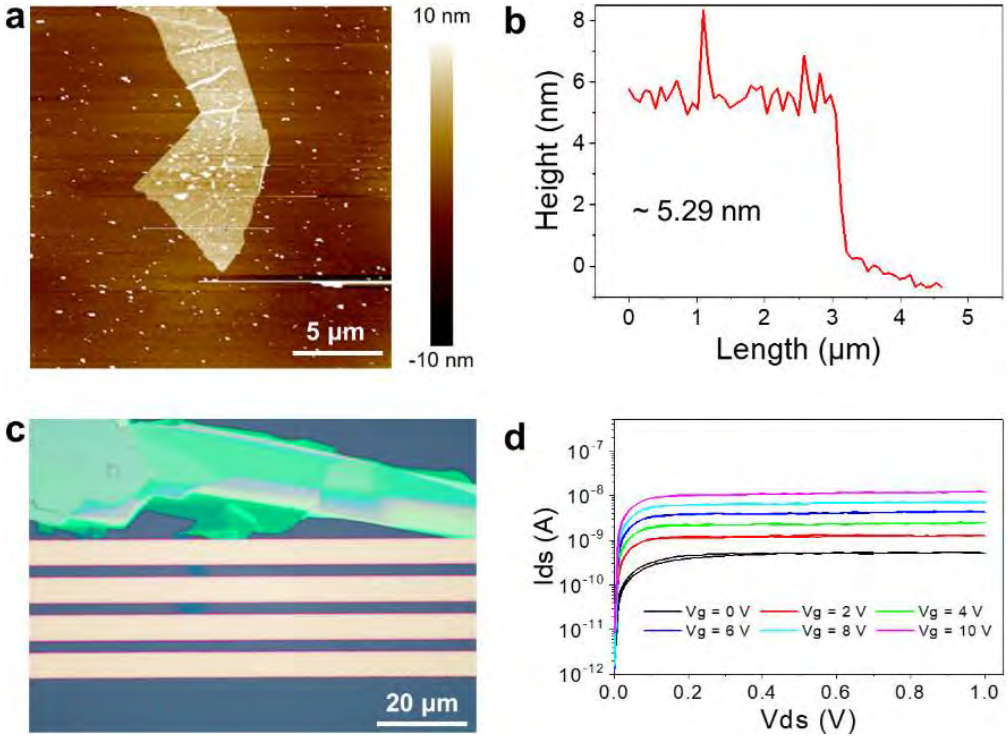

Figure 5.5 Topography map of the transistor with transferred source/drain and its electrical performance. (a) AFM topography map of ME MoS_2 on a substrate. (b) ME MoS_2 thickness. (c) Optical microscope image of the transistor. (d) Output plot of the transistor based on ME MoS_2.

We have fabricated an array of devices featuring MoS_2 flakes of varying thicknesses, and the output plots for four such devices are displayed in Figure 5.6. For a direct comparison, the output curves are presented using a consistent scale for both V_{ds} and the source-drain current (I_{ds}). The V_g is increased from 0 V to 10 V with steps of 2 V. The trend of current change in response to V_g is consistent across all transistors. However, there is a noticeable variation in the current levels, which suggests device-to-device variability. This variation is deemed acceptable when considering the disparate channel widths and the range of thicknesses present in the ME MoS_2 employed in the fabrication of these four transistors.

The use of MoS_2 transistors with transferred source/drain has revealed a low output current, which can likely be attributed to the contact resistance between the channel and source/drain. Furthermore, the structural design of these transistors presents challenges when attempting to integrate them into 1T1M cells.

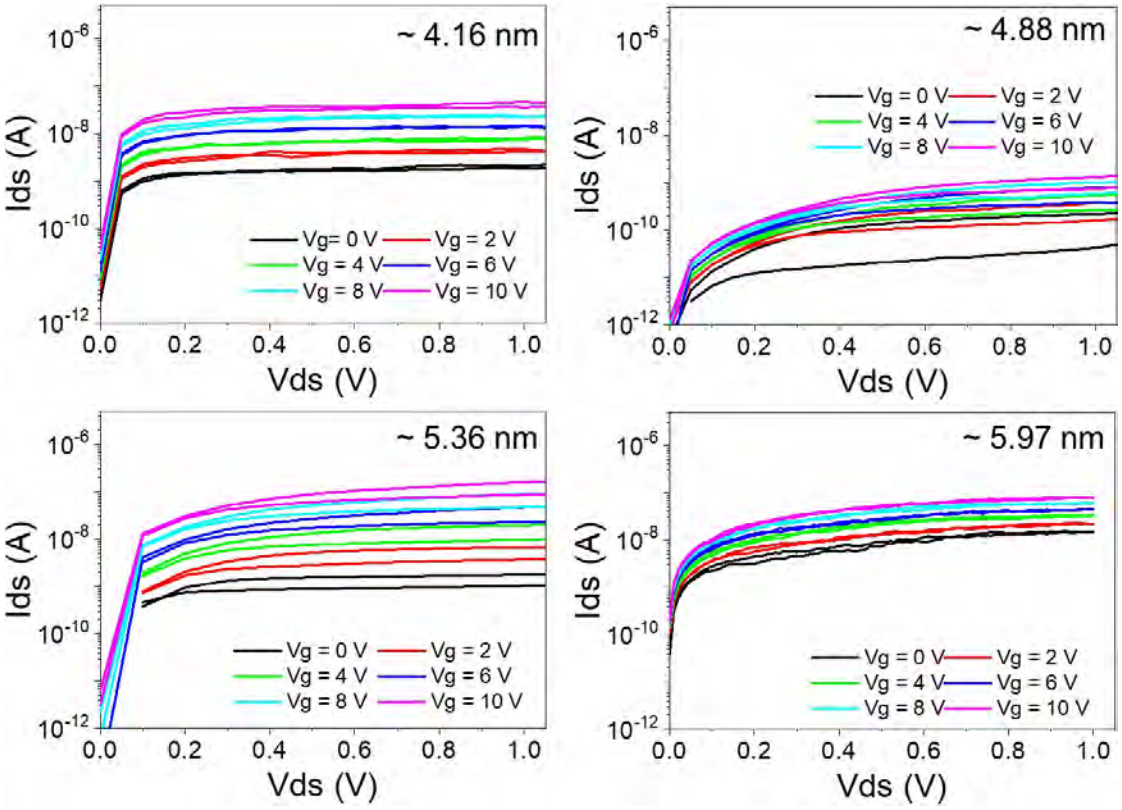

Figure 5.6 Output curves of 4 MoS_2 transistors using transferred source/drain. The channel length of all transistors is 4 μm. The top-right corner is the thickness of the ME MoS_2 used in each transistor.

5.2.4. Transistors fabricated using EBL method

To enhance the performance of MoS_2 transistors, we employed the EBL method for the creation of the source and drain electrodes. The fabrication process encompasses the following steps:

i) Exfoliating MoS_2 flakes from the bulk MoS_2 crystal.

ii) Transferring the MoS_2 flakes onto a 300 nm SiO_2/Si substrate using a dry transfer method.

iii) Characterizing the MoS_2 flakes with AFM to verify their thickness and quality.

iv) Utilizing EBL to image the source and drain patterns onto the MoS_2 flake, where the channel length and width are ascertained.

v) Depositing metal via electron beam evaporation to form the source and drain electrodes.

vi) Executing a lift-off process to eliminate any unwanted metal.

These meticulous steps ensure the precise construction of the MoS_2 transistors, optimizing their performance and reliability.

The channel topography of the transistors is ultimately displayed in Figure 5.7, showcasing three MoS_2 transistors along with their output curves. In the sequence from Figure 5.7a to Figure 5.7c, the topography maps of the transistor channels are presented, with the channel lengths and widths indicated in the bottom-left corner of each map. The channel lengths are uniformly approximately 2 μm, while the widths vary slightly, ranging from 1.2 μm to 2.3 μm, reflecting the inherent difficulty in controlling the size of the mechanically exfoliated MoS_2 flakes. The corresponding output curves are displayed adjacent to the SEM images on the right (Figures 5.7d to 5.7f).

Upon comparison of Figures 5.7d to 5.7f, it is observed that all transistors exhibit analogous I-V curves, signifying a consistent property of MoS_2 as a transistor channel material. Regardless of the varying channel widths and MoS_2 flake thicknesses, the output performance of these transistors remains highly comparable under the applied Vg, which ranges from -20 V to 40 V. This consistency suggests that the variability between devices is within acceptable limits.

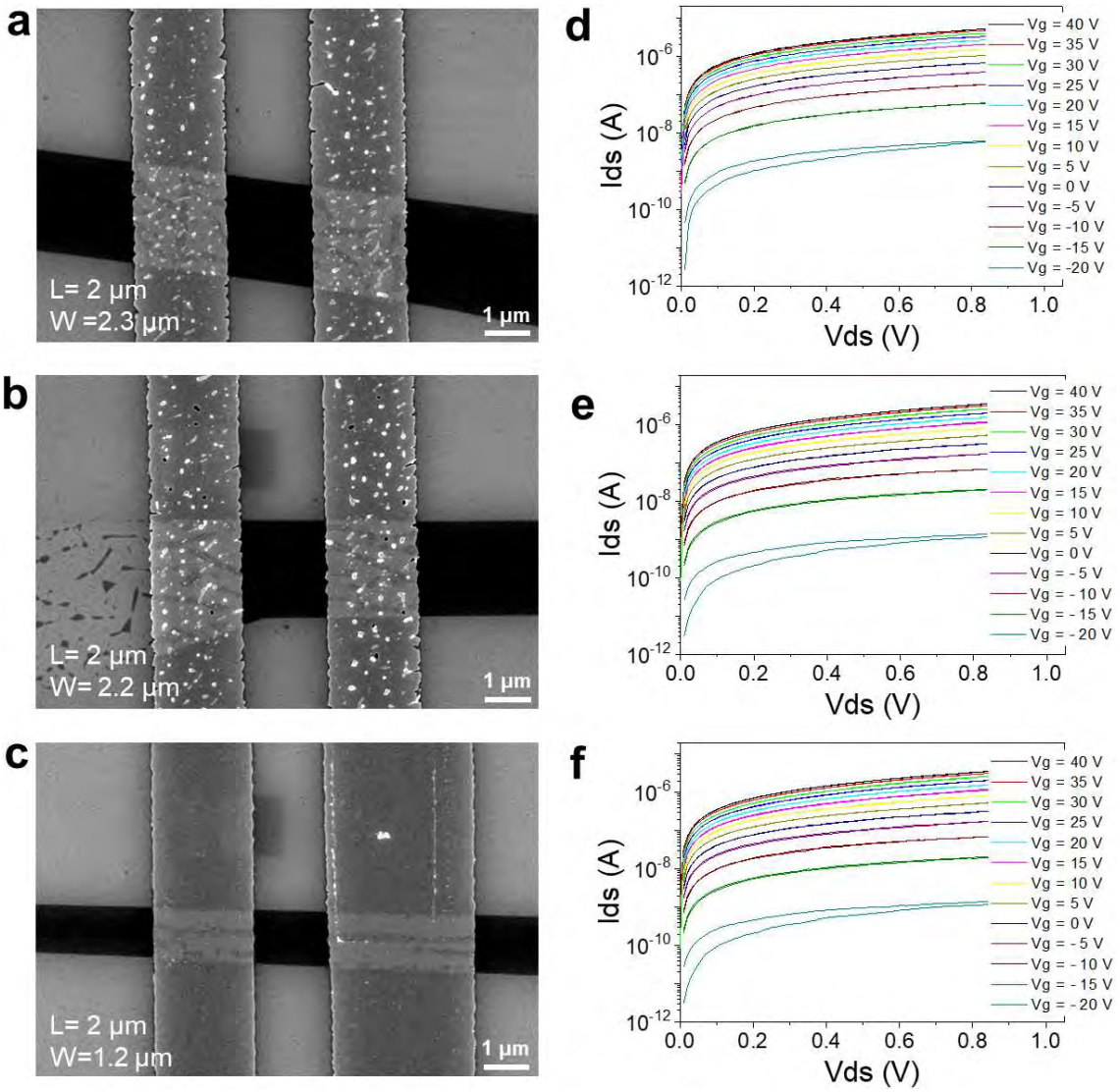

Figure 5.7 SEM images of the channel in the MoS_2 transistors and the output curves. (a)-(c) SEM images of three transistors and their channel length and width. (d)-(f) Output curves of the MoS_2 transistors in (a) to (c).

In pursuit of a more comprehensive analysis of the performance of ME MoS_2 transistors, we created six additional transistors using exfoliated MoS_2 as the channel material. Upon the completion of the fabrication process, we characterized the output curves for each transistor, with these initial results depicted as black lines in Figure 5.8. Subsequently, we stored the transistors in a dry box for a duration of one month, maintaining the internal humidity at approximately 10%. The subsequent output curves, post one-month storage, are represented by red lines in Figure 5.8. Throughout both testing phases, no gate bias was applied to the transistors.

The visual distinction between the black and red lines in Figure 5.8 is quite evident, highlighting a performance discrepancy. The findings suggest that the current of the ME MoS_2-based transistors undergoes degradation over time. Nonetheless, the observed reduction in current is only from 10^{-6} A to $10^{-7}/10^{-8}$ A, which remains within acceptable scale. The thickness of the MoS_2 flakes for each transistor is indicated in the top-right corner of the respective plots in Figure 5.8. Our study indicates that variations in MoS_2 thickness do not exert a significant impact on the retention performance of the back-gate transistors.

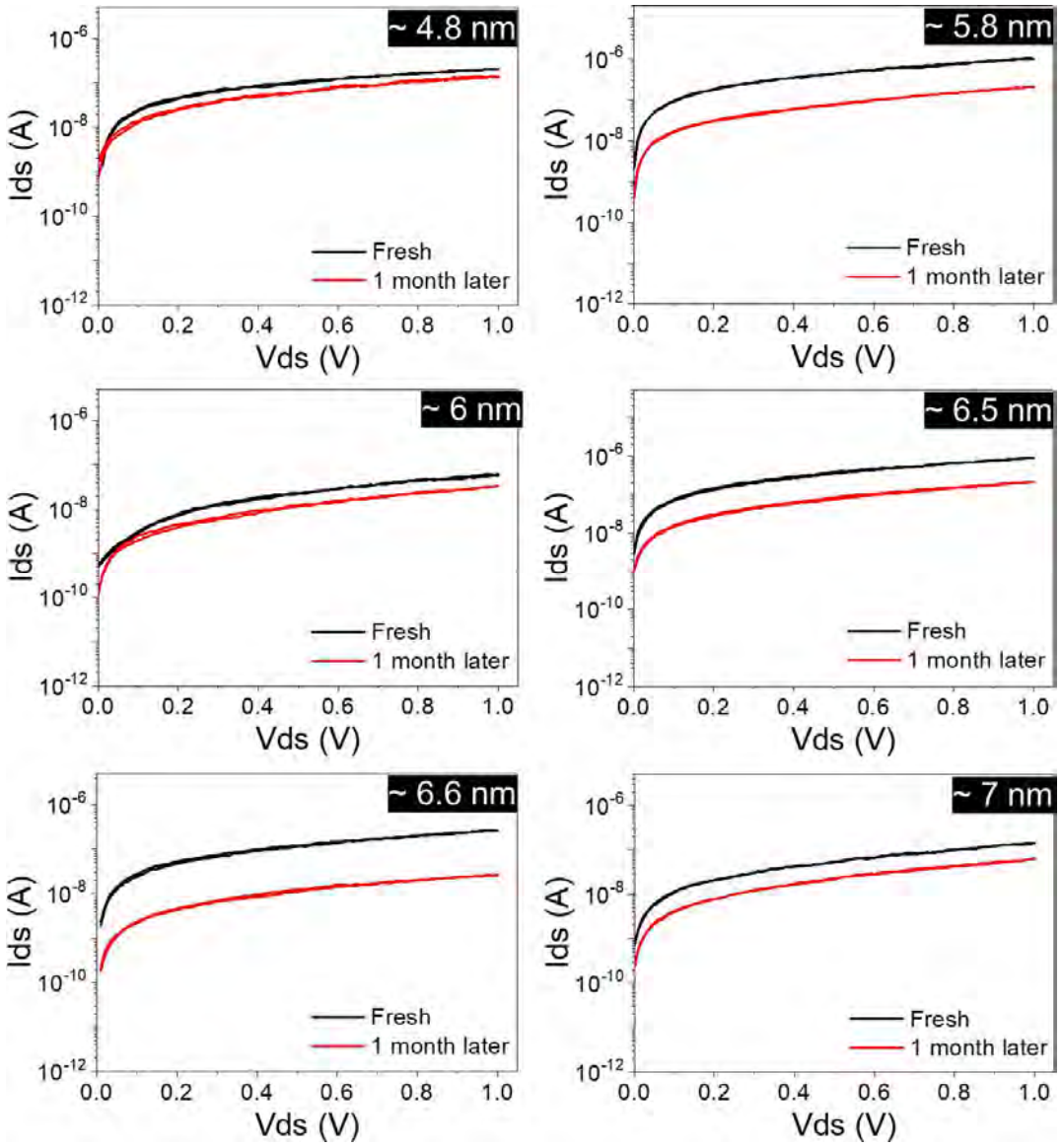

Figure 5.8 Output curves of 6 MoS_2transistors after long time. Black curves present the fresh output curves at $V_g = 0$ V. Red curves present output curves at $V_g = 0$ V after 1 month later.

We suppose that the observed decay in the planar current is attributable to the adsorption of atmospheric moisture by the MoS_2 channel, as suggested by reference [247]. To shield the MoS_2 from environmental exposure, we implemented a protective layer of ME h-BN with a thickness of approximately 10 nm atop the transistor, as illustrated in Figures 5.9a and 5.9b.

Initially, upon fabricating the transistors, we characterized and recorded their output curves, which are indicated as fresh in the plots with black lines. Later, we transferred the ME h-BN layer over the transistors and stored them in a dry environment with a humidity level of 10%. After a period of one month, we retrieved the transistors, reassessed their output curves, and represented these new measurements with red lines in the plots.

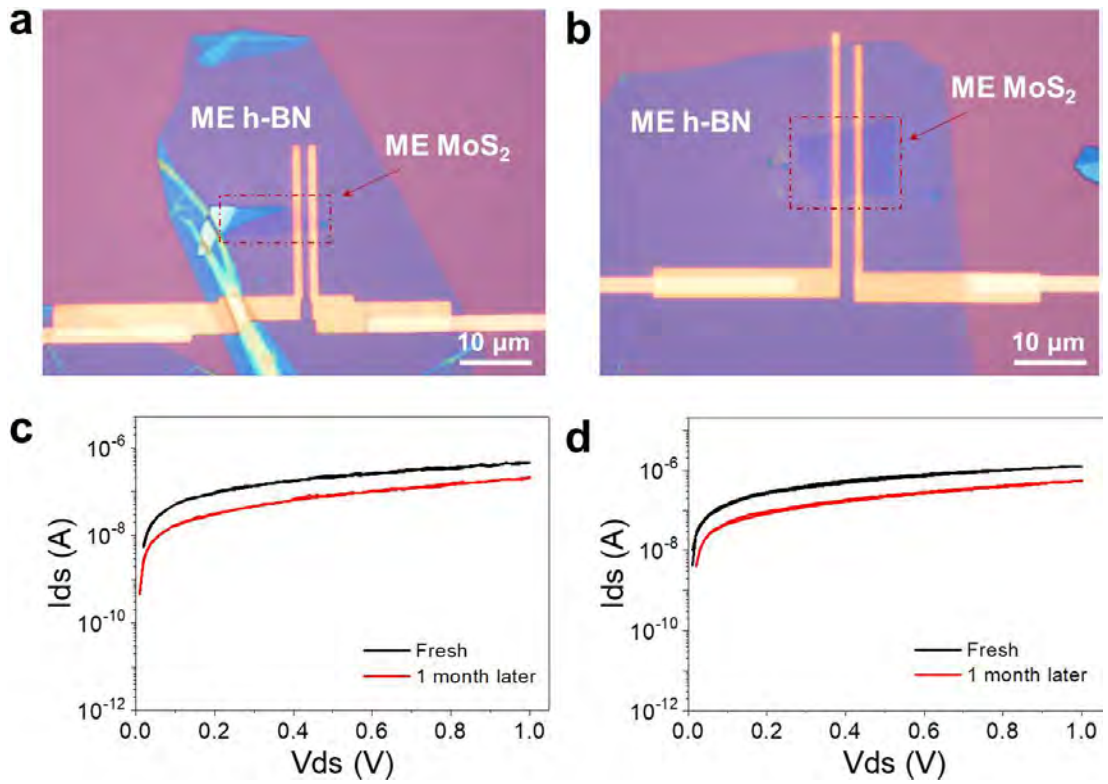

Figure 5.9 ME h-BN as a protective layer for MoS_2 transistors. (a)-(b) Optical microscope images of two MoS_2 transistors covered by ME h-BN flakes. (c)-(d) Output curves of the transistors in (a) and (b), respectively. Black lines are the output curves obtained from fresh devices and red lines are the output curves obtained from the transistor 1 month later.

However, this protective approach did not yield the desired outcome, as evidenced by the output curves in Figures 5.9c and 5.9d, which show no significant deviation from the initial curves in Figure 5.8—those without the h-BN overlay on the MoS_2 surface. This is contrary to other studies that have reported positive results using ME h-BN as a protective layer for MoS_2 transistors [107]. We speculate that during the initial electrical characterization, the MoS_2 may have already absorbed moisture from the air, rendering the subsequent protection ineffective. Nevertheless, it is plausible that the transistor performance could be restored through an annealing process [247].

The transistors fabricated via the EBL method in the research exhibit a decreasing output current level, as shown in Figure 5.8. Despite this decrease, the final output current remains consistent among all transistors. This consistency in low current levels is beneficial for use as a current limiting element in electronic devices, particularly memristors. The low current can be employed to restrict the width of conductive filaments in memristors, facilitating the reset process from the LRS to HRS state.

5.3. 1T1M cell

5.3.1. Characterization of 1T1M cell

Each 1T1M cell consists of one back-gated transistor with mechanically exfoliated MoS_2 as the semiconducting channel in which 300 nm SiO_2 is used as gate dielectric and one memristor with a top-to-down vertical structure like Au/Ag/CVD h-BN/Au. The MoS_2 channel has a length of 2 μm and a width that varies from one device to another from 2 μm to 6 μm, and the memristor has a lateral size of 500 nm by 600 nm. The devices are fabricated on a 300 nm SiO_2/Si wafer via electron beam lithography, electron beam evaporation, wet transfer, and lift-off. The entire fabrication process is described in Figure 10a-e. The h-BN stack, grown via CVD on Cu foil, was purchased in Graphene Supermarket; the fact that we used commercial sources for the 2D materials gives more relevance to this study, as it can be reproduced by anyone.

The transfer of the h-BN stack was done following a standard wet transfer process, consisting of PMMA spin coating, and backing at 100 ºC for 3 min, etching the Cu foil in $FeCl_3$ solution for 2 hours, washing in HCl for 10 seconds, washing in pure water for

20 min, fishing the PMMA/h-BN stack with the target substrate, and removing the PMMA with an acetone bath for 12 hours. Regarding the MoS_2 channel of the transistors, bulk crystals from the Moly Hill mine were purchased on eBay, we exfoliated them using scotch tape and transferred them onto the target sample using a stage from Onway technology and a flexible and transparent stamp made of PDMS.

The correct fabrication of the devices was confirmed using an optical microscope (model LV100ND from Nikon), one SEM (model Gemini 500 from Carl Zeiss), a TEM (model JEM-2100 from JEOL), and one AFM (model Multimode V from Veeco). For the cross-sectional TEM experiments, sample preparation via a focused ion beam (FIB, model Helios NanoLab 450S) was needed. All the devices were characterized using a SPA (model 4200 from Keithley) connected to a probe station (model M150 from Cascade).

5.3.2. Result and Discussion

Figure 10f-g shows that the surface of the mechanically exfoliated MoS_2 layer remains clean of contaminants even after being transferred on the 300 nm SiO_2/Si substrate. The morphology of the memristor device is presented in Figure 10h, where the top (horizontal) and bottom (vertical) electrodes can be observed. The h-BN film in between the two electrodes can also be easily identified, as it formed some wrinkles. The cross-sectional TEM images of the Ag/h-BN/Au memristors reflect the correct layer structure of the h-BN (~15 layers, see Figure 10i). However, the presence of local defects in the lattice of the h-BN and at the interfaces is evident, which is a major difference compared to mechanically exfoliated h-BN stacks [236]. Note that the presence of these defects is necessary to reduce the energy-to-breakdown and enable the memristive effect, and that mechanically exfoliated multilayer h-BN stacks do not exhibit stable switching [197].

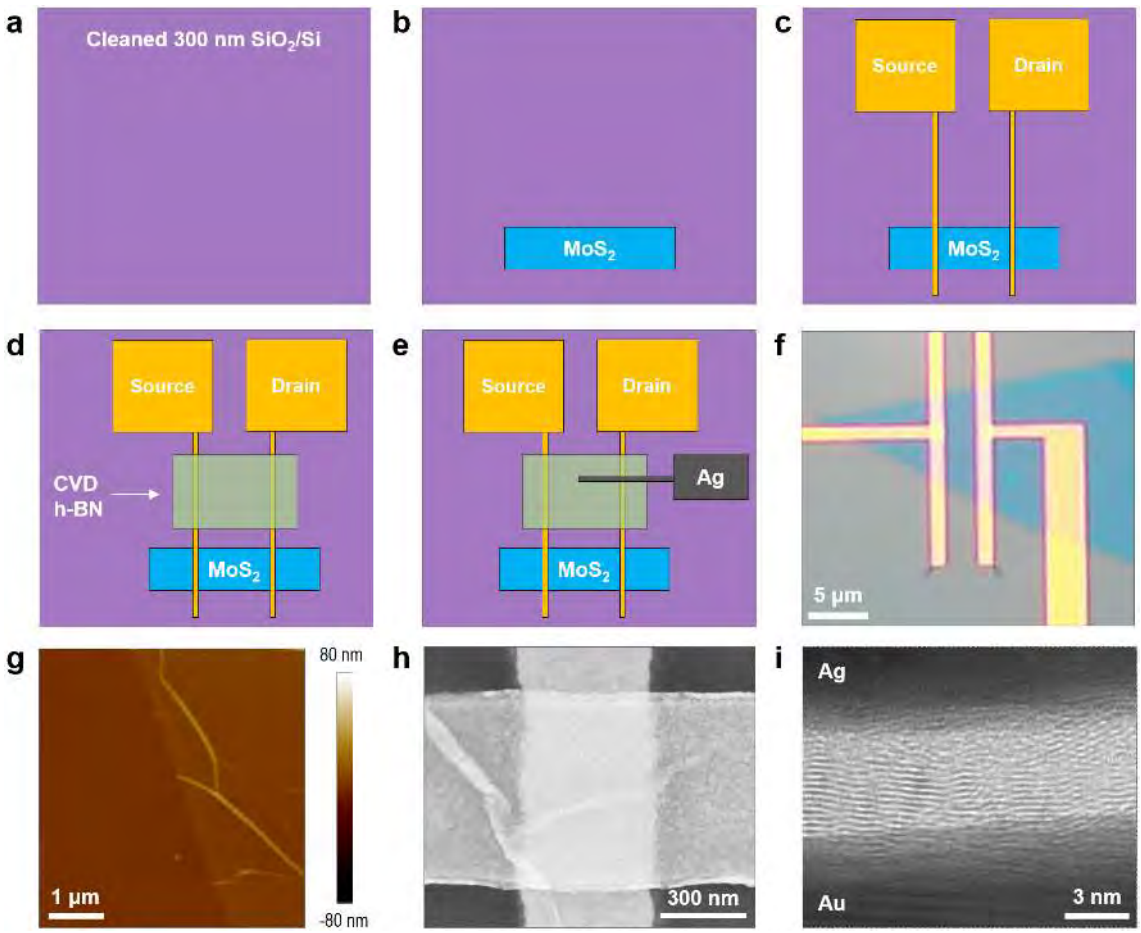

Figure 5.10 Fabrication and morphology of the 1T1M cell. (a-e) Fabrication flow for the 1T1M cells. (f) Optical microscope of the MoS_2 transistor. (g) AFM topographic map of the edge of the MoS_2 flake on the substrate. (h) Memristor device under the SEM view. (i) Cross-section TEM images showing the defect-rich layered structure of the h-BN stack.

After the 1T1M cell is fabricated, the electric characterization is going on with one SPA connected to a probe station. The connection between the terminals and the 1T1M cell is shown in Figure 5.11. SMU with voltage touches the top of Au/Ag/h-BN/Au (from top to bottom) memristor, and RVS will be applied through this probe. Another probe connects the GND to the source (S) of the MoS_2 transistor. By employing this method, when a voltage is applied across the SUM, the electrical current must traverse the memristor, proceed through the transistor, and ultimately return to the ground.

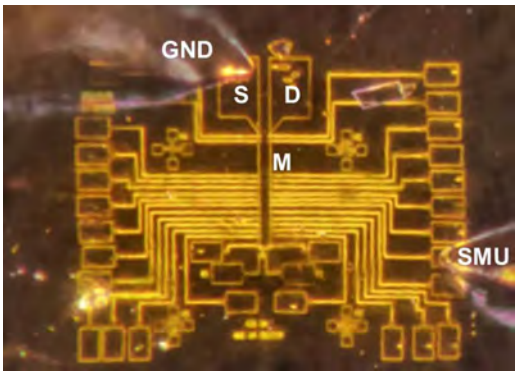

Figure 5.11 1T1M cell electrical characterization in the probe station.

We characterize the electrical properties of the MoS_2 transistors in DC (direct current) by applying RVS between the source and drain at different constant gate voltages (Figure 5.12a), as well as by applying RVS at the gate at a constant source-to-drain voltage (Figure 5.12b) – these figures-of-merit are often called output and transfer characteristics, respectively. As it can be seen, the transistor is normally in on-state (for V_g=0V), and it requires the application of a negative voltage to be switched off. This behavior has been also observed in other studies [248,249], which has been associated with unintentional n-doping of the MoS_2 channel.

Next, we characterize isolated Au/Ag/h-BN/Au memristors in DC by applying RVS, using a current limitation of 1 μA. The devices show a transition from the HRS to the LRS at ~1.65 V and a transition from LRS to HRS at ~0.1 V – these events are often called set and reset, respectively (see Figure 5.12c). Similar threshold-type RS in h-BN has been observed in multiple publications [229,250]. However, it is well known that the current limitation of the semiconductor parameter analyzer takes around ~70 μs to respond [220], meaning that during that time the current is unlimited and could uncontrollably damage the device. This produces a characteristic current overshoot and reduces the lifetime of the device – that might be the reason why references [196,251] only demonstrate a few RS cycles.

Then, we measure the 1T1M cell by applying ramped voltage stresses between the top electrode of the memristor and the source of the transistor, without using a gate voltage. Under these circumstances, the maximum current that can flow across the MoS_2 channel of the transistor is ~0.1 μA, and that will be also the maximum current

that can flow across the Au/Ag/h-BN/Au memristor. Figure 5.12d shows that the 1T1M cell successfully limited the current to ~0.1 μA without the current compliance function in the semiconductor parameter analyzer, but with the difference that the transistor-based current limitation is instantaneous.

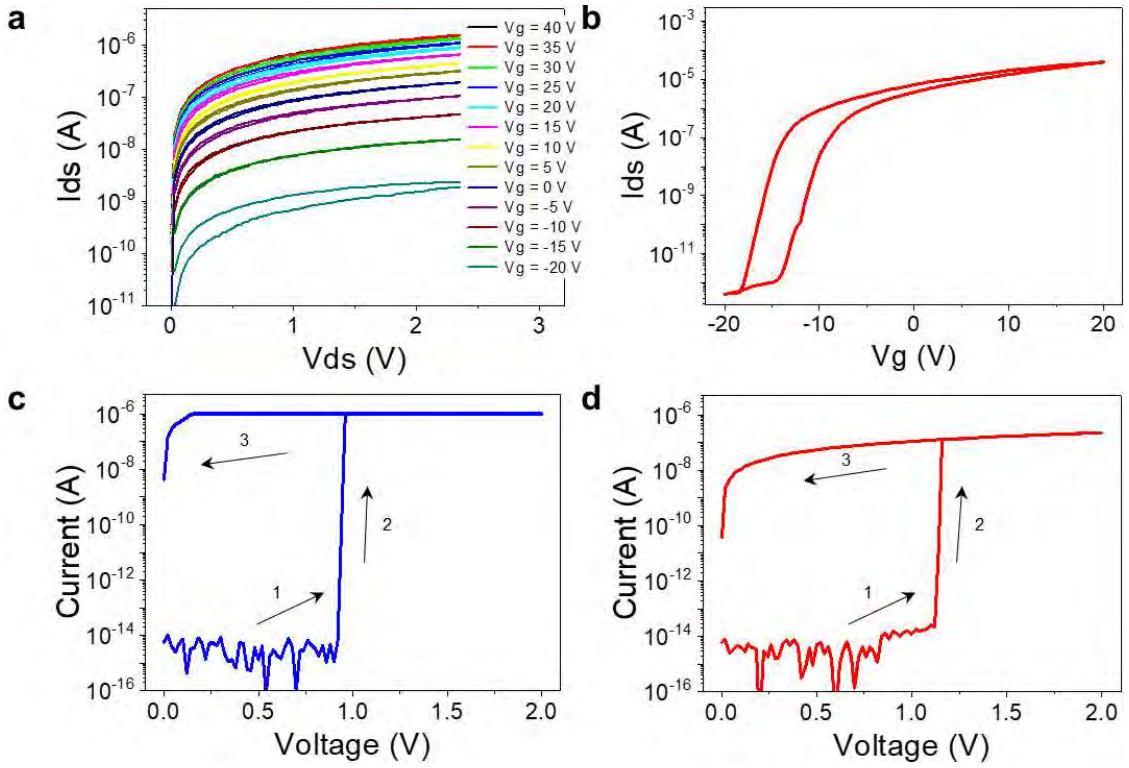

Figure 5.12 Electrical properties of the MoS_2 transistors and Au/Ag/h-BN/Au resistive switching devices. (a) Output characteristic curves of the MoS_2 transistor. The saturation current exhibited a positive relationship with the gate bias applied. (b) Transfer characteristic curve while V_{ds} = 5 V. (c) I-V curve of the Au/Ag/h-BN/Au memristor with a current limitation of 1 μA, imposed by the semiconductor parameter analyzer. (d) Performance of the same 1T1M cell than in plot c using the MoS_2 transistor as current limitation element.

Next, we analyze the variability of the threshold-type RS behavior from one device to another by measuring many more cells. The results indicate that all the cells could switch on below 1 V bias as the Ag+ ions are very diffusive and can easily form the conductive filament/s [252]. While the RS behavior is reproducible in all devices (with R_{HRS}/R_{LRS} ratios always above 100) the set and reset voltages and the state resistances

show variability from one cycle to another and from one device to another. Nevertheless, these deviations are like the ones observed in made of other materials, such as metal-oxides [253] and phase-change [254]. The LRS current can be easily adjusted by changing the gate voltage of the transistors (see Figure 5.14a), which could be used to match characteristics across different devices. However, this may not be needed because in most applications the threshold-type RS is used to identify two states with high R_{HRS}/R_{LRS} ratio, and small fluctuations of R_{HRS} and R_{LRS} as those observed in Figure 5.13 are allowed.

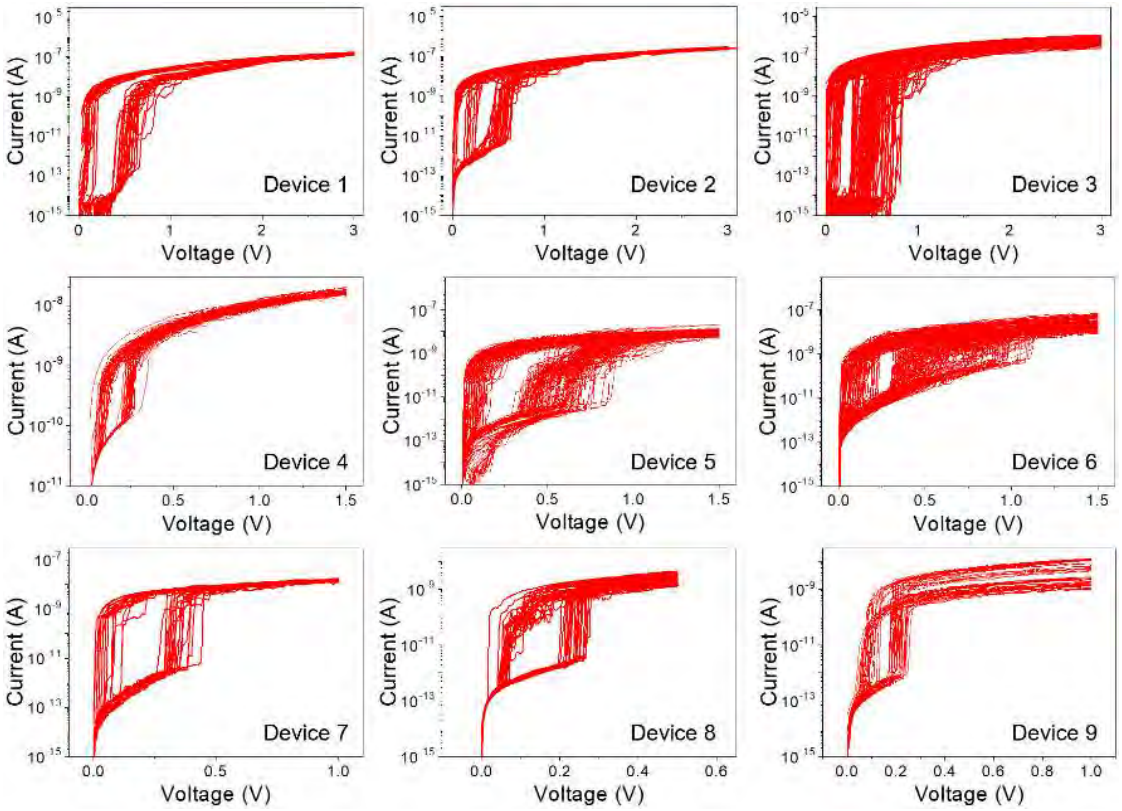

Figure 5.13 Device-to-device variability in all-2D 1T1M cells. I-V plots for nine different all-2D 1T1M cells exhibiting threshold-type RS behavior. All the devices show similar switching voltages and R_{HRS}/R_{LRS} ratios of more than 100, which allows for clearly identifying each state. There is an inherent variability of the state resistances and switching voltages, although this is allowed by the targeted applications of this type of device.

We also test the robustness of the RS behavior by applying long sequences of ramped voltage stresses to the all-2D 1T1M cells. As Figure 5.14b shows, there is an intrinsic variability of switching voltages and state resistances, which is in line with that

observed in other studies. Figure 5.14c shows the resistance versus cycle plot, in which it can be observed that the R_{HRS}/R_{LRS} ratio is always higher than 10, which allows easy state identification.

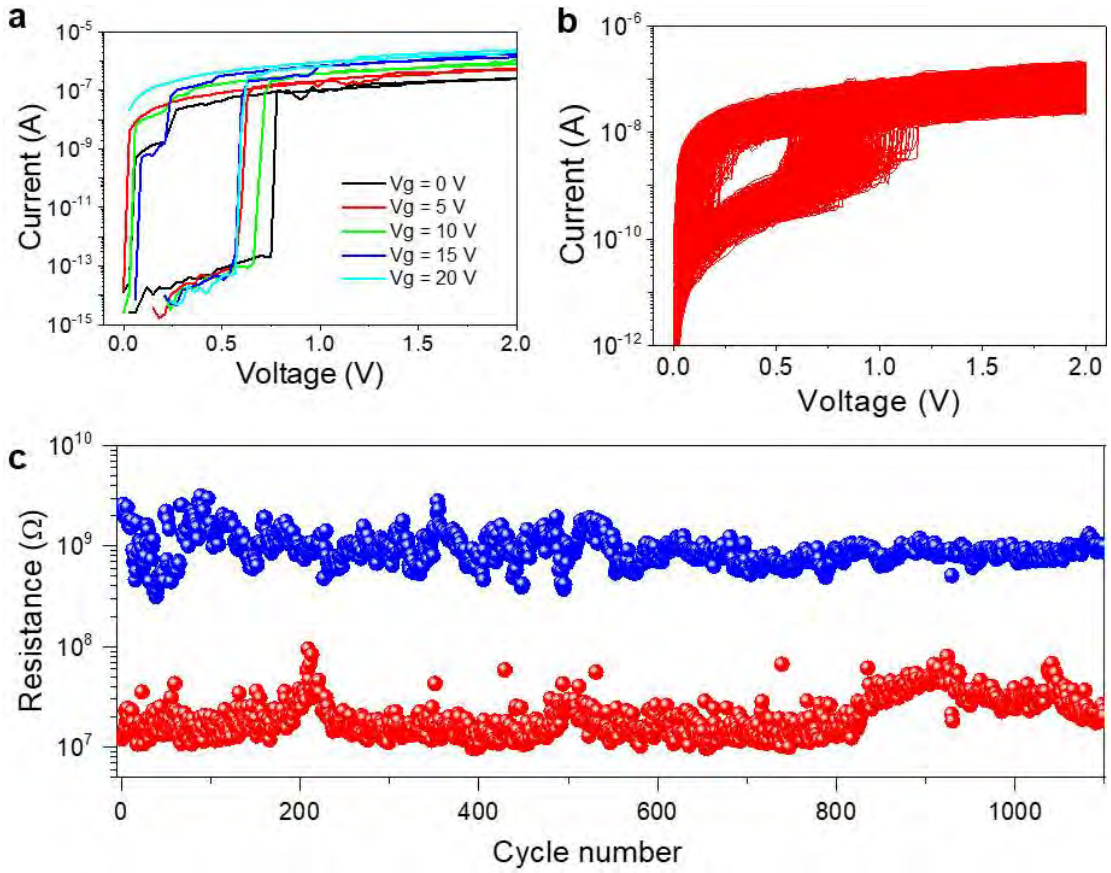

Figure 5.14 Electrical properties of the MoS_2/h-BN 1T1M cells. (a) Typical I-V plot showing threshold RS behavior in an Au/Ag/h-Bn/Au device for different gate voltages in the MoS_2 transistor. (b) Typical I-V plot showing threshold RS behavior in an Au/Ag/h-Bn/Au device for more than 1000 cycles. (c) Endurance plot measured in the 1T1M cell always has a LRS/HRS resistance ratio over 10, enough to detect the resistance of the states.

The set and reset voltages extracted from Figure 5.14b are plotted in Figure 5.15 The set voltage ranges from 0.6 V to 1 V, whereas the reset voltage has a narrower range of only 0.2 V. The device can set around 1 V and reset less than 0.5 V. The variability of the set and reset voltages is similar to the single Au/Ag/multilayer h-BN/Au memristors in Chapter 4.

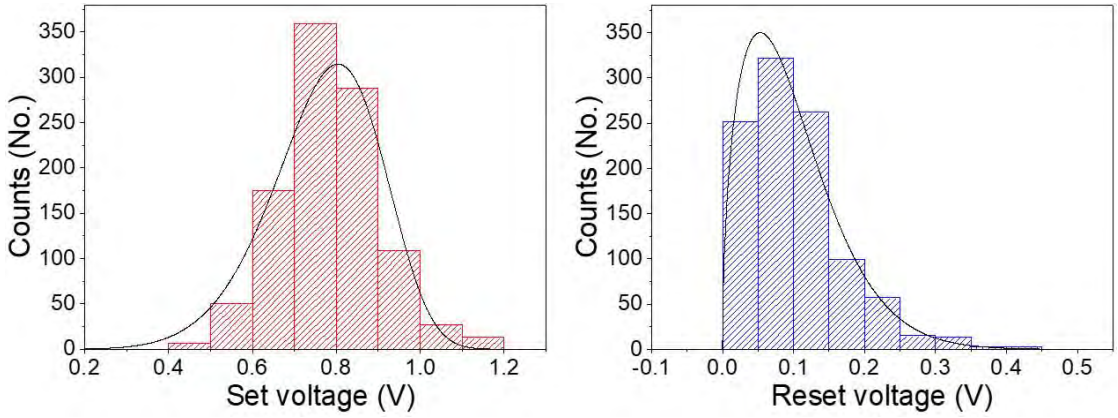

Figure 5.15 Statistical analysis of the device's set and reset voltages in Figure 5.14b. The black line is the Weibull distribution.

Finally, we compare the device performance of our all-2D 1T1M cells with that of others previously reported, as shown in Table 5.1. Our MoS_2/h-BN 1T1M cells are the only ones that exhibit threshold-type RS behavior, with the additional advantages of relatively small size and relatively high endurance. More importantly, we characterize several 1T1M cells, something not done in previous studies. In addition, our devices exhibit the lowest operation currents, which is beneficial for reducing energy consumption.

Table 5.1 Comparison of 1T1M cells based on 2D materials

Metrics	Ref. 238	Ref. 239	Ref. 240	Ref. 241	Ref. 242	This work
Transistor channel	1L CVD MoS_2	4L ME WSe_2	1L CVD WS_2	1L MOCVD MoS_2	2nm CVD MoS_2	3 nm ME MoS_2
Transistor size	L=2 μm	L=1.8 μm W=20.5 μm	L=1 μm	L=1 μm W=50 μm	L=2 μm	L=2 μm W=2 to 6 μm
Transistor Source/Drain	Au	Ag	Graphene	Au	Ti	Au
Transistor Gate	Back-gate	Back-gate	Top-gate	Back-gate	Back-gate	Back-gate
Memristor	Au/Ti/10 - 13 L CVD h-BN/Au	Ag/WSe_2/Ag	Au/Ti/5nm CVD h-BN/Graphene	Au/CVD MoS_2/Au	Ti/2 nm CVD MoS_2/p^+Si	Au/Ag/6 nm CVD h-BN/Au
Memristor size	0.5-1.5 μm^2	490 μm^2	12 μm^2	50 μm^2	NA	0.3-1 μm^2
Switching mode	Non-volatile bipolar	Non-volatile unipolar	Non-volatile bipolar	Non-volatile bipolar	Non-volatile bipolar	Threshold unipolar
R_{LRS}/R_{HRS}	~10^2	70	10^2	10^5	10^5-10^6	10^2
Switching cycles	50 (DC)	90 (DC)	1000 (AC)	5000 (AC)	35 (DC)	>1000 (DC)
Switching voltage	<1 V	1.7 V	2.5 V	4 V	3.5 V	<1 V
On current	<130 × 10^{-6} A	NA	10^{-5} A	10^{-5} A	10^{-5} A	10^{-9} to 10^{-7} A
Off current	10^{-12} A	NA	10^{-7} A	10^{-10} A	10^{-10} A	10^{-11} to 10^{-10} A
Test environment	<10^{-4} Torr	NA	NA	NA	Air	Air

5.4. Conclusion

In conclusion, we have fabricated 1T1M cells combining a 4 μm^2 MoS_2 transistor in series with a 0.3 μm^2 h-BN memristor. The h-BN memristors exhibit reproducible threshold-type RS without the need to use the current limitation tool integrated into the semiconductor parameter analyzer, using the MoS_2 transistor as a current limiting element. The 1T1M cells show low operation voltages below 1V and state currents that are consistent over multiple devices, and we readily measure endurances above 1000 cycles. This study contributes to the development of 2D materials-based devices and circuital building blocks with functional capabilities.

Chapter 6: Conclusion and perspectives

In conclusion, in this thesis, we have studied the dielectric property of 2D h-BN and explore its application in micro- and nano-scale electronic devices. We use multilayer h-BN that consists of small micro-flakes produced by mechanical exfoliation and large-area films synthesized via the chemical vapor deposition. The main mechanisms that produce the dielectric breakdown behavior is investigated through dozens of micro/nano scale MIM devices with multiple types of metals, Ag, Au, Pt and Ti, as top electrodes.

During this process, I have learned the mechanical exfoliation method to get 2D materials from bulk and wet transfer method to get clean h-BN from Cu foil. Moreover, I have learned how to use some large equipment used in the semiconductor industry, research institutes and universities, including photolithography, electron beam evaporation and electron beam lithography. In the characterization part, I have learned how to use the atomic force microscope, scanning electron microscope, the Raman spectrometer and the semiconductor parameter analyzer. One of the main advantages of the laboratory where I carried out this research is that I had unlimited access to all these machines, and my research required me to repeat the experiments multiple times to collect statistical information. Hence, I can happily say that I have mastered the use of all these machines, which I believe it will be very useful for me to find a job in the future.

In the first work, we investigate the dielectric breakdown behavior in mechanically exfoliated h-BN flakes, and the results indicate that:

- In mechanically exfoliated h-BN, the dielectric breakdown field depends on the type of metal electrode used. h-BN devices with metal electrodes having a lower diffusivity (like Pt) show higher dielectric breakdown field than others using electrodes like Au and Ti (which have higher diffusivity).
- When using Pt electrodes, one can get a dielectric breakdown voltage that follows a very close dependence with the thickness, leading to an average of 12 MV/cm.

Then we study the dielectric property of h-BN synthesized by chemical vapor deposition on Cu foil and get the conclusions below:

- CVD-grown h-BN has more defects than mechanically exfoliated one, resulting in observable dielectric breakdown at low voltage and observation of RS behavior.
- Memristors based on CVD-grown h-BN with the size of 120 nm × 250 nm are fabricated and characterized. The memristor's resistive switching varies depending on the top electrode metal used. The memristors are volatile with Ag electrodes, and non-volatile with Ti and Au electrodes.

In our third work, we connected a MoS_2-based transistor in series with a h-BN memristor to form a 1T1M cell to enhance the memristor's electrical performance. We have drawn some conclusions from this study.

- Transistor based on MoS_2 works well as a current limitation element in the 1T1M. The current limitation forced by the transistor can limit the width of the conductive filaments in h-BN, ensuring the revertible threshold resistive switching in Au/Ag/h-BN/Au memristors.
- 1T1M cells combining a 4 μm^2 MoS_2 transistor in series with a 0.3 μm^2 h-BN memristor achieve more than 1000 cycles, which is higher than the single memristors using the same materials and structure previously achieved in this work.
- The 1T1M cell has a low operation voltage of 1 V and a very low off-state current of around 10^{-11} A, which is beneficial for energy savings.

Some areas still require further study. For instance, thinner ME h-BN flakes of less than 5 nm need to be examined, and more MIM samples are needed to conduct dielectric breakdown research. Moreover, CVD-grown multilayer h-BN needs to be more uniform after wet transfer to reduce device-to-device variability in memristors. For that reason, the research team to which I belonged is now exploring industrial CVD-grown samples from the company Aixtron, which is the only supplier capable of providing very good quality that is furthermore consistent from one batch to another. While the 1T1M cell has shown over 1000 cycles in DC mode, it is believed that it can achieve a higher endurance in pulse mode, which requires further research.

Overall, the data about multilayer h-BN dielectrics and resistive switching layers has yielded interesting results that can serve as the foundation for deployment of this material in circuits containing transistors and/or memristors, which have applications for data storage and in-memory computing – although dealing with real applications was out of the scope of this PhD thesis, as we focus on material and device properties.

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Appendix A: Scientific curriculum vitae

PERSONAL INFORMATION

Name: Bin Yuan
Date of birth: October 24th, 1989
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Phone: +86 13584813423
Email: bin_yuan2016@126.com

EDUCATION BACKGROUND

Nov. 2020 ~ Present	PhD in Nanoscience University of Barcelona
Sep. 2016 ~ Jun. 2019	Master in Materials Science and Engineering FUNSOM, Soochow University
Sep. 2007 ~ Jun. 2011	Bachelor in Materials Forming and Control Engineering Taiyuan University of Technology

RESEARCH EXPERIENCE

- **Research Topic 1:** 2D material mechanical exfoliation and dielectric research.

  1. Mechanical exfoliation of h-BN materials.
  2. Metal-Insulator-Metal device fabrication.
  3. Topography and electrical characterization and data analysis.

- **Research Topic 2:** Memristor based on CVD-grown h-BN.

  1. Use EBL and E-beam evaporator to fabricate the h-BN memristor.
  2. Electrical measurements with semiconductor parameter analysis.

- **Research Topic 3:** 1T1M cell fabrication and characterization.

  1. Transistor based on MoS_2 fabrication and parameter analysis.
  2. 1T1M cell fabrication.
  3. Electrical characterization of 1T1M cell.

EQUIPMENT SKILLS

- **Device fabrication:**
  Photolithography, electron beam evaporation, magnetron sputtering, atomic layer deposition, electron beam lithography

- **Device characterization:**
  Optical microscope, scanning electron microscope, atomic force microscope, semiconductor parameter analyzer.

JOURNAL PAPERS

1. Mario Lanza*, Felix Palumbo*, Yuanyuan Shi, Fernando Aguirre, Santiago Boyeras, **Bin Yuan**, Eilam Yalon, Enrique Moreno, Tianru Wu, Juan B. Roldan, "Temperature of conductive nanofilaments in hexagonal boron nitride based memristors showing threshold resistive switching," *Advanced Electronic Materials***,** 8, 8, 2100580, 2022.

2. Yiping Xiao, Wenwen Zheng, **Bin Yuan**, Chao Wen, Mario Lanza*, "Highly accurate thickness determination of 2D materials," *Crystal Research & Technology*, 56, 6, 2100056, 2021.

3. **Bin Yuan**, Xianhu Liang, Liubiao Zhong, Yuanyuan Shi, Felix Palumbo, Shaochuan Chen, Fei Hui, Xu Jing, Marco A. Villena, Lin Jiang, Mario Lanza*, "150 nm × 200 nm Cross-point hexagonal boron nitride based memristors," *Advanced Electronic Materials*, 6, 12, 1900115, 2020.

4. Shaochuan Chen, Mohammad Reza Mahmoodi, Yuanyuan Shi, Chandreswar Mahata, **Bin Yuan**, Xianhu Liang, Chao Wen, Fei Hui, Deji Akinwande, Dmitri B. Strukov, Mario Lanza*, "Wafer-scale integration of two-dimensional materials in high-density memristive crossbar arrays for artificial neural networks," *Nature Electronics***,** 3, 638-645, 2020.

5. Kaichen Zhu, Xianhu Liang, **Bin Yuan**, Marco A. Villena, Chao Wen, Tao Wang, Shaochuan Chen, Fei Hui, Yuanyuan Shi, Mario Lanza* "Graphene-boron nitride-graphene cross-point memristors with three stable resistive states," *ACS Applied Materials & Interfaces*, 11, 41, 37999-38005, 2019.

6. Marco A. Villena, Fei Hui, Xianhu Liang, Yuanyuan Shi, **Bin Yuan**, Xu Jing, Kaichen Zhu, Shaochuan Chen, Mario Lanza*, "Variability of metal/h-BN/metal memristors grown via chemical vapor deposition on different materials," *Microelectronics Reliability*, 102, 113410, 2019.

7. Yuanyuan Shi, Xianhu Liang, **Bin Yuan**, Victoria Chen, Haitong Li, Fei Hui, Zhouchangwan Yu, Fang Yuan, Eric Pop, H.-S. Philip Wong, Mario Lanza*, "Electronic synapses made of layered two-dimensional materials," *Nature Electronics*, 1, 458-465, 2018.

8. Na Xiao, Marco A. Villena, **Bin Yuan**, Shaochuan Chen, Bingru Wang, Marek Eliáš, Yuanyuan Shi, Fei Hui, Xu Jing, Andrew Scheuermann, Kechao Tang, Paul C. McIntyre, Mario Lanza*, "Resistive random access memory cells with a bilayer TiO_2/SiO_X insulating stack for simultaneous filamentary and distributed resistive switching," *Advanced Functional Materials*, 27, 33, 1700384, 2017.

9. Felix Palumbo, Xianhu Liang, **Bin Yuan**, Yuanyuan Shi, Fei Hui, Marco A. Villena, Mario Lanza*, "Bimodal dielectric breakdown in electronic devices using chemical vapor deposited hexagonal boron nitride as dielectric," *Advanced Electronic Materials*, 4, 3, 1700506, 2018.

10. Fei Hui, Shaochuan Chen, Xianhu Liang, **Bin Yuan**, Xu Jing, Yuanyuan Shi, Mario Lanza*, "Graphene coated nanoprobes: A review," *Crystals*, 7, 9, 269, 2017.

CONFERENCE

1. IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits, 2019, 2-5 July, the Grand Hyatt, Hangzhou, China.

2. Xinahu Liang, Bin Yaun, Yuanyuan Shi, Fei Hui, Xu Jing, Mario Lanza, Felix Palumbo, Enhanced reliability of hexagonal boron nitride dielectric stacks due to high thermal conductivity, IEEE International Reliability Physics Symposium, 2018, 11-15 March, Burlingame, CA, USA.

3. IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits, 2017, 4-7 July, the Ritz Carlton, Chengdu, China.

4. China Resistive Random Access Memory International Workshop, 2017, 12-13 June, Soochow University, Suzhou, China.

AWARDS

- 2018 Postgraduate Academic Scholarship, Soochow University
- 2017 Postgraduate Academic Scholarship, Soochow University
- 2016 Postgraduate Academic Scholarship, Soochow University

OTHER SKILLS

- College English Test (CET) Level 4 (461 points), Level 6 (471 points).

Appendix B: Summary in official language

En conclusió, en aquesta tesi, hem estudiat la propietat dielèrtica del 2D h-BN i l'hem explorat en aplicacions en dispositius electrònics a l'escala micro- i nano-. Utilitzem h-BN multilayer que consisteix en petites micro-llamades produïdes per exfoliació mecànica i pel·lícules de gran àrea sintetitzades a través del depòsit de vapor químic. Els principals mecanismes que produeixen el comportament de ruptura dielèrtica s'han investigat a través de dúzies de dispositius MIM a l'escala micro/nano amb diversos tipus de metalls, Ag, Au, Pt i Ti, com a electrodes superiors.

Durant aquest procés, he après el mètode d'exfoliació mecànica per obtenir materials 2D del massís i el mètode de transferència húmid per obtenir h-BN net des del full de coure. A més, he après com utilitzar algunes grans màquines utilitzades en la indústria semiconductor, instituts de recerca i universitats, inclús la litografia fotogràfica, la evaporació de raig electrò i la litografia de raig electrò. En la part de caracterització, he après com utilitzar el microscopi d'una sola volta, el microscopi electrò de barret, el espectròmetre Raman i l'analyzer de paràmetres semiconductors. Un dels principals avantatges del laboratori on vaig dur a terme aquesta recerca és que tenia accés il·limitat a totes aquestes màquines, i la meva recerca em va requerir repetir les proves múltiples vegades per recollir informació estadística. Per tant, puc dir feliçment que he dominat l'ús de totes aquestes màquines, i crec que serà molt útil per mi per trobar un treball en el futur.

En la primera feina, hem investigat el comportament de ruptura dielèrtica en fulls de h-BN exfolats mecànicament, i els resultats indiquen que:

- En el h-BN exfolat mecànicament, el camp de ruptura dielèrtica depèn del tipus d'electro metallí usat. Els dispositius de h-BN amb electrodes metalls amb una difusivitat més baixa (com el Pt) mostren un camp de ruptura dielèrtica més alt que els altres que utilitzen electrodes com l'Au i el Ti (que tenen una difusivitat més alta).

- Quan s'utilitzen electrodes de Pt, es pot obtenir un voltatge de ruptura dielèrtica que segueix una dependència molt estreta amb el gruix, conduint a una mitjana de 12 MV/cm.

A continuació, hem estudiat la propietat dielèrtica del h-BN sintetitzat per CVD en full de coure i hem obtingut les conclusions següents:

- El h-BN CVD crescut té més defects que el exfolat mecànicament, resultat en una ruptura dielèrtica observable a baixa tensió i observació del comportament RS.
- Els memristors basats en h-BN CVD- crescut amb una mida de 120 nm × 250 nm s'han fabricat i caracteritzat. L'intercanvi resistiu dels memristors varia segons el metall de l'electro superior utilitzat. Els memristors són volàtils amb electrodes d'Ag i no volàtils amb electrodes de Ti i Au.

En la nostra tercera feina, hem connectat un transistor basat en MoS_2 en sèrie amb un memristor de h-BN per formar una cel·la 1T1M per millorar el rendiment elèctric del memristor. Hem traçat algunes conclusions d'aquest estudi.

- El transistor basat en MoS_2 funciona bé com a element de limitació de corrent en la 1T1M. La limitació de corrent imposa pel transistor pot limitar l'amplada del filament conductor en h-BN, assegurant l'intercanvi resistiu umbral revertible en memristors Au/Ag/h-BN/Au.
- Les cel·les 1T1M que combinen un transistor MoS_2 de 4 μm^2 en sèrie amb un memristor h-BN de 0.3 μm^2 assoliran més de 1000 cicles, que és més alt que els memristors individuals que utilitzaven els mateixos materials i estructura en aquesta feina.
- La cel·la 1T1M té un voltatge d'operació baix de 1 V i un corrent d'estat fora molt baix d'alrededor de 10^{-11} A, el que és beneficios per a l'estalvi d'energia.

Algunes àrees encara requereixen més estudi. Per exemple, els fulls de h-BN ME més prims de menys de 5 nm necessiten ser examinats, i més mostres MIM són necessàries per dur a terme la recerca de ruptura dielèrtica. A més, el h-BN multilayer CVD necessita ser més uniforme després de la transferència húmid per reduir la variabilitat del dispositiu al dispositiu en memristors. Per aquest motiu, l'equip de

recerca al qual pertanyo està explorant mostres CVD industrials de l'empresa Aixtron, que és l'únic proveïdor capaç de proporcionar una bona qualitat que és, a més, consistent de lot en lot. Mentre que la cel·la 1T1M ha mostrat més de 1000 cicles en mode de corrent continu, es creu que pot assolir una major resistència en mode de puls, el que requereix més recerca.

En general, les dades sobre dielèctrics de h-BN multilayer i capes d'intercanvi resistiu han donat resultats interessants que poden servir com a base per a la implementació d'aquest material en circuits que contenen transistors i/o memristors, que tenen aplicacions per a l'emmagatzematge de dades i en la computació en memòria - encara que tractar amb aplicacions reals estava fora de l'abast d'aquesta tesi de doctorat, ja que estem enfocant en propietats de materials i dispositius..

Appendix C: List of acronyms

IoT	internet of things
2D	two-dimensional
h-BN	hexagonal boron nitride
CVD	chemical vapor deposition
MIM	metal-insulator-metal
1T1M	one-transistor-one-memristor
MoS_2	molybdenum disulfide
SiO_2	silicon dioxide
Al_2O_3	aluminum oxide
HfO_2	hafnium dioxide
Si	silicon
high-k	high dielectric constant
CMOS	complementary metal oxide semiconductor
DRAM	dynamic random-access memory
IC	integrated circuit
NbS_2	niobium disulfide
TMDs	transition metal dichalcogenides
WS_2	tungsten disulfide
WSe_2	tungsten diselenide
SS	sub-threshold swing
CaF_2	calcium fluoride
$SrTiO_3$	strontium titanate
Bi_2SeO_5	bismuth selenite
FET	field effect transistor
SnO_2	tin dioxide
Bi_2O_2Se	bismuth oxyselenide
ADF	annular dark-field
B	boron
N	nitride
ME	mechanical exfoliation
LPE	liquid-phase exfoliation
PVD	physical vapor deposition
MBE	molecular beam epitaxy
IPA	isopropanol
Cu	copper
Ni	nickel
Pt	platinum
Fe	iron
H_2	hydrogen
Ar	argon
SiC	silicon carbide

MOCVD	metal-organic chemical vapor deposition
N_2	nitrogen
CAFM	conductive atomic force microscope
RS	resistive switching
RTN	random telegraph noise
Ti	titanium
Au	gold
HRS	high resistance state
LRS	low resistance state
TEM	transmission electron microscope
EFTEM	energy-filtered transmission electron microscopy
HAADF	High-angle annular dark-field
STEM	scanning transmission electron microscope
W	tungsten
Ag	silver
AFM	atomic force microscope
EBL	electron beam lithography
DC	direct current
PDMS	polydimethylsiloxane
OM	optical microscope
PMMA	polymethyl methacrylate
$FeCl_3$	ferric chloride
HCl	hydrochloric acid
DI	deionized
BE	bottom electrode
UV	ultraviolet
DUV	deep ultraviolet
EUV	extreme ultraviolet
Cr	chromium
TMAH	tetramethylammonium hydroxide
NMP	n-methylpyrrolidone
BD	dielectric breakdown
E_{BD}	dielectric breakdown strength
RVS	ramped voltage stress
e-beam	electron beam
3D	three-dimensional
SEM	scanning electron microscope
SPA	semiconductor parameter analyzer
I-V	current-voltage
V_{BD}	breakdown voltage
$T_{h\text{-}BN}$	thickness of h-BN
PLA	polylactic acid
CH_2Cl_2	Methylene Chloride
TE	top electrode

Ta	tantalum
TaOx	tantalum oxide
TiN	titanium nitride
H_2O_2	hydrogen peroxide
I-t	current-time
SMU	Source-measure unit
GND	ground
V_{ds}	source-drain voltage
V_g	gate voltage
I_{ds}	source-drain current
S	source
D	drain