Design and implementation of high-level multilevel inverters: focusing on 15-level, 25-level, and 33-level topologies with asymmetrical configuration and optimal component choices

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DOCTORAL THESIS

Design and Implementation of High-Level Multilevel Inverters: Focusing on 15-level, 25-level, and 33-level Topologies with Asymmetrical Configuration and Optimal Component Choices

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“Replacing traditional energy sources completely with renewable energy will be a challenging task. However, by adding renewable energy to the grid and gradually increasing its contribution, we can realistically expect a future powered completely by green energy.″

Tulsi Tant

Preface

The rapid evolution of renewable energy technologies has underscored the necessity for innovative solutions to enhance efficiency and reduce costs. This study introduces a novel topology for a single-phase 15-level asymmetric multilevel inverter (MLI), which is extended to a 25-level and 33-level variant. By optimizing the design to use fewer semiconductor switches, the proposed topology addresses the cost and size issues and significantly improves the inverter's reliability and efficiency. This research aims to contribute to the growing field of photovoltaic systems by offering a solution that minimizes total harmonic distortion (THD) and maximizes output voltage levels, ensuring better performance in grid-connected applications.

- ## Thesis Objective

The primary objective of the PV system is to generate active power. Intelligent control of PV systems can address many power quality issues and enhance overall system performance. This is achieved through the use of multifunctional inverters in solar PV systems. Multilevel inverter technology is crucial in solar-based renewable energy systems. The utilization factor of the PV system is significantly improved when the multifunctional capabilities of the inverter are leveraged. Renewable energy systems (RES) must be highly efficient and safe for secure and reliable grid interconnections. Consequently, next-generation solar PV systems must integrate more excellent controllability by providing ancillary services. Inverters that offer these services are known as multifunctional inverters. Therefore, a comprehensive study of multifunctional inverters with various control methods is necessary. The primary objectives of this thesis are as follows:

- We present a novel topology for a single-phase 15-level asymmetric multilevel inverter (MLI) to minimize component requirements.
- To develop a 25-level variant suitable for renewable energy applications, effectively reducing system costs and size by enhancing the initial 15-level MLI structure.
- To mitigate voltage stress through asymmetrical configuration and optimal component choices by designing a 33-level MLI.

- ## Thesis Outline

Chapter 1 provides an overview of renewable energy resources in multilevel inverters, discussing their types, topologies, advantages, and disadvantages. Chapter 2 reviews previous work on multilevel inverters, identifies research gaps, and sets research objectives—chapter 3 details power quality enhancement in grid-integrated photovoltaic systems using hybrid techniques, with results and comparisons. Chapter 4 covers energy management of grid-connected hybrid solar/wind/battery systems using optimization techniques, including results and comparisons. Chapter 5 uses optimization methods to examine fault analysis in grid-connected wind energy, with results and comparisons. Chapter 6 analyzes 15-level and 25-level multilevel inverter topologies for photovoltaic applications, focusing on low THD and providing result analysis. Chapter 7 details the design and analysis of 33-level MLI topologies for photovoltaic applications, emphasizing low THD and providing result analysis. Chapter 8 concludes the thesis and discusses future research directions.

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Abstract

The primary goal of this thesis is to establish multilevel inverter (MLI) topologies for industrial settings. Because of its numerous benefits, including low power dissipation on power supplies and low harmonic contents, MLI topologies are utilized in medium- and high-power applications, such as active power filters, FACTS devices, and machine currents. The chosen switching strategies are crucial in removing harmonic distortion from the output voltage provided by the MLI. Depending on the inverter's power requirements, different topologies and control strategies may be selected. However, they have several drawbacks over MLI, such as the need for separate power sources for each stage. Consequently, MATLAB/SIMULINK is used to simulate MLI.

This work aims to offer a unique topology for a single-phase 15-level asymmetric MLI to minimize component requirements. The suggested design uses asymmetric DC sources to reach a maximum 15-level output voltage through an H-bridge topology. To enable a 25-level version appropriate for renewable energy applications, the original 15-level MLI structure is further improved, lowering system costs and dimensions. However, the higher component count in MLI presents reliability issues, particularly about the decrease of total harmonic distortion, which continues to be a research focus. Several factors are examined for the proposed 15-level- and the extended 25-level MLI, including total standing voltage, multilayer inverter cost function, and power loss. Next, it facilitates the integration of renewable energy sources and streamlines the use of components by contributing to a novel topology for 15-level asymmetric MLI. Even though multilevel inverters have many benefits, future developments in this field must address reliability issues related to overall harmonic distortion reduction. Then, a unique 33-level asymmetrical single-phase MLI is built, utilizing fewer components and a lower Total Standing Voltage (TSV) at the switches. Variable-rated switches are employed to lower the overall cost of the inverter, and the distribution of stress among the switches is carefully examined. The suggested design combines four asymmetrical DC sources with twelve switches to generate 33 voltage output levels. The inverter's performance is determined by many crucial factors, including TSV, efficiency, power loss, and cost function (CF). Using a range of combinational loads, the MLI was evaluated in dynamic load conditions with unforeseen load disturbances, and it was discovered to be stable throughout the operation. A thorough comparison uses graphical representations based on stress

across switches, stress distribution, switch count, DC source count, gate driver circuits, component count factor, TSV, CF, and other existing topologies. It is demonstrated to be more efficient and better in every way. According to simulation and experiments, the Total Harmonic Distortion (THD) is within IEEE guidelines. The suggested framework was created in MATLAB/Simulink and tested using hardware in a lab environment.

Resumen

El objetivo principal de esta tesis es establecer topologías de inversores multinivel (MLI) para su uso en entornos industriales. Debido a sus numerosos beneficios, incluida la baja disipación de potencia y el bajo contenido de armónicos, las topologías MLI se utilizan en aplicaciones de potencia media y alta, como filtros de potencia activos, dispositivos FACTS y drivers de máquinas eléctricas. Las estrategias de conmutación elegidas son cruciales para eliminar la distorsión armónica en el voltaje de salida proporcionado por el MLI. Dependiendo de los requisitos de potencia del inversor, se pueden elegir diferentes topologías y estrategias de control. Sin embargo, los inversores multinivel tienen el inconveniente de la necesidad de fuentes de energía independientes para sus etapas. En consecuencia, se utiliza MATLAB/SIMULINK para simular el comportamiento completo de los MLI propuestos.

El objetivo de este trabajo es ofrecer una topología única para un MLI asimétrico monofásico de 15 niveles con el objetivo de minimizar los requisitos de componentes. El diseño sugerido utiliza fuentes de CC asimétricas para alcanzar un voltaje de salida máximo de 15 niveles mediante el uso de una topología de puente H. Para permitir una versión de 25 niveles apropiada para aplicaciones de energía renovable, la estructura MLI original de 15 niveles se mejora aún más, reduciendo así los costos y las dimensiones del sistema. Sin embargo, el mayor número de componentes en MLI presenta problemas de fiabilidad, particularmente con respecto a la disminución de la distorsión armónica total, que continúa siendo un foco de investigación. Para el MLI propuesto de 15 niveles y el extendido de 25 niveles, se examinan una serie de factores, incluido el voltaje permanente total, la función de costo del inversor multinivel y las pérdidas energéticas. A continuación, facilita la integración de fuentes de energía renovables y agiliza el uso de componentes al contribuir a una topología novedosa para MLI asimétrica de 15 niveles. Aunque los inversores multinivel tienen muchos beneficios, los desarrollos futuros en este campo deben abordar cuestiones de confiabilidad relacionadas con la reducción general de la distorsión armónica. Luego, se propone un MLI monofásico asimétrico exclusivo de 33 niveles, que utiliza menos componentes y un voltaje permanente total (TSV) más bajo en los interruptores. Para reducir el costo total del inversor, se emplean interruptores de clasificación variable y se examina cuidadosamente la distribución de tensión entre los interruptores. El diseño sugerido combina cuatro fuentes de CC asimétricas con doce interruptores para generar 33 niveles de salida de voltaje. El rendimiento del inversor está determinado por una serie de factores cruciales, incluidos

TSV, eficiencia, pérdidas de potencia y función de costo (CF). Utilizando una variedad de cargas combinadas, el MLI se evaluó en condiciones de carga dinámica con perturbaciones de carga imprevistas y se descubrió que era estable durante toda la operación. Se realiza una comparación exhaustiva basada en la tensión entre los interruptores, la distribución de la tensión, el recuento de interruptores, el recuento de fuentes de CC, los circuitos de controlador de puerta, el factor de recuento de componentes, TSV, CF y otras topologías existentes. Está demostrado que es más eficiente y mejor en todos los sentidos. Según la simulación y los experimentos, la distorsión armónica total (THD) se encuentra dentro de las pautas del IEEE. El marco sugerido se creó en MATLAB/SIMULINK y se puso a prueba utilizando hardware en un entorno de laboratorio.

Resum

L'objectiu principal d'aquesta tesi és establir topologies d'inversors multinivell (MLI) per utilitzar-los en entorns industrials. A causa dels seus nombrosos beneficis, inclosa la baixa dissipació de potència i el baix contingut d'harmònics, les topologies MLI s'utilitzen en aplicacions de potència mitjana i alta, com ara filtres de potència actius, dispositius FACTS i *drivers* de màquines elèctriques. Les estratègies de commutació triades són crucials per eliminar la distorsió harmònica al voltatge de sortida proporcionat pel MLI. Depenent dels requisits de potència de l'inversor, es poden triar diferents topologies i estratègies de control. Tot i això, els inversors multinivell tenen l'inconvenient de la necessitat de fonts d'energia independents per a les seves etapes. En conseqüència, es fa servir MATLAB/SIMULINK per simular el comportament complet dels MLI proposats.

L´objectiu d´aquest treball és oferir una topologia única per a un MLI asimètric monofàsic de 15 nivells amb l´objectiu de minimitzar els requisits de components. El disseny suggerit utilitza fonts de CC asimètriques per assolir un voltatge de sortida màxim de 15 nivells mitjançant l'ús duna topologia de pont H. Per permetre una versió de 25 nivells apropiada per aplicacions d'energia renovable, l'estructura MLI original de 15 nivells es millora encara més, reduint així els costos i les dimensions del sistema. No obstant això, el nombre més gran de components en MLI presenta problemes de fiabilitat, particularment pel que fa a la disminució de la distorsió harmònica total, que continua sent un focus de recerca. Per al MLI proposat de 15 nivells i l'estès de 25 nivells, s'examinen una sèrie de factors, inclòs el voltatge permanent total, la funció de cost de l'inversor multinivell i les pèrdues energètiques. A continuació, facilita la integració de fonts d'energia renovables i agilitza l'ús de components en contribuir a una nova topologia per a MLI asimètrica de 15 nivells. Tot i que els inversors multinivell tenen molts beneficis, els desenvolupaments futurs en aquest camp han d'abordar qüestions de confiança relacionades amb la reducció general de la distorsió harmònica. Després, es proposa un MLI monofàsic asimètric exclusiu de 33 nivells, que utilitza menys components i un voltatge permanent total (TSV) més baix als interruptors. Per reduir el cost total de l'inversor, es fan servir interruptors de classificació variable i s'examina amb cura la distribució de tensió entre els interruptors. El disseny suggerit combina quatre fonts de CC asimètriques amb dotze interruptors per generar 33 nivells de sortida de voltatge. El rendiment de l'inversor està determinat per una sèrie de factors crucials, inclosos TSV, eficiència, pèrdues de potència i funció de cost (CF). Utilitzant una varietat de càrregues combinades, l'MLI es va avaluar

en condicions de càrrega dinàmica amb pertorbacions de càrrega imprevistes i es va descobrir que era estable durant tota l'operació. Es fa una comparació exhaustiva basada en la tensió entre els interruptors, la distribució de la tensió, el recompte d'interruptors, el recompte de fonts de CC, els circuits de controlador de porta, el factor de recompte de components, TSV, CF i altres topologies existents. Està demostrat que és més eficient i millor en tots els sentits. Segons la simulació i els experiments, la distorsió harmònica total (THD) és dins de les pautes de l'IEEE. El marc suggerit es va crear a MATLAB/SIMULINK i es va posar a prova utilitzant maquinari en un entorn de laboratori.

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LIST OF ABBREVIATIONS

ATSFRBFNN	Adaptive TS-Fuzzy-based RBF Neural Network
BESS	Battery Energy Storage System
BN	Bayesian Network
CF	Cost Factor
CM	Common-mode
DSP	Digital Signal Processor
EMC	Electromagnetic Compatibility
EV	Electric Vehicles
FC	Fuel Cells
GCPVS	Grid-connected PV System
GWO	Grey Wolf Optimisation
IBatMFOA	Improved Bat search Algorithm with Moth Flame Optimisation Algorithm
IC	Incremental Conductance
IH	Induction Heating
IVRI	Impedance-Voltage Rise Index
MFGCI	Multi-Functional Grid-Connected Inverters
MG	Micro Grid
MLI	Multilevel Inverter
ML-MFGCI	Multilevel Multifunctional Grid-Connected Inverters
MPPT	Maximum Power Point Tracking
MPSO	Modified Particle Swarm Optimization
NGPC	Non-linear Generalized Predictive Control
PCC	Point Of Common Coupling
PI	Proportional-Integral
PIR	Proportional-Integral Resonance

PLD	Programmable Logic Device
PMS	Power Management System
PQ	Power Quality
PSC	Partial Shading Conditions
PV	Photo-Voltaic
PWM	Pulse-Width Modulation
RES	Renewable Energy Systems
RPM	Reduced Power Mode
SiC	Silicon Carbide
SPRPC	Single Point Reactive Power Control
SRFT	Synchronous Reference Frame Theory
STATCOM	Static Synchronous Compensator
SVPWM	Space Vector Pulse Width Modulation
THD	Total Harmonic Distortion
TSC	Thyristor-Switched Capacitor
TSV	Total Standing Voltage
VCS	Viral Colony Search
VS	Variable-Step
VS-PO	Variable Step Perturb & Observe
VSS-RLMLS	Variable Step Size Robust Least Mean Logarithmic Square-Based Control Scheme
ZSI	Z-source Inverter

Chapter 1

Introduction to Multilevel Inverters and Renewable Energy Integration

This chapter gives a brief overview of the renewable energy resources available and introduces the cascaded H bridge multi-level inverter, which is one of the topics of this thesis. The main objective of a multilevel inverter is to reduce the THD in the operating system. This is usually achieved by increasing the number of DC sources and switching them. However, this method will increase the power losses. That is why the new topology will try to reduce the component without lowering the quality output of the converter. Due to a multilevel inverter's stepped output waveform characteristic, the Total Harmonic Distortion (THD) content is low compared to the conventional two-level inverters [1]. The present project studies and analyzes three-phase multilevel inverters and their different topologies and configurations. The primary purpose of our research is to study the modulation techniques and compare them with each other, analyzing their advantages and disadvantages. Their applications have been analyzed according to their functioning, such as the cascaded inverter, which could also serve as a rectifier/charger for the batteries of an electric vehicle. In contrast, the car was connected to an AC supply. One first impression of a multilevel power converter is that many switches may lead to complex Pulse-Width Modulation (PWM) switching algorithms. However, early developments in this area demonstrated the relatively straightforward nature of multilevel PWM. Our project presents the fundamental methods and reviews some novel research. The methods are divided into the traditional voltage source and current-regulated methods. Some discrete current-regulated methods are presented herein, but due to their nature, the harmonic performance is not as good as that of voltage-source methods. Voltage-source methods also more easily lend themselves to Digital Signal Processor (DSP) or Programmable Logic Device (PLD) implementation. Although we have discussed numerous topologies and modulation methods, several more can be found. Another goal of this project is to introduce concepts related to reducing the number of isolated voltage sources

and sensors. This can be important in the high-power quality cascaded multilevel inverters, which require several voltage sources and knowledge of the DC voltage levels.

1.1. Overview

Numerous industrial applications have begun to require higher power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and megawatt power levels. It is troublesome for a medium voltage grid to directly connect only one power semiconductor switch. As a result, a multilevel power converter structure has been introduced as an alternative in high-power and medium-voltage situations. A multilevel converter not only achieves high power ratings but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced with a multilevel converter system for a high-power application. The concept of multilevel converters has been introduced since 1975. The term multilevel began with the three-level converter. Subsequently, several multilevel converter topologies have been developed. However, the elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage DC sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as multiple DC voltage sources. The commutation of the power switches aggregates these various DC sources to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the DC voltage sources to which they are connected [2].

The converters must be designed to obtain a quality output voltage or a current waveform with a minimum amount of ripple content. In high power and high voltage applications, the conventional two-level inverters have some limitations in operating at high frequency, mainly due to switching losses and constraints of the power device ratings: series and parallel combination of power switches to achieve the power handling voltages and currents. Conventional two-level inverters produce THD levels of around sixty percent even under normal operating conditions, which are undesirable and cause more losses and other power quality problems on AC drives and utilities. Two or more power switches can be connected in series for high-voltage applications to provide the desired voltage rating. However, the characteristics of devices of the same type are not identical. For the same OFF-state current, their OFF-state voltages differ. Even during the turn-off

of the switches, the variations in stored charges cause differences in the reverse voltage sharing. The switch with the least recovered charge faces the highest transient voltage. For higher current handling, the switches are connected in parallel; however, because of uneven switch characteristics, the load current is not shared equally. If a power switch carries more current than the others, its power dissipation increases, increasing the junction temperature and decreasing the internal resistance [3]. This, in turn, increases its current sharing and may damage the devices permanently, which is undesirable for critical applications.

1.2. Motivation

From a technical and scientific perspective, there is an urgent need to develop new technologies that can offer greater conversion efficiencies at a lower production cost, as this will improve the entry of solar technologies into the energy market. Several studies have been dedicated to solving these problems for better reliability, performance, and competitiveness of solar-based energy technologies. PV cells are used in solar-based technologies to convert solar energy into electrical energy. Various control techniques, power converter topologies, and power tracking methods have been developed to harvest power from renewable energy sources efficiently. Yet, more studies are still focusing on integrating renewable energy sources into the power grid for better efficiency. In this regard, more attention is given to power converters and their controls owing to their vital role in power conversion and output power regulation from these resources. The importance and the development of a modified multilevel inverter are also highlighted in this review. In general, this paper focuses on utilizing multilevel inverters for PV systems to motivate and guide society to focus on inventing an efficient and economical multilevel inverter with the combined capabilities of these converters reported in the literature [4].

1.3. Multilevel Modulation

This chapter presents the fundamental methods of PWM. The methods are divided into the traditional voltage-source and current-regulated methods. An advantage of the current-regulated techniques is the need to control the current directly since the higher-level control (vector control, reactive power control, active rectifier, etc.) nearly always outputs commanded currents. However, current controls typically depend on event scheduling and are analog implementations that can only be reliably operated up to a certain power level. Some discrete current-regulated methods are

presented herein, but due to their nature, the harmonic performance is not as good as that of voltage-source methods [5].

1.4. Multi-Level Inverter and its Types

1.4.1. 3-level Inverter

Compared to two-level inverters, three-level inverters have smaller output voltage steps that mitigate motor issues due to long power cables between the inverter and the motor. These issues include surge voltages and rate of voltage rise at the motor terminals and motor shaft bearing currents. The three-level inverter has many switching states compared to a two-level inverter. In the proposed scheme, a three-level space vector PWM inverter is easily implemented as a conventional two-level space vector PWM inverter. Therefore, the proposed method can also be applied to multilevel inverters [6].

1.4.2. 5-level Inverter

This topology consists of a full-bridge inverter, an auxiliary circuit (comprised of one switching element and four diodes), and two capacitors as voltage dividers. The multilevel inverter is connected after the DC power supply. The main point of the auxiliary circuit is to generate half-level DC supply voltage. It also reduced the layout complexity compared to other multilevel inverter topologies, such as flying-capacitor topology, diode-clamped topology, and hybrid topology, and these topologies can be studied in various papers. Five level Single Phase flying capacitor inverter Advantages (i) Controlling of real and reactive power flow is possible (ii) Does not require any clamping diodes (iii) No transformer is required for achieving the required number of voltage levels [5] (iv) Balancing capacitor share single DC source.

1.4.3. 7-level Inverter

The topology of the 7-level inverter is similar to the 5-level topology, but only the auxiliary circuit was added with an additional circuit. Generally, a 7-level inverter consists of a full bridge inverter, two bidirectional switches (the auxiliary circuit), and three capacitors as voltage dividers, illustrated in Figure 2. To ensure that the power flows from the PV arrays to the grid, high DC bus voltages are necessary. The LCL filter filters the current to be injected into the utility grid. Seven output voltage levels can be achieved when the switching signal for the IGBTs in the topology is done correctly. Though the multilevel inverters hold attractive features, using more switches in the conventional configuration limits its wide range of applications. Therefore, a renewed 7-level

multilevel inverter topology is introduced, incorporating the most miniature unidirectional switches and gate trigger circuitry, ensuring minimum switching losses and reducing size and installation cost. The new topology is well-suited for drives and renewable energy applications [7]. The performance quality of THD and switching losses of the new MLI are compared with conventional cascaded MLI and other 7-level reduced switch topologies using carrier-based PWM techniques.

1.4.4. 9-level Inverter

For the 9-level inverter, we use four h-bridge inverters in each phase. The main advantage of PWM is that power loss in the switching devices is shallow. When a switch is off, there is practically no current, and when it is on, and power is being transferred to the load, there is almost no voltage drop across the switch. The conventional inverter has multiple sources; 16 switches and more voltage sources are required. This inverter requires a single solar panel, fewer switches, and an integrated boost converter, which increases the inverter's input voltage. It uses seven switches to produce a level output stepped waveform. The work aims to produce nine 9-level waveforms using solar and boost converters [8].

1.4.5. 15-level Inverter

In this inverter, the DC source magnitude is unequal. The DC source magnitudes are designed with binary voltage forms such as 3V, 6V, and 12V. Here the output voltage is 15 level and they are 21V, 18V, 15V, 12V, 9V, 6V, 3V, 0V,-3V,-6V,-9V,-12V,-15V,-18V and -21V respectively. Reducing the switch count and stress on the power electronic switches while maintaining a sinusoidal stepped output remains challenging. This work proposes A multilevel inverter topology that utilizes twelve switches and four DC voltage sources to produce a 15-level staircase output voltage waveform. The objective is to reduce the harmonic in the output voltage, reduce the filter requirement cost, and maintain high efficiency throughout the operating range [9].

1.4.6. 25-level Inverter

Researchers have developed numerous inverters with various topologies for high efficiency and reliability. These inverters can be used in applications requiring medium and high power. Multilevel inverters provide the right solution for the PV system to achieve high performance of renewable energy generation. This suggested setup had twelve standalone solar PV arrays and a 25-level H-bridge multilevel inverter. A cascading system with sinusoidal PWM control is advised

to achieve various voltage levels on the inverter's output side. A novel 25-level single-phase asymmetrical multilevel inverter topology with a reduced device count is designed. The proposed MLI architecture produces a maximum of 25 output voltage levels without H-bridge utilizing asymmetrical DC sources and can be used for grid-connected renewable sources. This topology reduces the total components, cost, and system size. Despite various MLI advantages, the reduced component count topology reduces a THD value, making the system more reliable [10].

1.4.7. 33-level Inverter

At the 33-level, the value of DC sources is selected as a 1:2:4:8 ratio. The proposed basic units are used as building blocks to form a cascaded multilevel inverter, i.e., the proposed topology consists of cascaded basic units, and it uses a lower number of switching devices and gate driver circuits. The design of the proposed topology consists of two main parameters: the number of cascaded basic units and the number of DC sources in each basic unit. These two parameters can be used to design the desired multilevel inverter based on the operational conditions. Therefore, the proposed topology offers good flexibility in designing. The comparison results with some recently introduced topologies showed that the proposed topology effectively reduces the component count. The simulation results obtained in MATLAB /SIMULINK and the experimental results of a 31-level inverter are presented and verified in their performance [11].

1.5. Advantages and Disadvantages

A multilevel converter has several advantages over a conventional two-level converter that uses high switching frequency PWM. The attractive features of a multilevel converter can be briefly summarized as follows.

- Staircase waveform quality: Multilevel converters can generate the output voltages with very low distortion and reduce the dv/dt stresses, reducing Electromagnetic Compatibility (EMC) problems.
- Common-mode (CM) voltage: Multilevel converters produce smaller CM voltage; therefore, the stress in a motor's bearings connected to a multilevel motor drive can be reduced. Furthermore, CM voltage can be eliminated by using advanced modulation strategies
- Input current: Multilevel converters can draw input current with low distortion.

- Switching frequency: Multilevel converters can operate at fundamental and high switching frequency PWM. Lower switching frequency usually means lower switching loss and higher efficiency.

Unfortunately, multilevel converters do have some disadvantages. One particular disadvantage is the need for more power semiconductor switches. Although lower voltage-rated switches can be utilized in a multilevel converter, each switch requires a related gate drive circuit. This may cause the overall system to be more expensive and complex. Plentiful multilevel converter topologies have been proposed during the last two decades. Contemporary research has engaged novel converter topologies and unique modulation schemes. One of the most critical problems in controlling a multilevel voltage source inverter is to obtain a variable amplitude and frequency sinusoidal output by employing simple control techniques. Indeed, in voltage source inverters, non-fundamental current harmonics cause power losses, electromagnetic interference, and pulsating torques in AC motor drives. The harmonic reduction can then be strictly related to the performance of an inverter with any switching strategy. Various Pulse Width Modulation control schemes have been developed in multilevel voltage source inverters.

1.6. Pulse Generation

The Pulse Generator block generates square wave pulses at regular intervals, shown in Figure 1.1, and displays the Source Block Parameters for P2 in a simulation environment, likely Simulink. The parameters specify a time-based pulse type with the simulation time used for the time parameter (t). The amplitude is denoted by 'a', and the period is indicated by 'p'. The pulse width is one-third of the period (130/3 %), and the phase delay is 1/1500 seconds. The checkbox for interpreting vector parameters as 1-D is selected, indicating that the input vector will be processed as a one-dimensional array. These settings are crucial for defining the characteristics and timing of the pulse signal within the simulation. The block waveform parameters, Amplitude, Pulse Width, Period, and Phase delay determine the shape of the output waveform. The Pulse Generator can emit scalar, vector, or matrix signals of any data type [12]. They use scalars to specify the waveform parameters to cause the block to emit a scalar signal. To cause the block to emit a vector or matrix signal, use vectors or matrices, respectively, to specify the waveform parameters. Each waveform parameter element affects the output signal's corresponding element. For example, the first element of a vector amplitude parameter determines the amplitude of the

first element of a vector output pulse. All the waveform parameters must have the exact dimensions after scalar expansion. The data type of the output is the same as the data type of the Amplitude parameter.

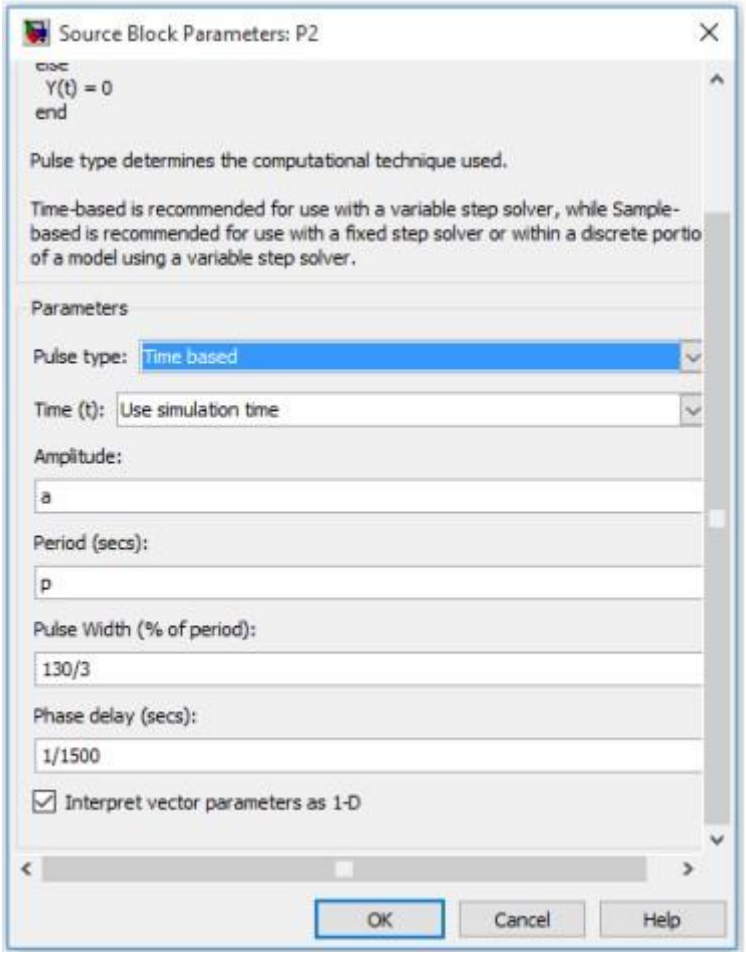

Figure 1.1 Pulse generator parameter dialogue box

1.7. Multilevel Inverters in Renewable Energy System Applications

Due to the MLI's capabilities of producing high-quality voltage waveforms through low switching frequency operation, they are thus preferred for high and medium power applications. MLIs have been widely used in various applications such as power supplies applications; Renewable Energy Systems (RESs) such as PV systems, wind energy conversion systems (WECS) and Fuel Cells (FC); Electric Vehicles (EV); Induction Heating (IH) and numerous other fields. Many MLI topologies have been integrated with RESs in grid-connected systems to add the power

generated by the RESs to the grid [13]. Much attention has been given to PV-based power generation due to its numerous advantages, such as ease of allocation, longer life, absence of noise, lack of pollution, lesser installation time, high mobility and components' portability, and ability to produce power output that can meet peak load requirements. Hence, PV arrays have found many industrial applications, such as battery recharging systems, solar hybrid vehicles, satellite power systems, solar-based water-pumping machines, etc. For this reason, many countries are investing heavily in renewable energy-based projects. However, specific problems are associated with PV generation systems, such as low conversion efficiency and interference from climate conditions. The power of PV cells is directly a function of the solar intensity/radiation but depends less on the temperature. A complete PV system comprises solar panels, batteries, DC-DC voltage converters, and controllers. The work of the DC-DC voltage converters is to match the load characteristics with the characteristics of the solar panels. DC-DC voltage converters have three categories: boost, buck, and buck-boost converters. The expected voltage level determines the section of the appropriate form of DC-DC voltage converter. Batteries are used to make the PV systems act as the natural feeder source so that it is possible to achieve constant voltage levels corresponding to different loads. Another battery saves power and provides temporary compensation for power fluctuations. A solar panel is made up of several PV cells that are connected either in series or parallel or as series-parallel external connections.

1.8. Total Harmonic Distortion

When a signal passes through a non-ideal, non-linear device, additional content is added at the harmonics of the original frequencies. THD is a measurement of the extent of that distortion. When the primary performance criterion is the ″purity″ of the original sine wave, the measurement is most commonly defined as the ratio of the RMS amplitude of a set of higher harmonic frequencies to the RMS amplitude of the first harmonic, or fundamental, frequency. In a multilevel inverter, THD analysis is performed on both voltage and current [14].

1.9. Renewable Energy Resources

A study of renewable energy resources is presented in [15]. Fossil fuel-based technologies have advanced our quality of life based on fossil fuels. The use of fossil fuels in our day-to-day lives comes at a very high price. The use of fossil fuels must be controlled, and the usage of renewable energy resources has to be increased to save fossil fuels – oil, natural gas, and coal - for the future

and reduce the cost to the middle class. The usage of renewable energy resources will also minimize global warming. The empowerment of every energy user in a new energy economy based on two renewable sources is to make them an energy manager by conserving energy, reducing carbon footprints, and installing distributed renewable energy sources. To meet the carbon reduction targets, it is essential to use renewable and sustainable energy sources. There is a need to replace the traditional fossil fuel-based vehicles with electric cars and the stationary power from conventional fuels, coal, gas, and oil, with green sources for sustainable energy fuel for the future.

1.9.1. Solar and Photovoltaic

With today's increasing demand for electricity, loss reduction, efficiency enhancement, and making the grid environment-friendly are necessities. Electricity must be generated, dispersed, and distributed in real-time. It is required to manage demand and provide it in real time while ensuring stability and power quality to consumers. Innovative distribution is distributing energy more smartly. RES are small power resources, like solar photovoltaic, cogeneration systems, wind turbines, microturbines, backup generators, and energy storage devices, which will be aggregated to satisfy regular demands [16]. It provides energy wherever it is needed. It also provides a cheaper and faster option than massive structured power plants. RES like wind and photovoltaic (PV) are substantially used for power generation as an alternative to conventional ones. In the current global scenario, PV features a greater installed capacity than the other RES, like hydro and wind. PV generation has become the rising star of this pack because of its versatility. It is often implemented with little or no upfront costs, e.g., small solar home systems or sizeable solar energy plants are often developed to get MWs of power. In contrast with wind or tidal generation, PV is often deployed globally, albeit with varying potentials. These merits have made PV the renewable energy technology with the highest installed capacity in the world. Consequently, the interest in analysis within the space of grid-tied electrical solar power conversion systems is growing exponentially. A primary goal of those converters is to increase the ability to deliver to the grid by adequately following the utmost point of the PV panel, reducing losses and harmonic distortion while providing high dependableness. Power conversion systems are planned to interface the PV generators with the grid. The four main topologies are square measure centralized topology, string, multi-string, and module topology. These days, centralized topology is thought obsolete, whereas a growing interest has been shown in string and multi-string topology because of its increased MPPT capability and inherent modularity. One rising answer for high- or medium-voltage

transformer-less power conversion is represented by multilevel converters as interfaces for grid-connected PV systems. Solar energy is a significant renewable energy source. The heat energy from the sun - solar thermal energy – can heat water 3 to a high temperature and be pressurized conventionally to run a turbine generator. Solar PV sources are arrays of cells of silicon materials that convert solar radiation into direct current electricity. A crystalline silicon wafer costs very high, but new light-absorbent materials have significantly reduced the cost. The manufacture of PV cells is based on two different types of material:

- a semiconductor material that absorbs light and converts it into electron-hole pairs, and 4.
- a semiconductor material with junctions that separate photo-generated carriers into electrons and electron holes.

1.9.2. Grid-Connected PV system

The former account for more than 99% of the total installed capacity among grid-connected PV systems and stand-alone PV systems. As there is no need for a battery in the grid-connected system, all generated power is transferred to either a connected load or grid. Therefore, the generated solar power reduces the consumption of fossil fuels based on other energy sources supplying the grid, whose savings act as energy storage for the future. The grid-connected system has more reliability, less maintenance, and scalability of future expansion. Environmental awareness, technological development, incentives, and regulations will unleash the sun's power. Due to constant reductions in the prices of the PV system, manufacturers of the inverter are competing more profoundly. Inverters are now obtained with less weight, smaller size, and less cost [17]. There are two ways of reducing the size of inverters; one is through the use of Silicon Carbide (SiC) in switching devices, which increases the switching frequency and, hence, reduces the size of the inductors. Nevertheless, the SiC power devices technology is in the initial stage. Therefore, these devices' prices are higher than conventional silicon devices, and their applications are also limited. Another way is the use of multilevel inverter technologies, which decrease the losses and voltage rating of devices and reduce the size of the inductor, the requirement of the cooling systems, and increases the switching frequency, thus reducing the size of an entire PV system.

1.9.3. A brief review of Multilevel grid-connected inverters

Continuous development of higher-voltage and higher-current power semiconductor devices is ongoing for grid-connected distributed generation systems. But there is hues competition between

the new converter topologies with medium-voltage devices and traditional power converter topologies configuration with high-voltage semiconductors while maintaining traditional converter topologies (mainly two-level voltage and current source inverters), and by developing new converter topologies with conventional semiconductor technology, known as multilevel inverters. The latter method has the advantage of familiar circuit configuration and ease of control. New semiconductors are also more expensive, and they opt for higher-power technologies. Along with this, other power-quality standards also need to be satisfied. Also, there are some additional requirements like filters. Hence, choosing a new converter topology like a multilevel inverter is better. Therefore, using a multilevel converter is not a challenging issue, as many such topologies are proposed in various kinds of literature. Multilevel inverters were first introduced by Nabe et al. in 1975 and have become very popular in grid-connected renewable sources, FACTS devices, and all medium voltage drives. Multilevel inverters offer a better-quality output voltage waveform than two-level inverters but need many switches and additional gate driver circuits, making the system more complicated and less reliable. These drawbacks inspired researchers to develop new inverter topologies presented by authors in references [18], like a reduced switch inverter, asymmetric inverters, hybrid inverters, etc., for multifunctional grid-connected applications in RES.

1.9.3.1. Control of grid-connected inverter by PQ Theory

This type of control uses Clark transformation sensed grid voltage, and load currents are transformed into the stationary α-β frame. PR controllers are used in these types of control because time-varying quantizes like grid current impose steady-state error if controllers are used. Lower-order harmonics compensator implementation is easy in this controller type and can be applied without affecting controller dynamics. To obtain the best performance of the PR controller, the controller frequency has to be identical to the grid frequency. Therefore, an adaptive adjustment of the controller frequency is necessary if grid frequency variations are encountered in the utility network. Lower-order harmonics compensation is easy with the controller, but this computational burden increases with this compensator for higher-order harmonics compensation. An excellent dynamic response is seen in this type of control. Implementation in hardware is complex with this type of control. Power factor controls are not entirely possible in this method. Also, the phase angle of the grid voltage is not essential; only the filtered grid voltage is required to generate the current. However, the theory uses voltage signals to compute instantaneous active and reactive

powers. Any distortion and unbalance in voltage will lead to the inaccurate calculation of reference source currents, which should contain only the actual fundamental frequency component of the load current.

1.9.3.2. Control of grid-connected inverter by DQ Theory

This control park transformation transforms the control variable into a synchronously rotating reference frame. As a result of this, the control variables become dc quantities. In this control structure, it is necessary to know the exact phase angle of grid voltage to perform the accurate transformation. Commonly, Proportional-Integral (PI) controllers are associated with this control. The synchronous reference frame control structure involves cross-coupling and feed-forward of the grid voltages. Hence, during grid voltage fluctuation, the dynamics of this controller become high, and any change in grid voltage amplitude changes the d- and q-axis components of the voltage, resulting in a fast response of the control system. Easy hardware implementation with reasonable current control and good dynamic response is possible with this controller. Poor harmonic compensation for lower-order harmonics is seen in this controller compared to p-q control [19]. The steady-state error is also not eliminated. A delay in response is also there, and this delay is due to the filter used to filter signals in the d–q frame for extraction of the reference current waveform. Generating voltage templates (sine and cosine) is also essential in calculating reference source currents.

1.10. Challenges and Future Research

Renewable energy systems have gained more application in the power grid due to the advancements in power electronics devices and related technologies. However, this has generated many concerns regarding power quality, protection, energy storage, the intermittent nature of the grid fed to the grid, and system reliability. Hence, several standards and codes have been developed for grid-interfaced RESs to ensure the power quality at the grid is maintained [20]. Given the reviewed literature, there are areas in this regard that demand more studies; these are highlighted as follows:

- The intermittent nature of the power produced by RESs remains one of the major issues in grid-connected RESs. It is believed that RESs's contribution to the global energy market will increase in the future; hence, this problem of power fluctuations in grid-connected RESs demands to be addressed.

- MLIs have been widely used in grid-connected and industrial applications over time due to their numerous advantages. However, researchers have recently begun to introduce hybrid topologies, which are developed from classical topologies; these hybrid methods are developed to meet high grid code standards and address power quality problems in a cost-friendly manner. Since most of these new topologies have not been evaluated in grid-connected RESs, there is a need to investigate their performance in grid-integrated applications.
- More studies are needed on the performance analysis of the recent MLIs to address the issues encountered in the grid-connected RES applications efficiently. Studies should also focus on the role of MLIs in innovative grid technologies.
- The efficiency of the Maximum Power Point Tracking (MPPT) algorithm is affected by many factors, but the most obvious are the nonlinear nature of the PV system, the system's working conditions, and the variations in ambient conditions. Most often, the algorithm developers do not consider these changes, and this has been the source of system failure in certain working conditions. Thus, designing the PV module controller is a tedious task that demands more attention to achieve stability.
- It is imperative to evaluate the performance of these novel topologies in grid-integrated applications, as the majority of them have not yet been examined in the context of grid-connected RESs.
- MLI control and modulation systems should be more robust, flexible, and fault tolerant.
- In recent times, researchers and industries have begun developing hybrid topologies to address power quality challenges successfully and meet demanding grid standards cost-efficiently.
- More research is needed on quantitative approaches for solving MLI nonlinear systems.
- New voltage balancing techniques must be employed in MLIs to minimize capacitor size and increase inverter power density.
- Resonant converters with single DC source MLIs are suggested.
- Smart grid systems must include the integration of microgrid load interactions with MLIs as an essential component.
- Renewable energy sources are increasingly evolving towards a future smart grid as they are integrated into networks utilizing appropriate MLIs. For MLI topology creation and

control, this poses considerable hurdles. There have been many breakthroughs in this sector.

1.11. Overall Objective

The main objective of the PV system is to generate active power. Intelligent control of PV systems can lead to the solution of many power quality problems and improvement of overall system operation. This is achieved by utilizing multifunctional inverters in solar PV systems. Multilevel inverters are a vital technology in solar-based renewable energy systems. The utilization factor of the PV system is greatly improved when the multifunctional capability of the invert is explored. RES should be highly efficient and safe for secure and reliable grid-interconnected operations. Consequently, the next-generation solar PV systems must integrate more controllability by providing ancillary services. With these kinds of services, inverters are called multifunctional inverters. Given this, a detailed study of multifunctional inverters with various controls is required. The primary objective of this thesis is as follows,

- To minimize component requirements by presenting a novel topology for a single-phase 15-level asymmetric MLI.
- The objective is to develop a 25-level variant suitable for renewable energy applications. This variant effectively reduces system costs and size by building upon the initial 15-level MLI structure. The innovative approach to enhancing the initial structure demonstrates the efficiency of the 25-level variant.
- The objective is to design a 33-level MLI that effectively mitigates Voltage Stress. This design is crucial as it demonstrates the system's ability to handle high-stress levels through Asymmetrical Configuration and Optimal Component Choices.

1.12. Description of Tool

MATLAB provides various tools and methods for analyzing skin lesions in medical imaging. Its image-processing toolbox provides dermatologists and researchers with a complete collection of tools for performing tasks such as segmentation, feature extraction, and classification of skin lesions. Algorithms in MATLAB, such as region expanding, thresholding, and edge detection, help to segment skin lesions from images, allowing for the exact identification of

damaged areas. Feature extraction approaches capture helpful information from segmented lesions, such as shape, texture, and color features important for characterization and classification. Furthermore, the machine learning capabilities of MATLAB allow for the design and training of categorization models utilizing extracted features. This enables the development of systems that automatically distinguish between benign and malignant tumors based on obtained patterns, helping in early diagnosis and treatment decisions. The interactive design of the platform enables easy viewing of findings and integration of numerous algorithms into a unified workflow. The versatility of MATLAB's algorithm implementation and its extensive visualization and analysis features make it a versatile and extensively used platform for exploring and creating innovative methodologies for skin lesion analysis in the medical industry.

1.13. Organization of thesis

This thesis is categorized into eight chapters. This chapter also gives clear research objectives, followed by the organization of the thesis.

Chapter 1 presents an overview of the renewable energy resources used in multi-level inverter and a brief discussion on the multi-level inverter. This chapter also presents the types of multi-level inverters by viewing their respective topologies. Some of the main advantages and disadvantages of each multi-level inverter are also introduced.

Chapter 2 then addresses reviews of previous work for the multi-level inverter. It also investigates various active power/reactive power control algorithms for multifunctional inverters with different modes of operation. Based on the work reported in the literature, some research gaps have been identified, and the objectives have been set for further research.

Chapter 3 provides detailed information about power quality enhancement in a grid-integrated photovoltaic system using hybrid techniques. Furthermore, the result analysis and comparisons are discussed in precise detail.

Chapter 4 provides detailed information about the Energy Management of Grid-Connected Hybrid Solar/Wind/Battery Systems using Golden Eagle Optimization with Incremental Conductance. Furthermore, the result analysis and comparisons are also discussed with precise information.

Chapter 5 provides detailed information about implementing Grid-Connected Wind Energy during Fault Analysis using Moth Flame Optimization with Firebug Swarm Optimization. Furthermore, the result analysis and comparisons are also discussed with precision.

Chapter 6 provides detailed information about the Design and analysis of 15-level and 25-level Multilevel Inverter Topologies with low THD for Photovoltaic applications. Furthermore, the result analysis and comparisons are also discussed with precise information.

Chapter 7 provides detailed information about the Design and analysis of 33-level MLI Topologies with low THD for Photovoltaic applications. Furthermore, the result analysis and comparisons are also discussed clearly. Finally, Chapter 8 addresses the conclusion of the overall thesis and its future scope.

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Chapter 2

Literature Review on Multilevel Inverters in Renewable Energy Systems

Over the last decade, energy demand from the power grid has increased significantly due to the increasing number of users and the emergence of high-power industries. This has led to a significant increase in global emissions with conventional energy generation. Therefore, the penetration of renewable energy resources into the power grid has increased significantly. Photovoltaic systems have become the most popular resource as their potential is enormous. Thus, the worldwide installed PV capacity has increased to more than 635 gigawatts (GW), covering approximately 2% of the global electricity demand. Power electronics are an essential part of photovoltaic generation; the drive for efficient power electronic converters is gaining more and more momentum. Multilevel inverters (MLI) have become more attractive to researchers than two-level inverters due to their ability to provide lower electromagnetic interference, higher efficiency, and larger DC link voltages. This passage reviews multilevel inverters based on their classifications, development, and challenges, with practical recommendations for utilizing them in renewable energy systems. Moreover, PV systems with various maximum power point tracking (MPPT) methods have also been extensively considered in this chapter. The importance and the development of a modified multilevel inverter are also highlighted in this review. In general, this review focuses on utilizing multilevel inverters for PV systems to motivate and guide society to focus on inventing an efficient and economical multilevel inverter with the combined capabilities of these converters reported in the literature. Many research works are in the literature conducted for power quality improvement in grid-connected PV systems. All these existing approaches mentioned above could not wholly minimize the Power Quality (PQ) issues. This literature section briefly discusses a few significant influences on the existing literature works.

2.1. Review of various techniques for PV-based MLI

Libin Xu et al. [1] have presented a novel MPPT Method for efficient tracking during fast varying radiation. It has two phases: (1) the computation stage and (2) the regulating step. The computation phase contains the coarse and fine placement operations, which provide an initial duty

cycle value based on the converter's properties and IV curve characteristics. In the compute phase, the duty cycle was similar to the MPP duty cycle, which improves tracking speed. However, their duty cycle oscillates steadily, resulting in power losses.

MAHMOUD N. ALI et al. [2] have presented an efficient FLC-dependent Variable-Step (VS) IC MPPT process for the PV model. The VS-IC-MPPT estimation was based on the degree of power-voltage relationship. An efficient fuzzy was presented for this goal by introducing five practical areas surrounding the MPPT. The proposed Fuzzy logic was created to change the duty cycle step size. The proposed method can improve MPPT efficiency when changing the incremental conductance method step size. The MPPT process has deficiencies in precision and convergence speed.

Sumaya Jahan et al. [3] demonstrated a progressive control method for Grid-Tied Multilevel Inverter PQ Improvement. The suggested controller was a Proportional-Integral Resonance (PIR) through harmonic and lead compensator feedback. The primary goal of the control technique is to get the most power out of the NPC converter and into the grid. The PIR controller ensured the maximum constant voltage was provided at the input side. Separate voltage and current controllers were employed in this system to supply the maximum power while also generating the sinusoidal output voltage and current. But, if the grid was weak, the performance would not be up to the mark and would be unacceptable.

An ideal hybrid control strategy has been shown by P. Rajesh et al. [4] to improve PQ in grid-connected systems. The suggested hybrid method was named Improved Bat search Algorithm with Moth Flame Optimisation Algorithm (IBatMFOA) because it combined the features of both the Moth Flame Optimisation Algorithm (MFOA) and the Improved Bat Algorithm (IBat). The bats' search behavior function was altered by using the crossover and mutation functions. MFOA was used to lower the error function and improve the IBat technique's searching behavior. Enhancing the PQ based on active and reactive power variability was the primary objective of the suggested IBatMFOA technique. MFOA was optimized to reduce power variation and reach the aim. The efficiency of the entire system was increased by applying the IBatMFOA approach.

A Variable Step Size Robust Least Mean Logarithmic Square-Based Control Scheme (VSS-RLMLS) for the Optimised PV module has been presented by Parida A. and Subudhi B. [5]. The VSS-RLMLS algorithm in the suggested control method accurately gathers the essential elements of the nonlinear load under dynamic circumstances, producing a reference current. This

permits the VSC to operate efficiently and supplies the grid with high-quality power by reducing the harmonics of the loads. It was discovered that the suggested control had the best PQ effectiveness and the lowest grid current THD.

Ricsa Alhassane Soumana et al. [6] have presented a novel control technique for multifunctional grid-connected PV system (GCPVS) modules. The primary goal of this work is to improve the PQ at the point of standard coupling (PCC). The control approach considers the inverter's power rating, determined by its maximum current modulus. It controls the GCPVS's reactive power compensation, active power injection, and current harmonic filtering, in addition to restricting the inverter current to avoid overrating activities.

An EMS and Development of PQ with Grid Combined FLC has been presented by Himabindu Eluri and M. Gopichand Naik [7]. This publication uses incremental conductance (IC) approaches to accomplish the MPPT P&O rule. For an AC/DC microgrid, the design and implementation of an EMS with FLC have been completed. In addition to EMS design, MG's PQ has been enhanced. The FLC achieves a desirable SoC while simultaneously extending battery life. To address concerns with PQ in the event of nonlinear and unbalanced load circumstances, an EMS grid-integrated MG based on FOLC was implemented. On the other hand, limiting the subsequent voltage change to the same command as the previous action as power increased was feasible.

A Grey Wolf Optimisation (GWO)--based on optimal grid-connected solar PV with improved PQ attributes has been proven by T. Nagadurga et al. [8]. This research proposes to overcome these issues in RES-incorporated grid-connected PV systems by combining GWO with a static synchronous compensator (STATCOM). By employing the GWO technique, the sporadic nature of solar PV generation under shaded situations can be utilized. One of the many specialized power electronic devices that successfully lower PQ issues like THD and voltage sag/swell is STATCOM. By employing some fine-tuned parameters to keep the DC connection voltage constant, the fast-acting PI controller was meant to operate a STATCOM.

Maximum power point tracker (MPPT) based on an Adaptive TS-Fuzzy based RBF Neural Network (ATSFRBFNN) has been presented by Priyadarshi N et al. [9] and is used for grid-integrated PV systems. The innovative learning algorithm offers precise and quick PV power tracking in variable solar insolation. Enhanced damping circulating current limiting inverter has

been utilized to produce the gating signal of VSI, reduce power loss, and prevent PQ problems. Furthermore, this technique failed to track the MPP under unpredictable weather conditions.

Ouai et al. [10] have proposed a novel strategy that significantly enhances the Power Quality (PQ) of large grid-tied PV systems. This method, which provides soft and fixed DC voltage through active filtering, ensures a sinusoidal grid current. The decoupled control of real/reactive power with a fuzzy logic controller further adds to its effectiveness. The suggested novel strategy has proven highly effective in reactive power compensation, generation, and active filtering. However, it falls short compared to the parallel active filter regarding output power quality.

Hasheminamin et al. [11] have developed a robust and economical method to decrease the voltage level via Single Point Reactive Power Control (SPRPC). This control strategy, which works by absorbing reactive power after a nominated point, effectively reduces the rise in voltage level. The method has proven to be robust and economical, helping to reduce the increase in the voltage level of the affected grid. However, it does involve a significant number of calculations to evaluate the PQ performances of the grid system.

Fekkak et al. [12] proposed the modeling and controlling of a transformer-less grid-connected PV system. The MPPT control technique, based on a fractional open circuit voltage algorithm, was modified and combined with a boost converter to achieve good tracking accuracy and deliver a fast response. MPPT is used to track the MPP and control the amplitude and frequency requirements of the utility AC grid. However, the modeling of this proposed system was done without considering the system losses.

Chettibi and Mellit [13] presented a control technique for enhancing power quality in a hybrid system connected to the grid. This grid-tied hybrid structure comprises PV, fuel cells, and batteries. This method regulates the system's power flow by neuron fuzzy gain tuners. This method improved power quality, reactive power control, and voltage stabilization. However, the system showed more complexity when validating the experimental data in a few cases.

Abadlia et al. [14] proposed a sliding mode-based control technique for the grid-tied hybrid system to improve its power quality features. This technique made the system more elastic, flexible, well-organized, and straightforward. However, this control technique may sometimes

cause energy loss, change in dynamics, and system instability because of high-frequency oscillations called chattering.

Zeng et al. [15] proposed the Multi-Functional Grid-Connected Inverters (MFGCI) for renewable source incorporation and PQ improvement. The Pareto approach was used to derive the optimal solution of the model. This method avoided using an extra power quality conditioner in the microgrid. However, the capacity of MFGCI was a limitation, as it could be used only for actual power generation, and total compensation could not be done by using this method.

Kollimalla et al. [16] demonstrated a variable P&O MPPT algorithm that was implemented to track the MPP during sudden changes in irradiance. This technique includes three algorithms: the current perturbation algorithm, the adaptive control algorithm, and the variable perturbation algorithm. The variable perturbation algorithm dynamically decreases the perturbation size, which is wholly based on the polarity of the change in power. Still, it requires a large data storage area and extensive computation.

Elmetennani et al. [17] presented the MPPT technique, implemented using a hybrid dynamical technique to model the PV generator. The designed MPPT algorithm for optimizing the PV chain production monitors the functionality of each power conductor device. The designed MPPT structure uses a multicellular converter instead of a classic DC/DC converter to overcome the properties of its specific topology. The design of the MPPT algorithm is entirely suitable for multiple-cell structures, but the same procedure was not followed when designing the N-cell structure.

Keyrouz [18] demonstrated an intelligent Bayesian network (BN) method used for MPP tracking of a PV array under partial shading conditions (PSCs). This method achieves efficient robustness, tracking efficiency, and speed performance, demonstrated through different simulated scenarios. In the proposed method, the PV array is desired to operate at any period. In this proposed algorithm, the additional computational burden on the processor is added, whereas an enormous number of particles is required to cover the entire system.

Robles Algarín et al. [19] presented a fuzzy controller for tracking the MPP to improve the PQ features. This research developed an optimal MPPT technique tested under varying climatic conditions. Using a fuzzy controller, this method can supply the maximum possible power to a

battery in an off-grid PV system. The proposed technique uses a more straightforward hardware setup with only one voltage sensor. A closed-loop MPPT technique was developed based on a conventional PI controller, although the fuzzy controllers used in the method are costly.

Koad et al. [20] demonstrated a new MPPT technique that implements a PV system based on the PSO algorithm and the Lagrange interpolation formula. Here, the proposed PSO shows better results because of its simple implementation and capability to achieve MPP in various environmental circumstances. An optimum number of iterations is required to achieve the MPP, but detecting the resulting power loss and convergence issues is difficult.

The study by S. Mohapatra et al. proposed inverter topologies. In that, the author looked at various switching topologies, including flying clamped inverters, neutral point clamped inverters, H-bridge inverters with cascading NPC inverters, FC inverters, and CHB inverters, all of which require more parts than the inverter that is being proposed. It has a complicated circuit and high switching loss. A hybrid cascaded multilevel inverter topology with fewer switching elements and DC sources has been designed. The author introduced the hybrid inverter without employing the pulse width modulation technique. Results indicate output with reduced harmonic content [21].

The suggested approach uses a single PV source that operates asymmetrically. This mode provides eight positive and eight harmful voltage levels (17 levels, including 0V) without a separate switching mechanism. Eleven switches are supplied in a cascading pattern to produce various voltage levels from a single PV source. The output of a dc source is increased using a dc-dc sumo converter. This increased the DC source's production, which the inverter received. The output side of an asymmetrical mode of operation has seventeen voltage levels. An Atmega16 microprocessor controls the power electronics switches. The proposed model is created using MOSFET. Simulink takes into account the R load. Per the simulation's findings, the proposed inverter has a very low total harmonic distortion [22].

Ajmal Farooq et al. introduced a new topology for low harmonic distortion. The authors proposed a novel topology for a multilevel inverter with seventeen levels for high-power applications and the fewest possible components. Low switching loss and low dv/dt stress are the outcomes. Two bidirectional switches, six unidirectional switches, and four DC sources make up the design of the suggested inverter. The proposed model provides seventeen voltage levels, comprising eight positive, eight negative, and one zero voltage level, using ten IGBTs and four standalone DC

sources. The voltage of DC sources is chosen using a 1:3 ratio. If V 1 is 25 V, V 2 will be 75 V, three times V 1. The PWM approach is sinusoidal. The capacitor is used to compress harmonics. The Proposed model has the advantage of minimum harmonic distortion with a cascaded hybrid inverter with sine pulse width modulation technique [23].

Felipe Bovolini and Grigoletto propose a new five-level architecture for an inverter with lower harmonic content and no transformer in their paper. The PV system uses this topology. The suggested inverter topology utilizes reactive power. This proposed model uses a straightforward modulation mechanism to provide a five-level single-phase transformerless inverter. Circuits employ capacitors. The grid neutral point is connected to the PV stack negative point to achieve minimal leakage current or virtually nil [24].

In their paper, N. Kalaiarasi et al. discuss hybrid architecture for nine-level inverters for photovoltaic applications. This suggested model employed a cascaded configuration of half-bridge inverters connected in series. The calculated output at the AC voltage level is 2*n+1, where the total number of sources is represented by n. The total of all inverter output voltages is the inverter's overall output. Compared to traditional VSI and CSI, staircase output is achieved with lesser harmonics and higher output voltage [25].

Different topologies for inverter operation and control strategies for multilevel inverters were represented by Zina Boussada et al. Diode Clamped Inverter Topology is one of them. The existence of a DC bus on phase reduces the need for capacitors. This makes it impossible to employ this topology. Topology for Flying Clamped Capacitors. Only one DC source is required for this setup. The advantage is that balance flying capacitors and clamping diodes are not required. The second one is Cascaded Topology. This topology is straightforward. This topology creates a bridge converter based on a full-bridge converter coupled in a cascaded configuration. High power levels benefit significantly from this topology [26].

The suggested multilayer inverter is designed utilizing a T-type inverter with sub-switches of H-bridges, as described by C. Dhanamjayulu et al. Using the staircase PWM approach, 17 voltage levels can be obtained with various loads. The proposed inverter can be used for applications involving facts and unconventional energy. Fewer power switches were needed in the proposed model, which led to lower costs and better performance. More efficiency was obtained for both linear and non-linear loads [27].

In their research paper, T Raju J et al. offer new topologies designed for multilevel inverters to generate 11 voltage levels at the output side. Their topology recommended an inverter with fewer DC sources. As a result, a simple inverter circuit with good output performance reduces the harmonics present in the inverter by using the PWM waveform technique [28].

Using a contemporary UPFC, T.A. Sivakumar and M. Mary Linda [29] have shown the dynamic performance of grid-connected wind farms. This manuscript intends to increase the system's transmission capability and boost AC grids' emotional response by decreasing power quality concerns by utilizing UPFC interconnected at PCC. By properly switching the semiconductor devices of the UPFC, the waveform distortions are reduced. A PI controller with current-controlled pulse width modulation controls the switching (PWM). The Modified Particle Swarm Optimization Technique (MPSO) adjusts the PI controller's gains. However, since these systems need constant online tweaking of their gain settings and have severe nonlinearities or variable characteristics, it was unable to manage them successfully.

By using HVDC and STATCOM centered on a non-linear controller, M. Darabiana et al. [30] suggested a Non-linear Generalized Predictive Control (NGPC) for the stability study in a hybrid power system of series and parallel compensators in the presence of wind farms. This system uses HVDC to increase the damping of the transmission network connected to the DC system. At the same time, STATCOM is used as a parallel compensator to increase the reactive power of the wind farm. The observer’s design assesses the controller's robustness to system functional characteristics alterations. But because of internal issues, they performed less.

The improvement of steady-state and transient operation has been proved by Reza Hemmati, Hossein Faraji, and Narges Yavari Beigvand [31] using a DFIG wind turbine coupled with an energy storage system and FACTS devices. A DFIG connected to the external grid implements the suggested control method. The DFIG also incorporates a battery, a thyristor-controlled reactor (TCR), and a thyristor-switched capacitor (TSC). These gadgets are built into grid-side, rotor-side, and DC link converters. The suggested control strategy simultaneously accomplishes several objectives, such as voltage compensation, damping fluctuations, etc. But this results in oscillations in the voltage level, stator, and electromagnetic torque because there isn't a constant switching frequency.

Haidar et al. [32] proposed estimating wind farm reactive, quick changes using an adaptive one-dimensional convolutional neural network. By incorporating an additional predictive control block into the traditional control scheme, this research suggests a predictive control system for SVCs. Its foundations are deep neural networks, specifically adaptive 1D-CNN. Effective learning weights are used to increase the prediction accuracy and computational complexity of the 1D-CNN training process. However, a feed-forward loop half-cycle time delay negatively impacts the effectiveness of SVC.

A Novel Hybrid Method for Multi-Objective Reactive Power Planning through FACTS Devices and Renewable Wind Resources has been demonstrated by Rahmad Syah et al. [33]. The solution is a multi-objective hybrid technique that combines viral colony search (VCS) with particle swarm optimization (PSO) while taking into account linear and non-linear restrictions (VCS). VCS is a new optimization technique based on how viruses look for host cells to kill and induce the best virus to enter the cell to reproduce. The suggested model employs the PSO to improve local and international searches. Additionally, the data is sorted using the Pareto criterion's non-dominated sorting. The system's performance needed to be sufficiently developed, which caused additional faults in the voltage stability.

Franco Fernand Diaz et al. [34] presented a model predictive control (MPC) strategy to regulate the converter to control PV power. With the help of this technique, high-performance gain can be achieved, the over-current situations can be limited, and the operation is stable. In the precious works, PV-based inverters were placed to insert full active power for ordinary operation. However, the newly created grid procedure requires injecting reactive power to support voltage for the period of voltage sag. Hence, the solar cell must change the Panel array’s operation location from MPPT on actual status to a Reduced Power Mode (RPM) when voltage assistance is needed to confront high current situations. In this chapter, the MPC technique is exploited to manage a PV-based array system with a boost converter to compensate for the effect of power from the solar array on actual conditions and other fault conditions. The MPC approach can check the maximum power point under solar irradiation level modifications and minimize solar power when required by the system. This type of control strategy forecasts the upcoming power provided by the PV array system in terms of the achievable switching states, voltage, and current from the solar panel. The

incorrectness between the reference power and forecast power from the solar panel is mitigated by its cost function.

Hasheminamin Maryam et al. [35] have proposed a Single Point Reactive Power Control (SPRPC) to minimize the voltage level by absorbing the reactive power. The main advantage of this method is that it is robust, economical, and well-organized in removing the voltage rise in the affected grid. This work proposes an innovative, fresh, extensive method that attempts voltage rise mitigation by a fundamental reactive power control technique, that is to say, SPRPC. That results in more profits from the network phenomenon, removing harmonics with more robustness and less cost while servicing a broader system section by pleasing only one node. Regarding this, the most impressive point of the system is that the awareness of voltage sensation must be acknowledged. Consequently, an Impedance-Voltage Rise Index (IVRI) is defined as the short circuit impedance of the interconnecting network and its result on voltage execution to assist with better node options. The primary purpose of this SPRPC technique, apart from the low cost, is that all different PV-based inverters in the Distribution network can stay at their integrity power factor without needing an inverter. As represented above, the inverter's rating for the solar-based system at a suitable node is only 30 KVA and even less than the accumulative amount of absorption of reactive power of all remaining PV-based inverters in swag-related scenarios. The cumulative measure of the initial rating of inverters is even better than the absolute assimilation. The control technique is mentioned as a distributed networking operation side algorithm, as introducing a centralized regulator in one of the load connections may not be reasonable for residential-based customers. Moreover, other communication system connections can also have advantages, while distribution networking allows more solar generators to enter the system. In other words, the overall consolidation capability of the PV array into the communication system can be expanded. One more remarkable outcome for the SPRPC algorithm is that the applicable anatomy demands a controlled number of switching patterns to serve its execution; at the same time, all other PV array-based inverters can stay as unaltered with a power factor as unity. This control algorithm is cost-efficient and robust and provides executable results that can be practically used for any voltage rise striking the distributed network and improving the hostile capacity while enhancing the voltage stability of the system for both day and night. However, the developed SPRPC technique requires a specific quantity of computation; it confronts lots of shifting and excess calculations for all other PV-based inverters.

Patra Sandipan et al. [36] have developed a three-phase grid-connected system with single and dual-stage circuits. Utilizing the space vector pulse width modulation (SVPWM) smoothens the switching sequence to improve power quality. The SVPWM switching technique is the most significant modulation approach for 3- 3-phase inverters because of its broader modulation extent and comfort in execution technique. Contradictory to some other modulation strategies, it delivers shallow harmonic distortion characteristics. The Z-source inverter (ZSI), mainly utilized in grid-affiliated solar systems, is required to regulate the DC and inverter sides. The factor of the buck-boost converter is observed with the help of the modulation index. The boost factor can be controlled by the duty interval of the shoot-through zero state over the non-shoot-through state of the SVPWM switching algorithm just because it provides the same zero voltage to the load terminal side. The addressable shoot-through period is restricted by the zero-state period and is observed by the modulation index. The SVPWM technique has established its inferiority over other carrier-based maximal boost control approaches in various prospects. Hence, the SVPWM switching technique is executed for ZSI control in circuits. The power transistors are regulated by suitable switching temporal order to shape the output. To mitigate the restricted and oscillated output voltage level in PV by minimizing the high emphasis on the switching pattern of the inverter, the practical application has been transformed from a 3-phase PWM into a 3-phase PWM Inverter with a boost converter. It also has disadvantages, such as high cost and difficulty in two-stage power transition. The modern power electronics investigation has initiated a new ZSI to mitigate these disadvantages. However, this type of circuit was expected to have decreased losses comparatively, which must be analyzed in the future.

Kumar et al. [37] illustrated a 3-phase grid connected to a photovoltaic (PV) system with battery energy storage to enhance power quality features. With the help of the Variable Step Perturb & Observe (VS-PO), the Maximum Power Point Tracking (MPPT) strategy has been exploited to force the PV-based generation to accomplish the maximum power process. A boost converter connects the Solar panel array to the general DC bus. This converter is regulated through the MPPT technique, which is detached to maximize the PV array's voltage level. A Battery Energy Storage System (BESS) and a bi-directional converter, also affiliated with the DC bus, regulate the voltage at a constant value. The bi-directional converter can conduct the battery in both charging mode (bus voltage is much better than the requisite load voltage) and discharging mode (bus voltage is lower than the requisite load voltage). To ensure the PV panel array works at maximum power

point (MPP), VS-PO is used promptly. Because of this, when the operating location is very close to the MPP, the disturbance is minor, and when the operating area is too distant, the disturbance is high. It also enhances both algorithm quality and tracking speed. The control method used in this chapter is recommended to be economical and self-directed for any modification in the load side. A 3-phase hybrid filter is established and constituted by a shunt passive filter and a series of active filters affiliated with the standard grid to balance the reactive power and load current harmonics. A hybrid filter balances the reactive power needed by the load side and minimizes the harmonics level. However, the practical application of hybrid filters in the network makes it too complicated and expensive.

Chettibi, N, and A. Mellit [38] have presented an intelligent-based control technique for grid-connected hybrid systems with solar panels, batteries, and fuel cells. This technique uses neuron fuzzy gain tuners to regulate the power flow of this system. This method has the advantage of enhancing power quality, controlling reactive power, and stabilizing the voltage. The essential purpose of the energy management network is to monitor the entire power flow and its sharing between the distributed generation resources so that the load power demands are mitigated. About its convenience of producing solar power, the total amount of power requirement, and the battery's state of charge, the Power Management System (PMS) determines the regulated orders for localized controllers of the auxiliary power generators ((SOFC) & (BESS)) and decides their condition of procedures. In this chapter, the solar energy source is mentioned as the original energy source where the SOFC composed with the BESS are utilized as additive power sources. The management operation starts by computing the net power, equivalent to the variation between the solar panel's produced power and the load side's power. The active and reactive power flow is dynamically regulated by online calibration of the Proportional Integral (PI) parametric quantity that assures gratification at any period of the load demand. Furthermore, the formulated PMS can regulate the power set-points for SOFC and BESS precisely by considering various preconditions of demand and supply. The vital benefit of this particular strategy can be concluded as the lack of a requirement for an accurate numerical model of the network and the ability and strength against the disturbance. As the appearance of this paper, the formulated control strategy should be executed on the advanced program to affirm its skillfulness, feasibility, and efficiency experimentally.

Adel Choudar et al. [39] have demonstrated localized power management of hybrid Photo-Voltaic (PV) with energy storage-based distributed generation for the microgrid (MG). MGs are planned to function in both island and grid-tied modes where a broad extent of control, security, and energy management are requisite to ensure optimum operation. The principal purpose of this instant production is to declare an improved establishment scheme for a solar array-based active method. The electric energy needed by the grid manipulator is conferred as an acknowledgment of MG's input. The executed control strategy should decently divide the whole power reference between the scheme portion. Numerous constraints are taken into account in the repartition phenomenon, such as the availableness of the solar power (difference with the level of solar irradiation), the power request acknowledged by the grid manipulator and the state of charge of energy storage elements (when it is fully supercharged, we should not reserve the power, anonymously, when it is empty, we should reload or recharge it), etc. Considering these constraints, a proper operative mode is chosen; then, the planned energy management control strategy will compute and dispatch the power acknowledgment to the devoted controllers of the various energy sources (PV, Battery, and ultra-capacitor). A specific intention has been paid to the solar power restriction mode, which occurs when the addressable PV array power is much greater than the grid request and both energy storage units are ultimately charged. But sometimes, the operating point of the solar array should be shifted from a maximum power point limit to a modest power point. This action is fragile because the power and voltage curve of the PV panel array is nonlinear.

Zhang et al. [40] have illustrated energy management in micro gird (MG) with distributed energy sources to improve the system’s efficiency, security, and reliability and reduce the emission of radiation. This work's performance measurement is supplementarily adapted to MG functioned as grid-tied, stand-alone, and networked modes. Each MG comprises a PV panel, a hydrogen fuel cell, a hydrogen storage tank, an electrolyzer, and a load. This work aims to initiate MG execution measures for the MG performance assessment from extensive prospects: environmental effect, cost, and quality of service. From here, quality of service is the ratio of supply power/demand power. By performance evaluation, the optimal designing and working of the MG can be attained. Models of a grid-tied MG, stand-alone MG, and an MG network system with multi-agents are planned for the computer simulation on the power generation, consumption, distribution, and

energy level of storage. At the same time, the topography of those designs does not extend the modeling. First, considering the stand-alone system, load forecasting reduced the daily electrical energy exhausted by about a specific percentage. The quantity of Hydrogen (H2) stored energy oscillates dramatically, and the capability of the H2 tank is significant. In this case, since the electrical energy produced is not adequate to meet the daily energy demand, no load shift is present at that place. Furthermore, both the quality of service and whole performance metrics are maximized with the size of the PV panel; merely the emission value is always equivalent to one, zero emission and price basis is also changeless which depends on the charge of the PV panel. Secondly, considering the grid-tied mode of MG, load forecasting is an essential phenomenon in the daily exhausted electric power, which drops 25% in 4 days, and a few loads in the period of daytime are displaced to the nighttime. Because of the connection to the grid, the H2 energy storage system's capability is down when compared with stand-alone MG.

The size of the PV panel has a minimal consequence on the emission and quality of service indexes. Merely. It does enhance the cost index. Consider the system with multiple numbers of MG's; the control of the power statistical distribution powerfully distorts the performance of MG. However, the entire performance index alternative of any particular index is maximized with the power generation of MG from renewable-based energy sources. The distributed and ever-changing system with multiple MG's can be simulated regarding present-day programs. This type of model can be formulated in the future with a primary focus on load requirement, prediction, energy presentation, and planning, along with real-time dynamic costs. Furthermore, the design activity of the distributed energy generation will also be attributed to the establishment of heat and power generation for the transient outcome of the network.

Abadlia Issam et al. [41] have proposed a power control technique based on sliding mode in grid-connected hybrid systems. This technique can make the system more expandable, flexible, efficient, and robust. For this, it achieves higher performance. For grid-connected system control formula topography and performance, executions are essential. To deliver a reliable control scheme, more stipulations and constraints are crucial. Specifically, power control perturbation and instrumentation prices are the average duty of any power scheme. The quality of an algorithmic program defines modern control techniques as an outcome of raised expenditure to execute. In this chapter, a simple Sliding Mode Controller (SMC) algorithm is formulated and used to control P

and Q powers in a grid-connected hybrid power system comprised of solar panels and a hydrogen Fuel Cell (FC) generator. It excludes controlling both the power output of the PV generator and inverter output for maximum power.

An easy cascaded loop also regulates the FC network, which operates the maximum power and regulates the output voltage. In that respect, there are two critical aspects to this work. The first goal is to implement hydrogen energy as a secondary to the traditional energy storage systems to get better variableness and indeterminacy of the PV sources with the cost-efficient storage system. The second one is to produce an autonomous control of both active and reactive power grids with better compensation of reactive power with the help of the SMC control strategy. The obtained outcomes confirm the efficiency of the SMC-based system. SMC control techniques are easy and provide the benefits of: employ to insert maximum solar power, rectifying the utilization of FC energy for taking full advantage of an essential Hydrogen (H2) tank level, and ensuring an autonomous active and reactive power control with better compensation of reactive power, at the same time regulate the output current in phase with the utility voltage through SMC technique. The necessary augmentation of this paper has appeared with the modeling of SMC. The SMC algorithm is established with a simple topography and high-performance index. This concept was formulated to fulfill all suggestions for grid-connected power generation systems with proper control behaviors. The outcome demonstrates that the network enables a high-quality active power–reactive power control with better decoupling, satisfactory compensation of reactive power, and excellent power factor. However, this control strategy can produce high-frequency vibration, referred to as chattering, that may cause a change in dynamics, energy loss, and system unstableness.

Tejwani, Vinod, and Bhavik Suthar [42] have implemented the design, analysis, and modeling of hybrid Photo-Voltaic (PV) with Fuel Cell (FC) to compensate for the reactive power characteristics. A hydrogen-based FC is an evidenced application, and its usage and the solar scheme can lead to power stability in standalone or grid-connected systems. Many commercial enterprises in the formulated countries use the active power factor recompense method to balance the power factor management. Likewise, some of the specialized applications demand fantastic power quality that has stimulated the usage of active power filters. In this particular case, the higher

expenditure of active power system search can partially be paid by interconnecting hybrid PV-FC on the DC side of the system.

The grid-connected hybrid PV-FC system can produce an additive operation for power factor improvement and active filtering. The employed control technique in this work has the benefit that the hybrid PV-FC system will operate for the whole day. The grid requisite and codes can deliver these subsidiary services. However, the consolidation trouble related to improving a grid-connected system using the FC source as the substitute system must be better interpreted and authenticated in the literature. Moreover, and perhaps more significantly, the dynamic fundamental interaction between system elements of such a system (PV-FC) that happens while operating real-world loads (distributed generation system) remains to be explored.

Arun Kumar Verma et al. [43] have demonstrated that a grid-interconnected solar photovoltaic (PV) based array can improve AC mains' power quality. A three-phase voltage source converter (VSC) mitigates the load unbalance, harmonic currents, and reactive power compensation for Power Factor Correction (PFC). The proportional Integral (PI) controller is used to balance the voltage of the DC bus at the time of variation in load. Moreover, this analysis uses the synchronous reference frame theory (SRFT) to control power generation from solar PV panels. Additionally, its 3-phase VSC regulates the harmonic current and balances linear and non-linear loads. Both zero voltage regulation and PFC of the implemented control strategy have been attained, and execution of this particular network is found to be quite tolerable.

Abadlia et al. [44] have demonstrated power management control for Renewable Energy Sources (RES) with an Energy Storage System (ESS) in a stand-alone grid-connected mode, with the help of a fuzzy logic control strategy to manage the power flow. The primary purpose of this paper is to balance the power generation produced, which ensures the continuity of energy and increases hydrogen production. Photo-voltaic (PV) is considered as a primary source. ESS is a substitute power source utilized in the essential periods comprising Fuel Cell (FC) and battery as an alternative. The control technique assures an optimum operating network at various environmental conditions, enables the delivery and increase of the accomplishment of the hydrogen at the same time, and suggests a perfect resolution for function in stand-alone applications. This is evaluated by the computer simulation outcome elaborating power sharing among the solar-generated power, battery power, load demand, hydrogen production, produced FC power, and the

charging/discharging mode of the battery under various premises of solar-generated power and variation in load. Additionally, an uncomplicated control strategy is working for the charging/discharging condition of the battery. It accessed outcomes using MATLAB/Simulink software to demonstrate that the established intelligent technique, often a considerable resolve for controlling power flow that warranted the controversial load requirements, enables the battery's electric energy stock.

2.2. Problem Statement

The utilization of renewable energy systems in power grids has been enhanced due to advancements in power electronics devices and related technologies. However, challenges remain about electricity quality, grid reliability, and security. To ensure grid power quality, many standards and guidelines have been established for grid-connected RES. Based on the reviewed literature, it is understood that additional research is required in the following areas.

- The integration of renewable energy systems to grids using suitable MLIs has gradually been moving grid systems towards the future smart grid. This comes with significant challenges and presents some MLI topology development and control opportunities. Thus, there are numerous innovations in this field.
- Regulating DC-link voltage and controlling the MPPT in MLIs usually requires a PI-based controller associated with certain limitations. Several soft computing and hybrid methods-based control systems can be evaluated for better multidimensional control.
- The efficiency of the MPPT algorithm is affected by many factors. Still, the most obvious is the nonlinear nature of the PV system, the system working conditions, and the variations in ambient conditions. Most of the time, algorithm developers do not consider these changes, which has been the source of system failure in specific working conditions. Thus, designing the PV module controller is a tedious task that demands more attention to achieve stability.
- A key determinant of selecting the proper MPPT is to find the optimal MPPT method with fast performance, low tracking errors, and no oscillation around the GMMP. The evaluation of MPPT techniques typically comes with various degrees of complexity; hence, many studies are ongoing to address most identified problems. Therefore, efforts should be

geared towards finding a simpler, faster, and cost-efficient MPP tracker that could offer better reliability and efficiency.

2.3. Summary

This chapter has briefly outlined the aspects of multilevel inverters to highlight the need for further investigation. This chapter has briefly outlined the elements of multilevel inverters to underline the need to produce new inverters or modified combinations of inverters for grid-connected and PV systems. MLIs have been elaborated in various aspects, such as classifications, advantages, disadvantages, and their abilities to enhance energy conversion in modern energy systems. Based on this review, a modified approach using MLIs for different levels should employ standard MLIs to reduce the switching count. Modified MLIs are promising solutions for PV and other renewable energy systems in size, cost, less THD, and high-efficiency energy conversion. Besides, the most recent MLIs grid-connected PV systems and the methods for minimizing current leakage suppression were highlighted in this work. Lastly, the challenges and practical recommendations for developing an efficient system were highlighted to motivate and guide society to focus on inventing an efficient and economic MLI grid-connected system that combines most of the used and reported inverters' capabilities.

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Chapter 3

Power Quality Enhancement in a Grid-Integrated PV System

a. Using Hybrid Techniques: Grey Wolf Optimization (GWO) and Binary Particle Swarm Optimization (BPSO).

Photo-voltaic (PV) arrays are how the PV system was designed to supply solar power in recent years. The PV generator shows nonlinear voltage-current characteristics and temperature- and radiation-dependent MPPT. Multiple different MPPs show up in the PV module's power–voltage characteristic when there is uneven solar insolation. Therefore, a hybrid combination of Grey Wolf Optimization (GWO) and Binary Particle Swarm Optimization (BPSO) has been suggested to handle multiple MPPs. The author used a hybrid method since this combination is not found in any literature. The primary benefit of the proposed method is its capacity to accurately predict the global MPP (GMPP) in a short amount of time and to continue doing so even in various scenarios. A 31-level MLI with a lower blocking voltage process was created to simplify the circuit design further. The PV system's effectiveness was examined by running the entire system on the MATLAB platform.

3.1. Introduction

The maximum energy demand has emerged in recent years, making renewable energies like wind and solar more desirable for power grid applications [1]. Due to improvements in semiconductor technology, PV modules, among these renewable powers, are used on a larger scale because of their lower production costs [2]. Administrations are also taking many actions to encourage the use of solar energy because it is clean and environmentally friendly [3]. The grid or loads cannot utilize the electricity PV systems generate immediately. The acquired energy can be effectively used with power converters [4]. Non-linear loads and elevated converter usage bring on several power quality issues. Power quality issues are caused by harmonic current exported to the grid, which raises harmonic level and voltage variations [5, 6]. The two power conversion stages in the PV system lead to a decrease in efficiency and a rise in system reliability [7]. The

inverter's design and control must be done effectively to improve the PV-organized grid system's final power output [8]. Reactive power compensation and unity power factor preservation are two benefits of inverter control in photovoltaic systems [9], [10]. A comprehensive review of the literature found that the hybrid BPSO–GWO combination has not been used to create an MPPT. Therefore, this work aimed to use the BPSO–GWO to create an MPPT that would effectively track a PV system's performance under different circumstances.

3.2. Problem Statement

- Due to its greater robustness and quicker convergence than other optimization techniques, this field has drawn significant attention from the research community, as evidenced by the numerous works published in the literature.

- In addition, compared to other evolutionary approaches, it requires fewer operators and variables for modification, which is advantageous when a quick design process is taken into account.

- Electric power fluctuates due to the PV array's random nature. These oscillations harm electric power systems' stability and power quality.

- The utility was extremely concerned about the high degree of solar energy penetration in distribution systems, which poses a threat to THD, voltage regulation, and stability for the entire system.

3.3. Contributions

- To improve the PQ features, a hybrid BPSO–GWO-based PV system connected to the grid is introduced. By using BPSO, maximum power transfer from the PV array to the grid is guaranteed.

- In the event of an abrupt change in the amount of sunlight, the suggested MPPT technique offers extremely effective performance with a prompt response.

- This study investigates a hybrid control system that can give a grid-connected photovoltaic inverter multiple uses. Despite solar energy's unpredictable nature, this approach ensures a steady supply of energy.

- The primary benefits of this suggested approach are its quicker MPPT performance and lower complexity compared to the Gauss-Newton method, as the hybrid algorithm does not contain double derivative terms.

3.4. Modelling of the PV Array

The quantity of PV modules is maximized to lower energy costs, which meets load demand. Moreover, processing parameters, geographic location, and temperature all influence the PV module's output power. By relating the PV panel in series or parallel, the voltage and capacity of the PV system are calculated [11]. The MPPT technique is taken into consideration in the PV system to boost the PV output power. Reducing the steady-state oscillation and eliminating the variable irradiance level increase the MPPT technique's efficiency. Figure 3.1 displays the MPPT technique's overall block diagram.

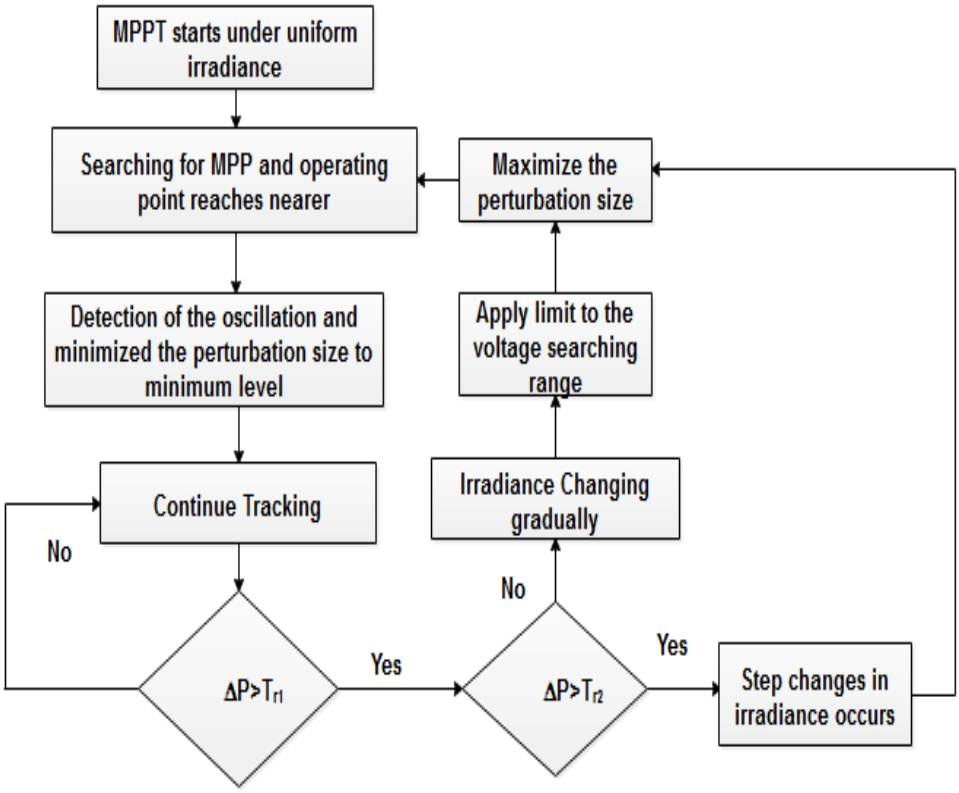

Figure 3.1 The overall flow of MPPT.

Similarly, MPP's operating point oscillates between the subsequent samples. However, a unique mechanism detects the oscillation, reducing the perturbation size until a positive minimum value is reached [12]. In this case, a lower power tolerance is permitted to accommodate the minor power flickers that arise. Because of the slight oscillations, there is a power difference (ΔP) between the successive samples. The smallest possible perturbation size is attained since the ΔP/P value stays below the threshold limit.

3.5. Proposed Method

The unshaded PV array receives high radiation levels in various environments, while the shaded area only receives lower radiation levels. The amount of shaded area defines the partial condition, and the proportion of irradiation on the shaded parts to the unshaded parts defines its shading factor. When a partial operational state is identified, the shading factor is assumed, and the condition is fully considered. MPPT requires accurate partial shading identification and thorough appraisal to demand the appropriate process and monitor the MPP.

3.5.1. 31-Level Multi-Level Inverter

Figure 3.2 displays the proposed method's block diagram. This study suggests a modified setup for a 31-level MLI that uses a lower maximum blocking voltage protocol. This process provides several levels with the fewest power electronic buttons. The following are the primary benefits of the suggested design: reductions in installation space, number of switches, power diodes, gate driver circuits, and cost. The implementation procedure supports managing the extent of DC sources [13]. This calculation aims to identify the MLI's ideal DC voltage ratio, establishing the range of voltage levels possible for the resulting high PQ. Figure 3.3 displays the Simulink structure for the 31-level MLI with the blocking voltage process. The P-Channel MOSFET, which has a smaller range than electron flow, is used as the charge carrier in MOSFET SL3 in Figure 3.3.

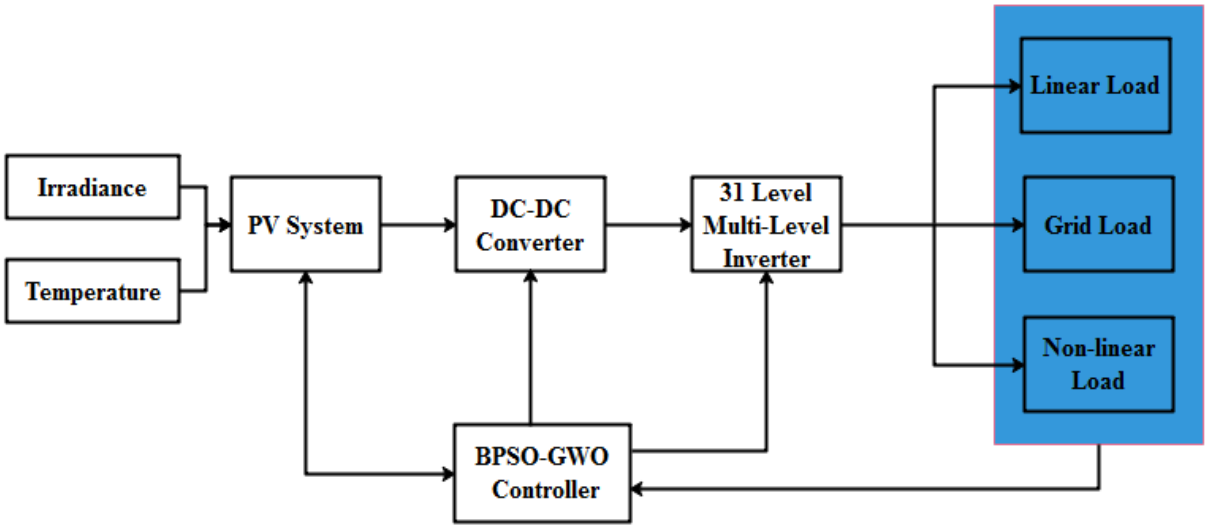

Figure 3.2 Block diagram of the proposed method under various loads.

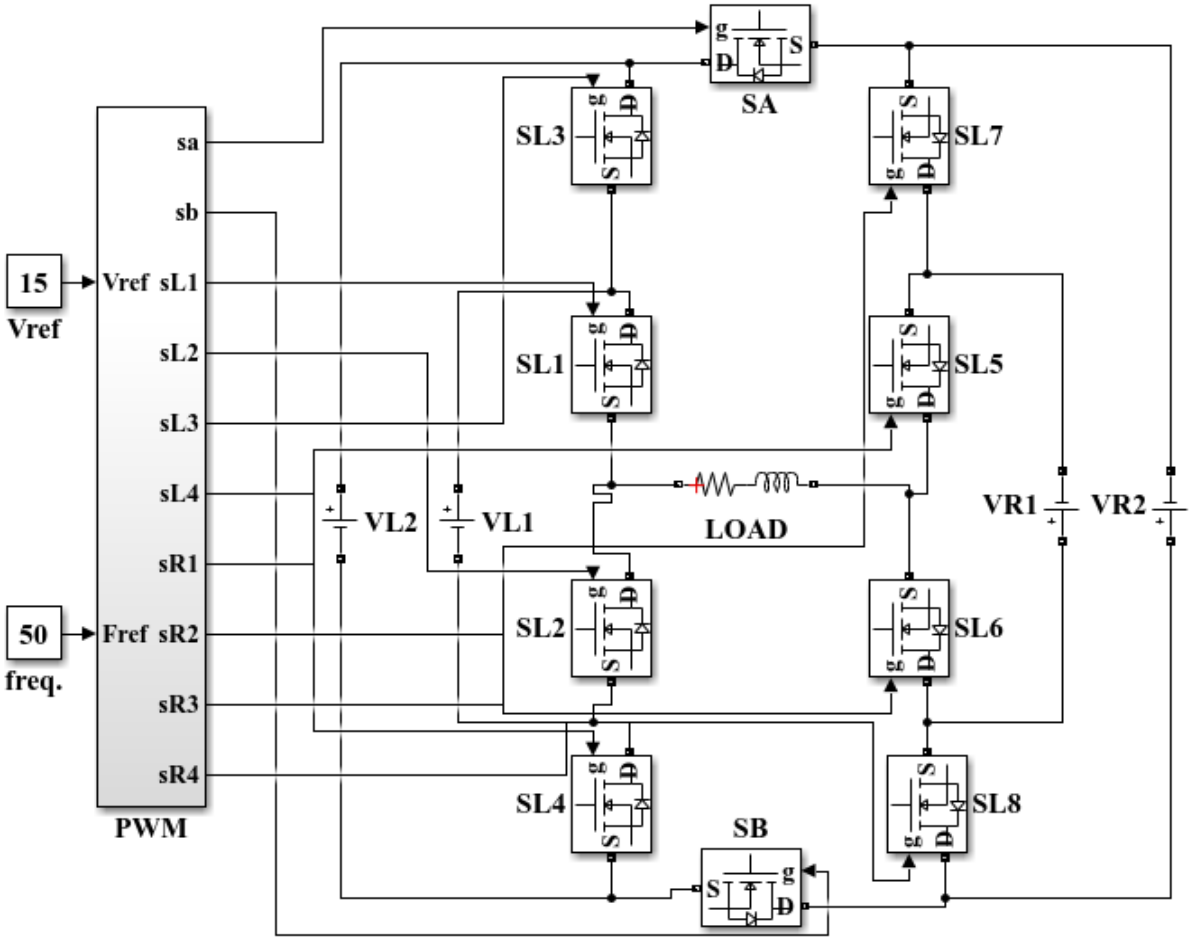

Figure 3.3 Design of 31-level MLI with blocking voltage process.

To maximize power output from photovoltaic panels under non-uniform solar irradiance conditions, like PSCs, a novel evolutionary computing method called grey wolf optimization was utilized to create a global maximum PowerPoint tracking system. When the BPSO–GWO approach was used in a simulation, it was discovered to be highly effective at maximizing the power yield from photovoltaic panels in situations with uneven solar irradiance.

3.5.2. Preliminaries

This study used the suggested BPSO–GWO algorithm to control the DC/AC and DC/DC converters. The method works well for integrating PV into the grid to achieve smooth PQ and is very simple to implement with few adjustment parameters. Additionally, it is a better fitness solution with a fast convergence rate, and the controller's response was examined at both constant

temperature and variable irradiance. The outcomes demonstrate how well the suggested controller enhances system efficiency.

3.5.2.1. Binary Particle Swarm Optimization

Initially, the BPSO method was used to implement the global MPPT technique to address overlapping problems related to partial shading. The PV system's effectiveness rose because the BPSO-based MPPT performance consistently reached the GMPP. The PV power and conversion rate are calculated as the input for BPSO, and output is defined as the change in reference current. The MPPT method is implemented using the GWO algorithm [14]. The combination used to track the PV's GMPP is called BPSO. To maximize the power extracted from the PV setups, the maximum global point is reached using the BPSO. The bit string and particle velocity in BPSO are generated in the interval [0, 1]. The bit chance of obtaining a value of one is the definition of the particle's velocity. The BPSO should be sufficient to improve the efficiency of the distribution system.

$X^i{}_k$ and $V^i{}_k$ denotes the position and velocity at k^{th} iteration, correspondingly. The i^{th} velocity at iteration $k+1$Is considered using Equation (3.1).

$$V^i{}_{k+1} = \omega . V^i{}_k + C1 . R1\ (P_{best} - X^i{}_k) + C2 . R2\ (G_{best} - X^i{}_k) \tag{3.1}$$

Random values are characterized as $R1$ and $R2$; The inertia weight factor is characterized as ω, as stated in Equation (3.1).

k_{max}refers the maximum number of iterations that BPSO takes into account. Additionally, Equation (3.2) illustrates how the particle's position has been modified by adding its previous position and velocity value.

$$X^i{}_{k+1} = X^i{}_k + V^i{}_{k+1} \tag{3.2}$$

Particle swarm expression is preserved, remaining unaltered in BPSO. The modification is achieved by using the logistic transformation $S(V^i{}_{k+1})$, as Equations (3.3) and (3.4) validate.

$$S(V^i{}_{k+1}) = sig\ mod\ e\left(V^i{}_{k+1}\right) = \frac{1}{1+exp(V^i{}_{k+1})} \tag{3.3}$$

If rand $<S(V^{i}{}_{k+1})$ then: $X^{i}{}_{k+1} = 1$; (3.4)

Else: $X^{i}{}_{k+1} = 0$;

Sigmoid limiting transformation is characterized as $S(V^{i}{}_{k})$; quasi-random value designated between $[0, 1]$ which is characterized as $rand$. Figure 3.4 displays the flowchart for BPSO–GWO.

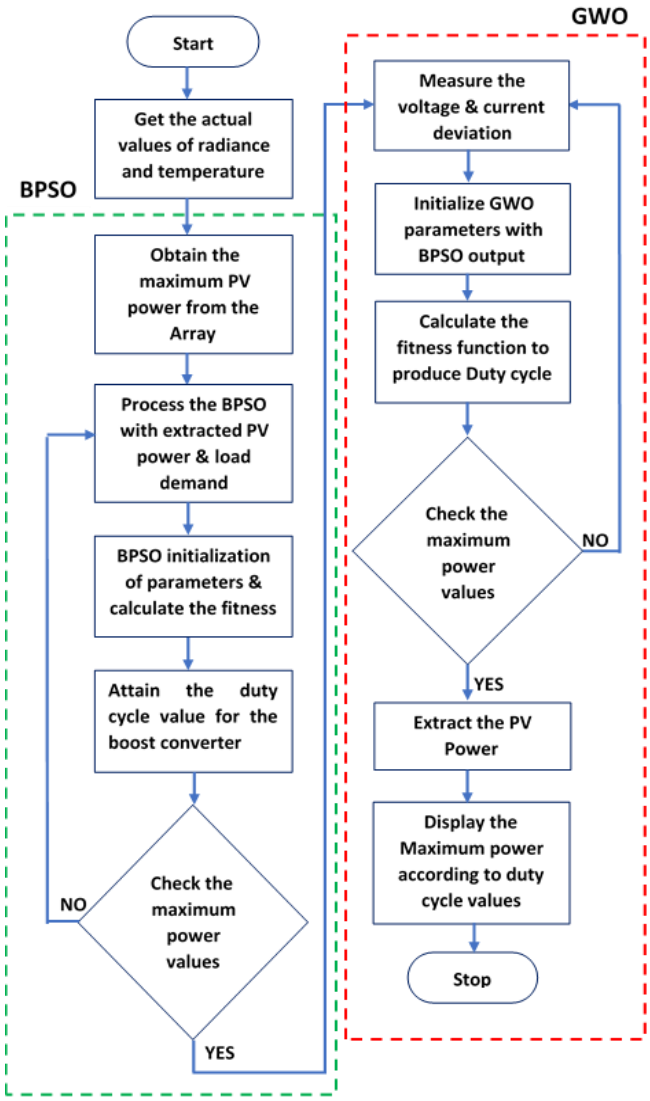

Figure 3.4 Flowchart of BPSO–GWO

3.5.2.2. Grey Wolf Optimization

The GWO method is suggested to solve this obstacle (MPP), tracking the global maximum power point and optimizing the PV system's energy extraction. During incorrect irradiation, the P-V curve is classified by several peaks with different local peaks (LPs) and one global peak (GP). It is interesting to note that wolves' correlated coefficient vectors almost approach zero when they locate the MPP. The proposed method aims to integrate GWO with duty-cycle control. Specifically, it sustains the duty cycle at a constant value at the MPP, mitigating steady-state oscillations in conventional MPPT. This reduces power loss due to fluctuation, leading to increased system efficiency. To apply the GWO-based MPPT, a grey wolf definition is given to duty cycle D.

Generally, GWO is influenced by grey wolves' hunting and leadership styles. The wolves are characterized into four levels, i.e., alpha. (α), beta (β), Delta (δ), and omega (ω). The GWO typically relies on the following presumptions: (1) The optimum, second, and third optimum solutions are indicated by the symbols α, β, and δ, respectively. (2) The omega wolf (ω) is supposed to be the last level. (3) The alpha, beta, and delta wolves are considered the best options since they have more knowledge about the possible location of prey. The three wolves know the prey because the alpha wolf is far more knowledgeable than the other two. (4) The omega wolf follows the three best wolves. One way to think of the global best position ($gbest$) From the AHCS as a prey location vector is [15]. The GWO procedure is described as follows:

A. Encircling prey

Equation (3.5) denotes the encircling performance of grey wolves.

$$Y^{t+1} = Y_p^t - B^t \times \left| D^t \times Y_p^t - Y^t \right| \tag{3.5}$$

Prey's position vector is characterized as Y_p^t, the coefficient vectors are referred to as B^t and D^t, Grey wolf's location vector refers. Y^t. Equations (3.6) and (3.7) are characterized as coefficient vectors of B^t and D^t, Correspondingly.

$$B^t = 2b^t rand_1 - b^t \tag{3.6}$$

$$D^t = 2rand_2 \tag{3.7}$$

The exploration rate is quantified as b^t; $rand_1$ and $rand_2$characterize the random vectors between 0 and 1. The exploration rate is gradually reduced throughout the iterations from 2 to 0. Equation (3.8) specifies the exploration rate.

$$twob_j^t = 2 - \frac{2t}{N_{max}} \tag{3.8}$$

N_{max}Refers maximum iterations.

B. Hunting

The alpha wolf is in charge of managing the hunting process for grey wolves. During the hunting season, the surviving beta and delta wolves occasionally assist as guides. Nevertheless, finding the prey location in a search space is very challenging. The alpha, beta, and delta wolves possess superior intelligence regarding the probable whereabouts of their prey. Grey wolves employ these prey positions to process their hunting behavior. Equations (3.9) to (3.11) encourage the GWO's hunting procedure.

$$Y_1 = Y_\alpha^t - B_1^t \times |D_1^t \times Y_\alpha^t - Y^t| \tag{3.9}$$

$$Y_2 = Y_\beta^t - B_2^t \times \left|D_2^t \times Y_\beta^t - Y^t\right| \tag{3.10}$$

$$Y_3 = Y_\delta^t - B_3^t \times \left|D_3^t \times Y_\delta^t - Y^t\right| \tag{3.11}$$

Y_α^t, Y_β^t, and Y_δ^tThe positions of alpha, beta, and delta wolves are represented correspondingly. Equation (3.12) provides the average positions derived from the alpha, beta, and delta wolves. The average position gives the grey wolf's ideal location.

$$Y^{t+1} = \frac{Y_1+Y_2+Y_3}{3} \tag{3.12}$$

The convergence factor for the GWO is reduced linearly through the number of iterations, from 2 to 0. The PV array's output power likewise varies in tandem with changes in the external atmosphere. The process for tracking the power must be restarted to prevent it from becoming an

endless loop. Equation (3.13) states that the process is re-initialized once the output power difference is satisfied.

$$Absolute \left|\frac{P_{real}-P_m}{P_m}\right| > \Delta P \tag{3.13}$$

Actual output power is quantified as P_{real}, PV output power is characterized as P_m, The threshold for output power change is stated as ΔP (0.2). The duty cycle equation is represented as (3.14):

$$D_i(k+1) = D_i(k) - B^t H^t \tag{3.14}$$

where $D_i(k+1) = new\ duty\ cycle\ value$. Figure 3.5 shows the controller architecture that was created for this PV system. $I_a, I_b, and\ I_c$ The current flow through the three-phase sources is shown in Figure 3.5. The instantaneous shunt voltage at the quadrature axis is stated by V_{IsQ}. The direct axis current Id* is produced by feeding the error between the reference and actual current into the BPSO–GWO controller. Since it controls reactive power, the current Iq* on the quadrature axis is set to zero. Next, the output and actual current fed into the electrical grid are compared.

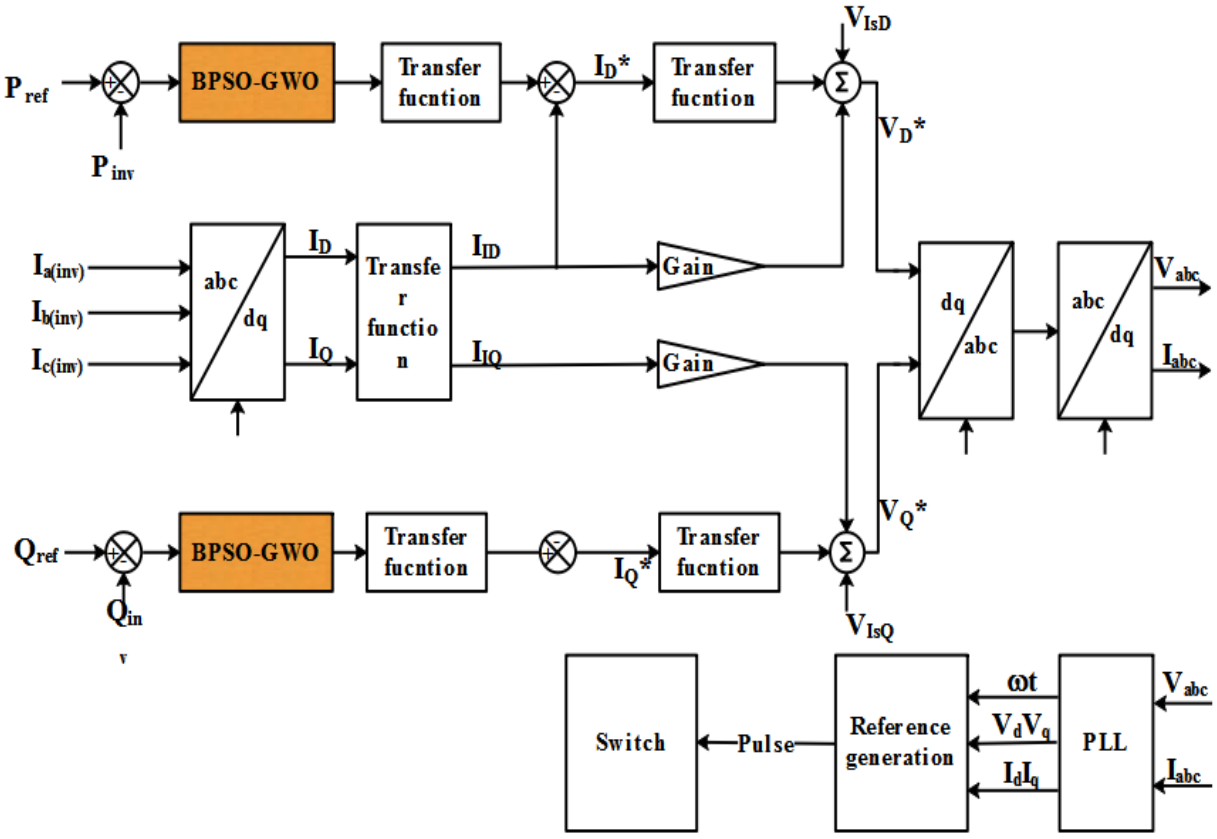

Figure 3.5 The control circuit of BPSO–GWO

As seen in Figure 3.5, the controller's goal is to send all of the PV system's generated active power to the grid while producing zero reactive power to achieve a unity power factor unless the grid operator requests reactive power. Direct axis current Id* is created by feeding the error between the reference and actual current into the BPSO–GWO controller. Reactive power is produced by setting the quadrature axis current, Iq*, to zero. Next, a comparison is made between the output current and the actual current fed into the electrical grid. The current control produces the gate signal linked to the error difference between the two signals. The voltage control loop undergoes the same evaluation procedure. Next, the three-phase voltage and current are synchronized using the Phase Locked Loop (PLL). Switching pulses are generated from the computed voltage and current and are utilized to activate the switches inside the MLI.

C. Fitness Function Source

This section describes how the fitness function for the suggested BPSO-GWO method was derived. Equation (3.15) is the resultant formulation of the fitness function for the proposed algorithm.

$$Pd_k^i > Pd_k^{i-1} \tag{3.15}$$

where P signifies power, d refers duty cycle, $i$refers number of current grey wolves, and $k$refers the number of iterations.

3.6. Results and Discussion

The MATLAB/Simulink platform was utilized to implement the suggested method. Sun Power (SPR 305W) is the name of the designed photovoltaic model used in this study. To extract the maximum power, the PV module uses the suggested BPSO–GWO algorithm to function, and this section shows the simulation's results. The grid-tied PV system was modeled, and the BPSO–GWO was used to analyze the PQ. The boost converter's duty ratio is regulated using the suggested method to improve power quality. The proposed method's Simulink model with the 31-level MLI is shown in Figure 3.6.

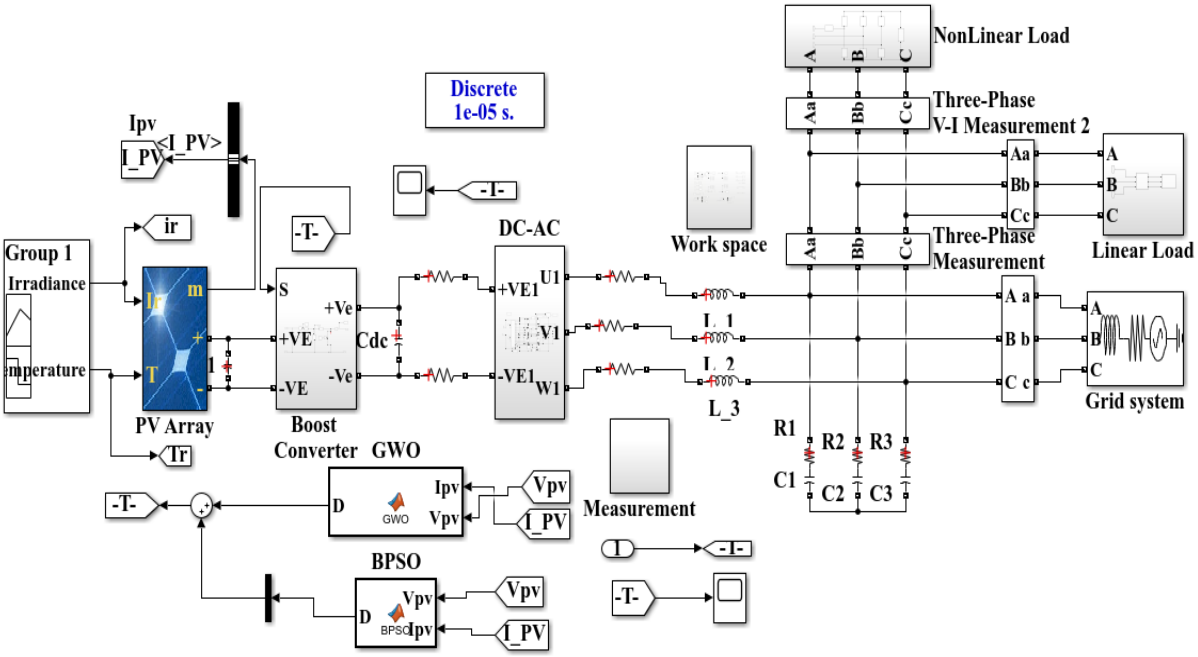

Figure 3.6 Simulink diagram of BPSO–GWO

This paper offers some practical suggestions for enhancing MPPT performance. Even with the implementation of multiple MPPT techniques to date, some improvements in MPPT are still needed to reach maximum efficiency. According to the study's findings, the suggested BPSO–GWO technique performs well under uniform solar irradiation (SI). Figures 3.7–3.9 unequivocally demonstrate that the proposed method obtained the maximum power compared to the other MPPT algorithms in the figures below. The concept of PV power tracking about temperature and irradiance is explained in detail in the statistics; concurrently, the duty cycle values and DC link voltage are shown.

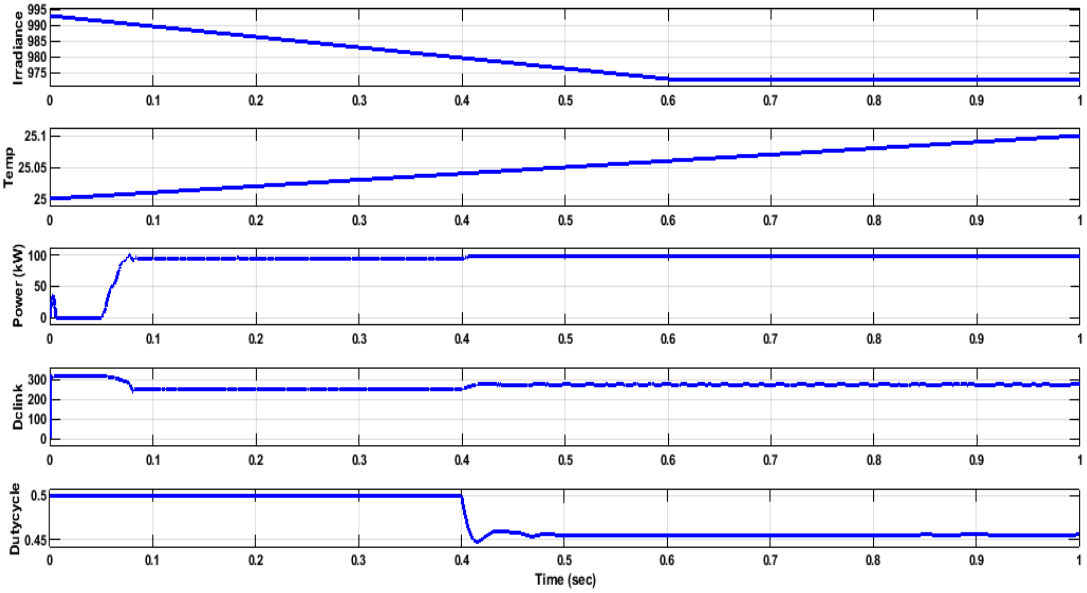

Figure 3.7 PV performance of BPSO

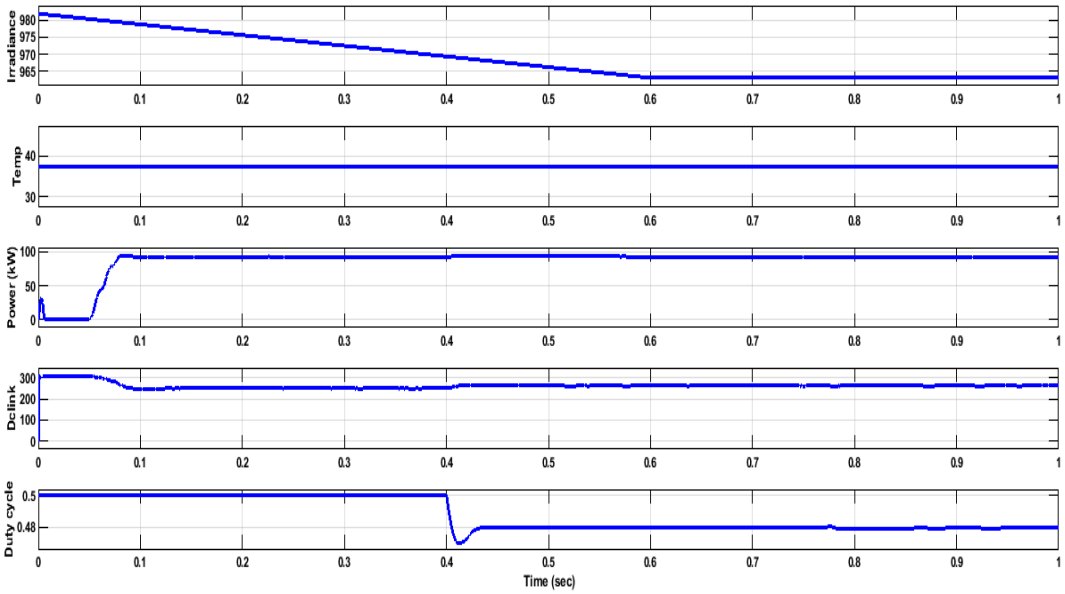

Figure 3.8 PV performance of GWO.

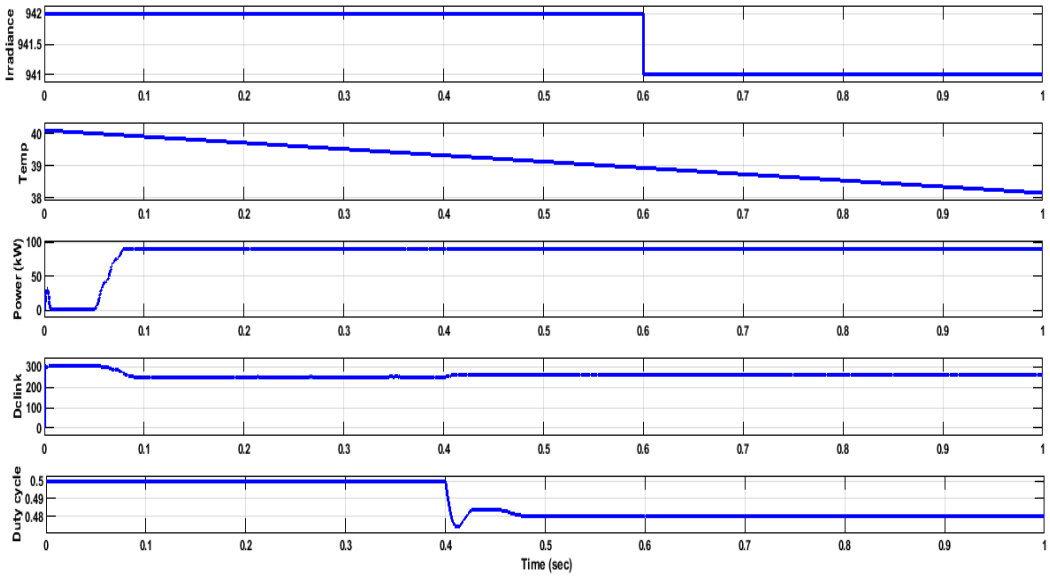

Figure 3.9 PV performance of BPSO–GWO.

Figure 3.10 shows the comparative evaluation of PV power through different techniques. According to Table 3.1, the suggested BPSO–GWO technique outperformed the independently utilized BPSO and GWO techniques, achieving a maximum power of 92.930 kW. Table 4.1 shows that the BPSO and GWO extracted maximum power levels of 88.209 and 90.238 kW, respectively.

Table 3.1 Assessment of PV under linear load.

Methods	**PV Power (kW)**
BPSO	88.209
GWO	90.238
Proposed BPSO–GWO	92.930

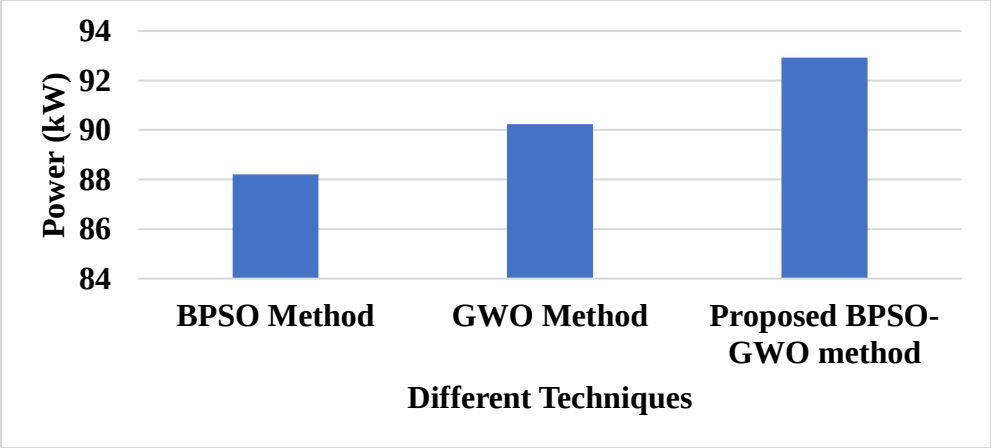

Figure 3.10 THD of 31-level MLI

The output FFT analysis for the PV system under various loads using the BPSO–GWO technique is shown in Figures 3.11 and 3.12. The 31-level MLI with the voltage-blocking process accomplished a 3.70% THD, as shown in Figure 3.11. Under varying loads, a comparable idea paired with the suggested BPSO-GWO achieved a THD of 1.60%. The simulated results obtained from the FFT analysis of the output waveform for grid, nonlinear, and linear loads using BPSO–GWO are shown in the following table. The evaluation of the 31-level MLI using the suggested BPSO-GWO controller is tabulated in Table 3.2.

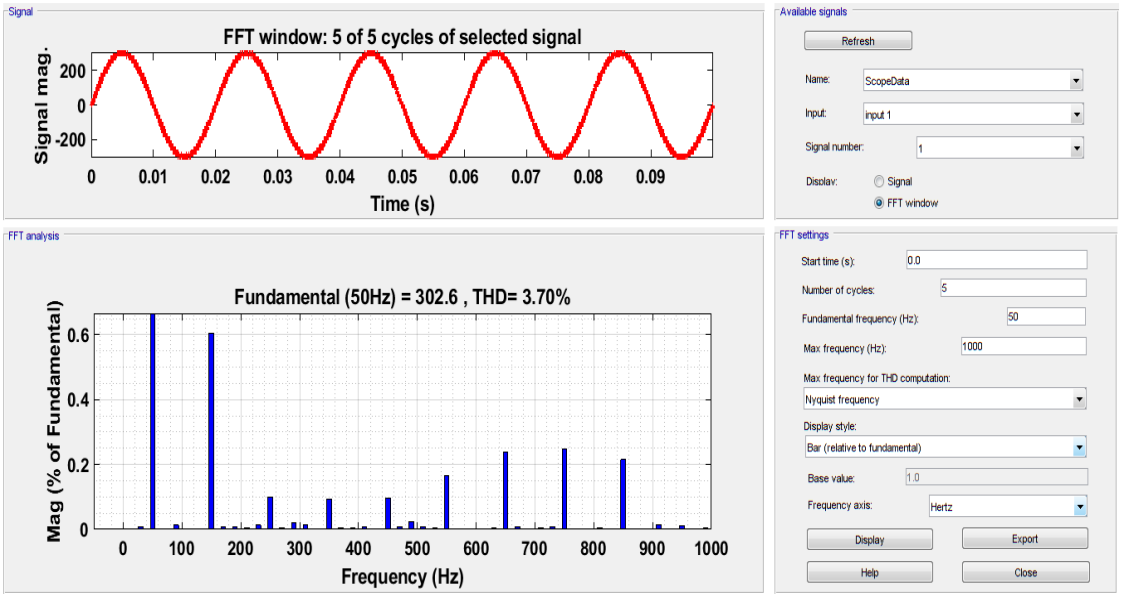

Figure 3.11 THD of 31-level MLI.

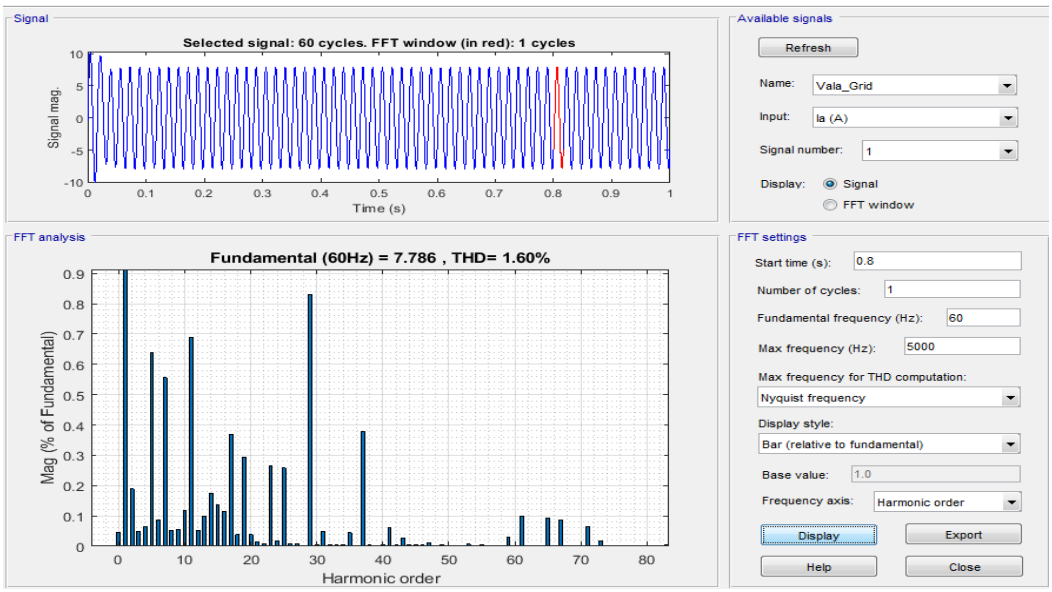

Figure 3.12 FFT of 31-level MLI with BPSO–GWO.

Table 3.2 FFT analysis of the 31-level MLI.

Methods	THD (%)
MLI without a controller	3.70
MLI with hybrid BPSO–GWO	1.60

3.6.1. THD under Linear and Nonlinear Loads

Table 3.3 presents the results of the THD analysis of the 31-level MLI using the suggested BPSO–GWO method under different loads, including linear, nonlinear, and grid loads. The suggested BPSO–GWO method produced a THD of 1.60%, which is significantly higher than that of other currently used techniques like GA (5.13%) and ANN (2.86%).

Table 3.3 Comparison of the FFT analysis.

Methods	THD (%)
GA	5.13
ANN	2.86
BPSO controller	3.12
GWO controller	2.28
Hybrid BPSO–GWO	1.60

The simulation findings indicate that, compared to GA and ANN methods, the suggested BPSO–GWO method accomplished less THD in the 31-level MLI blocking voltage process.

3.7. Summary

The MPPT approach, which dynamically modifies power extraction, must be used in the PV system to determine the maximum power in PV. The hybrid BPSO–GWO combination was presented here, demonstrating that this technique's convergence speed was one of its key features. Due to the faster convergence of the global peak, BPSO was applied in the final phase of this research after GWO had handled the first few stages of MPP tracking. Furthermore, a blocking voltage procedure was incorporated into the design of a 31-level MLI, which lowers the system's overall complexity. The findings showed that the suggested BPSO–GWO method could achieve lower THD (1.60%) than the current techniques. We used the BPSO–GWO method to help us reach a maximum power of 92.930 kW from the solar PV panel.

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b. Using Hybrid Techniques: Adaptive Cuckoo Search Algorithm (ACSA) and Fuzzy Logic Controller (FLC).

RES are widely used to support higher energy demand caused by industrialization and increased population. Due to the widespread use of nonlinear electronic equipment, the issues related to power quality are more in grid-connected PV systems. The power electronic converters inject harmonics into the system, leading to various problems in power quality. In this research paper, a new hybrid method is introduced to enhance the power quality in grid-connected PV systems, and this hybrid method involves the combination of both the Adaptive Cuckoo Search Algorithm (ACSA) and Fuzzy Logic Controller (FLC). ACSA monitors the power extracted from the PV array, which it does with high precision and is more straightforward to operate and control. Moreover, FLC delivers a rapid and effective response. Therefore, the ACSA-FLC combination will increase the performance of MPPT. From the evaluation results, ACSA-FLC minimizes the THD up to 3.64 %, 4.09 %, and 5.62% for 3-level, 5-level, and 27-level MLI, respectively.

3.8. Introduction

RES such as Solar, wind, and hydro are pollution-free, easily erectable, and limitless, so they represent reliable alternatives to conventional energy sources, e.g., oil and natural gas [1]. However, these systems' efficiency and performance are still under development. Among them, PV systems are mainly used as they are light, clean, and easily installable [2]. This system connection to the grid requires special conditions for a high-quality electric power system. This paper presents the interfacing of a three-phase grid-connected PV system. DC-DC boost converter with MPPT is used to extract the maximum power from the sun and transfer it to the grid [3]. In any PV-based system, the inverter is a critical component responsible for controlling electricity flow between the DC source and loads or grid, so a voltage source inverter converts the DC power into AC power before injecting it into the grid [4]. Therefore, to improve the output of power quality of the PV systems, the design and control of the inverter should be done effectively [5]. In grid-connected PV systems, controlling the inverter most properly helps to maintain the unity power factor and deliver proper reactive power compensation to the load [6].

3.9. Contribution

- ACSA-FLC is analyzed under inconstant environmental situations and unexpected deviations of irradiance levels.
- The variation in PV power and its conversion rate denotes the input constraints for FLC, while the change in current value denotes the output constraints.
- ACSA is used to calculate the MPPT value and is utilized to monitor the Global MPP (GMPP) of the PV.
- Here, the ACSA-FLC is proposed to achieve the global peak point that extracts the maximum power from the PV system.

3.10. Proposed method

The general block diagram of a grid-tied PV system is shown in Figure 3.13. Different topologies are available for the grid-connected PV systems and here dual-stage configuration is used. In the dual-stage configuration process, both power conversion stages are convoluted between the PV system and utility grid side. The grid-tied PV structure comprises a PV panel, converter, inverter, and the grid to evaluate the performance of power quality features. In this proposed ACSA-FLC, the boost converter is exploited for the DC-DC stage and the MLI is utilized for DC-AC stage. Nowadays, boost converters are used widely in many industries as they fulfill a variable DC supply requirement. In these systems, boost converters are used to boost the output voltage of the solar panel.

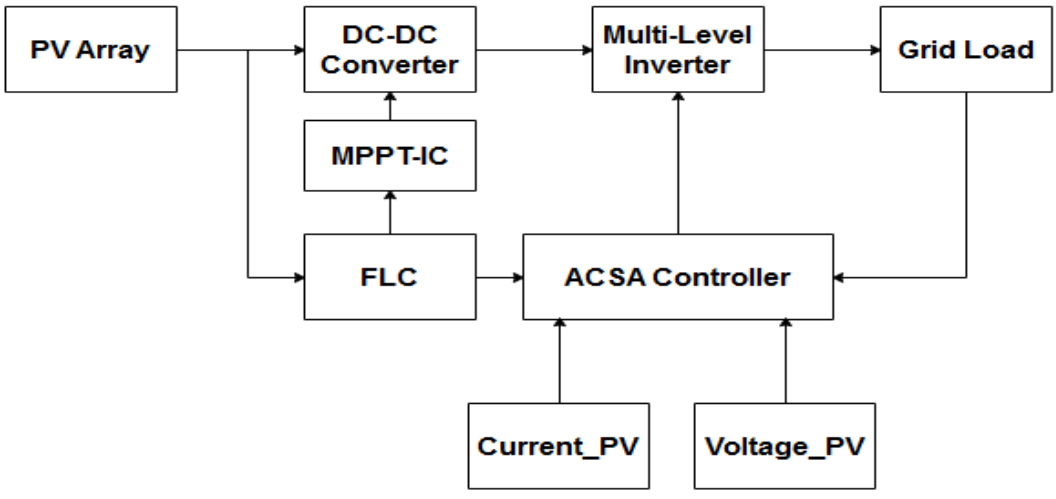

Figure 3.13 Overview of the proposed model

The PV cells generate electric power from the PV radiations, and the output from the PV is DC. The highest power from the PV cells can be extracted from the maximum PowerPoint. However, the effectiveness of the PV cell depends upon the irradiance and cell temperature, which deviates the extracted power from the maximum power. Therefore, this change requires a control technique to track the MPP. The low irradiance can also cause PQ problems in the distribution grid. The power quality also depends upon the inverter topology. In this model, IC is used for MPP tracking.

3.10.1. Incremental Conductance

Among various techniques, the Perturb-and-Observe (P&O) process is a commonly exploited MPPT. However, in this current research, the IC [7] is exploited to track the maximum power point to improve outcomes better than those provided by the P&O [8]. IC entirely depends on the P-V curve and regulates the duty cycle value to modify the PV operating point. This IC is established to overcome the shortcomings of P&O, and then MPP is attained using the connection amongst $\frac{\partial I}{\partial V}$ and$-\frac{I}{V}$, which is stated in equation (3.17).

$$P = V\,I \tag{3.17}$$

Equations 3.18, 3.19, and 3.20 are represented by using the products of equation 3.17 on both sides.

$$\frac{\partial P}{\partial V} = \frac{[\partial(VI)]}{\partial V} \tag{3.18}$$

$$\frac{\partial P}{\partial V} = I\frac{\partial V}{\partial V} + V\frac{\partial I}{\partial V} \tag{3.19}$$

$$\frac{\partial P}{\partial V} = I + V\frac{\partial I}{\partial V} \tag{3.20}$$

At MPP, the eqn. 3.21 is written as

$$\frac{\partial P}{\partial V} = 0 \tag{3.21}$$

Consequently, the eqn. 3.22 is stated as

$$\frac{\partial I}{\partial V} = -\frac{I}{V} \tag{3.22}$$

The above-mentioned condition is utilized to adjust the converter's switching characteristics. MPPT regulates the PWM pulses until the condition is fulfilled. For this reason, the voltage of PV must be reduced to attain the peak point from the MPPT curve.

3.10.2. Fuzzy Logic Control

The theory of FLC depends on the model related to binary logic values (0,1). Every value has fractional memberships and is deliberated through a definite proportion. The results of FLC produce the value of the direct duty cycle (D). MPPT is attained when FLC modifies the D value of PWM to produce proper switching pulses for the Integrated Gate Bipolar Transistors (IGBT) device of a boost converter. FLC is a nonlinear controller that does not need exact mathematical modeling and consists of three parts: fuzzification, rule base, and defuzzification. In the fuzzification stage, the inputs are changed into fuzzy values. The rule base is a set of rules which gives the relation between input and output [9]. It is also called the black box of the FLC. Finally, in the defuzzification stage, the fuzzy values are converted to non-fuzzy values, which control the PV system.

3.10.3. An adaptive Cuckoo search algorithm

ACSA [10] consists of two key constraints: a direct exploration that depends on Levy flights and a random exploration that relies on the probability of a host bird determining an alien egg in the nest. The host bird recognizes unhealthy eggs through a probability constraint arrested number (n), discovery rate (pa), and levy coefficient λ. The cuckoo indiscriminately selects the position of the nest to place eggs via equations (3.23) and (3.24).

$$X_{pq}^{gen+1} = X_{pq}^{gen} + S_{pq} \times Levy(\lambda) \times \alpha \tag{3.23}$$

$$Levy(\lambda) = \left| \frac{\Gamma(1+\lambda) \times sin\left(\frac{\pi \times \lambda}{2}\right)}{\Gamma\left(\frac{1+\lambda}{2}\right) \times \lambda \times S^{(\lambda-1)/2}} \right|^{1/\lambda} \tag{3.24}$$

where λ is constant $(1 < \lambda \leq 3)$; random number generated between $[-1,1]$ is expressed as α; The gamma function is stated as Γ; Step size is taken as S > 0.

The optimal step size is attained by equation (3.25).

$$S_{pq} = X_{pq}^{gen} - X_{fq}^{gen} \tag{3.25}$$

where p, $f\epsilon\{1,2,\ldots.,m\}$ and q$\epsilon\{1,2,\ldots.,D\}$Or randomly chosen indexes, f is chosen randomly, but its value must differ from p. When the host bird finds the cuckoo egg, it selects the particular egg value with probability using equation (3.26).

$$pro_q = \left(\frac{0.9\times fit_q}{\max(fit)}\right) + 0.1 \tag{3.26}$$

where fitness value is specified as fit_q; q is specified as the proportionality index present in the nest position q. If the host bird recognizes the cuckoo egg, it will toss it outside and establish a new nest using equation (3.27). Otherwise, the egg will propagate and be prosperous for the succeeding group.

$$nest_q = X_{q,min} + rand(0,1) \times (X_{q,max} - X_{q,min}) \tag{3.27}$$

Figure 3.14 illustrates the control circuit diagram for the proposed ACSA-FLC. The exploited duty cycle value is used to break the transient situation to decide, and the developed result will raise the tracing time at the MPP.

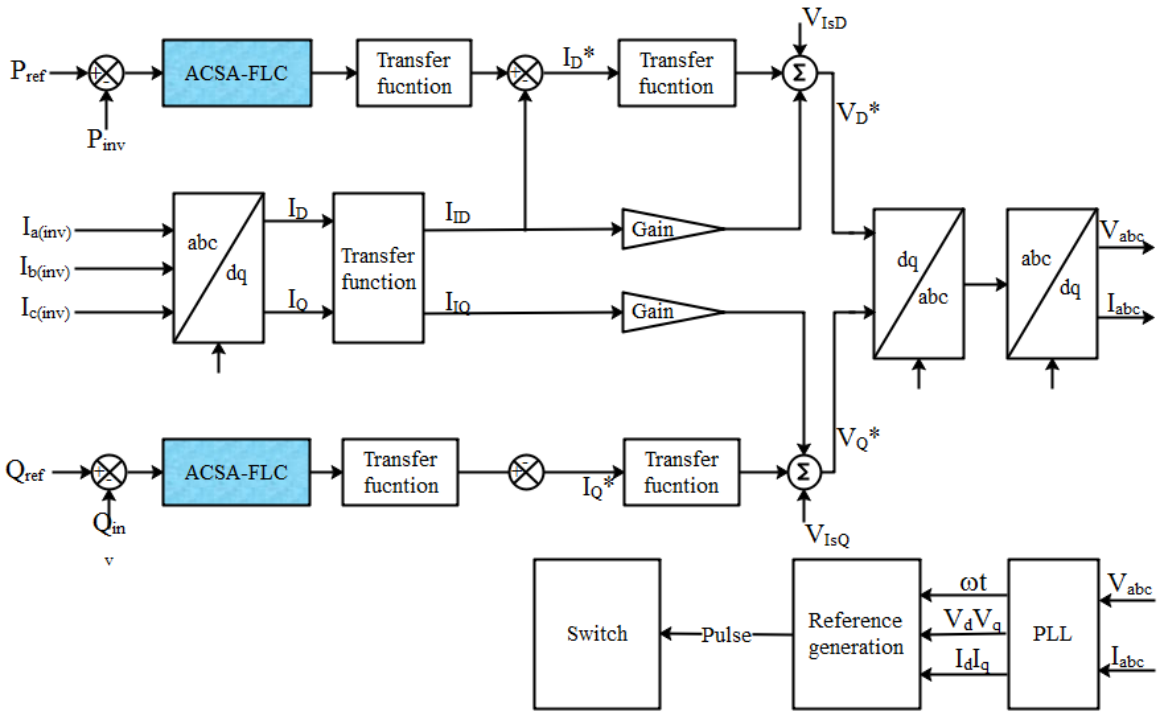

Figure 3.14 Control Circuit Diagram

3.11. Results and Discussion

This section presents the experimental tests of the PV system operating with the MPPT based on the PSO. This section presents the simulation outcomes associated with the PV system operating with ACSA-FLC, designed with a PV model named Sun Power (SPR 305W). PV cells are utilized to create a PV array using MATLAB, as shown in Fig. 3.15. The probability and proficiency of the proposed system are calculated based on PQ development.

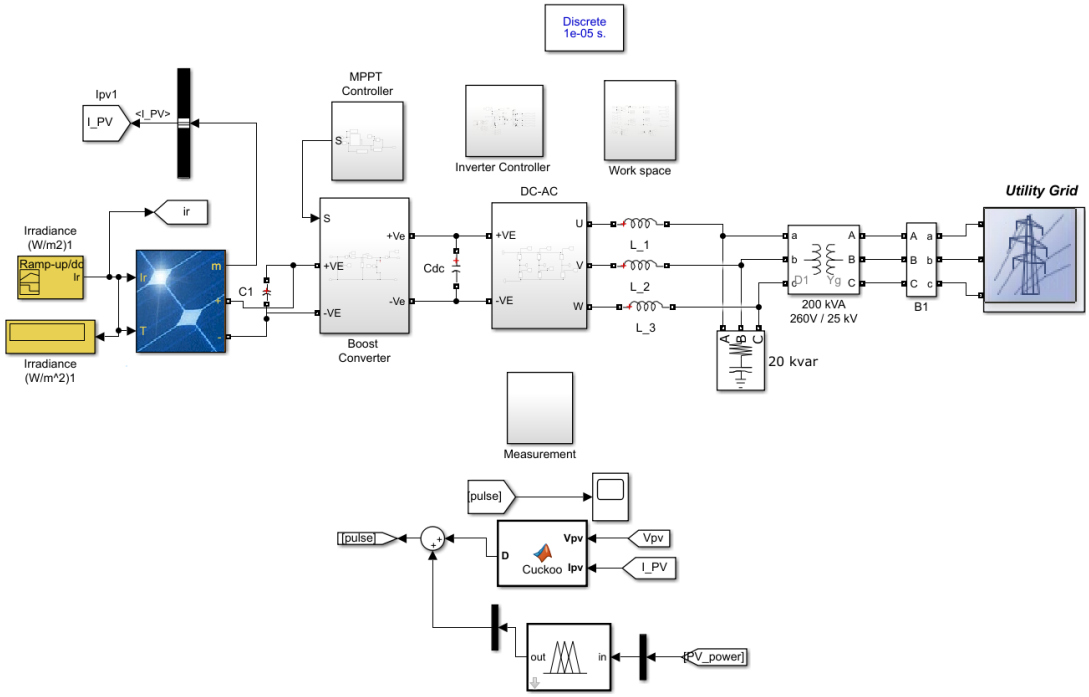

Figure 3.15 Simulink design of ACSA-FLC

ACSA-FLC regulates the converter's duty ratio to enhance power quality. This proposed process's efficiency is tested by changing the levels of irradiation and cell temperature.

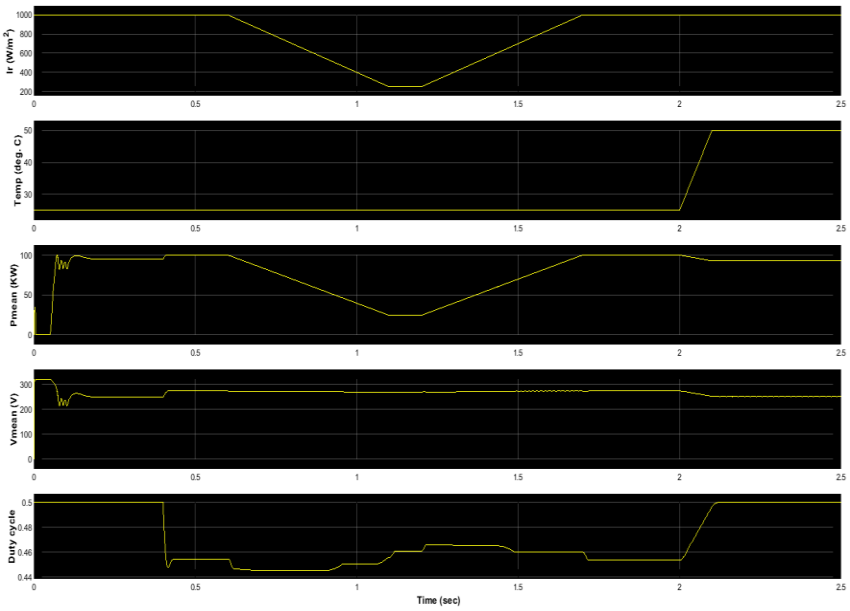

Figure 3.16 Duty cycle and PV power at different conditions

Fig. 3.16 examines the behavior of the proposed method when the PV's irradiation value is changed, demonstrating the resultant AC power produced by the modelled PV system while varying the solar irradiation level.

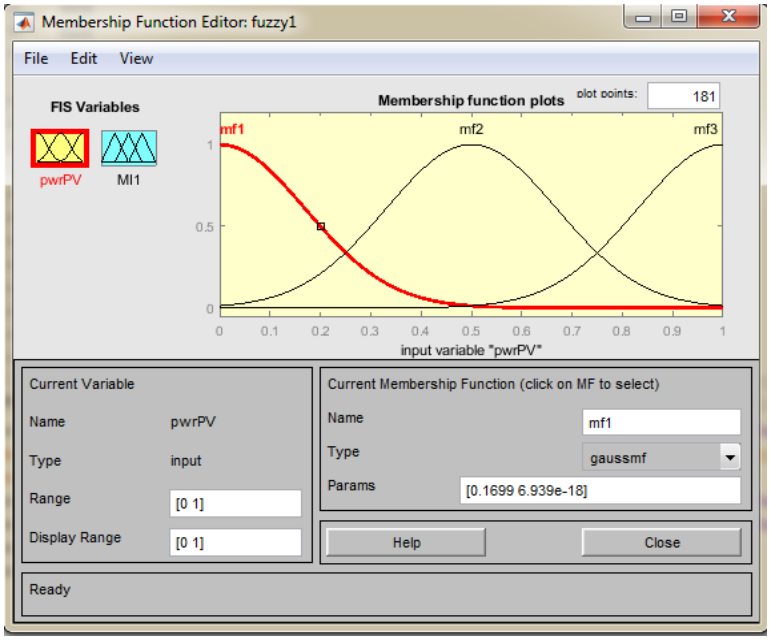

Figure 3.17 Input membership function

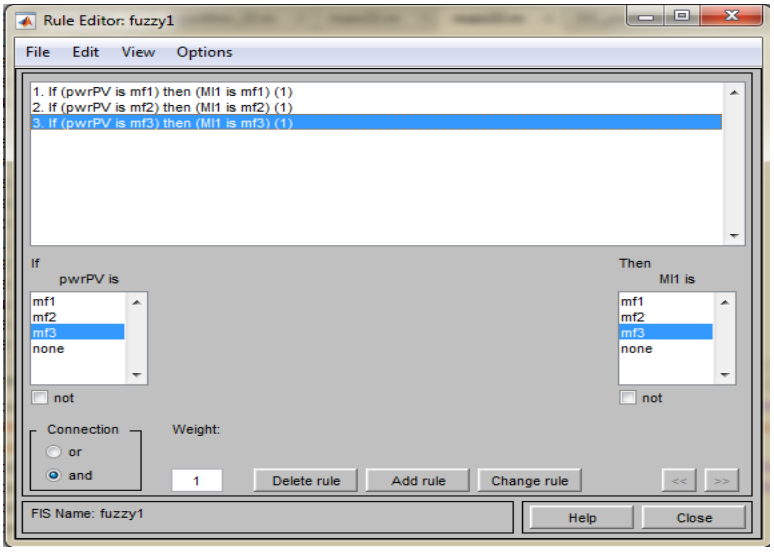

Figure 3.18 Fuzzy rules dialogue box

In this work, a fuzzy controller with a single input and single output was designed. The power from PV is given as input to FLC, and the modulation index is used to control the boost converter from which the output is extracted. The value of the modulation index will be between 0 and 1. The Gaussian membership functions were used in the fuzzification stage. The membership function of input PV power is shown in Fig 3.17.

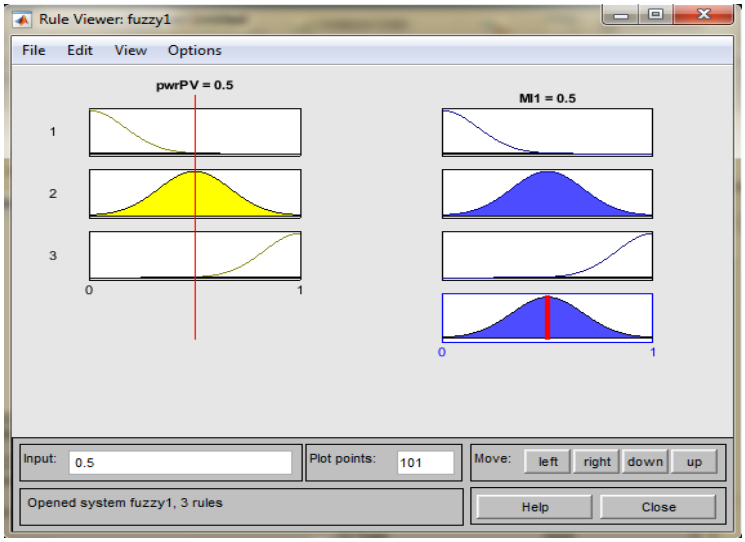

Figure 3.19 Rule viewer dialogue box

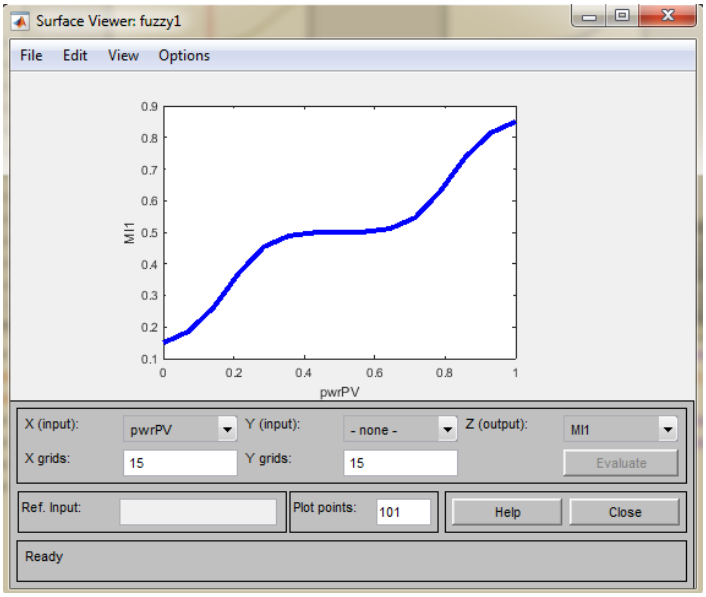

Figure 3.20 A surface viewer of modulation index

Using the input PV power and output modulation index, FLC provides three membership functions defined in Figure 3.17. The maximum range of PV power for the modulation index is (0 to 1), and all three fuzzy rules are applied to the controller. The rule and surface viewer are given in Figures 3.18 and 3.19, respectively. Finally, the modulation index value will be used to modify the duty ratio of the boost converter. Figure 3.20 demonstrates the modulation index value generated by the FLC.

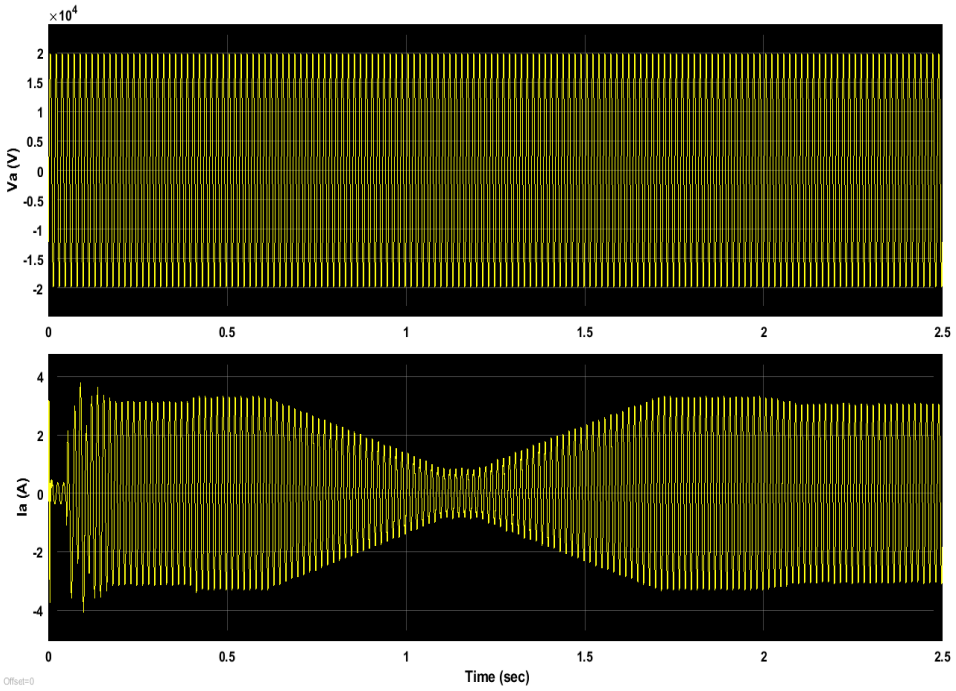

Figure 3.21 Performance of grid

Various performance parameters, such as PV power, duty cycle, and load demands, are investigated under different circumstances to verify the PQ enhancement. The utility grid constraints are specified in Fig 3.21, and the extracted power from the PV is demonstrated in Fig 3.22.

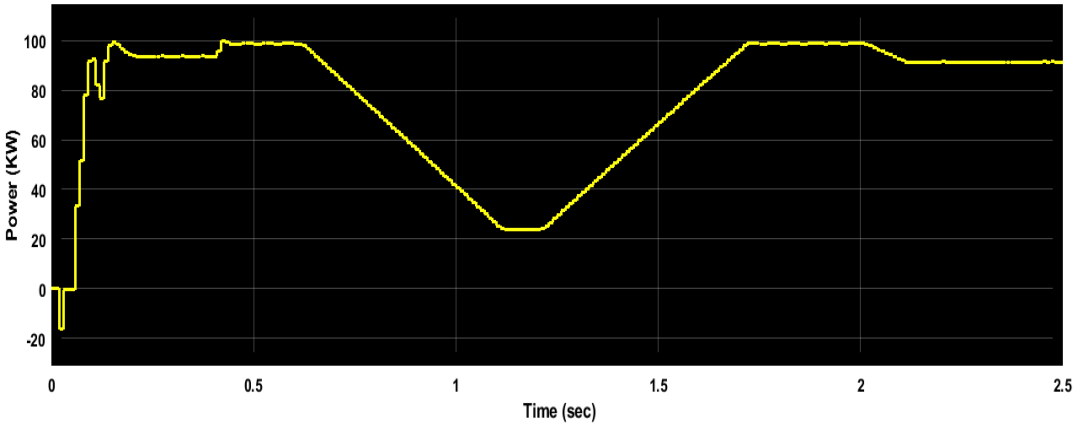

Figure 3.22 Extracted PV Power

The harmonic analysis of load side current is completed in dissimilar circumstances, and the extent of the analysis is specified in Fig 3.23.

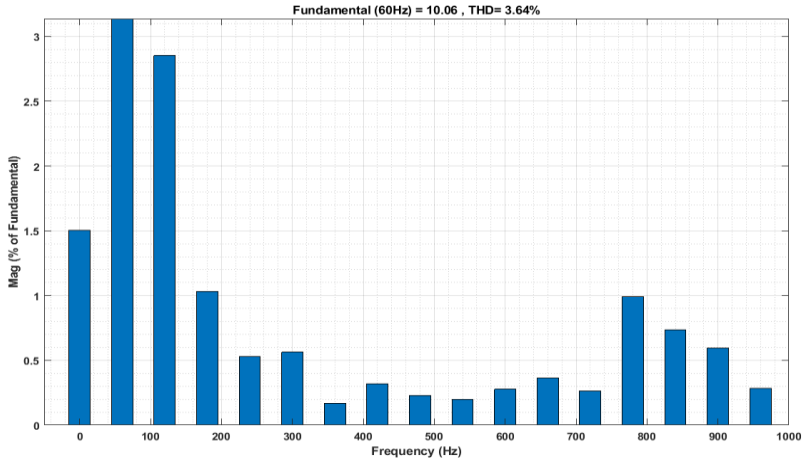

Figure 3.23 THD measurement of 3-level MLI

Furthermore, the FFT analysis of the inverter output current is given in Fig. 3.23, which shows that the current's THD level is 3.64%. The performance of the ACSA-FLC was validated using a comparative analysis with some existing techniques. The following results characterize ACSA-FLC as a promising methodology for PQ improvement in PV systems under grid-side faults. The proposed ACSA-FLC provides better results than the other existing techniques, as mentioned in Table 3.4. Figure 3.24 illustrates the THD measurement of 5-level MLI.

Table 3.4 Assessment of THD for 3-level MLI

Approaches	**THD (%)**
ANN-PI	8.44
Improved IC-MPPT	17.95
PI	12.86
RBFNN	4.81
ACSA-FLC	3.64

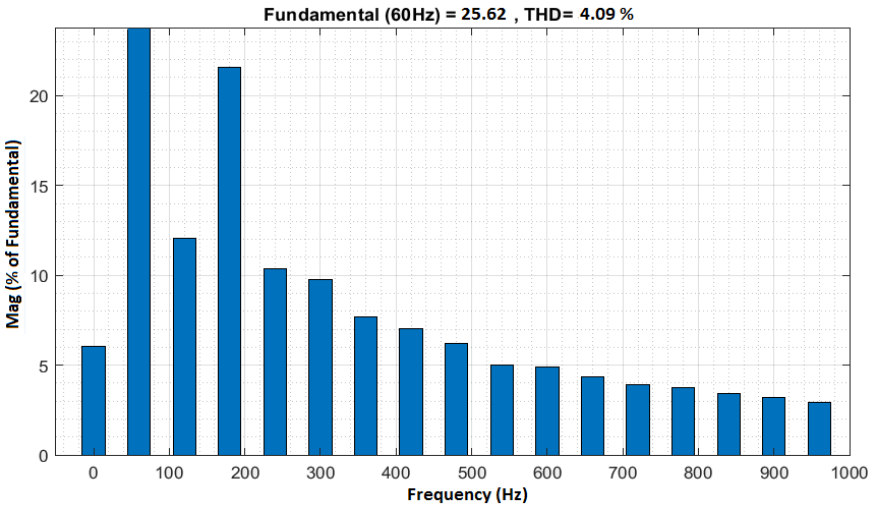

Figure 3.24 THD measurement of 5-level MLI.

Table 3.5 Assessment of THD for 5-level MLI

Approaches	**5-level MLI**
ANN-PI	8.44
Improved IC-MPPT	4.18
PI	12.86
RBFNN	4.81
ACSA-FLC	4.09

The comparison tables 3.4 and 3.5 display the harmonic error values of 3-level and 5-level MLI of the proposed ACSA-FLC and the existing methods RBFNN and PSPWM. Compared with the existing techniques, ACSA-FLC successfully improves the features of PQ.

Table 3.6 Assessment of THD for 27-level MLI

Approaches	**27-level MLI**
PSPWM	17.14
PSPWM and Modified SOPWM	6.59
ACSA	6.05
FLC	5.87
ACSA-FLC	5.62

Table 3.6 shows that ACSA-FLC achieves better results and has demonstrated the ability to operate very actively and robustly under a variety of circumstances. Figure 3.25 displays the THD values for the 27-level MLI, and Table 3.6 presents a comparative analysis of THD for different MLI levels using both existing and proposed techniques.

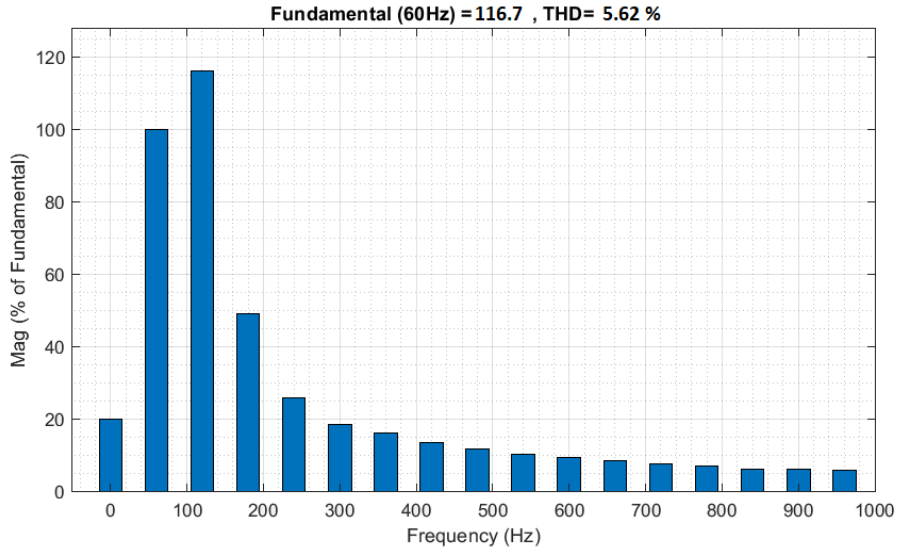

Figure 3.25 THD of 27-level MLI.

In the earlier techniques, the ANN-PI was used to improve PQ features. While the THD was reduced to 8.44% by the ANN-PI, the harmonics were only condensed up to 12.86% by the conventional PI. Simultaneously, the suggested ACSA-FLC decreased the THD to 3.64%, a significantly better optimal reduction than previous methods. Table 3.7 concludes that, compared to PI and ANN, the suggested ACSA-FLC controller achieves significantly lower THD in all MLI levels.

Table 3.7 Evaluation of THD by different MLI

Techniques	**3-level MLI**	**5-level MLI**	**27-level MLI**
ACSA	4.59	5.02	6.05
FLC	4.01	4.18	5.87
ACSA-FLC	3.64	4.09	5.62

3.11.1. Comparative Analysis

3.11.1.1. Study of Linear Load:

The extracted PV power obtained using the suggested technique is displayed in Figures 3.26, 3.27, and 3.28. The figures also show performance metrics like duty cycle and voltage.

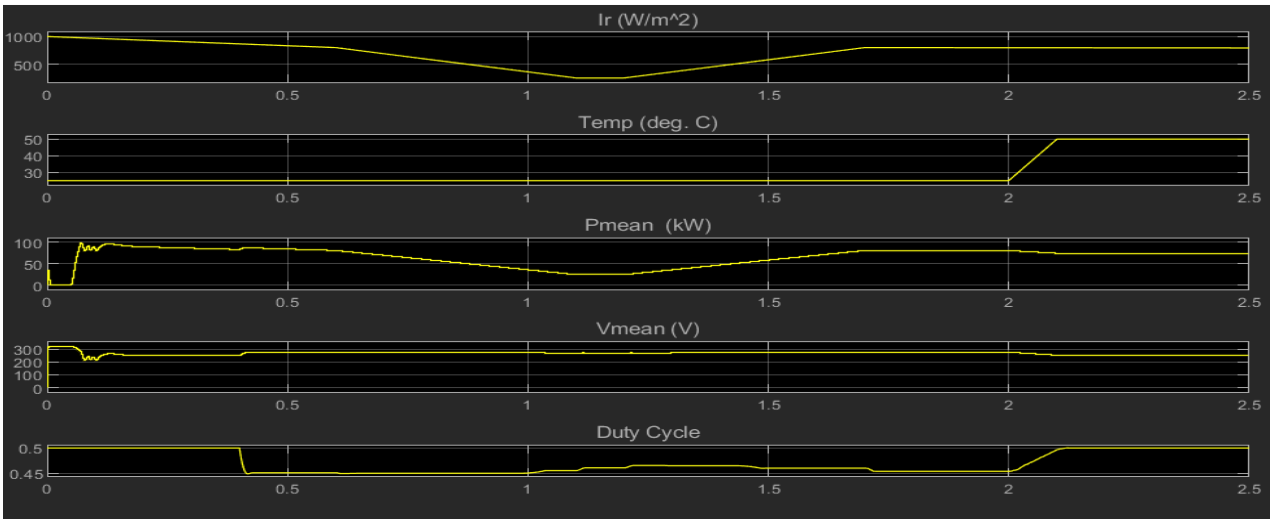

Figure 3.26 PV performance using ACSA

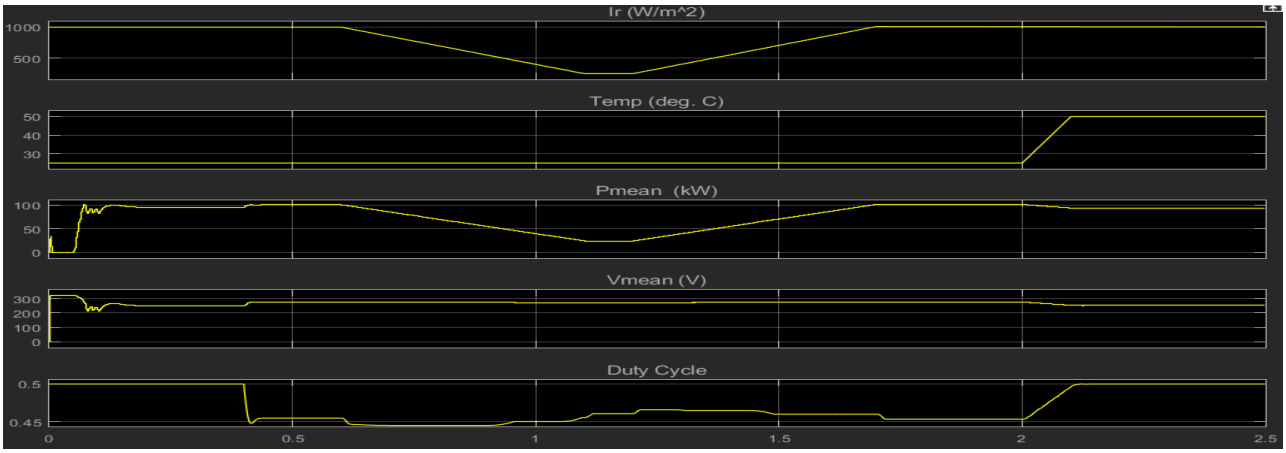

Figure 3.27 PV performance using the FLC method

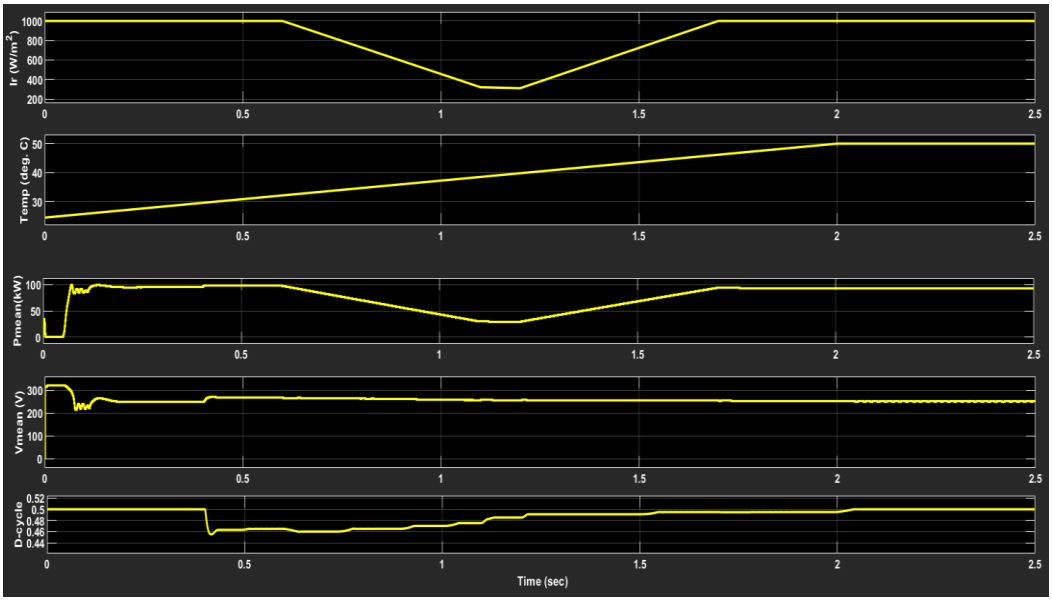

Figure 3.28 PV performance using ACSA-FLC

Table 3.8 analysis makes it abundantly evident that the suggested ACSA-FLC achieves a maximum power of 91.10 kW, significantly more than the maximum power of 74.22 kW and 80.36 kW that the separately tested ACSA and FLC achieved.

Table 3.8 Assessment of PV Power

Method	PV Power (kW)
ACSA	74.22
FLC	80.36
ACSA-FLC	91.10

3.11.2. Study of THD on Linear Load

Comparison tables 3.9 and 3.10 clearly show that the ACSA-FLC controller's error harmonics outperform the current techniques by a wide margin. Using the ACSA-FLC, PQ's features are successfully enhanced, which was not achievable with other approaches at the time.

Table 3.9 THD comparison for 3-level MLI

Method	THD (%)
ACSA	4.22

FLC	3.98
ACSA-FLC	**3.07**

Table 3.10 THD analysis with existing method

Techniques	**THD (%)**
IC-MPPT	17.95
ACSA-FLC	**3.07**

3.11.3. Study of Non-Linear Load

Figures 3.29, 3.30, and 3.31 below illustrate the extracted PV power obtained using the suggested method. These figures also prominently display performance values like voltage and duty cycle values.

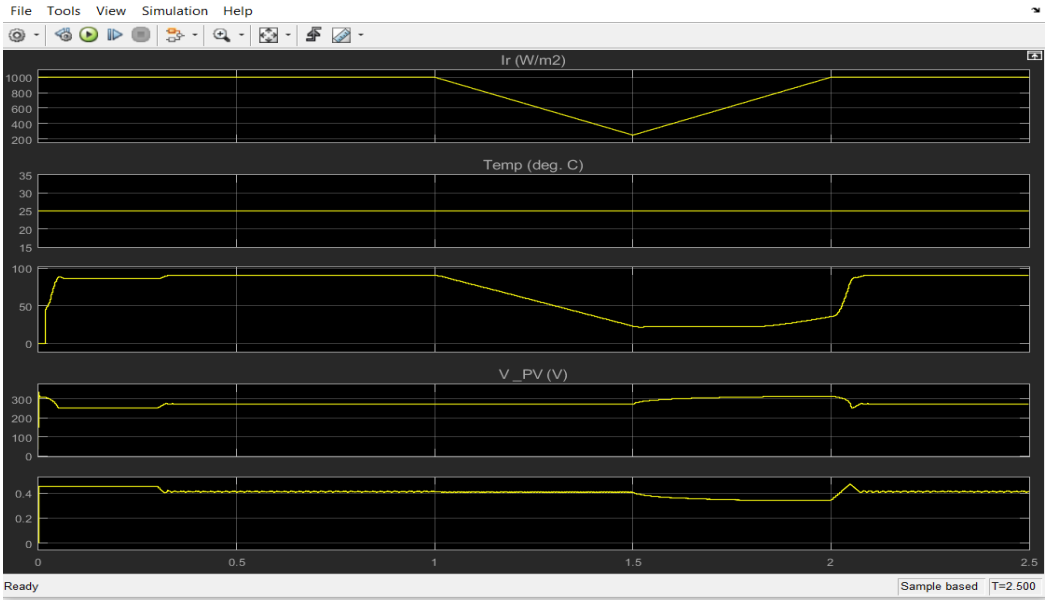

Figure 3.29 Performance of PV using ACSA

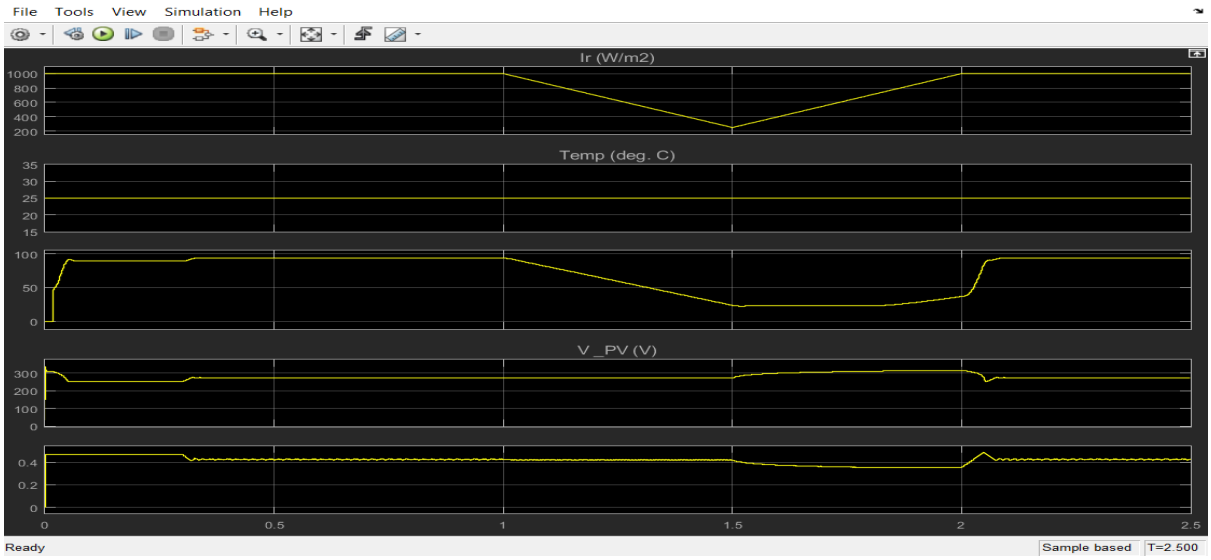

Figure 3.30 Performance of PV using FLC

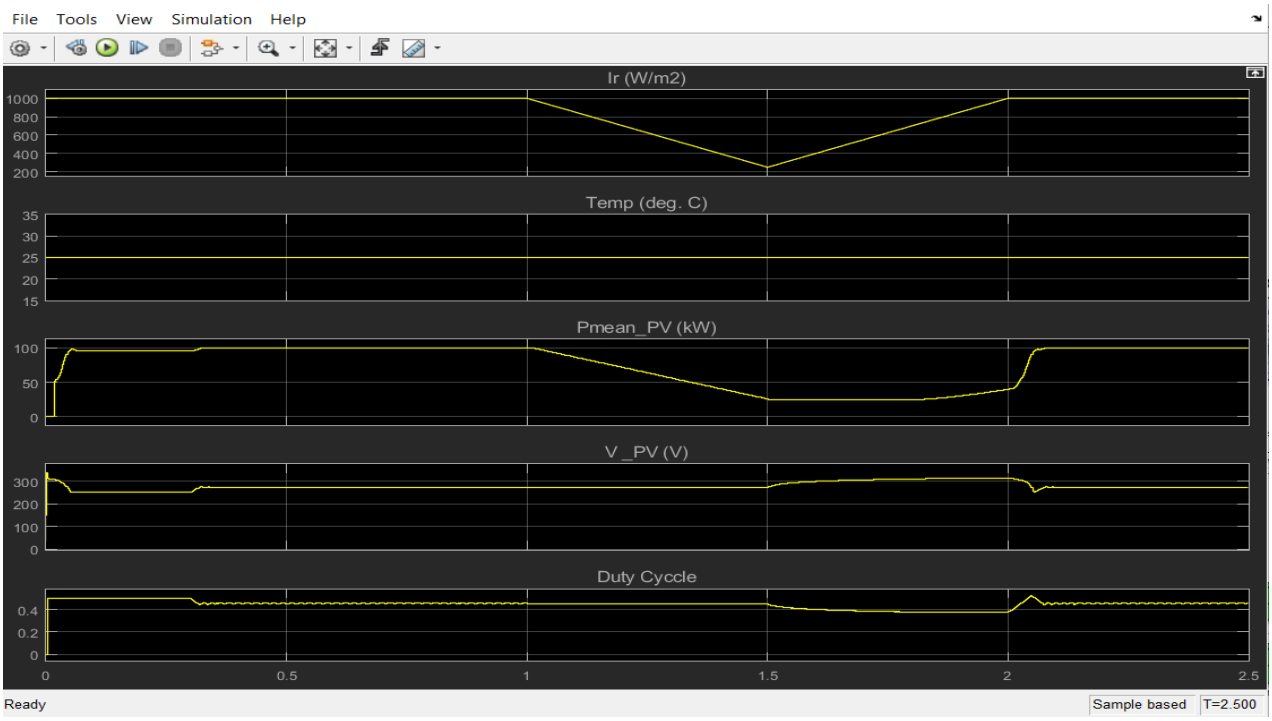

Figure 3.31 Performance of PV using ACSA-FLC

Table 3.11 analysis indicates that the suggested ACSA-FLC accomplishes a maximum power of 97.47 kW, significantly more than the maximum power of 88.281 kW for FLC and 86.29 kW for the separately tested ACSA.

Table 3.11 Evaluation of PV Power

Method	PV Power (kW)
ACSA	86.29
FLC	88.281
ACSA-FLC	97.47

3.11.4. THD Study on Non-Linear Load

Table 3.12 analysis shows that the proposed ACSA-FLC achieves a maximum THD reduction of 3.34%, which is significantly better than the 4.19% THD reduction for the separately validated ACSA and 3.93% for the FLC.

Table 3.12 THD comparison of non-linear load

Method	THD (%)
ACSA	4.19
FLC	3.93
Hybrid ACSA-FLC	3.34

3.12. Summary

In this study, the quality of output power extracted from the PV system is improved by combining FLC and ACSA. By considering the PV power and load demand, the ACSA and FLC both produce a modulation index. To control the boost converter's duty ratio and enhance power quality, the modulation indices are derived from the ACSA algorithm and fuzzy controller. The THD level reduction results from the current RBFNN are 4.81%. However, the suggested method's power quality improvement allowed the THD to be reduced to 3.64 %, 4.09 %, and 5.62 % for 3-level, 5-level, and 27-level MLI, respectively. These are significantly better THD level reduction results than RBFNN and all other currently used methods. The results show that the ACSA-FLC reduces THD, PV power, and grid voltage/current. Compared to current controllers like RBFNN and IC-MPPT, the suggested approach produces output power of higher quality and performs better.

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Chapter 4

Energy Management of Grid-Connected Hybrid System using Golden Eagle Optimization with Incremental Conductance

Normally, PV uses solar energy conversion to produce electrical energy. A charging controller is necessary when using photovoltaics to maximize PV performance. The MPPT and DC-DC converter are the two components that make up the charging controller. To achieve the PV's peak power, a DC-DC converter is utilized to adjust the output voltage of the solar energy system. These days, RES is applied far more widely to support and meet the increased energy needs brought on by population expansion and industrialization. The increasing number of power system users and the erratic nature of the electric load make meeting the massive power demand difficult for electric utilities and system operators. Thus, power demands have built up over time and threaten the system's operation. Golden Eagle Optimization with Incremental Conductance (GEO-INC), an efficient Energy Management System (EMS), is suggested to satisfy the load demand. Three distinct systems are needed to create an efficient EMS: a battery, a wind turbine, and a PV module. The suggested technique efficiently regulates the transition between the wind turbine and the battery storage system while drawing more power from the PV panel. The proposed method achieves 1.98% distortion from the results, less than the current methods.

4.1. Introduction

These days, growing environmental concerns about the wasteful use of fossil fuel-derived electricity have focused on how important it is to produce electricity from environmentally friendly renewable energy sources like solar and wind [1]. Because solar energy is widely available, flexible in terms of system size, and able to provide both on- and off-grid solutions, it plays a significant role in meeting the needs of various nations [2]. A PV installation is usually static and requires no cooling systems, solid and tall towers, or vibration [3]. To maximize the output power from the PV array using an MPPT algorithm, it is necessary to implement an intermediate conversion stage that interfaces the PV array with the power system [4]. Numerous studies have been conducted in the literature to maximize power MPP extraction, control reactive and active

power, and improve power quality by lowering harmonic current distortion [5]. The literature presents a variety of MPPT techniques [6]. Perturb & Observe (P&O), the most popular MPPT method, is employed for its straightforward implementation, quicker MPP tracking, and other financial benefits [7].

4.2. Problem Statement

This section outlines the current problems facing the EMS and explains how the suggested methodology resolves them.

- The issue with the EMS is that, because of the high cost of the system and the storage subsystem, using a single renewable energy source, like solar or wind power, is not enough to meet demand over extended periods.
- System performance has decreased due to improper parameter selection in the RES material and design, as well as limitations regarding load, generator, battery, converter, and cost function.
- The ideal number of features to utilize the standard hourly data could not be provided without outages over a year due to constantly fluctuating hourly and daily weather circumstances.

4.3. Proposed Methodology

Figure 4.1 shows the block diagram of the grid-connected RES using the suggested GEO-INC.

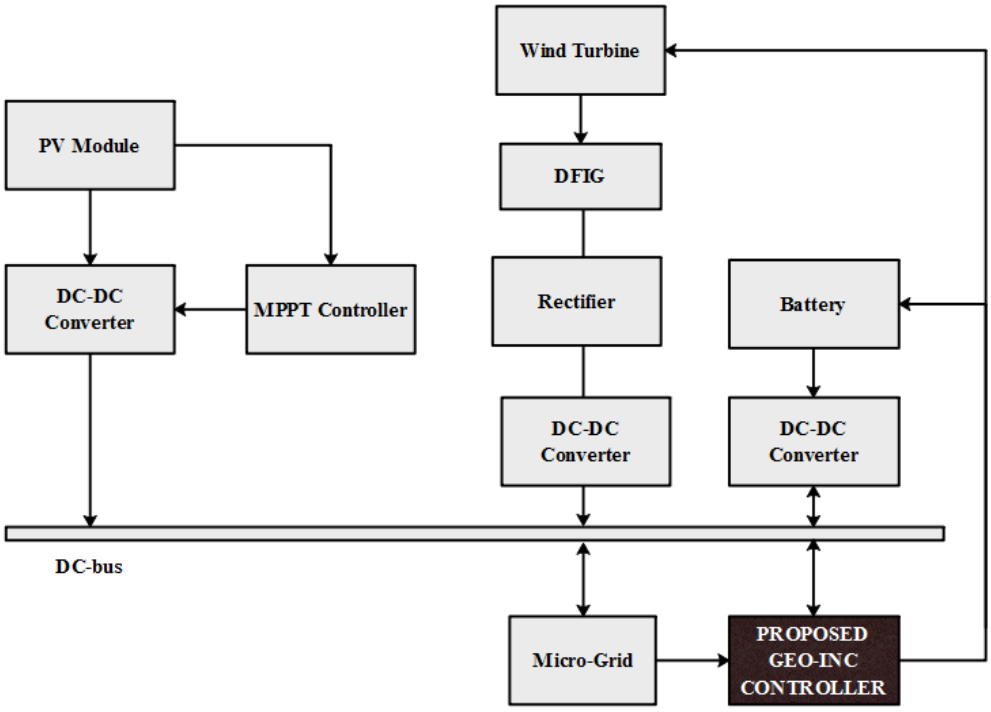

Figure 4.1 Block Diagram of proposed GEO-INC

This diagram shows that the suggested controller receives the grid's load demand and input power from the three. This gives the control variables the necessary unpredictability during processing the input values, making them appropriate for the MPPT study. The suggested controller determines those control variables, generates the proper duty cycle, activates the multi-level inverter, and extracts the maximum power.

4.3.1. Golden Eagle Optimization (GEO)

This subsection describes the suggested mathematical method for modeling the movements of golden eagles [8, 9] as they hunt for prey. Equation (4.1) can be utilized to estimate the golden eagle's attack vector.

$$\overrightarrow{A_\iota} = \overrightarrow{X_f} - \overrightarrow{X_\iota} \tag{4.1}$$

Eagle ιattack vector is specified as $\overrightarrow{A_\iota}$; Best position is shown as$\overrightarrow{X_f}$; the current location is designated as$\overrightarrow{X_\iota}$. In $j$dimensional space, equation (4.2) displays the scalar form of the hyperplane.

$$h_1x_1 + h_2x_2 + \cdots .. h_nx_n = d \rightarrow \sum_{j=1}^{n} h_jx_j = d \tag{4.2}$$

$$\sum_{j=1}^{n} a_j x_j = \sum_{j=1}^{n} a_j^t x_j^* \quad (4.3)$$

Using Equation (4.4), determine the constant and variable values.

$$c_k = \frac{d - \sum_{jj \neq k} a_j}{a_k} \quad (4.4)$$

c_k refers destination point $c\ of\ k$-th element, a_j refers j-th element of attack vector $\overrightarrow{A_\iota}$, dThe right-hand side of (4.2) refers to the general depiction of the destination point on the cruise hyperplane referred to in Equation (4.5).

$$\overrightarrow{C_\iota} = \left(c_1 = random, c_2 = random, \dots c_k = \frac{d - \sum_{jj \neq k} a_j}{a_k}, \dots, c_n = random\right) \quad (4.5)$$

In Equation (4.6), the step vector for the golden eagle i in the iteration is stated as,

$$\Delta x_i = \overrightarrow{r_1} P_a \frac{\overrightarrow{A_\iota}}{\left\|\overrightarrow{A_\iota}\right\|} + \overrightarrow{r_2} P_c \frac{\overrightarrow{C_\iota}}{\left\|\overrightarrow{C_\iota}\right\|} \quad (4.6)$$

Golden eagles are affected by attack and cruise in iteration t, p_a^t refers to the attack coefficient in t, and p_c^trefers cruise coefficient in t. The Euclidean norms of attack and cruise vectors ($\left\|\overrightarrow{A_\iota}\right\|and\left\|\overrightarrow{C_\iota}\right\|$) are designated using Equation (4.7).

$$\left\|\overrightarrow{A_\iota}\right\| = \sqrt{\sum_{j=1}^{n} a_j^2}, \left\|\overrightarrow{C_\iota}\right\| = \sqrt{\sum_{j=1}^{n} c_j^2} \quad (4.7)$$

The golden eagle's location in iteration t + 1 is designed by adding a step vector in t.

$$x^{t+1} = x^t + \Delta x_i^t \quad (4.8)$$

The linear transition revealed in Equation (4.9) is exploited to compute transitional standards.

$$\begin{cases} P_a = P_a^0 + \frac{t}{T} |P_a^t - P_a^0| \\ P_c = P_c^0 + \frac{t}{T} |P_c^t - P_c^0| \end{cases} \quad (4.9)$$

T refers to maximum iterations, P_c^0 and P_c^t refers to starting and final values for p_a, Correspondingly.

4.3.2. Incremental Conductance (INC)

According to the literature, the P&O approach is the most popular and successful MPPT method for reaching maximum power. The suggested IC [10] addresses the shortcomings of the

conventional P&O methodology. Now, MPP is accomplished using the link among partial cap I. over partial cap V and minus cap I. over cap Vng $\frac{\partial I}{\partial V}$ and $-\frac{I}{V}$, as specified in Eq. (4.10).

$$P = V\,I \tag{4.10}$$

After taking the derivative on Eq. (4.10) at both sides, the Eq. (4.11) is expressed as

$$\frac{\partial P}{\partial V} = 0 \tag{4.11}$$

Accordingly, the Eq. (4.12) is stated as

$$\frac{\partial I}{\partial V} = -\frac{I}{V} \tag{4.12}$$

Therefore, this equation (4.12) manages a boost converter's duty cycle. After that, MPPT regulates the inverter's PWM signal until the maximum power is obtained.

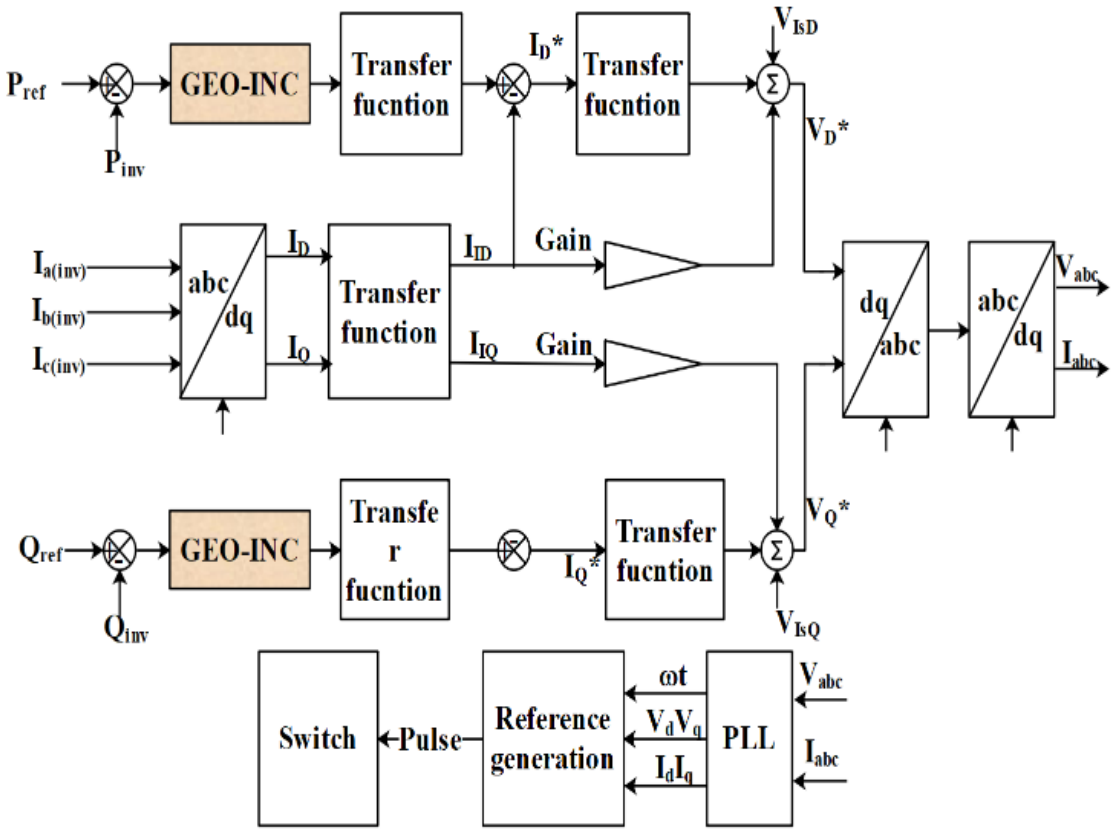

Figure 4.2 Control circuit diagram of proposed GEO-INC

Figure 4.2 shows the control circuit suggested for this PV/wind/battery system. When an alteration in sunlight or a disruption in the reference voltage causes a change in power, the recommended GEO-INC effectively regulates the PV module.

4.4. Result and Discussion

The investigation's results were validated using MATLAB software. The GEO-INC in the grid-connected RES is implemented and simulated using MATLAB R2018a. It operates on a Windows 8 system with an Intel Core i3 processor and 4GB RAM.

The suggested GEO-INC is tested in simulations to ensure that the control method has a compensatory effect under a range of irradiation scenarios. This study uses batteries, wind, and solar energy to create several hybrid system designs. The suggested model's simulation is shown in Figure 4.3. The correct scaling factor modifies the duty cycle value, enabling the PV to reach its peak and draw its maximum power.

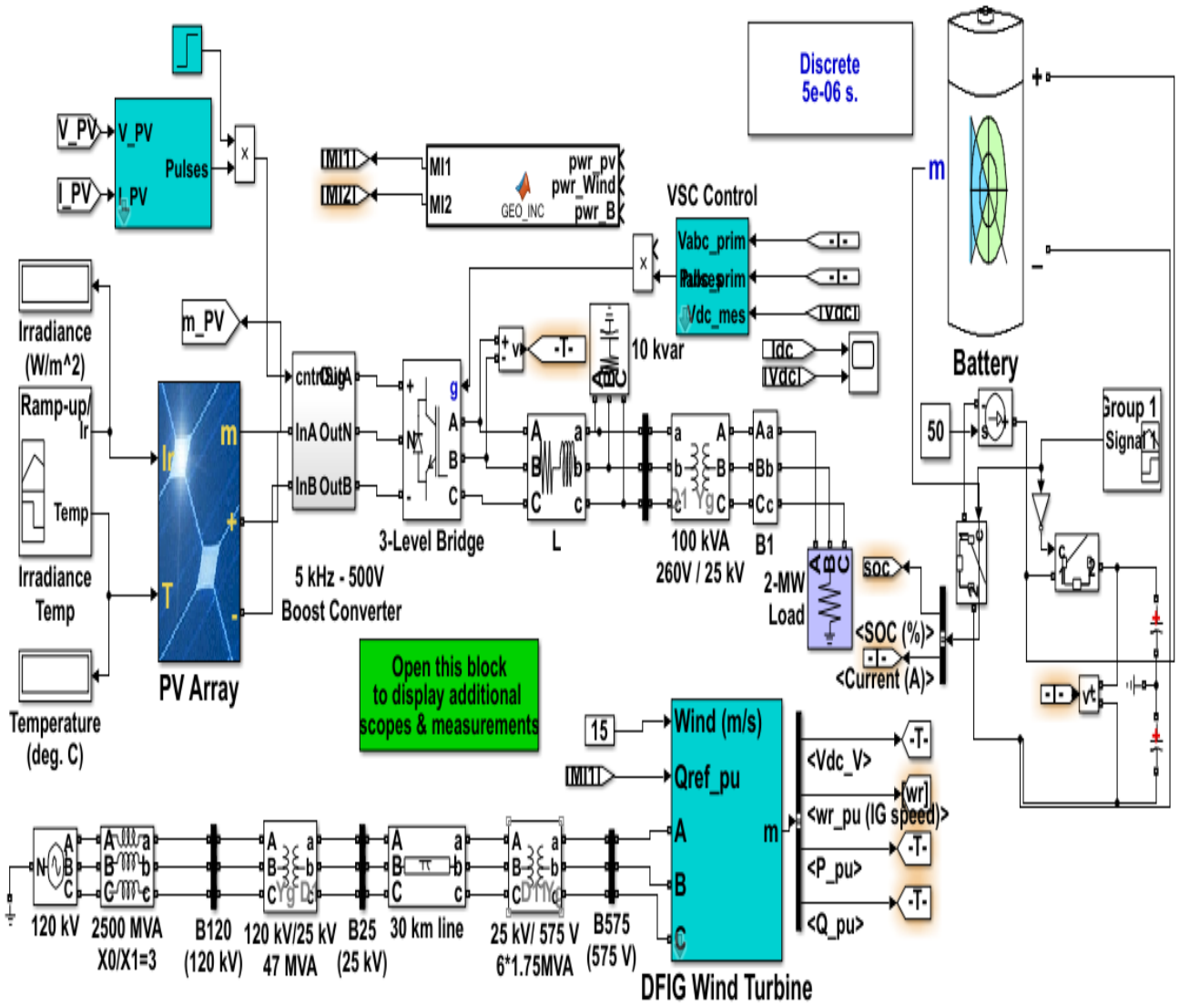

Figure 4.3 Simulink model of GEO-INC

The GEO variables used in the simulation are 200 for the population size, 200 for the number of iterations, 2.5 for the attack propensity, and 100 for the archive size.

4.4.1. Performance analysis

Three integrated controllers are used for the process of GEO-INC in grid-connected RES: P&O, INC, and GEO-P&O.

4.4.1.1. MPPT Current and Voltage

The voltage and current readings from the MPPT are shown in Figures 4.4 and 4.5. Figures 4.4 and 4.5 show that the proposed GEO-INC has higher MPPT current/voltage values and improved system performance in both stable and dynamic states.

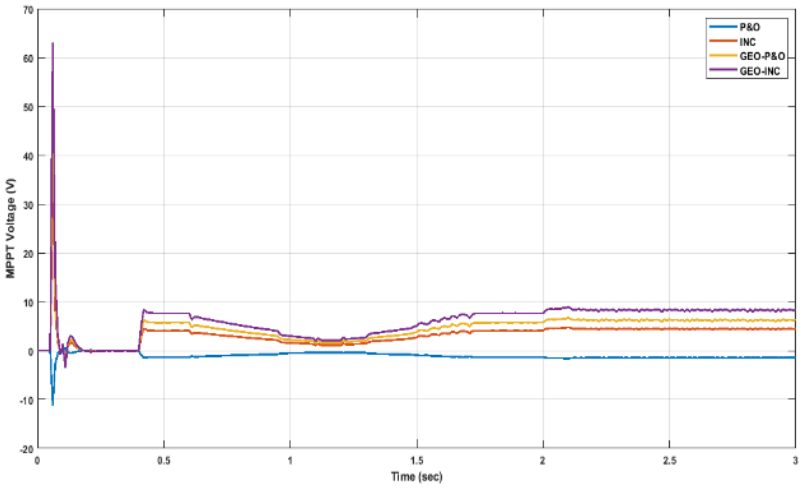

Figure 4.4 Analysis of MPPT voltage

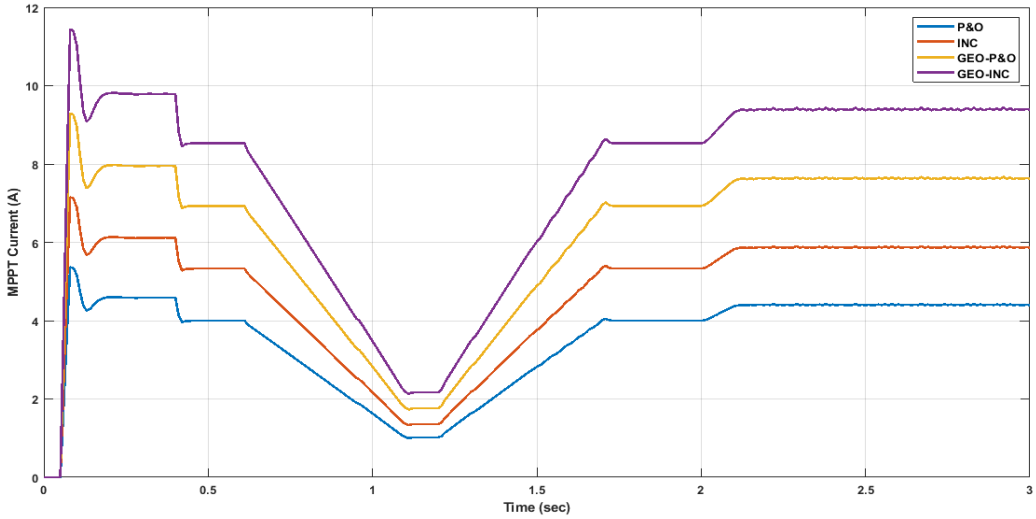

Figure 4.5 Analysis of MPPT's current

4.4.1.2. Grid voltage

Figure 4.6 shows the grid voltage between 0.92s and 1.04s in graphical form. It shows that, compared to conventional demand compensation systems, the suggested GEO-INC generates more voltage.

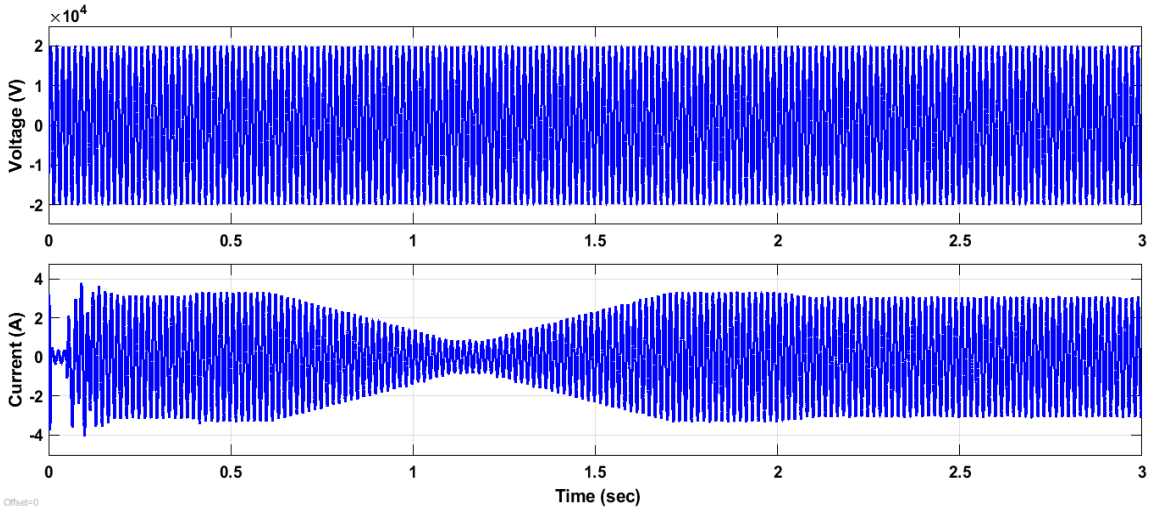

Figure 4.6 Analysis of Grid Voltage

4.4.1.3. Real and Reactive power

Figures 4.7 and 4.8 depict the utility grid's real and reactive power. Consequently, the proposed GEO-INC controller can satisfy the grid's growing energy needs.

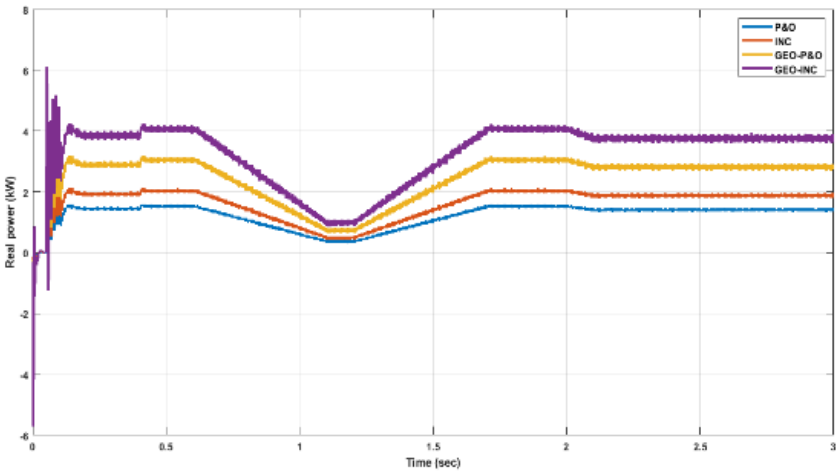

Figure 4.7 Analysis of Real power

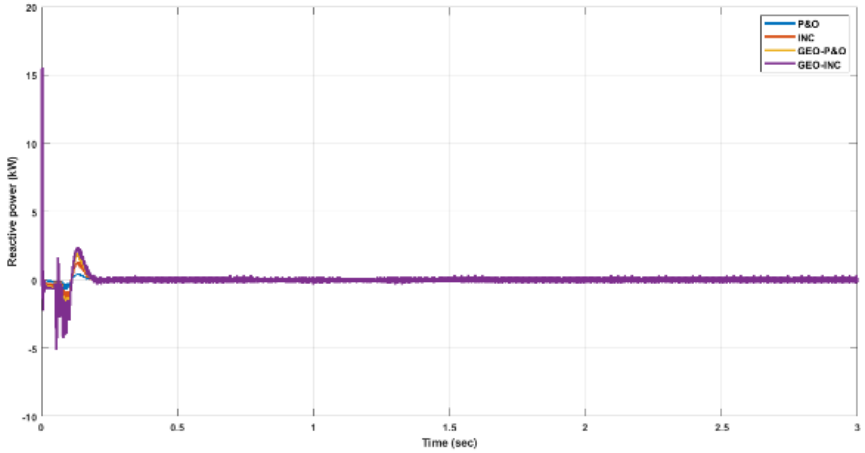

Figure 4.8 Analysis of Reactive Power

4.4.2. Comparative analysis

The efficacy of the GEO-INC is tested to validate the system against previous RES designs. The proposed GEO-INC control is compared with the existing 3IMPL and 3MPLL control algorithms to demonstrate the uniqueness of control techniques. Figure 4.9 displays the analysis of THD.

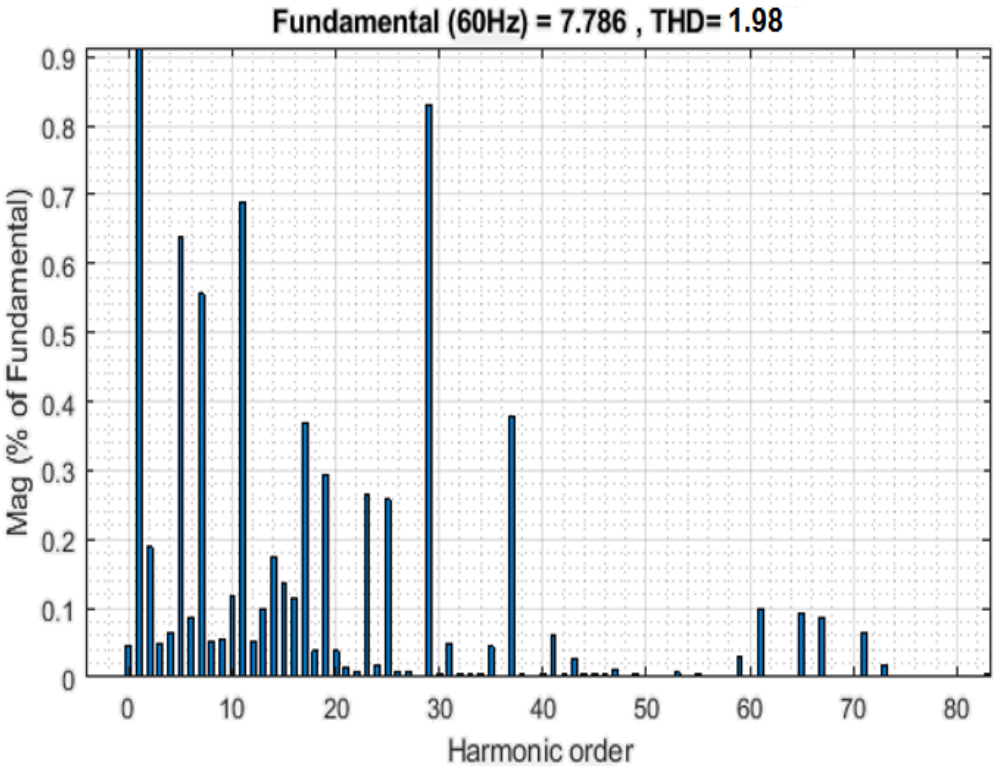

Figure 4.9 Performance of FFT Analysis

Figure 4.10 and Table 4.1 present the findings of the THD comparison. The magnitude component of 3IMPL has harmonics, quantified as 4.8% and 3%.

Table 4.1 Comparative Analysis of THD

Techniques	THD (%)
3MPLL	4.8
3IMPL	3
P&O	5.1
INC	4.9
GEO-P&O	3.1
Proposed GEO-INC	1.98

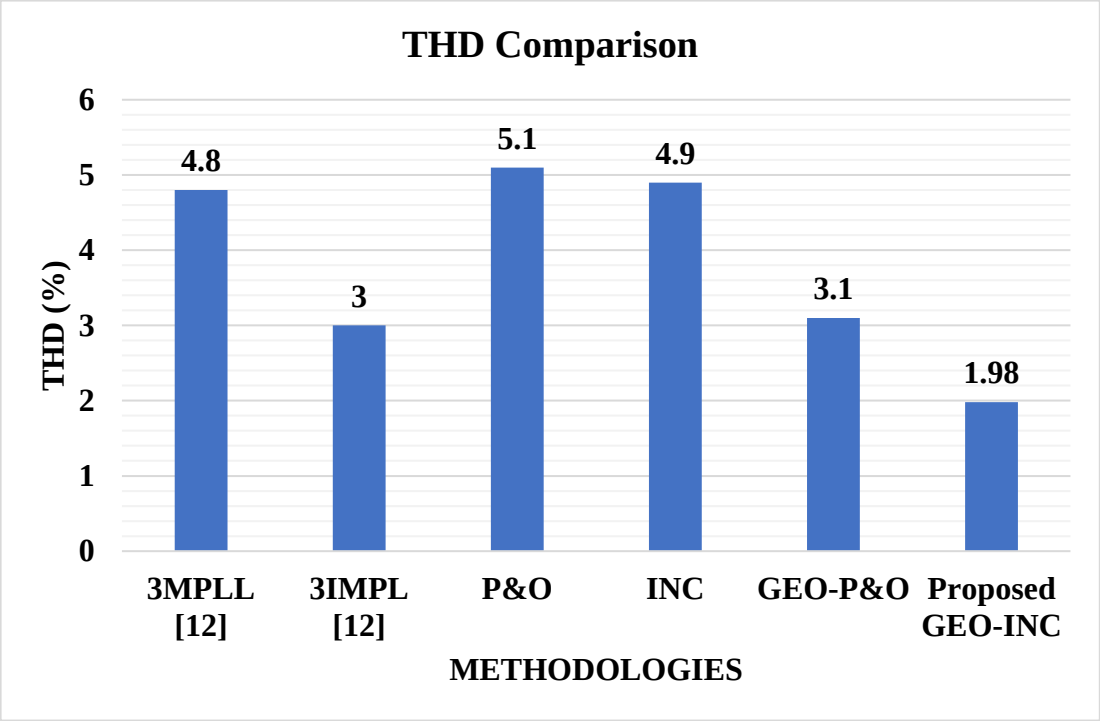

Figure 4.10 Graphical diagram of THD

Table 4.2 compares battery, wind, and PV power. It shows that compared to the current controller, which generates less power, the proposed GEO-INC achieves higher power generation.

Table 4.2 Comparison of Power Generation

Time (Min)	PV Power (W)		Wind Power (W)		Battery Power (W)	
	MPPT Controller	Proposed GEO-INC	MPPT Controller	Proposed GEO-INC	MPPT Controller	Proposed GEO-INC
0	50	67.78	35	50.62	2	19.12
10	54.26	69.28	42.18	52.35	-22.2	2.72
20	54.26	70.08	42.18	54.71	-43.1	1.37
30	54.26	70.27	42.18	55.10	-43.1	3.48
40	54.26	76.25	42.18	57.19	-22.1	2.51
50	54.26	76.25	42.18	57.19	2.9	8.70
60	54.26	76.25	42.18	57.19	16.13	19.68
70	54.26	76.25	42.18	57.19	22.24	26.81

4.5. Summary

RES are becoming more and more common because of their abundance, accessibility, and simplicity in harnessing for the production of electricity. Peak power from the PV output is obtained using the MPPT method to maintain the ideal PV value. The incremental conductance method is one of the methods that make up MPPT. In this study, an efficient EMS will be built using a PV/wind/battery system by employing the GEO-INC methodology. The modulation index from the recommended GEO-INC technique was used to control an efficient transition between battery and wind power. The simulation results show that compared to the current 3IMPL approaches, the proposed GEO-INC has a THD of 1.98 percent and generates additional power.

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Chapter 5

Implementation of Grid-Connected Wind Energy during Fault Analysis using Moth Flame Optimization with Firebug Swarm Optimization

In modern trends, the Voltage profile has become increasingly critical when incorporating wind turbine energy sources because of changes in fault ride-through capabilities throughout voltage reaction. Ripple, voltage magnitude changes, and injected harmonics due to conversion switches are power quality issues for grid-integrated Doubly Fed Induction Generators (DFIG) wind sources. In this study, FACTS devices like the Static VAR compensator (SVC), Thyristor Controlled Series Compensator (TCSC), Unified Power Flow Controllers (UPFC), and Static Synchronous Compensator (STATCOM) are used to stabilize wind energy with DFIGs. The MATLAB simulation test cases also analyzed three lines to ground fault (LLL-G) of fault measures, which showed a 9 MW that transferred to the utility grid. Therefore, injecting or absorbing reactive power is suggested to stabilize the system using Moth Flame Optimization with Firebug Swarm Optimization (MFO-FSO). The simulation results demonstrate that the proposed MFO-FSO-based STATCOM devices outperform the current Non-linear Generalized Predictive Control STATCOM, which only achieves 0.9815 per unit voltage stability by completing a higher voltage profile of 0.9925 per unit voltage stability with a reactive power injection of 1.82 MVAR.

5.1. Contribution

The significant contributions of this paper are stated as follows:

- FACTS devices are used with the MFO-FSO approach to address the transmission line's power quality issue.
- The primary contribution is developing the best control framework for eradicating harmonic disturbances using identical FACTS devices.
- To give the nominal outcomes, proposed MFO-FSO with FACTS devices are utilized to balance the reactive power for DFIG-based wind turbines.

5.2. Modelling of FACTS devices

The transmission network uses the FACTS devices to achieve a reliable, stable, and secure power system network. Hence, it is essential to identify the proper allocation and size of the FACTS devices during the device placement.

5.2.1. Modelling of SVC

SVC integrates a thyristor-controlled reactor and a thyristor-switched capacitor illustrated in Figure 5.1. The reactive power is injected into the system when the load is highly inductive. Similarly, the reactive power is absorbed by the SVC, when the system has a higher reactive power flow. The reactive power range is limited as follows: -100 MVAR ≤ Q_{svc} ≤ 100 MVAR.

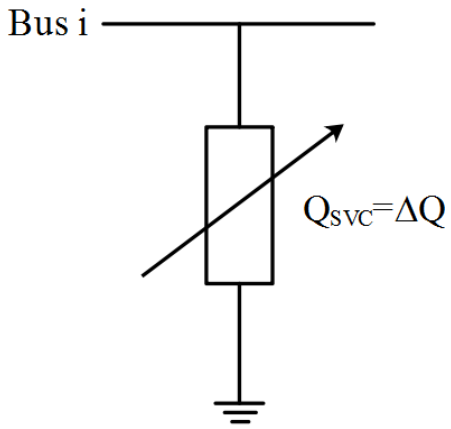

Figure 5.1 Model of SVC

The location of the SVC in a node is expressed in the following equation (5.1).

$$\Delta Q = Q_{SVC} \tag{5.1}$$

Where the size of SVC is represented as ΔQ. The Reactive Power Dispatch (RPD) issue with SVC placement is given in the following section:

5.2.2. Modelling of TCSC

The TCSC modifies the effective series reactance of the transmission line. Its placement in the network is used for continuous power control in the transmission line network. In the power system network, the TCSC controls the power flow and can eliminate sub-synchronous resonance. Moreover, the TCSC improves the transient stability and damps out the inter-area power oscillations. The TCSC model in a transmission line is illustrated in Figure 5.2.

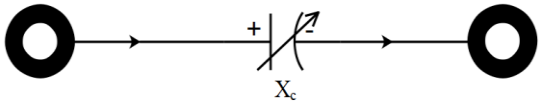

Figure 5.2 Model of TCSC

The location of the TCSC in a node is expressed in the following equation (5.2).

$$X_{TCSC} = r_{TCSC}.X_{Line} \quad (5.2)$$

Where the transmission line reactance is specified as X_{Line} and r_{TCSC} Represents the coefficient that specifies the degree of composition by TCSC. The operating range of the TCSC is selected between -0.8 X_{Line} and 0.2 X_{Line} To avoid overcompensation. The ideal position of the reactance is obtained by minimizing the reactance among the specified ranges. The TCSC's variable capacitance is also adjusted based on the load requirement.

5.2.3. Modelling of UPFC

The modeling of UPFC is the combination of TCSC and SVC coupled with the bus. Hence, the power flow in UPFC occurs based on the line reactance, phase angle, and bus voltage. The diagram of UPFC is given in the following Figure 5.3, and equation (5.3) expresses the power flow of the UPFC.

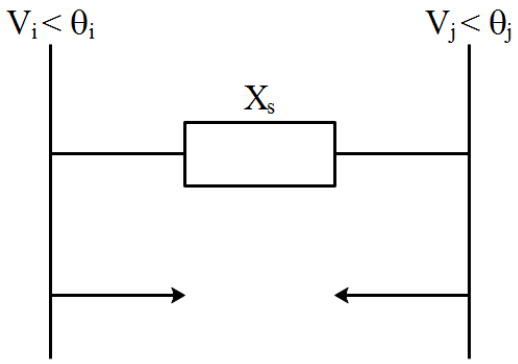

Figure 5.3 Model of UPFC

$$P_{ij} = \frac{V_i V_j}{X_{ij}} \sin(\delta_i - \delta_j) \quad (5.3)$$

If the UPFC is located between the node i and j, the admittance matrix adjusts the reactance. The reactance is equal to the X_s Insertion leads to a change in the Jacobian matrix between two nodes and appropriate power.

5.2.4. Modelling of STATCOM

The basic model of the STATCOM is illustrated in Figure 5.4. This STATCOM model is connected to the wind farm bus via a coupling transformer. A power electronic Voltage Source Converter (VSC) creates the STATCOM. The VSC of STATCOM is used to control reactive power.

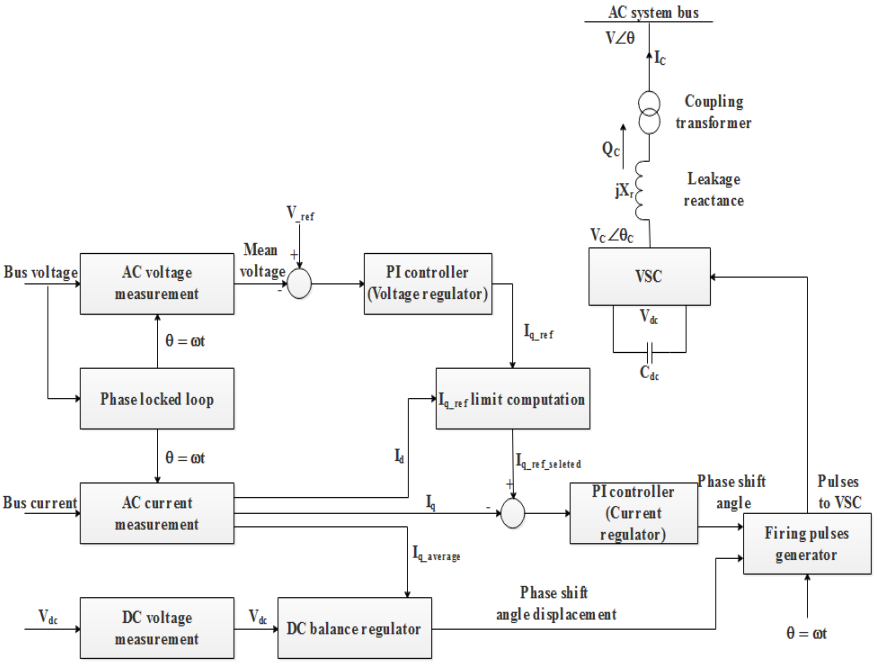

Figure 5.4 STATCOM Model

The controller output Q_c is related to the difference in voltage extent $(V_c - V)$which is shown in the following equation (5.4).

$$Q = \frac{V(V_c - V)}{X} \tag{5.4}$$

Where generated voltage is specified as (V_c) through system voltage (V). The reactive current reference is referred to as (I_{q-ref})And the voltage mean value is specified as (V_{mean})And the reference voltage value is designated as(V_{ref}).

5.3. Proposed Method

5.3.1. Moth Flame Optimization

Moths approach nearby light sources in a winding pattern to build stable points with them. While the moths' location in space solves the flexibility of the issue in which it has been used, the arrangement in computation is addressed by the moths. By randomly generating moths in the solution space, MFO calculates each moth's fitness values. The optimal location is then marked with the flame. The spiral movement function determines how the moths update their location. MFO is modernized after using the position equation to determine the flame's ideal placement. MFO follows identical steps for updating its location and creating new locations, such as the moth. The equation (5.5) expression for the moth position is initially constructed using a subsequent function.

$$M_i = S(M_i, F_j) \tag{5.5}$$

If M_i symbolizes the i^{th} Moth, j^{th}Flame is nominated through F_j and S is stated as the spiral path. The route of the moth is labeled in equation (5.6),

$$S\left(M_i, F_j\right) = D_i . e^{bt} . \cos(2\pi t) + F_j \tag{5.6}$$

D_i is stated as the distance between the i^{th} moth and j^{th} flame. b is stated as constant; t refers to the time limit of [-1,1]. D_i is calculated using equation (5.7),

$$D_i = \left|F_j - M_i\right| \tag{5.7}$$

In equation (7), M_i signifies i^{th} Moth, F_j signifies j^{th} flame and $D_i$indicates nodes' distance. Those formulations are mentioned in equation (5.8),

$$Flame\ no = round\ \left(N - 1 * \frac{N-1}{T}\right) \tag{5.8}$$

The maximum flame number is stated as N; Iterations with the maximum number are stated as T.

Results from MFO indicate that it can successfully handle a particular class of global streamlining problems. MFO, for instance, was successfully applied to a plan-related problem in international development. When the moth boundaries are predetermined, it can lead to early convergence and the inability to merge boundary sets. Future upgrades to the conventional MFO should achieve

more advanced execution. Therefore, Firebug Swarm Optimization is used with MFO to boost performance.

5.3.2. Firebug Swarm Optimization (FSO)

The FSO algorithm starts with $NM\ and\ NF$Male and female bugs arbitrarily scattered in the solution space because every male bug consumes a collection of NFfemale bugs. Let $\boldsymbol{m}(m).\boldsymbol{F}$ be the D by NF matrix, whose sections correlate to female bug places, denoted by F. The problem formulation update equations (5.9) and (5.10) are presented.

$$M_x \leftarrow repmat(\boldsymbol{m}(m).\boldsymbol{x}, \mathbf{1}, \boldsymbol{N_F}) \tag{5.9}$$

$$M_y \leftarrow repmat(\boldsymbol{m}(a).\boldsymbol{x}, \mathbf{1}, \boldsymbol{N_F}) \tag{5.10}$$

Where a is a random number among one and NF. The repmat (A, m, n) proceeds a medium that comprises m duplicates of A laterally the row measurement and n duplicates laterally the column measurement. Thus, if A is a p by q indexes at that time repmat (A, m, n) returns a mp by nq matrix that is formulated in equation (5.11)

$$\boldsymbol{m}(m).\boldsymbol{F} \leftarrow \boldsymbol{m}(m).\boldsymbol{F} + C_1 \odot (M_x - \boldsymbol{m}(m).\boldsymbol{F}) + C_2 \odot \left(M_y - \boldsymbol{m}(m).\boldsymbol{F}\right) \tag{5.11}$$

Since these numbers in $\boldsymbol{C_1}$ are chosen to be much bigger than$\boldsymbol{C_2}$, The above update sends each female bug. When $\boldsymbol{C_2}$ was kept shorter than$\boldsymbol{C_1}$, The FSO algorithm performed much better. The subsequent equation (5.12) shows the conceptual update rule for male bugs moving towards the most potent female bug.

$$\boldsymbol{m}(m).\boldsymbol{x} \leftarrow \boldsymbol{m}(m).\boldsymbol{x} + C_3 \odot (\mathrm{g} - \boldsymbol{m}(m).\boldsymbol{x}) \tag{5.12}$$

Even as the concept of herd cohesiveness, Eq. (5.13) is suggested, in this aspect, the FSO differs significantly from methods such as the PSO, in which every particle strives for a unique global optimal solution.

$$\boldsymbol{m}(m).\boldsymbol{x} \leftarrow \boldsymbol{m}(m).\boldsymbol{x} + C_4 \odot (\mathrm{g} - \boldsymbol{m}(b).\boldsymbol{x}) \tag{5.13}$$

This investigation for the finest reproductive mates is a potential solution. The vector x is articulated in terms of x^1 and x^2 via the triangular law of vector calculation mentioned in Equation (5.14).

$$x = x^1 + a(x^2 - x^1) = (1 - a)x^1 + ax^2 \tag{5.14}$$

From the above points, it is evident that the migration of male bugs through location. $\boldsymbol{m}(m).\boldsymbol{x}$) To appropriate female bug is attained through Equation (5.15):

$$\boldsymbol{m}(m).\boldsymbol{x} \leftarrow \boldsymbol{m}(m).\boldsymbol{x} + \boldsymbol{a}(\boldsymbol{g} - \boldsymbol{m}(m).\boldsymbol{x}) \tag{5.15}$$

Furthermore, Equation (5.15) is simple and relatively cheap, resulting in the updated equation given Equation (5.16),

$$\boldsymbol{m}(m).\boldsymbol{x} \leftarrow \boldsymbol{m}(m).\boldsymbol{x} + C_4 \odot (\mathbf{g} - \boldsymbol{m}(b).\boldsymbol{x}) \tag{5.16}$$

Likewise, Equation (5.17) is used to explain the weak motion of female bugs towards a different male insect:

$$\boldsymbol{m}(m).\boldsymbol{F} \leftarrow \boldsymbol{m}(m).\boldsymbol{F} + C_1 \odot (M_x - \boldsymbol{m}(m).\boldsymbol{F}) + C_2 \odot \left(M_y - \boldsymbol{m}(m).\boldsymbol{F}\right) \tag{5.17}$$

The two terms, $\boldsymbol{C_1} \odot (M_x - \boldsymbol{m}(m).\boldsymbol{F})$ *and* $\boldsymbol{C_2} \odot \left(M_y - \boldsymbol{m}(m).\boldsymbol{F}\right)$Characterizes the movement in the direction of the dominant male bug and random male bug correspondingly. This method aids in selecting the best answer while keeping the diversity of possible answers. Figure 5.5 depicts the flowchart for the proposed method.

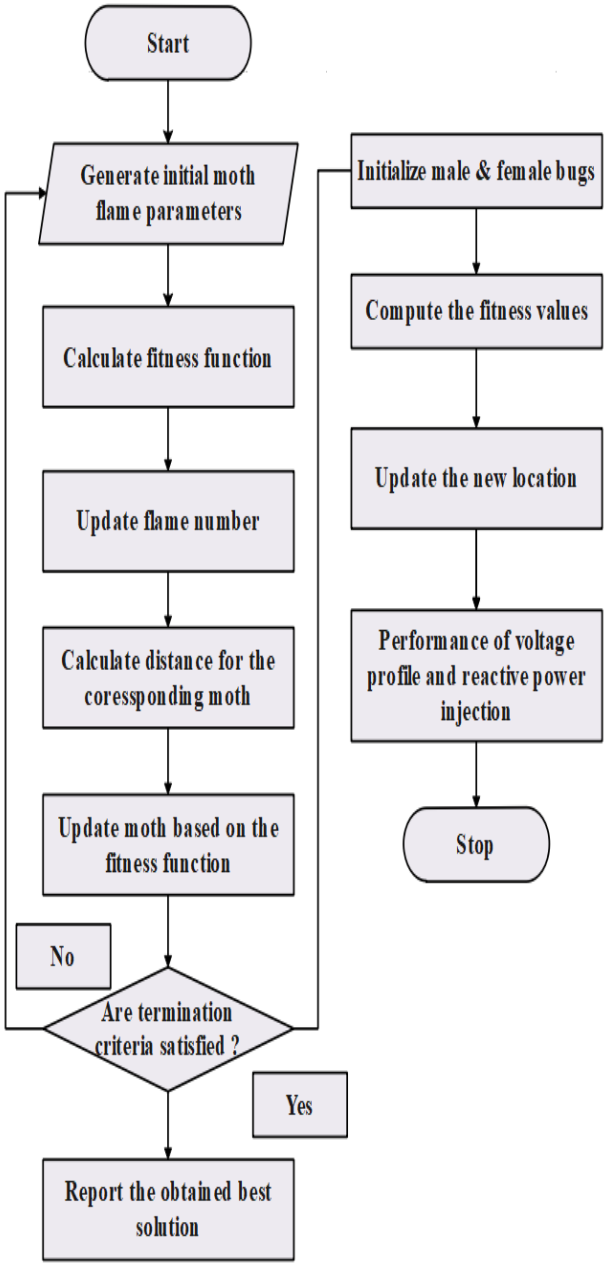

Figure 5.5 Flowchart of proposed MFO-FSO

5.4. Result and Discussion

This entire system is simulated using the MATLAB/SIMULINK R2018a. In this proposed system, an MFO-FSO-based FACTS model is used to inject/absorb reactive power to maintain stable power quality in the wind turbine. The overall Simulink model of the proposed method is given in Figure 5.6. The specifications of the generator and turbine are given in Table 5.1.

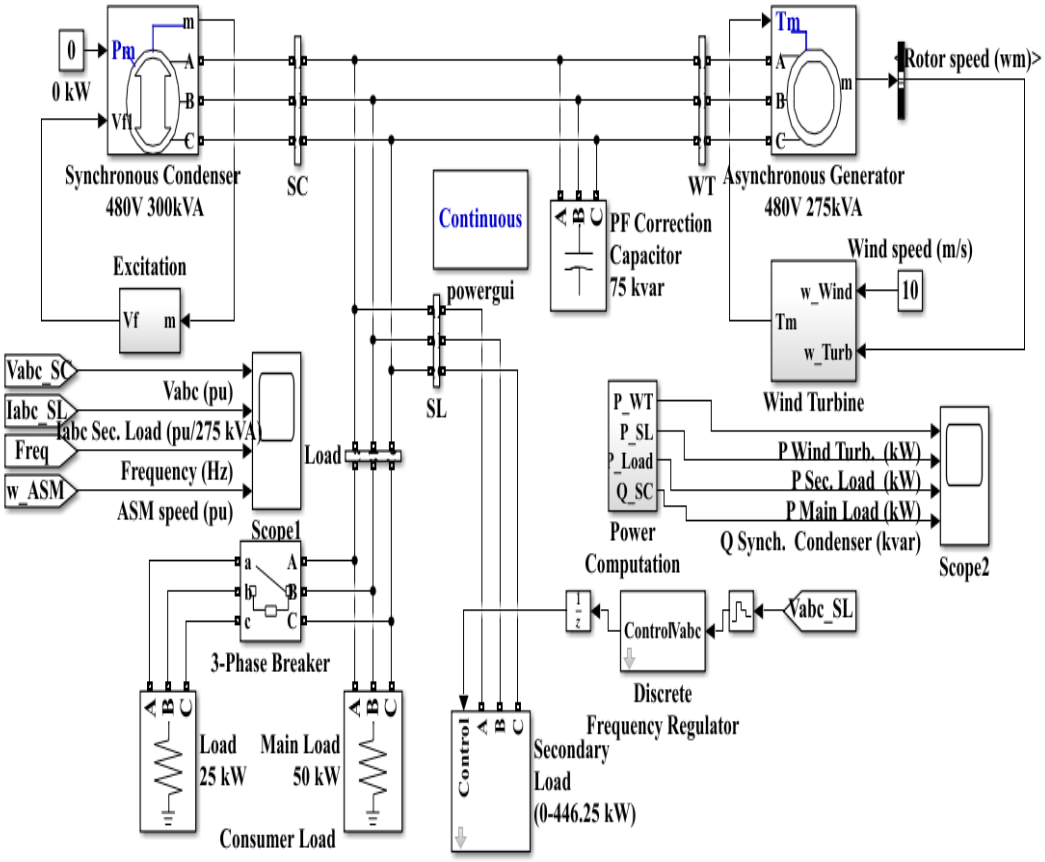

Figure 5.6 Simulink model for wind turbine induction generator

Table 5.1. Specifications of DFIG Generator

Nominal frequency (Hz)	50
Friction factor	0.01
Rotor (pu)	0.004377
Initial conditions [deg]	-0.01
Wind speed (m/s)	9
Stator (pu)	0.004843
Pitch angle (deg/s)	2
Rotational speed (pu)	1
Maximum pitch angle (deg)	45
Output power (W)	2*1.5e6
Gain: [Kp Ki]	5,25

Magnetizing inductance (pu)	6.77

The fault period effect and fault duration balance of the wind farm connected to the grid are analyzed using this proposed machine underneath various faults. The fault vicinity effect over the behavior of the wind farm is studied under different fault sorts, while the proposed machine has and does not have FACTS. In this proposed device, any of the faults are created inside the wind turbine induction generator at a distinct version of time for extraordinary sorts of faults.

5.4.1. Performance of SVC under three-phase Fault condition

Figures 5.7, 5.8, and 5.9 show SVC's performance under three-phase fault conditions. During the fault period, the natural and reactive power of the wind decreased from 9 to 6 MW and 4.5 to 3 MVAR, respectively.

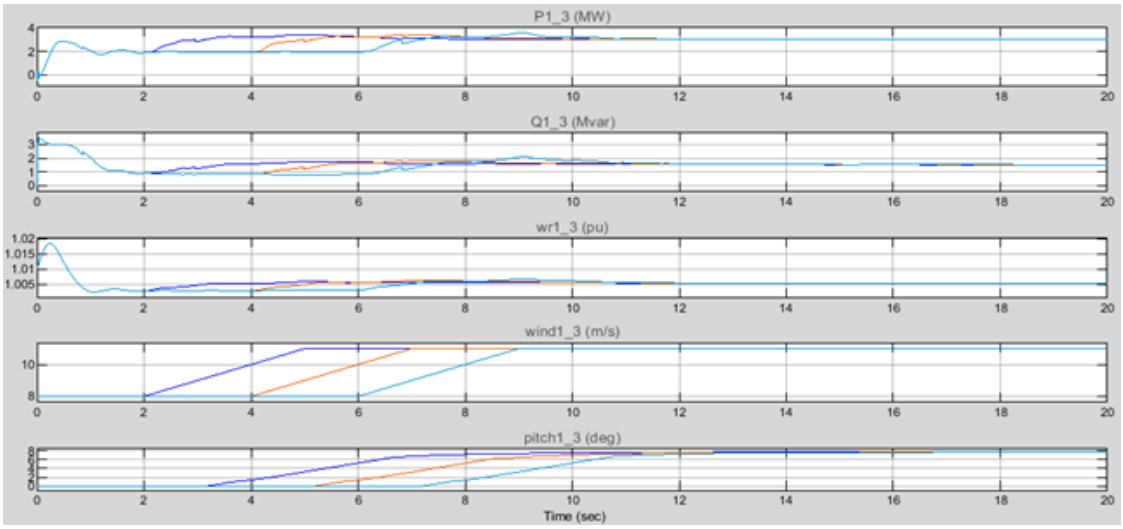

Figure 5.7 Performance of wind turbine

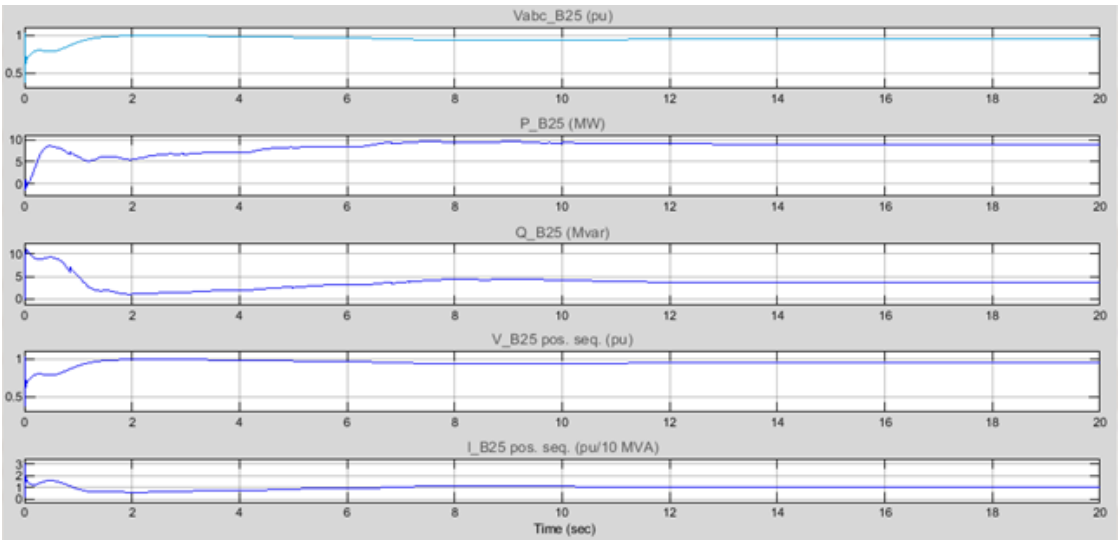

Figure 5.8 Performance at bus B25

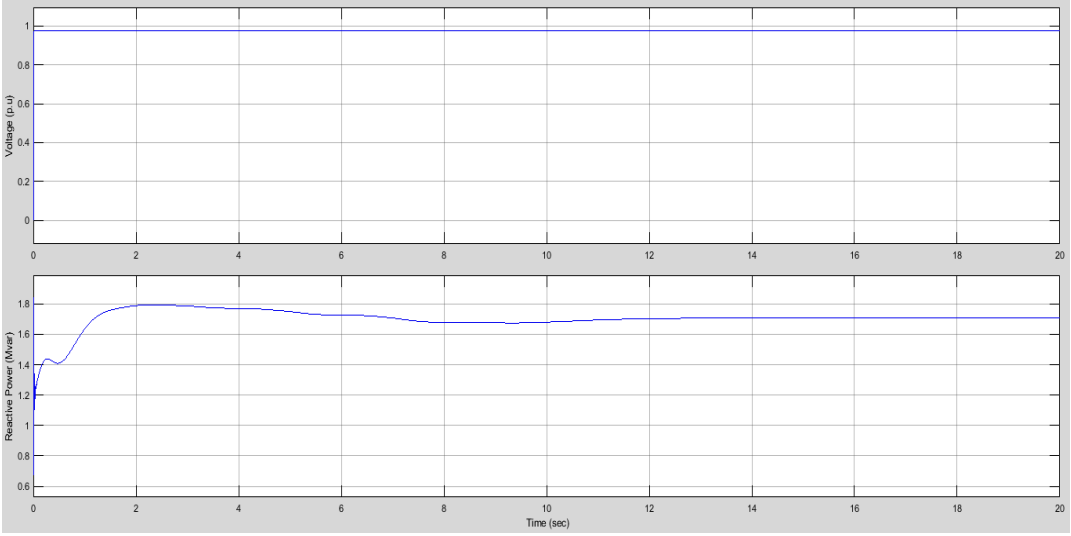

Figure 5.9 Performance of SVC

Once the fault has occurred, the pitch angle is reduced to 6 deg. Finally, the pitch angle is going to 0 deg after 17 sec. The voltage of the B25 is increased from 0.9 to 1 Pu. The natural and reactive power of the B25 is decreased from 9 to 6 MW and 4 to 2 MVAR, respectively. Figure 7.9 clearly indicates that the proposed MFO-FSO-based SVC achieves a voltage magnitude of 0.9744 per unit with a reactive power injection of 1.74 MVAR.

5.4.2. Performance of TCSC under three-phase Fault conditions

Figures 5.10 and 5.11 show the performance of the wind turbine and B25, respectively, when the system has TCSC during the LLL-G fault. Where figure 5.12 shows the reactive power injection of TCSC.

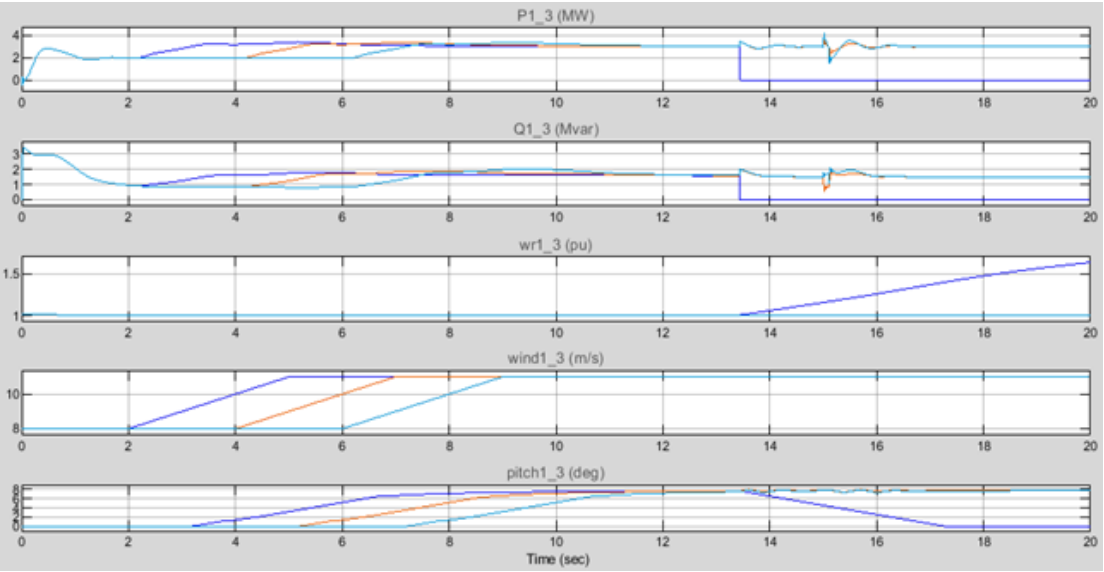

Figure 5.10 Performance of wind turbine

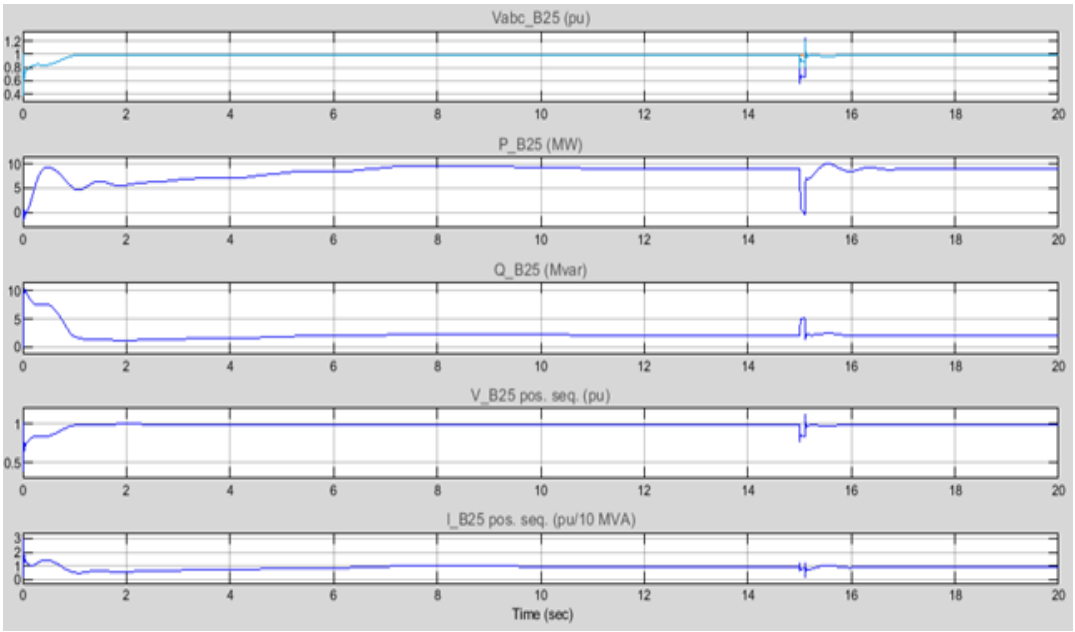

Figure 5.11 Performance at bus B25

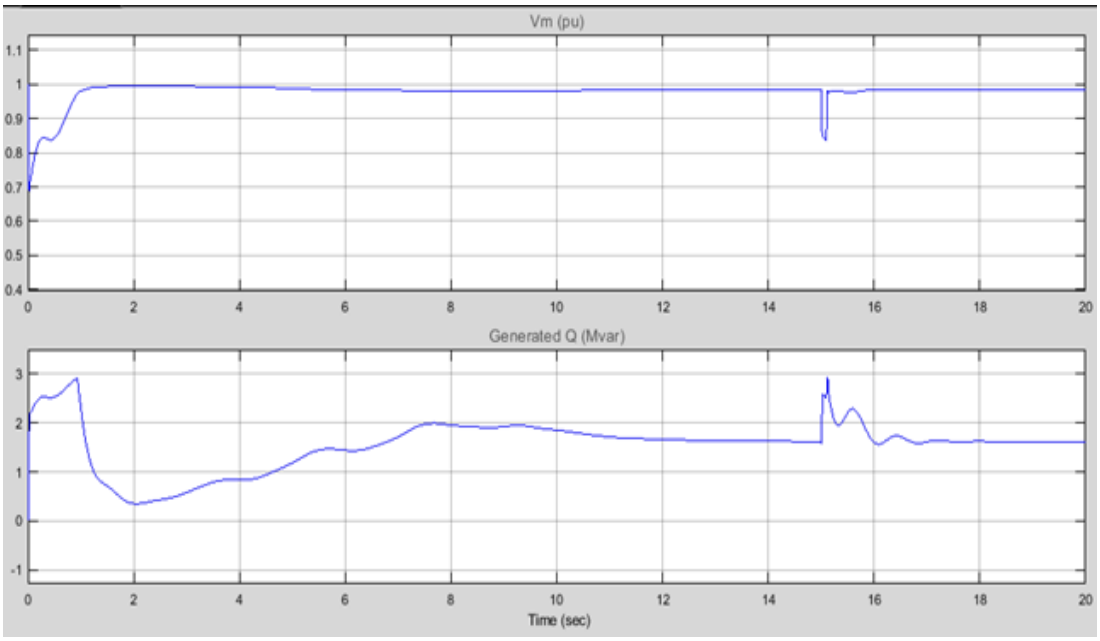

Figure 5.12 Performance of TCSC

When the system runs from 13.41 to 15.11s intervals, the reactive power and pitch angle are increased from 4.3 to 4.5MVAR and 7 to 8deg, respectively. The B25 and real power voltage are stabilized at 0.94Pu 9MW and 2Pu, respectively. The reactive power is 4.6MVAR at 13.41 and 4.5MVAR at 15.01 and 15.11s. Figure 5.12 indicates that the proposed MFO-FSO-based TCSC achieves a voltage magnitude of 0.9813 per unit with a reactive power injection of 1.68 MVAR.

5.4.3. Performance of UPFC under three-phase Fault condition

Figures 5.13 and 5.14 show the performance of the wind turbine and B25, respectively, when the system has UPFC during the LLL-G fault. Where figure 5.15 shows the reactive power injection of UPFC.

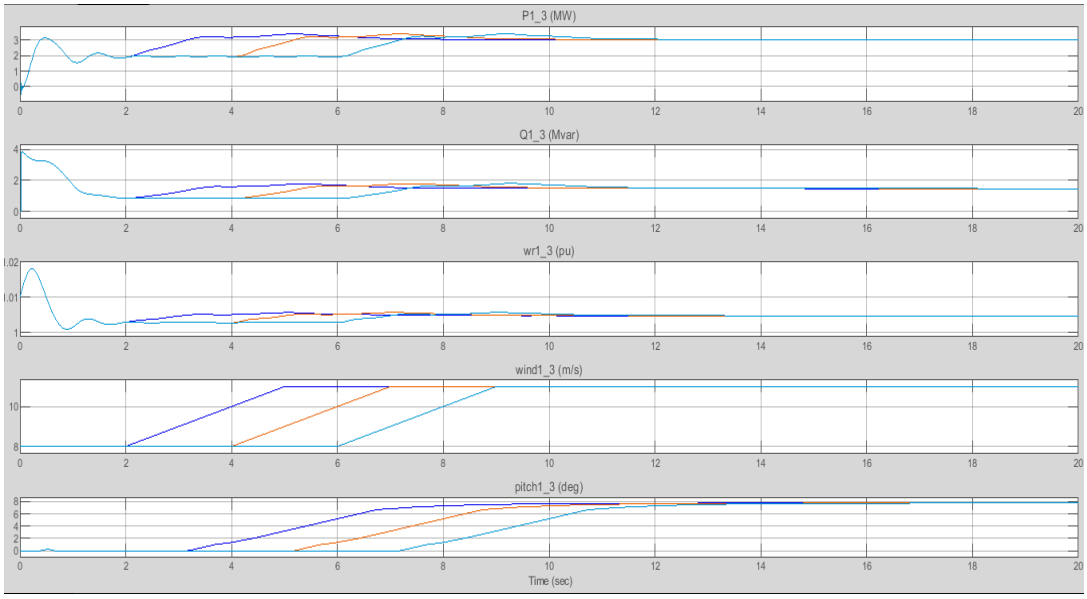

Figure 5.13 Performance of wind turbine

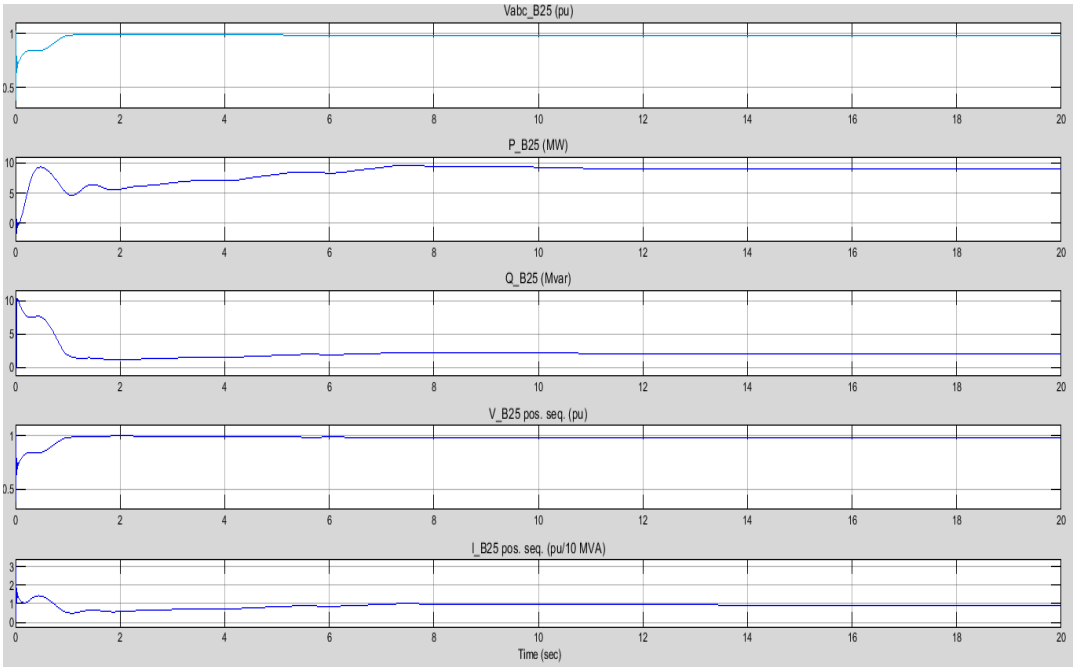

Figure 5.14 Performance at bus B25

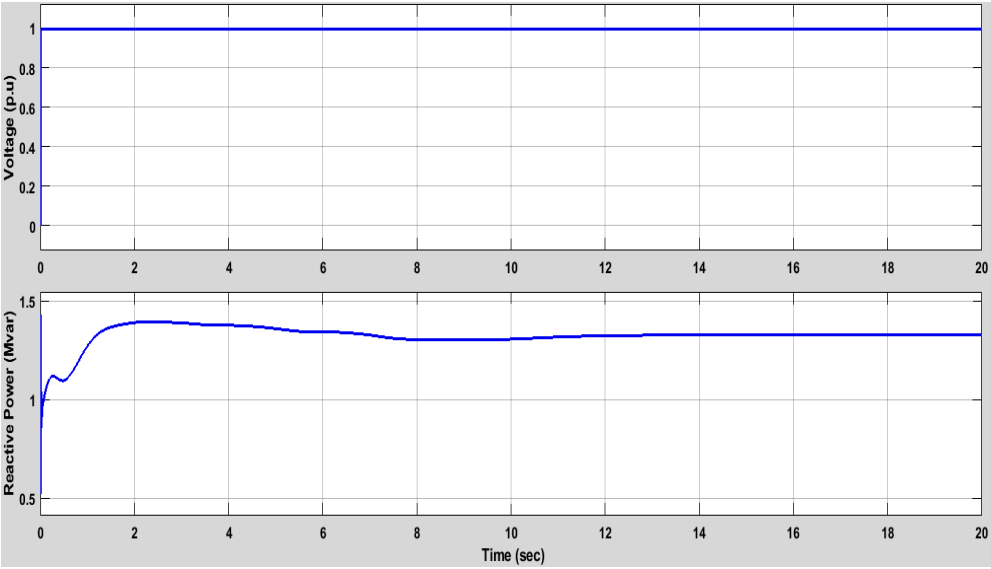

Figure 5.15 Performance of UPFC

The fault location of the LLL-G fault in the wind turbine is 15.11s. The real power of the wind is 9MW, and it decreased to 0.5MW at the first fault at 15.1 sec. Furthermore, this absolute power is decreased to 0MW in 15.11s. The reactive power of the wind turbine is reduced by 2 and 1MVAR at 15.1 and 15.11s, respectively. Then, this reactive power goes to 0. The pitch angle is going 8, 7, and 6.8 deg when the wind farm runs at 14, 15.1, and 15.11s, respectively. Usually, the voltage of the B25 is 1Pu stable from 11 to 14s. In the first fault, the B25 voltage is decreased from 1 to 0.4Pu at 15.1s, and in the second fault, it is increased from 0.4 to 1.3 t at 15.11s. Figure 5.15 clearly indicates that the proposed MFO-FSO-based UPFC achieves a voltage magnitude of 0.9972 per unit with a reactive power injection of 1.33 MVAR.

5.4.4. Performance of STATCOM under three-phase Fault condition

Figure 5.16 shows the wind farm with LLL-G fault when the system is presented without STATCOM. Figure 5.17 shows the B25 performance. The fault location of the LLL-G fault in the wind turbine is 15.11s. The real power of the wind is 9MW, and it decreased to 0.5MW at the first fault at 15.1 sec. Furthermore, this absolute power is reduced to 0MW in 15.11s. The reactive power of the wind turbine is decreased by two and 1MVAR at 15.1 and 15.11s, respectively. Then, this reactive power goes to 0. The pitch angle is going 6.8 deg when the wind farm runs at 14, 15.1, and 15.11s, respectively. Usually, the voltage of the B25 is 1Pu stable from 11 to 14s. In the first fault, the B25 voltage is decreased from 1 to 0.4Pu at 15.1s,

and in the second fault, it is increased from 0.4 to 1.3 t at 15.11s. The real power of B25 is 9MW, which is changed by 0, 3, and 0MW at 15.1, 1, 5.11, and 16s, respectively. The reactive power is changed from 2 to 11, 2, and 0 at 15.1, 1, 5.11, and 16s respectively.

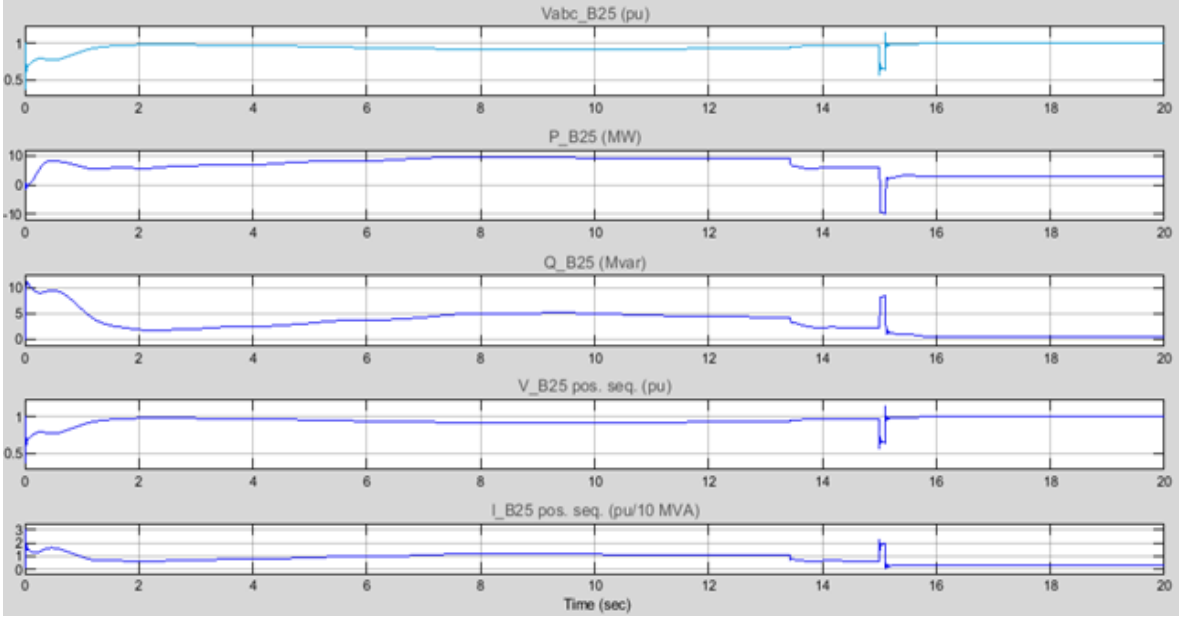

Figure 5.16 Performance of wind turbine

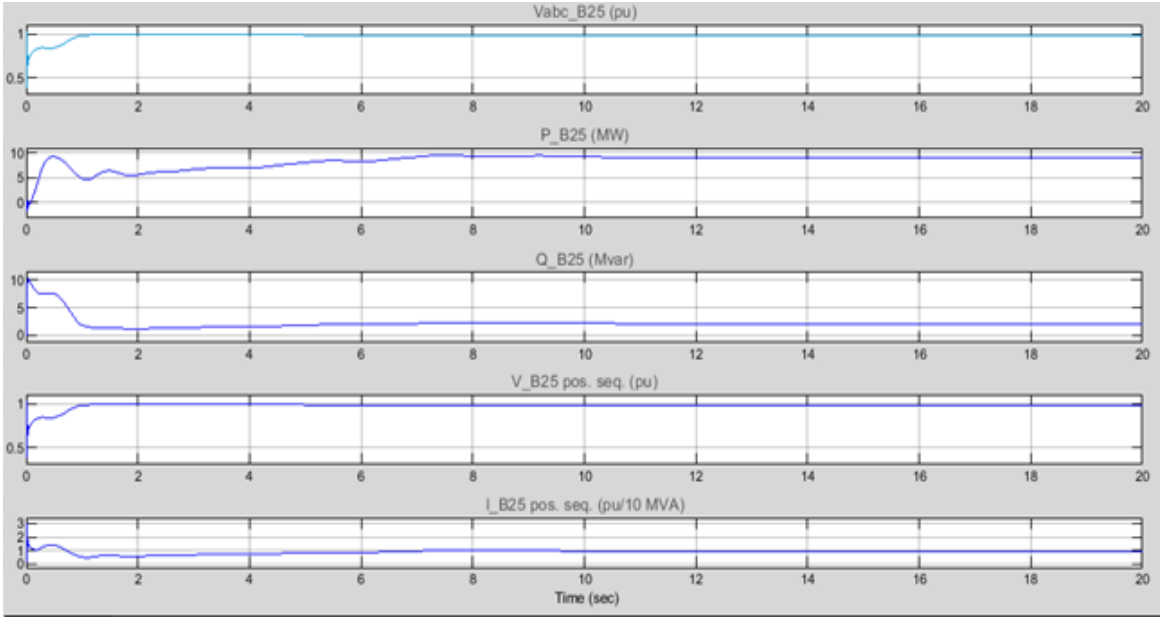

Figure 5.17 Performance of Bus B25

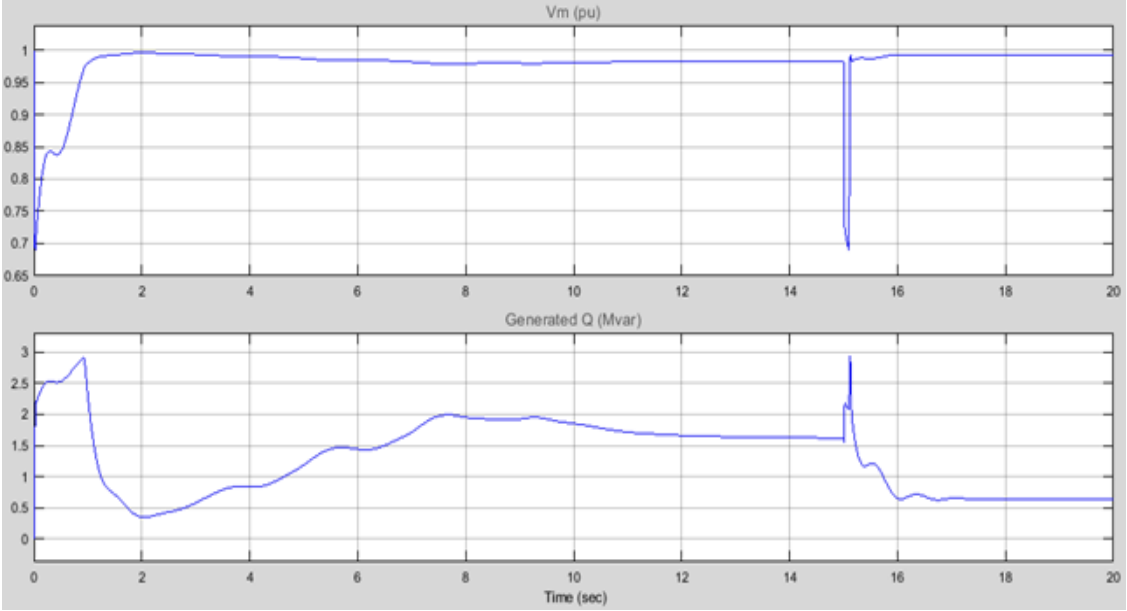

Figure 5.18 Performance of STATCOM

Figure 5.18 shows the wind turbine performance when the system has STATCOM during the LLL-G fault. The wind turbine's real power is 9MW at 13.41s. In the first and second faults of 15.01 and 15.11s, the real power is stabilized at 9MW. The reactive power is stabilized in 4.5MVAR at the first, second, and third faults of 13.41, 15.01, and 15.11s, respectively. The pitch angle varies from 7 to 8deg when the wind farm runs at 18s. The voltage of B25, real and reactive power is stabilized at 0.9925Pu, 9MW, and 2Pu, respectively. The voltage magnitude of STATCOM of all three faults is 0.98Pu. The reactive power is 1.65MVAR at 13.41s (first fault) and 1.6MVAR at 15.01 and 15.11s (second and third fault). Furthermore, this 1.6MVAR is stable after the three faults. Table 5.2 shows the performance analysis of FACTS devices.

Table 5.2 Performance Analysis of FACTS Devices

Parameters	**SVC**	**TCSC**	**STATCOM**	**UPFC**
Reactive Power (MVAR)	1.82	1.77	1.65	1.33
Voltage Magnitude (per unit)	0.9594	0.9732	0.9925	0.9972

5.4.5. Comparative analysis

For comparison, the wind farm with the three-line ground fault (LLL-G) of STATCOM under LLL-G. Table 5.3 tabulates the comparative analysis of STATCOM. It clearly shows that the proposed MFO-FSO achieves the maximum voltage magnitude of 0.9a, 925 p.u. with reactive power injection of 1.82 MVAR. Meanwhile, NGPC-based STATCOM achieves a voltage magnitude of 0.9815, less than the proposed MFO-FSO-based STATCOM devices.

Table 5.3 Comparative Analysis of STATCOM

Parameters	**NGPC based STATCOM**	**Proposed MFO-FSO based STATCOM**
Voltage Magnitude (per unit)	0.9815	0.9925

5.5. Summary

This study focused on the multiple difficulties connecting the FACTS devices to a grid-coupled nonlinear wind turbine. When a defect occurs in a transmission line, the reactive power and voltage magnitude are injected using traditional means. To provide the necessary reactive power during grid outages, the comparable model is shunt-linked to the terminal to which the wind turbine system is connected. On the other hand, a unique control approach known as MFO-FSO is created to increase the efficacy of DFIG power. The modeling of DFIG-based wind turbines in light of current trends and the next stage of problem identification are both significantly assisted by this research. The wind system is coupled to the proposed MFO-FSO-based FACTS model to provide the necessary reactive power during grid disturbances. The simulation results demonstrate that the proposed MFO-FSO model with STATCOM for the wind farm offers voltage stability of 0.9925 per unit with a reactive power input of 1.82 MVAR, outperforming the current NGPC-based STATCOM, which only provides 0.9815 per unit. Future work has expanded this research to include analyzing wind turbine systems using permanent magnet synchronous generators while including various FACTS devices.

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Chapter 6

Design and Analysis of 15-level and 25-level Multilevel Inverter Topologies

This study aims to minimize component requirements by presenting a novel topology for a single-phase 15-level asymmetric multilevel inverter. Utilizing an H-bridge configuration, the proposed design achieves a maximum 15-level output voltage using asymmetric DC sources. The initial 15-level multilevel inverter structure is further enhanced to facilitate a 25-level variant suitable for renewable energy applications, effectively reducing system costs and size. However, the increased component count in multilevel inverters poses reliability challenges, especially concerning total harmonic distortion reduction, which remains a focal point for researchers. Various parameters, including total standing voltage, multilevel inverter cost function, and power loss, are scrutinized for the proposed 15-level and the expanded 25-level multilevel inverters. This study contributes to a new topology for a single-phase 15-level asymmetric multilevel inverter, streamlining component usage and paving the way for renewable energy integration. Despite the inherent advantages of multilevel inverters, addressing reliability concerns associated with total harmonic distortion reduction remains imperative for future advancements in this domain.

6.1. Introduction

Numerous scholars have put forth several methods in the literature to enhance power quality in grid-connected photovoltaic systems [1], [2]. Afterward, hysteresis current controllers were used instead of conventional controllers [3]. In photovoltaic systems without transformers, hysteresis current controllers performed better at eliminating leakage current than conventional controllers [4]. In contrast, the current hysteresis control could not provide a workable fix for the shoot-through problems [5]. Several researchers created new MLI [6] and tried to modify older inverter technologies [7] to improve power quality in PV systems. However, none of these strategies could offer a complete fix for the issues with power quality [8]. Multilevel Multifunctional Grid-Connected Inverters (ML-MFGCI) could decrease switching losses and harmonics [9]. On the other hand, because they lacked additional functionality, the current ML-MFGCIs did not operate

to their total capacity. Cascaded H-bridge MLI control with high THD under various conditions was employed in specific tests. A novel hybrid approach is necessary [10].

6.2. Modelling of Converter for PV system

This section is devoted to presenting the application of the proposed MLIs to PV systems and how the asymmetrical input DC voltages needed by the MLI are obtained using an isolated DC/DC buck-boost converter.

6.2.1. Application of the Proposed MLIs to PV Systems

The circuit suggested for using the proposed 15-level and 25-level MLIs is depicted in Figure 6.1 (a) and (b). In grid-connected applications, the control of the DC/DC converter implements a maximum power point tracking (MPPT) algorithm, as is shown in the figure. Then, the load is composed of a grid connection through a line filter.

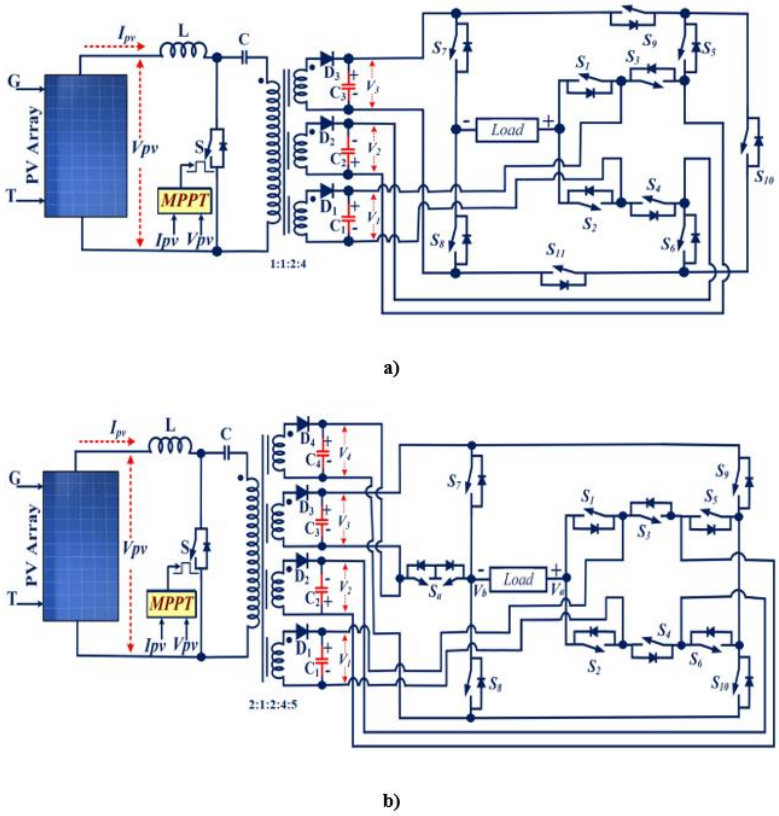


Figure 6.1 Solar-based converters for the proposed, (a) 15-level MLI and (b) 25-level MLI.

6.2.2. DC/DC Buck-Boost Converter Characterization

A converter interface to properly connect a PV generator with the suggested 25-level MLI is shown in Figure 6.2. This DC/DC buck-boost converter generates the four asymmetrical voltage values used as voltage input of the 25-level MLI, and it is based on the isolated Single-Ended Primary-Inductor Converter (iSEPIC). A simplified variation of this converter is used to generate the three asymmetrical voltage values used at the input of the proposed 15-level MLI. Different topologies for Single-Input and Multiple-Output (SIMO) DC/DC converters are presented in [45]. In this reference, some isolated DC/DC converter topologies, such as Single-Switch Flyback converter, Single-Switch Forward converter, isolated Zeta converter, isolated SEPIC converter, and isolated Ćuk converter, are introduced and proposed as frontend in PV applications. The iSEPIC converter is handy when an output voltage higher and/or lower than the input voltage is needed, including galvanic isolation. As stated in [46], iSEPIC converters are used in PV applications to interface varying solar panel voltages and the system's battery or grid voltage requirements. Other related applications include battery-powered devices, automotive electronics, LED lighting, portable electronics, uninterruptible power supplies (UPS), fuel cell systems, energy harvesting, medical devices, isolated power supplies, or DC microgrids.

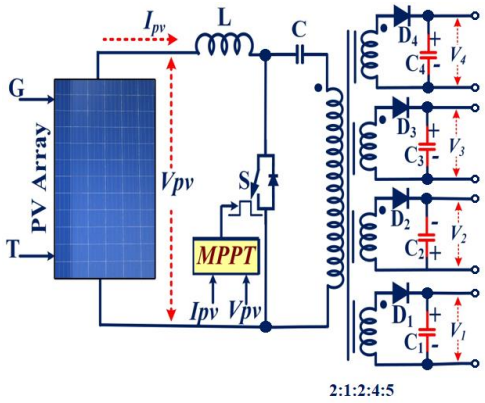


Figure 6.2 DC/DC buck-boost converter for the PV application of the 25-level MLI.

The use of SEPIC converters (isolated and non-isolated) in renewable energy applicators is widely referenced in the specialized literature. In [47, 48], two studies on non-isolated DC/DC converters for PV applications are presented. In these studies, the SEPIC converters are presented as the ideal topology for MPPT applications because their operation is independent of radiation and temperature, which allows them to track maximum power point and their high-power

conversion efficiency. In [49], a variation of the classical SEPIC structure of high voltage gain is presented as an adequate alternative for renewable energy applications. Reference [50] presents a modified iSEPIC converter for a solar power system to obtain a constant output voltage from the PV generator. In [51, 52], the iSEPIC converter suits the DC/DC stage on PV inverters for medium and large-scale PV applications. As a final example, in [53], an iSEPIC converter is proposed as a multipurpose power electronic interface (PEI) that is competent in utilizing dual sources (PV generator and grid) during the charging process for plug-in electric vehicles. The feature of the iSEPIC converter proposed in this section is simulated to demonstrate the suitability of this topology in the proposed application. The simulation is performed using MATLAB/SIMULINK 2022a software. The 1Soltech 1STH-215-P solar PV panel parameters were used to describe the PV generator formed by two PV modules associated in series. The main characteristics of this module are summarized in Table 6.1.

Table 6.1 Ratings of the PV module used in simulations.

Parameter	**Value**
The voltage at the maximum power point, V_{MPP}	29.0 V
Open circuit voltage, V_{OC}	36.3 V
Temperature coefficient of V_{OC}	– 0.361 %/ºC
Current at the maximum power point, I_{MPP}	7.35 A
Short-circuit current, I_{SC}	7.84 A
Temperature coefficient of I_{SC}	0.102 %/ºC
Maximum power, P_{MPP}	215 W
Temperature coefficient of P_{MPP}	– 0.495 %/ºC
Diode saturation current	$6.301 \cdot 10^{-12}$ A
Diode ideality factor	0.94504
Shunt resistance	269.6 Ω
Series resistance	0.3715 Ω

The MPPT algorithm implemented in the simulations is a classical Perturb & Observe (P&O), which is very easy to implement and offers a fast and accurate response in most cases.

Table 6.2 summarizes the values of the components used in the buck-boost converter simulation. Using a DC/DC buck-boost converter, the output power of the PV generator can be increased from 60 V (close to the MPP value) to 165 V. The selection of 20 kHz as the switching frequency compromises the size of the reactive components (smaller at a higher switching frequency) and the switching losses (higher at a higher switching frequency). The selected frequency is the lowest outside the audible range.

Table 6.2 Specifications of the DC/DC buck-boost converter.

Parameter	Value
Inductance: L	4.2 mH
Capacitor: C	33 µF
Switching frequency: f_s	20 kHz
Duty Cycle (D) in steady state	0.53

The DC/DC buck-boost converter specifications are obtained assuming operation in continuous conduction mode (CCM) and when the PV generator operates near the maximum power point conditions, i.e., $V_{pv} \approx 60$ V and $I_{pv} \approx 7.5$ A. In [54], the steady-state analysis of the non-isolated and isolated type SEPIC pulse width modulated (PWM) DC/DC converters for CCM is exhaustively presented. The results of this analysis are used in the following equations to determine the specifications of the proposed DC/DC buck-boost converter. Equation (6.1) is used to calculate the relationship between the input voltage (V_{pv}) and output voltage (V_{On}) of the DC/DC buck-boost converter.

$$V_n = n \cdot \frac{D}{1-D} \cdot V_{pv} = \frac{N_2}{N_1} \cdot \frac{D}{1-D} \cdot V_{pv} \quad \rightarrow \quad V_n = \frac{N_2}{2} \cdot \frac{0.53}{1-0.53} \cdot 60\ V \tag{6.1}$$

Where n is the transformer ratio, N_1 and N_2 are the number of turns of the transformer's primary and secondary coils, and V_n is the DC/DC converter output voltages.

The buck-boost converter's inductor (L) is designed using Equation (6.2), where f_s is the switching frequency, ΔI_L is the inductor current ripple, which is given as 5% of the rated current, and V_{pv} is the converter input voltage.

$$L = \frac{V_{pv}}{f_s \cdot \Delta I_L} \cdot D \;\; \rightarrow \;\; L = \frac{60}{20{,}000 \cdot \frac{5}{100} 7.5} \cdot 0.53 \approx 4.2\ mH \tag{6.2}$$

The capacitor (C) of the DC/DC buck-boost converter is designed from Equation (6.3), where the ripple of the capacitor voltage is determined as 10% of the rated output voltage.

$$C \geq \frac{I_{pv}}{f_s \cdot \Delta V_C}(1 - D) = \frac{I_{pv}}{f_s \cdot \frac{10}{100} \cdot V_{pv}}(1 - D) \;\; \rightarrow \geq \frac{7.5}{20{,}000 \cdot \frac{1}{10} \cdot 60} \cdot 0.47 \approx 29.4\ \mu F \tag{6.3}$$

The condition of CCM is attached when the magnetizing inductance of the used transformer (L_T) meets Equation (6.4).

$$L_T \geq L \cdot \frac{D}{1-D} \;\; \rightarrow \;\; L_T \geq 4.2\ m \cdot \frac{0.53}{1-0.53} \cdot 0.53 \approx 4.7\ mH \tag{6.4}$$

Finally, the value of the output capacitors (C_1 to C_4) is estimated using Equation (6.5), where the ripple of the output voltage is determined as 10% of the rated output voltage.

$$C_n \geq \frac{I_{pv}}{n \cdot f_s \cdot \Delta V_{Cn}} \cdot (1 - D) = \frac{I_{pv}}{n \cdot f_s \cdot \frac{10}{100} \cdot V_n} \cdot (1 - D) \tag{6.5}$$

The proposed value for these capacitors is presented in Equation (6.6).

$$C_1 \geq \frac{7.5 \cdot 0.47}{\frac{1}{2} \cdot 20{,}000 \cdot \frac{10}{100} \cdot 33} \approx 100\ \mu F \quad C_2 \geq \frac{7.5 \cdot 0.47}{1 \cdot 20{,}000 \cdot \frac{10}{100} \cdot 66} \approx 27\ \mu F$$

$$C_3 \geq \frac{7.5 \cdot 0.47}{2 \cdot 20{,}000 \cdot \frac{10}{100} \cdot 132} = 6.8\ \mu F \; C_4 \geq \frac{7.5 \cdot 0.47}{\frac{5}{2} \cdot 20{,}000 \cdot \frac{10}{100} \cdot 165} = 4.7\ \mu F \tag{6.6}$$

Figure 6.3 shows the obtained simulation results for the four output voltages of the DC/DC proposed converter.

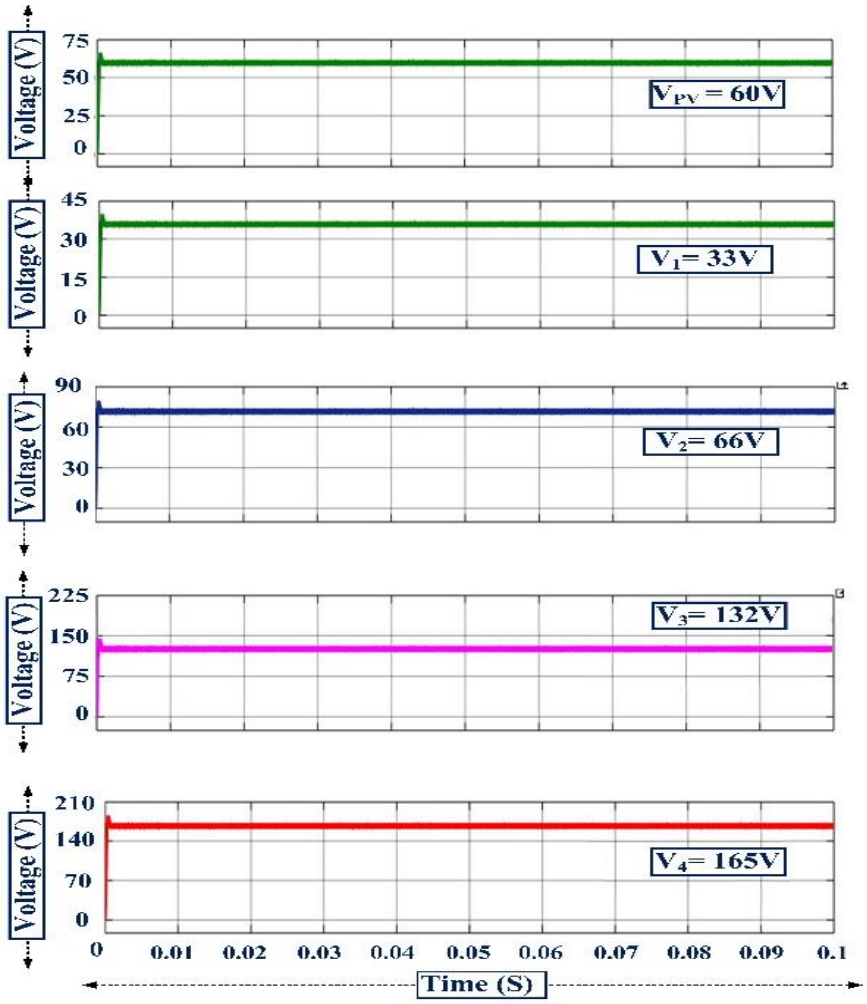


Figure 6.3 Output voltage of the solar PV generator and the DC/DC buck-boost converter

Finally, and assuming V_{Omax} = 400 V as the maximum MLI output voltage, the expression utilized to determine the minimum step of the DC/DC buck-boost converter (V_{Ostep}) is shown in Equation (6.7), where *nl* is the MLI inverter number of output voltage levels.

$$V_{Ostep} = \frac{V_{Omax}}{\frac{nl-1}{2}} \rightarrow V_{Ostep} = \frac{800}{nl-1} \tag{6.7}$$

The minimum voltage step for the 15-level MLI is VOstep-15 ≈ 57 V, and for the 25-level MLI, it is VOstep-25 ≈ 33 V. Table 6.3 summarizes the output voltage values of the DC/DC buck-boost converter for the two proposed MLIs. Note that the 15-level MLI needs three asymmetrical DC voltages, while the 25-level MIL needs four (Table 6.3).

Table 6.3 DC asymmetric voltages are used in the proposed MLI.

DC voltage	15-level	25-level
V_1	57 V	33 V
V_2	114 V	66 V
V_3	228 V	132 V
V_4	---	165 V

These results are based on the turns ratio specified for the transformer in the proposed circuit and the proposed duty cycle D = 0.53 in Equation (6.1). They can be calculated using Equation (6.8).

$$D = \frac{V_n}{n \cdot V_{pv} + V_n} \rightarrow D = \frac{165}{2.5 \cdot 60 + 165} = \cdots = \frac{33}{0.5 \cdot 60 + 33} \approx 0.53 \quad (6.8)$$

The design of the DC/DC buck-boost converter proposed as a frontend for the presented 15-level MLI is not included, but it is similar to the procedure given in this section for the characterization of the iSEPIC proposed as a frontend for the 25-level MLI.

6.3. Proposed Multilevel Inverters

This section presents the two proposed MLIs. The characterization of the MLIs is based on a simplified circuit because the main objective of this work is to evaluate the advantages of the proposed design. The proposed DC/DC buck-boost converter is not used for this characterization, and the asymmetrical voltages for the MLI are obtained from independent DC sources. Furthermore, the load used in the MLI characterization is not the grid. In this case, a resistive and resistive-inductive load is used.

6.3.1. Asymmetrical 15-level MLI

Figure 6.4 shows the proposed 15-level MLI, which consists of eleven switches, S_1 through S_{11}, and three voltage sources, labeled V_1, V_2, and V_3. The three DC sources are stacked asymmetrically due to their different voltage levels and are by the values reported in Table 6.3. The proposed MLI architecture minimizes the number of power quality issues and achieves lower Total Stating Voltage (TSV) compared to other proposed topologies in the specialized literature.

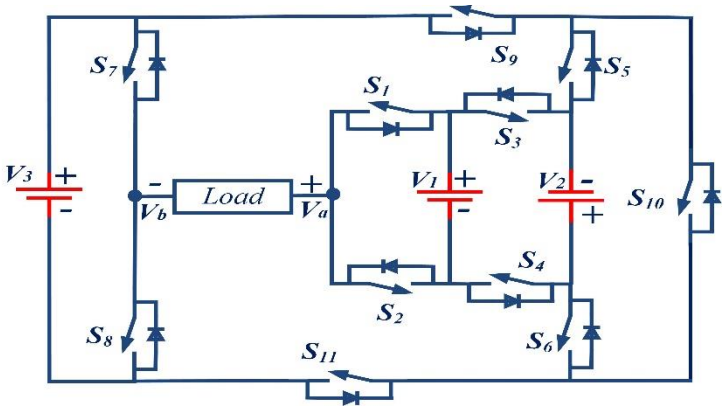


Figure 6.4 Topology of the proposed 15-level MLI.

Table 6.4 depicts the main characteristics of the 15 operation modes (or level states) of the proposed 15-level MLI. The state of each switch (mark "√" denotes the ON state) in each level state, the active DC sources, and the MLI output voltage are shown. The output voltage column displays the resulting voltage for the corresponding switching state, ranging from $-7 \cdot V_{Ostep\text{-}15}$ to $+7 \cdot V_{Ostep\text{-}15}$ in increments of $V_{Ostep\text{-}15}$. This range of output voltages allows for versatile applications and precise control over the system's output.

Table 6.4 Switching table for the 15-Level MLI.

Level	Switches state											Active DC sources	Output Voltage
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}		
L1	√			√	√			√	√			$V_1 + V_2 + V_3$	$+7 \cdot V_{Ostep\text{-}15}$
L2		√		√	√			√	√			$V_2 + V_3$	$+6 \cdot V_{Ostep\text{-}15}$
L3	√			√		√		√	√	√		$V_1 + V_3$	$+5 \cdot V_{Ostep\text{-}15}$
L4	√		√		√			√	√			V_3	$+4 \cdot V_{Ostep\text{-}15}$
L5	√			√	√		√		√			$V_1 + V_2$	$+3 \cdot V_{Ostep\text{-}15}$
L6		√		√	√			√		√	√	V_2	$+2 \cdot V_{Ostep\text{-}15}$
L7	√			√		√		√			√	V_1	$+V_{Ostep\text{-}15}$
L8	√		√		√			√		√	√	---	0
L9		√	√		√			√		√	√	$-V_1$	$-V_{Ostep\text{-}15}$
L10	√		√			√		√			√	$-V_2$	$-2 \cdot V_{Ostep\text{-}15}$

L11		√	√			√		√			√	$-(V_1 + V_2)$	$-3 \cdot V_{Ostep-15}$
L12		√		√		√	√				√	$-V_3$	$-4 \cdot V_{Ostep-15}$
L13		√	√		√		√			√	√	$-(V_1 + V_3)$	$-5 \cdot V_{Ostep-15}$
L14	√		√			√	√				√	$-(V_2 + V_3)$	$-6 \cdot V_{Ostep-15}$
L15		√	√			√	√				√	$-(V_1 + V_2 + V_3)$	$-7 \cdot V_{Ostep-15}$

Figure 6.5 shows the obtained results from the simulation of the proposed 15-level MLI operation. Switches are in a "1" state if turned ON; otherwise, they are in a "0" state. The MLI provides an output voltage of 400 V using a 100 Ω resistor as load.

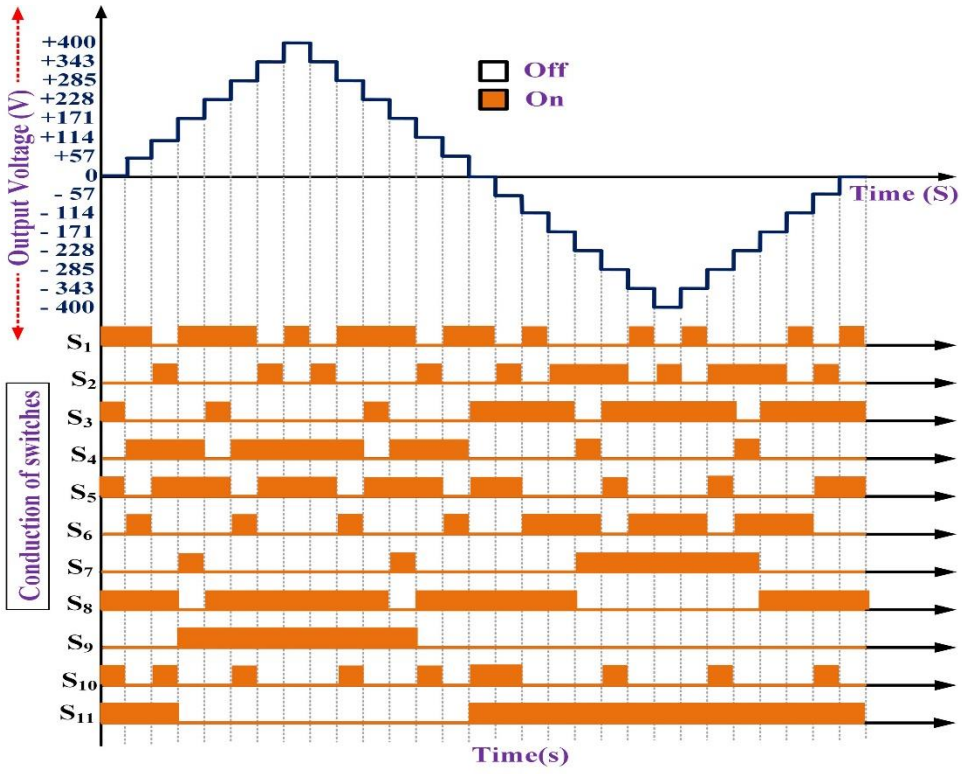


Figure 6.5 Operating modes of the proposed 15-level MLI topology.

6.3.2. Asymmetrical 25-level MLI

Figure 6.6 shows the proposed 25-level MLI topology. The system comprises eleven switches, S_1 through S_{11}, and four voltage sources, labeled V_1, V_2, V_3, and V_4. The four DC sources are stacked asymmetrically due to their different voltage levels and are by the values reported in Table 6.3.

The proposed MLI architecture minimizes the number of power quality issues and achieves lower Total Stating Voltage (*TSV*) compared to other similar topologies proposed in the specialized literature.

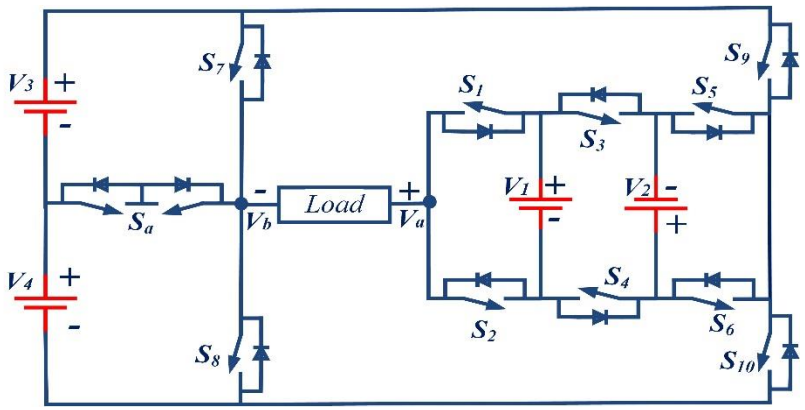


Figure 6.6 Topology of the proposed 25-level MLI.

Table 6.5 depicts the main characteristics of the 25 operation modes (or level states) of the proposed 25-level MLI. The state of each switch (mark "√" denotes the ON state) in each level state, the active DC sources, and the MLI output voltage are shown. The output voltage column displays the resulting voltage for the corresponding switching state, ranging from $-12 \cdot V_{Ostep-25}$ to $+12 \cdot V_{Ostep-25}$ in increments of $V_{Ostep-25}$. This range of output voltages allows for versatile applications and precise control over the system's output.

Table 6.5 Switching table for the 25-level MLI.

Level	**Switching States**											**Active DC sources**	**Output voltage**
	S_a	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}		
L1		√			√	√			√	√		$V_1 + V_2 + V_3 + V_4$	$+12 \cdot V_{Ostep-25}$
L2			√		√	√			√	√		$V_2 + V_3 + V_4$	$+11 \cdot V_{Ostep-25}$
L3		√			√		√		√	√		$V_1 + V_3 + V_4$	$+10 \cdot V_{Ostep-25}$
L4		√		√		√			√	√		$V_3 + V_4$	$+9 \cdot V_{Ostep-25}$
L5			√	√		√			√	√		$-V_1 + V_3 + V_4$	$+8 \cdot V_{Ostep-25}$
L6	√			√	√	√				√		$V_1 + V_2 + V_3$	$+7 \cdot V_{Ostep-25}$

L7	√		√		√	√				√		$V_2 + V_3$	$+ 6 \cdot V_{Ostep-25}$
L8	√	√			√		√			√		$V_1 + V_3$	$+ 5 \cdot V_{Ostep-25}$
L9	√	√		√		√				√		V_3	$+ 4 \cdot V_{Ostep-25}$
L10		√			√	√			√		√	$V_1 + V_2$	$+ 3 \cdot V_{Ostep-25}$
L11			√		√	√			√		√	V_2	$+ 2 \cdot V_{Ostep-25}$
L12		√			√		√		√		√	V_1	$+ 1 \cdot V_{Ostep-25}$
L13		√		√		√			√		√	---	0
L14			√	√		√		√		√		$- V_1$	$- 1 \cdot V_{Ostep-25}$
L15		√		√			√	√		√		$- V_2$	$- 2 \cdot V_{Ostep-25}$
L16			√	√			√	√		√		$- (V_1 + V_2)$	$- 3 \cdot V_{Ostep-25}$
L17	√	√			√		√				√	$V_1 - V_4$	$- 4 \cdot V_{Ostep-25}$
L18	√		√		√		√				√	$- V_4$	$- 5 \cdot V_{Ostep-25}$
L19	√		√	√		√					√	$- (V_1 + V_4)$	$- 6 \cdot V_{Ostep-25}$
L20	√	√		√			√				√	$- (V_2 + V_4)$	$- 7 \cdot V_{Ostep-25}$
L21	√		√	√			√				√	$- (V_1 + V_2 + V_4)$	$- 8 \cdot V_{Ostep-25}$
L22			√		√		√	√			√	$- (V_3 + V_4)$	$- 9 \cdot V_{Ostep-25}$
L23			√	√		√		√			√	$- (V_1 + V_3 + V_4)$	$- 10 \cdot V_{Ostep-25}$
L24		√		√			√	√			√	$- (V_2 + V_3 + V_4)$	$- 11 \cdot V_{Ostep-25}$
L25			√	√			√	√			√	$- (V_1 + V_2 + V_3 + V_4)$	$- 12 \cdot V_{Ostep-25}$

Figure 6.7 shows the obtained simulation results of the proposed 25-level MLI operation. Switches are in a "1" state if turned ON; otherwise, they are in a "0" state. The MLI provides an output voltage of 400 V using a 100 Ω resistor as load.

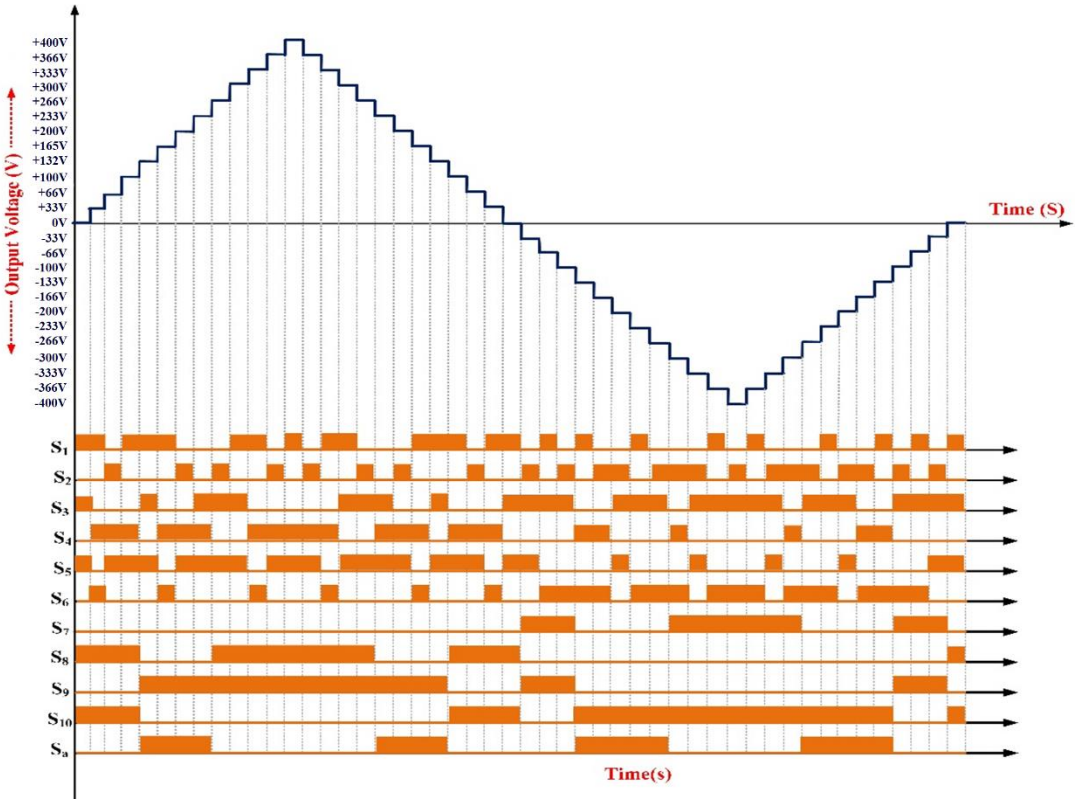


Figure 6.7 Operating modes of the proposed 25-level MLI topology.

6.4. MLI Performance Evaluation

Evaluating the performance of multilevel inverters is crucial for optimizing their efficiency and cost-effectiveness in various applications. Total standing voltage (*TSV*), representing the sum of voltage levels in the inverter, is a crucial metric in assessing its output quality and harmonic content. Additionally, the component count per level factor offers insights into the complexity and scalability of the inverter design, impacting both manufacturing and maintenance costs.

Cost functions provide a comprehensive framework for assessing the economic viability of different multilevel inverter configurations, considering factors such as component prices, assembly expenses, and operational costs. Furthermore, analyzing power loss and efficiency helps quantify energy conversion losses and overall system effectiveness, guiding design choices toward achieving optimal performance with minimal energy wastage. Integrating these metrics facilitates comprehensive performance evaluation, enabling engineers to refine multi-level inverter designs for enhanced functionality and sustainability.

6.4.1. Total Standing Voltage and Component Count per Level Factor

The *TSV* significantly influences the circuit's switch choice. The blocking voltage for all the semiconductors in the layout is added up to produce this value. Calculating the *TSV* involves determining the total maximum blocking voltages (*MBV*) across all switches (from $i = 1, 2, 3, \ldots, m$), which is derived from Equation (6.9).

$$TSV = \sum_{i=1}^{m} MBV_{Si} = MBV_{S1} + MBV_{S2} + MBV_{S3} + \cdots + MBV_{Sn} \tag{6.9}$$

The *TSV* per unit (TSV_{PU}), representing the ratio of the overall *TSV* to the maximum voltage levels of the proposed MLI, can be mathematically derived using Equation (6.10).

$$TSV_{PU} = \frac{TSV}{V_{Omax}} \tag{6.10}$$

The normalized voltage stress (*NVS*) compares the voltage stress experienced by a single switch and the maximum stress endured by the circuit, as determined by Equation (6.11).

$$NVS = \frac{Voltage\ stress\ across\ switch}{Maximum\ voltage\ stress\ in\ the\ circuit} \tag{6.11}$$

6.4.1.1. TSV of 15 levels MLI

The 15-level MLI has 11 unidirectional switches. The maximum voltage stress (or *MBV*) across the unidirectional switches is MBV_{Si}, where $i = 1, 2, 3, \ldots, n$. The stress across each unidirectional switch is represented as follows:

$MBV_{S1} = V_1 = 1 \cdot V_{Ostep\text{-}15}$

$MBV_{S2} = V_1 = 1 \cdot V_{Ostep\text{-}15}$

$MBV_{S3} = V_1 + V_2 = 3 \cdot V_{Ostep\text{-}15}$

$MBV_{S4} = V_2 + V_1 = 3 \cdot V_{Ostep\text{-}15}$

$MBV_{S5} = V_2 = 2 \cdot V_{Ostep\text{-}15}$

$MBV_{S6} = V_2 = 2 \cdot V_{Ostep}\text{-}15$

$MBV_{S7} = V_3 = 4 \cdot V_{Ostep\text{-}15}$

$MBV_{S8} = V_3 = 4 \cdot V_{Ostep\text{-}15}$

$MBV_{S9} = V_1 = 1 \cdot V_{Ostep\text{-}15}$

$MBV_{S10} = V_2 = 2 \cdot V_{Ostep\text{-}15}$

$MBV_{S11} = V_1 = 1 \cdot V_{Ostep\text{-}15}$

And the *TSV* is calculated from the equation (6.12).

$$TSV = (1 + 1 + 3 + 3 + 2 + 2 + 4 + 4 + 1 + 2 + 1) \cdot V_{Ostep-15} = 24 \cdot V_{Ostep-15} \quad (6.12)$$

Table 6.6 depicts the voltage stress distribution across each power switch within a 15-level MLI, alongside the maximum stress. S_1, S_2, S_9, and S_{11} demonstrate the lowest and most normalized voltage stress (*NVS*) levels at $V_{Ostep\text{-}15}$ and 25%, respectively. On the other hand, S_5, S_6, and S_{10} experience twice this stress and *NVS*, each at $2 \cdot V_{Ostep\text{-}15}$ and 50%. Conversely, S_3 and S_4 endure triple this stress and *NVS*, rated at $3 \cdot V_{Ostep\text{-}15}$ and 75%, respectively. In contrast, S_7 and S_8 bear the highest voltage stress at $4 \cdot V_{Ostep\text{-}15}$, with an *NVS* of 100%.

Table 6.6 Normalized voltage stress for power switches of 15-level MLI

Switch	***MBV***	***NVS***	**Impact of stress on switches**
S_1	$1 \cdot V_{Ostep\text{-}15}$	$1 \cdot V_{Ostep\text{-}15}/4 \cdot V_{Ostep\text{-}15}$	25%
S_2	$1 \cdot V_{Ostep\text{-}15}$	$1 \cdot V_{Ostep\text{-}15}/4 \cdot V_{Ostep\text{-}15}$	25%
S_3	$3 \cdot V_{Ostep\text{-}15}$	$3 \cdot V_{Ostep\text{-}15}/4 \cdot V_{Ostep\text{-}15}$	75%
S_4	$3 \cdot V_{Ostep\text{-}15}$	$3 \cdot V_{Ostep\text{-}15}/4 \cdot V_{Ostep\text{-}15}$	75%
S_5	$2 \cdot V_{Ostep\text{-}15}$	$2 \cdot V_{Ostep\text{-}15}/4 \cdot V_{Ostep\text{-}15}$	50%
S_6	$2 \cdot V_{Ostep\text{-}15}$	$2 \cdot V_{Ostep\text{-}15}/4 \cdot V_{Ostep\text{-}15}$	50%
S_7	$4 \cdot V_{Ostep\text{-}15}$	$4 \cdot V_{Ostep\text{-}15}/4 \cdot V_{Ostep\text{-}15}$	100%
S_8	$4 \cdot V_{Ostep\text{-}15}$	$4 \cdot V_{Ostep\text{-}15}/4 \cdot V_{Ostep\text{-}15}$	100%
S_9	$1 \cdot \cdot V_{Ostep\text{-}15}$	$1 \cdot V_{Ostep\text{-}15}/4 \cdot V_{Ostep\text{-}15}$	25%
S_{10}	$2 \cdot \cdot V_{Ostep\text{-}15}$	$2 \cdot V_{Ostep\text{-}15}/4 \cdot V_{Ostep\text{-}15}$	50%
S_{11}	$1 \cdot \cdot V_{Ostep\text{-}15}$	$1 \cdot V_{Ostep\text{-}15}/4 \cdot V_{Ostep\text{-}15}$	25%

6.4.1.2. TSV of 25 levels MLI

The 25-MLI has 11 switches. One switch is bidirectional, and ten are unidirectional. Voltage stress across the bidirectional switches is half of the applied voltage, as stated in Equation (6.13).

$$MBV_{Sa} = \frac{V_3 + V_4}{2} = \frac{(4+5)\cdot V_{Ostep-25}}{2} = 4.5 \cdot V_{Ostep-25} \quad (6.13)$$

The maximum voltage stress (or *MBV*) across the unidirectional switches is MBV_{Si}, where i = 1, 2, 3, …, n. The stress across each unidirectional switch is represented as follows:

$MBV_{S1} = V_1 = 1 \cdot V_{Ostep-25}$

$MBV_{S2} = V_1 = 1 \cdot V_{Ostep-25}$

$MBV_{S3} = V_1 + V_2 = 3 \cdot V_{Ostep-25}$

$MBV_{S4} = V_1 + V_2 = 3 \cdot V_{Ostep-25}$

$MBV_{S5} = V_2 = 2 \cdot V_{Ostep-25}$

$MBV_{S6} = V_2 = 2 \cdot V_{Ostep-25}$

$MBV_{S7} = V_3 = 4 \cdot V_{Ostep-25}$

$MBV_{S8} = V_4 = 5 \cdot V_{Ostep-25}$

$MBV_{S9} = V_2 = 2 \cdot V_{Ostep-25}$

$MBV_{S10} = V_2 = 2 \cdot V_{Ostep-25}$

And the TSV is calculated from the equation (6.14).

$$TSV = (4.5 + 1 + 1 + 3 + 3 + 2 + 2 + 4 + 5 + 2 + 2) \cdot V_{Ostep-25} = 29.5 \cdot V_{Ostep-25} \quad (6.14)$$

Table 6.7 presents the voltage stress distribution among each power switch within a 25-level MLI, alongside the maximum stress. S_1 and S_2 exhibit the lowest and most normalized voltage stress (*NVS*) levels at $1 \cdot V_{Ostep-25}$ and 11.11%, respectively. S_5, S_6, S_9, and S_{10} encounter twice this stress and *NVS*, each at $2 \cdot V_{Ostep-25}$ and 22.22%. Meanwhile, S_3 and S_4 sustain triple this stress and *NVS*, rated at $3 \cdot V_{Ostep-25}$ and 33.33%, respectively. Among them, S_7 experiences the least stress and *NVS* at $4 \cdot V_{Ostep-25}$ and 44.44%, respectively. In contrast, S_8 faces the highest voltage stress at $5 \cdot V_{Ostep-25}$, with an *NVS* of 55.55%. Lastly, S_a registers a stress level of $4.5 \cdot V_{Ostep-25}$ with an *NVS* of 50%, representing half of the maximum *NVS.*

Table 6.7 Normalized voltage stress for power switches of 25-level MLI

Switches	***MBV***	***NVS***	**Impact of stress on switches**
S_a	$4.5 \cdot V_{Ostep-25}$	$4.5 \cdot V_{Ostep-25}/9 \cdot V_{Ostep-25}$	50%
S_1	$1 \cdot V_{Ostep-25}$	$1 \cdot V_{Ostep-25}/9 \cdot V_{Ostep-25}$	11.11%

S_2	$1 \cdot V_{Ostep\text{-}25}$	$1 \cdot V_{Ostep\text{-}25}/9 \cdot V_{Ostep\text{-}25}$	11.11%
S_3	$3 \cdot V_{Ostep\text{-}25}$	$3 \cdot V_{Ostep\text{-}25}/9 \cdot V_{Ostep\text{-}25}$	33.33%
S_4	$3 \cdot V_{Ostep\text{-}25}$	$3 \cdot V_{Ostep\text{-}25}/9 \cdot V_{Ostep\text{-}25}$	33.33%
S_5	$2 \cdot V_{Ostep\text{-}25}$	$2 \cdot V_{Ostep\text{-}25}/9 \cdot V_{Ostep\text{-}25}$	22.22%
S_6	$2 \cdot V_{Ostep\text{-}25}$	$2 \cdot V_{Ostep\text{-}25}/9 \cdot V_{Ostep\text{-}25}$	22.22%
S_7	$4 \cdot V_{Ostep\text{-}25}$	$4 \cdot V_{Ostep\text{-}25}/9 \cdot V_{Ostep\text{-}25}$	44.44%
S_8	$5 \cdot V_{Ostep\text{-}25}$	$5 \cdot V_{Ostep\text{-}25}/9 \cdot V_{Ostep\text{-}25}$	55.55%
S_9	$2 \cdot V_{Ostep\text{-}25}$	$2 \cdot V_{Ostep\text{-}25}/9 \cdot V_{Ostep\text{-}25}$	22.22%
S_{10}	$2 \cdot V_{Ostep\text{-}25}$	$2 \cdot V_{Ostep\text{-}25}/9 \cdot V_{Ostep\text{-}25}$	22.22%

6.4.2. Component Count per Level Factor and Cost Functions

Inverters with low *TSV* values are based on switches with low maximum blocking voltages, which reduces construction costs. The element count level factor is also considered to obtain the number of partial elements involved in the inverter's construction. The component count factor represents the number of semiconductors used in a circuit. A reduced number of semiconductors will reduce the circuit resistance, which reduces losses and increases system efficiency. The component count per level factor (F_{CCL}) is calculated from equation (6.15).

$$F_{CCL} = \frac{N_S + N_D + N_C + N_{DK} + ng}{N_L} \tag{6.15}$$

Where N_S stands for the number of switches, N_D stands for the number of diodes, N_C stands for the number of capacitors, N_{DK} stands for the number of gate driver circuits, *ndc* is the number of DC sources used in the circuit, and N_L stands for the number of levels of the considered MLI.

The use of a cost function of MLI is an essential factor when comparing MLI in terms of possible economic cost. Equation (6.16) formulates the cost function (*CF*) to characterize the proposed MLI. Parameters such as the total standing voltage and the component count factor are used in its definition [55].

$$CF = N_S + N_{DK} + ndc + N_D + N_C + \alpha \cdot TSV_{PU} \tag{6.16}$$

TSVPU is the total standing voltage per unit, calculated by Equation (6).

The parameter α in Equation (6.15) is a weight coefficient that multiplies the total standing voltage per unit. This work has considered two possible values for this coefficient: one less than unity (α = 0.5) and another greater than one (α = 1.5).

Since neither diodes nor capacitors are used in the suggested MLI topologies, the cost function described in Equation (6.15) can be simplified to that presented in Equation (6.17).

$$CF = N_S + N_{DK} + ndc + \alpha \cdot TSV_{PU} \tag{6.17}$$

Finally, the proposed MLI's cost-effectiveness is determined using the cost function per level (CFL), that is, the value of the cost function determined by Equation (6.16) divided by the number of levels of the MLI considered, as shown in Equation (6.18).

$$CF_L = \frac{N_S + N_{DK} + ndc + N_D + N_C + \alpha \cdot TSV_{PU}}{N_L} \tag{6.18}$$

6.4.3. Power Loss and Efficiency

Switch-related conduction losses and switching losses make up the total switch losses. Equation (6.19) is used to determine the conduction losses (P_{cl}) for each switch [55].

$$P_{cl}(t) = \left[V_S + R_S i^{\beta}(t)\right] \cdot i(t) \tag{6.19}$$

Where i is the peak output current, R_S is the conduction resistance of the switch (in ON-state), V_S is the voltage drop across the switch, and β is a switch specification constant provided by the manufacturer. It is a critical parameter for accurately modeling and understanding the power loss characteristics of a switch. It allows us to predict how the power loss will scale with the current, which is vital for optimizing power electronic systems' efficiency and thermal management. Equation (6.20) provides the generalized relation for calculating the average conduction power losses (P_{CL}), considering the number of switches (N_{SW}) conducting at the same time (t) to produce each level.

$$P_{CL} = \frac{1}{2\pi}\int_0^{2\pi} [N_{SW}(t) \cdot P_{cl}(t)]\, dt \tag{6.20}$$

The switching losses (P_{SL}) can be calculated using Equation (6.21).

$$P_{SL} = f\left[\sum_{q=1}^{N_{SW}} \left(\sum_{i=1}^{N_{ON}} E_{ONqi} + \sum_{i=1}^{N_{OFF}} E_{OFFqi}\right)\right] \tag{6.21}$$

Where f is the fundamental frequency, N_{ON} and N_{OFF} are the number of times the switch q turns ON or OFF in one fundamental cycle, and E_{ON} and E_{OFF} are the turn-on and turn-off energy loss, respectively.

The total power losses (P_{TL}) are calculated from the Equation (6.22):

$$P_{TL} = P_{CL} + P_{SL} \tag{6.22}$$

And the efficiency (η) of the MLI is calculated from the Equation (6.23):

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT} + P_{TL}} \tag{6.23}$$

Where POUT and PIN are the MLI output and input powers. Finally, the output inverter power (POUT) can be estimated from Equation (6.24), where VRMS and IRMS are the root mean square values of the output voltage and current, respectively.

$$P_{OUT} = V_{RMS} \cdot I_{RMS} \tag{6.24}$$

6.4.4. Comparative studies

This section compares the proposed MLI with other multi-level inverters proposed in previous research works.

6.5. Proposed 15-level MLI

It is noticed that the proposed 15-level MLI architecture is less expensive than other modern designs. Table 6.8 compares the proposed MLI to several present topologies by considering essential elements such as the number of switches, used DC sources, gate driver circuits, capacitors, overall standing voltage, and components at each level. When overall standing voltage is compared to the other topologies, it is found that the proposed design has the smallest value. The proposed 15-level MLI has a low value of cost function per level, 1.65 and 1.88, for the values of α 0.5 and 1.5, respectively.

Table 6.8 Characteristics of 15-level MLI designs

Reference	N_L	N_S	N_{DK}	**ndc**	N_D	N_C	F_{CCL}	TSV_{PU}	CF_L	
									α = 0.5	α = 1.5
[41]	15	16	16	7	-	-	2.60	-	-	-
[42]	15	10	10	5	2	-	1.80	1.06	1.84	1.91
[43]	15	10	10	5	-	-	1.66	-	-	-
[44]	15	10	10	4	-	-	1.60	4.60	1.75	2.06

Proposed MLI	15	10	10	3	-	-	1.53	3.42	1.65	1.88

Figure 6.8 provides a comparative analysis of different 15-level MLI topologies. Each subfigure (a to f) illustrates a distinct aspect of the MLI topologies, comparing the references [41 – 44] and the proposed system. (a) Switches count (N_S): This bar chart displays the number of switches used in each topology. The proposed system shows a significantly reduced count of switches compared to the reference topologies, indicating a more efficient design that could result in lower cost and potentially higher reliability. (b) DC sources count (*ndc*): This graph illustrates the number of DC sources required for each topology. Again, the proposed system uses fewer DC sources than the other topologies, suggesting improved power efficiency and reduced complexity in the power supply design. (c) Gate driver circuits count (N_{DK}): Here, the number of gate driver circuits is compared. The proposed topology requires the fewest gate driver circuits, which could lead to a simple control scheme and possibly lower operational costs. (d) Total System Volume (*TSV*): This bar chart indicates the TSV for each topology. The proposed system has a notably lower *TSV*, implying better space utilization, which is crucial in applications where the inverter size is a limiting factor. (e) Component count per level (F_{CCL}): This plot shows the component count per level. The proposed system demonstrates a lower count, indicating a less complex system per level, which might contribute to ease of maintenance and scalability. (f) Cost function per level count (CF_L): The final chart compares the cost function per level, with the proposed system showing a marginally higher cost per level but still within a competitive range. Overall, the proposed system appears to outperform the referenced topologies regarding reduced component counts and system volume, which are beneficial for creating more compact, cost-effective, and efficient inverters. The slight increase in the cost function per level for the proposed system might be justified by the benefits in other areas.

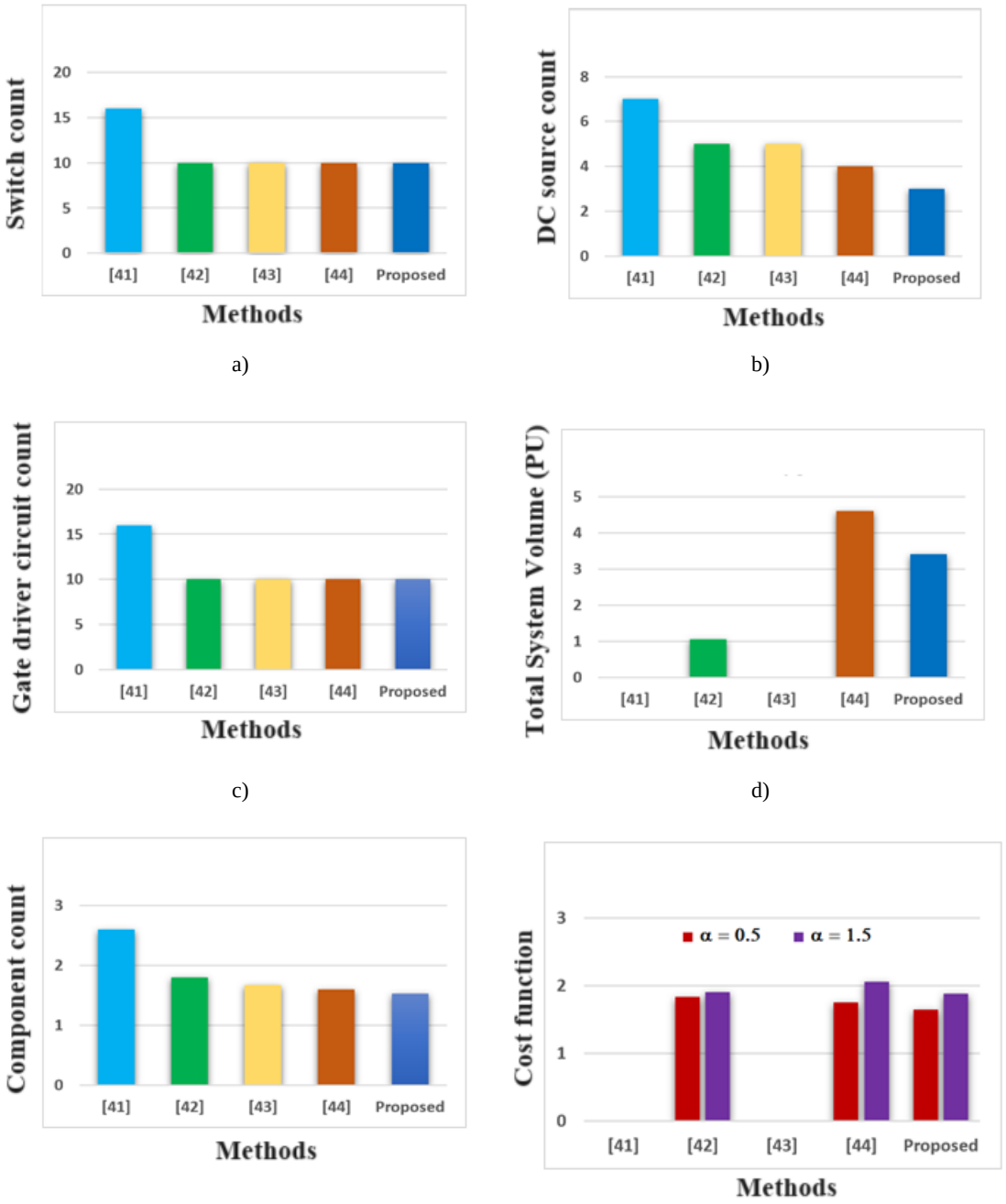


Figure 6.8 Comparison of various 15-level MLI topologies. a) Switches count, b) DC sources count, c) Gate driver circuits count, d) TSV, e) Component count per level, f) Cost function per level.

6.6. Proposed 25-level MLI

The proposed 25-level MLI architecture is less expensive than other modern designs. Table 6.9 compares the proposed MLI with different current configurations while adjusting for critical

elements like the number of switches, the amount of DC sources, the amount of gate driver circuits, the number of capacitors, the quantity of overall standing output power, and the number of components per level. In comparison, the proposed 25-level MLI reports a low THD value of 3.20 in contrast to the THD reported in [28], [33], and [34] using a switch count of 10 to14 and has a least-cost function value as tabulated in Table 6.9.

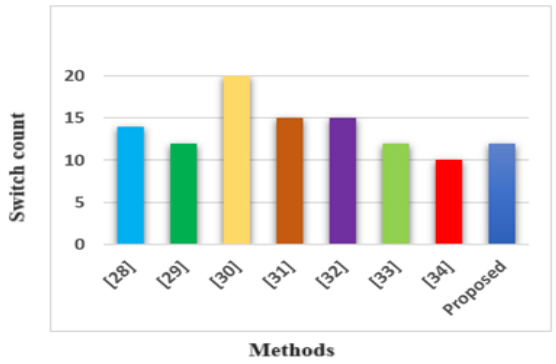
Table 6.9 Characteristics of 25-level MLI designs

Reference	N_L	N_S	N_{DK}	*ndc*	N_D	N_C	F_{CCL}	TSV_{PU}	***THD (%)***	CF_L	
										$\alpha = 0.$	$\alpha = 1.$
[28]	25	14	10	4	-	4	1.28	6.16	4.38	1.40	1.65
[29]	25	12	10	4	-	-	1.04	5.00	-	1.14	1.34
[30]	25	20	16	8	-	-	1.76	3.33	-	1.83	1.96
[31]	25	15	15	6	-	-	1.44	4.50	-	1.53	1.71
[32]	25	15	15	3	-	3	1.44	2.00	-	1.48	1.56
[33]	25	12	12	2	-	2	1.12	4.00	4.20	1.20	1.36
[34]	25	10	10	4	8	-	1.28	4.50	3.26	1.37	1.55
Proposed MLI	25	11	11	4	-	-	1.04	2.87	3.20	1.10	1.21

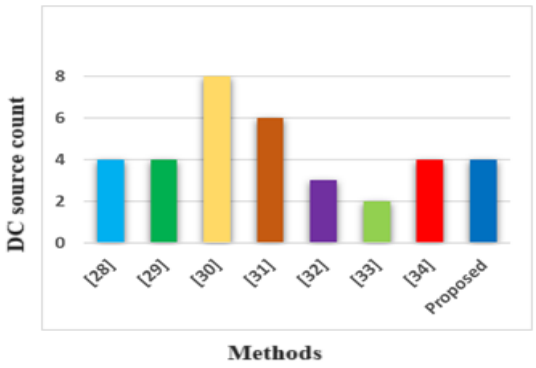
Figure 6.9 compares 25-level MLI topologies, including several references and a proposed system. Each subfigure (a-f) targets a specific parameter: a) Switches count (N_S): The bar chart suggests that the proposed system requires a higher number of switches compared to some reference topologies but is on par or better than others. A higher switch count can correlate with greater control over the output but may also imply higher costs and complexity. b) DC sources count (*ndc*): The DC source requirement is substantially less for the proposed system, implying a significant improvement over the other referenced designs. Fewer DC sources could mean lower costs and a more straightforward power management system. c) Gate driver circuits count (N_{DK}): The proposed topology shows a moderate number of gate driver circuits needed, which indicates a balance between control complexity and hardware requirements. d) Total System Volume (*TSV*): The proposed system ranks in the middle range regarding *TSV*. This indicates that while it's not the most compact, it maintains a reasonable balance between size and functionality. e) Components count per level (F_{CCL}): For the number of components per level, the proposed system appears to

use more components than some of the reference models but fewer than others. This could indicate a design that favors performance or flexibility at the cost of increased parts. f) Cost function per level (C_{FL}): The cost function analysis shows two scenarios for the proposed system: one with a significance level of 0.5 and one with 1.5. In both cases, the proposed system's cost function is higher than all reference topologies, suggesting that while it may offer benefits in other areas, it comes at a higher cost.

In summary, Figure 6.9 indicates that the proposed 25-level MLI system has been designed with inevitable trade-offs in mind. While it improves upon the number of DC sources needed and has a competitive *TSV*, these come at the expense of a higher cost function and an increased number of switches and components per level. These trade-offs could reflect a design optimized for performance or specific application requirements rather than purely for cost or component minimization.



a)



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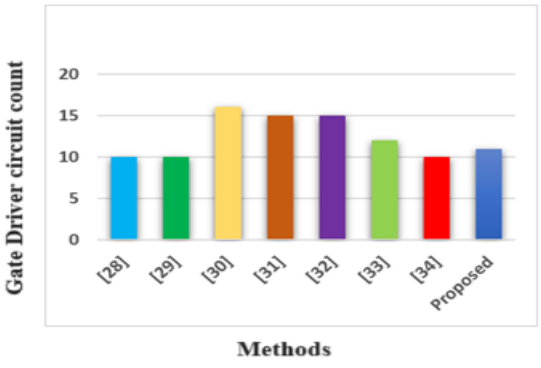

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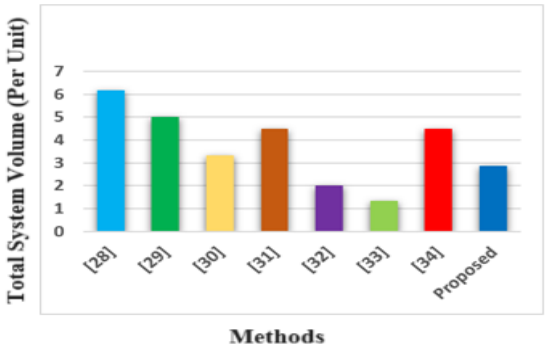
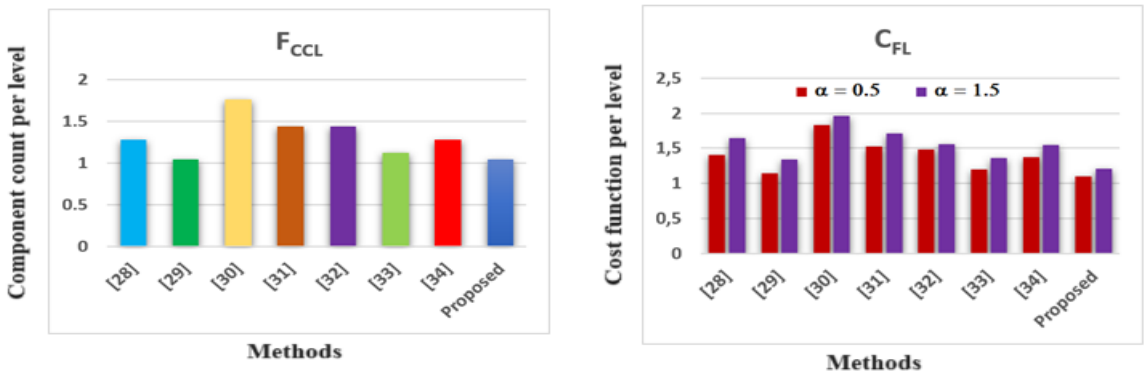


d)



e) f)

Figure 6.9 Comparison of various 25-level MLI topologies. a) Switches count, b) DC sources count, c) Gate driver circuits count, d) TSV, e) Component count per level, f) Cost function per level

6.7. Simulation and Experimental Results

This section shows the results obtained in the simulations and the laboratory tests on the proposed MLI.

6.7.1. Proposed 15-level MLI

Using MATLAB/SIMULINK 2022a, the numerical simulations of the proposed 15-level MLI were performed. Figure 6.10 shows the voltage levels of switching states of the inverter output voltage. Figure 6.11 shows the inverter output voltage as V_O = 400 V and output current as I_O = 4 A, respectively (100 Ω resistor is used as load). According to Figure 6.12, the THD obtained using the FFT analysis is 3.35%. The numerical simulations are validated in the laboratory using an inverter arrangement. The prototype comprises three DC input sources (V_1, V_2, and V_3), eleven 3600 V, 75 A IGBTs, and a 100 Ω load resistor.

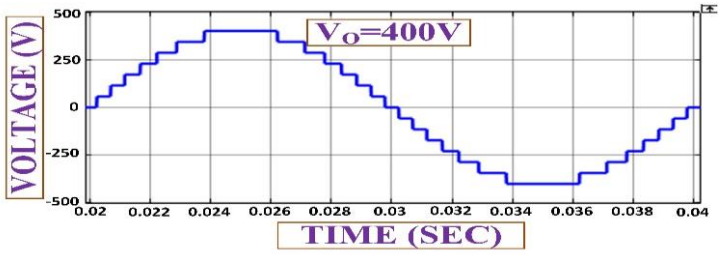


Figure 6.10 Simulation output voltage waveform of the proposed 15-level MLI

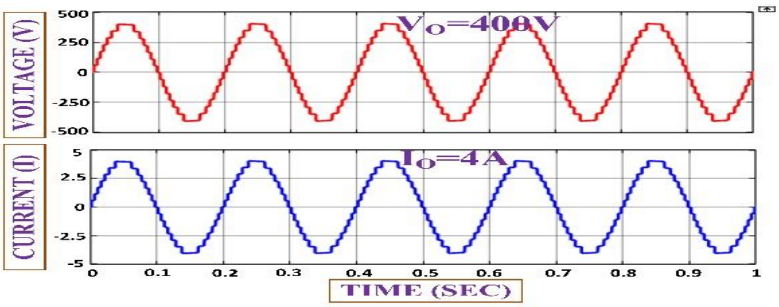


Figure 6.11 Simulation output voltage and current waveforms of the proposed 15-level MLI

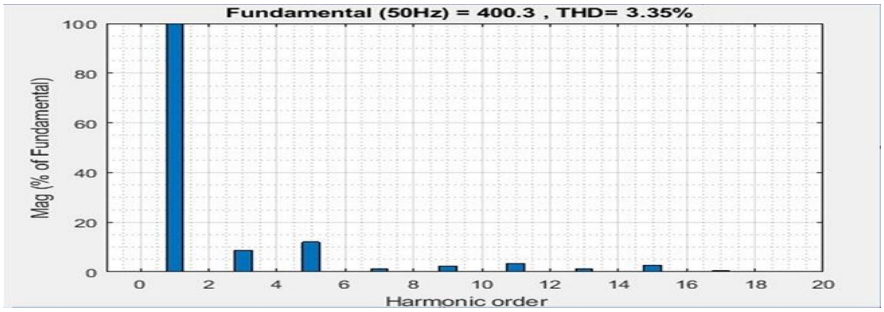


Figure 6.12 Simulation THD of proposed 15-level MLI

The dSPACE RTI1104 (Real-Time Interface) is a robust and versatile hardware-in-the-loop (HIL) system for real-time simulation and rapid control prototyping. It integrates seamlessly with MATLAB/SIMULINK, enabling engineers to efficiently develop and test control algorithms and embedded systems. The RTI1104 provides high-performance I/O capabilities, including analog and digital inputs and outputs, and various communication interfaces, making it ideal for applications in automotive, aerospace, industrial automation, and renewable energy sectors. Its real-time processing capabilities ensure that control systems can be tested under realistic conditions, reducing development time and enhancing the reliability and performance of the final product. By leveraging the dSPACE RTI1104, developers can quickly iterate on designs and validate them in a controlled, real-time environment, facilitating a smoother transition from simulation to physical implementation. Figure 6.13 displays the experimental results with the output voltage V_O = 400 V. Figure 6.14 displays the experimental results with the voltage V_O = 400 V and current I_O = 4 A for a resistive load of 100 Ω. According to IEEE standards, the experimentally measured THD, which is 3.32%, is displayed in Figure 6.15, and it is comparable to the modeling THD.

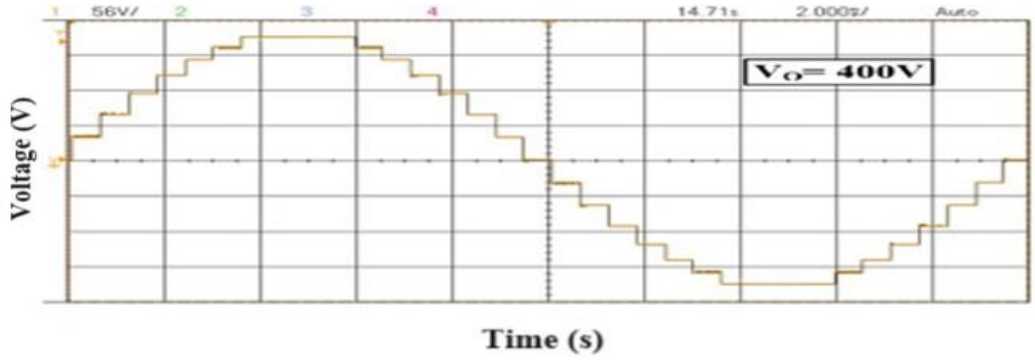


Figure 6.13 The experimental output voltage waveform of the proposed 15-level MLI

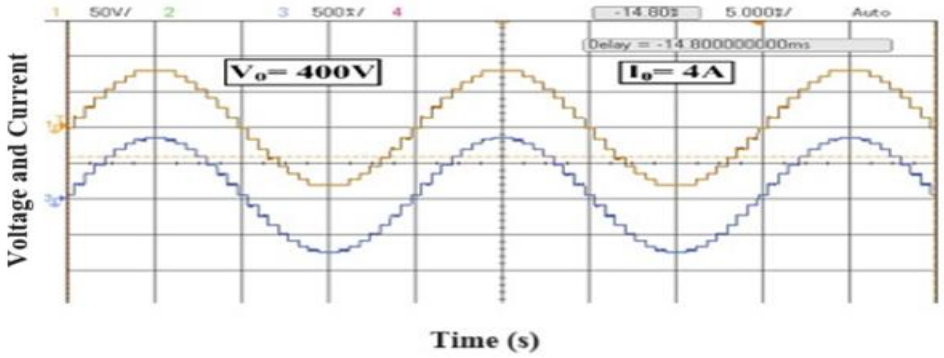


Figure 6.14 Experimental output voltage and current waveforms for R-load

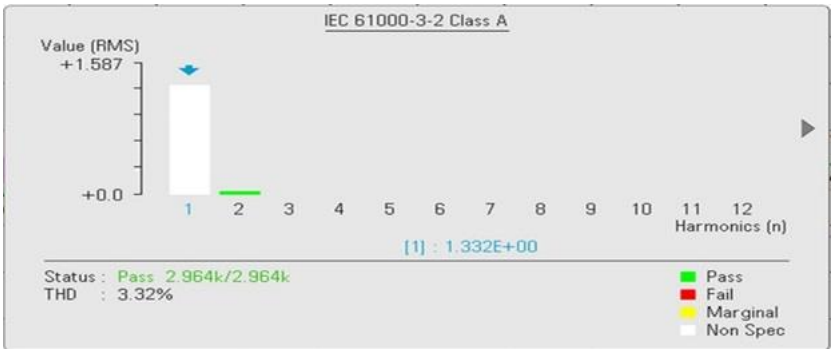


Figure 6.15 Experimental THD of proposed 15-level MLI

6.7.2. Proposed 25-level MLI

The proposed 25-level MLI simulation results are shown in Figure 6.16. Figure 6.17 represents the output voltage, V_O = 400 V, and current, I_O = 4 A. The THD obtained from the FFT analysis is 3.20%, displayed in Figure 6.18. A 25-level inverter prototype is used in the laboratory to experimentally evaluate and confirm the simulation results. The system has four input DC sources (V_1, V_2, V_3, and V_4), eleven 600 V, 75 A IGBTs (CM75DU-12), and a 100 Ω load resistor.

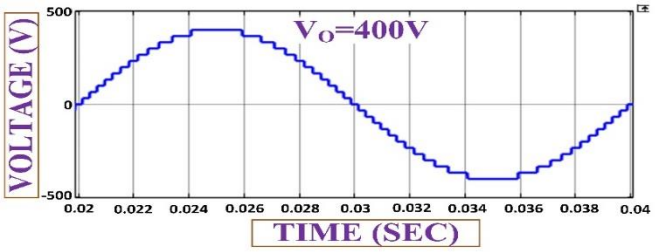


Figure 6.16 Simulation output voltage waveform of the proposed 25-level MLI

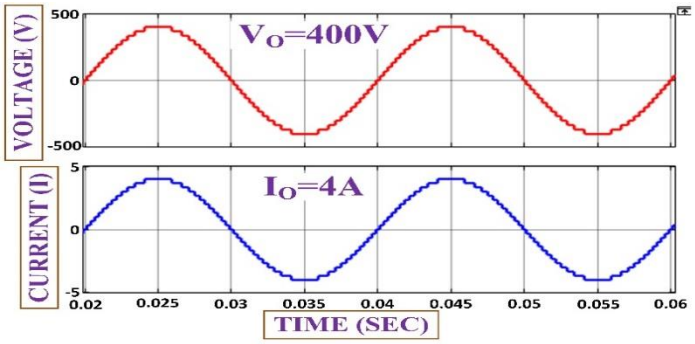


Figure 6.17 Simulation output voltage and current waveforms of the proposed 25-level MLI

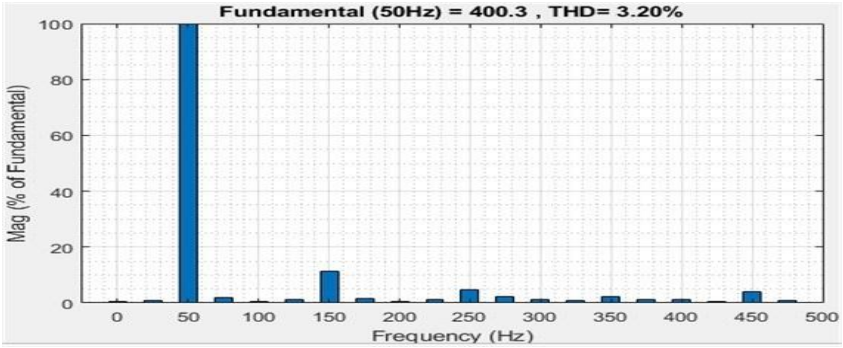


Figure 6.18 THD simulation of proposed 25-level MLI

The dSPACE RTI1104 processor's controller board generates pulses to control IGBTs by utilizing switching angles. Experimental outcomes are illustrated in Figure 6.19, where the output voltage is set at V_O = 400 V. Additionally, Figure 6.20 shows experimental results with V_O = 400 V and I_O = 4 A current for a 100 Ω resistor as load. Figure 6.21 exhibits the output voltage and current waveforms using a motor as an R-L load, featuring an inductance of L = 98 mH and an output current of 6.8 A. To assess the effectiveness of the proposed MLI, dynamic load transitions were examined for the R-L load configuration, as depicted in Figure 6.22. Furthermore, Figure 6.23 illustrates the behavior of the L-R load configuration under load disturbance conditions. As

indicated by Figure 6.24, the experimentally determined THD of 3.20% closely aligns with the modeled THD value.

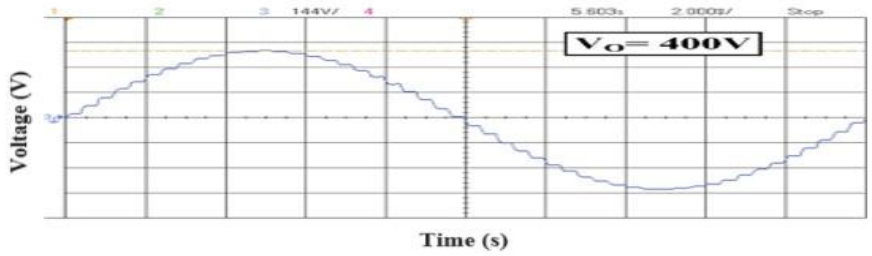


Figure 6.19 Experimental output voltage waveform of the proposed 25-level MLI

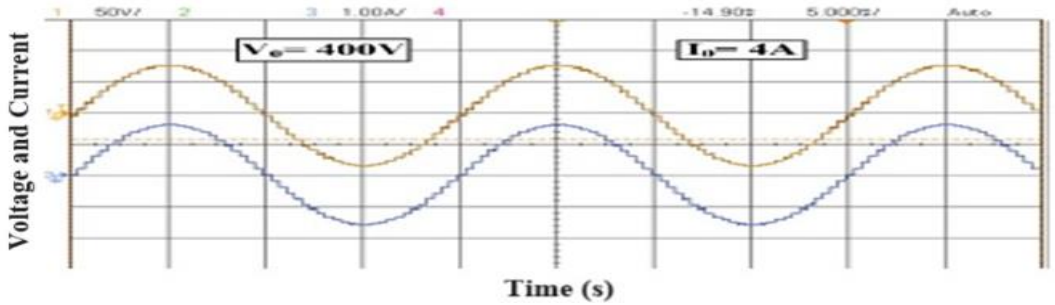


Figure 6.20 Experimental output voltage and current waveforms for R load

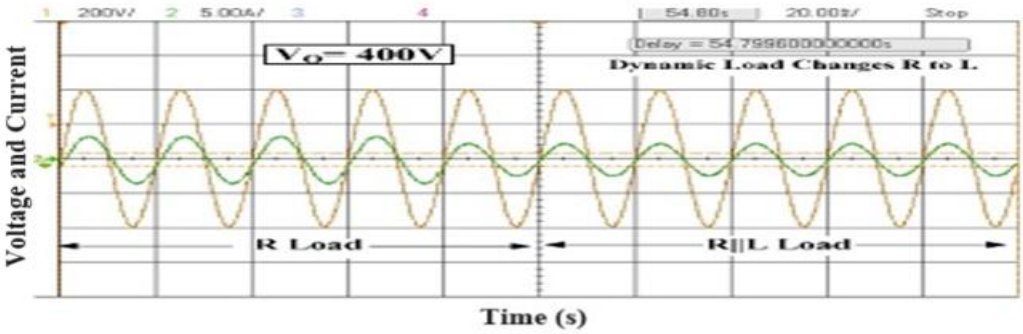


Figure 6.21 Experimental output voltage and current waveforms for R-L load

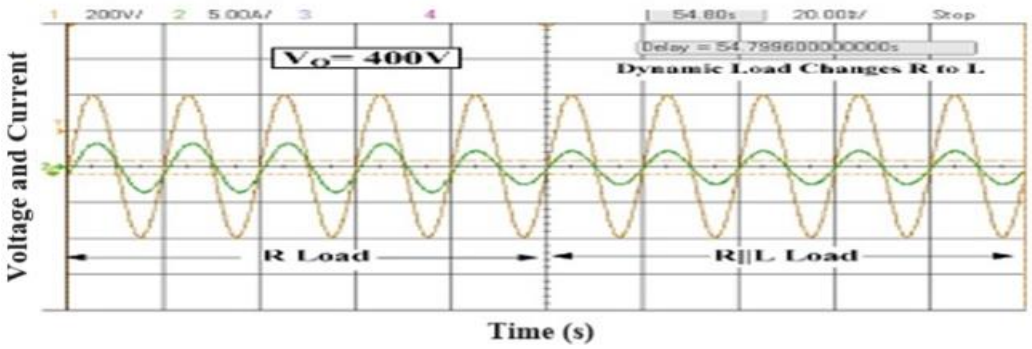


Figure 6.22 Experimental waveforms during dynamic load changes from R to R-L load

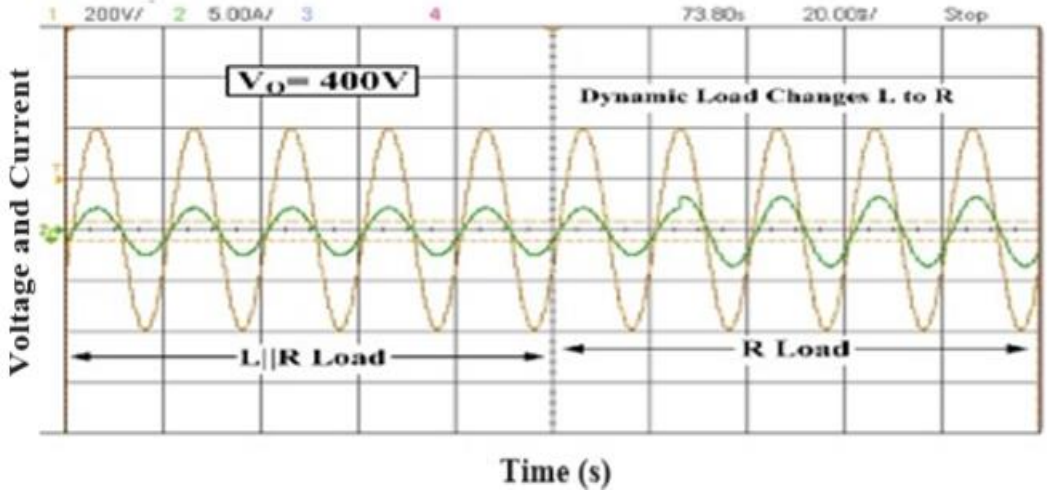


Figure 6.23 Experimental waveforms during dynamic load changes from R-L to R load

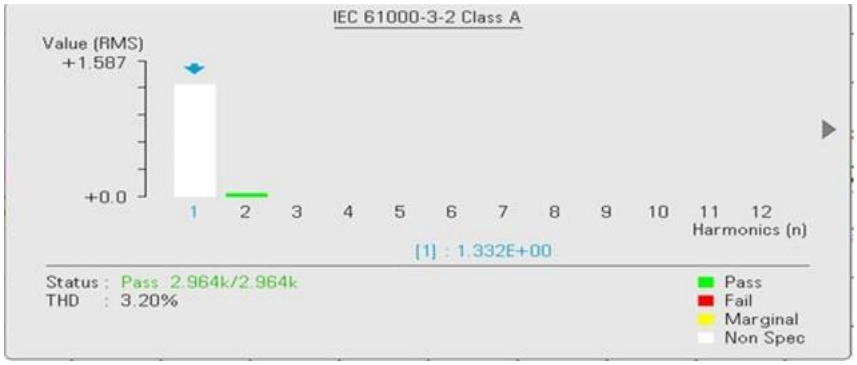


Figure 6.24 Experimental THD value of proposed 25-level MLI

Figure 6.25 depicts a practical setup of a multilevel inverter controlled by a dSPACE DS1104 controller. The multilevel inverter circuit is prominently visible in the central workspace, consisting of numerous power electronics components connected by a network of colored wires, which indicate the complex interconnections necessary for the inverter's operation. The dSPACE

DS1104 controller, placed on the right, is a real-time interface commonly used for control and automation tasks in power electronics and motor control applications. The oscilloscope and other measurement instruments are likely integrated into the setup to monitor the inverter's output waveform and ensure it meets the desired specifications. A computer running software, presumably for programming the dSPACE controller and analyzing data, is part of the setup. A resistive load and a motor suggest the system may be tested under various load conditions to evaluate its performance and efficiency in practical applications. This arrangement indicates an advanced experimental setup for research and development in power electronics and control systems.

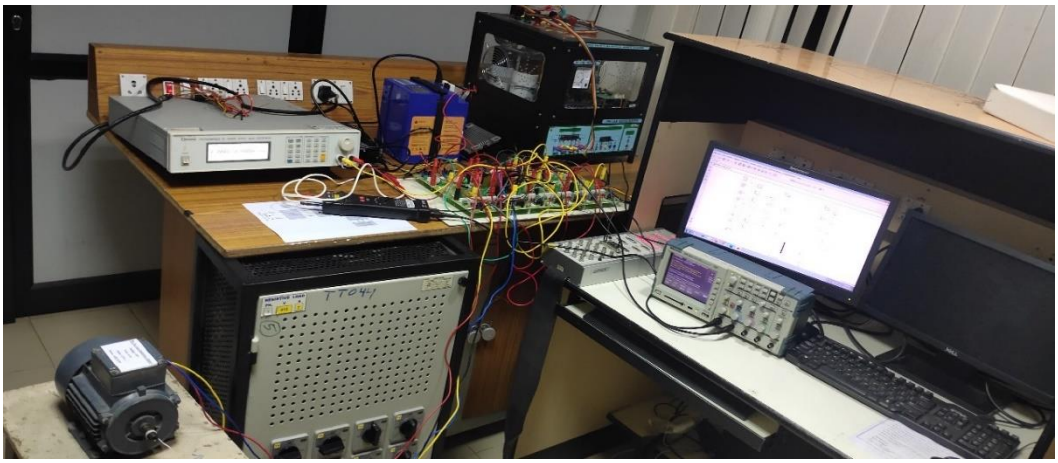


Figure 6.25 Experimental setup

6.7.3. Power losses and efficiency estimation in the proposed MLIs

Power loss and efficiency were calculated for both 15-level- and 25-level proposed MLI, considering R and R-L load. The conduction losses are computed using Equations (6.19) and (6.20). As an example, and in the case of the proposed 15-level MLI operating with R load, the obtained result is shown in Equation (6.25), where the values of R_S = 400 mΩ and V_S = 0.6 V are obtained from the IGBTs datasheet, and β = 1 is assumed for switches based on IGBT devices.

$$P_{CL} = [V_S + R_S \cdot I] \cdot I \cdot N_{SW} = [0.6 + 0.4 \cdot 2.82] \cdot 2.82 \cdot 11 = 53.60\ W \quad (6.25)$$

The switching losses of one switch q are calculated by applying Equations (6.21), where the turn-on (E_{ONq}) and turn-off (E_{OFFq}) energy losses are calculated by Equations (6.26) and (6.27), respectively [43].

$$E_{ONq} = \frac{1}{6} \cdot V_{SWq} \cdot I \cdot t_{on} \quad (6.26)$$

$$E_{OFFq} = \frac{1}{6} \cdot V_{SWq} \cdot I' \cdot t_{off} \quad (6.27)$$

Where the time to turn ON and OFF of the switch q are ton and toff, respectively, I and I' are the switch currents before and after turning ON and OFF, and V_{SWq} is the OFF-state switch voltage. The obtained results are presented in Table 6.10.

Table 6.10 Power loss and efficiency calculation for the proposed MLI.

Parameter	15-level		25-level	
	R Load	**R-L Load**	**R Load**	**R-L Load**
V_{RMS}	282.82 V	282.82 V	282.82 V	282.82 V
I_{RMS}	2.82 A	4,80 A	2.82 A	4.80 A
P_{OUT}	797.55 W	1357.54 W	797.55 W	1357.54 W
P_{CL}	53.60 W	133.06 W	53.60 W	133.06 W
P_{SL}	0.22 W	0.37 W	0.37 W	0.62 W
P_{TL}	53.82 W	133.43 W	53.97 W	133.68 W
P_{IN}	851.37 W	1490.97 W	851.52 W	1491.22 W
η	93.68 %	91.05 %	93.66 %	91.03 %

6.8. Summary

A novel asymmetrical 25-level MLI (multilevel inverter) topology and a 15-level topology are proposed utilizing fewer semiconductor switches. This design reduces the inverter's cost and size while improving its efficiency and reliability. The MLIs demonstrate low total harmonic distortion (THD) and can generate the required output voltage levels with minimal wastage. The total standing voltage (TSV) and cost function were computed by evaluating configurations with varying MLI quantities. The results indicate that the recommended MLI's lower TSV value enhances its competitiveness, speed, and cost-effectiveness. Experimental comparisons showed that the structure is highly suitable for grid-connected applications and dynamic voltage restorer (DVR) technologies, generating electricity with low harmonic content within IEEE standards. The

MLIs also performed well with renewable energy sources. Additionally, the availability of multiple isolated DC sources makes them useful for single-phase applications. This work is particularly promising for battery storage in standalone and alternative facilities, such as residential and hotel sectors.

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Chapter 7

Designing and Deploying 33-Level Multilevel Inverter: Mitigating Voltage Stress Through Asymmetrical Configuration

This chapter describes a new single-phase 33-level asymmetrical multilevel inverter (MLI) with fewer elements and total standing voltage (TSV). The stress distribution among the switches is thoroughly investigated, and variable-rated switches are used to reduce the total cost of the inverter. The proposed structure produces 33 voltage output levels by combining twelve switches and four asymmetrical DC sources. Several critical parameters calculate the inverter's performance, including TSV, power loss, cost function (CF), and efficiency. The MLI was verified during various load circumstances with unpredicted load variables using combinational loads, and it proved stable over the entire condition. The suggested topology was established in MATLAB and verified in a research laboratory through a hardware setup.

7.1. INTRODUCTION

Multilevel inverters are popular in both academia and industry. Multilevel strategies improve the inverter's output power quality while enabling higher voltage levels in electronic circuits. [1]. Low-medium-rated semiconductor switches are available on the market and can be used to increase power levels. To create a high-rated converter with standard two-level operation, switches must be connected sequentially. Because of their advantages, multilevel inverters are used in a wide range of applications, such as UPS systems [2], hybrid PV-UPS systems [3], traction [4], ships [5], renewable systems [6], electric vehicles [7], and power quality. Despite their differences, multilevel converters often require many switches, incur higher losses and costs, and employ significant modulation techniques. Several research studies are being conducted to address these issues. MLIs are classified into three types: neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) [9]. Over the last two decades, the advantages and disadvantages of the three types of MLIs mentioned above have been thoroughly investigated. In summary, the significant disadvantages of these MLIs include changing the voltage in the NPC,

the control complexity required to balance voltages in the FC, and the increased number of switches and independent excitations in the CHB. Due to their modular architecture, cascaded MLIs may have higher voltage levels and dependability than other MLI topologies. [10]. Asymmetric MLI topologies have varying DC-link voltages, whereas symmetric cascaded inverters have equal DC sources. Asymmetric topologies may provide more diverse output voltage values than symmetric topologies. These are impossible to implement practically, and it isn't easy to balance the supplied power across every circuit source with the load when there are two or more excitations of the same magnitude [11]. Many techniques for adjusting the size of input sources are described [12] to achieve higher output levels in an asymmetric design.

In recent years, scholars have proposed numerous new architectures. Several of them are thoroughly examined. An H-bridge was proposed as part of a cascading basic components framework [13]. Because of the high conduction losses, this arrangement allows for more switches. [14] and [15] identify a second-order relationship between the circuit's peak inverse voltages (PIV) and level count. As a result, the inverter is expensive and unsuitable for applications that require high voltage. Each basic unit has a distinct design that includes many bidirectional switches. [16], the cost of this architecture rises as the number of DC sources grows. [17] Describes various methods for estimating the excitation values. The number of IGBTs in this arrangement is small, but the cost is high due to the variety of DC sources. [18] Introduces a novel structure in which each unit consists of two excitations. This architecture's basic units use bidirectional switches, making the topology less robust and increasing power losses. [19] A novel framework, including two algorithms for selecting DC sources, was introduced. However, the symmetric operation involves a large number of switches. An alternative topology is illustrated in [20]. Although this architecture reduces the number of components used, the symmetrical mode still has many switches.

The cascaded structure is addressed in [21] and [22] to reduce the standing voltage. As illustrated in [23], the architecture employs additive and subtractive techniques to produce nine levels of output from two unequal DC excitations. [23] Provides a series-connected linear direct current source value development. In contrast, this architecture necessitates higher switch voltage ratings and increased stress across the inverter's switches. In [24], the authors proposed a novel architecture utilizing four DC excitations and ten power electronic switches in each unit to provide

thirteen levels of voltage output to boost output voltage levels while reducing switch count; [25] proposes a new MLI with a redesigned H-bridge and numerous dc-sources.

Although these topologies require fewer gate driver circuits, bidirectional power electronic switches tend to increase switch count and inverter size gradually. Another option is to use modular topologies with an integrated polarity switcher to reduce the inverter's standing voltage. [26] and [27] are two examples. The ST-type architecture uses 12 power electronic switches to provide seventeen output voltage levels, with input excitation magnitudes selectable using the trinary progression technique. Despite having fewer sources than output levels, these topologies have more switches [26]. Each module in [27] provides nine and 17-level voltage outputs in symmetric and asymmetric configurations, ten power switches, and four input sources. Another system proposed by [28] uses ten switches to create seventeen tiers. Despite using asymmetric DC sources in this system, the maximum stress across the power electronic switches remains significant [29]. [12] Describes a single-source MLI that uses a variety of configurations, including equal and unequal sources and series and parallel voltage balancing methods in capacitors, to double the magnitude of the input voltage. The inverter TSV is low because there is no additional H-bridge circuit. The inverter [13] can generate 13 levels at its output using two unequal sources and dual capacitors. Because of the connection type, cascading with the other modules provides higher levels at the output without using an additional H-bridge, reducing stress across the switches in this configuration. MLI [15] discusses using T-type architecture and cross-sectional-connected units to generate output. Stress across the switches is high due to the additional power switches used in this configuration to facilitate the capacitor's charging and discharging behavior.

This study proposes and implements an asymmetric 33-level MLI architecture to reduce THD and voltage stress on switches. The impact of voltage stress on topology is extensively covered, along with power loss estimates. Power loss, efficiency, total harmonic distortion (THD), circuit complexity, voltage levels, number of DC sources, voltage stress on switches, and voltage levels are all factors that determine MLI performance. In a controlled laboratory setting, the designed MLI is tested under various loading conditions, including static, dynamic, combined, and inductive loads and resistive and inductive loads, using simulations run in the MATLAB/Simulink environment. The designed MLI finds application in grid-integrated renewable energy systems and drives, provided that a distinct DC source excitation is accessible.

7.2. ANALYSIS OF PROPOSED 33-LEVEL INVERTER STRUCTURE

This section implements a fundamental unit and a generalized extended structure for the proposed 33-level MLI architectures. The respective MLI parameters are developed using the design equations, and the switching states, load current paths, maximum blocking voltage (MBV), and total standing voltage (TSV) tabulations are represented by a reference output voltage waveform. Several MLI parameters are calculated to estimate the MLI's performance.

7.2.1. Basic unit of the proposed 33-level MLI

Figure 7.1 depicts the fundamental unit of the developed 33-level MLI topology. It consists of twelve unidirectional semiconductor switches and four input DC voltage sources. The switch is a high-power IGBT/MOSFET, which includes an anti-parallel diode and gate-driver circuitry. Current can flow in both directions, whereas voltage can only be blocked in one direction using anti-parallel diodes. The magnitudes of the input DC sources V1, V2, V3, and V4 are chosen in the ratio of 1:2:4:9. With a Vdc value of 25V, the basic unit of the proposed architecture can generate thirty-three levels of voltage at the output:

$$V_1= 1V_{dc},\ V_2= 2V_{dc},\ V_3= 4V_{dc},\ V_4= 9V_{dc} \tag{7.1}$$

The basic unit generates 33 voltage levels, including 0V, $\pm1V_{dc}$, $\pm2V_{dc}$, $\pm3V_{dc}$, $\pm4V_{dc}$, $\pm5V_{dc}$, $\pm6V_{dc}$, $\pm7V_{dc}$, $\pm8V_{dc}$, $\pm9V_{dc}$, $\pm10V_{dc}$, $\pm11V_{dc}$, $\pm12V_{dc}$, $\pm13V_{dc}$, $\pm14V_{dc}$, $\pm15V_{dc}$ and $\pm16V_{dc}$ at its output with a step size of V_{dc} with the DC voltage sources of V_1= 25V, V_2= 50V, V_3= 100V, V_4= 225V. The switching states for the proposed 33-level MLI during both levels of operation (positive and negative) are represented in Table 7.1. The current paths to the load, along with the voltage stress on the switches and maximum blocking voltage (MBV), are provided in Table 7.1. The various operating modes of the MLI during the positive cycle are represented in Figure 7.2. The highlighted lines indicate the current flowing through the active elements during each level of operation.

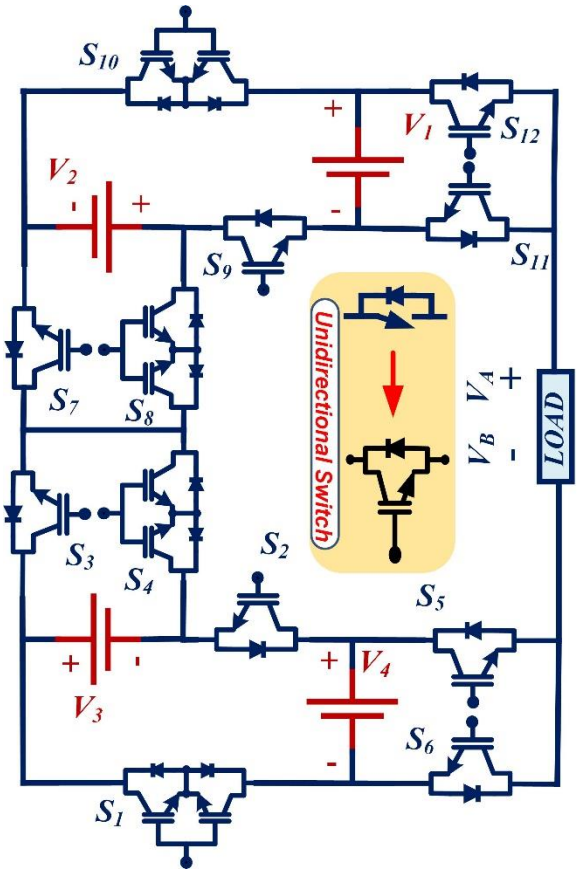

Figure 7.1 Proposed 33-level MLI topology

It was found that redundant switches exist for some levels of operating voltages. The developed 33-level topology is designed based on the parameters. Therefore, for one basic unit of MLI, n=1, the switches count N_{SW} is 12, the input DC sources count N_{dc} is 4, and the total number of the level N_L is 33 with a load voltage of V_0=400V. The maximum output voltage levels for the implemented 33-level inverter configuration are $\pm 16V_{dc}$, which can be accessed from $\pm\left(\frac{N_L-1}{2}\right)$.

Table 7.1 Switching sequence for the developed 33-level MLI structure

Switching states												Output voltage V0	Active Sources
S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12		
	1	1			1	1		1			1	**16*Vdc***	**V4+V3+V2+V1**
	1	1			1	1		1		1		**15Vdc**	**V4+V3+V2**

	1	1			1		1	1			1	**14Vdc**	**V4+V3+V1**
	1	1			1		1	1		1		**13Vdc**	**V4+V3**
	1	1			1	1			1	1		**12Vdc**	**V4+V3-V1**
	1		1		1	1		1			1	**11Vdc**	**V4+V2+V1**
	1		1		1	1		1		1		**10Vdc**	**V4+V2**
	1		1		1		1	1			1	**9Vdc**	**V4+V1**
	1		1		1		1	1		1		**8Vdc**	**V4**
	1	1		1		1		1		1		**7Vdc**	**V3+V2**
	1	1		1			1	1			1	**6Vdc**	**V3+V1**
	1	1		1			1	1		1		**5Vdc**	**V3**
	1	1		1		1			1	1		**4Vdc**	**V3-V1**
	1		1	1		1		1			1	**3Vdc**	**V2+V1**
	1		1	1		1		1		1		**2Vdc**	**V2**
	1		1	1			1	1			1	**Vdc**	**V1**
	1		1	1			1	1		1		**0**	
1		1			1	1			1	1		**-Vdc**	**-V1**
	1		1	1			1		1		1	**-2Vdc**	**-V2**
	1	1		1			1		1	1		**-3Vdc**	**-V2-V1**
1			1		1		1	1			1	**-4Vdc**	**-V3+V1**
1			1		1		1	1		1		**-5Vdc**	**-V3**
1			1		1	1			1	1		**-6Vdc**	**-V3-V1**
1			1		1		1		1		1	**-7Vdc**	**-V3-V2**
1		1		1		1			1		1	**-8Vdc**	**-V4**
1		1		1		1			1	1		**-9Vdc**	**-(V4+V1)**
1		1		1			1		1		1	**-10Vdc**	**-(V4+V2)**
1		1		1			1		1	1		**-11Vdc**	**-(V4+V2+V1)**
1			1	1			1	1			1	**-12Vdc**	**-V4-V3+V1**
1			1	1			1	1		1		**-13Vdc**	**-(V4+V3)**

1			1	1		1			1	1		**-14Vdc**	**-(V4+V3+V1)**
1			1	1			1		1		1	**-15Vdc**	**-(V4+V3+V2)**
1			1	1			1		1	1		**-16Vdc**	**-(V4+V3+V2+V1)**

The switching states & resulting output voltages are crucial aspects of the proposed system design. Table 7.1 comprehensively maps the switching configurations and the associated output voltages. The system comprises twelve switches, S_1 through S_{12}, and 4 voltage sources, labeled V_1, V_2, V_3, and V_4. The table is organized in rows, each representing a distinct switching state and columns representing the switch positions, output voltage (V0), and the active sources contributing to the output voltage. The switch positions are indicated by a binary state, with '1' representing a closed switch and an empty cell representing an open switch. The output voltage column (V0) displays the resulting voltage for the corresponding switching state, ranging from $-16Vdc$ to $16Vdc$ in increments of $1Vdc$. This range of output voltages allows for versatile applications and precise control over the system's output. The active sources column identifies the voltage sources contributing to the output voltage for each switching state. For instance, when switches S_2, S_3, S_6, S_7, S_8, and S_{12} are closed, the output voltage is 16Vdc, and the active sources are V_4, V_3, V_2, and V_1, indicating that all four voltage sources are collectively contributing to the output. Table 7.1 is vital for understanding the system's behavior under different switching conditions. It enables the analysis and prediction of the output voltage based on the switching state, facilitating the development of control algorithms and strategies for optimal system performance.

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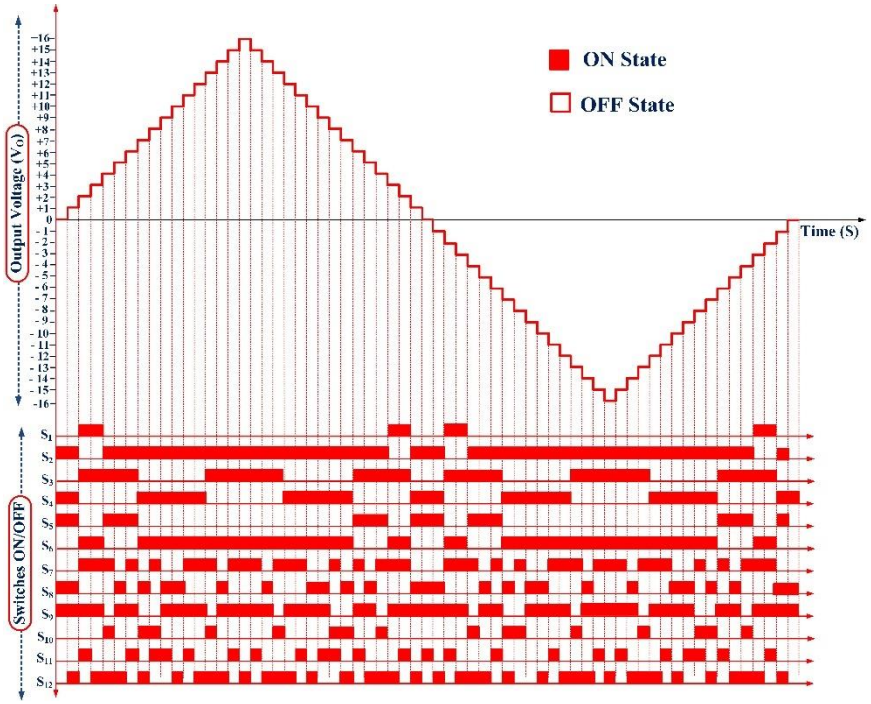


Figure 7.2 staircase typical output of 33-level

7.2.2. Extended MLI structure

Figure 7.3 depicts the generalized MLI architecture that is encompassed to accomplish higher output levels. Cascaded structures efficiently use DC sources in asymmetrical operation to generate higher voltages at the output. Table 7.2 shows the equivalences of MLI design.

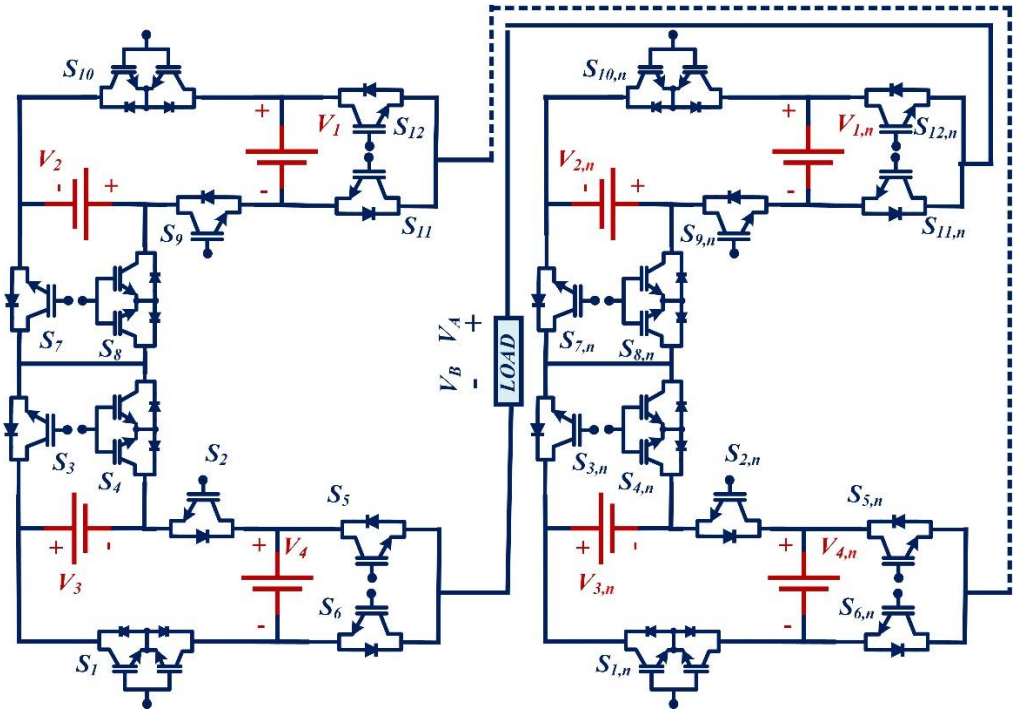


Figure 7.3 Comprehensive design of suggested MLI

The N_sAre required for comprehensive design is as follows:

$$N_s = 12n \tag{7.2}$$

For an extended topology, *Ndc* are evaluated as:

$$N_{dc} = 4n \tag{7.3}$$

The extended topology determines the NL, as is:

$$N_L = 2(17n) - 1. \tag{7.4}$$

An extended topology's voltage at the load terminals is considered as follows:

$$V_0 = 16n \times V_{dc} \tag{7.5}$$

Equation (7.6) is used to find the maximum output voltage that has been developed as follows,

$$V_{0,max} = \pm\left(\frac{N_L - 1}{2}\right) \tag{7.6}$$

As a whole, DC sources,

$$V_{1,n} = V_1 = V_{dc},\ V_{2,n} = V_2 = 2V_{dc},\ V_{3,n} = V_3 = 4V_{dc},\ V_{4,n} = V_4 = 9V_{dc}, \tag{7.7}$$

It is possible to calculate the extended MLI's TSV by:

$$\sum_{i=1}^{n} MBV_{S,n} = \sum_{i=1}^{n} V_{S,n} \quad (7.8)$$

To calculate the TSV, we add up all the maximum blocking voltages.

$$TSV = MBVs_{1,n} + MBVs_{2,n} + \ldots\ldots\ldots + MBVs_{n} \quad (7.9)$$

As a result, the TSV is determined as:

$$TSV = 2\sum_{i=1}^{n} MBV_{S,2n+1} \quad (7.10)$$

Table 7.2 Equivalences of MLI design

S.no	Constraints	Basic units	Chosen voltage levels
1	Switches	12n	$6\left(\frac{N_L-1}{16}\right)$
2	Voltage levels	32n+1	N_L
3	TSV	64n	$2(N_L-1)$
4	Gate driver circuits	12k	$6\left(\frac{N_L-1}{16}\right)$
5	TSV_{PU}	4n	$2\left(\frac{N_L-1}{16}\right)$

7.3. PERFORMANCE EVALUATION

Considerations such as THD, power losses, cost function (CF), efficiency, and circuit parameters can be used to assess the analysis. Reduced total system voltage (TSV) across the switches allows more efficient use of the inverter's power supply by reducing losses and enabling a lower-rated switch. The performance parameters are calculated using the following parameters:

7.3.1. TSV Calculation

A critical factor in the MLI's efficiency and cost-effectiveness is TSV. Reducing stress across the semiconductor switches allows for a more cost-effective inverter design [26]. When turned off, a power device's standing voltage is the highest voltage stress it can withstand. TSV is equivalent to maximum blocking voltages across all switches added together. The TSV can be assessed using the modes of operation depicted in Figure 7.4. The blocking voltage of S_1 at V0=±16*Vdc*, ±15*Vdc*, ±14*Vdc*, or ±13*Vdc* is used to determine the maximum voltage-blocking

capacity of S1. Every one of these voltage levels disables S1. This causes a blocking voltage to be applied to S_1 by V_3 and V_4. Being complementary, S_1 and S_2 put equal voltage stress on both switches. To illustrate the MBV across all power switches, consider the following:

$MBVs_1 = MBVs_2 = V_{S1} = V_{S2} = V_3 + V_4 = 4V_{dc} + 9V_{dc} = 13V_{dc}$

$MBVs_3 = MBVs_4 = V_{S3} = V_{S4} = V_3 = 4V_{dc}$

$MBVs_5 = MBVs_6 = V_{S5} = V_{S6} = V_4 = 9V_{dc}$

$MBVs_7 = MBVs_8 = V_{S7} = V_{S8} = V_2 = 2V_{dc}$

$MBVs_9 = MBVs_{10} = V_{S9} = V_{S10} = V_1 + V_2 = 1V_{dc} + 2V_{dc} = 3V_{dc}$

$MBVs_{11} = MBVs_{12} = V_{S11} = V_{S12} = V_1 = 1V_{dc}$

Figure 7.5 depicts the mean value across all switches. The TSV is calculated by adding the maximum blocking voltages across all switches. Therefore, it can be determined using the given formula (7.11).

$$TSV = MBVs1 + MBVs2 + \ldots\ldots\ldots + MBVsn \quad (7.11)$$

$$TSV = 2(VS1 + VS3 + VS5 + VS7 + VS9 + VS11$$
$$= 2(13Vdc + 4Vdc + 9Vdc + 2Vdc + 3Vdc + 1Vdc) = 64Vdc$$

To calculate the TSV per unit (TSVpu), the following equation (7.12) is as follows,

$$TSV_{PU} = \frac{V_{TSV}}{V_{OMAX}} \quad (7.12)$$

Where $TSV_{PU} = 4$

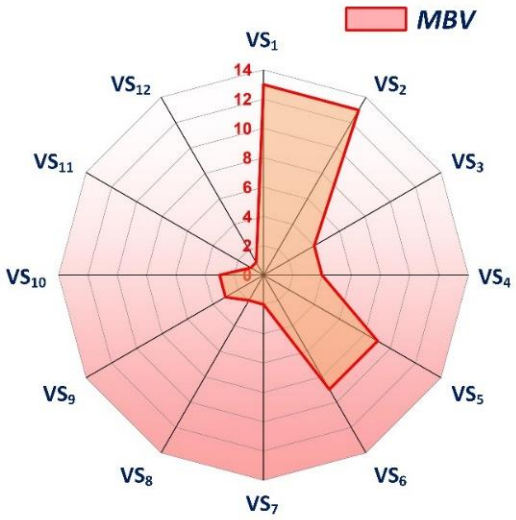


Figure 7.4 Maximum voltage stress across switches

Figure 7.5 depicts the stress distribution effect, computed using the power switches' TSV and MBV values, a normalized voltage stress metric. This shows how evenly distributed the stress is among the switches. This value is determined by dividing the voltage stress across a single switch by the maximum stress in the circuit, as shown in equation (7.13) [27].

$$\text{Normalized voltage stress (NVS)} = \frac{Actual\ voltage\ stress\ across\ switch}{Maximum\ voltage\ stress\ in\ the\ circuit} \tag{7.13}$$

Table 7.3 Saturation voltage for power switches normalized

Switches	**MBV**	**NVS**	**Impact of NVS**
S_1, S_2	$13V_{dc}$	$13V_{dc}/13V_{dc}$	100%
S_3, S_4	$4V_{dc}$	$4V_{dc}$ /$13V_{dc}$	29.76%
S_5, S_6	$9V_{dc}$	$9V_{dc}$ /$13V_{dc}$	65.23%
S_7, S_8	$2V_{dc}$	$2V_{dc}$ /$13V_{dc}$	11.38%
S_9, S_{10}	$3V_{dc}$	$3V_{dc}$ /$13V_{dc}$	21.07%
S_{11}, S_{12}	$1V_{dc}$	$1V_{dc}$ /$13V_{dc}$	5.67%

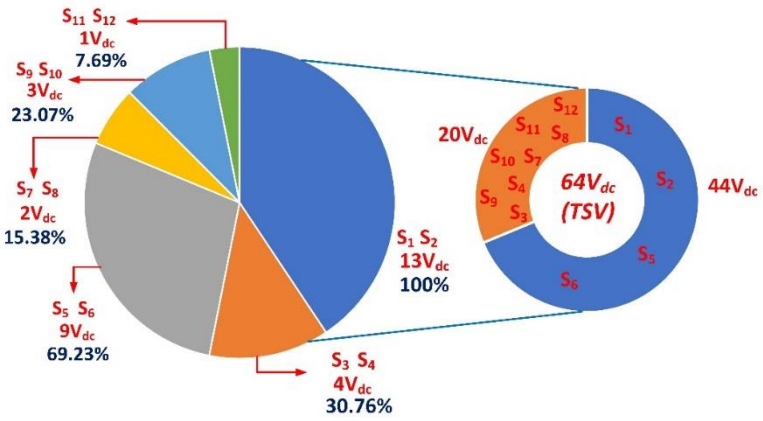


Figure 7.5 Influence of voltage stress distribution

Table 7.3 shows the voltage stress across all 33 MLI levels and the maximum stress for each power switch. The lowest stress and NVS, namely *Vdc* and 7.69 percent, are applied exclusively to switches S_{11} and S_{12}. Double the lowest stress and NVS, at 2Vdc and 15.38%, are found in power switches S_7 and S_8. With a maximum stress voltage of 13Vdc and an NVS of 100 %, power switches S1 and S2 are inoperable. The S9 and Sl0 power switches exceed the minimum NVS with stresses of 3Vdc and NVS values of 23.17%. The NVS is 30.76 %, lower than half of the maximum NVS, and the stress between switches S3 and S4 is 4*Vdc*. Power switches S_5 and S_6 are under a voltage stress of 9Vdc, and the NVS is 60.23% below the maximum NVS. Table 7.4 displays the circuit's overall stress distribution.

Table 7.4 Stress Distribution of power switches

Stress distribution	**Switches (N_{St})**	**Switches under stress % (N_{St}/N_S)**	**MBV (V_{dc})**	**MBV % (MBV/TSV)**
Maximum Stress	S_1, S_2	15 %	25	40 %
Intermediate Stress	S_3, S_4, S_5, S_6	35 %	25	40 %
Minimum Stress	S_7, S_8, S_9, S_{10}, S_{11}, S_{12}	50 %	12	20 %

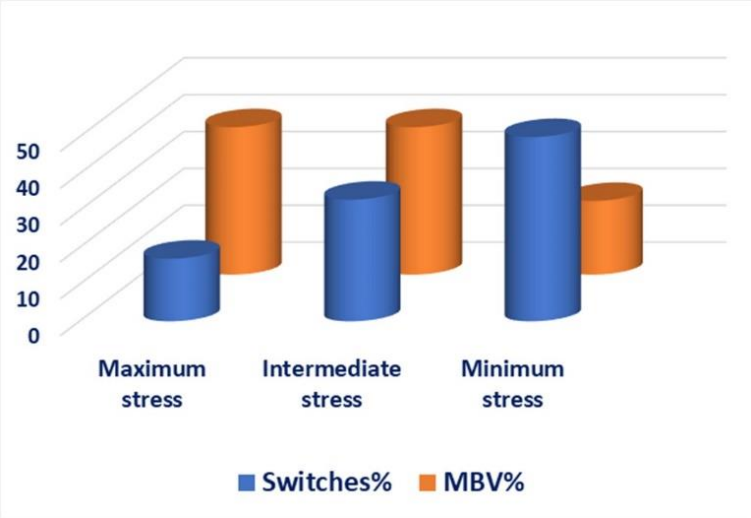


Figure 7.6 Stress distribution over the switches

Under the 33-level MLI structure, four switches (S_1, S2, S5, and S6) undergo a stress of 44*Vdc*, accounting for 68% of total stress; the other eight switches undergo a stress of 20Vdc, representing 32% of the total stress. Consequently, the 33-level MLI allows the power switches to share the load effectively. Consequently, the design minimizes the TSV value and MLI cost while efficiently using a maximum number of DC sources and switches. Figure 7.6 displays the stress distribution graphically. Eight switches are determined to have lower stress; these switches are then rated with a low voltage, resulting in low cost. Due to the selection of high-rated switches and the subsequent stress they undergo, the remaining four switches incur a price increase. Consequently, the inverter's size, complexity, and total cost are reduced due to the circuit's operation of variable-rated switches.

7.3.2. Cost Function

Finding the optimal MLI for a given application relies heavily on the cost function (CF). So, the following equation (7.14) [28] is used to find the cost factor.

$$CF = (N_S + +N_{gd} + N_D + N_C + \alpha TSV_{PU}) \times N_{DC} \quad (7.14)$$

No matter what, the weight coefficient α will never be less than one and greater than one. A count of components at the level is here:

For α=0.5, CF/level = (26×4)/33 = 3.15

For α=1.5, CF/level = (30×4)/33 = 3.63

The suggested MLI is economically viable because its cost is lower than that of other contemporary topologies.

7.3.3. Calculation of Power Loss

It is possible to evaluate these for the established topology using the method given in [17]. As a result of voltage drop, semiconductor devices incur conduction losses when conducting while in the on state. When a semiconductor device is in its state, its conduction losses can be determined by multiplying its voltage v_{on}(t) and current $i(t)$ values. The computed results are tabulated in Table 7.5. Figure 7.7 shows the efficiency variation as a function of load. Conduction and switching losses caused by switches combine to form the total losses. To compute the switches' conduction losses using equation (7.15).

$$P_{Cl} = \left[V_S + R_S i^{\beta}(t)\right] i(t) \tag{7.15}$$

The voltage drop of a diode is $V_{d,}$ and that of an IGBT switch is V_S. The switch resistance is denoted as R_S, while the equivalent diode resistance is R_d. We can use the following generalized relationship to estimate conduction power losses (PCl): at any given time, we can calculate the diodes N_d and the switches N_{IGBT} using equation (7.16).

$$P_{Cl} = \frac{1}{2\pi}\int_0^{2\pi}\left[N_{IGBT}(t)P_{cl,IGBT}(t)\,dt\right] \tag{7.16}$$

The switching losses are determined using equation (7.17).

$$P_{Sl} = f\sum_{K=1}^{N_{switch}}\left[\sum_{j=1}^{N_{on,k}} En_{on,kj} + \sum_{j=1}^{N_{off,k}} En_{off,kj}\right] \tag{7.17}$$

While the switches are isolated, they use energy (E_{off}), and when conducting, they use energy (E_{on}). To determine total power losses (P_{loss}), (7.18) can be used.

$$P_{loss} = P_{cl} + P_{sl} \tag{7.18}$$

To calculate the efficiency (η), the (7.19) is used.

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out}+P_{loss}} \tag{7.19}$$

Expressly, P_{out} signifies the output power; P_{in} signifies the input power. Power can be calculated using the following equation:

$$P_{out} = V_{rms} I_{rms} \tag{7.20}$$

Table 7.5 Calculations of Power loss and efficiency

Parameters	R-Load (100Ω)	R-Load (150Ω)	L-Load (187mH)
I_{rms} (A)	2.82	1.88	4.8
V_{rms} (V)	282.84	282.84	282.84
Switches turn-on loss E_{on} (W)	0.21	0.14	0.37
Conduction losses P_{cl} (W)	58.47	30.5	145.15
Switching losses P_{sl} (W)	0.52	0.35	0.89
Switches turn off loss E_{off} (W)	0.31	0.21	0.52
Output power P_{out} (W)	797.6	531.7	1357.63
Total losses P_{loss} (W)	58.9	30.85	146.04
Efficiency η (%)	94.1	95.2	90.3
Input power P_{in} (W)	856.5	562.55	1503.67

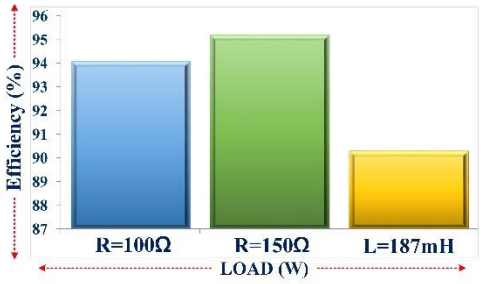


Figure 7.7 Efficiency of MLI with different loads

7.4. RESULT ANALYSIS AND DISCUSSION

We compare the proposed MLI to other structures using various essential parameters to ensure its validity. These parameters include the NS, Ngd, Ndc, ND, NC, TSV, CC/L, CF/L, and NL/NS. The pertinent comparisons are summarised in Table 7.6, and equivalent representations

are revealed in Figure 10. Compared to other topologies, the recommended 33-level MLI is cost-effective and efficient across all parameters. The in-depth comparisons are as follows. The number of DC sources significantly affects the topology's applicability to real-world scenarios—the circuit's cost and voltage stress rise as the DC source voltage rises. Although configurations [31–33] only require one input, the increased use of capacitors and diodes results in a relatively high component count (as shown in Table 7.7). Since the suggested design uses fewer overall components and DC sources, it is a good option for better power quality. The number of levels to switches (NL/NS) proportion is displayed in Figure 7.8 and compared to all other topologies in Table 7.7 [27]. This ratio defines the total cost and efficiency of the topology. A lower NL/NS ratio allows for fewer switches, which increases the potential for producing higher voltage levels. Consequently, it is possible to get higher output levels with fewer switches. With a rating of 2.75, the suggested configuration overcomes other configurations. The designed topology is ideal for renewable energy systems in light of the preceding. By approximating the IGBT switches rating concerning stress across the switches, TSVpu is pivotal in determining the overall cost of the inverter. The rating switches used, which are more expensive, are directly proportional to the load on the switches. The result is an increase in the total cost of the circuit. With a TSV of 64Vdc and a TSVpu of 4, the suggested topology reduces stress across the switches compared to other configurations. The comparison between *TSVpu* and *NL*/*NS* ratios is illustrated graphically in Figure 7.9. We can deduce that the suggested topology offers excellent performance from the stress across switches at a low cost.

Table 7.6 Comparative assessment of various levels.

Methods	N_L	N_S	N_L/N_S	N_{gd}	N_D	N_C	N_{dc}	**CC/L**	***THD* %**	TSV_{PU}	**C.F**	
											α=0.5	**α=1.5**
[26]	33	18	1.83	18	-	-	8	1.33	-	5	9.33	10.54
[32]	33	21	1.57	21	32	16	1	2.75	-	-	-	-
[33]	33	18	1.83	18	18	6	1	1.84	-	-	-	-
[34]	33	14	2.35	14	8	-	5	1.24	6.17	4.37	5.78	6.44
[35]	33	14	2.35	14	2	-	7	1.12	2.06	5.87	6.9	8.23
[36]	33	16	2.06	16	-	-	7	1.18	5.9	6	7.42	8.69
[37]	33	24	1.37	15	-	-	9	1.45	4.54	9.62	11.94	14.57

[38]	33	22	1.5	15	-	-	9	1.39	-	9.5	11.38	13.97
[39]	33	18	1.83	18	18	-	8	1.87	-	5	13.69	14.9
[40]	35	12	2.9	12	2	2	5	0.94	2.2	5.52	4.39	5.18
[41]	31	16	1.93	12	-	-	6	1.2	-	6.33	6.03	7.25
[42]	31	20	1.65	20	-	-	8	2.06	3.26	7	15.39	17.09
[43]	31	14	2.21	14	-	-	4	1.03	3.35	5.86	4.0	4.74
Proposed	33	12	2.8	12	-	-	4	0.84	2.03	4	3.15	3.63

The cost-effectiveness of the topology can be determined by varying the weight coefficient α, which is an essential component of the MLI cost function. The value of α can vary between 0.5 (<1) and 1.5 (>1). Cost functions of 3.15 for α = 0.5 and 3.63 for α = 1.5 in the 33-level MLI that was developed are lower than other topologies and are determined to be profitable.

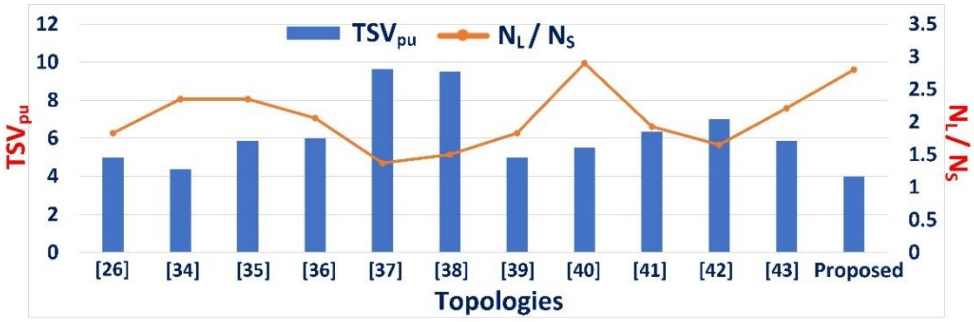
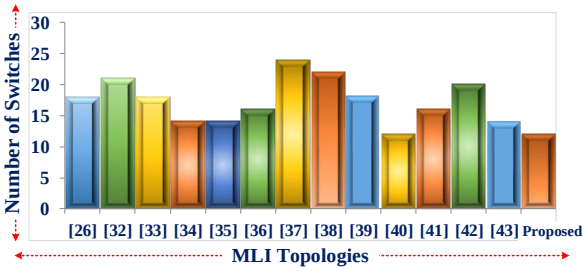
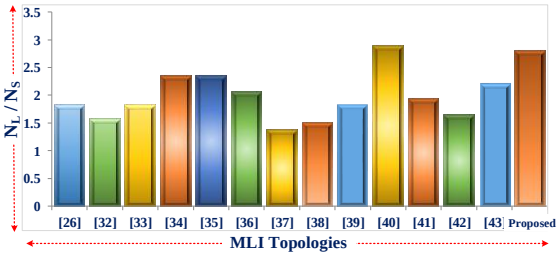


Figure 7.8 Evaluation of TSV_{pu} vs N_L/N_S



(a)



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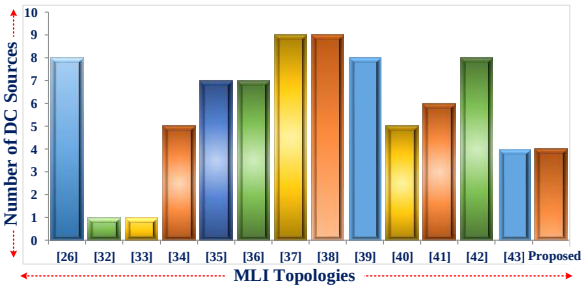
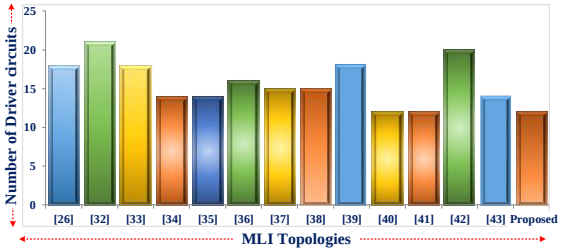


(c)



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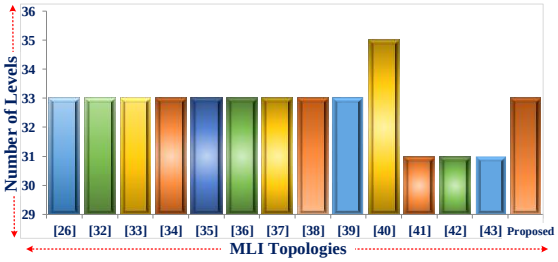

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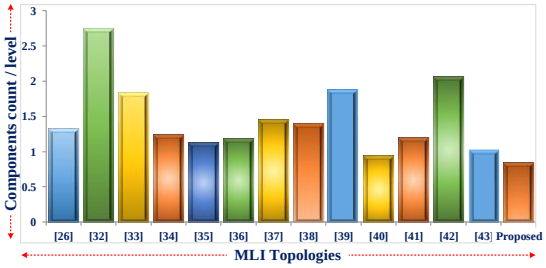
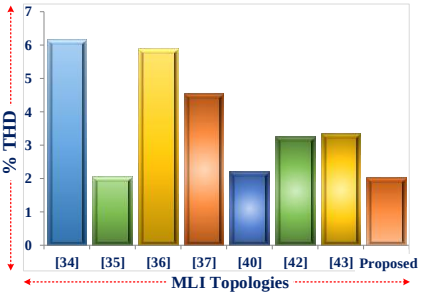
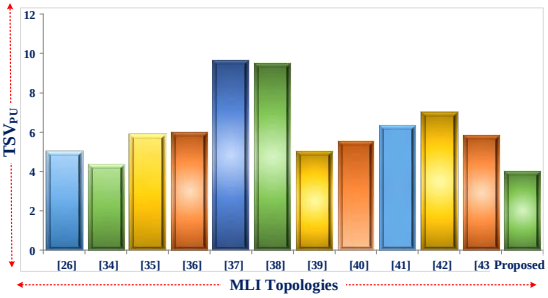


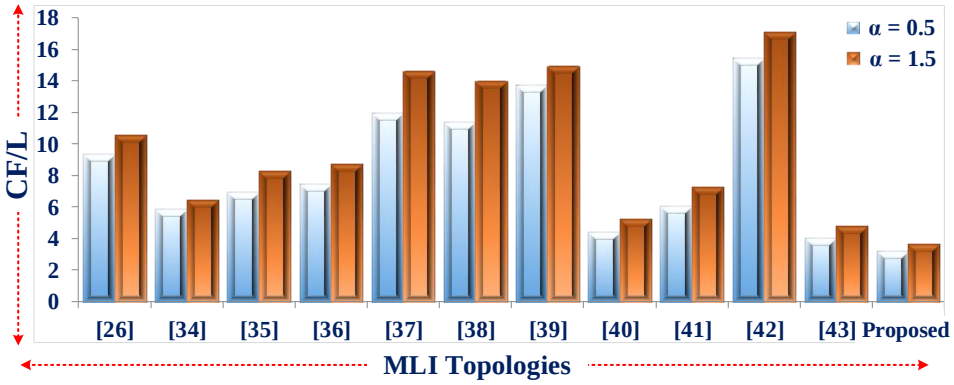
(f)



(g)



(h)



(i)

Figure 7.9 Evaluation of 33-level MLI (a) N_S, (b) N_L/N_S, (c) N_{dc}, (d) N_{gd}, (e) N_L, (f) CC/L, (g) THD% (h) TSV_{PU}, (i) CF/L

The parametric comparisons show that the proposed MLI performs better than the existing topologies. The suggested inverter design reduces switch count, TSV, and driver circuitry significantly. Because of these significant advantages, the MLI topology may be more cost-effective in the long run due to a smaller installation area and lower total cost.

V1=25V, V2=50V, V3=100V, and V4=225V are the input DC sources used in the designed MLI configuration. The 33-level MLI that was developed also has its levels represented. The simulation THD of 2.03% is lower than the standards set by IEEE. The MLI's simulation constraints and corresponding parameters are in Table 7.8. Due to its many advantages, including reduced switching losses and less complexity, this method is preferred over conventional pulse width modulation (PWM).

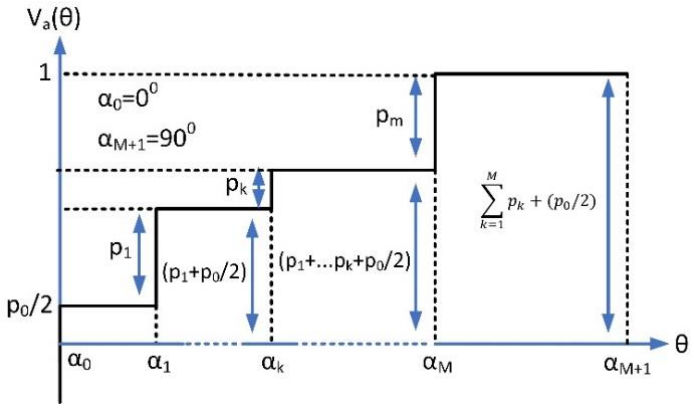


Figure 7.10 Representation of Quarter-wave staircase

Figure 7.10 shows the generalized quarter-wave representation. The relationship between N and the phase switching angles per quarter-wave M, excluding $\alpha 0$, is assumed by $M=(N-1)/2$ [30]. Figures 7.11 and 7.12 show the output voltage current waveform obtained from the simulations conducted in MATLAB/Simulink. Figure 7.13 shows the THD for 33-level.

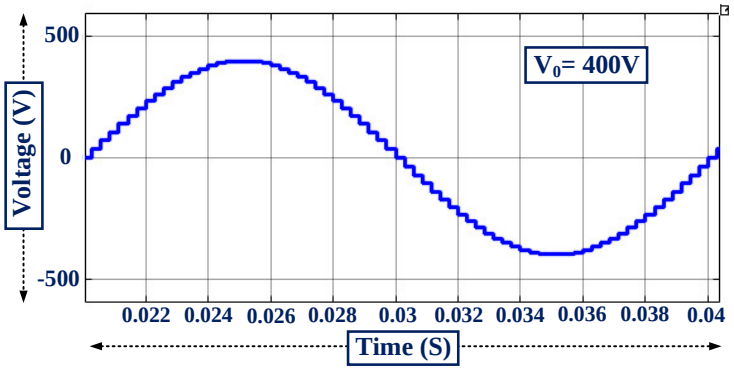


Figure 7.11 Results of Output voltage

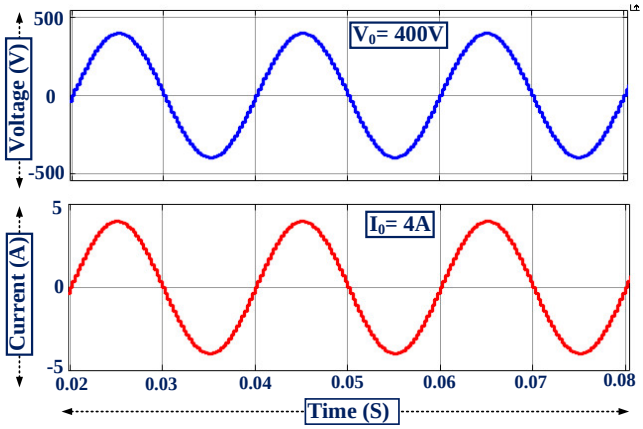


Figure 7.12 Representation of Output voltage and current

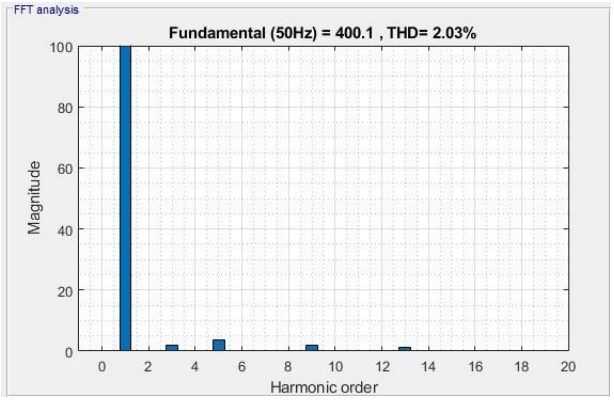


Figure 7.13 THD for 33-level MLI

Table 7.7 Simulation parameters

Parameter	***Ratings***
IGBT	CM75DU-12H
Switching frequency	5 kHz
Voltage Sources	V_1= 25V, V_2= 50V, and V_3= 100V, V_4= 225V
Fundamental frequency	50Hz
Load Resistance	100Ω, 150Ω

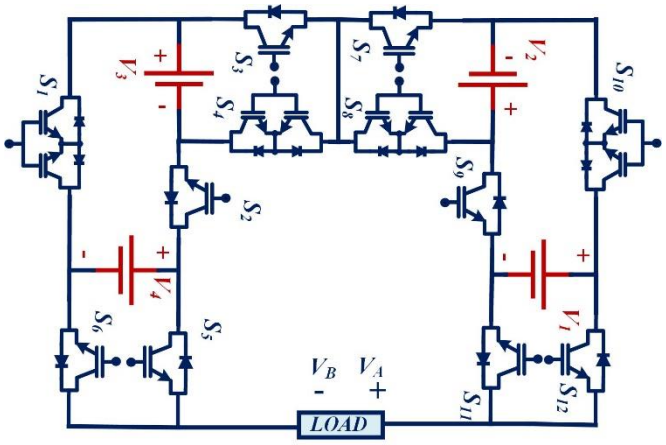


Figure 7.14 The circuit design of 33-level MLI

Figure 7.14 shows the circuit design of 33-level MLI. This representation includes a quarter-wave, with the option for an additional half-step at the origin. The normalized width and height concerning the DC supply voltage ratio of pk are present for each k^{th} step that appears at αk. An additional half-step with p0/2, which appears at the 0th phase angle, $\beta 0 = 0$, is needed to produce even values of **N**. The relationship between N and M, excluding $\alpha 0$, is specified by M=(N-1)/2 [30]. Figure 7.15 shows the Output voltage of 33-level MLI. Figures 7.16 and 7.17 show the voltage and current for R and L load.

The developed MLI is put through its paces in various dynamically loaded scenarios, including R-L and L-R loads. Figure 7.18 shows the waveforms for the case where the load is R||L

when an inductive load is suddenly added and connected to the existing resistive load during operation. Figure 7.19 shows the corresponding representations of the waveforms for the case when the load L||R, during the operation of the R-L load, the inductive load is disconnected at a particular instant, and the resistive load operates alone after a specific duration. Figure 7.20 displays the experimental test-hit ratio (*THR*). The suggested MLI remains stable in the face of unexpected changes in load. Figure 7.21 depicts the experimental setup, while Figure 7.22 highlights the MLI's outstanding features.

Table 7.8 Experimental specifications

Item	**Range**
IGBT	600V, 75A
DC source	0-500V
R-Load	100Ω & 150Ω
Controller	dSPACE RTI 1104
GATE Driver	TLP-250
Motor Load	Single-phase, 230V, 0.5 HP
L-Load	187 mH

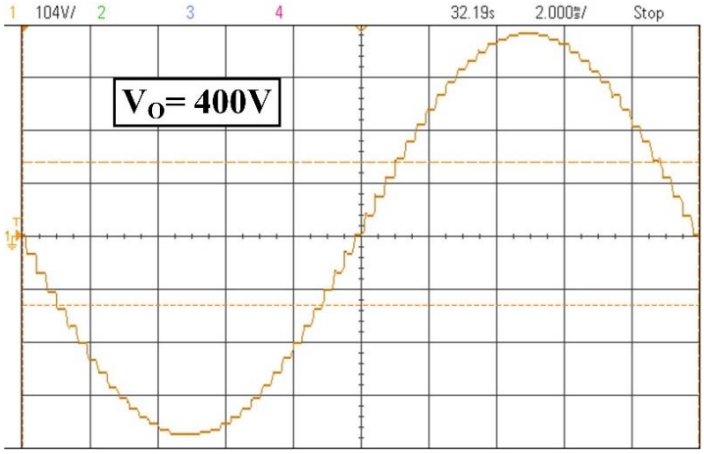


Figure 7.15 Output voltage of 33-level MLI

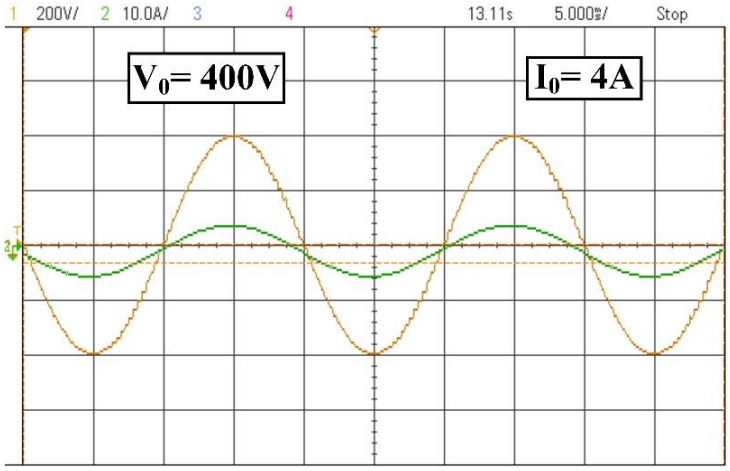


Figure 7.16 Voltage and current for R-Load

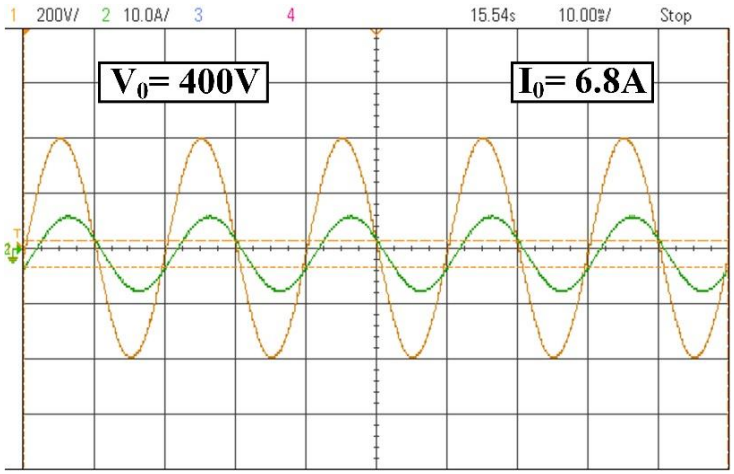


Figure 7.17 Voltage and current for L-Load

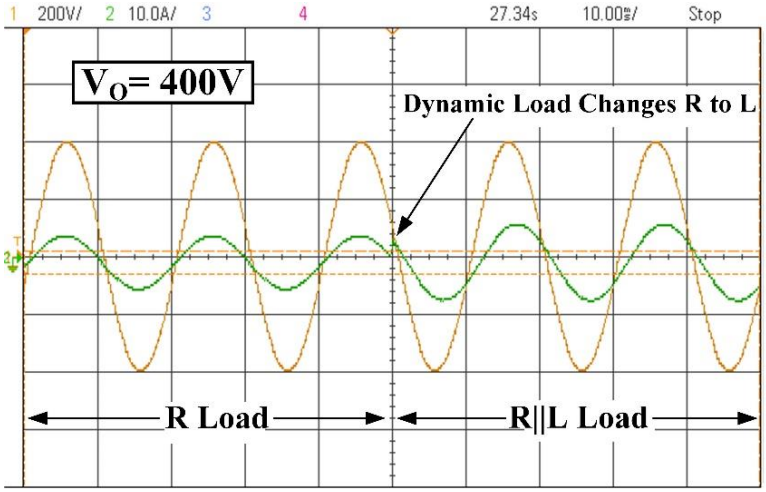


Figure 7.18 Voltage and current for R||L-Load

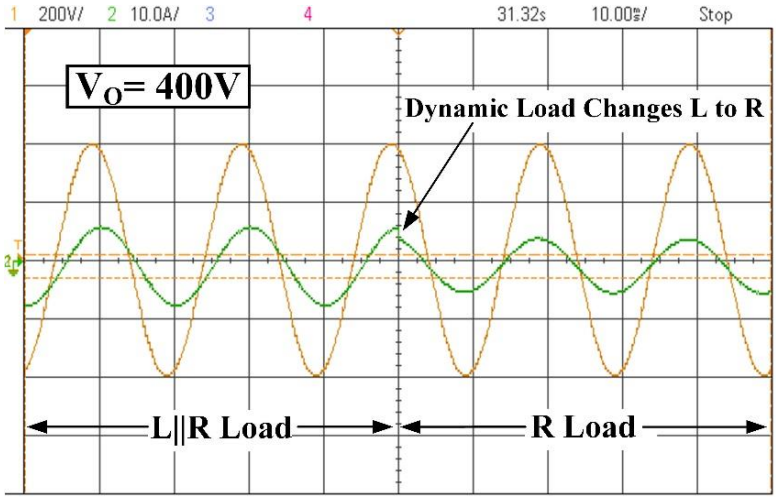


Figure 7.19 Voltage and current for L||R-Load

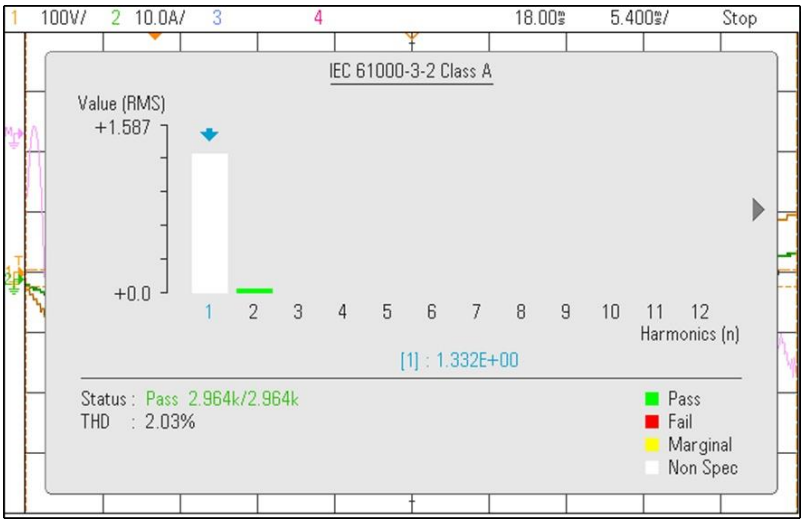


Figure 7.20 THD performance during experimental analysis

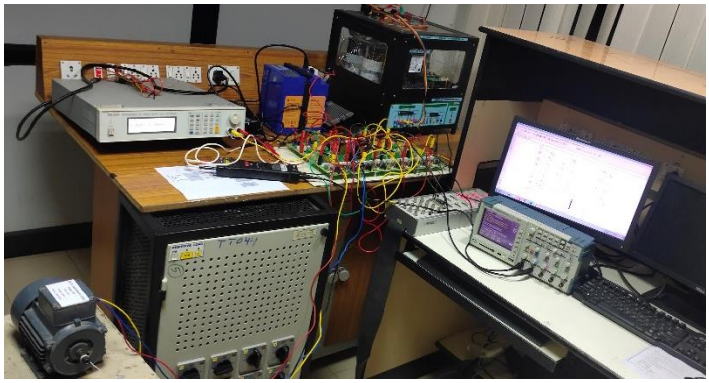


Figure 7.21 Experimental arrangement of 33-level MLI

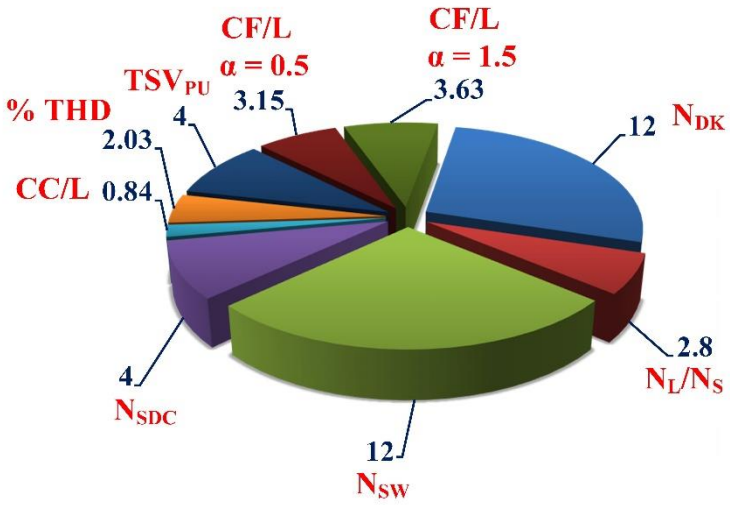


Figure 7.22 Characteristics of 33-level MLI

7.5. Summary

With fewer components and less TSV, the novel asymmetrical MLI produces 33 voltage levels. A thorough analysis is conducted to select the proper switches to reduce the inverter's size and cost. Increasing the output voltage is the goal of an extended circuit. The developed MLI is determined to perform better based on several metrics than other MLI architectures already in use. To achieve higher output, MLI exploits fewer DC sources and power switches. Only 17 % of the switches operate at total capacity; the MLI's TSVPU is 4; consequently, the inverter's price drops. According to the comparisons, the suggested MLI is efficient, cheap, and low TSV. Many hybrid and renewable energy storage applications can benefit from this topology, which employs low-rated switches and unequal DC sources. We test the MLI under dynamically loaded conditions to see how well it performs, and we find that it stays stable while running. With an efficiency of 95.2 %, the experimental and simulation THD obtained is 2.03 %. The cost function α is lower than other topologies, with values of 3.15 and 3.63, respectively.

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Chapter 8

Conclusion and Future Scope: Optimizing Multilevel Inverters for Efficiency and Cost-effectiveness

This thesis introduces a novel multilevel inverter topology that is entirely dependent on the connections between basic modules. PV systems can utilize the suggested circuit, which can function with both symmetrical and asymmetric inverters. Two DC sources in the basic module can have different magnitudes for symmetrical and asymmetrical structures. The DC source magnitude in the symmetrical multilevel inverter is the same for every module. However, in an asymmetrical design, the magnitude of the DC source for fundamental modules is unequal, and their magnitudes are obtained through binary and trinary progression. The results of the comparison demonstrate that the suggested circuit has fewer components, less power loss, and increases the inverter's efficiency. Furthermore, when compared to modern topologies, the overall standing voltage on switches is reasonable. Renewable energy systems with low to medium power levels can be equipped with the suggested inverter. The operation and performance of the suggested architecture are validated by analyzing simulation and experimental data for 15, 25, and 33-level inverters.

First, a new asymmetric 25-level MLI topology with fewer semiconductor switches is proposed, coupled with a 15-level topology. The goal of this design is to increase the inverter's efficiency and dependability while lowering its cost and size. The MLIs that are being shown have low total harmonic distortion (THD) and can produce the necessary output voltage levels with very little loss. Configurations with different MLI amounts were assessed to calculate the total standing voltage (TSV) and cost function. The findings show that the lower TSV value of the suggested MLI improves its speed, cost-effectiveness, and competitiveness. According to experimental comparisons, the structure produces energy with a low harmonic content that complies with IEEE requirements, making it ideal for grid-connected applications and DVR technologies. Additionally, the MLIs fared well while using renewable energy sources. Additionally, they are helpful for single-phase applications because several isolated DC sources are available. This

research has great promise for battery storage in stand-alone and alternative buildings, such as those in the hotel and residential sectors. The novel asymmetrical MLI topology can produce 33 voltage levels with fewer parts and fewer TSV. Low voltage-rated switches are chosen after a careful examination of the stress distribution across the switches is done in order to minimize the size and expense of the inverter. An extended circuit's aim is to raise the output voltage. Based on several criteria, the designed MLI is found to perform better when compared to other MLI architectures that are currently in use. The MLI uses fewer power switches and DC sources to reach larger output levels. Out of all the switches, only 17% are running at maximum capacity, and the TSVPU of the MLI is 4. As a result, the cost of the inverter decreases. The comparisons show that the proposed MLI has a low TSV, is inexpensive, and is efficient. This architecture, which uses uneven DC sources and low-rated switches, can be advantageous for a wide range of hybrid and renewable energy storage applications. We also undertake performance tests of the MLI under dynamically loaded settings and discover that it runs stable. The calculated THD from simulation and experimentation is 2.03%, with an efficiency of 95.2%. Compared to other current topologies, the cost function α is less, with values of 3.15 and 3.63, respectively.

8.1. Future Scope

Future research will concentrate on applying the proposed multilevel inverter (MLI) in real-world scenarios to validate the theoretical findings and performance improvements discussed in this study. This includes the practical implementation of the proposed DC/DC buck-boost inverter based on the fundamental isolated Single-Ended Primary-Inductor Converter (SEPIC) topology. The goal is to assess the operational efficiency, reliability, and overall performance of the MLI under actual conditions, thus bridging the gap between theoretical simulations and practical applications. Additionally, the research will be expanded to include a comprehensive analysis of different inverter levels. This will involve evaluating various design components and configurations to verify their effectiveness and efficiency across multiple inverter levels. Such an extension will ensure a thorough understanding of the performance characteristics and potential improvements in design, further enhancing the practical viability and robustness of MLIs in renewable energy systems.