TESI DOCTORAL

Títol: ***SCINTILLATOR PAD DETECTOR: VERY FRONT END ELECTRONICS***

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'Scintillator Pad Detector: Very Front End Electronics'

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A mi familia,

Por la ayuda que me han dado durante todos estos años y por la paciencia que han tenido en los momentos más difíciles.

A mis amigos,

Porque no hace falta decirles nada para que estén ahí, siempre que los necesito.

A mis compañeros,

Porque entre todos hemos diseñado una parte de un Detector Europeo del debemos estar orgullosos.

Abstract

High Energy Physics Laboratory in La Salle is a member of a Credited Research Group by La Generatitat. This group is formed by a part of the ECM department, a part of the Electronics department at UB (University of Barcelona) and La Salle's group. Together, they are involved in the design of a subdetector at LHCb Experiment at CERN: the SPD (Scintillator Pad Detector).

The SPD is a part of LHCb Calorimeter. That system provides high energy hadrons, electrons and photons candidates for the first level trigger.

The SPD is designed to identify charged tracks for this first level trigger. This detector is a plastic scintillator layer, divided in about 6000 cells of different size to obtain better granularity near the beam. Charged particles will produce, and photons will not, ionization on the scintillator. This ionization generates a light pulse that is collected by a Wavelength Shifting (WLS) fibber that is twisted inside the scintillator cell. The light is transmitted through a clear fibber to the readout system.

For cost reduction, these 6000 cells are divided in groups using a MAPMT of 64 channels for receiving information in the readout system. The signal outing the SPD PMTs is rather unpredictable as a result of the low number of photostatistics, 20-30 photoelectrons per MIP, and the due to the response of the WLS fibber, which has low decay time. Then, the signal processing must be performed by first integrating the total charge and later subtracting to avoid pile-up as a result of working at 40MHz clock.

This PhD is focused on the VFE (Very Front End) of SPD Readout System. It is performed by a specific ASIC (designed by the UB group) which integrates the signal, makes the pile-up compensation, and compares the level obtained to a programmable threshold (distinguishing electrons and photons), an FPGA which programs the ASIC thresholds, pile-up subtraction and mapping the channels in the detector and finally LVDS serializers, in order to send information to the first level trigger system.

Not only mechanical constraints had to be taken into account in the design of the card as a result of the little space for the readout electronics but also, on one hand, the radiation quote expected in the environment and on the other hand, the distance

between the VFE electronics and the racks were information is sent and the signal range that this kind of experiments usually have.

Resumen

El Laboratorio de Altas Energías de la Salle es un miembro de un grupo acreditado por La Generalitat. Este grupo está formado por parte del departamento de Estructura i Constituents de la Matèria de la Facultad de Física de la Universidad de Barcelona, parte del departamento de Electrónica de la misma Facultad y el grupo de La Salle. Todos ellos están involucrados en el diseño de un subdetector en el experimento de LHCb del CERN: El SPD (Scintillator Pad Detector).

El SPD es parte del Calorímetro de LHCb. Este sistema proporciona posibles hadrones de alta energía, electrones y fotones para el primer nivel de trigger.El SPD está diseñado para distinguir entre electrones y fotones para el trigger de primer nivel. Este detector está formado por una lámina centelleadora de plástico, dividida en 6000 celdas de diferente tamaño para obtener una mejor granularidad cerca del haz. Las partículas cargadas que atraviesen el centelleador generarán una ionización del mismo, a diferencia de los fotones que no la generarán. Esta ionización generará, a su vez, un pulso de luz que será recogido por una WLS que está enrollada dentro de las celdas centelleadoras. La luz será transmitida al sistema de lectura mediante fibras claras.

Para reducción de costes, estas 6000 celdas están divididas en grupos, utilizando un MAPMT (fotomultiplicadores multiánodo) de 64 canales para recibir la información en el sistema de lectura. La señal de salida de los fotomultiplicadores es irregular debido al bajo nivel de fotoestadística, unos 20-30 fotoelectrones por MIP, y debido también a la respuesta de la fibra WLS, que tiene un tiempo de bajada lento. Debido a todo esto y a la alta frecuencia del experimento (40MHz), el procesado de la señal, se realiza primero mediante la integración de la carga total y finalmente por la substracción de la señal restante fuera del período de integración.

Esta Tesis está enfocada en el sistema de lectura de la electrónica del VFE del SPD. Éste, está formado por un ASIC (diseñado por el grupo de la UB) encargado de integrar la señal, compensar la señal restante y comparar el nivel de energía obtenido con un umbral programable (que distingue entre electrones y fotones), y una FPGA que programa estos umbrales y compensaciones de cada ASIC, y mapea cada uno de los canales recibidos en el detector y finalmente usa serializadores LVDS para enviar la información de salida al trigger de primer nivel.

En el diseño de este tipo de electrónica se deberá tener en cuenta, por un lado, restricciones del tipo mecánico: el espacio disponible para la electrónica en sí, es limitado y escaso, por otro lado, el nivel de radiación que deberá soportar es

considerable y se tendrá que comprobar que todos los componentes usado superen un cierto test de radiación, y finalmente, también se deberá tener en cuenta la distancia que separa los VFE de los racks dónde la información es enviada y el tipo de señal con el que se trabaja en este tipo de experimentos: mixta y de poco rango.

Resum

El Laboratori d'Altes Energies de La Salle és un membre d'un grup acreditat per la Generalitat. Aquest grup està format per part del Departament d'Estructura i Constituents de la Matèria de la Facultat de Física de la Universitat de Barcelona, part del departament d'Electrònica de la mateixa Facultat i pel grup de La Salle. Tots ells estan involucrats en el disseny d'un subdetector en l'experiment de LHCb del CERN: el SPD (Scintillator Pad Detector).

El SPD és part del Calorímetre de LHCb. Aquest sistema proporciona possibles hadrons d'alta energia, electrons i fotons pel primer nivell de trigger.

El SPD està format per una làmina centellejeadora de plàstic, dividida en 600 cel.les de diferent tamany per obtenir una millor granularitat aprop del feix. Les partícules carregades que travessin el centellejador generaran una ionització del mateix, a diferència dels fotons que no la ionitzaran. Aquesta ionització, generarà un pols de llum que serà recollit per una WLS que està enrotllada dins de les cel.les centellejadores. La llum serà transmesa al sistema de lectura mitjançant fibres clares.

Per reducció de costos, aquestes 6000 cel.les estan dividides en grups, usant MAPMT (fotomultiplicadors multiànode) de 64 canals per rebre la informació en el sistema de lectura. El senyal de sortida dels fotomultilplicadors és irregular degut al baix nivell de fotoestadística, uns 20-30 fotoelectrons per MIP, i degut també a la resposta de la fibra WLS, que té un temps de baixada lent. Degut a tot això, el processat del senyal, es realitza primer durant la integració de la càrrega total i finalment per la correcció de la cua que conté el senyal provinent del PMT.

Aquesta Tesi està enfocada en el sistema de lectura de l'electrònica del VFE del SPD. Aquest, està format per un ASIC (dissenyat pel grup de la UB) encarregat d'integrar el senyal, compensar el senyal restant i comparar el nivell d'energia obtingut amb un llindar programable (fa la distinció entre electrons i fotons), una FPGA que programa aquests llindars i compensacions de cada ASIC i fa el mapeig de cada canal rebut en el detector i finalment usa serialitzadors LVDS per enviar la informació de sortida al trigger de primer nivell.

En el disseny d'aquest tipus d'electrònica s'haurà de tenir en compte, per un costat, restriccions de tipus mecànic: l'espai disponible per l'electrònica és limitat i escàs, i per un altre costat, el nivell de radiació que deurà suportar és considerable i s'haurà de comprobar que tots els components superin un cert test de radiació, i finalment, també s'haurà de tenir en compte la distància que separa els VFE dels

racks on la informació és enviada i el tipus de senyal amb el que es treballa en aquest tipus d'experiments: mixta i de poc rang.

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Chapter 1: Introduction

Chapter 1. Introduction

LHCb is one of the detectors hold at CERN (Conseil Européen pour la Recherche Nucléaire). It is the world largest High Energy Physics research center. Located on the Swiss–French border, CERN houses a variety of different accelerator machines and experiments. Founded in 1954, the laboratory was one of Europe's first joint ventures and is now including 20 Member States.

CERN's accelerators and detectors require cutting edge technology, and this is the reason why CERN works in close collaboration with the industry, searching for mutual benefit.

Figure 1. Aerial view of CERN accelerator complex.

LHCb is formed by several subdetectors described in the next Chapter; one of these subdetectors is the Calorimeter where the work done is related to. The Calorimeter is divided in four subdetectors again: the Hadronic Calorimeter (HCAL), the Electromagnetic Calorimeter (ECAL), the Preshower (PS) and the Scintillator Pad Detector (SPD).

The main goal of the Calorimeter is provided charged particles for first level trigger. These charged particles could be electrons or hadrons. On one hand, the hadrons give a great volume of energy in HCAL which is enough to distinguish them, and on the other hand, the electrons give its energy in the PS and ECAL but the distinction provided by deposited energy is not enough in this case: the desposited energy by photons is such as the energy deposited by electrons, therefore

distinguishing between charged particles or not charged is needed. The SPD is in charged of this function.

This PhD is focused on the design of the Very Front End Electronics involved in the Readout Unit of the SPD. The particular environment, the mechanical constraints, the working frequency as well as the kind of signal will make the electronics solution as a unique one. In this document will be discuss the restrictions and solutions provided for its design.

The following document is divided into the chapters mentioned below, in which the work done during these years is explained. The structure of the document is as follows: In Chapter 1, the global vision of the document is given. In Chapter 2, the context where this work is involved is explained. Chapter 3 gives some keys to take into account in this kind of experiments. Chapter 4 is focused on the subdetector that the group is in charge of designing. In Chapter 5 the solution of this part of the subdetector is described. Chapter 6 shows the results achieved not only during the prototype's design but also the series ones. In Chapter 7, work's conclusions are described. And finally, papers and publications resulting from research work are detailed in Chapter 8.

Chapter 2: Context

Chapter 2. Context

This Chapter explains the context where the PhD has been done. First of all it is explained the group where the work is related to, later it is explained the LHC, the particle accelerator where the experiment of LHCb belongs to, and finally, the LHCb and its subdetectors (SPD is one of them).

2.1. LIFAELS

The Experimental High Energy Physics group from Universitat de Barcelona had applied to join the LHCb Collaboration in 1998. Prior to this occasion, they offered the Departament d'Electrònica from Enginyeria i Arquitectura La Salle (Universitat Ramon Llull), together with the Departament d'Electrònica at UB, the possibility to join the collaboration in order to design the front end electronics of the SPD in LHCb. This event led to the creation of a group working in high energy physics instrumentation related to the LHCb project in EALS, which has continued to grow according to the project needs (LIFAELS). This collaboration was officially promoted by an agreement between both universities, signed at the end of the academic year 2001-2002. The presented PhD belongs to LIFAELS, the group working in instrumentation for high energy physics mentioned above.

2.2. LHC

The Large Hadron Collider (LHC) is a particle accelerator which will probe deeper into matter than ever before. Due to switch on in 2008, it will ultimately collide beams of protons at energy of 14 TeV.

Four experiments, with their corresponding detectors, will study what happens when the LHC's beams collide. They will handle as much information as the entire European telecommunications network does today.

As well as having greater energy than any other accelerator in the world, the LHC will also have the most intense beams. Collisions will happen so fast (40 million times a second) that particles from one collision will still be travelling through the

detector when the next collision happens. Understanding what happens in these collisions is the key to the success of the LHC.

The detectors are:

- ALICE
- ATLAS
- CMS
- LHCb (framework of this study)

2.3. LHCb (Large Hadron Beauty Collider) Experiment

A proton–proton collision with a centre of mass energy of 7+7 TeV has a high $b\bar{b}$ production cross section, about 500 μbarn[1] [1]. As a consequence, the LHC will be by far the most copious source of beauty particles ever built. The high luminosity of the machine will make available with large statistics Bu, Bd, Bs, Bc mesons and a variety of b–hadrons. This suggested installing on LHC a specialized b–physics detector. The name of this detector is LHCb and it is located in LHC P8 (see next figure). Its purpose is to study with high precision CP violation in the B mesons system and to look for new physics effects in rare decays of b–hadrons. The experimental data is expected to bring a deep understanding of the flavor physics inside the Standard Model and to suggest possible extensions.

[1] *A barn is the unit used in particle physics to measure cross sections that is the effective surface seen by a moving particle on the target. 1 barn = 10^{-28} m^2*

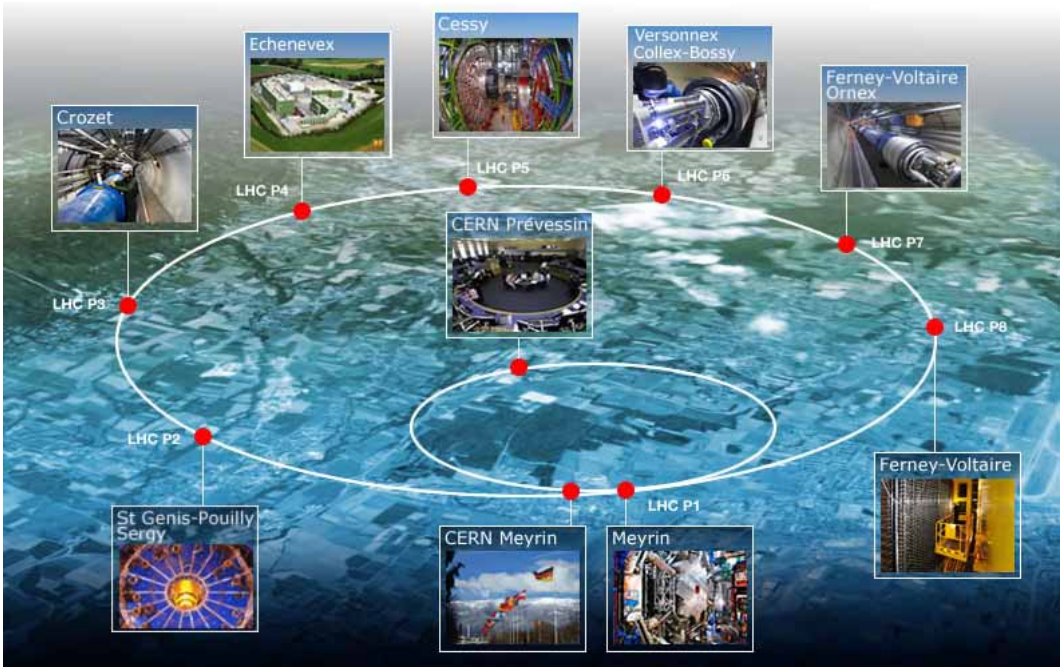

Figure 2. Different points of detectors.

Most of the particle trajectories of interest lie inside a cone of a few hundred mrad apertures, so there is no need to surround the interaction point with detectors. The LHCb design is then very different from the one of the others LHC detectors and from collider experiments in general. The chosen geometry is that of a single–arm forward spectrometer. In this configuration the detector can obtain the same precision as a double–arm one, but the statistics collected is cut in half. Figure 3 shows the actual LHCb layout. The total length of the detector is about 20 meters and it is limited by the cavern dimension. In order to analyze the experimental data, a right handed coordinate system has been defined. Its origin has been fixed on the interaction point; z runs along the beam axis, y points upwards and x points toward the centre of the LHC ring.

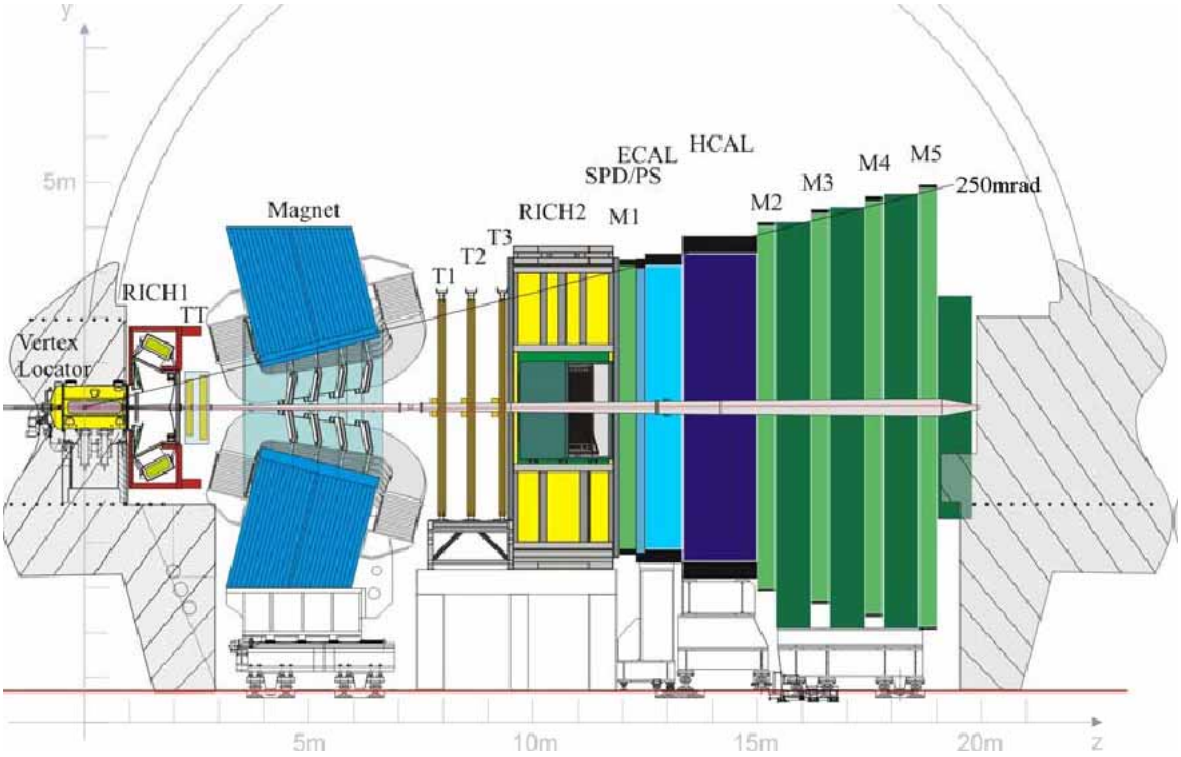

Figure 3. View of LHCb Detector

Given the overall detector shape, the single sub–detectors have to be designed to adapt to the events of interest. In particular, a robust and highly performing trigger and a particle identification system are mandatory in order to study the wide range of decay modes.

The LHC bunch crossing clock is 40MHz, which is a very high rate. Taking into account the various subdetectors, we find about 94900 channels (from 1 to 12 bit of resolution, which means 87 Kbytes in total) have to be processed each 25ns. This implies that information rate is about 3.48TBytes/s. It is obvious that is not possible to record or study such amount of information, for this reason and to select "interesting events" (only at the 0.5% of events there is a useful decay to study CP violation) a trigger system is designed to discard non interesting events.

2.3.1. VERTEX LOCATOR (VELO)

The hadrons produced in proton–proton primary interactions in LHC and containing beauty (anti–beauty) quarks are highly Lorentz boosted in the laboratory

reference frame and they travel about one centimeter before decaying. The spatial localization of the secondary vertices originated by b–hadrons decays is important information for the event selection system. The primary interaction point is then surrounded by a vertex locator. This device is constituted by 21 silicon stations placed along the beam direction, which can measure particle trajectories in cylindrical coordinates (r, θ, z). The silicon stations are placed at a radial distance from the beam which is smaller than the aperture required by LHC during injection and must therefore be retractable [3].

2.3.2. MAGNET

To measure charged particle momentum it is necessary to introduce a magnetic field. LHCb requires a dipole field with a free aperture of ±300 mrad horizontally and ±250 mrad vertically. In particular, the tracking detectors have to provide momentum measurement for charged particles with a precision better than 0.5% for momentum up to 200 GeV/c. This demands an integrated field of 4 Tm for tracks originating near the primary interaction point. Furthermore, good field uniformity along the transverse coordinate is required by the muon trigger.

The complicated shape of the coils and the high magnetic forces would make a superconducting magnet too expensive and mechanically unstable. LHCb has, therefore, moved to the design of a warm magnet cooled with water. To reduce electrical power requirements to about 4.2 MW, the pole faces are shaped to follow the acceptance angles of the experiment. Besides significantly lower costs, faster construction and lower risks, the warm coils offer additional advantages. A warm dipole permits rapid ramping–up of the field, synchronous to the ramping–up of LHC magnets, as well as regular field inversions to reduce systematic errors on asymmetries in CP violation [4].

This magnetic field will affect the electronics, and then it must be protected in some way as it is described in Chapter 4.

2.3.3. RICH DETECTORS

Particle identification (PID) is a fundamental requirement for LHCb. It is essential for the physics to separate pions from kaons in selected B meson decays. At wide polar angles the momentum spectrum is softer; hence the particle identification system consists of two RICH detectors. The upstream detector, RICH 1, covers the low momentum charged particle range~1-60 GeV/c using aerogel and C4F10 radiators, while the downstream detector, RICH 2, covers the high momentum range from~15 GeV/c up to and beyond 100 GeV/c using a CF4 radiator. RICH 1 has a wide acceptance covering the full LHCb acceptance from ±25 mrad to ±300 mrad (horizontal) and ±250 mrad (vertical) and is located upstream of the magnet to detect the low momentum particles. RICH 2 is located downstream of the magnet and has a limited acceptance of ±25 mrad to ±120 mrad (horizontal) and ±100 mrad (vertical) where there are mainly high momentum particles.

RICH 1 has vertical optical layout symmetry whereas for RICH 2 the symmetry is horizontal. Hybrid Photon Detectors (HPDs) are used to detect the Cherenkov photons in the wavelength range 200-600 nm. The HPDs are surrounded by external iron shields and are placed in Mumetal cylinders to permit operation in magnetic fields up to 50 mT.

2.3.4. TRACKING SYSTEM (TT, T1, T2, T3)

The tracking system is composed by four tracking stations. Its purpose is to detect tracks in the zone between RICH1 and RICH2 and to measure particles momentum from their curvature in the magnetic field. This system also has to determinate the direction of the particles crossing the two RICH detectors and it has to connect the information from the Vertex Locator with the information from the calorimeters and the muon chambers.

The tracking stations named respectively T1, T2 and T3 are placed downstream the magnet, just before RICH2. Each of these three stations is built using two different technologies. The innermost part, where the particle flux is greater, is called

Inner Tracker (IT), while the outermost part is named Outer Tracker (OT). The IT covers a cross–shaped area around the beam pipe, approximately 120cm wide and 40cm high.

Each IT station consists of four silicon strip detection layers, with two ±5° stereo views sandwitched in between two layers with vertical strips [5]. The OT, on the other hand, is constituted of straw–tube drift chambers.

The fourth tracking station is called Trigger Tracker (TT) and it is placed between RICH1 and the magnet. The TT station fulfils a two–fold purpose. Firstly, it is used to reconstruct the trajectories of low–momentum particles, which are bent out of the experiment acceptance by the magnetic field and thus do not reach stations T1–T3.

Moreover, the TT is used in the trigger to assign transverse momentum information to large impact parameter tracks. The TT is built entirely using the IT technology, but, in contrast with stations T1–T3, it will be split in two sub–stations, with a gap of 30cm in between the second and third detection layers [5].

2.3.5. *CALORIMETERS (SPD/PS, ECAL, HCAL)*

The main purpose of the LHCb calorimeter system is the identification of photons, electrons and hadrons and the measurement of their energies and positions. The collected data is immediately used in the L0 trigger to select the high pT^2 particles. Since this is a real–time selection, the information from the calorimeters has to be available within the 25 ns separating two bunch crossings. The selected data is also used for the complete reconstruction of electromagnetic and hadronic showers, but this analysis requires long time and so it is not part of the L0 trigger. The other essential function of the calorimeter system is the detection of photons with enough precision to allow identification of decay channels which contain in the final state a prompt photon or a neutral pion.

The calorimeter system is constituted of three different sections. The first one, the one closer to the interaction point, is constituted of two detection planes located just

[2] *p_T stands for transverse momentum, that is the fraction of the linear momentum perpendicular to the beam direction.*

before and just after a 15mm thick lead wall. The detector elements are 15mm thick scintillator pads, which are called respectively Scintillator Pad Detector (SPD) and PreShower detector (PS). A groove in the scintillator holds the helicoidal WaveLength Shifter (WLS) fiber which collects the scintillation light. The light from both WLS fiber ends is sent by long clear fibers to multianode photomultipliers that are located above and below the detector. Since the number of interacting particles per unit surface varies of two orders of magnitude moving from centre to the outer edge, the SPD/PS has been divided in three concentric zones with different spatial granularity.

The Electromagnetic Calorimeter (ECAL) is placed just downstream the PS. It has a sampling structure of 2mm lead sheets interspersed with 4mm thick scintillator plates.

The produced light is collected by WLS filers, which are then bunched together and read by phototubes. Similarly to SPD/PS, ECAL is divided in three zones with different spatial granularity.

The Hadronic Calorimeter (HCAL) is the last calorimeter section. The sampling structure has 16 mm thick iron plates spaced with 4 mm thick scintillator plates, readout via WLS fibers. Given the dimensions of the hadronic showers and the performance requirements of the hadron trigger, the HCAL cells were chosen larger than those of ECAL. Furthermore, a lateral segmentation into only two zones has been adopted [6]. More details about the Calorimeters are explained on Chapter 4.

2.3.6. MUON SYSTEM (M1, M2, M3, M4, M5)

Muon triggering and offline muon identification are fundamental requirements of the LHCb experiment. The main requirement for the LHCb muon system is to provide a high–pT muon trigger at the earliest trigger level (L0). In addition, the muon trigger must unambiguously identify the bunch crossing, requiring a time resolution better than 25 ns. The heavy– flavour content of triggered events, enhanced by requiring the candidate muons to have high transverse momentum, is

utilized also offline, to accurately identify muons reconstructed in the tracking system and to provide a powerful B–meson flavour tag.

The muon system consists of five muon tracking stations, named M1, M2, M3, M4 and M5, placed along the beam axis and interspersed with shields to attenuate hadrons, electrons and photons. The first station is located just downstream RICH2 and before the calorimeters, which constitute the attenuator between M1 and M2. These two stations are the ones used to evaluate pT for the L0 trigger. The other three stations are positioned after M2 and are interspaced with iron walls 80 cm thick [7].

Stations M2–M5 are constituted of four layers of Multi–Wire Proportional Chambers (MWPC), while the outermost part of M1 has only two MWPC layers in order to reduce the material budget seen by the calorimeters [8]. In the innermost region of the first station, where the particle flux is higher, the MWPC technology is not suitable. Here the Gas Electron Multiplier (GEM) technology is used, in the form of a triple–GEM detector [9], [10].

2.3.7. TRIGGER & DATA STORAGE

The LHCb sub–systems will produce a large quantity of raw data, which has to be combined and analyzed in order to extract the final results.

The online analysis is clearly not possible as a result of the large amount of data, about 3.48Tbytes/s. The adopted strategy is that of a cascade– like system, in which the lower levels operate very fast and rough decisions and pass the selected events to the upper levels. The implemented system consists of two layers.

• *Level zero trigger (L0)*. The lowest level of trigger is completely implemented in custom electronics. The input frequency is 40 MHz, corresponding to the proton–proton bunch crossing, while the output frequency is 1 MHz. It takes data from SPD, PS, ECAL, HCAL and from the muon system and selects particles with pT. Also the VELO Pile–Up system is considered, in order to reject high–multiplicity events. This rejection assures that the selection is based on b–signatures rather than large combinatorics and that the selected events will not occupy a disproportional fraction

of the data–flow bandwidth or available processing power in the subsequent trigger level.

• *High Level Trigger (HLT).* The HLT is a software trigger and it is based on data from all sub–detectors. The input frequency is 1 MHz and the output frequency is 2 kHz [11].

2.3.8. FRONT-END ELECTRONICS ARCHITECTURE

The front-end architecture chosen for LHC has to a very large extent been determined by the intrinsic problem of making a hardwired short latency trigger, with an efficient event selection, for complicated B events. A fast first level trigger has been found capable of making an event rate reduction of the order of 1 in 10. This has for the chosen LHCb luminosity enforced the use of a front-end architecture with a first level trigger rate of up to 1MHz. This was considered to be highest rate affordable for the DAQ system and required readout links. All sub-detectors store sampled detector signals at the 40 MHz bunch crossing rate in 4 μs deep pipeline buffers, while the hardwired first level trigger (L0) makes the required trigger selection.

The path that information follows: it begins at Front End System level which works at the same frequency as bunch-crossing, namely 40MHz. This information arrives to the Level0 system that is in charge of making the first trigger selection. Then, the HLT recognizes proper events and finally and gets the L0 decision. Finally, the filtered information arrives to the DAQ system.

2.3.9. ONLINE SYSTEM

The task of the Online system is to ensure the transfer of the data from the front-end electronics to permanent storage under known and controlled conditions. This includes the movement of the data themselves, but also the setting up of all the operational parameters of the experiment and the monitoring of these and the environmental parameters, such as temperatures or pressures. The online system also

has to ensure that all detector channels are transferring their data at the same time, relative to the collisions of the particles in the accelerator.

The LHCb Online system consists of three components:

- *Data Acquisition (DAQ) system*: Its purpose is transporting the data belonging to a given bunch crossing, identified by the trigger, from the detector front-end electronics to permanent storage.
- *Timing and Fast Control (TFC) system*: The TFC system drives all the stages of the data readout of the LHCb detector between the Front-End electronics and the online processing farm by distributing the beam-synchronous clock, the L0 trigger, synchronous resets and fast control commands.
- *Experiment Control System (ECS):* It ensures the control and monitoring of the operational state of the entire LHCb detector. This encompasses the traditional Detector Control, such as high and low voltages, temperatures, gas flows, or pressures, but also the control and monitoring of the Trigger system and the TFC and DAQ systems. The hardware components of the ECS are somewhat divers, mainly as a consequence of the variety of the equipment to be controlled. This ranges from standard crates and power supplies to individual electronics boards. In LHCb a large effort was made to minimize the number of different types of interfaces and connecting busses. The field busses have been restricted to:
    - SPECS, Serial Protocol for ECS, a serial bus providing high-speed, 10Mb/s, control access to front-end electronics [37]
    - CAN (Controller Area Network[3])
    - (fast)Ethernet

Figure 4 shows the general architecture of the LHCb online system.

[3] .ISO Standard 11898., see e.g. www.iso.org

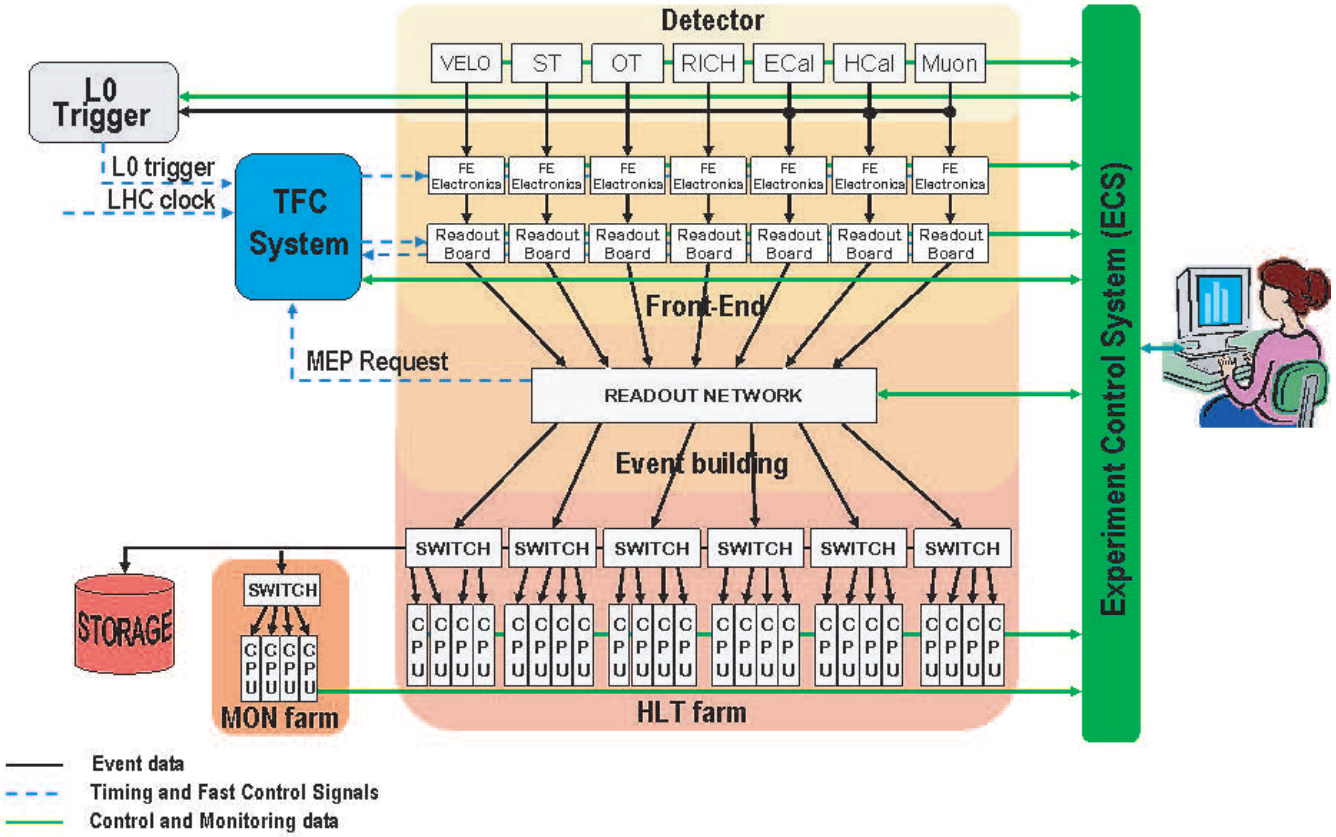

Figure 4. General architecture of LHCb Online System

Chapter 3: Electronics in particle physics

Chapter 3. Electronics in particle physics

Electronics in instrumentation is very important to advance in any field. Focusing in the field of particle physics[4], where the LHCb detector belongs to, the kind of electronics that is used must accomplish some requirements.

On first term, the environment where these electronics must hold with magnetic fields, as it is said in the last Chapter; there is a magnet which makes a magnetic field in order to measure the charged particle momentum, on second term a radiation quote produced by the collision of particles. This fact will imply that every component used in the design must be radiation tolerant; therefore the amount of components that can be used is limited. The kind of signals used in particle physics has to be taken into account as well, as a result of being small range, noisy and sometimes with a difficult processing. This fact forces in most cases a full custom design for the processing.

On last term, the mechanical form of the detector implies some constraints again: large distances from Front End Electronics to the racks where the information is processed. This fact implies the use of several techniques for avoiding interference, noise, skew, jitter…and also the power consumption has to be taken into account in order to decide which way is the best to feed the Front End Electronics.

Next pages explained with more detail these effects on the electronics.

4 High energy physics (HEP) study phenomena occurring at very high energies, creating conditions under which matter behaves in non usual ways and then new Nature laws manifest. HEP experiments consist normally in colliding accelerated particles with other accelerated particles or with fixed targets. Collision produces complicated reactions which are detected, stored and studied in order to find these new Nature laws.

3.1. Radiation Environment

The main applications where radiation environment is a key consideration are medical equipment, high energy physics, nuclear power plants, astronomy, aerospace field and military.

Radiation effects on electronics devices can be divided into two categories: cumulative effects and Single Event Effects (SEE).

3.1.1. Cumulative Effects

They are due to the creation or activation of microscopic defects in the device. Each defect is not significant in itself but the accumulation of these effects can cause the failure of the device. The cumulative effects are mainly of two kinds:

Displacement Damage

Non-ionizing energy losses in silicon cause atoms to be displaced from their normal lattice sites, seriously degrading the electrical characteristics of semiconductor devices. In displacement damage, it is a common practice to express the radiation environment in terms of particle fluency (particles/cm2). Since the damage induced is a function of the nature and energy of the particle, the Non-Ionizing Energy Loss (NIEL) is used as a parameter for correlating the effects observed in different radiation environments. Though this correlation is not free from uncertainties and failures in some cases, it is still commonly used to translate a complex radiation environment into a simpler mono-energetic equivalent, namely 1 MeV neutrons. The macroscopic effect of displacement damage varies with technology. CMOS devices are practically unaffected up to particle fluencies much higher than those expected at LHC [12]. In bipolar technologies, displacement damage increases the bulk component of the transistor base current, leading to a decrease in gain. Other devices which are sensitive to displacement damage are some kinds of light sources, photodetectors and optocouplers.

Total Ionizing Dose (TID)

TID effects are due to the energy deposited in electronics by radiation in the form of ionization. The unit for TID in the International System is the Gray (Gy), but the radiation effects community still widely uses the old unit, the rad. The conversion between the two units is simple: 1 Gy = 100 rad. The performance of electronics is affected by the dose deposited in the silicon dioxide used in semiconductor devices for isolation purposes. Ionization in this material leads to the generation of electron-hole pairs, which can be separated by a local electric field. Holes can be trapped in the oxide or migrate to the Si-SiO_2 interface to participate in the complex mechanism of interface states creation. Both kinds of defects (trapped holes or interface states) accumulate to affect the behavior of the semiconductor devices.

The consequent macroscopic effect varies with technology. In CMOS technologies, threshold voltage of transistors shifts, mobility and transconductance decrease, noise and matching performance degrade, and leakage currents appear. In bipolar technologies, transistors gains decrease and leakage currents appear.

3.1.2. Single Event Effects

These effects are due to the direct ionization of a single particle, which is able to deposit the necessary amount of energy to disturb the correct operating of the device.

Single Event Effects (SEEs) are divided in three groups:

Permanent SEEs

Also known as 'Hard errors', they may be destructive.

Single Event Latchup (SEL) occurs in CMOS technologies. The onset of a parasitic p-n-p thyristor is triggered by the depositing of ionizing energy in a sensitive point of the circuit. This leads to an almost short-circuit current on the power lines, which can permanently damage the device. Sometimes, this condition can be local and the current can be limited (microlatch), but the effect can still be destructive.

Single Event Burnout (SEB) occurs in power MOSFETs, BJT and diodes when these power devices are in the 'off' state. The short-circuit current induced across the high voltage junction can permanently damage the device.

Single Event Gate Rupture (SEGR) also affects power MOSFETs in the 'off' state. The dielectric gate can be permanently damaged when, due to the energy deposited by an incoming particle, the electric field across the oxide is temporarily increased beyond the breakdown limit.

Static SEEs

Static effects are not destructive, and happen whenever one or more bits of information stored by a logic circuit are overwritten by the charge collection following the ionization event. This effect is defined **Single Event Upset (SEU**). A special case of SEU is called Single Event Functional Interrupt (SEFI). This happens in complex circuits due to an error induced on a bit of information which controls a special function of the circuit (most often, a special test mode). A reset is necessary to bring the circuit back to the operational condition.

Transient SEEs

Charge collection from an ionization event creates a spurious signal that can propagate in the circuit. This can happen in most technologies, and its effect varies very significantly with the device, the amplitude of the initial current pulse, and the time of the event in relation to the circuit. Typical examples are transient pulses in combinatorial logic, which can propagate and ultimately be latched in a register, and rail-to-rail voltage pulses at the output of operational amplifiers **(SET**).

3.1.3. Safety Factors

The radiation level estimations for LHCb are generated from Monte Carlo simulations with FLUKA. Uncertainties related to the Monte Carlo simulations and their assumptions on interaction models are normally estimated to be of an order of a factor two. The radiation hardness qualification of components will also have uncertainties associated with them (e.g. dosimeter uncertainties). The components

themselves may have significant uncertainties depending on the origin of the components. ASICs from a well defined processing batch will only have a relatively small uncertainty on their measured radiation hardness. Commercial components purchased as a single lot from a well defined production batch will normally also only have limited radiation hardness variations. Commercial components purchased in different lots from independent distribution sources can be expected to have significant variations in radiation hardness.

The safety factors to apply to the qualification of components for LHCb strongly depends on the type of radiation effect, the type of component and the specific use of the component in LHCb. The final choice of safety factors used all boils down to general risk management. The total risk of failing components compromising the correct function of LHCb must be minimized within an acceptable budget. Components used in locations where they cannot easily be exchanged must be qualified with significant safety factors. Components (e.g. modules) that can be exchanged within a few hours can potentially be qualified with lower safety factors.

A clear distinction must be made between accumulated effects and single event effects. Single event effects are of statistical nature and may therefore occur at any time and at any place (obviously proportional to flux of particles and sensitivity of components). For single event effects it is important to ensure that the time between failures is sufficiently long to guarantee an effective running of the whole experiment over extended periods. Single event upsets can be recovered by a simple re-initialization of the electronics. The re-initialization of the electronics can be done at several levels. State-machines or pipeline registers can normally be recovered by a "simple" reset. Single event upsets in configuration registers will require a reloading of parameters via ECS (Experiment Control System). In both cases it will be necessary to restart active data taking with the DAQ system. It is important to ensure that this kind of soft failure does not occur so often that the system will spend a significant part of its time resolving random single event upsets. Single event upsets that prevents single detector channels to work correctly can in many cases be accepted during limited time periods, if and only if this do not significantly affect the physics and the triggers of the experiment. Bit flips in event data itself can normally be tolerated if they do not have any effect on the correct handling of following

events. Single event latchup's (and single event burnout) will in many cases be a fatal failure requiring repair, unless special latchup protection circuits have been used. Single event Latchup must therefore be proven to happen sufficiently seldom that the whole LHCb experiment can work for several weeks without repair. Even hard failures can in some cases be accepted during extended periods if it can be guaranteed that the failure do not seriously affect the physics performance of the experiment. In many cases a few local "dead" detector channels will not have a significant effect on the physics of the experiment. It must though be ensured that local failures are prevented from disturbing higher levels of the system and thereby affect data collected from other parts of the detector.

Cumulative effects risk to make large parts of an electronic system unusable after a given radiation threshold has been reached. Such a situation may occur after several years of operation at a time when the components used have become obsolete and cannot be purchased commercially. For systems with large variations in radiation levels for different parts of the system (e.g. small part of front-end electronics very close to beam line) it can be envisaged to exchange limited parts of the electronics system after a certain number of years. For systems with a more uniform radiation exposure it is unrealistic to start exchanging components when they start to fail one by one. In this case it must be proven that the system can stand the radiation levels over many years of operation (10 years).

Safety factors for cumulative effects (total dose and displacement damage)

- Simulation uncertainty => Factor 2
- Radiation qualification uncertainty => Factor 2
- Component to component variation :
    - Same fabrication line, no technology changes=> Factor 2
    - Same manufacturer, unknown fabrication line=> Factor 100
    - Different manufacturer=> Re-qualification required

For cumulative effects this adds (multiplies) up to total safety factors between 8 to 400. It is clearly seen that large safety factors are required if the components used do

not come from the same fabrication line (or similar line with same process) as the components initially qualified for radiation resistance. It is in fact quite difficult in practice to guarantee that commercial components come from production lines with the same process characteristics. The safety factor related to this (100) can though be significantly lowered (2) if a new production lot, all coming from the same production line (but not necessarily the same as the qualified ones), are re-qualified by testing a new set of samples from the final lot.

The safety factor of 100 for the case of an unknown fabrication line does in fact not really make sense since certain technology changes may have very large effects on the radiation tolerance and is in principle unpredictable. The chosen safety factor has been taken as to have some confidence that in practice things will not get worse than this. In most cases such a large safety factor will enforce a re-qualification except for locations with very low radiation levels (e.g. concrete tunnel).

The minimum total safety factor of 8 can only in special justified cases be decreased. If it can be justified that the radiation qualification has been made with very precise monitoring of the radiation levels the safety factor related to this can potentially be decreased. If a thorough radiation qualification of a statistically significant part of the final production batch have been made (more than 10 units) the safety factor related to component to component variations can potentially be decreased. The acceptance of such exceptional cases can only be made after a special review organized by the electronics coordinator and a final acceptance by the LHCb technical board.

Safety factors for single event effects

- Simulation uncertainty => Factor 2
- Radiation qualification uncertainty=> Factor 2

As single event effects are a question of statistics, the number of possible failures must be estimated and the effect of the failures on the system must be evaluated. No strictly defined radiation hardness criteria can therefore be given. From a system perspective a few guidelines can though be defined. Acceptable failure rates for different failure types can be defined at the system level. To define acceptable failure rates for individual sub-systems a simple model assuming ~10 independent sub-

systems (individual sub-detectors, L0 trigger, HLT trigger, DAQ, etc.) in LHCb is used. Failure rates must be handled differently according to the following classification:

Single bit flips in event data with no effect on following events. Single bit errors in event data can in general be accepted when it is assured that it will not have any negative effect on following events

SEU requiring reset of front-end electronics and re-synchronize DAQ system. Bit flips in state-machines, pipeline registers and other synchronization logic in the front-end electronics, that only needs a front-end reset sequence (L0 +HLT front-end reset) to recover correct function, can potentially be handled at rates up to several times per minute if really required.

SEU requiring instant re-initialization of front-end electronics via ECS. Bit flips in setup and configuration registers in the front-end electronics will need to be corrected by the ECS system downloading new configuration data.

SEU in configuration data that can wait for next planned re-configuration. For bit flips in configuration data that does not need immediate correction for LHCb to continue to work efficiently one can possibly wait for the next reconfiguration to be made (~once per day). Even in this case it is important to have schemes to detect that such a condition has occurred.

Hardware failures requiring instant repair. Fatal system failures requiring instant repair for the experiment to work is obviously the most serious failure mechanism. Such failures can be caused by single event latchup in integrated circuits or single event burn out in a power supply (or other possible failure mechanisms not related to radiation). The time required to repair such failures strongly depend on the location of the electronics:

Counting room: Radiation levels in the counting room is so low that electronics will not be affected and immediate access can be given while LHC is running. Electronics can be repaired with a few hours notice (assuming spare parts available).

Cavern with insignificant residual radiation: Can in principle be accessed with a few days notice. Access periods will strongly depend on the running conditions of the LHC machine itself. At startup of LHC it is planned to have short weekly shut-

downs of the LHC machine. When reliable operation of LHC is achieved, access to the cavern will depend on agreed shut-down periods between all the LHC experiments and the LHC machine.

Cavern with residual radiation: Residual radiation will in some cases limit access to long shutdown periods (~once per year) where things have time to cool down. The regions around the interaction point (vertex tank) and the beam pipe will in this respect pose potential problems. Electronics where a single point failure can prevent LHCb to collect worthy physics data should never be placed in zones with significant residual radiation.

Inside detectors: Electronics located inside detectors can only be repaired when detectors are open which can only be done during long shut-down periods (once per year). Electronics modules vital for the global LHCb experiment must never be placed inside detectors in most cases, but for example, for the SDP VFE there is no other way to manage it.

Hardware failures not requiring instant repair: Electronics dealing with limited number of isolated detector channels can normally be accepted to have hardware failures for limited time periods without affecting seriously the physics of LHCb. For electronics located in the cavern, without residual radiation these failures will be repaired at the first possible occasion (~once per month). For electronics located in zones with significant residual radiation, or within the detector itself, repairs can only be performed once per year and it must be ensured that only an insignificant number of detector channels will be lost over a period of one year of running.

3.1.4. Material Activation

Materials can become activated when hadronic interactions occur within them; that is the case of the LHCb experiment where, as in any accelerator environment, a multitude of radionuclides can be produced due to spallation reactions. On the other hand not all interactions yield radioactive isotopes; the resulting nuclide can in fact also be stable. Many radioactive isotopes have short half-lives and disappear rather quickly, while other have longer decay constants and remain active in the material

for an extended period of time. In the latter case, the materials have to be considered as radioactive and an appropriate handling and disposal schemes have to be devised [39]. Some studies have been performed with FLUKA simulation code [40, 41], to determine the induced radioactivity of the materials in the LHCb experimental setup with the aim of defining a Radioactive Waste Reference Zoning for LHCb equipment.

One of the main concerns in the design of the experiment was to keep the material budget to a minimum within the acceptance from the interaction point (IP) to the Calorimeters. Although the impact on the physics measurements was the main reason to do so, this also results in a reduced amount of hadronic interactions, and thus activation, in the region from the IP to z ~ 1200cm. A significant amount of activation is expected in the Calorimeters and Muon Filters, particularly in the very forward region, and very closes the IP.

Figure 5 shows the simulations in SPD/PS after 10 years of operation and 2 years of cooling [39].

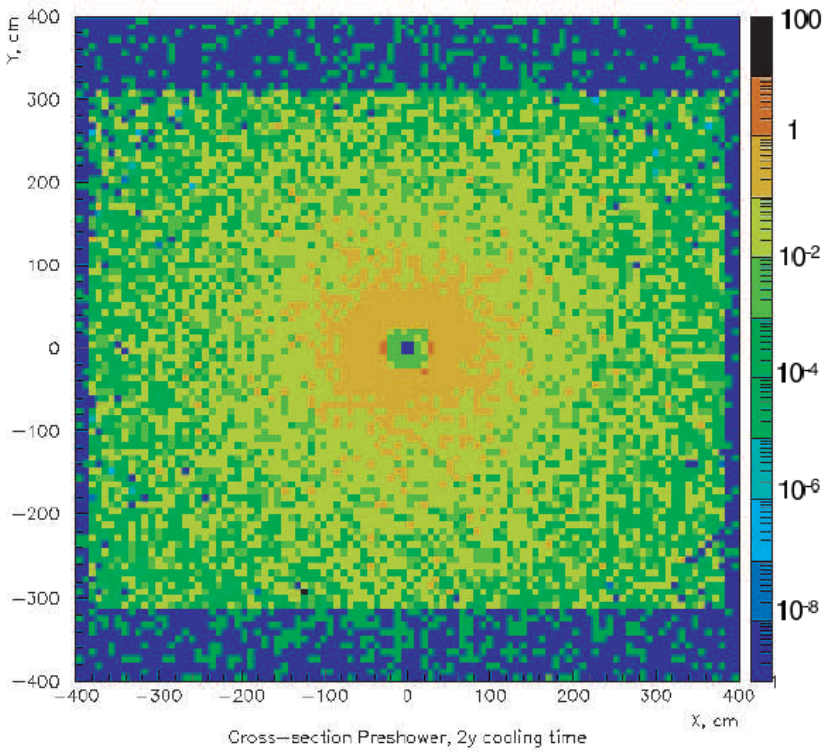

Figure 5. Relative activity in the SPD-PS lead, averaged over the lead thickness. 10 years of operation and 2 years cooling time.

3.1.5. *Figures*

Some figures about radiation in Calorimeter found by simulation, is shown in the Table 1.

	Sub-system	*x (m)*	*y (m)*	*z (m)*	*Total dose (Rad) (10 years)*	*1 Mev Neutron eq. (10 years)*	*Hadrons > 20 Mev (10 years)*
Calorimeters	SPD FE	-4.0<x<4.0	+3.5 -3.5	12.2	max = $5.8*10^3$ ave = $3.5*10^3$	$9.3*10^{11}$ $8.2*10^{11}$	$4.8*10^{10}$ $4.1*10^{10}$
	Preshower FE	-4.0 <x< 4.0	+3.5 -3.5	12.4	max = $5.8*10^3$ ave = $3.5*10^3$	$9.3*10^{11}$ $8.2*10^{11}$	$4.8*10^{10}$ $4.1*10^{10}$
	ECAL crates	-4.0 <x<4.0	3.8 <y< 5.5	13	max = $3.7*10^3$ ave $=2.2*10^3$	$1.1*10^{12}$ $8.5*10^{11}$	$3.5*10^{10}$ $2.5*10^{10}$
	HCAL crates	-4.0 <x<4.0	3.8 <y< 5.5	14	max $=4.8*10^3$ ave = $3.3*10^3$	$1.9*10^{12}$ $1.3*10^{12}$	$5.5*10^{10}$ $3.8*10^{10}$

Table 1 Radiation quotes for Calorimeter.

As it is assumed, as a result of these figures, the electronics of the VFE must be radiation tolerant. The radiation tolerance of the unqualified commonly commercial components (COTS)s of the VFE card as well as the ASIC, was tested through irradiation with heavy ions and the experiment was carried at the Gran Accelerateur National d'Ions Lourds (GANIL) in Caen [15]. After extrapolating the results to the LHCb environment, the expected SEU cross-section value is $4.2 \cdot 10^9$ neutrons·cm^{-2}·year^{-1} and can be concluded, considering a 6000 channels detector, that will be less

than 2.73 ≈ 3 SEU/year, that is a very satisfactory result. Concerning the Single Event Latch-up effect and for a maximum LET of 15 $MeV \cdot cm^2 \cdot mg^{-1}$ foreseen in the LHCb none has been detected; and, therefore, with a confidence limit of 90% the probability to find a SEL is smaller than one every 20 years. No effect was observed in the ASIC performance for an accumulated dose of 40 KRads.

More information about Radiation Effects at LHCb can be found in [12], [13], [14], [15].

3.2. Signal Characteristics

Most common signals in particle physics have the same characteristics:

- Analog in most cases
- Short range
- The need for a specific discriminator
- Volume of data rate

Particle physics experiments commonly have the same distribution, as it is mentioned in Chapter 2: front end electronics near the particle beam working at high frequency and the system processing of data generated by the front end working at low frequency, far away.

Front end electronics usually have a specific discriminator. In fact, it is usually designed specifically for the experiment, an ASIC. This is a result of the small range of signals obtained from the experiment, in most cases a small analog signal that needs to be amplified, integrated and must make it differential for its posterior treatment. Differential lines are common in these experiments as a result of its robustness in front of hardness environment.

The data rate volume in this kind of experiment is very high. Therefore, the design of the data processing path is one of the most tedious tasks in the experiment. However, it is impossible to treat the whole volume of data available, making it necessary to identify the 'good' events, those containing information, this identification is made at Level 0 Trigger. Afterwards, the analysis is made at HLT with a low level data rate.

Communication between two systems is also a critical point, as a result of the distance between them. Actually, LVDS has become a standard for these kinds of links where optical fibber system is not possible to implement.

3.3. LVDS Signals

3.3.1. Introduction

Low-Voltage Differential Signaling (LVDS) is a new technology addressing the needs of today's high performance data transmission applications.

It is not a common characteristic for Electronics in particle physics but a good solution for the problems in transmission that this kind of Electronics has.

The LVDS standard is becoming the most popular differential data transmission standard in industry. It is also designed to meet the needs of future applications, since the power supply may be as low as 2V. This technology is based on the ANSI/TIA/EIA-644 LVDS Interface Standard.

LVDS delivers high data rates while consuming significantly less power than competing technologies. In addition, it brings many other benefits, which include:

• Low-voltage power supply compatibility

• Low noise generation

• High noise rejection

• Robust transmission signals

• Ability to be integrated into system level ICs

LVDS technology features a low voltage differential signal of 330mV (250mV MIN and 450mV MAX) and fast transition times. This allows the products to address high data rates ranging from 100's Mbps to over 1 Gbps. Additionally, the low voltage swing minimizes power dissipation while providing the benefits of differential transmission.

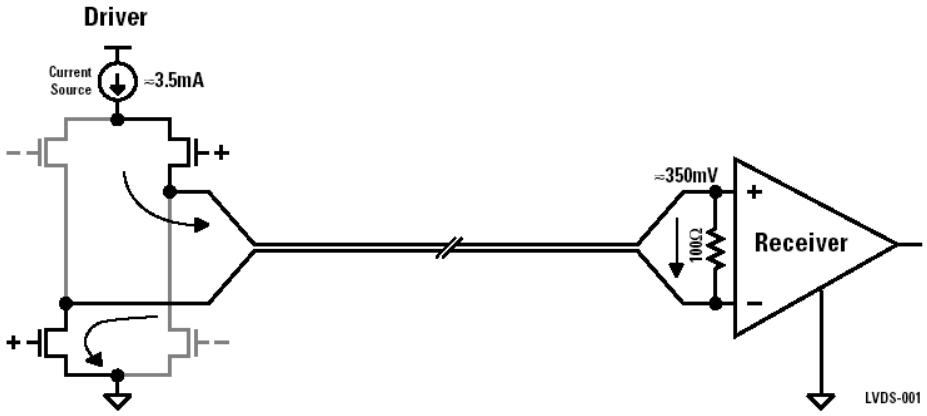

Figure 6. Diagram of LVDS Driver and Receiver

The LVDS technology is used in simple line driver and receiver physical layer devices as well as more complex interface communication chipsets. The Channel Link chipsets multiplex and demultiplex slow TTL signal lines provides a narrow, high speed, low power LVDS Interface. These chipsets provide dramatic system savings in cable and connector costs, as well as a reduction in the amount of physical space required for the connector footprint.

LVDS solutions provide designers with a new alternative for solving high speed I/O interface problems. LVDS delivers Megabits @ milliwatts for the bandwidth hungry data transmission applications of today and tomorrow.

The next pages explain the most important topics applied to the work carried out.

3.3.2. Why use low-swing differential?

The differential data transmission method used in LVDS is less susceptible to common-mode noise than single-ended schemes. Differential transmission uses two wires with opposite current/voltage swings instead of the one wire used in single-ended methods to convey data information. The advantage of the differential approach is that if noise is coupled onto the two wires as common-mode (the noise appears on both lines equally) and is thus rejected by the receivers, which looks at only the difference between the two signals.

The differential signals also tend to radiate less noise than single-ended signals, due to the cancelling of magnetic fields. In addition, the current-mode driver is not prone to ringing and switching spikes, further reducing noise.

Because differential technologies such as LVDS reduce concerns about noise, they can use lower signal voltage swings. This advantage is crucial, because it is impossible to raise data rates and lower power consumption without using low voltage swings. The low swing nature of the driver means data can be switched very quickly. Since the driver is also current-mode, very low – almost flat – power consumption across frequency is obtained. Switching spikes in the driver are very small, so that ICC does not increase exponentially as switching frequency is increased. Also, the power consumed by the load (3.5 mA x 350 mV = 1.2 mW) is very small in magnitude.

Another voltage characteristic of LVDS is that drivers and receivers do not depend on a specific power supply, such as 5V. Therefore, LVDS has an easy migration path to lower supply voltages such as 3.3V or even 2.5V, while still maintaining the same signaling levels and performance. In contrast, technologies such as ECL or PECL have a greater dependence on the supply voltage, which makes it difficult for migrating systems using these technologies to lower supply voltages.

3.3.3. Termination

The transmission medium must be terminated to its characteristic differential impedance to complete the current loop and terminate the high-speed (edge rates) signals. That requirement is the same, whether the LVDS transmission medium consists of a cable or of controlled impedance traces on a printed circuit board.

If the medium is not properly terminated, signals reflect from the end of the cable or trace and may interfere with succeeding signals. Proper termination also reduces unwanted electromagnetic emissions and provides optimum signal quality.

To prevent reflections, LVDS requires a terminating resistor matched to the actual cable or PCB trace differential impedance. Commonly, 100W media and terminations are employed. This resistor completes the current loop and properly terminates the signal. This resistor is placed across the differential signal lines as close as possible to the receiver input.

Maximum Switching Speed

The maximum switching speed of an LVDS Interface is a complex question, and the answer depends on several factors. These factors are the performance of the line driver (edge rate) and receiver, the bandwidth of the media, and the required signal quality of the application.

Since the driver outputs are very fast, the limitation on speed is commonly restricted by:

1. How fast TTL data can be delivered to the driver – in the case of simple PHY devices that translate a TTL/CMOS signal to LVDS.

2. Bandwidth performance of the selected media (cable) – type and length dependent.

Channel Link devices (SerDes) capitalize on the speed mismatch between TTL and LVDS by serializing the TTL data into a narrower LVDS data stream (more about this further on.)

3.3.4. Saving Power

LVDS technology saves power in several important ways. The power dissipated by the load (the 100W termination resistor) is a mere 1.2 mW. In comparison, an RS-422 driver typically delivers 3V across a 100W termination. It dissipates 90 mW of power — 75x more than LVDS.

LVDS devices are implemented in CMOS processes, which provide low static power consumption. The circuit design of the drivers and receiver require roughly one-tenth the power supply current of PECL/ECL devices.

Besides the power dissipated in the load and static IDD current, LVDS also lowers system power through its current-mode driver design. This design greatly reduces the frequency component of IDD. The IDD vs. frequency plot for LVDS is virtually flat, between 10 MHz and 100 MHz. The quad device, DS90C031/2 uses less than a total of 50 mA, for driver and receiver at 100 MHz. This can be compared to TTL/CMOS transceivers, the dynamic power consumption of which increases exponentially with frequency.

3.3.5. Configurations

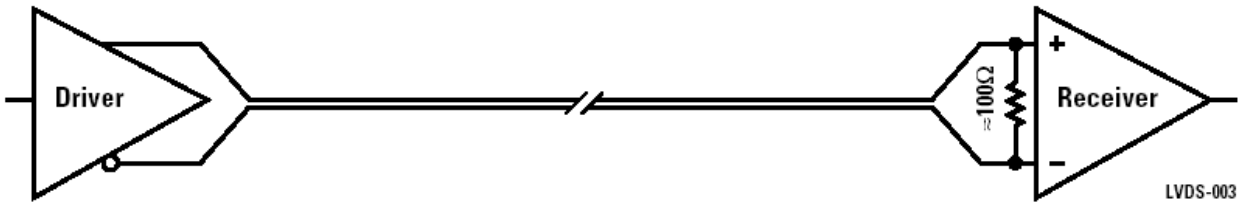

Figure 7. Point to point configuration

LVDS drivers and receivers are commonly used in a point-to-point configuration, as shown in the previous figure.

Dedicated point-to-point links provide the best signal quality due to the clear path they provide. In this configuration, LVDS is capable of transmitting high-speed signals over substantial lengths of cable while using remarkably little power and generating very little noise. However, other topologies/configurations are also possible.

When the system architect is more interested in minimizing the number of interconnections than in raw performance, LVDS is a great technology to consider. LVDS is well suited for bi-directional signaling and bus applications.

3.3.6. Economical interface

LVDS is a cost-effective solution:

1. LVDS CMOS implementations provide better price/performance ratios as compared to custom solutions on elaborate processes.

2. High performance can be achieved using common, off-the-shelf CAT3 cable and connectors, and/or FR4 material.

3. LVDS consumes very little power, thereby reducing or eliminating power supplies, fans and other peripherals.

4. LVDS is a low-noise and noise-tolerant technology, minimizing problems.

5. LVDS transceivers are cost-efficient products that can also be integrated around digital cores providing a higher level of integration.

6. LVDS moves data much faster than TTL, so multiple TTL signals can be serialized or multiplexed into a single LVDS channel, reducing board, connectors, and cabling costs.

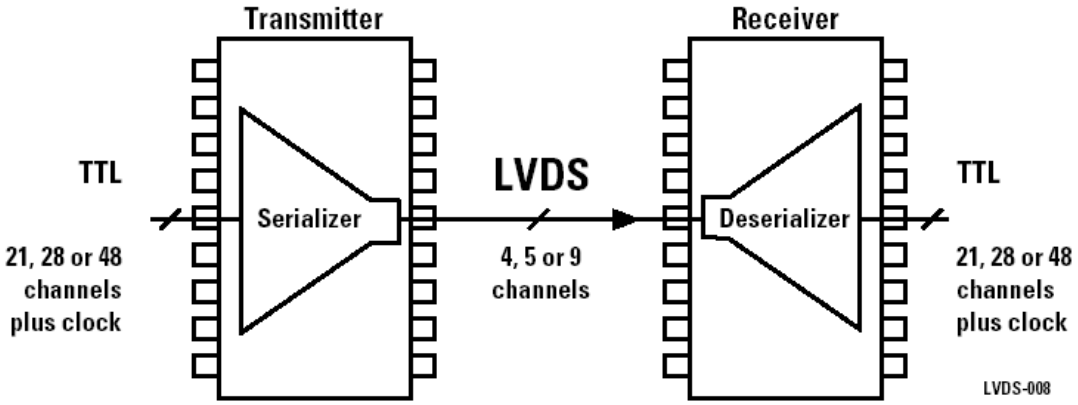

Figure 8. Channel Link Chipset

In fact, in some applications, the Printed Circuit Board (PCB), cable, and connector cost savings greatly overshadow any additional silicon costs. Smaller PCBs, cables and connectors also result in a much more ergonomic, user-friendly system.

More information about LVDS and BUSLVDS can be found in [16].

Chapter 4: Calorimeter-SPD

Chapter 4. Calorimeter – SPD

4.1. Calorimeter

As it is described at Chapter 2, the Calorimeter system performs several functions. It selects high transverse energy hadrons, electrons and photon candidates for the first trigger level, which provides a decision 4 microseconds after the interaction each 25ns. It provides the identification of electrons which is essential to flavor tagging through semileptonic decays.

The main purpose of the calorimeter system is the identification of hadrons, electrons and photons, and the measurement of their energies and positions. This information is the basis of the Level 0 trigger, and therefore has to be provided with sufficient selectivity in a very short time. The set of constraints resulting from this functionality defines the general structure and the main characteristics of the calorimeter system and its associated electronics [23]. The ultimate performance for hadron and electron identification will be obtained at the off line analysis level. The requirement of a good background rejection and reasonable efficiency for these channels adds demanding conditions on the detector performance in terms of resolution and shower separation [24].

The general structure is that of an electromagnetic calorimeter (ECAL) followed by a hadron calorimeter (HCAL). The most demanding identification is that of electrons. Within the bandwidth allocated to the electron trigger the electron Level 0 trigger is required to reject 99% of the inelastic pp interactions while providing an enrichment factor of at least 15 in B events. This is accomplished through the selection of electrons of large transverse energy E_T. The rejection of the high background of charged pions requires longitudinal segmentation of the electromagnetic shower detection, i.e. a preshower detector (PS) followed by the main section of the ECAL (25 X_0). The optimization of its thickness (2.5 X_0) results from a compromise between trigger performance and ultimate energy resolution [25]. The electron trigger must then reject the photons. This is reduced by the introduction, in front of the PS, of a scintillator pad detector (SPD) plane used to select charged particles. At Level 0, the background to the electron trigger will then be dominated

by photon conversions in the upstream spectrometer material, which cannot be identified at this stage. To obtain optimal energy resolution for high energy photons, the ECAL must be at least 25 X_0 thick, enough to contain them [26]. On the other hand, the trigger requirements on the HCAL resolution do not impose a stringent hadronic shower containment condition. Its thickness has therefore been set to 5.6 interaction lengths [27]. Figure 9 shows a view of the Calorimeter.

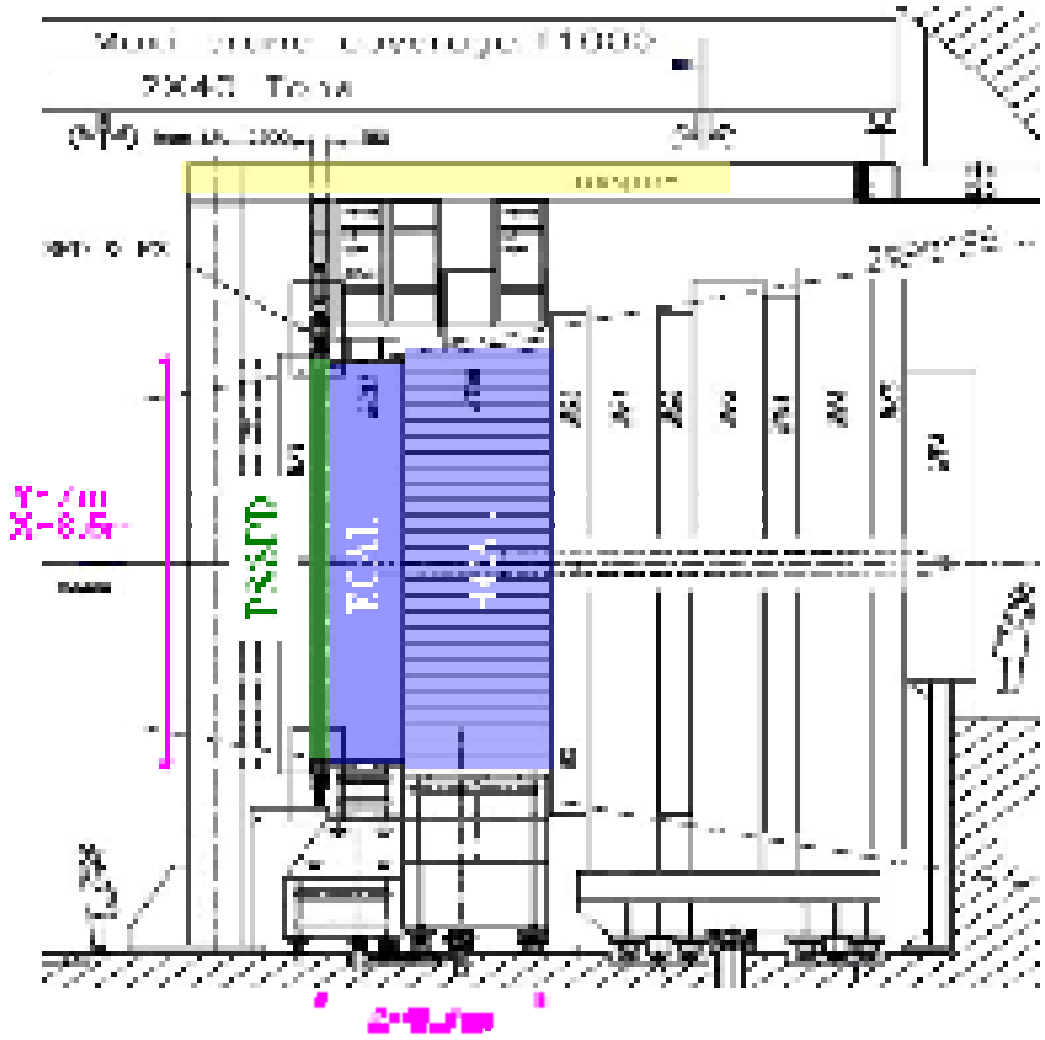

Figure 9. View of the Calorimeter

The PS/SPD, ECAL and HCAL adopt a variable lateral segmentation since the hit density varies by two orders of magnitude over the calorimeter surface. Segmentation in three different sections has been chosen for the ECAL and

protectively for the SPD/PS. Given the dimensions of the hadronic showers, the HCAL is segmented into two zones with larger cell sizes.

From the point of view of electronics, all calorimeters follow the same basic principle: scintillation light is transmitted to a PMT by WLS fibbers. The single fibbers for the SPD/PS cells are read out using multi-anode photomultiplier tubes (MAPMT), while the fibber bunches in the ECAL and HCAL modules require individual phototubes. In order to have a constant E_T scale the gain in the ECAL and HCAL phototubes is set in inverse proportion to their distance from the beam pipe. Since the light yield delivered by the HCAL module is a factor 30 less than that of the ECAL, the HCAL tubes operate at higher gain.

The basic structure is dictated by the need to handle the data for the Level 0 trigger as fast as possible. The front-end electronics and the PS/SPD photomultipliers are located at the detector periphery. The HCAL and ECAL phototubes are housed directly on the detector modules. The signals are shaped directly on the back of the photomultiplier for the PS/SPD or after 12 m and 16 m long cables for ECAL and HCAL respectively. They are then digitized in crates positioned on top of the detectors and the trigger circuits, hosted in the same crates, perform the clustering operations required by the trigger [28]. For each channel, the data, sampled at the bunch crossing rate of 40 MHz, are stored in a digital pipeline waiting for the Level 0 trigger decision. In order to exploit the intrinsic calorimeter resolution over the full dynamic range, ECAL and HCAL signals are digitized by a 12 bit flash ADC [29]. Ten bits are enough for the preshower, and the SPD information is only one bit, a simple discriminator recording whether a cell has been hit or not [30, 31]. The second requirement is to reduce the tails of signals associated to the bunch crossing preceding the one being sampled. For ECAL and HCAL, this goal can be achieved at the percent level by suitable signal treatment within 25 ns. In the case of the PS and SPD, the signal shape fluctuations require the longest possible signal integration time. Finally, in order not to degrade the resolution, the electronic noise must remain at the least significant bit level [32]. At the short shaping times being used, this requires careful design of the very front-end part.

4.2. SPD/PS Detector

The PS/SPD detector, consists of a 15 mm lead converter (2.5 X0) that is sandwiched between two almost identical planes of rectangular scintillator pads of high granularity with a total of 12032 detection channels (shown at figure 8 left). The sensitive area of the detector is 7.6 m wide and 6.2 m high. Due to the projectivity requirements, all dimensions of the SPD plane are smaller than those of the PS by ~0.45%. The detector planes are divided vertically into two halves. Each can slide independently on horizontal rails to the left and right side in order to allow service and maintenance work. The distance along the beam axis between the centre of the PS and the SPD scintillator planes is 56 mm. In order to achieve a one-to-one projective correspondence with the ECAL segmentation, each PS and SPD plane is subdivided into inner (3072 cells), middle (3584 cells) and outer (5376 cells) sections with approximately 4x4, 6x 6 and 12x12 cm2 cell dimensions.

The cells are packed in ~ 48 x48 cm2 boxes (detector units) that are joined into supermodules, shown at Figure 10.

Figure 10. Supermodules under construction

Each supermodule has a width of ~96 cm, a height of ~ 7.7 m and consists of detector units that form 2 rows and 13 columns. There are eight different supermodules per SPD and eight more for PS. The space available for the SPD/PS detector between the first muon chamber and the electromagnetic calorimeter is only

180 mm. This figure will affect directly on the design of the electronics. Figure 11 (right) shows an individual scintillator pad with the WLS fibber layout. The diameter of the WLS fibber groove is a few mm smaller than the tile size; exact parameters of the tile geometry can be found in [33]. The square structure of a pad is cut out from a 15 mm thick scintillator plate, and the scintillator surface is polished to reach the necessary optical quality. In order to maximize the light collection efficiency, WLS fibbers are coiled and placed into a ring groove that is milled in the body of the cell. The rectangular cross section of the groove is 4.1 mm deep and 1.1 mm wide. The groove contains 3.5 loops of WLS fibber. The number of loops was chosen to achieve an overall optimization of the light collection efficiency [34] and the duration of the time response [35]. Two additional grooves are milled in the scintillator allowing both ends of the WLS fibber to exit the plate. Light produced by an ionizing particle in the scintillator is guided by the WLS fibber to the exit of the detector box. At this point optical connectors (described in [33]) join the WLS fibbers to long clear fibbers. The two clear fibbers connected to the two ends of the WLS fibber of a given pad are viewed by a single MAPMT pixel [33]. The length of clear fibbers varies from 1.2 to 3.5m but all the fibbers connected to a particular PMT have the same length in accordance with the front-end electronics specification [30, 31]. The clear fibber allows the transport of the scintillator light from the SPD/PS planes over a few meters to the multi-anode PMT without significant attenuation.

The scintillator cells are grouped into self-supporting detector units that are packed inside square boxes with dimension 476 mm x 476 mm (SPD) and 478 mm x 478 mm (PS) boxes, yielding a total of 26 boxes per supermodule. Since there are three sections with different cell sizes for the SPD/PS planes, the boxes are filled with a different number of pads with sizes that add up to 119 mm for the SPD to 119.5 mm for the PS planes.

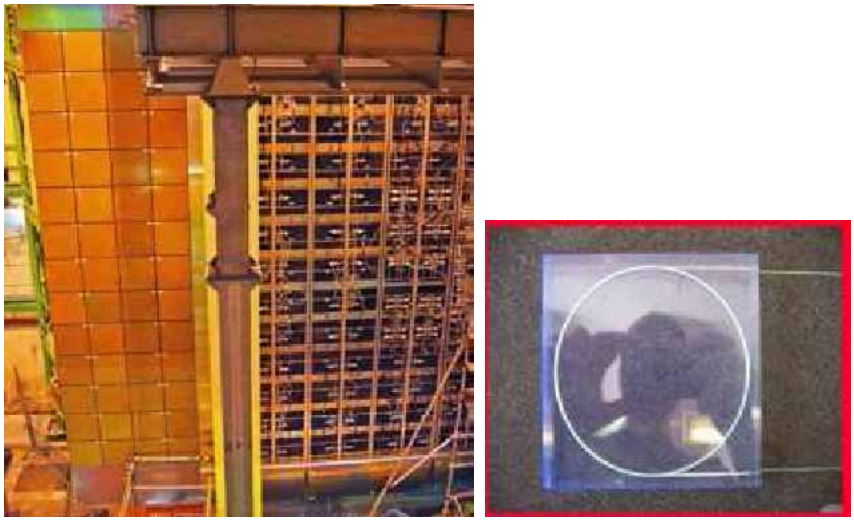

Figure 11. One half of the SPD/PS installed in the LHCb experimental hall (left). Individual scintillator pad (right)

Depending on the number of scintillator cells inside a unit, the boxes are equipped with one (outer region), four (middle region) or nine (inner region) output port(s) and light connector(s).

The detector units are designed to be mounted on a supermodule support plate. All supermodules of the SPD/PS planes have identical design. Each consists of 26 detector units mounted on a long aluminum strip in two columns. The photomultiplier tubes are located on both the top and bottom ends of the supermodule support outside the detector acceptance. The detector units are optically connected to the PMTs by bundles of 4x32 clear fibbers, enclosed in a light-tight plastic tube, by means of a photo-tube coupler.

The PMTs, described in point 4.4, are located inside boxes, at top and bottom of eight supermodules. Each supermodule contains two boxes, one in the top and one in the bottom. The detector is divided in two sides: C-Side and A-side. Figure 12 shows the final configuration for A-side. (C-side has a mirror-configuration).

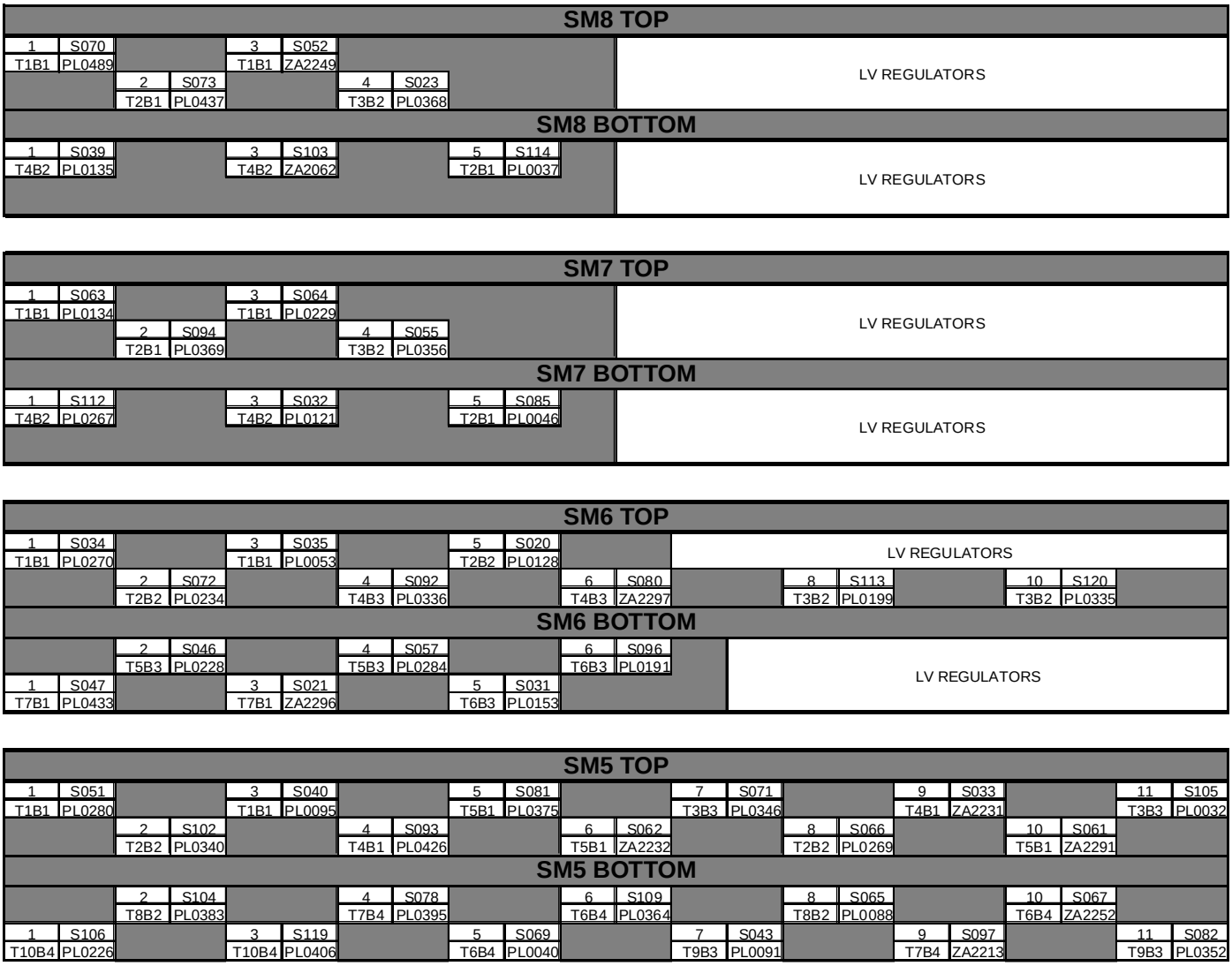

Figure 12. A-side configuration.

There are fifty VFE cards per side distributed in eight boxes, four boxes per bottom and four boxes per top. Each VFE card contains one PMT. The distribution inside boxes is not regular as the figure above depicts, this is a result of the distribution of the fibbers in order to have better granularity. Some boxes also contain LV Regulator Cards designed for feeding the VFE Cards.

The nomenclature of the Figure 12 is in Table 2:

Position of the card inside the box	Number of VFE Card
	Number of MAPMT

Table 2 Configuration inside boxes

The position of the cards inside the box are numbered from 1 to 11 and put in two rows. One row contains the odd numbers and the other one contains the even numbers.

The VFE Cards were numbered from S01 to S120, and the MAPMT were numbered by the reference number of the manufacturer.

The size of the boxes, around 96cmx70cmx12cm, and the position of the physical fibbers and the number of the cards, shown in next figure create important mechanical constraints to the VFE structure and also from the point of view of electronics this position implies several restrictions for the design. (See next pictures).

Figure 13. Left, view from the bottom of the detector. Right, view of a Box.

4.3. Photomultipliers -MAPMT

As it is explained in 4.2, the pad/preshower (SPD/PS) detector uses scintillator pad readout by wavelength-shifting (WLS) fibbers that are coupled to MAPMT via clear plastic fibbers. The choice of a 64 channel MAPMT allowed the design of a fast, multi-channel pad detector with an affordable cost per channel.

The PMT mentioned is a (8-stage) R5900-M64 manufactured by Hamamatsu [20, 35] and has a bialkali photocathode segmented into 64 pixels of 2 x 2 mm2.

The quality of the phototubes has been extensively studied using measurements of the nonuniformities of anode response within one MAPMT, the linearity over the required dynamic range of the PS, the absolute gain of the MAPMT channels and the electronics cross-talk. The nonuniformity of response within one MAPMT was found to be in a ratio of 1 to 2 (minimum to maximum) for most of the installed tubes. While the cross-talk between the PMT electronics channels has been measured to be negligible, a large amount of tubes shown a large cross-talk at the entrance. This has been one of the major rejection causes. The response linearity was found to be well within specification for all tested phototubes.

Specific measurements of the MAPMT behavior in the magnetic field were conducted as well. It has been discovered that these phototubes, primarily thought to be robust in a magnetic field were significantly sensitive to fields as weak as 10 Gauss. A dedicated magnetic shielding has been designed. A μ-metal cylinder (6 cm long with a 4 cm diameter) is used along the tube axis and the MAPMT (together with the VFE electronics) are hosted in a box made of soft iron. Special attention was given to evaluate the long term behavior of the phototubes subject to the conditions of the largest illumination of the PS (DC currents for the SPD are much smaller than for the PS [35]. At the initially foreseen working point of the PMT an unexpected spectacular exponential drop of the gain occurred after one month of illumination. The PMT gain was therefore divided by 10. As has been checked experimentally this does offer acceptable conditions of operation [42, 43].

4.4. Pulseshape characteristics

The main function of the SPD detector is distinguishing between charged and neutral particles; this distinction is done by comparing the energy deposited into the scintillator pads (Figure 14). Ideally only charged particles generate a relevant signal. However, high energy photons can create an electron through secondary processes such as Compton Effect or pair production. Applying a threshold of 1.4 MeV (~ 0.7 MIP) is the best way to reject photons with an acceptable efficiency for the trigger [17]. The resolution of the discriminator must be higher than 0.05 MIP in order to keep the energy resolution given by photostatistics in this threshold area.

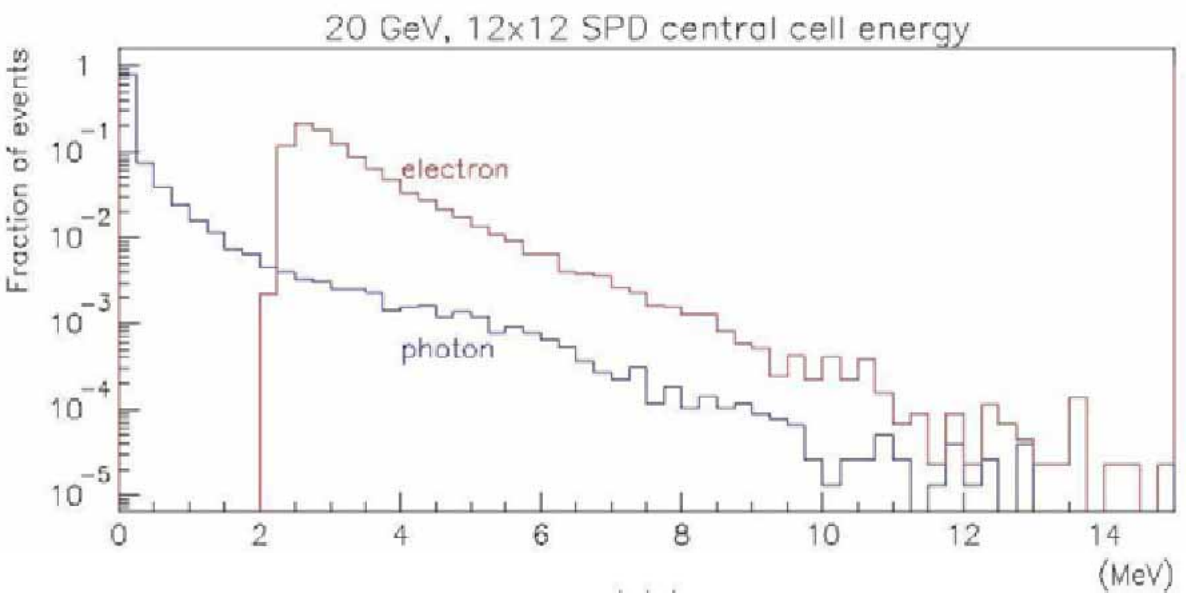

Figure 14. Deposited energy at central SPD cell.

The efficiency of the light collection system and the PMT photocathode leads to low photostatistics, around 15 photoelectrons. This efficiency also generates irregular pulse shapes, lasting longer than the bunch crossing period of 25 ns. The exponential behavior of the signal outing the PMTs makes no dead time between two consecutive bunch crossings (See Figure 15). Cosmic ray studies and simulations recommend the integration of the total charge of the signal and performing pile up[5] correction [20]. Besides, the PMT gain is limited by the maximum average current that can be used

[5] *Pile up correction: subtracting the signal fraction that belongs to the previous bunch crossing*

to avoid fast aging. For cells with a higher occupancy the MIP signal will be cut down to 100fC. Active bases shall be used to keep acceptable gains at low high voltage.

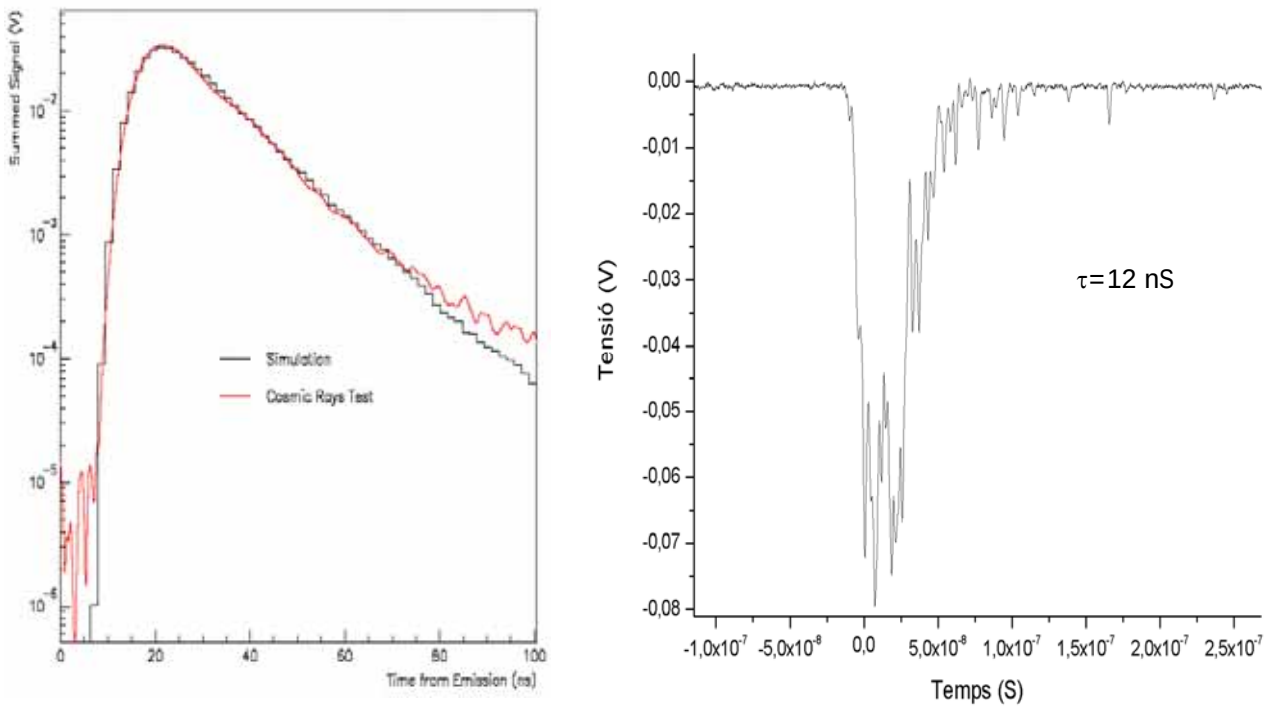

Figure 15. Typical MIP signal shape: (left) average and (right) single event.

4.5. L0 Calorimeter Triggers

The Calorimeter Triggers looks for high E_T particles: electrons, photons, p0 or hadrons. It forms clusters by adding the E_T of 2x2 cells and selecting the clusters with the largest E_T. Clusters are identified as electron, photons or hadron based on the information from the SPD, PS, ECAL and HCAL Calorimeter. The E_T of all HCAL cells is summed to reject crossings without visible interactions and to reject triggers on muon from the halo. The total number of SPD cells with a hit is counted to provide a measure of the charged track multiplicity[6] in the crossing.

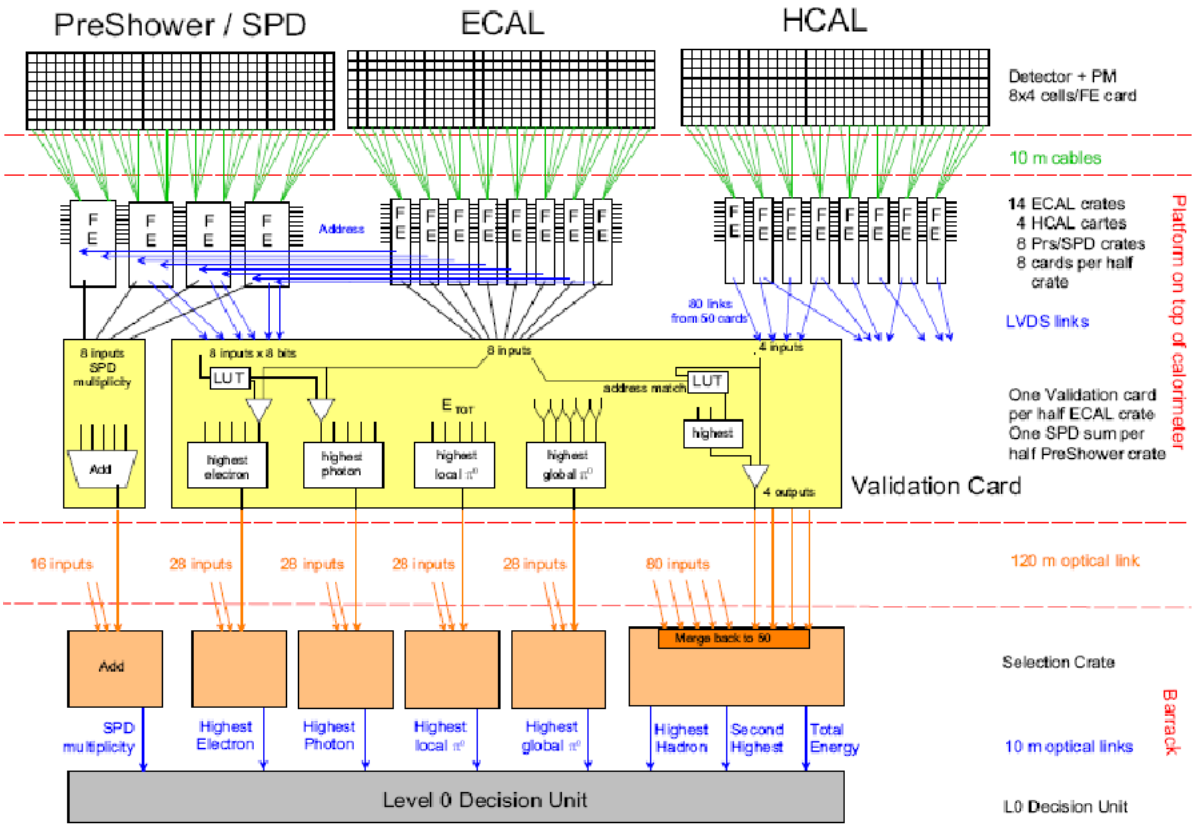

Figure 16. Architecture of Calorimeter Triggers

This zone of 2 by 2 cells is used, large enough to contain most of the energy, and small enough to avoid overlap between various particles. Only the particle with the highest E_T is looked at. Therefore at each stage only the highest E_T candidate is kept, to minimize the number of candidates to process.

[6] *This multiplicity is used to discard events.*

These candidates are provided by a three step selection system as shown in Figure 16:

- A first selection of high E_T deposits is performed on the Front-End card, which is the same for ECAL and HCAL. Each card handles 32 cells, and the highest ET sum over the 32 sums of 2x2 cells is selected. To compute these 32 sums, access to cells in other cards is an important issue.
- The Validation Card merges the ECAL with the PS and SPD information, prepared by the Preshower front-end card. It identifies the type of electromagnetic candidate, electron, photon and p0. Only one candidate per type is selected and sent to the next stage. The same card also adds the energy deposited in ECAL in front of the hadron candidates. A similar card computes the SPD multiplicity in the PreShower crates.
- The Selection Crate selects the candidate with the highest ET for each type; it also produces a measure of the total ET in HCAL and the total SPD multiplicity.

4.6. Readout Electronics

As the structure of the detector described in 4.2, functional design of the SPD readout is split into a Very Front End board, hosting the PMT, a Regulator Card which feeds the Very Front End Units sitting at the boxes located in the supermodules and a Control Card, sitting at the calorimeter front end crates[7], as depicted in Figure 17. An overview of SPD subsystem and its main connections is given in this figure.

The FEBs have two different data paths: the trigger one and the readout one. The outputs of these boards are connected to the standardized custom backplane, sending signals using LVDS levels to the Calorimeter Readout Controller (CROC) for the readout data path and to the Validation boards for the trigger data path.

The CROC performs the event formatting after the first trigger level. Data is then sent to the DAQ through optical links. The CROC also receives the Experiment Control System (ECS) implemented under SPECS protocol [37] and the 40 MHz bunch crossing clock, trigger and synchronous commands from the LHCb Timing and Fast Control system (TFC), and there from distribute them over the whole crate.

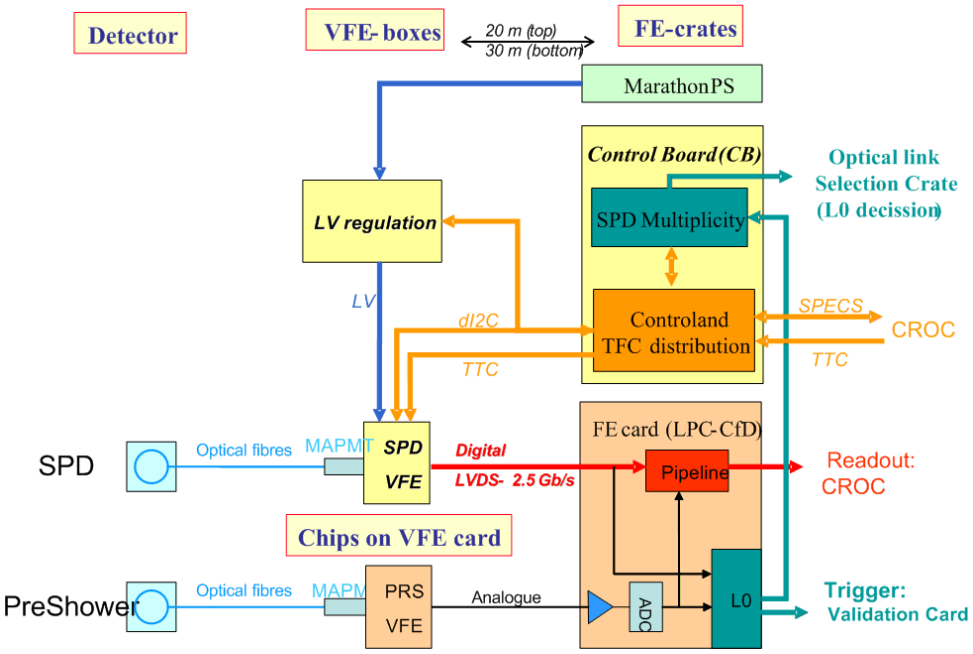

Figure 17. Block diagram of the SPD front-end elements.

[7] *Front End Crates: situated at top of the experiment, above the supermodules*

4.6.1. PS/SPD FE Board

The PS/SPD board handles 64 preshower data channels for raw data, read-out and trigger purpose, and 64 SPD single bit trigger channels. The PS raw data dynamic range corresponds to 10 bits, coding energy from 0.1 MIP (1 ADC count) to 100 MIPS. A general overview of the board is given in Figure 18.

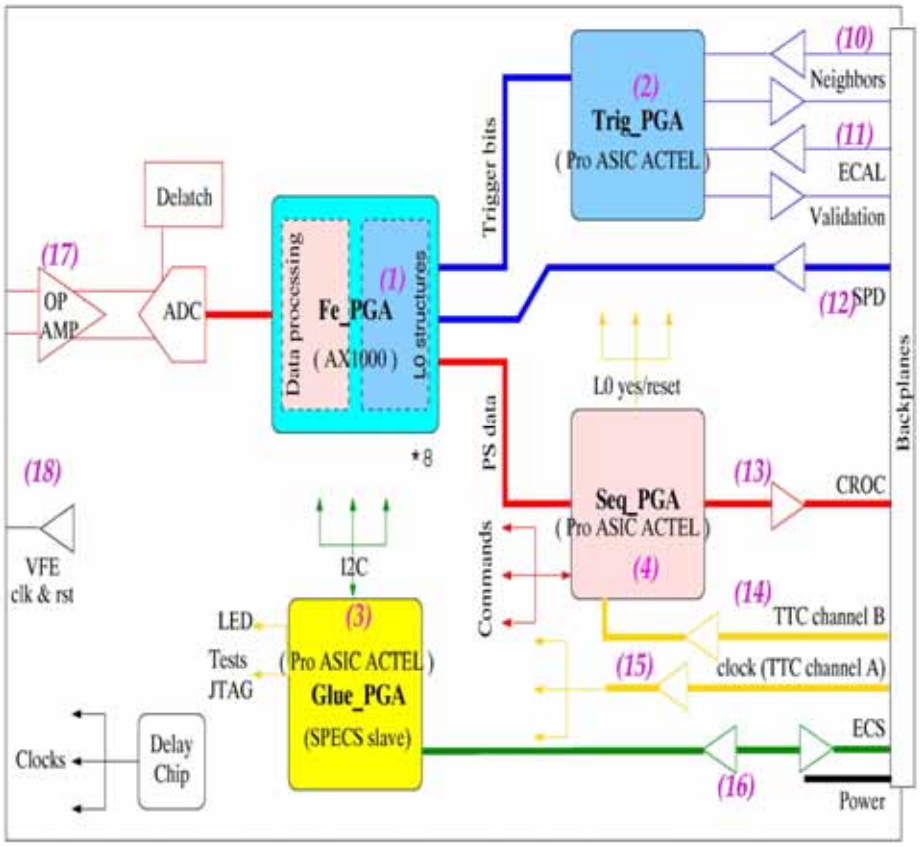

Figure 18. Block diagram of the PS/SPD FE Board.

Its general architecture contains five major components:

- An analog block receiving the 64 analog PS channels from the VFE part and digitizing them. Each channel is composed of a fully differential operational amplifier followed by a 10-bit 40 MHz differential ADC. A synchronization signal (clock and reset) is sent to the VFE.
- A processing block made of 8 identical FE PGAs. Each of them is in charge of processing 8 PS channels. After applying corrections for pedestal subtraction,

gain adjustment and pileup, the 10-bit data are coded into an 8-bit floating format. A trigger bit is produced for each channel by applying a threshold on the corrected data. Eight SPD channels are also received. Two PS and SPD channels are packed together, stored and retrieved after L0. Two blocks of memory per two channels are used in each FE PGA for the level-0 pipeline and de-randomizer. The processing block is very resource consuming. Since the VFE comprises two interleaved integrators working in alternance, the gain and offset corrections have to be applied differently for two consecutive events leading to two effective sub-channels per physical channel. Also the data inputs, 8 SPD channels of 1 bit and 8 PS channels of 10 bits are important. Consequently, the FE PGA chosen was the AX1000 of the ACTEL anti-fuse technology.

- A trigger block made of one TRIG PGA. It handles the processing for the production of the L0 information. The block receives the address of each cell and its local maximum of transverse energy from the ECAL FEB. As the ECAL electronics is organized per 32 channel boards, each 64 channel PS/SPD FEB is seen by the system as two 32 channel half boards, each receiving its own request address. The TRIG PGA is an APA450 of the ACTEL ProASIC plus Flash based FPGA family.
- A SEQ PGA builds the data block after a L0-Yes signal, and sends it to the CROC. It also issues control and synchronization signals for the other 8 FE PGAs and the TRIG PGA.
- A SPECS slave called GLUE PGA handling all the I2C communication of the board. The last two blocks, SEQ PGA and GLUE PGA, are identical to the ones of the ECAL/HCAL FE electronics and are described in reference [31].

4.6.2. *PS VFE Board*

The solution adopted for the PS is to alternate every 25 ns between two integrators and to reset one integrator when the other one is active such as in SPD. The signal is sampled by track-and-hold circuits and the output of the active integrator is chosen by a multiplexer, followed by a twisted-pair cable driver. All circuit elements are functioning in differential mode to improve stability and pickup-noise rejection. The circuit design is shown in next figure and detailed in [44].

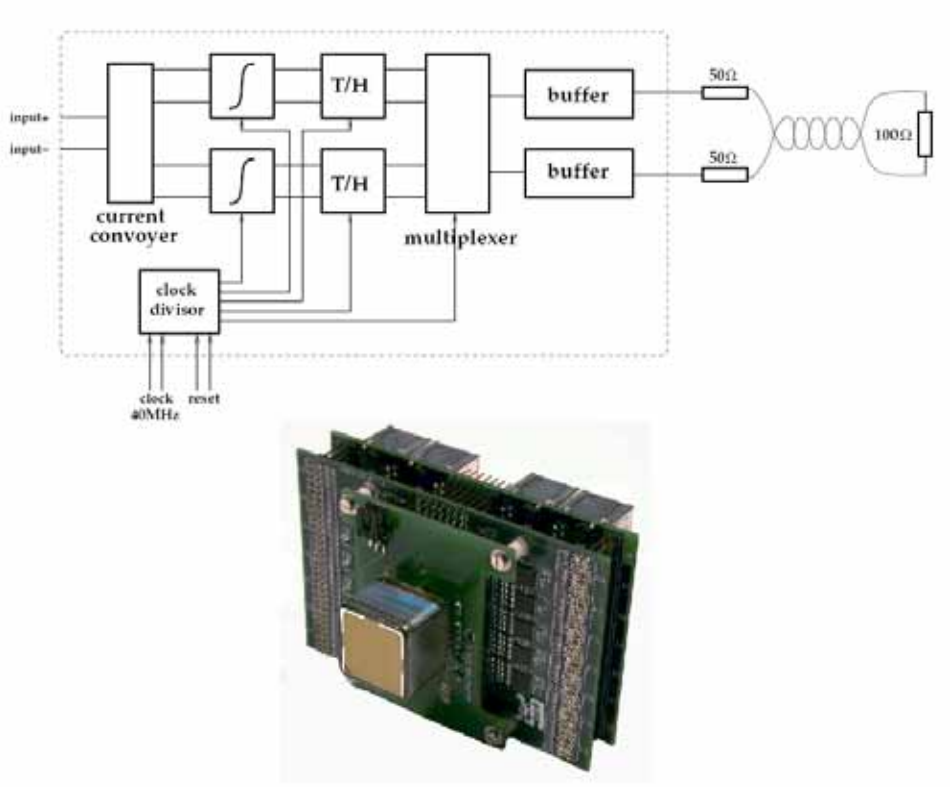

Figure 19. PS VFE picture at Bottom. Diagram Block of the PS ASIC at Top

The phasing of the clock with respect to the signal determines the start of the integration. Since the length of the 64 fibbers connected to a given PM is identical and the delay inside the PM is identical within a fraction of one ns, it is sufficient to have one clock adjustment per phototube. The amplifier integrator circuit is realized in monolithic AMS 0.8 μm BICMOS technology with 4 channels implemented per chip. The dynamic range is one Volt with a noise of 1 mV. Sixteen chips are grouped in a card on each phototube. The outputs of each chip (4 channels) are sent through

27 m long Ethernet cables from Kerpen Company with RJ45 connectors to the ADC placed in the FE Board. Two clock and two reset signals delivered by the corresponding FE Board are received by the VFE Board through a cable of the same type as those used for the signal.

4.6.3. *Control Board*

The CB is an 8 layers 9U card. It has two main functionalities: the trigger functionality and the control functionality. Figure 20 shows the block diagram of the CB.

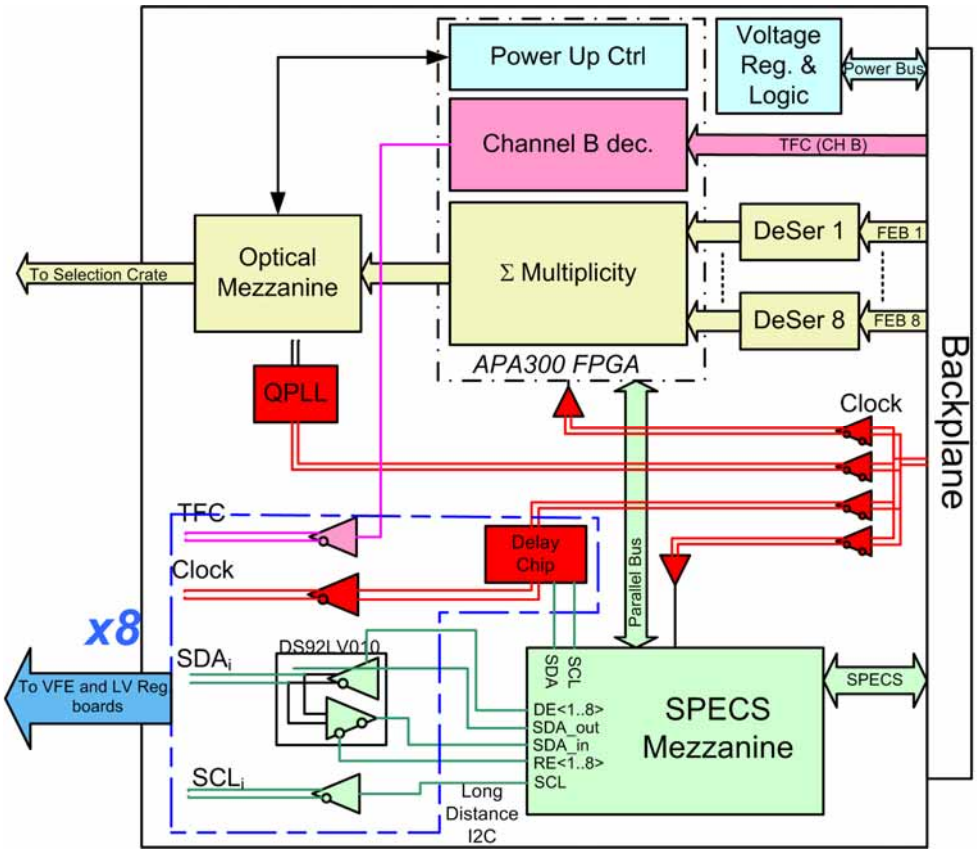

Figure 20. Block diagram of the CB

The former functionality consists on receiving and deserializing (DS90CR216) the multiplicity data from up to 8 different PS/SPD FEBs trough LVDS serialized point to point backplane links, adding these numbers and transmitting the information to the barrack through an optical link.

The later consists on providing ECS and TFC interface for up to 8 elements, either a VFE board or a LV regulation board. The communication between the CB and the VFE element is through SSTP Ethernet cables using shielded RJ45 connectors. Therefore, up to 4 pairs are available: 1 for the 40 MHz clock, 1 for the TFC (Fast

Time Control) signal and 2 for the ECS interface, a differential long distance I2C interface.

The SPECS slave is implemented trough a SPECS mezzanine card which is an LHCb standard ECS interface. The SPECS mezzanine provides a standard local I2C bus and a long distance I2C bus. The long distance I2C bus is based on 3 unidirectional signals: SCL, SDA_in, and SDA_out. These signals must be buffered by drivers. For long distance communication, LVDS drivers seem to be the best choice.

The FPGA used for the multiplicity also decodes the channel B lines of the TFC system, where synchronous command such resets or calibration pulses are coded. The FPGA serializes a reduced set of commands, explained on Chapter 5, and send them to the VFE trough a dedicated pair in the control cable.

The remaining pair on the cable transmits the 40 MHz clock to the VFE after being delayed by a programmable clock distribution ASIC to phase align the sampling of the analogue detector signals (integration start time is given by the edges 20 MHz clock) to the bunch crossings. This chip generates 4 differential outputs and each of them can introduce a maximum delay of 25ns to the clock, with independent steps of 1ns.

In addition to the trigger multiplicity and channel B decoding, the FPGA perform other tasks. On the hand, for testing and debugging purposes, the multiplicity data can be spied at the output of the optical mezzanine, when a proper type calibration trigger is send through the channel B data is written in a spy RAM

4.6.4. *LV Regulation Board*

LV regulation cards, based on CERN-ST Radiation Hard voltage regulators, will be installed in the VFE boxes. The VFE card requires many different supply voltages as reported in Chapter 5, making necessary the use of several regulators per card (such as +3.3V Analog, +3.3V Digital, +/-1.65V). In order to optimize the usage of the power regulator each regulator card will power up to 7 VFE cards. It results on a complex power distribution system, advising monitoring to be integrated in the same board. This is done using an FPGA which performs periodic analogue readouts of voltages and currents. LV card also performs temperature measurements using onboard probes and probes embedded in VFE cards. A block diagram of the board is shown in Figure 21.

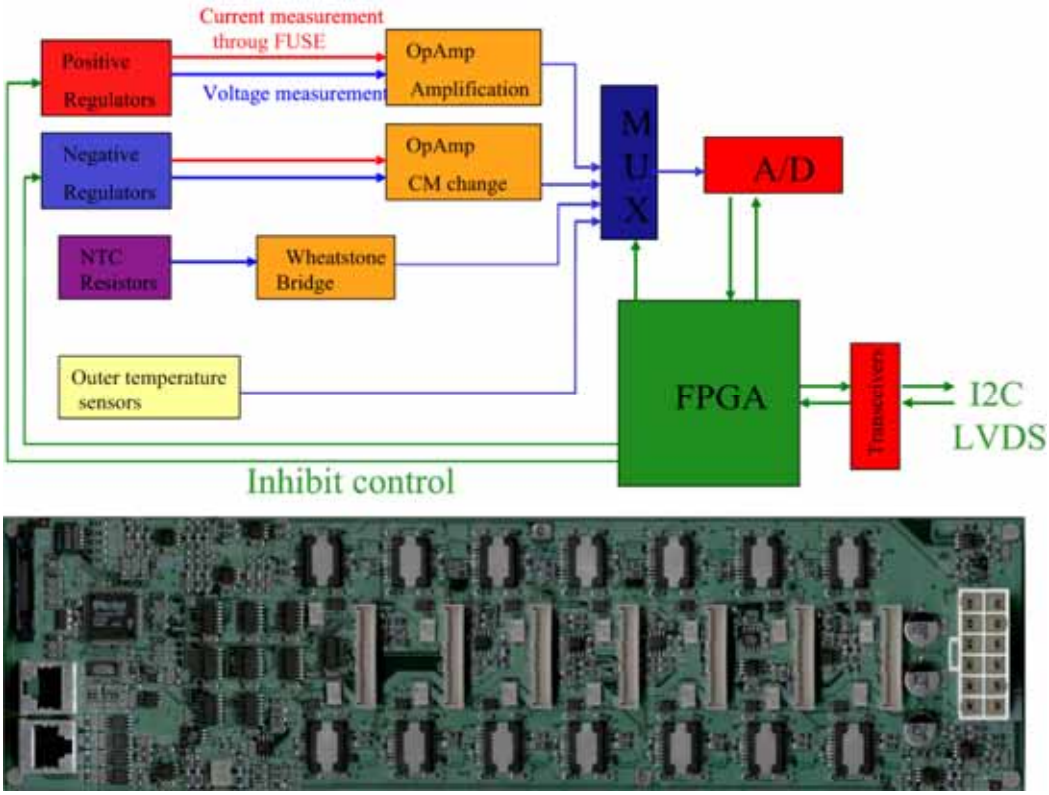

Figure 21. Block diagram and top view of the LV regulation board.

4.6.5. *VFE Units*

The signal of the scintillator pads is processed in a Very Front End unit, as depicted in next figure. This unit includes the photomultiplier described in the 4.4, [19], [20]. This PMT is in charge of converting the light pulse into charge.

As a result of the signal outing of the photomultiplier, the unit contains a full custom design to perform the discrimination between electrons from photons, a clock buffering network, a Control Unit is used to program the thresholds levels of the discrimination and program the level of the pile-up correction. This control unit also makes the mapping and monitories the possible influence of the radiation, such as latchups. The control Unit is implemented through a programmable FPGA.

LVDS serializers are used to send the information to the PS Front End card minimizing the number of cables.

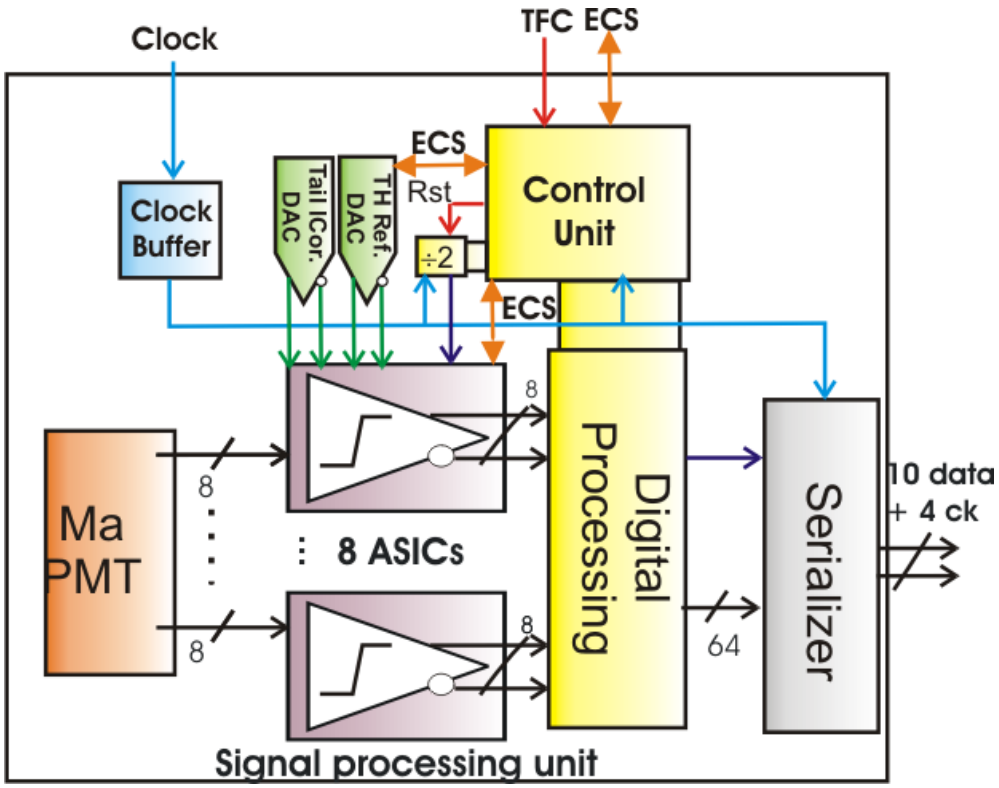

Figure 22. Block diagram VFE Unit.

Signal Processing

The PMT signal is amplified, shaped and discriminated through an 8 channel ASIC [21]. Figure 23 shows the functional architecture of each channel. The configuration is based on two interleaved processing units per channel to avoid any dead time and to be able to perform the pile-up compensation. The bunch-crossing clock is divided (outside the chip) and then used to multiplex by level the two paths of the channel each 25 ns. To prevent digital crosstalks on sensitive analogue parts, the latter are fully differential. The AMS BiCMOS 0.8 µm technology was chosen in order to take benefit from the advantages of bipolar transistors for high transconductance (for a given bias current) and low offset stages and of CMOS transistors for digital blocks and analogue switches.

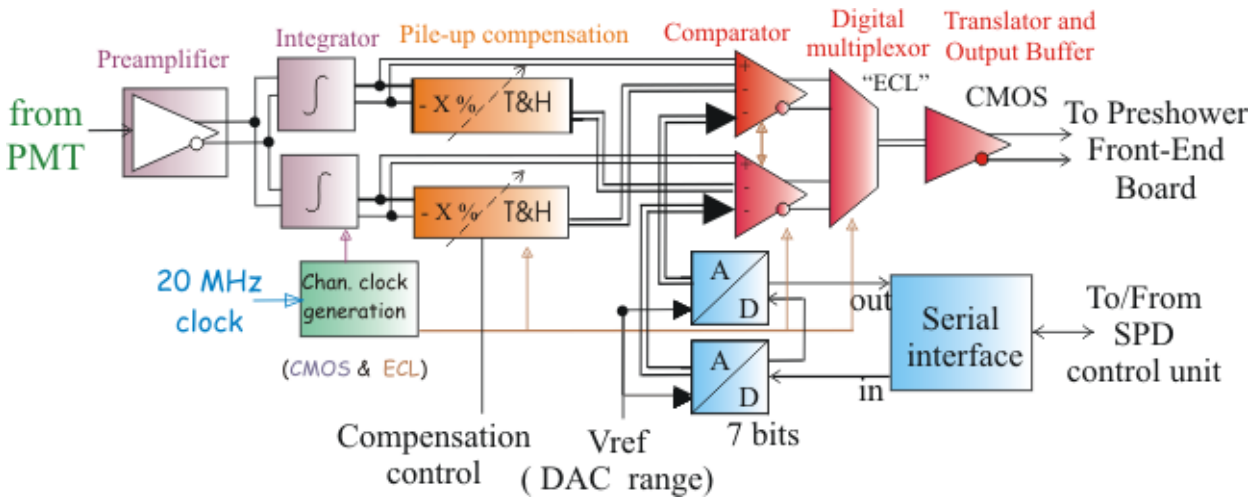

Figure 23. Functional diagram of a discriminator channel.

The PMT signal is single ended; it is preamplified and converted to differential by the first block of the discriminator. The signal is rather unpredictable due to low photo-statistics (about 15 phe/MIP) and it spreads over more than one clock period of 25 ns (decay time of WLS fibber is about 10 ns); to measure the energy deposition it is integrated. While one integrator is reset the other performs the integration and its output is continuously corrected and compared with a programmed threshold. The comparison is latched just before the end of the integration period. The pile-up

compensation system takes a fraction of the integrator output at this time (ideally the fraction that would appear in the next period) and stores it on a track and hold circuit. The fraction to subtract is tunable through an analogue signal to be able to correct differences in the time response coming from differences in cell sizes, fibber lengths or radiation doses. The comparison stage continuously subtracts from the integrator output the value stored in pile-up compensation block of the other path (that corresponds to the previous sample) and the threshold value set by a 7 bits DAC. Each path uses an independent DAC to be able to compensate the offsets due to process variations between different subchannels.

The voltage supply is fixed to 3.3 V, to minimize power dissipation. The required differential signal range for the analogue processing after integration is ±1V. The gain of the system is such a Minimum Ionizing Particle (MIP) signal will be equivalent to 100-200 mV depending on the gain of the PMT.

Techniques were applied to improve the radiation tolerance. Digital block is full-custom, with guard rings with to prevent latch ups and to protect against noise and cumulative effects, we use NAND gates wherever possible instead of NOR gates to be less sensitive to accumulative effects, and a Triple Voting Register (TVR) was used to minimize the SEU effects. Guard rings are also present in analogue blocks, especially for MOS transistors.

An engineering run was shared with other calorimeter chips to produce about 2000 units, 1300 have been packaged on an EDAQUAD QFP64 package and tested obtaining a yield of the 80 %.

In order to obtain these results, five runs of the ASIC were necessary.

RUN1 (Sep 2000)

This first run was used to test all the blocks per separate, and also was implemented one full channel from all the separate blocks. The tests show that the blocks designed work properly.

RUN2 (Jun 2001)

In the second run 4 full channels were implemented. In this run, the most important part were decided the kind of output that will be used between ECL vs.

CMOS. The performance of the outputs shows that the standard of CMOS was sufficient for the requirements.

RUN3 (Jan 2002)

Prior to this run, the pile-up correction was proved, and then in this case a new tunable substractor was implemented as well as of the on-chip DAC to program the thresholds and one full channel with digital control. The digital control was required in order to accomplish the requirement of the writable and readable registers to control the latchup.

RUN4 (Sep 2002)

The fourth run was used to test one complete channel (digital and analog), to test all the blocks per separate plus digital control. All this design was powered at 3.3V in order to reduce power consumption, showing the good performance at these voltage levels.

RUN5 (March 2003)

The fifth and the last run implemented with the eight full channels powered at 3.3V.

This full custom ASIC was designed by ECM's group.

Long distance LVDS serialized transmission

The 64 channels and the 20 MHz clock (the last for calibration purposes) are sent to the PS/SPD FEBs. The serializing factor in DS90CR215 chip is 7; thus 4 serializers are needed. Since each serializer has 3 data pairs and 1 clock pair, using standard shielded twisted pair (SSTP) LAN cables seems an economic solution.

Unfortunately, the skew margin of the serializing chipset is only of about 500ps, and the skew of commercial cables is higher than 2ns even for 30m long category 7 Ethernet cables. However, we observed that the skew between consecutive 30m cuts of the same pair is very low, usually lower than 500 ps. Taking benefit from the fact that 4 serializers and 4 cables of 4 pairs are needed, we designed a link with a custom board (see next figure) implementing a cross-connection scheme to send each pairs

corresponding to a given serializer through a different cable but through the same pair.

Since serializer has no pre-emphasis circuit[8], a passive (inductor in series with a resistor) pole-zero networks has been incorporated at the output of serializer to equalize the cable response. With a resistor of 150 Ω and an inductor of 1.5 μH an eye opening of 1.44 ns between LVDS thresholds (±100 mV) has been measured (see Chapter 6).

Figure 24. Cable Adaptation

A small board (see previous figure) is designed for soldering 14 twisted pair cables (10 for LVDS data + 4 clock for each serializer), for including this passive equalization network (tuned according the cable length) and for mounting a 2mm HM right angle female connector in VFE and FE ends.

Cooling System

The power dissipation of the card and the result of being house inside metallic boxes showed that the system could not work properly for a long time for the temperature achieved in some components during the use. Likewise, the maximum

[8] *The DS90CR494 64-channel LVDS multiplexer has pre-emphasis and was the first design option, but was found to be prone to SEL*

temperature of some components was exceeded. This fact forces the use of a cooling system.

The cooling is done by a cool water circuit around the boards. A conductive heating material is put on the cards, see Figure 25, and is in contact with an aluminium platform, which contains the circulating water.

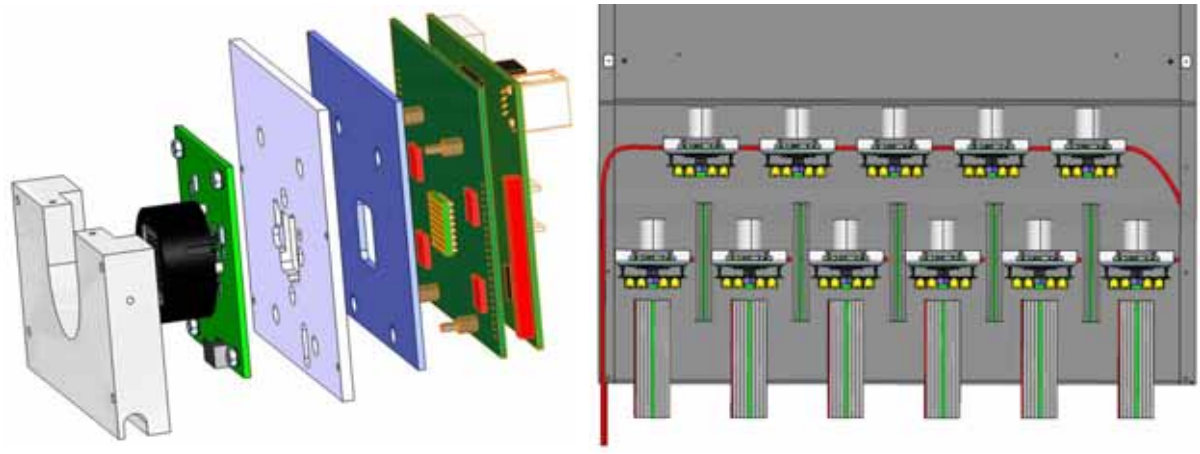

Figure 25. Left, Card. Right, cooling system inside boxes

This cooling system was designed by the Mechanics department of the Laboratoire Physique Corpusculaire of Clermont-Ferrand.

PMT Base Board

The MAPMT needs an active base, as it is explained some points above, and then a card containing it is needed. This board is the same as PMT Base Board of Pre-Shower [17], and it was provided by PS group. This fact implies some constraints for the design: the size of the card must accomplish the holes for the screw subjection and the ground connection. Next figure shows its size.

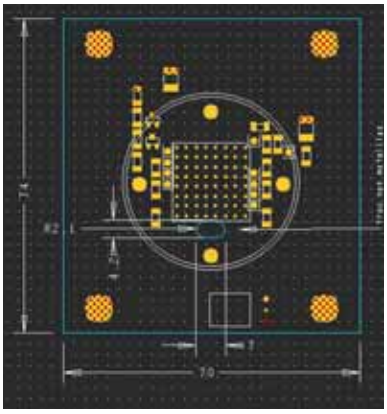

Figure 26. View of the measures of Base Board.

4.7. Grounding and Shielding

4.7.1. Grounding

The calorimeter ground configuration is a heavily interconnected ground network (mesh structure) as recommended in LHCb specification. The electronics of the calorimeter is distributed in many different locations, as it explained: the front end racks, the PS VFE and the SPD VFE. Although differential signals have been used wherever possible there are two delicate points that can not be avoided and lead us to think that a good ground from DC to hundreds of MHz is needed:

- The input stage of the ASICs is DC coupled to the PMT and it is a single ended signal by definition. Thus, ground parasitic currents should be minimized. This goal should be achieved with a mesh structure with very low impedance from DC to few hundreds of MHz.
- The SPD VFE to PS FE card connection is a 280 Mbits/s LVDS sensitive to attenuation and potentially sensitive to common mode differences.

Therefore all the mechanical structures should be properly interconnected and grounded as shown. The metallic structure of the detector is used to handle a very good ground between MaPMT, VFE boards and regulators.

In Figure 27 there is shown all the electrical connections between the SPD VFE elements (MaPMT readout units and regulator cards) and the FE racks, with

exception of the Low Voltage Power Supply ones. The low voltage supply connections include an independent conductor for ground connection apart from the neutral cables (those for power return connected to the floating Power Supplies).

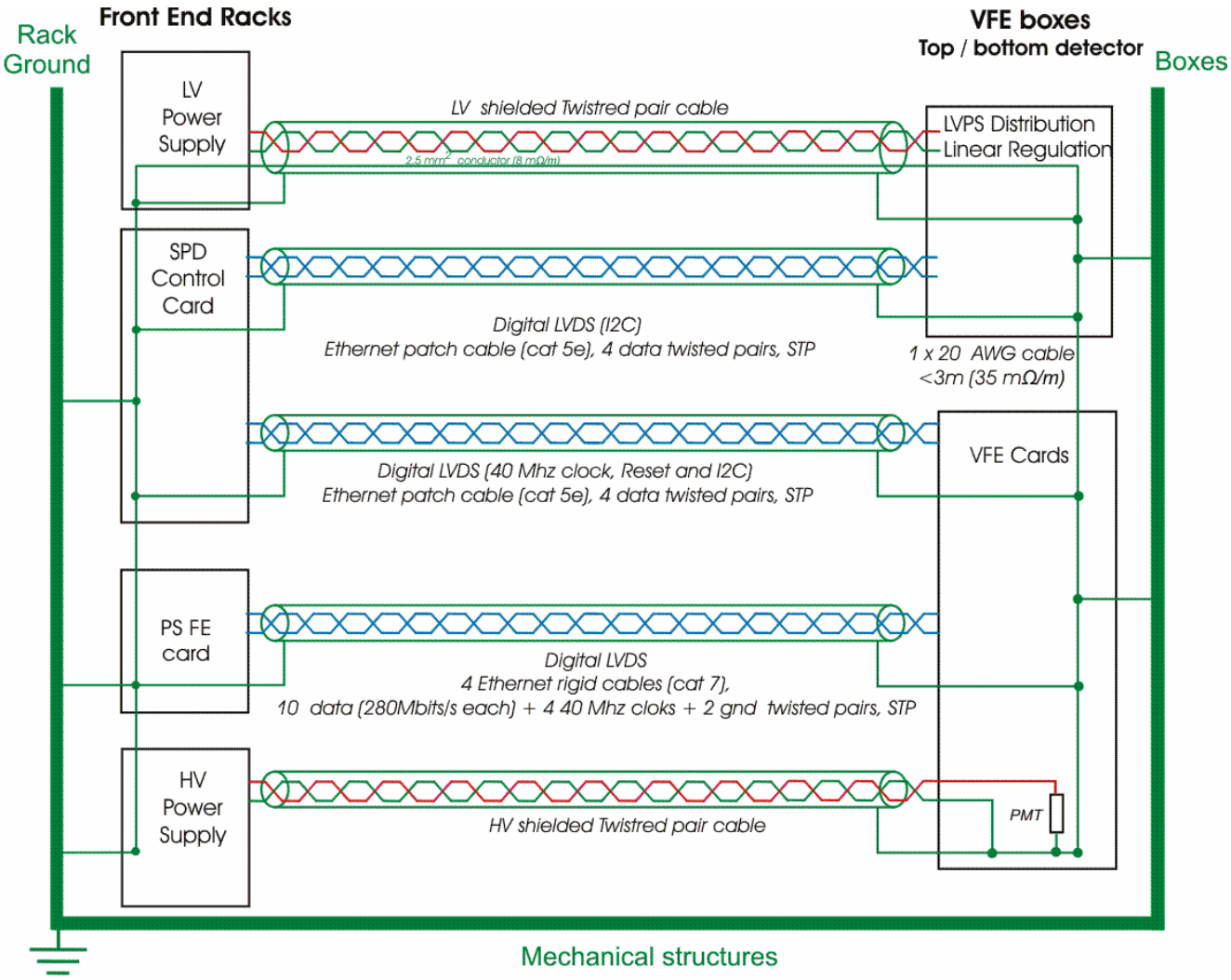

Figure 27. Scheme of the grounding of the SPD

Shielded twisted pair cables are use for the high voltage power supply connections and also for the low voltage ones. It is not foreseen a specific power filtering for the low voltage connection, the use of local regulation (inside the Faraday cage) is considered to be safe enough for the moment. Power filtering is put for the HV in the PMT baseboard (PS/SPD common).

4.7.2. Electromagnetic Compatibility

The metallic box that houses VFE units and regulator´s card should act as a Faraday Cage. The MAPMT/VFE boxes material is iron and thickness 5 mm.

A potential source of significant inductive noise in the LHCb environment is the coils of the main spectrometer magnet. The main victims of this interference in SPD VFE could be:

- The MaPMT. The metallic box plus a special μ-metal shielding around PMT protect the PMT (together with the 5mm iron box)
- The inductors used for cable equalization of the LVDS serialized link between VFE units and the FE of the PS. Special test have done at Orsay, showing effects smaller than a few % on the inductance value up to 400 gauss in the worst orientation.

Electromagnetic compatibility has been taken into account at the early design stage both for the ASIC and board designs. Sensitive analogue circuits are differential to reject common-mode noise as much as possible. Digital and analogue supplies are separated (even inside the ASIC). Decoupling is done as close as possible to the package, for the ASIC each channel has on-chip decoupling capacitors (100 pF) and guard rings are distributed between analogue and digital parts of the chip minimize substrate noise. Digital signals between cards are transmitted in LVDS. For the PCBs, planes for supply voltages and for ground are paired, making the effect of copper plane distributed capacitor.

Chapter 5: VFE Electronics Solution

Chapter 5. VFE Electronics Solution

This Chapter is focused in the VFE solution: Its requirements, its possible implementations and the solutions adopted. It is also explained the history of the card: from the first prototype to the final design.

5.1. VFE Requirements

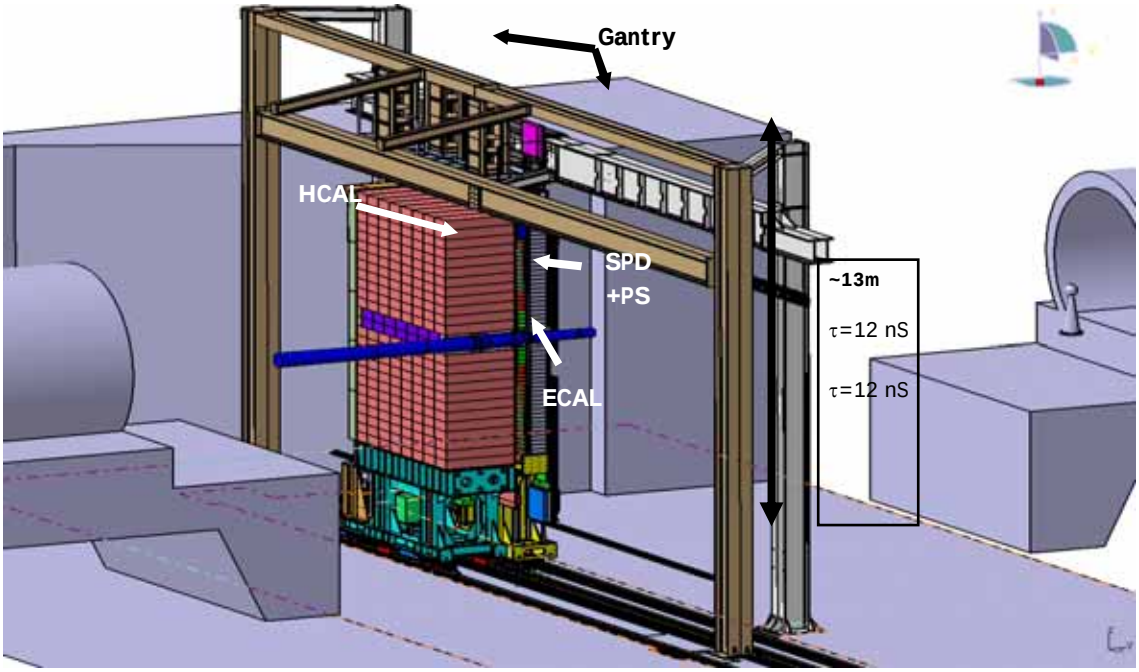

Figure 28. View of the Calorimeter

In the previous Chapters, the constraints for the design are explained. We can enumerate the most important ones:

- From the point of view of the Mechanics
- From the point of view of the Electronics
- From the point of view of Radiation

As it can be assumed, these requirements have been continuously evolving since its first definition at 1998, which had implied several prototypes and several changes

in the electronics design. The functional solution is explained in point 5.2 depicting the selected solutions for the whole constraints that there are just enumerated below.

The evolution is explained in points 5.3, and 5.5. The former is about the prototype history, which explains the several prototypes designed during these years and its tests and achievements; the later depicts the final prototype, its blocks, its functionalities, its components.

5.1.1. Mechanics requirements

From the point of view of mechanics there are several constraints to take into account:

- The space available for the electronics: As it is explained in the Chapter 4, on one hand, the VFE electronics is housed in boxes (sized 96x70x12) at the top and in the bottom of the supermodules; on the other hand, the distribution of the cells in order to obtain better granularity near the beam implies that the number of VFE Units per box is not uniform (as it is depicted in figure 12, there are four boxes containing 11 VFE Units). These two factors force the maximum size of the Units around 10cmx10cm.
- The cooling system is around the cards: some space must be left for the tubes and also the temperature on the system must be monitorized in order to solve some possible problems such as cooling malfunction or a current excess for any electronic problem.
- The position of the fibbers arriving to the boxes forced that the MAPMT has to be in a certain position in the VFE Unit, and also that the VFE Unit can only have one orientation in each box.. The Figure 29 shows it: the left plot depicted half SPD, with boxes at top and bottom. The clear fibbers at bottom arrive from the top part of the box, and the other way round at top. The right plot shows the detail of a box situated at top. It can be distinguished that the MAPMT are situated in bottom part of the card, and the cables output are in the top part.

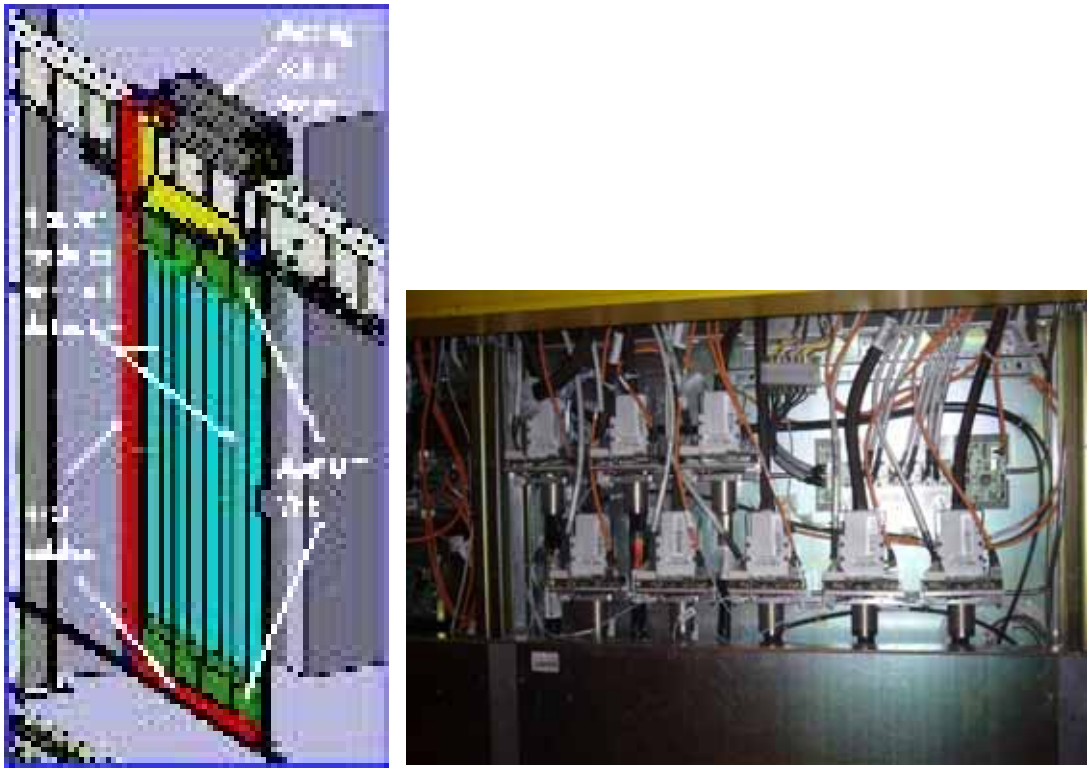

Figure 29. Left, half SPD. Right, top box detail.

- The position of the boxes: at top and bottom of the supermodules. The output information of the VFE Units must go to PS FEB; this implies a link up to 27m distance in the worst case.
- The design of the active base for the MAPMT is explained in the final design point. This card is designed also by the PS group, and its mechanics and subjection has to be taken into account.
- The mapping of the channels: As it is explained in last Chapter, the SPD is divided in two mirrored halfs (A/C side, top and bottom) around the beam and the cells are distributed in function of a better granularity. Of course, each of these channels corresponds to one of the PS channels (in the other part of the lead and therefore mirrored), and it must be something that makes the correspondence between them in order to process the information: the mapping.

5.1.2. Electronics requirements

From the point of view of electronics there are also several constraints to take into account:

- The analogue and small range signal outing the PMT.
- The requirements of the ASIC: The analogue input to fix the range of the thresholds, the analogue input to fix the amount of the pile-up subtraction, the current need for each of these inputs, the digital bus in order to program the thresholds, the symmetric power supply (+/-1.65V) for the analogue block and for the digital block
- The communication with the Control Card: Intelligence is needed to deal with the I2C and its commands.
- The 40MHz bunch clock: The most critical signal. It is received in an LVDS differential pair from the Control Card and it must be divided (the ASIC has two subchannels working at 20MHz clock each one, explained in last Chapter), and the jitter as well as the shape must be controlled.
- The output of the VFE Unit: 64 outputs per card must be sent to FEB. (LVDS link)
- The power supplies required: The fact that the ASIC has a symmetric power forces an extra electronics to convert these outputs to a standard CMOS (3.3V) VFE Unit's outputs.

5.1.3. Radiation requirements

From the point of view of radiation: As the VFE Unit must deal with a radiation quote, even with some possible SEE[9], all the components used in the design must be radiation tolerant. Therefore, if the components are not qualified, they must be irradiated in order to achieve (or not) this qualification.

[9] *SEE: Single Even Effects, explained in Chapter 3*

5.2. VFE functional solution

5.2.1. Electronics functional solution

From the point of view of electronics requirements, there are several critical points to decide: the ASIC requirements and the Intelligence (Control Unit as well as the division clock in the figure) required for the communication with the Control Card as well as the monitorizing of the VFE Unit.

The main ASIC requirements can be divided in two blocks: The analogue block and the digital block, as well as the power supply, explained later.

The digital block which consists on a serial programming interface must be done by the Control Unit (explained above).

The analogue block consists on the analogue signal required as reference for the on-chip DACs of the ASIC (threshold reference) and the analogue signal required as an amount of the pile-up subtraction.

These analogue signals are proportionate by two DACs monitorized and programmed by the Control Unit. As the current proportionate by the output of DACs was not enough to polarize the ASICs inputs, some OPs were needed to increase this current. A serial interface (I2C) with DACs was selected in order to minimize the number of pins required to command them.

The Control Unit and clock division: the Intelligence required must implement:

- It has to perform the division of the 40MHz clock for feeding the ASIC 20MHz clock
- It continuously must monitor SEUs in DACs or ASICs, and signal the errors in some way. It also should allow resetting the DACs (power cut-off) to recover from SEU hard errors in their I2C logic.
- It must provide interface with:
    - ECS system to access the registers corresponding to the ASIC on-chip DACs, the external DACs. According to global LHC requirements, any register can be read back from the ECS.

  - TFC system to provide a synchronous reset of the clock divider and synchronous RAM pattern injection.

- The digital processing consists on:
  - Mapping the PMT channel to given serializer channel to match the PS and SPD detector cell. There two different mappings due to different optical fibber orders. The right mapping according card position is selected through the ECS.
  - Injection of arbitrary patterns to test the detector data flow. Patterns are loaded into an injection RAM through the ECS. The generation of the pattern can be asynchronous or synchronous (TFC test command).

At first sight, the implementation of all of these functionalities could be made by two specific electronics:

- A typical solution with a microcontroller plus ROM plus RAM, commonly used in control applications environment.
- A specific solution made by an FPGA with state machines.

The first solution was rapidly refused as a result of the radiation environment. It was mandatory not to use a RAM-based solution, as a result of not passing the radiation qualification.

The second solution it was not good enough as it was expected. The only FPGAs that had the qualification of rad-tolerant were the antifuse ones. This kind of FPGAs was program-based in fuses; therefore, they were only one time programmable, and for prototyping they were not so useful.

It was decided not to implement the final FPGA until the final design, and in the previous prototypes a Flash-based FPGA could be used to make the tests in the easiest way.

At time to design this final prototype, the APA Flash-based family of Actel passed the qualification to radiation. Obviously, it was decided to use this family for the final FPGA. Of course, the design with this kind of FPGA must accomplish:

- Triple Voting Registers (TVRs) are used to minimize the SEU errors. This triple voting method consists in implement three identical paths (wherever is a critical data) to have a result and the final result is calculated as the majority of them.
- It has to monitorize SEU's in its own registers in order to signal these errors and giving the possibility to ECS for reading them.

More information on FPGA can be found in 5.2.2.

As it is described in the previous Chapter, each VFE unit contains 64 outputs. In order to minimize the number of cables it was decided to multiplex the output. As the distance between SPD-FEB was up to 27 meters, the design of the link was more complicated that it was expected at the beginning.

There are two main solutions for achieving this distance at high frequency: Optical fibber or LVDS link.

- The optical solution was not considered in the design.
- The LVDS link was easier to implement with some LVDS multiplexers available on COTs, but they must accomplish the radiation qualification and the transmission signal has to be tested.

Finally, the LVDS link was implemented with the serializer DS90CR215, with a 2mm hard metric connector and a custom cable, explained in LVDS transmission link. The tests on this link can be found on Chapter 6.

Another point to take into account is clock distribution. From the beginning of the design, the 40MHz clock as well as the 20MHz clock achieved by its division seems to be the most critical signals.

In the earliest prototypes, the shape of the clock in different points of the card (at this time there were only one card for each VFE Unit) denote degradation depending on the test point. Thus, it was decided to convert these signals to differential ones, avoiding white noise and interference, and reconverting to common mode signal as close as possible of the clock input (in case of inputs were not differential).

The 40MHz experiment clock arrives from Control Card by a differential pair in an LVDS range. It has to be converted in a common mode signal to feed the clock

input of the FPGA (and also it has to be converting in a symmetric power supply. The FPGA is powered by a symmetrical power supply to make easier the interface to ASICs). This clock also feeds the LVDS multiplexer, but in this case, the conversion is made as close as possible of the multiplexers.

The 20MHz input clock of the ASICs was prepared as a differential signal. The 20MHz clock output of the FPGA (the FPGA performs the clock division) is a common mode signal. Therefore, a conversion between common mode signal to LVDS signal is put as close as possible of the FPGA. The layout of this kind of signals will be explained later.

The last point for electronics requirements is the power supply. During the ASIC description is explained that the ASIC required a common CMOS power supply (3.3V), but a symmetric power supply: +1.65V/-1.65V, digital and analog. This is why the FPGA is also powered in an asymmetric way. It can be assumed that the interface with the Control Card or the interface with the PS FEB must be a standard CMOS (not symmetric): 3.3V/0V.

This fact will imply that, at some point, there must be a conversion between these levels (implemented by diodes, explained in the final design).

On the other hand, the number of power supplies given by the LV regulator card is considered (3.3V/0 digital, 3.3V/0 analogue, +1.65V/-1.65V digital, +1.65V/-1.65V analogue and 0.85V/-1.65V digital) and it must be taken into account in the routing.

From the point of view of mechanics, the main restriction was the size of the card and the position of certain components such as the MAPMT and output connector.

The maximum size of the card is around 10cmx10cm which forces the design in be separated in different cards and have a ‘sandwich’ solution. In the point next point there is a description of each card and some plots of the different layers of the cards. It has been separated into three cards where the separation of the electronics had been performed in order to minimize the mixed signal in a card, then it would be easy to route. The first one is the active base card for the PMT as we said, designed by the group of LPC. The second one is the analogue one, involving the ASICs at the

analogue circuitry, and the third one is the digital one, involving digital and LVDS signals.

From the radiation point of view, as it is explained in Chapter 3, all the components used must have a radiation qualification. On the other hand the FPGA firmware has been implemented in a triple-voting mode trying to avoid possible SEUs. The FPGA also monitorizes the possible SEUs in the communication to the off-chips DACs, the ASICs as well as its own registers giving the opportunity to read them back by the ECS.

From the cooling point of view, in order to monitorized the temperature in the VFE Unit, two temperature sensors were put in the card, and by the power supply link, the information of these sensors flow up to the regulator card which monitorize them.

5.2.2. FPGA Design

As it is mentioned in the previous point, the intelligence control was implemented through a Flashed-based FPGA from Actel, the family ProASIC^{PLUS}. The main advantages of this device are:

- The model used in the VFE design is the APA300 (300000 gates), but if more resources are need it can be easily change by other greater device of the same family as being pin to pin compatible.
- The kind of encapsulated is a TQFP208, avoiding the BGA footprint. It is difficult to found a farmer that gives reliability in the soldering of BGAs. (In the moment where the device was selected).
- The APA300 provides the resources needed, in number of memory cells, number of gates and in number of pins I/O.
- The programming of the device is on board by a specific cable provided by Actel.

Triple Voting

Taking into account the radiation environment, the FPGA must implement some techniques for avoiding the possible effects (In specific the SEE). The typical solution is implementing the Triple Voting Technique or Triple Voting Redundancy (TMR).

The TMR consists on having the information three times. The main key of this technique is what is called 'the majority voter'. The scheme can be found in Figure 30.

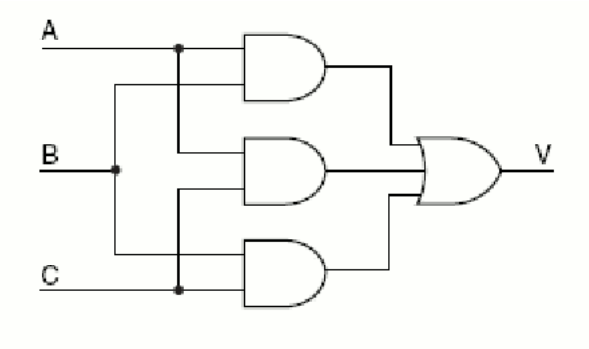

Figure 30. Majority Voter

The function of this block is the following: The output takes the value of the majority of the inputs. In our case, we use this block with the same input signal (three times the same signal). Thus, an error only can occur when two of these signals change (and the probability of changing to bits per SEU is very low).

There are different ways to implement the TMR. The easiest way is the Module-Level Protection, depicted in next figure.

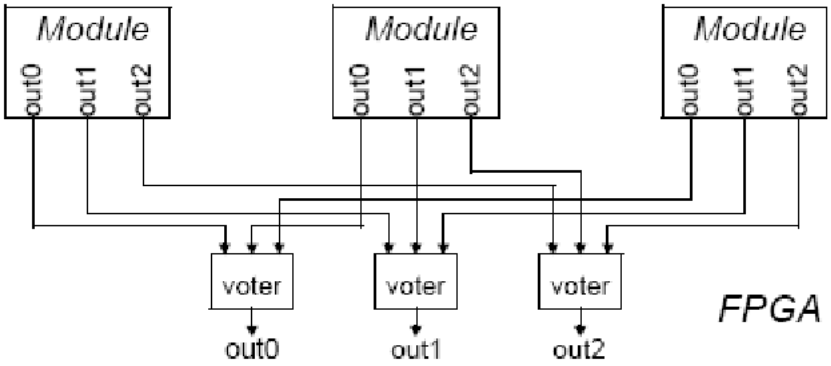

Figure 31. Module Level Implementation

The modules work in parallel, and in principle they have the same output. When an error occurs, one of the outputs of the voters is flipped. The main disadvantage is that it is impossible to know where the error has occurred, and then it is not possible to implement robust mechanism to recover the error (The modules can only be resynchronized by a reset). On the other hand the error can not be detected until it appears in the outputs.

As this technique presents limitations, in the VFE design has been implemented a low level solution: Gate-Level Protection, depicted at Figure 32.

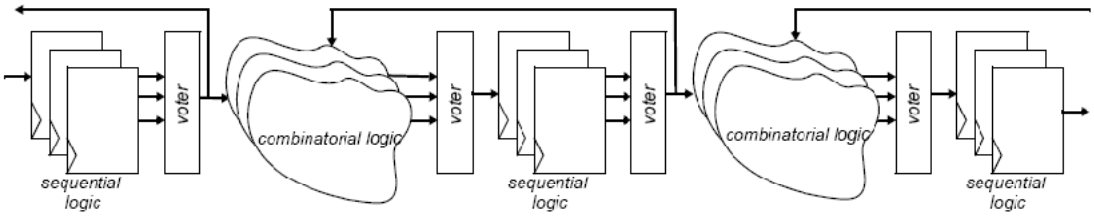

Figure 32. Gate Level Protection

In this case, if an error occurs, the data can be rewritten because there is a feedback.

More information about the implementation can be found in [46].

The use of the TMR implies several constraints in the design: On one hand, the occupancy of the FPGA is greater: more than three times the code without the TMR. This fact can imply a worst synthesis if the FPGA uses a lot of resources. On the other hand, the performance of the FPGA will be lower: the signals will have a delay in order to implement the TMR code (for i.e. the code implemented without the TMR had a maximum frequency of 57MHz and with the TMR this frequency was 42MHz).

Another point to take into account is the implementation in the software provided by the manufacturer. There some manufacturer that has this functionality in its options and it is easy to implement, but this was not our case.

VHDL Implementation

The Software used to implement the VHDL were *Synplicity Synplify* for the synthesis and *Actel Designer* for the implementation.

The Figure 33 shows the diagram block of the implemented code in the FPGA for accomplishing the requirements depicted in 5.2.1 and 5.2.2.

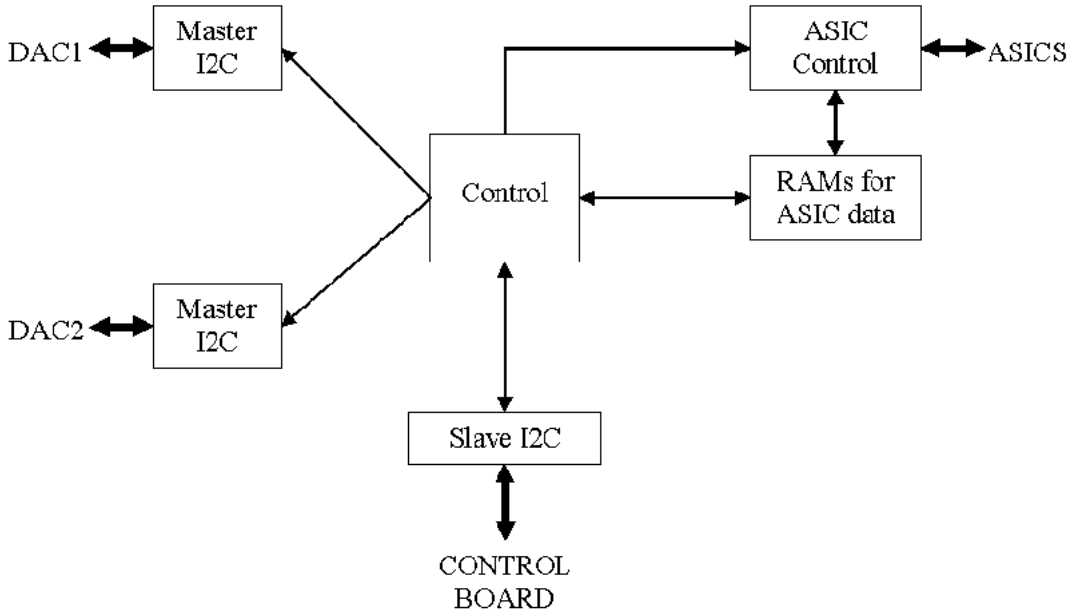

Figure 33. Diagram Block of code implemented in the FPGA

The *Control* is the block that monitorizes the rest of the blocks and it is charge of decoding the commands from the control block. An *I^2C slave* and *an I^2C Master* have been implemented for the I^2C communication with the external DACs. Finally, the block called *ASIC* is in charge of the communication with the digital interface of the ASIC.

More information about the VHDL implementation can be found in [46].

5.2.3. *PCB Layout and Design*

Apart from the electronics functional solution and the FPGA design, another key point of the work done is the PCB Layout of the VFE Unit. The techniques used for correct functionality and the number of layers were critical for a correct work.

In our case, the most critical signals were the LVDS signals. As a technology, LVDS is relevant in systems where data rates range from around 100 MHz to 2 GHz. In our case, the 40MHz or 20MHz clock there is not such as problem as the 280Mbits/s multiplexed link. At the link frequency, a PCB can no longer be treated as a simple collection of interconnections. Traces carrying these high-speed signals need to be treated as transmission lines. These transmission lines should be designed with appropriate impedance and they need to be correctly terminated.

The topics covered the range from impedance calculations and signal integrity to proper power supply design. They are relevant for any high-speed design, whether it employs ECL, CML, or LVDS.

Generalized design suggestions implemented are provided next.

The fast edge rate of an LVDS driver means that impedance matching is very important, even for short runs. Matching the differential impedance is important. Discontinuities in differential impedance will create reflections, which will degrade the signal and also show up as common-mode noise. Common-mode noise on the line will not benefit from the cancelling magnetic field effect of differential lines and will be radiated as EMI.

Controlled differential impedance traces should be used as soon as possible after the signal leaves the IC. Try to keep stubs and uncontrolled impedance runs to <12 mm or 0.5 in. Also, avoid 90° turns since these cause impedance discontinuities; use 45° turns, radius or bevel PCB traces. These techniques are implemented in the serializers up to the 2mm hard metric connector to avoid the problems explained above.

Minimize skew between conductors within a differential pair. Having one signal of the pair to arrive before the other creates a phase difference between voltages along the appearing signal pairs and radiate as common mode noise.

Use bypass capacitors in each package and make sure each power or ground trace is wide and short (do not use 50W dimensions) using multiple ways of minimizing inductance to the power planes.

PCB design using LVDS signals (Serializer's card)

There are some suggestions to follow when you are working with LVDS signals. Next paragraphs explain the suggestions used in design of the Serializer's card.

The use at least 4 PCB board layers (top to bottom): LVDS signals, ground, power, TTL signals is required. In our case, the serializer card is a ten-layer card, with components on both layers, top and bottom layer, class6 and made with FR-4. Five planes for different supplies and five layers for signals, a pair of them for the LVDS, the other pair for the CMOS ones, and a layer for the differential pair of clock are used. Dedicating planes for VCC and ground are typically required for high-speed design. The solid ground plane is required to establish controlled (known) impedance for the transmission line interconnections. A narrow spacing between power and ground will also create an excellent high frequency bypass capacity.

There must be isolation between fast edge rates CMOS/TTL signals from LVDS signals; otherwise the noisy single-ended CMOS/TTL signals may couple crosstalk onto the LVDS lines. The best way is routing TTL and LVDS signals on a different layer(s), which should be isolated by the power and ground planes.

Keeping drivers and receivers as close to the (LVDS port side) connectors as possible. This helps to ensure that noise from the board is not picked up onto the differential lines and will not escape the board as EMI, from the cable interconnect. This recommendation also helps to minimize the skew between lines. Skew tends to be proportional to length; therefore, by limiting length, we also limit skew.

Bypassing each LVDS device and also use distributed bulk capacitance. Surface mount capacitors placed close to power and ground pins work best.

In reference to *VCC pins:* One or two multi-layer ceramic (MLC) surface mount capacitors (0.1 μF and 0.01 μF) in parallel should be used between each VCC pin and ground if possible. For best results, the capacitors should be placed as close as possible to the VCC pins to minimize parasitic effects which defeat the frequency response of the capacitance. As the LVDS multiplexers contain a PLL, should have at least two capacitors per power type, while the other LVDS devices are usually fine with a 0.1 μF capacitor.

Power Distribution

EMI problems often start with power and ground distribution problems. EMI can be greatly reduced by keeping power and grounded planes quiet. Some suggestions are provided in the next paragraphs.

Power and ground should use wide (low impedance) traces: their job is to be a low impedance point.

Keeping ground PCB return paths short and wide. Provide a return path creating the smallest loop for the image currents to return.

Cables should employ a ground return wire connecting the grounds of the two systems. This provides for common-mode currents to return on a short known path and is especially important in box-to-box applications where ground return paths will help limit shifts in ground potential.

The fact of using two vias for connecting to power and ground from bypass capacitor pads to minimize inductance effects. Surface mount capacitors are good as they are compact and can be located close to device pins.

It is suggested to use vias in order to minimize the different impedance between planes.

Types of Traces

The type of traces that work well for differential lines is: Edge-coupled microstrip, edge-coupled stripline, or broad-side striplines (See Figure 34).

Edge-coupled microstrip lines offer the advantage that a higher differential ZO is possible (100W to 150W). Also, it may be possible to route from a connector pad to the device pad without any route. This provides a "cleaner" interconnection. A limitation of the microstrip lines is that these can only be routed on the two outside layers of the PCB, thus routing channel density is limited.

Stripline may be either edge-coupled or broad-side coupled lines. Since they are embedded in the board stack and typically sandwiched between ground planes, they provide additional shielding. This limits radiation and also limits coupling of noise onto the lines. However, they do require the use of vias to connect to them.

In our case, both types are used, but accomplishing the requirements explained in the differential traces point.

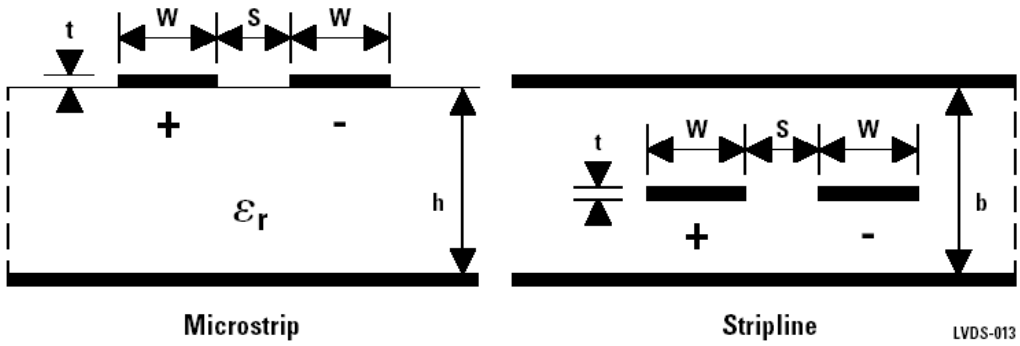

Figure 34. Microstrip and Stripline differential traces

Differential Traces

If differential traces are used in the design, some rules have to be taken into account.

The use of controlled impedance PCB traces that match the differential impedance of the cable and the use termination resistor was implemented as well as routing the differential pair traces as close together as possible and as soon as they leave the serializer or the transceiver. This helps to eliminate reflections and ensures that noise is coupled as common-mode. Signals that are 1mm apart radiate far less noise than traces 3mm apart, as magnetic field cancellation is much better with the closer traces. In addition, noise induced on the differential lines is much more likely to appear as common-mode, which is rejected by the receiver.

Matching electrical lengths between traces of a pair is a good way to minimize skew. Skew between the signals of a pair will result in a phase difference between the signals. That phase difference will destroy the magnetic field cancellation benefits of differential signals and EMI will result. A general rule is to match lengths of the pair to within 100 mils.

It has to minimize the number of vias and other discontinuities on the line, and to avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels instead.

Within a pair of traces, the distance between the two traces should be minimized to maintain common mode rejection of the receivers. For best results, both lines of the pair should be as identical as possible.

5.3. Prototype History

The definition of the Scintillator Pad Detector, its requirements and specifications has been in evolution since 1998, when the experiment started. This implies not only a slow lead, but also a great amount of prototypes of different ASIC versions and test versions, a tedious task to achieve a system containing every specification required.

On first term, the ASIC runs required of a setup in order to be tested. Once the full custom design was decided and finished, on the fifth run, the VFE unit design started.

First of all a prototype with all the functionalities but only with two discriminators was implemented. After that, a full complete VFE Unit was designed with the eight discriminators without the Control Unit (at this time, the unique FPGA that passed the radiation qualification was an antifused one, that was one time programmable. For this reason, it was not implemented). As a result the mechanical constraints and the space available for the VFE Units, the design was splitted into two cards: One containing the analog part and the connection to the PMT and the other one containing the digital part and the connection to the outputs of the VFE Unit.

In the third prototype, the kind of connectors was changed. 2mm high speed connectors were chosen to improve the performance of the outputs.

The prototypes designed up to final prototype are described in the paragraphs above.

The software used for the design of the earliest prototypes was *Microsim®*, which is obsolete, and the final prototype was design with *Altium Designer DXP*, that software contains multiple tools to make easy the design such as footprints wizards, impedance control, manufacturer rules improvement…

5.3.1. *ASIC prototypes*

Each ASIC run needs a prototype to be tested. These prototypes offer the necessary information on the behavior of analog signals and digital signals, components size, components required (It is necessary to consider that the definitive ASIC was produced in 2004) to define the requirements of the VFE unit.

The evolution of the cards was limited by the evolution of ASIC: ECL output signal levels or CMOS signal levels; digital programmable parts inside the discriminator or not; digital or analog pile up subtraction; DAC for thresholds inside ASIC, outside or both; swing of power supplies; number of powers supplies; current need for feeding the ASIC inputs…

5.3.2. *VFE Unit First Design*

All these constraints delayed the first design of the VFE unit up to the end of 2003. This design consisted only of two ASICs instead of the necessary eight, the LVDS serializer and the LVDS transceiver (for adapting the signal cable), DACs and without the Control Unit.

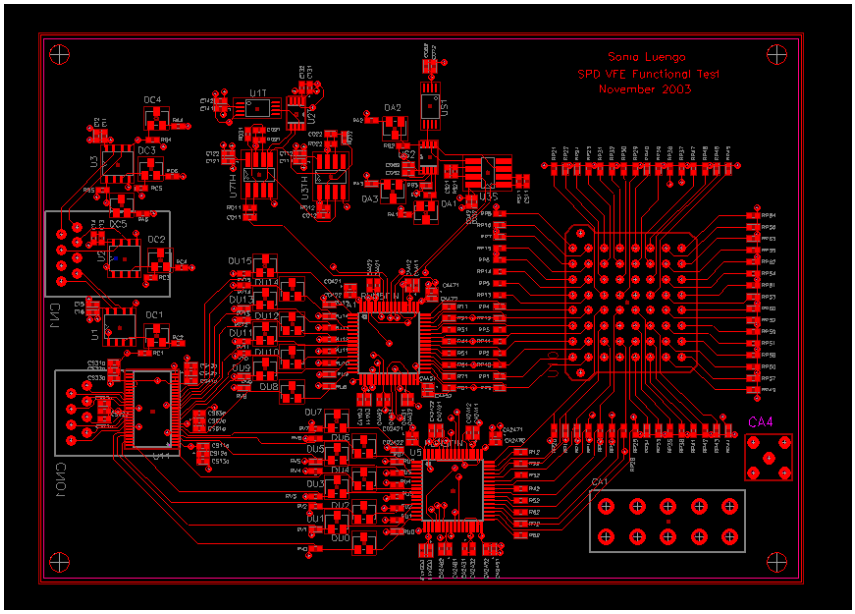

Figure 35. First VFE Unit

The main goal of this card was to test the functional design: The datapath from the photomultiplier to the LVDS multiplexer.

Tests showed that some signals were critical, such as the 40MHz clock, and the 20MHz, that up to now, these signals were common mode and the results show the need to convert all the clocks into a differential mode. Therefore, some rules in the layout (such as the rules explained in the point 5.2 referred to distribution of power supplies or routing the differential traces) and in the type of cables used had to be considered in the next prototypes in order to improve the shape and the jitter of these signals.

5.3.3. *VFE Complete Unit First Design*

This design ended in the first term of 2004. It had all the final components, including the eight ASICs, it is only lacking the FPGA. This time, what the FPGA qualified to be rad-tolerant was a onetime programmable antifuse Actel FPGA. As a result of being only one time programmable, the prototype used a Flashed-based FPGA instead of the antifused one. Differential mode for clocks was not designed yet.

The design was interrupted during three months, awaiting the tests of the LVDS link, explained in Chapter 4. This link was a tedious task, as a result of the 25 meters of cable needed to cover the distance between farest VFE Units and the FEBs.

In this prototype, the mechanical constraints, such as the space available were taken into account. For this reason, the design was split into two cards: The ASIC one, containing the PMT, the eight ASICs and the whole analogue circuitry (see Figure 36) and The Serializer one, containing the digital part, the level adaptation as well as the LVDS part with its differential traces (Figure 37).

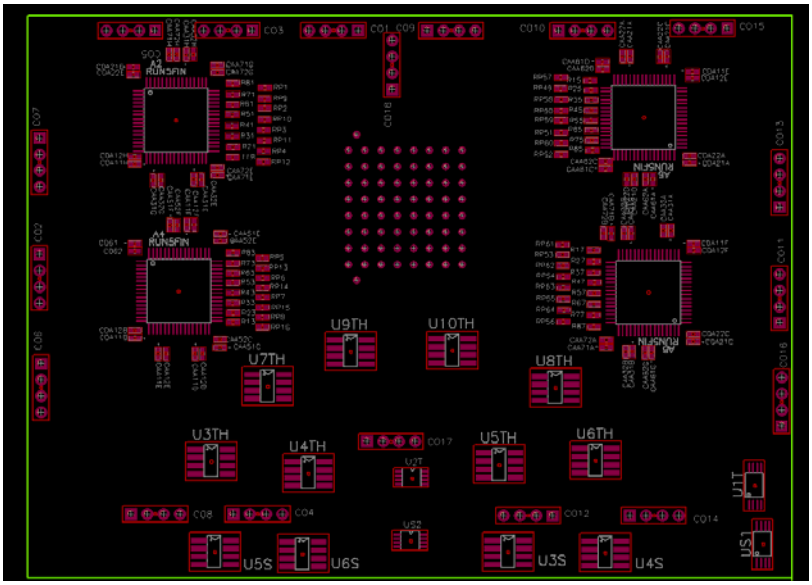

Figure 36. First Complete VFE. Board 1

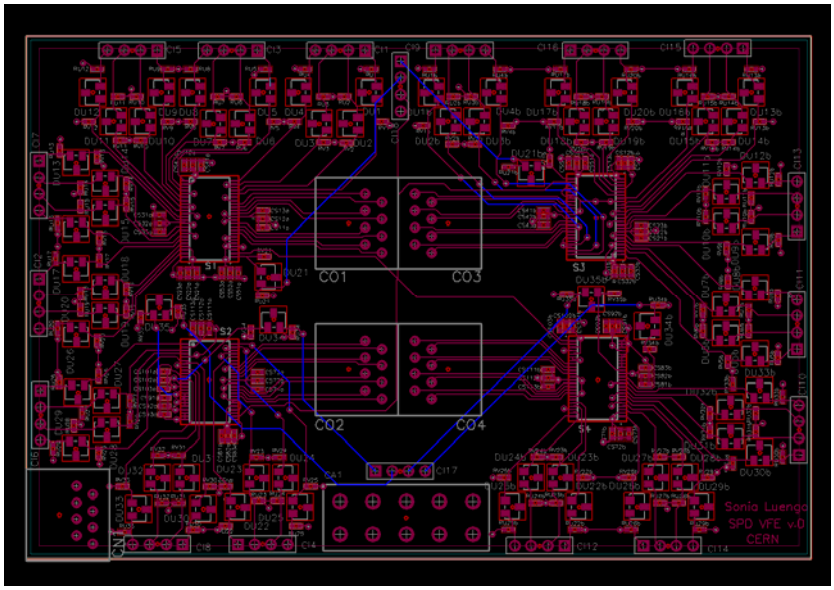

Figure 37. First Complete VFE. Board 2

At this time, the size of the card was one of the most important parts to test with all components required. The mechanics was starting to design, and the sizes started to be determined. Despite this fact, the final measures were not defined.

5.3.4. *VFE Complete Unit Second Design*

Considering the results obtained in the first design and in the final LVDS tests where the final cables were decided, the output connectors had to be changed. The LVDS link needed a fast connection, for this reason the connectors selected were High Speed, 2mm Hard Metric connectors.

In this attempt, the FPGA was not yet decided: Actel flash-based FPGAs were being tested for their radiation qualification and they seemed to work properly. If these FPGAs could be used the testing would be much easier, these ones are reprogrammable.

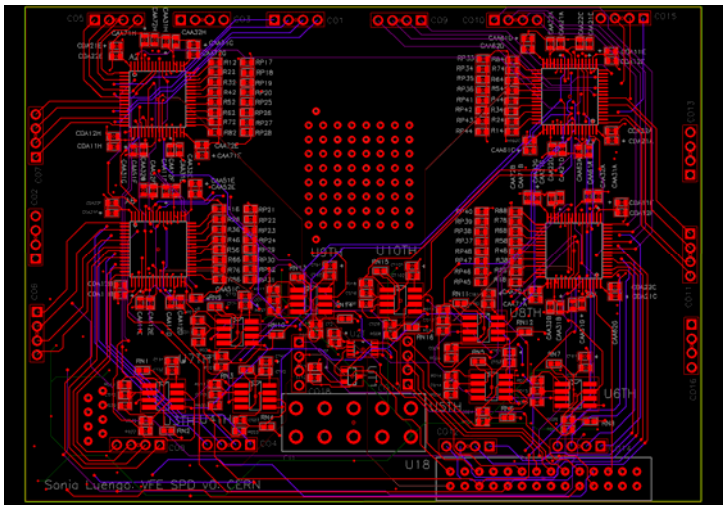

Figure 38. Second Complete VFE. Board 1

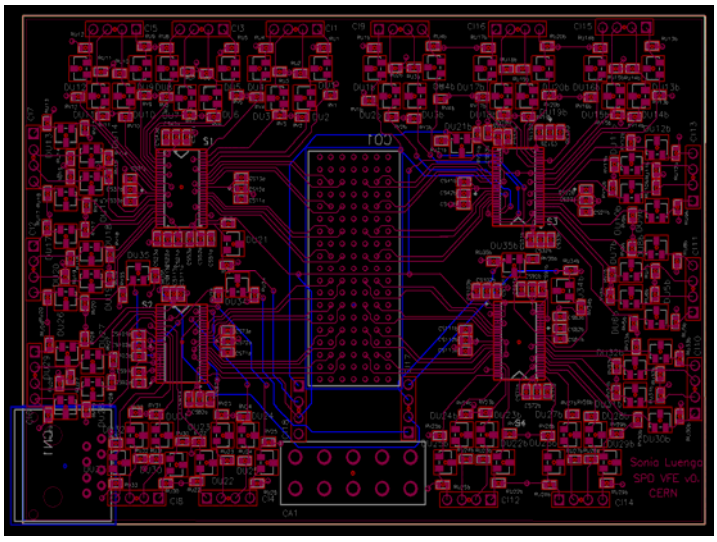

Figure 39. Second Complete VFE. Board 2

5.4. Final Design

In the final design a Flash-based FPGA was chosen by the fact that they passed the irradiation and achieved the radiation qualification. The rest of the electronics was the same as in the second complete unit design excepting the clock treatment. In this prototype, the conversion of each clock to a differential one was designed and tested. The jitter on the clock signals and the shape had a significant improvement. The validation of this card as the final design can be found in the tests performed in the prototype in Chapter 6.

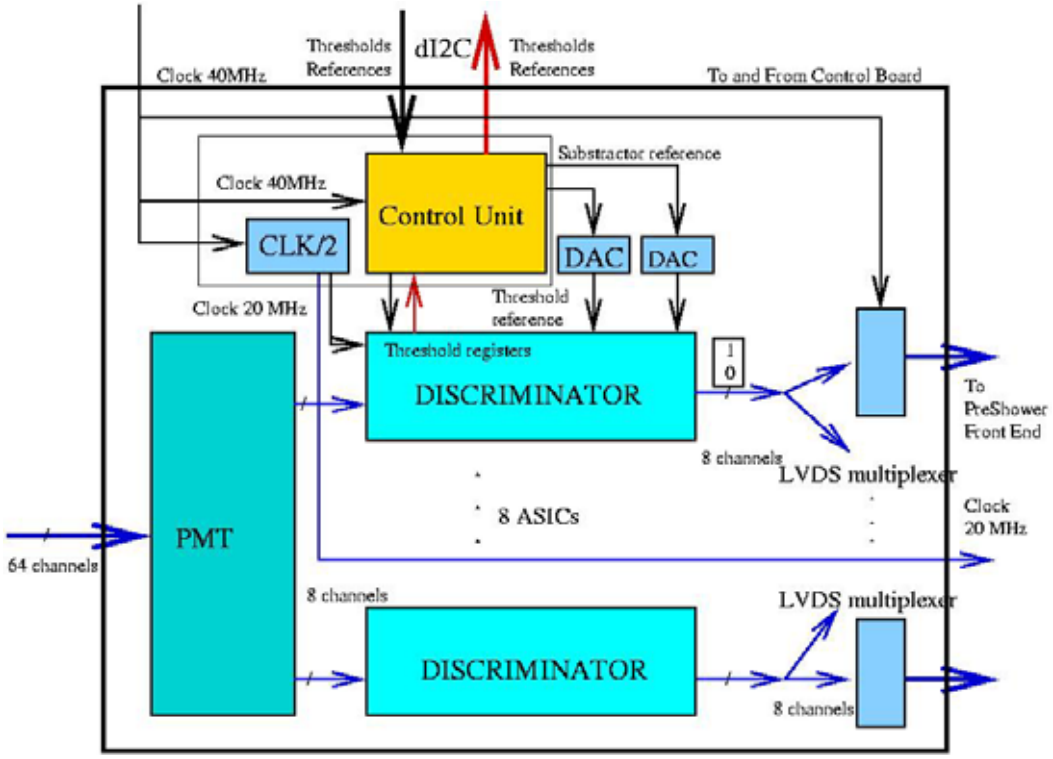

Figure 40. VFE Diagram block

The functional block of the VFE Unit, depicted in the Figure 40 are:

- ECS (Experiment Control System) link: involving the transceivers and the Control Unit.
- Light-Electrical Signal Converter: Photomultiplier and its circuitry.

- Analog-Digital Converter: involving the ASIC, the threshold DAC, the subtractor DAC as well as the OpAmps for giving the necessary current for ASIC's inputs.
- Output Adaptation: LVDS Serializers.
- Discrete components: The signal adaptation in power supplies required for the environment.

Each one of these blocks has different requirements and different design solutions. For this reason it is important to understand the functionality of each one of them. The points below explain each block: specifications, design solution and electronic components related to each block and the radiation qualification in some cases (Single Effects and Cumulative Effects) as the Chapter 3 explained that this kind of systems has.

5.4.1. ECS (Experiment Control System) link (Transceivers, Control Unit)

This block is formed by transceivers and the Control Unit (FPGA).

Communication between the Control Board-VFE Units is a digital-serial communication. The signals arrived from an RJ45 feeding the transceivers. These transceivers only adapt signals from differential LVDS levels to LVTTL signals. These LVTTL signals go to the FPGA which is in charge of receiving and translating the communication, as it is explained in 5.2.2.

The communication is made by a four-pair cable that follows a protocol following the I^2C standard: thresholds, levels of subtraction and control flow in this communication.

Transceivers (ECS link)

Functionality

Its function is making the link between the control card (up to 25 meters distance in calorimeter crates) and the control unit. They translate the diferential LVDS to LVTTL output.

Requirements

The main requirement is that its input must be a differential LVDS and the output must be LVTTL to communicate with the Control Unit. The maximum speed in the I^2C signals is about 1Mbit/s, and the bunch-crossing clock is 40MHz. The distance of the link can be from 5 up to 27 meters.

Electronics Components

For each signal a LVDS National transceiver is necessary. The DS90LV010 makes the conversion from differential LVDS signaling to unipolar CMOS signaling.

Radiation Qualification

Monitorising the power supply current we know if some latch-up or another effect occurs during test time at Ganil. Off-line are measured the output voltage linearity and the output load regulation previous and after irradiation. Results can be found in [15].

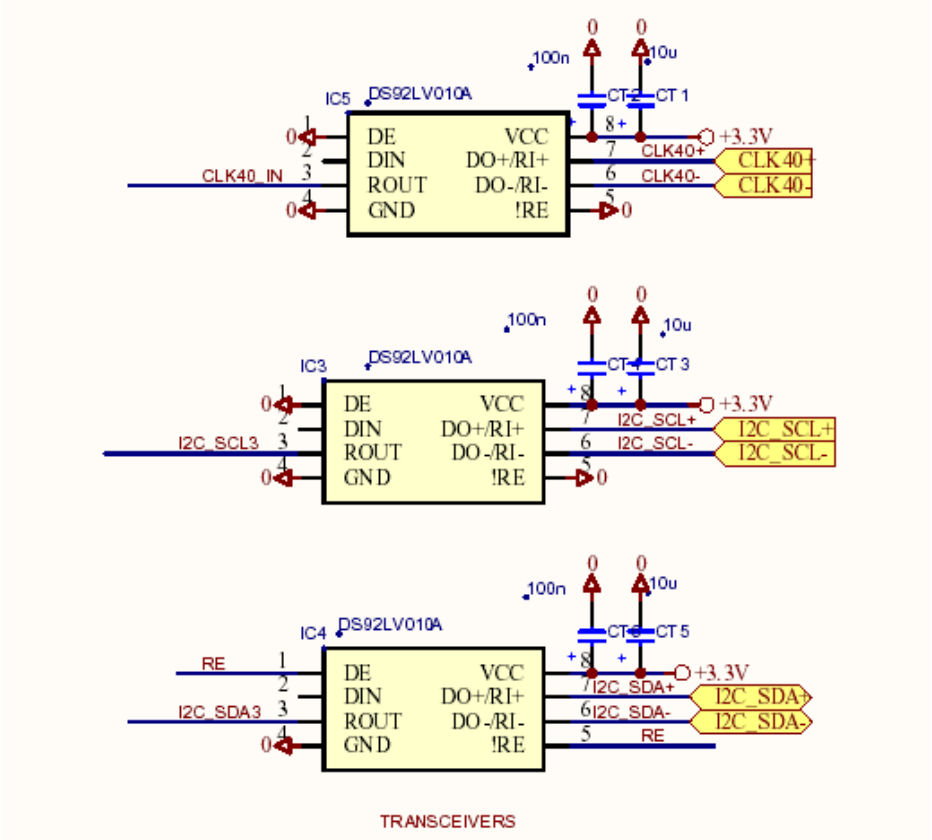

Figure 41. Schematics of LVDS Transceivers

Control Unit

Functionality

Its functionality is described 5.2.2. The following points are a summary of its functionalities.

Functionalities:

- I^2C bidirectional communication with the control board. A byte to control transmission errors is included. If the received command is not recognized, it will be ignored and the corresponding bit of the status register will be marked.
- Write and read ASIC registers.
- Write and read DACs (Vref and Vbias) via a local I2C bus.
- ASIC SEUs: Checking, correcting and signaling in the status register.
- DAC SEUs: Checking, correcting and signaling in the status register.
- DAC no longer responding: checking, reset and signaling in the status register.
- External DACs reset. If a TIME-out is detected it should be corrected.
- The control unit is for reading and resetting the status register. This register must indicate the following events:
    - SEUs in ASICs
    - SEUs in DACs.
- Problems with the I^2C bus: hang and reset of the DACs.
- Transmission errors between the Control Card and the VFE.
- In addition the proAsic allows the mapping of the VFE channels as needed through the pin-out definition.

Electronic Components

The Control Unit is implemented by Actel ProASICPlus, APA300.

Radiation Qualification

All the effects due to a radiation environment have been tested by the manufacturer. The summary of the tests is that the ProASIC^{PLUS} devices can be used in this kind of environment [47].

Table 3 summarizes the test data of the APA750. Only two upsets were observed in the whole experiment. The cross section per bit is obtained as 3.1 x 10^{-14} cm2 for neutron energies > 1.5 MeV and 6.02 x 10^{-14} cm^2 for neutron energies > 10 MeV. No other SEE was observed in any DUT.

The whole information about these tests can be found in [47].

DUT	Fluence (neutron/cm^2)		Flip-flop Upsets	
	> 1.5 MeV	> 10 MeV	DOS	DOH
LAPA1017-1	3.58 x 10^{10}	1.84 x 10^{10}	1	0
LAPA1017-2	3.58 x 10^{10}	1.84 x 10^{10}	0	0
LAPA1017-3	3.03 x 10^{10}	1.56 x 10^{10}	0	0
LAPA1017-4	2.57 x 10^{10}	1.33 x 10^{10}	1	0
LAPA1017-5	3.36 x 10^{10}	1.74 x 10^{10}	0	0

Table 3 Flip-Flop Upsets in DUR Shift Registers

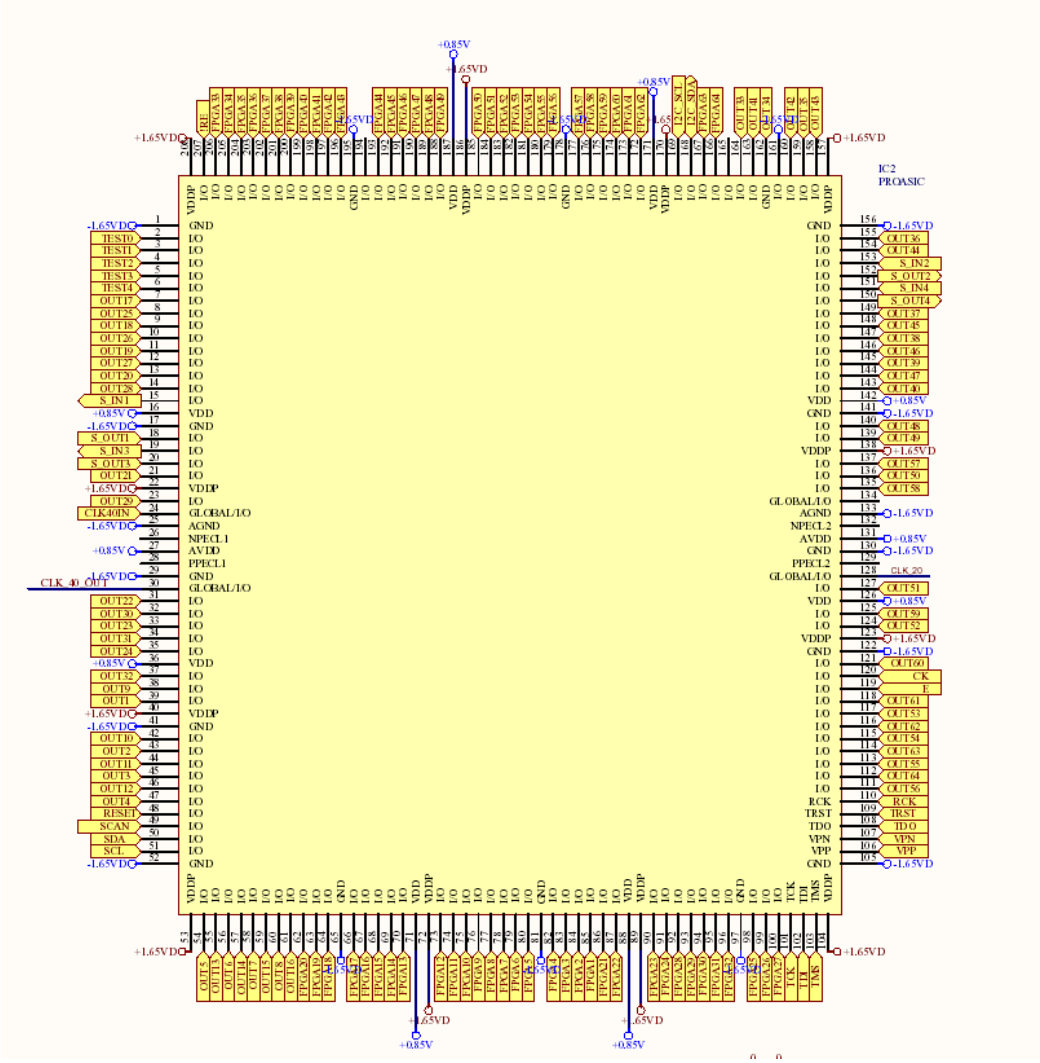

Figure 42. Schematics of FPGA

Description of inputs / outputs:

All the signals involving the FPGA are shown at figure 42.

- *OUTi: These signals are the 64 outputs of the ASICs. They come from the ASICs*
- *FPGAi: These signals are the 64 outputs of the ASICs remapped in the correct way. They go to the inputs of the LVDS serializers*
- *SINi /SOUTi /SCAN/ CK / E : Signals that program internal thresholds of the ASICs. They go to the ASICs*
- *TESTi : These signals test the serial LVDS link. They go to LVDS serializers*
- *CLK40IN: Input clock of 40MHz. It comes from the input stage (transceivers)*

- *SCL / SDA: Signals that control the I2C bus involved in programming of DACs*
- *RESET : Signal that control the Power Supply of DACs*
- *TCK /TDI /TMS /VPP /VPN /TDO /TRST /RCK: JTAG programming signals of the FPGA*
- *I2C_SCL /I2C_SDA: Signals that control the I2C bus involved in FE-VFE Communication. They go to transceivers*
- *!RE: Signal that controls the direction of transceivers (Receiver or Transmitter). It goes to transceivers*

5.4.2. *Light-Electrical Signal Converter: Photomultiplier*

This block is formed by the connection of optical fibbers, photomultipliers, and charged resistors of MAPMT (R7600-00-M64 de Hamamatsu) described at Chapter 4 [14].

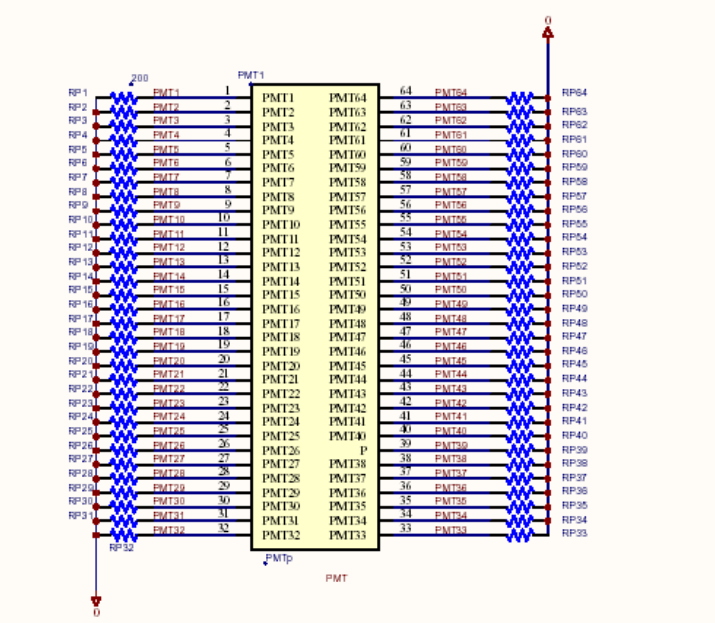

Figure 43. Schematics of Photomultiplier

The optical signal goes from the optical fibbers to photomultipliers, which are in charge of converting this optical signal into an electrical one. The 6000 channels of the SPD are divides in groups of 64, where these optical channels are plug to a

MAPMT. Its outputs give a current signal that is converted into a voltage signal by charge resistors. These outputs must be adapted to fulfill the requirements of the gain, stability and a special base has to be created in order fulfill the requirements of aging [36].

5.4.3. Analog-Digital Converter (ASIC, Threshold, Subtractor DAC, OpAmps)

This block is formed by the ASICs [20] and the circuitry the ASIC involves (threshold DAC, subtractor DAC, OPAmps, resistors, capacitors).

The analog signal from the outputs of the PMT is converted into a CMOS signal by the ASICs. The outputs of the ASICs give a '1' or '0' in order to distinguish if the particle crashed was charged or not. This result is achieved by analog signal processing (the function of ASICs): first, the analog signal is integrated; second, the part of the previous period is subtracted; finally, this signal is compared to a threshold level to consider if it is charged or not. Each ASIC has 8 channels; therefore eight ASICs are necessary to process the 64 output of PMT.

The percentage of subtraction is not generated inside the ASIC, but is given by a subtractor DAC, which is programmable by Control Unit. The threshold level is also programmable, but it is divided into two parts: one part is common for an ASIC and the other one is different for each subchannel of an ASIC. The common part is generated externally by a threshold DAC, also programmable. This level provides the range for the final threshold.

All these levels are programmed by the FPGA which receives the instructions from the ECS trhough the Control Card.

ASIC

Functionality

It is the most important part in the processing, explained in Chapter 4.

Electronics components on VFE

Each ASIC can process up to eight channel-information, therefore eight ASICs are necessary to process the 64 output PMT channels.

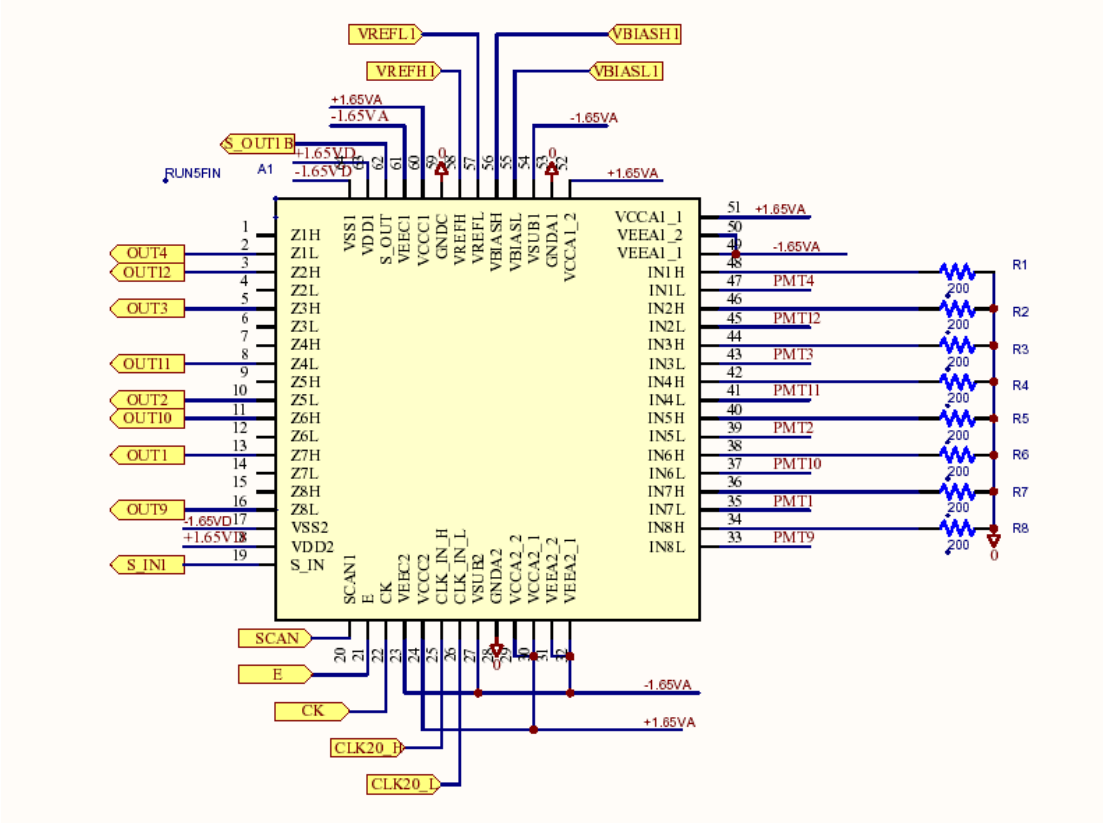

Figure 44. Schematics of an ASIC.

Description of inputs / outputs:

All the signals involving the ASICs are depicted at figure 44.

- *PMTi: Inputs of the ASIC (Each ASIC has 8 inputs/ 8 ASICs per card)*
- *OUTi: Outputs of the ASIC (Each ASIC has 8 outputs/ 8 ASICs per card)*
- *VREFLi/VREFHi: Differential pair that comes from the Threshold Reference DAC (There is a subindex because the signal comes from different OPAmps, each of these inputs needs 50mA and the DAC is not able to feed the eight ASICs, but the value is the same for all them, they have the same reference)*
- *VBIASLi/VBIASHi: Differential pair that comes from the Substractor Reference DAC. (There is a subindex because the signal comes from different*

OPAmps, each of these inputs needs 25mA and the DAC is not able to feed the eight ASICs, but the value is the same for all them, they have the same reference)

- *SOUTi / SINj / SCAN /CK / E: Signals that are in charge of programming the internal thresholds of each ASIC, comes from the Control Unit (FPGA). They are connected by daisy chain to minimize the signals needed from FPGA.*
- *CLK20H / CLK20L: Differential Clock Signal of 20 MHz (Remember that each ASIC has two subchannels working a 20 MHz clock).*

Threshold Reference

Functionality

It involves a DAC and eight OpAmps (one per ASIC). They provide the threshold reference for the ASICs (its internal DAC).

Requirements

The power suppy of the threshold reference must be a CMOS level but in a symmetric way (± 1.65V referred to GND) and must be differential. The resolution is 8 bits and it must provide up to 20mA per ASIC (it has low impedance output). It is necessary a band gap reference and a serial control is preferred in order to minimize the number of connections.

Electronic Components

Combines a DAC and low impedance OpAmps (one per ASIC to accomplish the 20mA input). The interface with DAC is in I^2C protocol.

Radiation Qualification

In the tests at Ganil, continuously the DACs registers are read by I2C bus and SPI bus, updating the value if this is wrong and monitoring the output voltage to confirm a SEU and to determine i f the written register is the same that feeds the DAC output. Monitorising the power supply current we know if some latch-up or another effect occurs during test time. Off-line are measured the output voltage linearity and the output load regulation previous and after irradiation [15].

The FPGA monitorizes the value of internal registers in order to avoid SEU and also monitorizes the I^2C signals in order to avoid SEL. If a SEL is detected, the FPGA can reset the DACs.

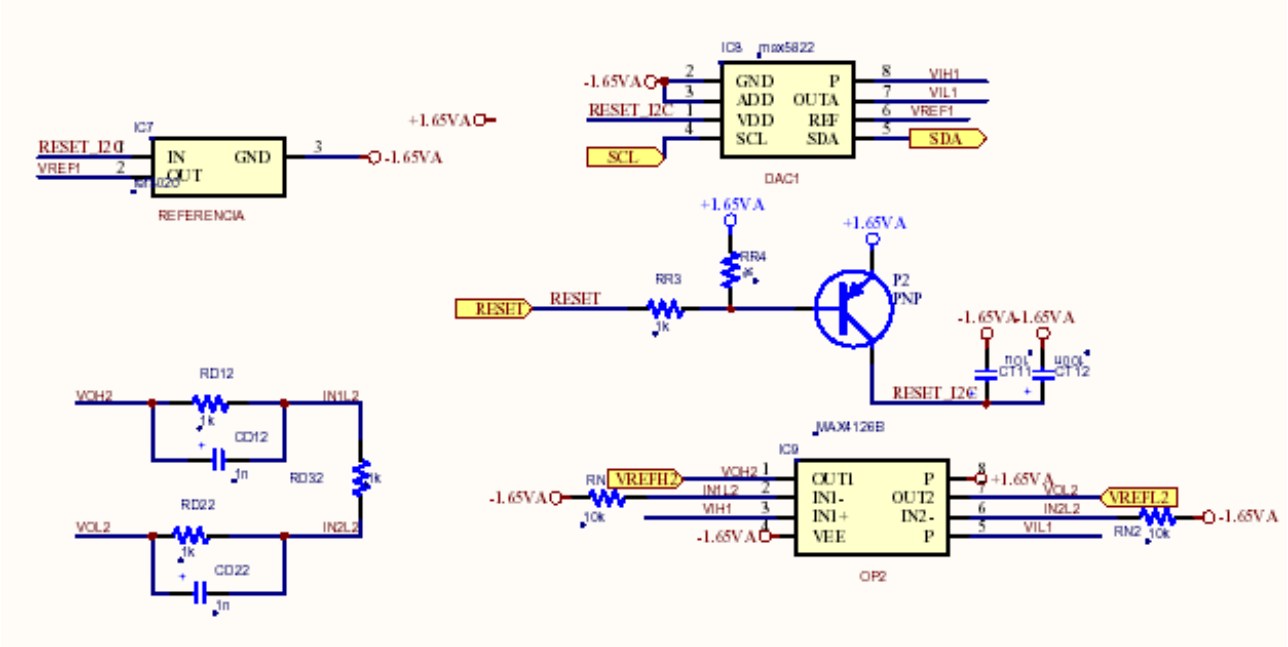

Figure 45. Schematics of Threshold Reference.

Description of inputs / outputs:

All the signals involving the theshold references are depicted at figure 45.

- *VREFLi/VREFHi: Differential pair that goes to the ASICs (There is a subindex because the signal outs from different OPs, each of the inputs of the ASICs needs 50mA and the DAC is not able to feed the eight ASICs, this is why there is an OP for each ASIC. In the figure above there is only one OP)*
- *SCL /SDA : Signals to program the DAC. It is a serial DAC that has to be program by an I2C protocol. These signals come from the Control Unit (FPGA)*

- *RESET: Signal that control the power supply of the DAC. Its function is to reset the DAC if a SEL is detected. This signal comes from the Control Unit (FPGA).*

Subtractor Reference

Functionality

Its function is ASIC pile-up correction due to the large tail of the signal.

Requirements

The power suppy of the subtractor reference must be a CMOS level (+3.3V/GND) and must be differential. The resolution needed is 8 bits and it must provide up to 5mA per ASIC (it has low impedance output). A serial control is preferred in order to minimize the number of connections. The component must be a rail to rail component because the range of the outputs must achieved the maximum value.

Electronic Components

It Combines a DAC with Rail to Rail Output and four OpAmps (one per two ASICs to accomplish the 5mA input). The interface with DAC is in I^2C protocol.

Radiation Qualification

The same tests at Ganil that the tests for the Threshold Reference.

The FPGA monitorizes the value of internal registers in order to avoid SEU and also monitorizes the I^2C signals in order to avoid SEL. If a SEL is detected, the FPGA can reset the DACs.

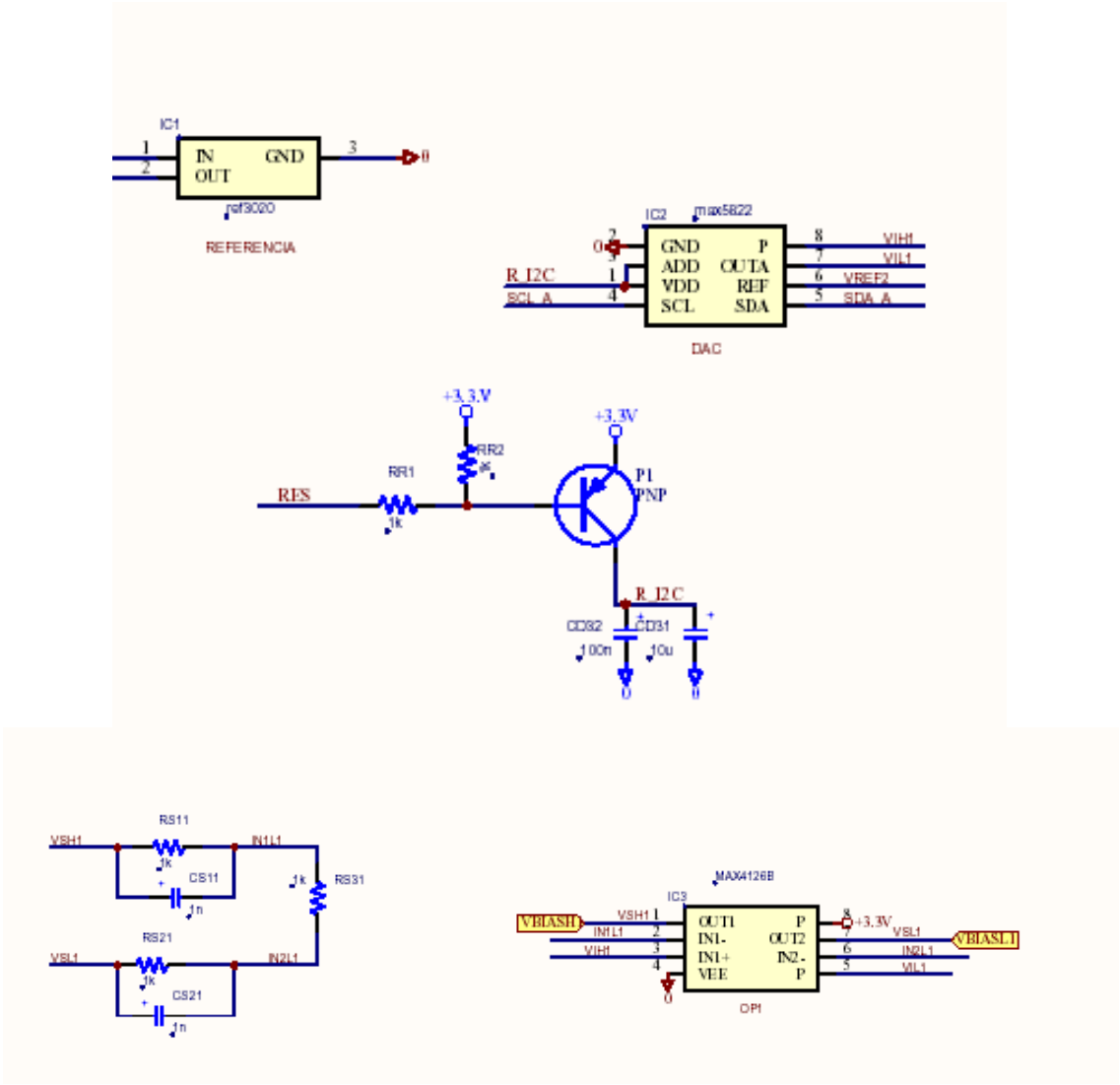

Figure 46. Schematics of Subtractor Reference. DAC and reference at top, OPAmp at bottom.

Description of inputs / outputs:

All the signals involving the subtractor references are depicted at figure 46.

- *VBIASLi/VBIASHi: Differential pair that goes to the ASICs (There is a subindex because the signal outs from different OPs, each of the inputs of the ASICs needs 25mA and the DAC is not able to feed the eight ASICs, this is why there is an OP for two ASICs.*
- *SCL_A /SDA_A: Signals to program the DAC. It is a serial DAC that has to be program by an I2C protocol. These signals come from the Control Unit (FPGA).*

- *RES: Signal that control the power supply of the DAC. Its function is to reset the DAC if a SEL is detected. This signal comes from the Control Unit (FPGA).*

It has to be remarked that this part is feed by a power supply of 3.3V, that it is different of the power supply of the ASICs and Control Unit (+/-1.65V). Therefore, an adaptation is needed.

5.4.4. Output Adaptation (LVDS Serializers)

This block is formed by LVDS multiplexers.

Functionality

Each SPD VFE board has sixty-four outputs. These outputs feed the PreShower FE board, implying that 64 different pair lines (cables) are needed for each VFE board. In order to minimize the number of cables a LVDS multiplexer has been added. These four multiplexers allow the sending of 70 bits at 40MHz (2.8Gbit/s) through 14 pairs. The output of the LVDS multiplexer must be compensated (with a pol-zero compensation) in order to avoid the effects of long cables (skin effect), but this compensation is not made in the VFE Unit as it explained in 4.6.3.

Requirements

The main requirements are three: the first one is having a multiplexation factor from 5 to 7 (a speed from 200Mbit/s to 300Mbit/s). The distance of the link is up to 27 meters long. The third requirement is that the serializers have a minimum size.

Electronic Components

The serializer DS90CR215 will be used. It multiplexes 7 bits into LVDS data pair. Each serializer has 3 data pairs and 1 clock pair. (4 serializers are needed, 10 data pairs and 4 clock pairs). A full custom cable for 4 pairs has to be made and high density 2mm Hard Metric connectors are used in the backplane and in the VFE unit. Characteristics of chipset:

- 21 bits to 3 data pairs + 1 clock pair.
- Differential output voltage 250mV (min), 290 (typ) and 450 mV (max) on 100 Ω.

- Differential input threshold:
    - High: +100mV.
    - Low: -100mV.
- Data rate: 40 Mbit/s x 7 = 280 Mbit/s per pair.
- No pre-emphasis.
- No DC balance.

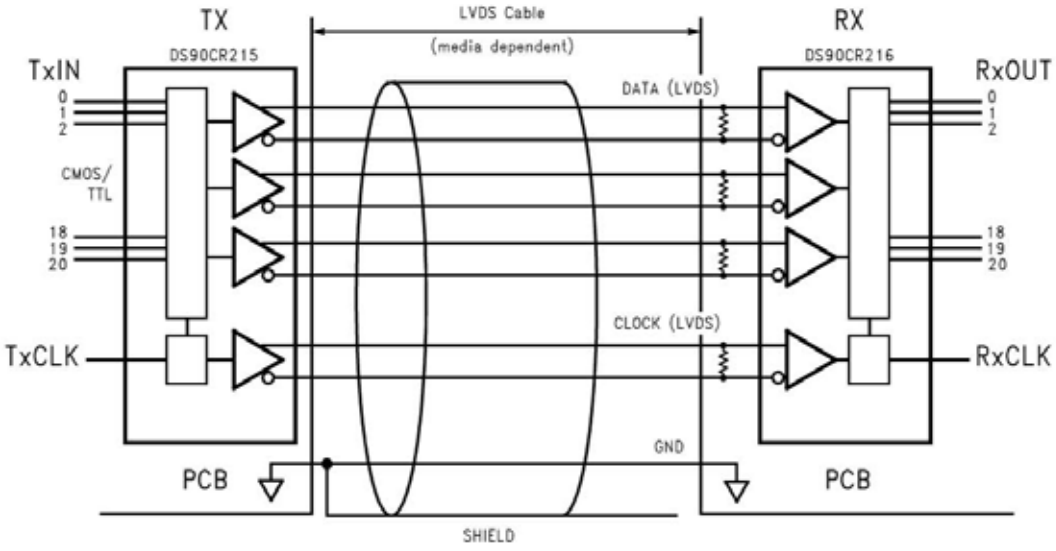

Figure 47. LVDS Link

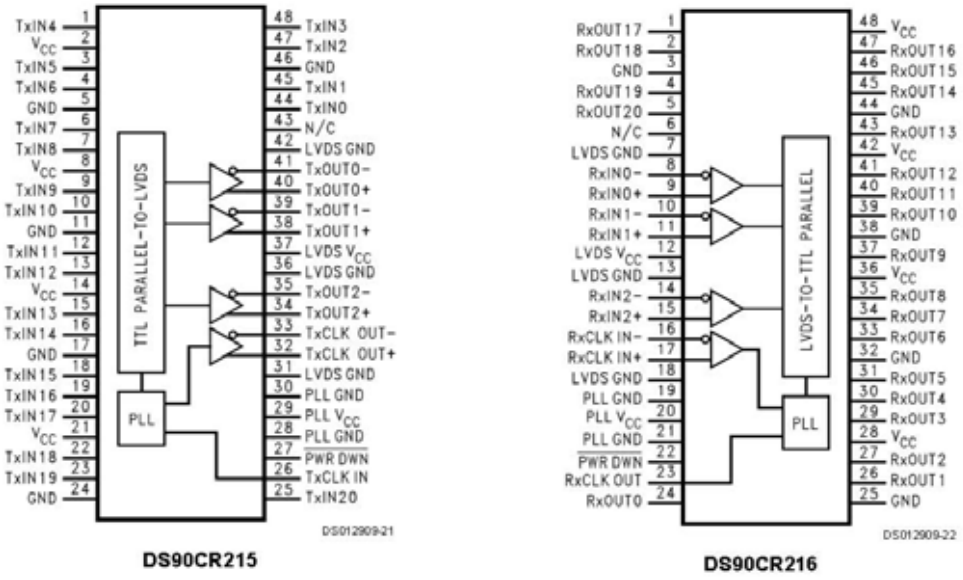

Figure 48. LVDS Chipset Link

The receiver skew margin (RSKM) definition according to National Application note 1059.

RSKM is the margin for data sampling at receiver inputs. This number is based on the pulse position (Tppos) and strobe position (Rspos) characteristics of the device:

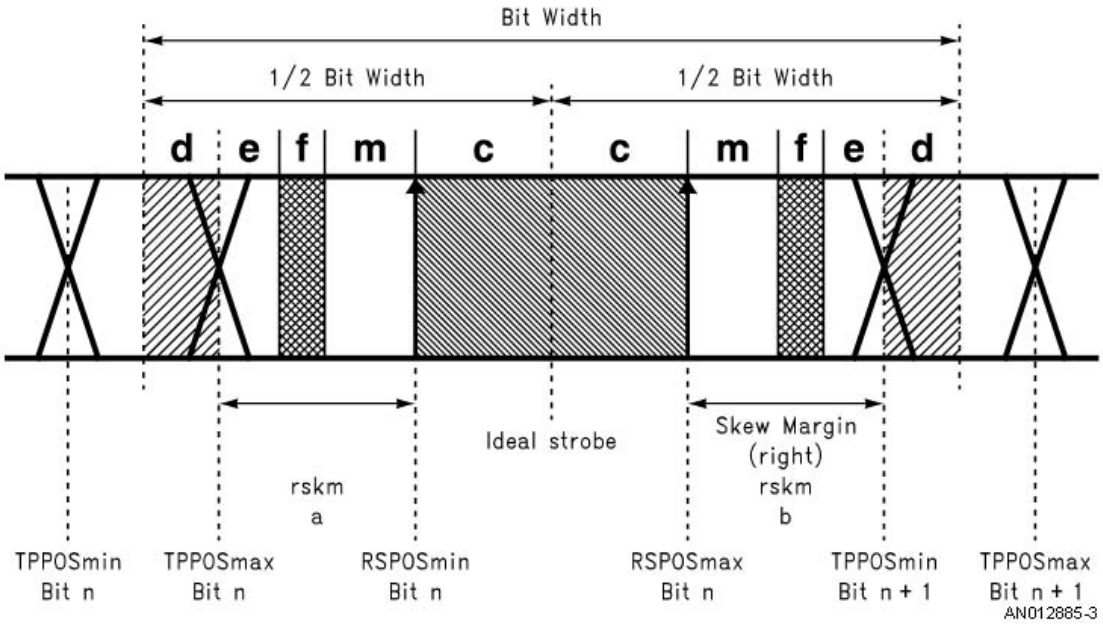

Figure 49. Frame

c: represents the setup and hold times for the receiver relative to the ideal strobe position (Rspos max and Rspos min).

d: is the variation of transmitter pulse position from ideal (Tppos max – ideal and ideal - Tppos min).

e: is the cable skew.

f: is the clock jitter.

m: is the remaining margin for data sampling: $m=rskm-(e+f)$.

For the DS90CR21X chipset RSKM=490 ps at 40 MHz. Since bit width is 3.57 ns, the opening time for an eye diagram should be 2.59 ns

Radiation Qualification

The same kind of tests as Transceivers made at Ganil [15].

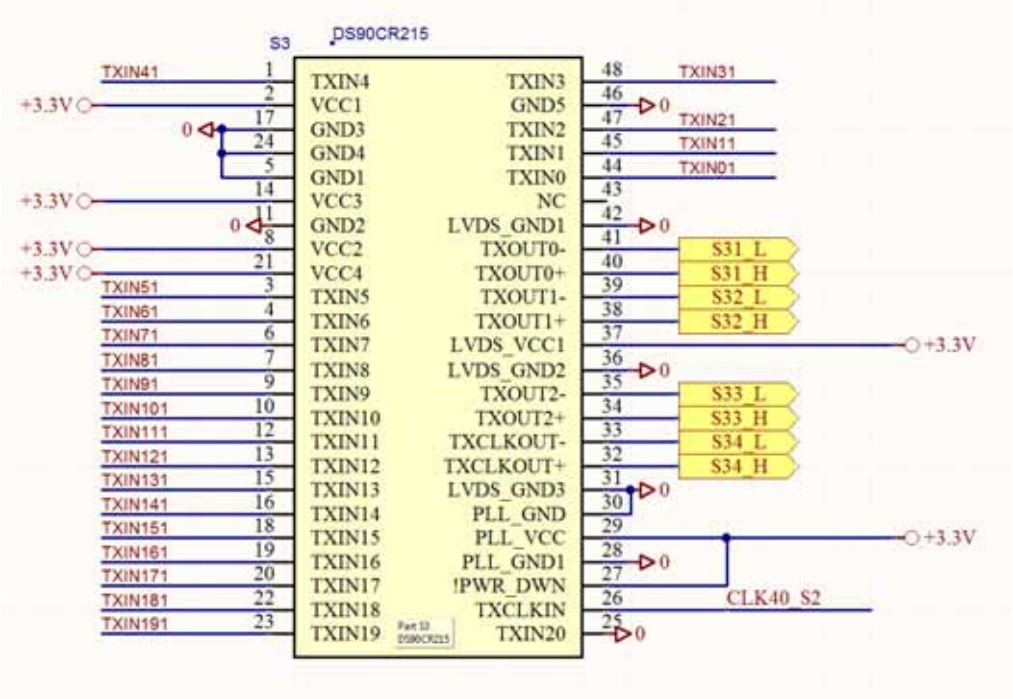

Figure 50. Schematics of LVDS Multiplexer

Description of inputs / outputs:

All the signals involving the serializers are depicted at figure 50.

- *TXINi: Outputs of the ASICs remapped, coming from Control Unit (FPGA)*
- *Si: Outputs of the serializers. Multiplexed LVDS at 280MHz. They are the outputs of the SPD.*
- *CLK40_3V: Input clock of serializer.*

Discrete components (Signal Adaptation, Discrete)

Power Adaptation

Functionality

One of the problems of the design of VFE board is the voltage levels of the components. For e.g. ASICs voltage supply is (+/-1.65V), and the output of the board should be 3.3V (for the PreShower FE board- SPD VFE board communication), this implies that needs a voltage level adaptation between both boards.

Requirements

The same as its function make a power signal range adaptation.

Electronic Components

This adaptation is done by a passive circuit (only 2 PIN diodes and 2 resistors).

Radiation Qualification

In the tests at Ganil, these pin diodes are only tested for TID effects, so they are not continuously monitored. Off-line we measured the rise, fall and delay time and the low and high output voltage as well as the I (V) characteristic previous and after irradiation [15].

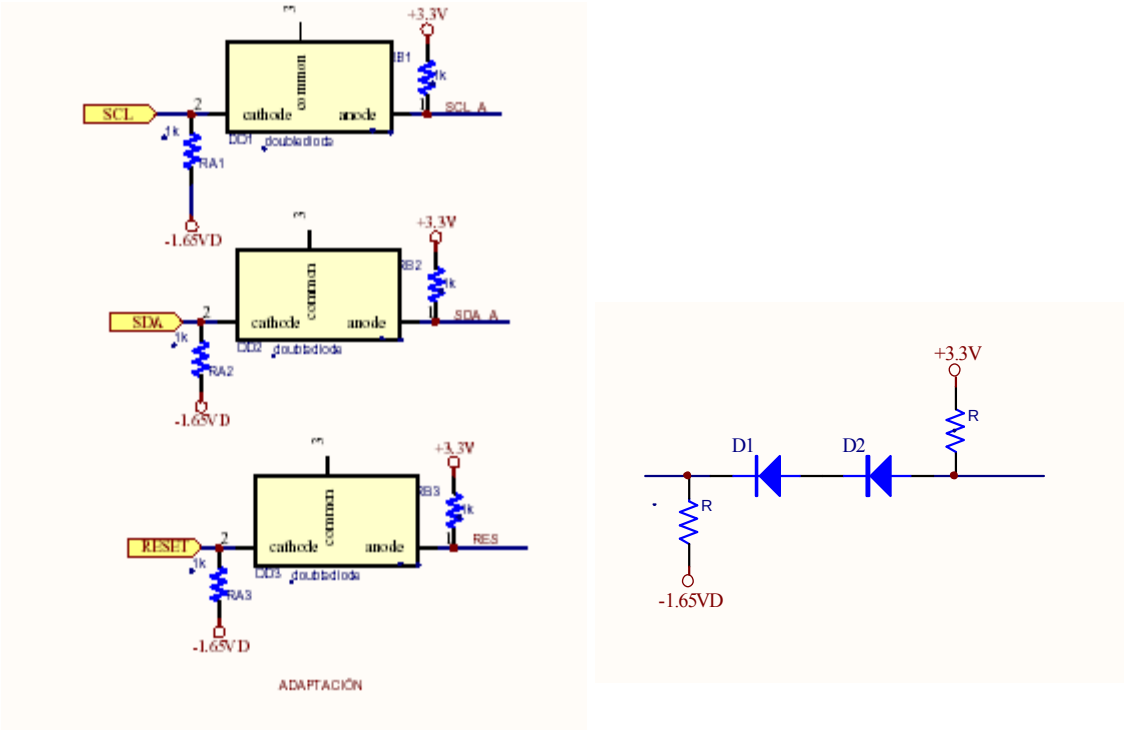

Figure 51. Schematics of Adaptation (left) and Detail of diodes (right).

Components powered by +1.65V/-1.65V:

- *ASICs*
- *Control Unit (FPGA)*
- *Clock Divider (FPGA)*
- *Threshold References (DAC, OPs, Reference and circuitry)*
- *Transceiver of the 20MHz Clock*
- *Components powered by +3.3V/GND:*
- *Substractor References (DAC, OPs, Reference and circuitry)*

- *Transceivers of the input stage (Clock and dI2C coming from Control Board)*
- *LVDS Serializers*

As the outputs of the ASICs have the first voltage levels and the inputs of the serializers need the second voltage levels, there are plenty of these adaptations. There are more than 70 adaptations, which imply a lot of passive components.

This adaptation was not implemented inside the ASICs because when it was decided to use these signal ranges, only one run of the ASICs left.

5.4.5. *Final PCB*

The final VFE Unit was separated in three cards. The Active Base was designed by people from LPC and it is not described in this point. The other two are: The ASICs Board and the Serializers Board.

The routing has followed the considerations depicted in 5.2.3.

ASICs Board

This board contains only the photomultiplier, the eight ASICs and their circuitry, the part of the threshold reference and the subtractor reference.

It is a ten-layer card, with components on both layers, top and bottom layer, class6 and made with FR-4. There are four planes for the different power supplies, a pair of layers for the clock signals, another pair for the analog signals and the last pair for the digital ones. Each of the signal layers has been refilled with a ground plane to prevent interferences or white noise. The figures below shows the signal layers of the card.

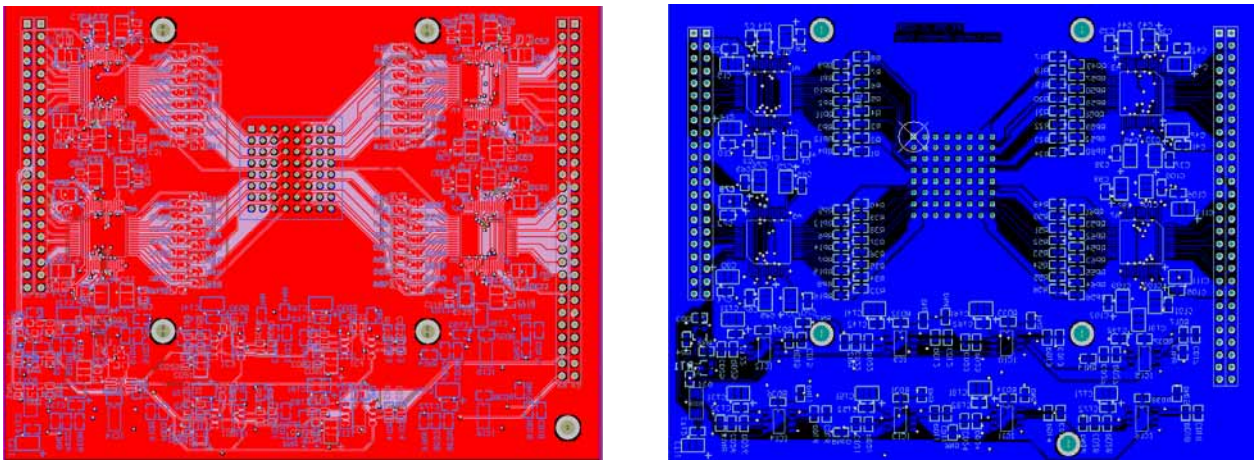

Figure 52. Left, Top Layer. Right, Bottom Layer

The Figure 52 depicted the top and bottom layer of the ASICs card. The position of the ASICs is important to minimise the lentgh of the analog traces from the photomultipliers. All these analog signals should have the same lentgh, the same delay, thus the ASICS are around the PMT at the same distance at top layer and in bottom layer.

In order to avoid the mixed signals, digital, LVDS or analog signals, the LVDS signals (the 20MHz clock) are separated in two layers (see Figure 54), the analogue signals such as the threshold reference and the subtractor reference are also separated in other pair of layers (see Figure 53).

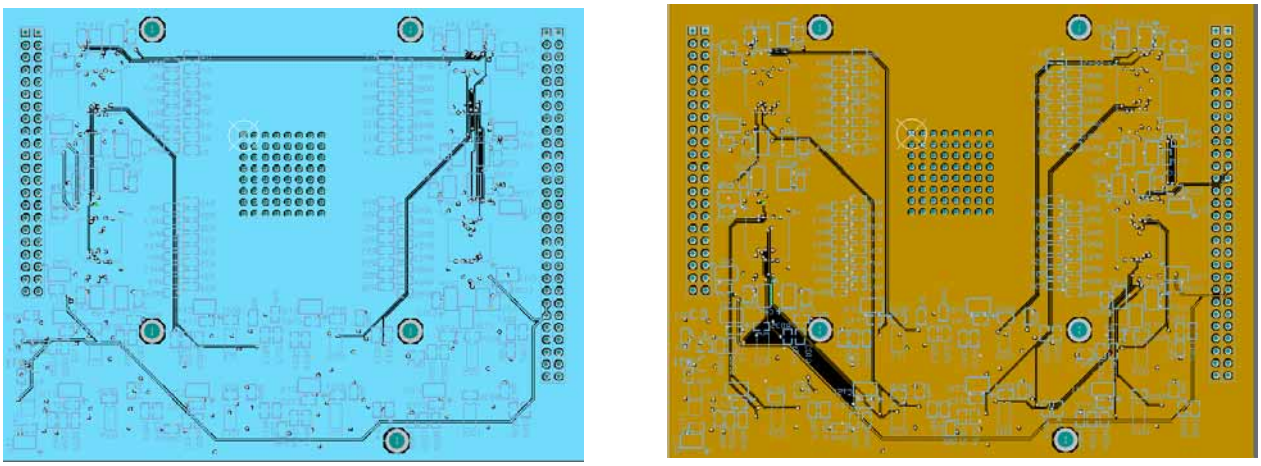

Figure 53. Left, Signal1 Layer. Right, Signal 2 Layer

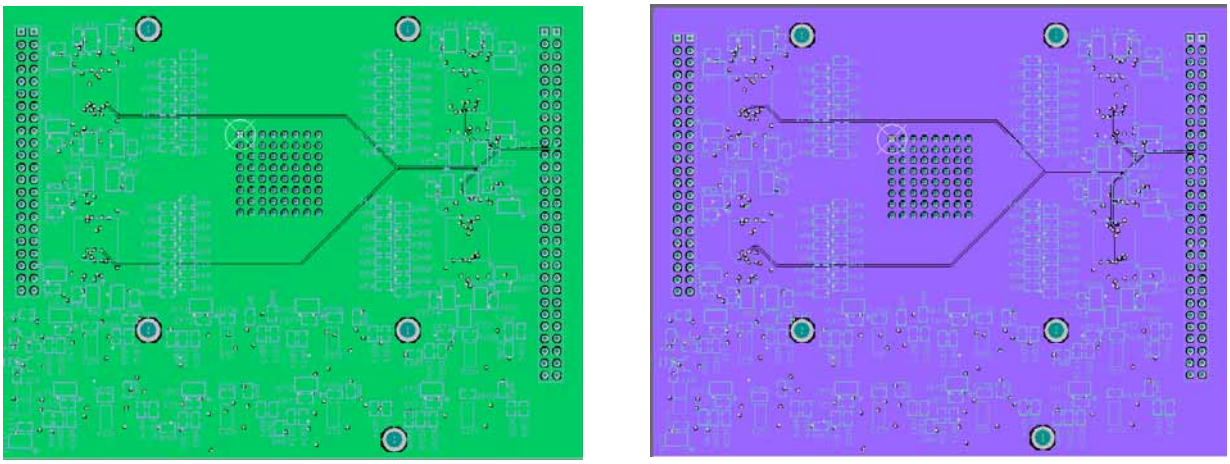

Figure 54. Left, Clock_H Layer. Right, Clock_L Layer

Input Stage/ Control Unit / Output Stage Board

The serializer board contains all the input stage (connectors, transceivers, and adaptation), the control unit (FPGA) and the output stage (asic's output adaptation, serializers and output high speed connector): The digital part.

The serializer card is a ten-layer card, with components on top and bottom layer, class6 and made with FR-4. Five planes for different supplies and five layers for signals, a pair of them for the LVDS, the other pair for the CMOS ones, and a layer for the differential pair of clock are used.

Next figures show several layers of the Serializers card.

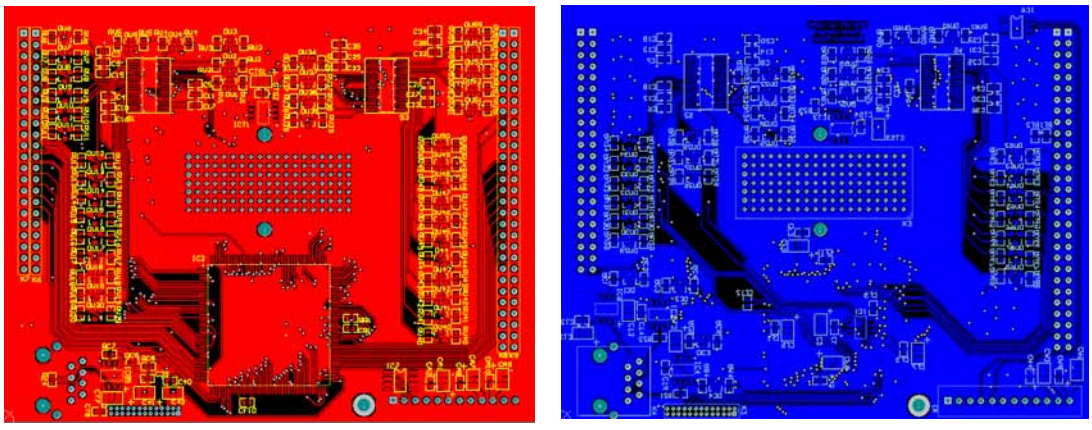

Figure 55. Left, Top Layer. Right, Bottom Layer. Both containing digital signals.

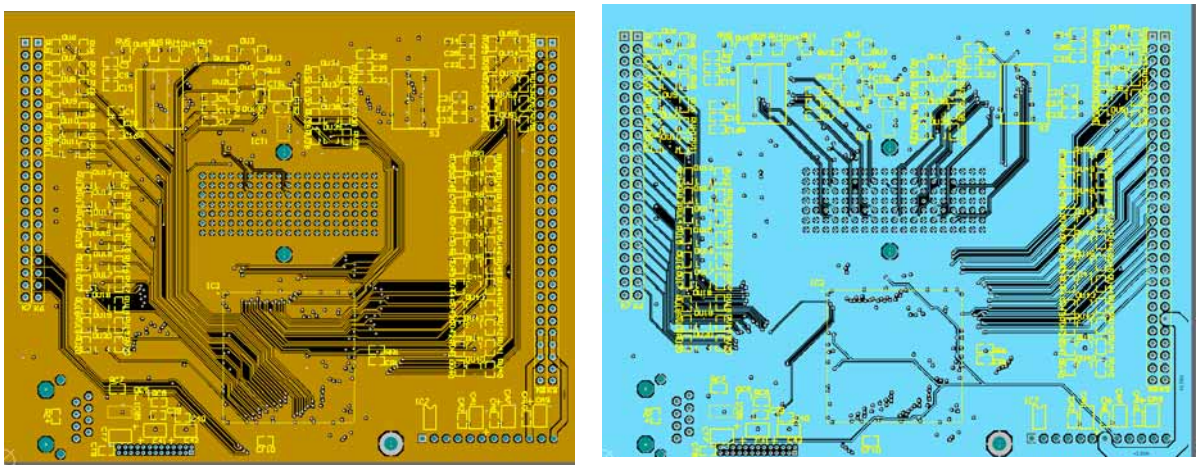

Figure 56. Left, Signal 1 Layer. Right, Signal 2 Layers. Both containing LVDS signals

In the same way as in the ASICs card, the routing tries to avoid mixed signals in the same layer. The Figure 56 right contains some digital signals, but in the center contains all the LVDS outputs to the hard metric connector. These signals should have the same length in order to avoid different delays (they are differential pairs at 280Mbit/s). The Figure 57 left shows the clock signals. Again the differential pairs should have the same length.

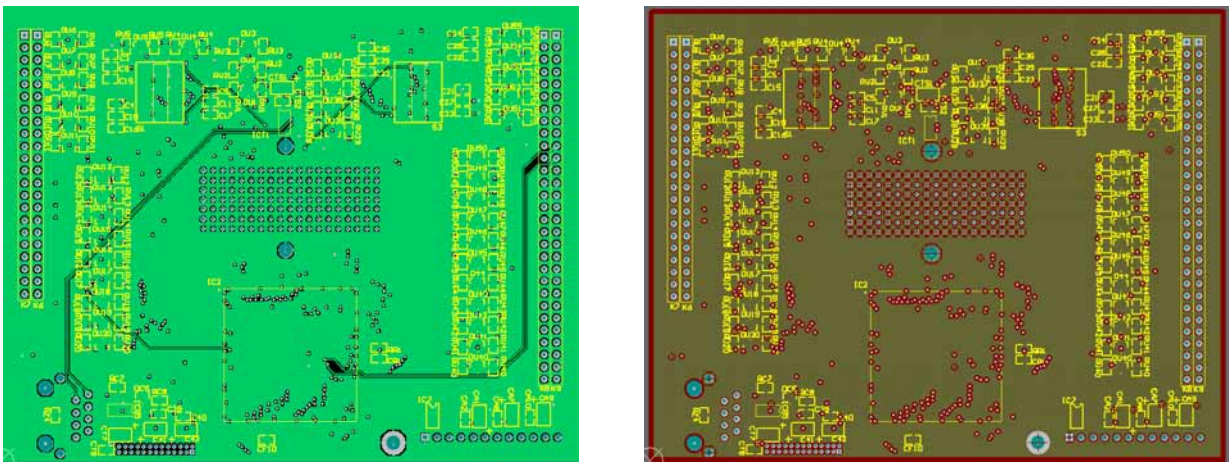

Figure 57. Left, CLK Layer. Right, GND Plane

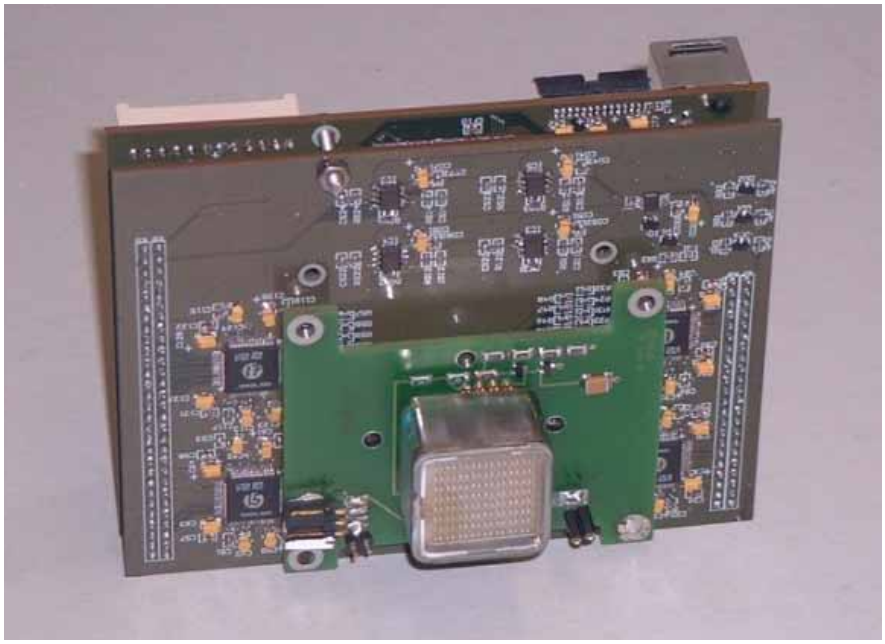

Figure 58. VFE's picture

Chapter 6: Tests and Results

Chapter 6. Tests and Results

6.1. Introduction

As it is mentioned in Chapter 2, the VFE Units are involved in a subdetector of a Calorimeter of LHCb. This fact implies that the definition of the specifications were a evolving and a long task. Final specifications were achieved three or four years after the beginning of the experiment, therefore a lot of changes had to be taken into account.

Belonging to a real experiment implies different kind of tests, not only the validation of the prototype but also the production of a series, mounting at the cavern and connecting to other subdetectors.

6.2. *Data Adcquisition Board (DAb)*

In order to make the most part of these tests, a dedicated setup was required. A setup formed by a card, which core is an FPGA (Altera Cyclone SmartPack) which implements the communication with VFE Unit, the deserialization of the output of the VFE and the communication with the PC environment, also created only for this purpose. A diagram block is depicted in Figure 59.

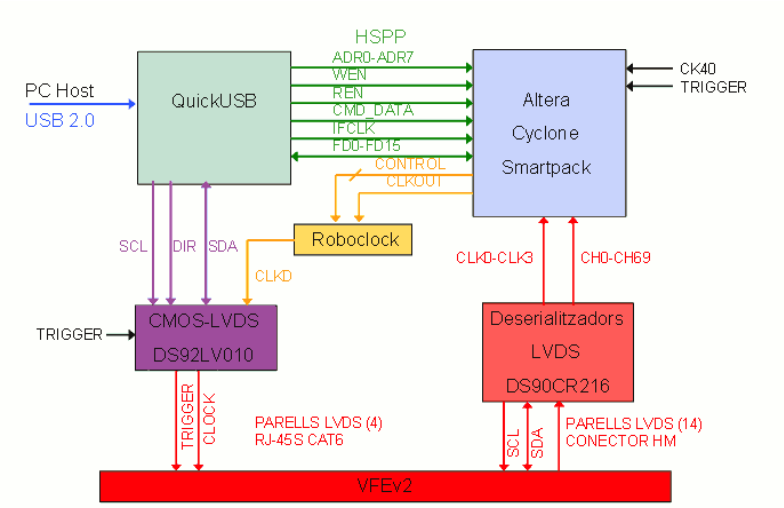

Figure 59. Diagram block of the Data Adcquisition Board for the VFE.

The main functionalities are:

- Emulating a DAQ for 64 channels.
- Emulating the Control Card in order to control the VFE Unit:
  - It has to emulate the experiment control clock with the possibility of having a delay (Using the Cypress Roboclock)
  - It has to emulate the I^2C differential bus that the VFE receives from the Control Card
- The interface with the PC is made by a USB commercial card (Quick USB of Bitwise) which gives:
  - A high-speed parallel port used in the communications with the FPGA
  - An I2C standard interface

6.3. Prototype Tests and Results

Four types of tests have been performed on the different versions of the VFE card: *Laboratory tests* in which the system is submitted to electrical probes measuring the good/bad performance of the card; *Test beams* in which the system performs the real data acquisition for a sample particle detector excited by a particle beam in a restricted area at CERN; C*ooling tests* in which the card is tested with a cooling system in order to achieve the proper temperatures for the integrated circuits; *LVDS tests* in which the 25meter distance link was tested.

6.3.1. Laboratory Tests

Functionality tests show the correct performance of the card. Each of the signals involved in any important function has to be tested. These measurements have been done by oscilloscope as it can be checked by the figures.

The items tested are:

- *Digital functionalities of the ASICs*

As it is explained In Chapter 4, there are some functionalities in the ASICs that are programmable such as the internal thresholds references for each subchannel. The signals: Scan In, Scan Out, CK and E are involved in this function. The signals between different ASICs in the same card are connected by Daisy Chain.

The figures below show these signals, which have correct values for ASIC performance, thus the rise and low time achieved are adequate values for a 20MHz clock processing.

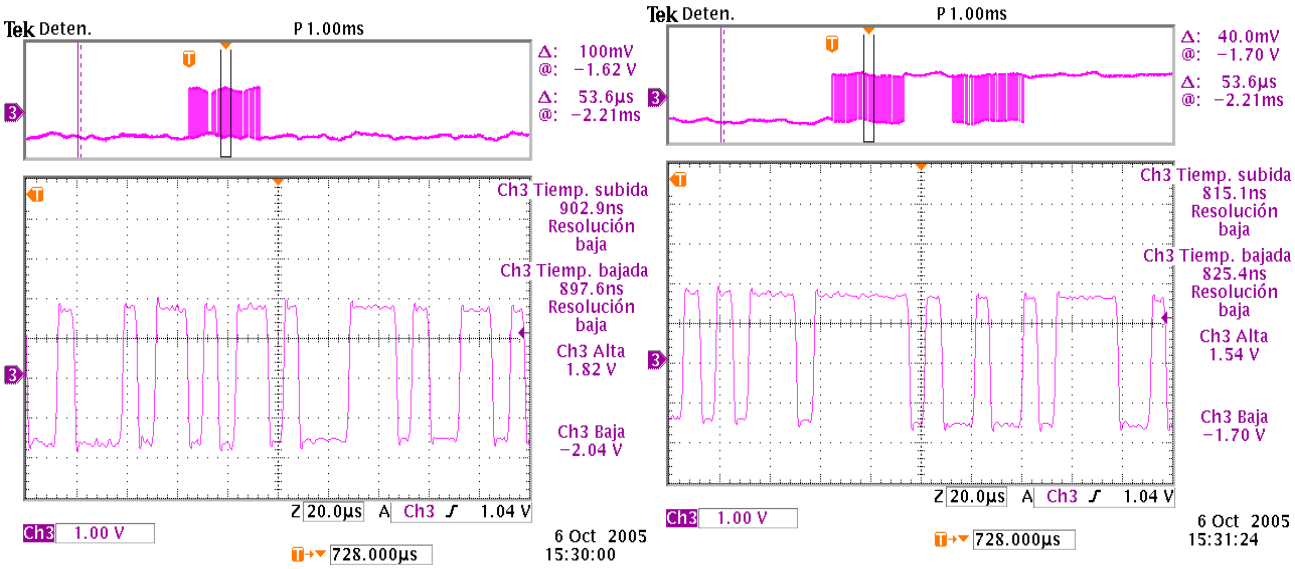

Figure 60. Scan in (left) and Scan Out (Right) fist ASIC.

The Figure 60 (as well as the Figure 61) has shown the behavior of the signals that control the digital part of the ASIC: Scan In, Scan Out, CK and E. The shape of the signals is good enough, and their functionality is accomplished. The measurement has been done by the oscilloscope in the unipolar mode. (These are not differential signals).

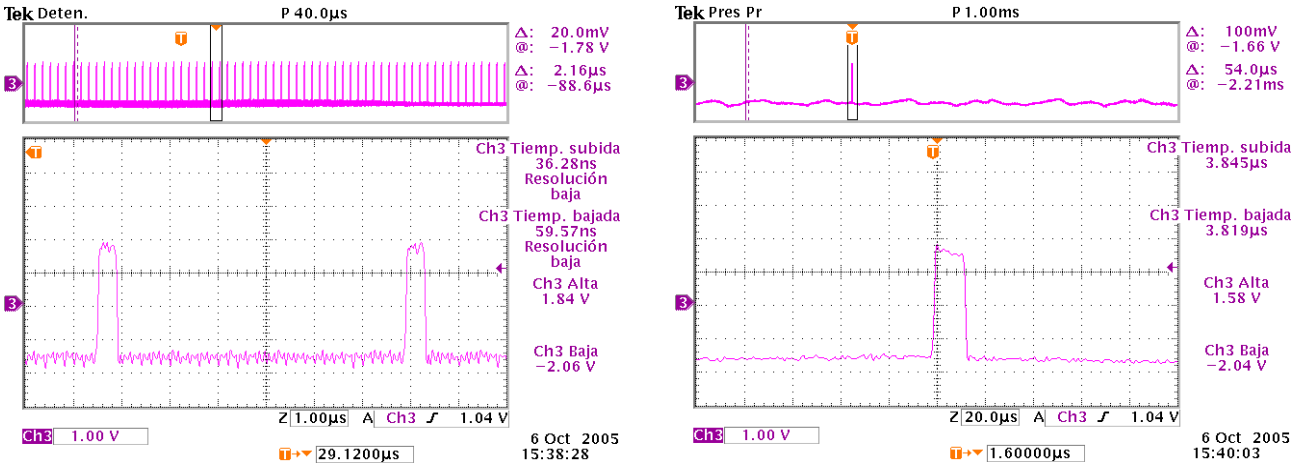

Figure 61. CK and E Signal.

- *Programming DACs:*

The two off-chip DACs are used to fix the external threshold reference and subtractor reference (pile up compensation). The interface to program DACs is I^2C bus. The signals of the bus (SDA, SCL) accomplish with the specifications required by the DACs: Setup and Hold Time.

Figure 62 depicted the I^2C bus between Control Unit and the DAC which controls the pile-up subtraction. It can be checked that the level adaptation in the power supply does not affect neither in the behavior nor in the shape. The measurement again has been done by the oscilloscope in common mode.

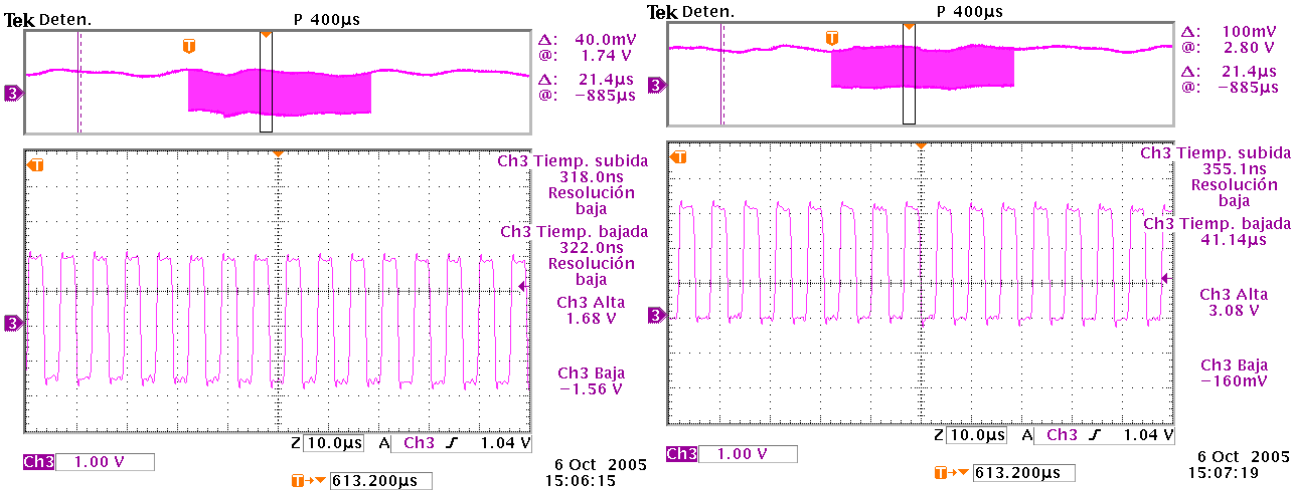

Figure 62. SCL signal going to DAC Vbias. Before (Left) and After Level Shifters (Right)

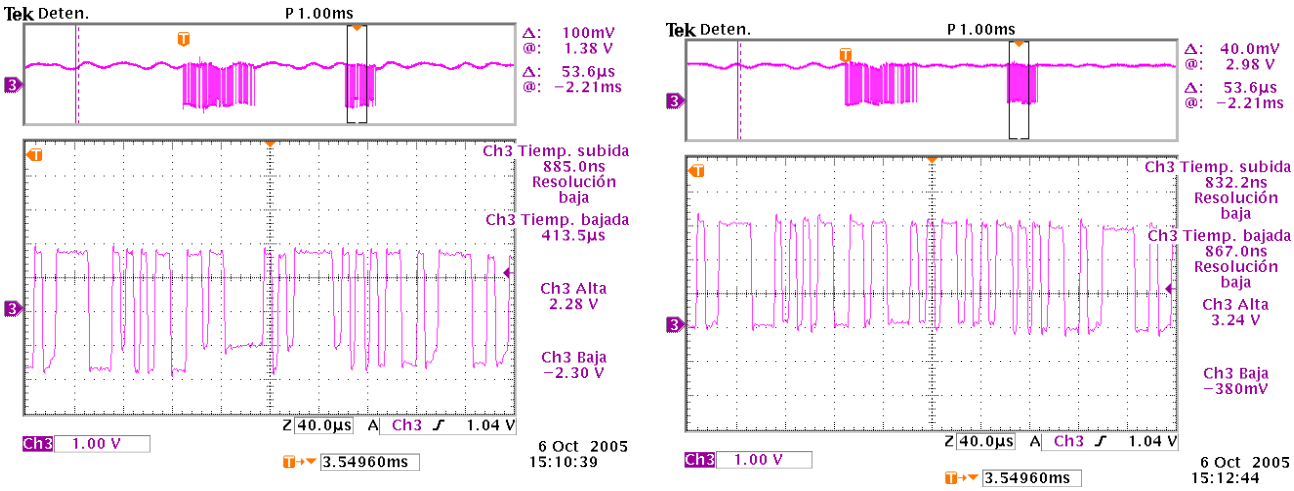

Figure 63. SDA signal going to DAC Vbias. Before (Left) and After Level Shifters (Right). Write and Read Access.

The same kind of test was made for the DAC which controls the reference for the threshold value. Figure 63 shows that the shape of the SDA as well as SDL signal is completely clear, accomplishing with the Setup and Hold time required by the DAC. The small ringing that it is shown by the figures in the level logic '1' does not affect because it is inside of the bandwith of the level '1' has in the DACs [48].

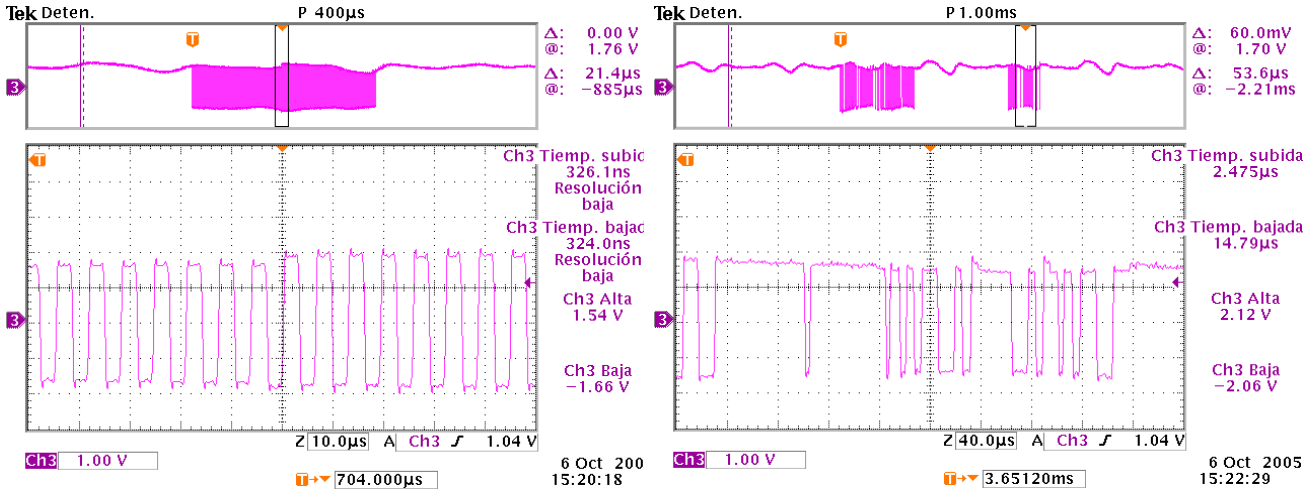

Figure 64. Left, SCL signal going to DAC Vref. Right, SDA signal going to DAC Vref.

- *Power consumption.*

As it is mentioned in the chapter before, VFE Unit is powered by a regulator card. These regulator cards are dimensioned for feeding up to seven VFE each one.

The current power consumption of a VFE Unit is showed in the Table 4:

Supply	Rshunt [mOhm]	Normal condition		Max switching (20 MHz)	
		DC [mA]	< RMS [mA]	DC [mA]	< RMS [mA]
+ 1,65 An	51	1431,37	29,41	1431,37	58,82
+ 1,65 Dig	600	150,00	2,50	418,33	2,50
-1,65 An	50	-1570,00	30,00	-1660,00	30,00
-1,65 Dig	400	-380,00	3,75	-665,00	3,75
0,85	1220	67,21	1,23	118,85	1,89
3,3 An	980	69,39	1,53	70,41	1,53
3,3 Dig	780	282,05	1,92	287,18	1,92
Gnd	980	-32,65	1,53	-32,65	1,53

Table 4 Power Consumption measured with a differential probe.

- *Mapping.*

Calorimeter is divided into a 6000 cells in order to have better granularity of the beam. This fact implies that each VFE Unit is associated to a location in the Calorimeter: Top or Bottom, A or C side. The outputs of the VFE Units go to PS FEB as the datapath explained in the Chapter 4. This fact implied that each channel of the SPD has to be distinguished from each other and has a unique position in the detector. In order to have more flexibility in the possible exchange of the VFE Units, different mappings had been defined, and they are programmable by the Control Unit of the VFE (the four mappings are depicted in Appendix 1).

This functionality was tested and it worked properly.

- *Noise.*

The maximum value of noise measured on the electronics is lower than the maximum value required by the Calorimeter's Electronics specifications (one LSB, around 12mV), described on Chapter 4. The histogram of Figure 65 has made with the information given by the measurements of noise for each card.

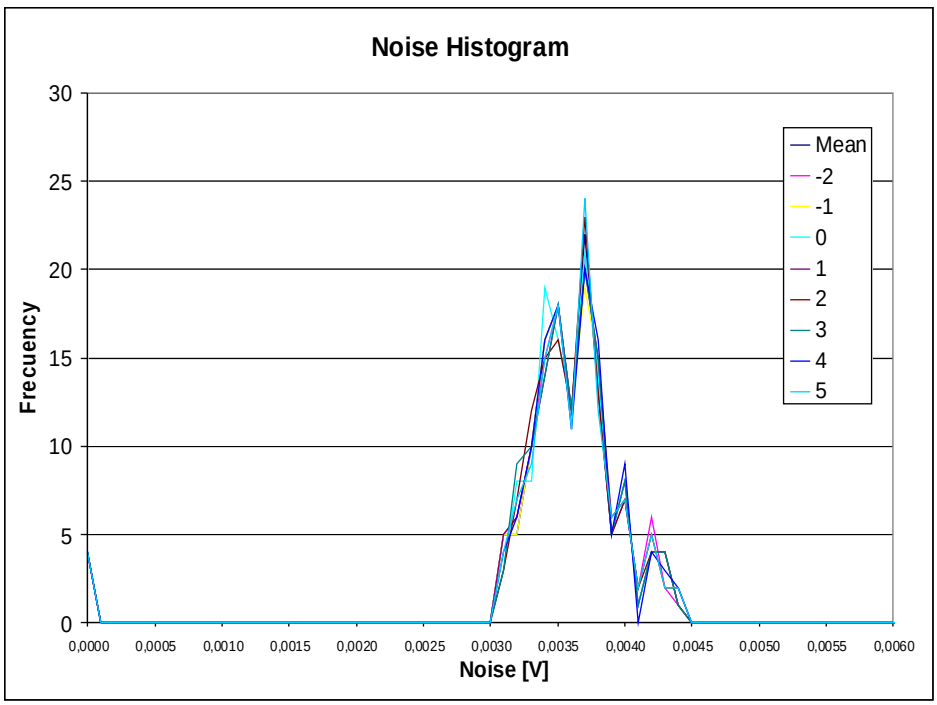

Figure 65. Noise measured without PMT

- *Interface with the Control Card*

All the signals which make the interface with the Control Card have to be tested. The shape of the signal has been checked in order to control the jitter, the skew and the shape.

The Figure 66 shows the behavior of the 40MHz clock proportionate by the DAb at the end of the cable without any compensation. The blue signal at top in both cases is the 40MHz clock source; the signal at bottom is the 40MHz clock measured at the end of the cable in differential mode or in common mode.

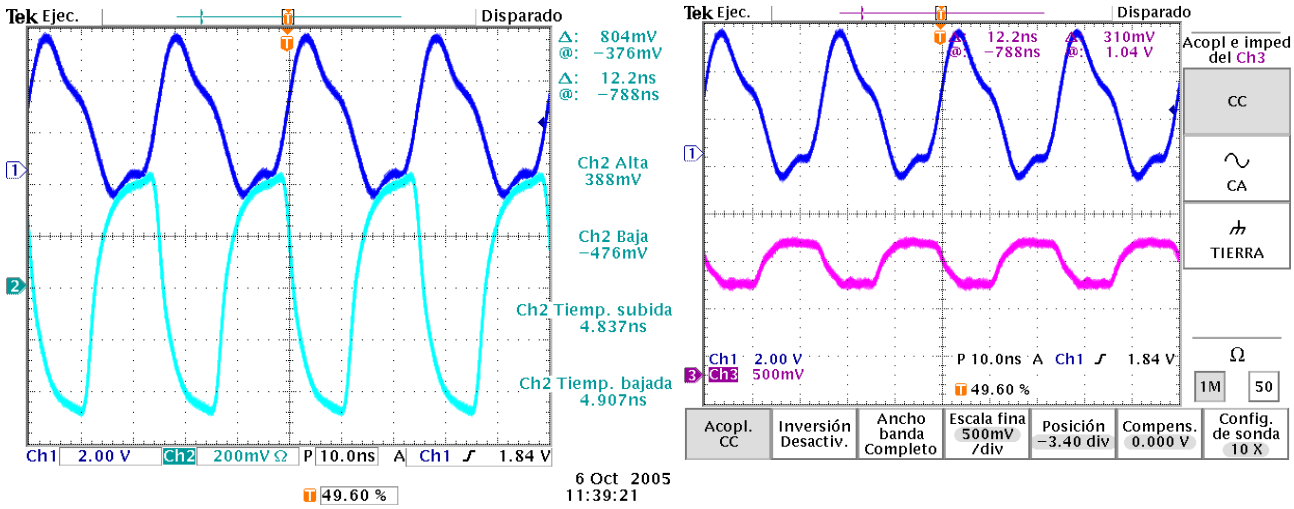

Figure 66. Differential Mode (Left) and Common Mode (Right). 40MHz clock measured at the end of the control cable without compensation

Figure 67 shows the Reset signal received also from the Setup Card emulating the Control Card. This signal is an LVDS differential and its shape has to be checked at the end of the control cable again. The plots had shown the proper shape of the signal before the power adaptation in the VFE Unit and after the power adaptation.

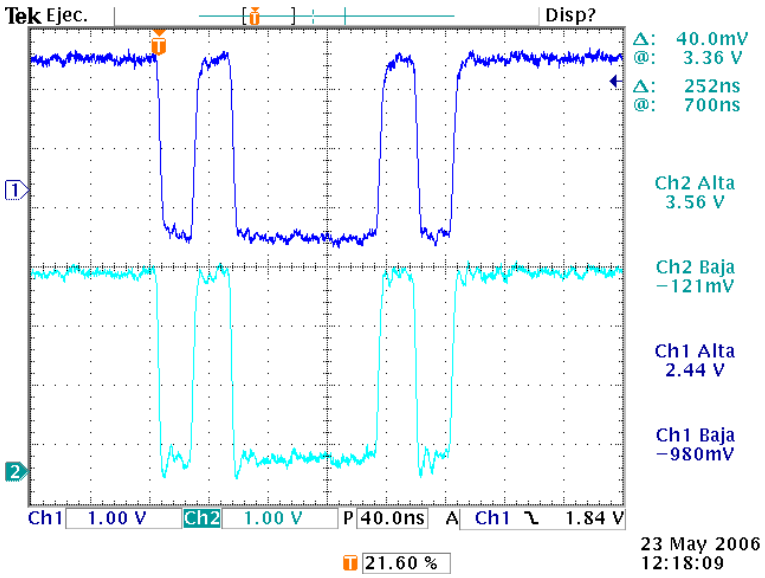

Figure 67. Reset by the differential pair before the power adaptation on Ch2 and after on Ch1.

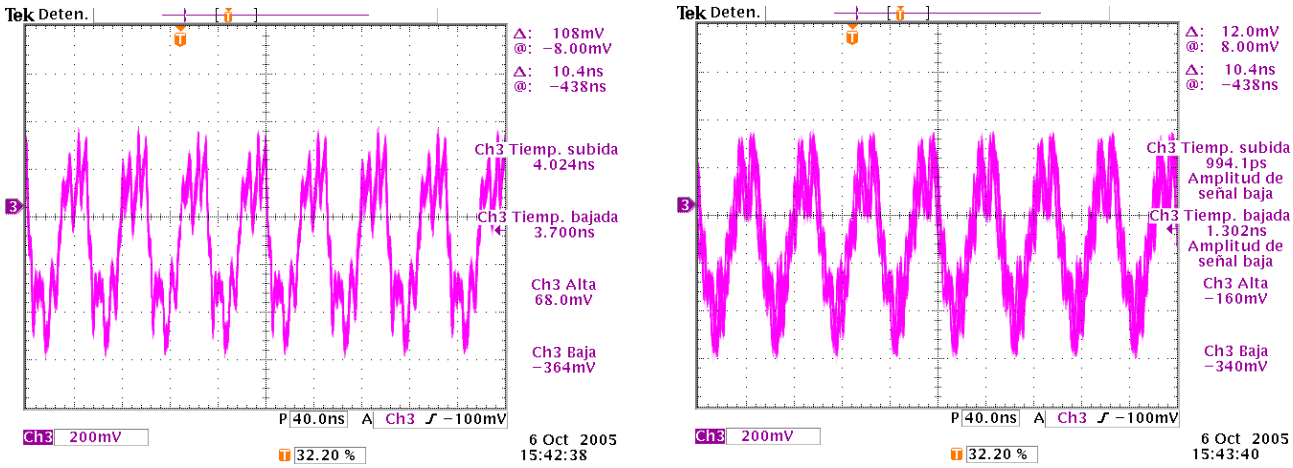

Figure 68. 20MHz Clock measured after transceiver. Clock high left, clock low right.

The shape of the 20MHz clock outing of the FPGA has to be checked. The output of the FPGA is a common mode and it has to be transformed in a differential signal to avoid noise, interference… and this transformation is made by an LVDS transceiver. The Figure 68 shows the shape of the signal at the output of the transceiver. The measurement has been done in a no differential mode. The Figure 69 shows the measurement in a differential mode.

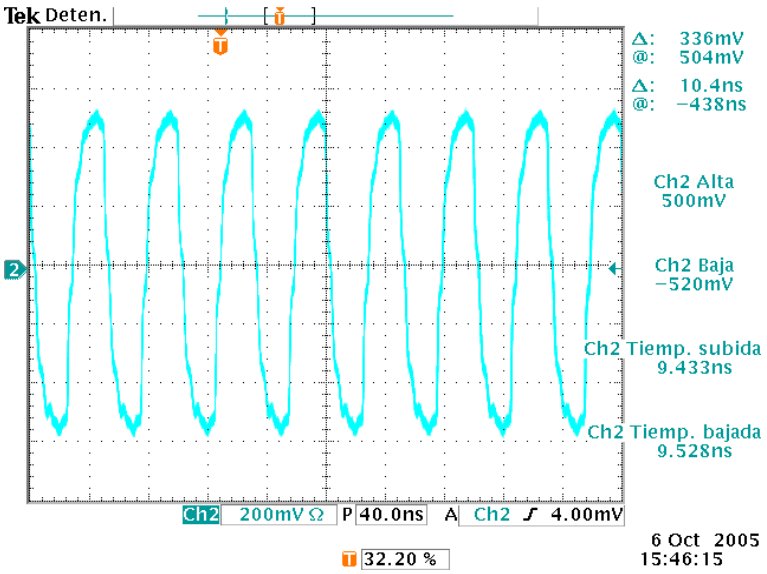

Figure 69. 20MHz clock measured in a differential mode.

- *I2C signals*

Now, the I^2C differential bus is tested. Again, the shape of the signals has been checked in order to control the shape. The Figure 70 shows the performance of write access (left) and read access (right) for the SDA signal. The measurement has made in a differential mode at the end of the control cable. It can be checked the right shape in both access. Undershoots are due to the FPGA acknowledge.

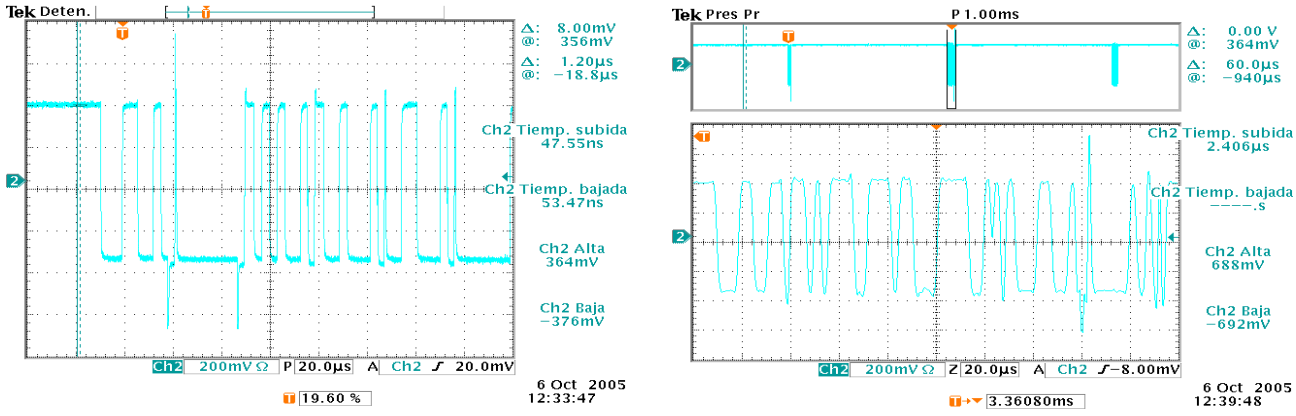

Figure 70. Differential Mode. SDA differential signal at the end of the control cable. Write Access (Left) and Read Access (Right).

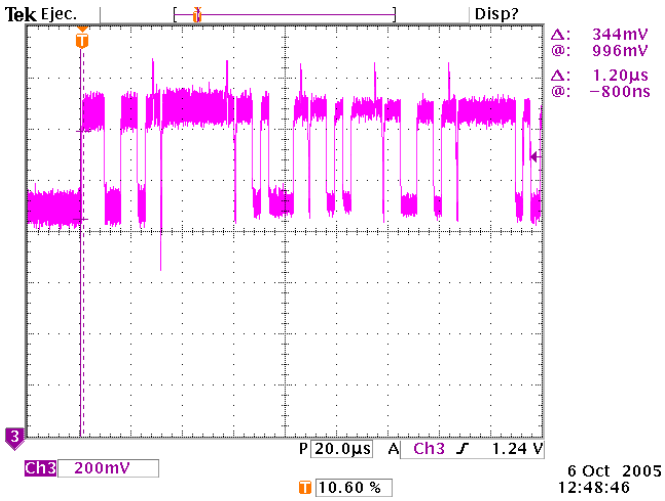

Figure 71. Common Mode. SDA differential signal at the end of the control cable measured on the RJ45.

The Figure 71 shows the common mode for the SDA signal. Again, the shape is good. Figure 72 shows the same test for SCL signal in differential mode and in common mode.

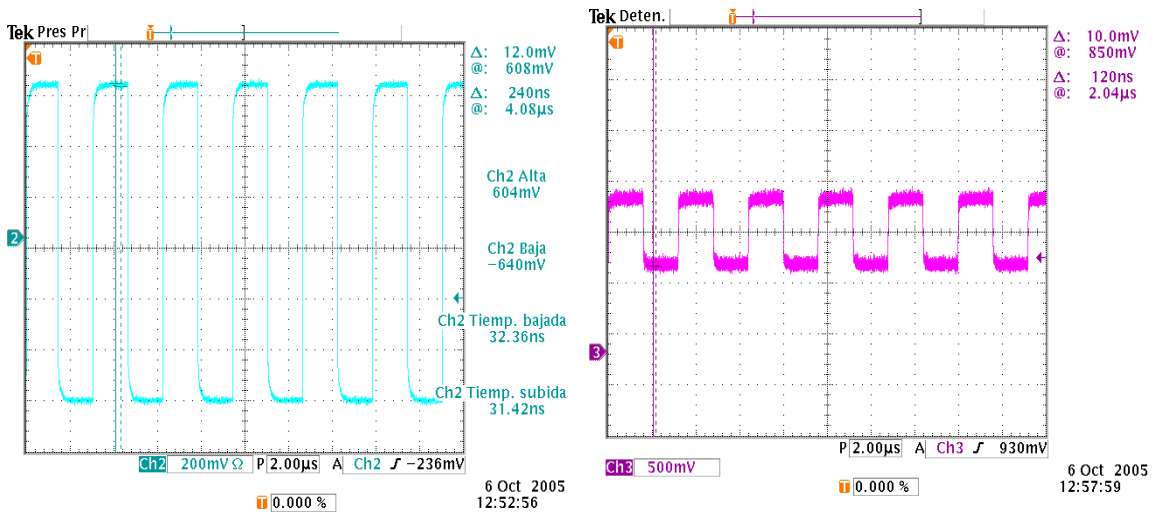

Figure 72. Differential Mode (Left) and Common Mode (Right). SCL differential signal at the end of the control cable measured on the RJ45.

- *Input and Output Data in the FPGA*

It is important to take into account the setup time and hold time in the receiving data from ASICs and the output data to Serializers at 40MHz clock. Figure 73 and

Figure 74 evaluate the setup and hold time of data at the output of the ASICs (input of FPGA) and the output of the FPGA later than the level shifters (input of serializers). Each figure shows that when the clock rises (pink), the data is stable.

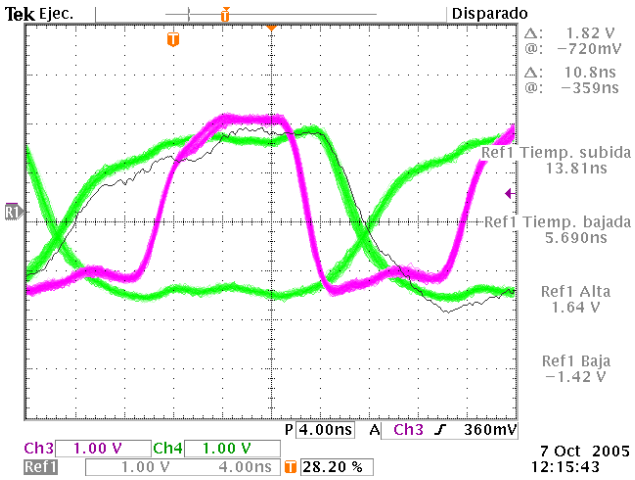

Figure 73. Setup and Hold Time on one output of one ASIC (Input of FPGA). Clock of 40MHz.

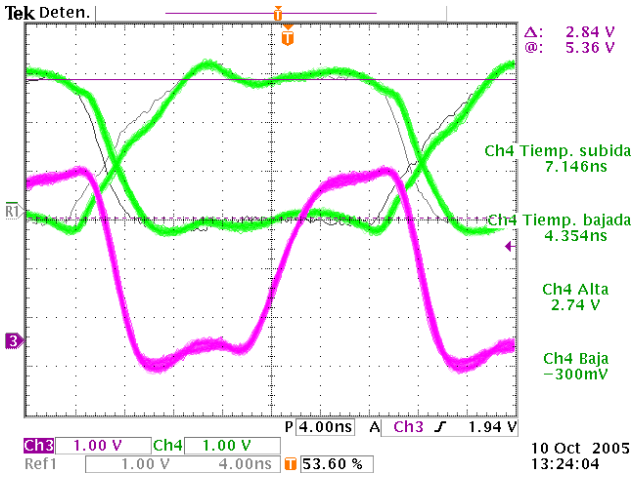

Figure 74. Setup and Hold Time on one output of FPGA (Input of Serializer). Clock of 40MHz.

- *Power On the FPGA*

The power on of different power supplies of the FPGA have to follow a significant order to start properly. Figure 75 shows the order accomplishing the time required between power supplies. If the delays between different power supplies are

not accomplished, the device coud have possible malfunctions or also it can be destructed internally.

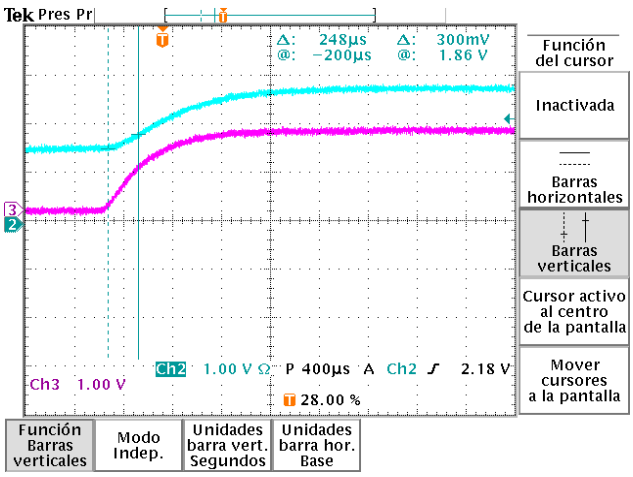

Figure 75. Power On of FPGA measured with a differential probe.

6.3.2. *Validation Protocol*

For the acceptance of the VFE prototype a validation protocol was defined. The tests involved in this protocol were:

1. Digital functionality of the FPGA (A flash-based FPGA): tests such as write and read asic registers, write and read dacs for vref for the internal thresholds and the amount of pile-up subtraction (via local I2C bus), checking and correction of ASIC's SEUs, DAC's SEUs, Clock Reset, Dacs Reset... This part is in charge of checking the funcionality of the most of the components of the VFE Unit. It was a good test to check the soldering of ASICs and DACs.
2. LVDS link: The FPGA is programmed by a known LVDS sequence, and it sends the sequence by the LVDS link. This test is very useful to check the path between FPGA and the output of the VFE Card: the level adaptations and the serializers.
3. Vref and Vbias Calibration. Each VFE has to be calibrated in order to find the best results of the reference for thresholds and for pile-up subtraction. This

test consits on make a sweep of all the values of the Vref and Vbias and check the results: the values should have an increasing order.

4. Offset and Noise measures without injecting any signal (from a photomultiplier or a special circuit designed for injecting signal). This test consists on making a sweep of all the possible values of the thresholds in order to check the transition that the channel must have. It is also useful to check possible dead channels due to the soldering, possible malfunctions and check the noise and the offset, as its name.
5. Injecting signal in the card. It is the same test as 4, but injecting signal in the card. This test is the last test, it is useful to check the whole path, from the MAPMT to the LVDS output. It also checks the ASIC functionality.

6.3.3. Test Beam Tests

Test Beam Tests were made at CERN. Its main goal is testing the electronics at the closest conditions of the experiment as possible. Several test beams were done in different prototypes:

Sep 2001: ASIC RUN 2, 4 full channels/ 4-layer board. The functionalities to test were:

- ECL vs. CMOS output
- Clock signal distribution
- Power Supply distribution

June 2002: ASIC RUN 2, 4 full channels / 4-layer board. The functionalities to test were:

- Improvements in board design
- Signals distribution

June 2003: ASIC RUN 3, 1 full channel and digital control/ 6-layer board. The functionalities to test were:

- Digital signal distribution vs. analog signal distribution
- Noise effect vs. number of layers

Figure 76 shows the set-up of the tests on this test beam at CERN.

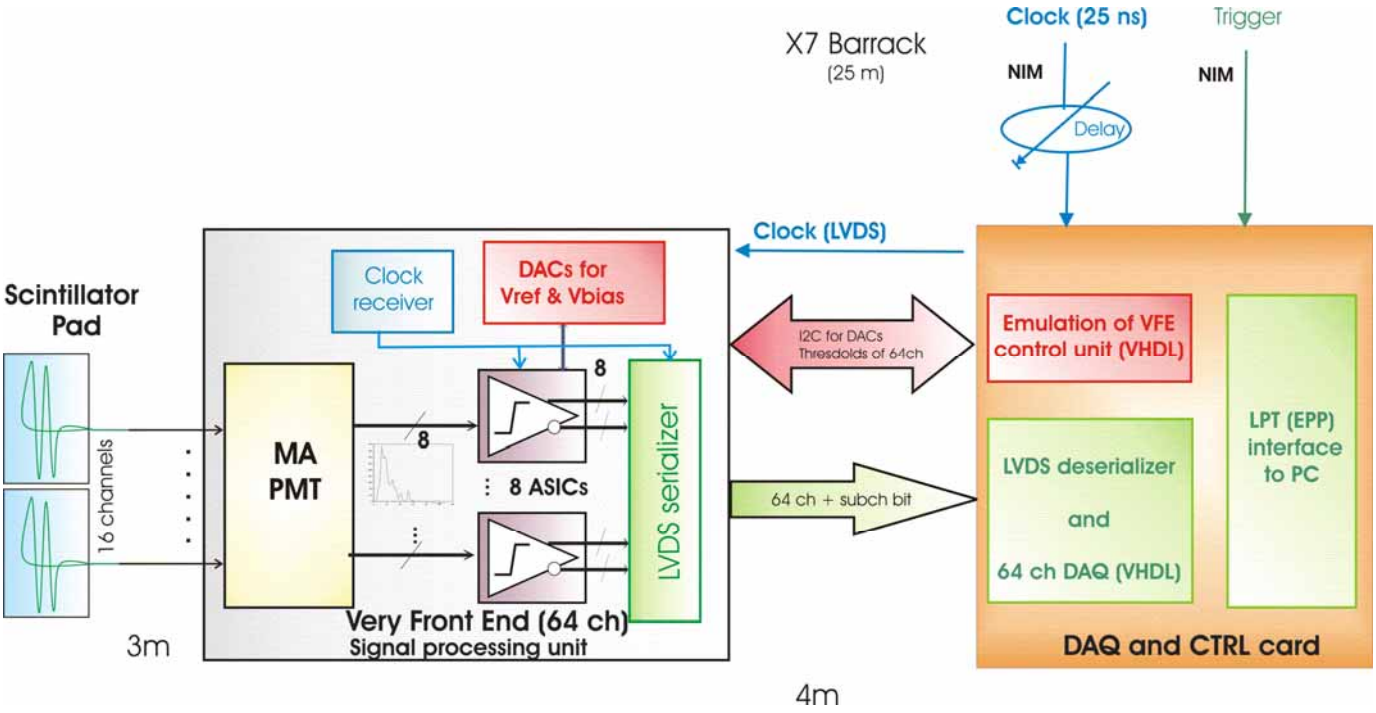

Figure 76. Test Beam Diagram Block

Next pages contain some of the results achieved in this test beam.

- *Signal Shape: Distribution in different clock periods*

Scenario: Using beam C. The PMT high voltage was set at 700V. These tests were made with whole signal and a fraction of signal. T0=76%, T1=19%, T2=4% and T3=1%.

The next figure shows the results obtained in the transition of '0' to '1' for a whole signal and for a fraction of signal. It could be checked that the signal has a tail in the next clock period.

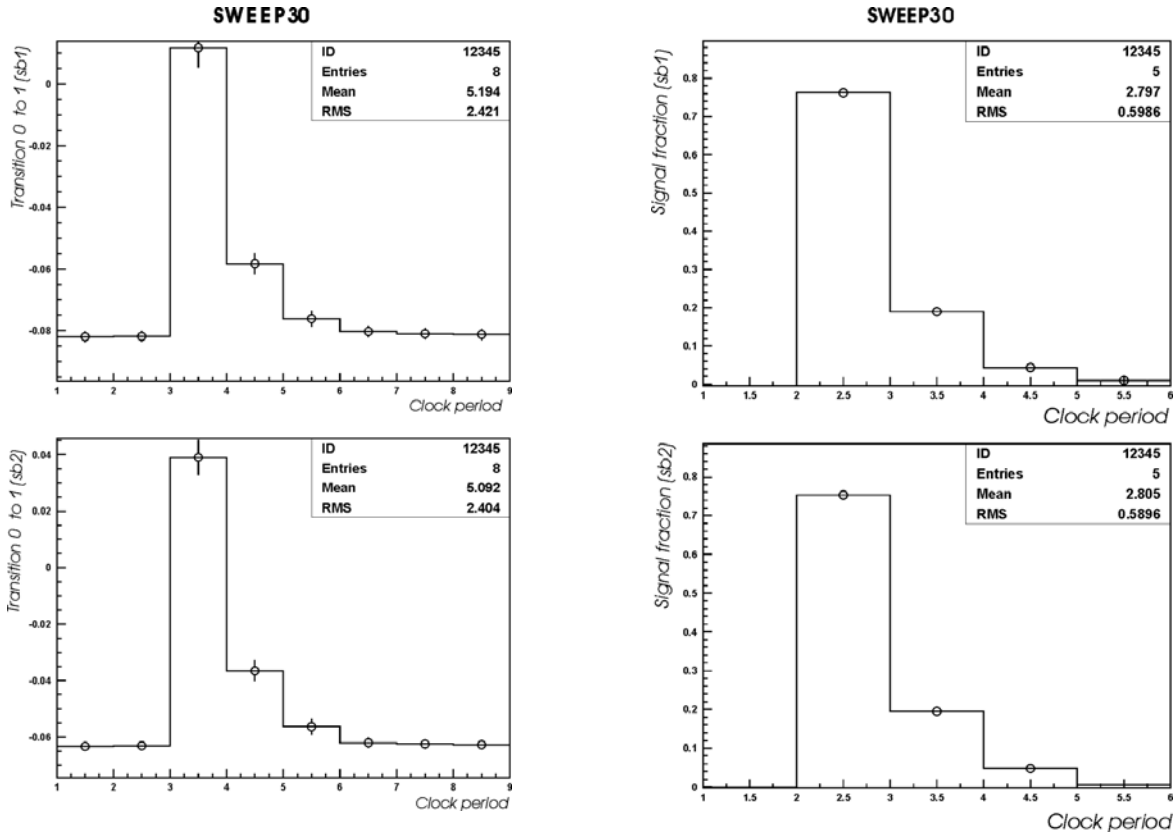

Figure 77. Results of signal shape

- *Photo statistics*

Two different scenarios were tested in order to know an approximation of the photostatistics.

1) MIP Signal: MIP signal of SWEEP30 (beam C. PMT at 700V)

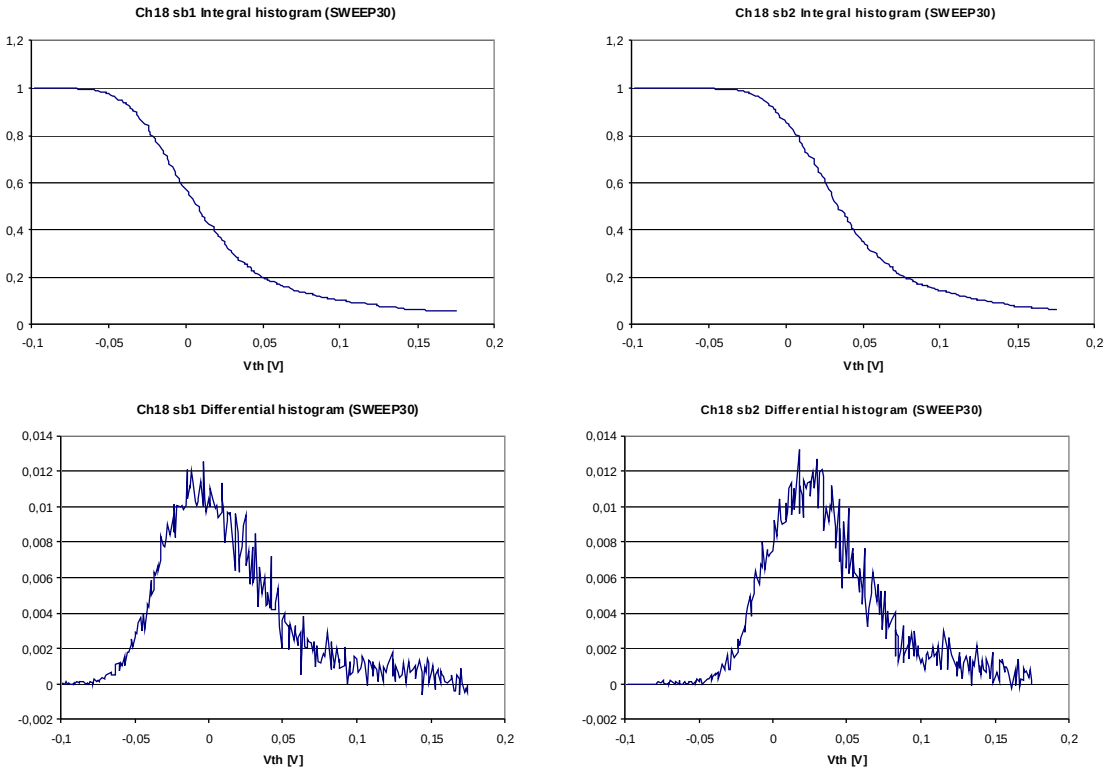

Figure 78. Photostatistics Results

The Figure 78 shows several plots of a sweep of the threshold value.

1) nphe (method1)

Assuming that light yield follow a poisson distribution:

$$nphe = \frac{\left(\left(\mu_{T0}-\mu_{ped}\right)+\left(\mu_{T1}-\mu_{ped}\right)+\left(\mu_{T2}-\mu_{ped}\right)+\left(\mu_{T3}-\mu_{ped}\right)\right)^2}{\left(\sigma^2_{T0}-\sigma^2_{ped}\right)+\left(\sigma^2_{T1}-\sigma^2_{ped}\right)+\left(\sigma^2_{T2}-\sigma^2_{ped}\right)+\left(\sigma^2_{T3}-\sigma^2_{ped}\right)}$$

Result: nphe ≈ 11 (for SWEEP30 and SWEEP102)

2) nphe (method2)

Gain of PMT ch11 at 700 V (50000) and chip with 470Ω (1.1 mV/fC) is known. Therefore:

$$nphe = \frac{S/G_{chip}}{G_{PMT}q} = \frac{S}{9.3} \approx 13$$

(Where 'q' is electron charge and 'S' is the MIP signal in mV for T0+T1+T2+T3).

Result: Nphe is about 16.

- *Signal for different HV*

1) MIP Signal: Beam B. SWEEP46 to SWEEP 51.

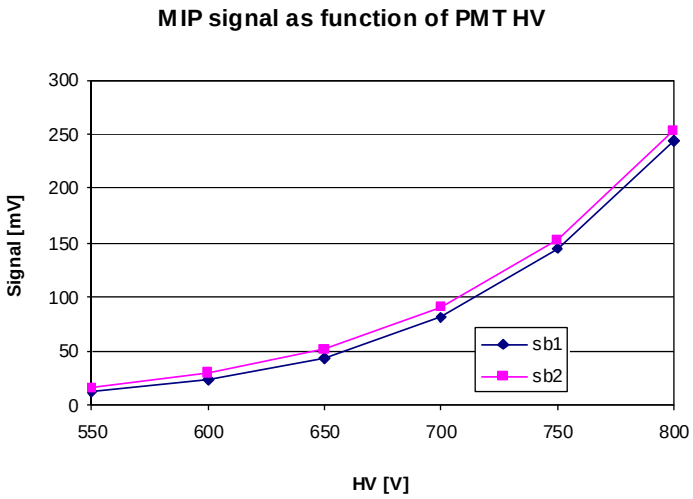

Figure 79. PMT Gain

2) PMT Gain estimation

Beam B. SWEEP46 to SWEEP 51. PMT estimated taking 11 phe

The Figure 80 shows a comparison with results at Barcelona test bench.

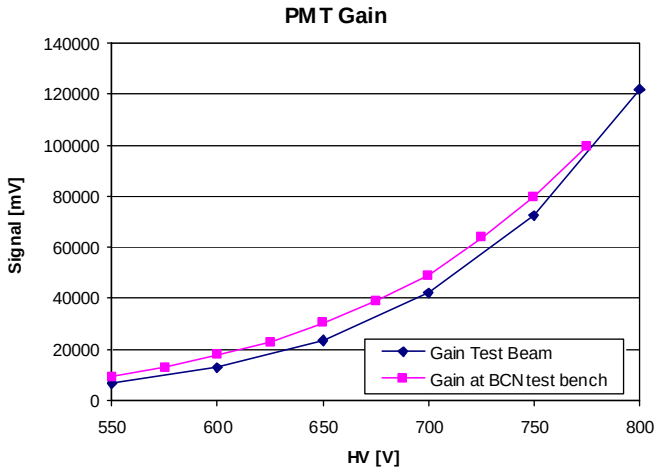

Figure 80. Results comparison

As a preliminary conclusion at this test beam, the system worked properly at test beam scenario, its functionality was correct and nothing seems not to work. Results obtained showed that any significant change had to be performed in the prototype.

6.3.4. *Cooling tests*

Cooling tests took place in Clermont-Ferrand at LPC (Laboratorie Physique Corpuscoulaire) between July and September 2005.

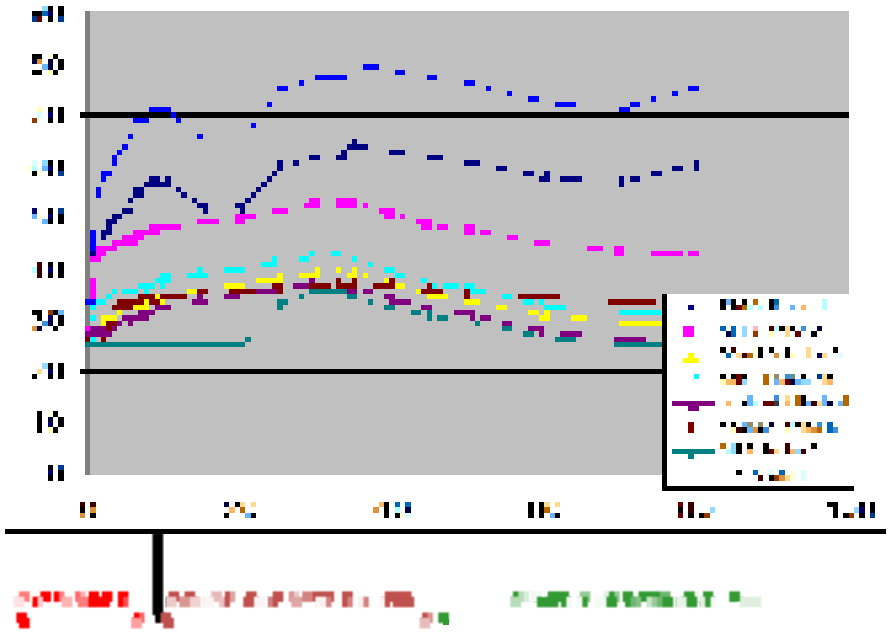

Figure 81. Cooling Results (X's: minutes, Y': º Celsius)

The results showed, see Figure 81, that the maximum temperature achieved with a low water pressure is close to the limit of the maximum value of temperature of the FPGA (80ºC). When the water pressure grows, the temperature is lower. By this way it could be checked that the mechanics design for the cooling was good enough and it was not necessary to put more aluminium material in the middle of the cards.

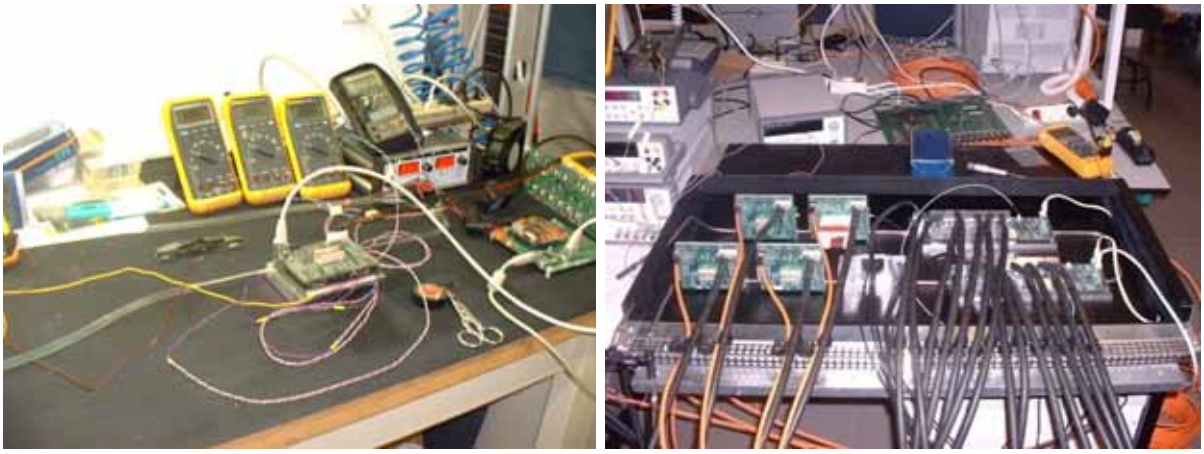

Figure 82. Cooling Test at LPC on 2005, left. Cooling Test at UB on 2006, right.

The previous figure shows the setup for cooling tests. The left plot shows a stand-alone test made by several temperature probes situated in different points of the prototype, and checking the temperature each five minutes. The right plot shows a cooling test of one full box emulating the real experiment.

6.3.5. LVDS Tests

Introduction

The 64 channels plus 1 half channel bit a SPD VFE unit should be sending to a FE card as it is described in Chapter 3. This data arrives to the FE cards through a rear connection in the backplane: very little space is available. Therefore, data will be serialized (multiplexed in time) in order to save space for interconnection and cabling.

As we explained in Chapter 4, there are a skew and jitter restriction for the proper performance of the link, and several cables were tested in order to achieve these requirements.

Cables to be qualified

The 4 twisted pair cables used for LAN (Ethernet) is the best candidates for price and availability. Each link will need 4 cables.

Another important characteristic is choosing between rigid and multifilar cables. The first ones are used for vertical cabling on LAN and have smaller attenuation than the multifilar ones, used for short patch cables. Patch cable are not usable due to his high attenuation at 30m and 150MHz.

The delay skew between cable pairs and the skin effect has been studied in 2003 and in 2004 for several commercial cables; the best candidate was the category 7 cables (LANMark) from Nexans.

The Nexans factory in Santander has developed a special prototype for the SPD trying to minimize skew.

The construction is similar: STP (pair shield + global shield), 100Ω impedance and 23 AWG. However total thickness (diameter) of LANMark is 8 mm vs. 10 mm or the prototype.

Test Set-Up

For the skew measurements a CMOS pulse is converted to 16 LVDS pulses.

Eye diagrams and other oscillograms are measured with the TDS7154B[10] (1,5 GHz, 20GS/s in real time and 1TS/s in repetitive mode) and a differential probe (1 GHz).

A Bit Error Rate (BER) test system is developed in VHDL using Cyclone PGA.

The picture below shows the test set-up:

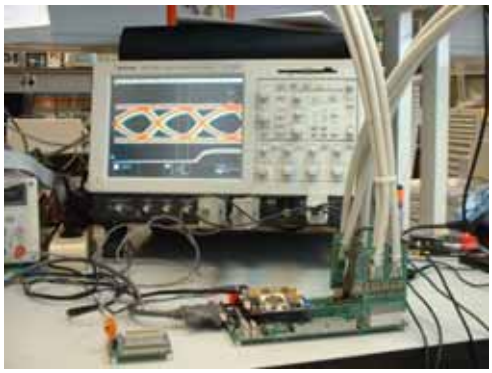

Figure 83. LVDS Set up picture

[10] *TDS7154B is an oscilloscope*

The BER test system consists on injecting some known patterns in the cable, and once the pattern is received, the sent pattern and the received pattern are compared. It is depicted in Figure 84.

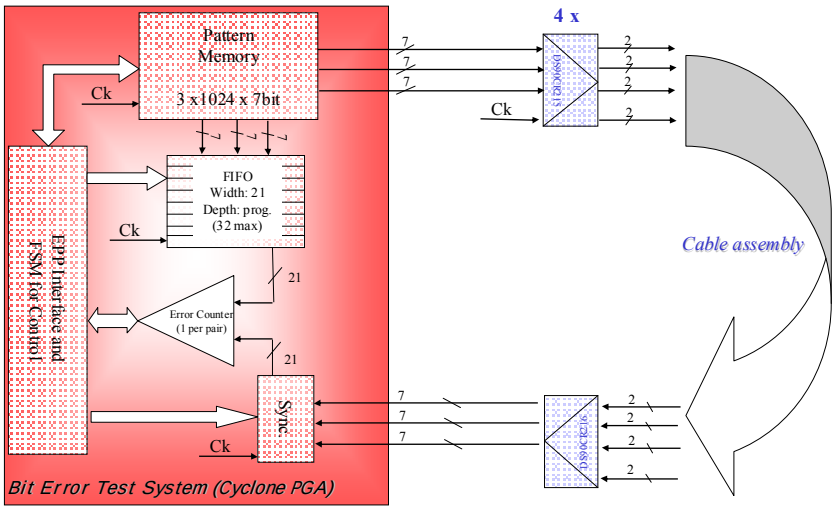

Figure 84. Diagram block of LVDS Test Setup

Driver Signal

Some pictures of output signal at the DS90CR125 over 100 Ω.

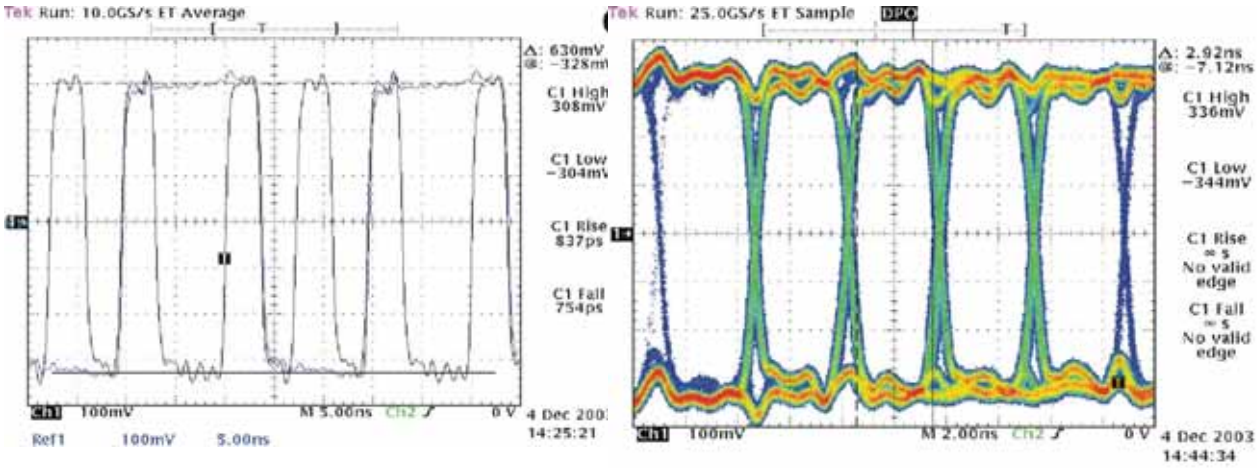

Figure 85. Output signal al LVDS multiplexer over 100Ω

Conclusions:

The dynamic output impedance of the driver considered as a current source is studied. According the Table 5 levels are right, just the voltage is almost linear with

resistance, except for 200 Ω where small attenuation is seen. In the signal shape for a load of 200 Ω a fast slope up to 400 mV is observed, followed by a slower rising (about 5ns).

	VoD high	***VoD low***
50 Ω	+ 158 mV	- 170 mV
100 Ω	+ 324 mV	- 328 mV
200 Ω	+ 604 mV	- 608 mV

Table 5 Different output impedance at LVDS link.

Skew measurements and compensation

Maximum difference between pairs (delay skew) has been measured for 4 cables of 30 m cable of each type:

	Skew 30 m [ps]	**Average Skew for 30 m [ps]**	**Average Skew/m [ps/m]**
LANMark	460 65 300 520	***340***	***11***
Prototype	740 690 900 820	***790***	***26***

Table 6 Cable characteristics at LVDS link

LANMark fulfils requirements and the prototype is close but does not reach 500 ps skew for 30 m.

Frequency Components Estimation

Signal after cable r(t) is considered to be the convolution of an "ideal" fast and arbitrary signal b(t) and the cable effects r(t): r(t)=b(t)*h(t). Method described in [38].

h(t) is approximated by several exponential decays.

On that case it is possible to calculate the inverse transfer function of cable load effects: $\hat{h}(t)$

It can be realized using a passive filter using a finite number of elements.

$$H(s) = 1 + \sum_{i=1}^{n} \frac{\alpha_i a_i}{s + a_i} = \prod_{i=1}^{n} \frac{s + b_i}{s + a_i}$$

$$\hat{H}(s) = 1 - \sum_{i=1}^{n} \frac{\beta_i b_i}{s + b_i} = \prod_{i=1}^{n} \frac{s + a_i}{s + b_i}$$

To estimate the filter parameters the step $\bar{r}(t)$ response is measured.

$$C(t) = 1 - \bar{r}(t) = b(t) + \sum_{i=1}^{n} q_i e^{-a_i t} \quad and \quad b(t) = q_0 e^{-a_0 t}$$

The step response (Figure 86) for 4 types of cable tested has been fitted to obtain a first order compensation:

$$C(t) = q_0 e^{-a_0 t} + q_1 e^{-a_1 t}$$

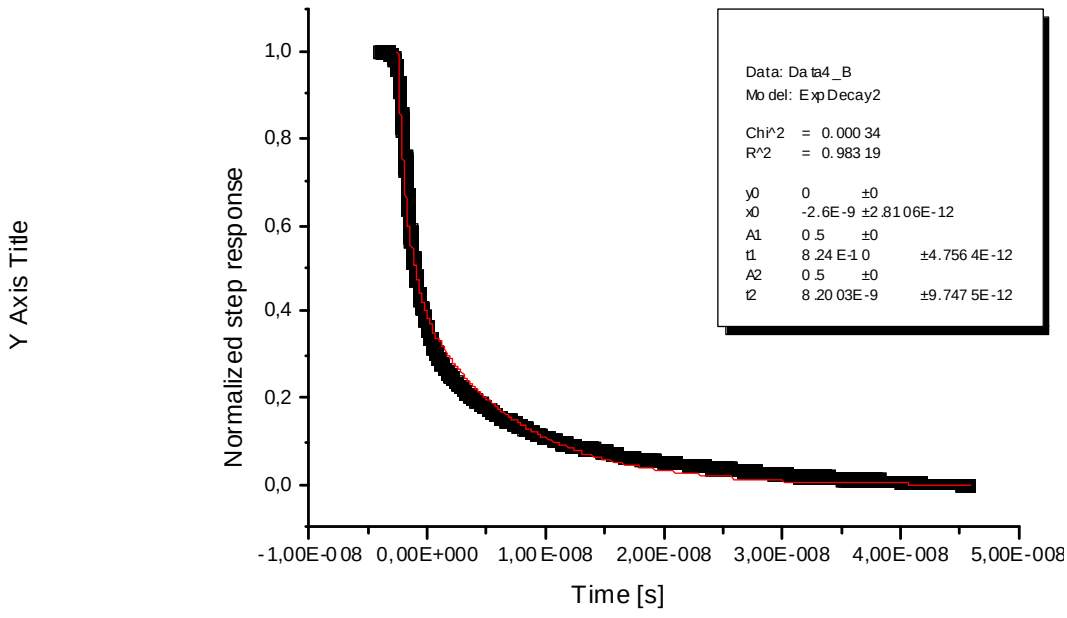

Figure 86. Step Response

	q0	a0 [ns]	q1	a1 [ns]	Rise time [ns]
LANMark	0.5	0.82	0.5	8.2	13
Prototype	0.5	0.89	0.5	8.9	11.5

Table 7 Cable Results for LVDS link

The filter parameters can be common for all the cables at first approximation, according to the fit the DC gain of the filter should be around 0,66 and the zero time constant about 8 ns.

Driver Compensation

The equivalent circuit in the driver is:

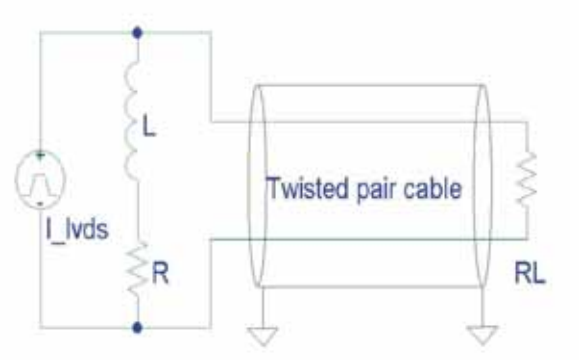

Figure 87. Equivalent Circuit

If we analyse this circuit, the resulting equations are:

$$V_O = I_i R_L \frac{s + \frac{R}{L}}{s + \frac{R + R_L}{L}}$$

Zero time constant: L/R

$$DC\ gain = \frac{R}{R_L + R}$$

Conclusions:

Compensation attenuates the DC and low frequency components and partially adapts the driver. According to previous considerations zero time constant should be 24 ns and DC gain about 0,88, this result on R=714 Ω and L=17μH. It is not possible to implement such a big inductor with enough quality (resonance frequency > 250 MHz), and then some tests should be done.

First Scenario: LANMark

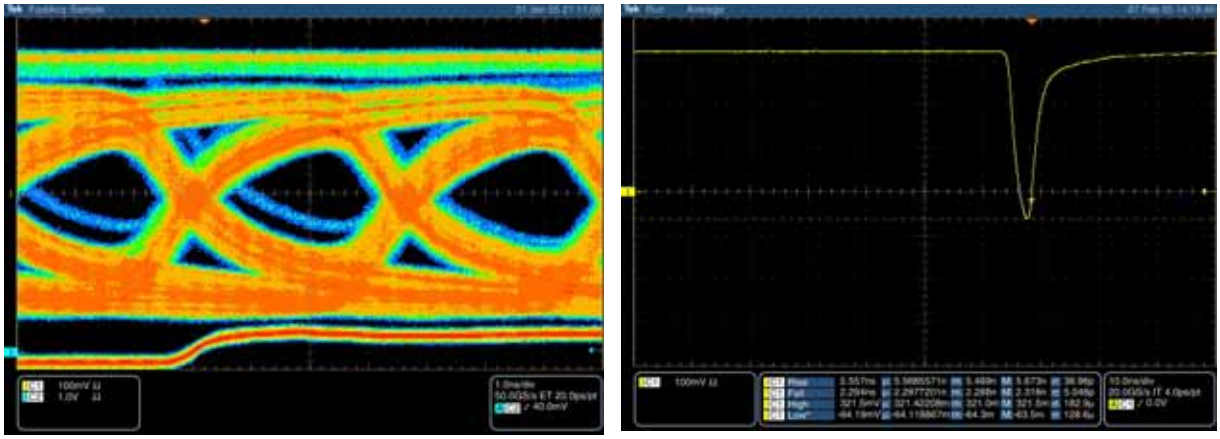

Figure 88. LanMark measurements

Inductance in the range 0,22 μH to 6,6 μH (the upper limit to use a commercial an inductor with res. freq. > 200MHz) are tested.

The eye patterns are taken with infinity persistence (with more than 1 M waveforms). For each inductance the resistor which provides best compensation (higher eye opening) is chosen experimentally. The IEEE standard short continuous random test pattern for Gigabit Ethernet (IEEE std 802.3) is used. 1 HOT pattern (1 followed by 100 0s) is tested.

Step response is also measured for all compensations:

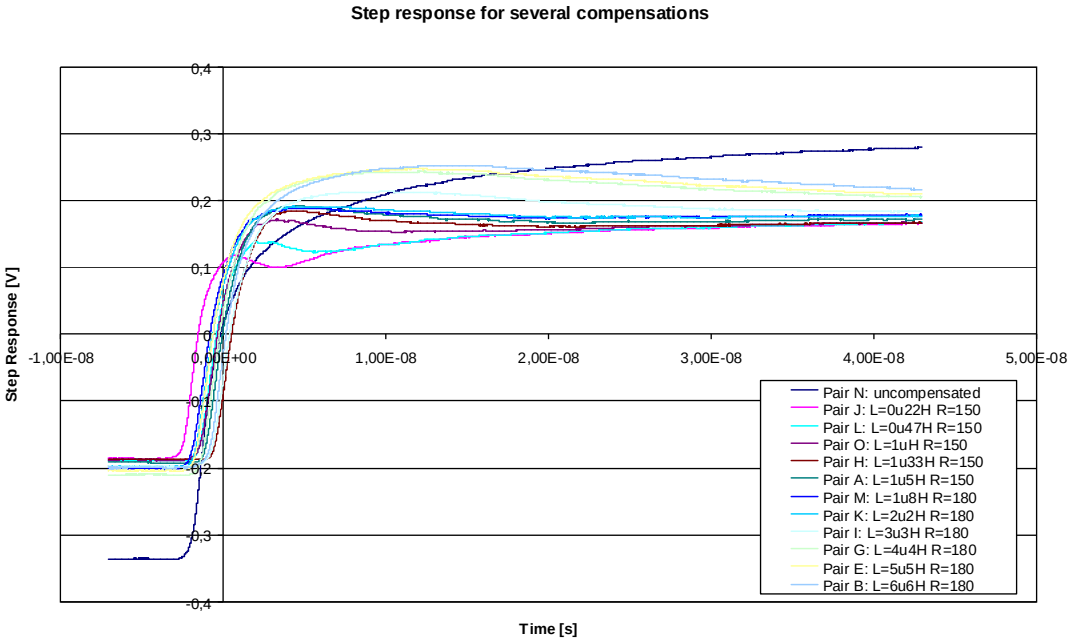

Figure 89. Step Response for all compensations

	Random Pattern	1 HOT pattern (current driver)					Step response (voltage driver)
	Eye Opening at ± 100mV [ns]	Pulse Opening at ± 100mV [ns]	Rise time [ns]	Fall time [ns]	High [mV]	Low [mV]	Rise time [ns]
uncompensated	-	-	Truncated	2,3	321	-64	13,5
L=0u22H R=150	low DC	1,4	1,6	1,8	194	-105	10,3
L=0u47H R=150	1	1,4	2,2	2,1	196	-130	2,85
L=1uH R=150	1,1	1,6	2,5	2,4	194	-132	2,2
L=1u33H R=150	1,3	2	2,6	2,2	190	-162	2,2
L=1u5H R=150	1,4	2	2,75	2,3	195	-165	2,2
L=1u8H R=180	0,95	1,6	2,9	2,2	203	-146	2,6
L=2u2H R=180	1	1,6	2,9	2,3	208	-142	2,5
L=3u3H R=180	1	1,8	3,5	2,3	197	-153	2,65
L=4u4H R=180	1,3	2	3,8	2,3	211	-175	2,7
L=5u5H R=180	1,1	2,2	3,8	2,2	203	-173	4
L=6u6H R=180	1	2	4,4	2,17	199	-161	4,4

Table 8 Summary of compensations for Lanmark.

Second Scenario: Proto

Good compensation also for L=1,5 μH and R=150 Ω, but worst eye opening (0,8 ns vs. 1,4 ns) for random pattern.

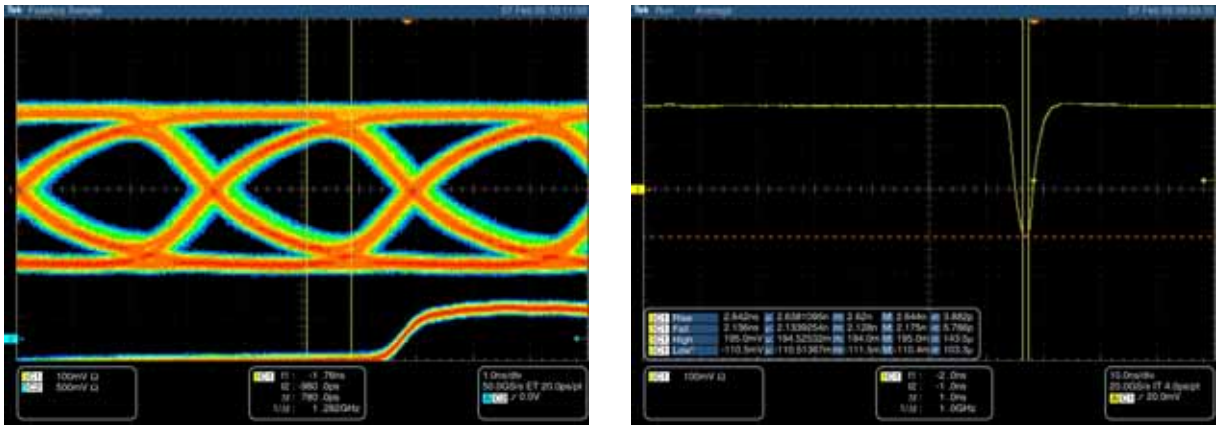

Figure 90. Proto Measurements

	Random Pattern	1 HOT pattern (current driver)					Step response (voltage driver)
	Eye Opening at ± 100mV [ns]	Pulse Opening at ± 100mV [ns]	Rise time [ns]	Fall time [ns]	High [mV]	Low [mV]	Rise time [ns]
uncompensated	-	-	Truncated	2,35	321	-21	12
L=1u5H R=150	0,8	1	2,65	2,15	195	-110	-

Table 9 Results of compensation of Proto

BER Test Results

1) For the LANMark:

No errors for 5000 s with any compensation for random or 1 hot pattern. That means a BER<10^{-12} for each pair and BER<10^{-13} for the full link.

It works even without compensation: BUT the error rate depends on the equalization and on the skew: if the skew is high the pair might have errors if it is not compensated.

2) For the prototype:

No errors for 5000 s with or without compensation with random test pattern (BER<10^{-12} for each pair and BER<10^{-13} for the complete link).

For 1 hot pattern 216 errors in 1 s, that means BER>10^{-4} for the uncompensated pair and no errors in 5000 s for the compensated ones (BER<10^{-12} for each pair and BER<10^{-13} for the complete link).

The clock of the system has been increased until errors appear on the transmission of a pair (results maximum clock frequency).

	Max. Freq. RND pattern [MHz]	Max. Freq. for 1 HOT pattern [MHz]	RND eye opening at ± 100mV [ns]	1 HOT opening at ± 100mV [ns]	Skew vs. clock [ns]
LANMark					
L=0u47H R=150	57,5	> 58	1	1,4	-0,4
L=1uH R=150	58	> 58	1,1	1,6	-0,13
L=1u33H R=150	57,5	> 58	1,3	2	0,15
L=1u5H R=150	58,5	> 58	1,4	2	0,4
L=1u8H R=180	58	> 58	0,95	1,6	0
L=2u2H R=180	59	> 58	1	1,6	0,15
L=3u3H R=180	58	> 58	1	1,8	-0,15
L=4u4H R=180	58	> 58	1,3	2	-0,1
L=5u5H R=180	53	> 58	1,1	2,2	-0,4
Uncompensated	50	48	-	-	-0,35
Prototype					
L=1u5H R=150 (9 pairs)	From 53 to 55	From 53 to 55	0,8	1	
Uncompensated	45	37	-	-	-

Table 10 Summary of compensations for Proto

Conclusion

LVDS tests were tedious. The requirements, 280Mbits/s and up to 27 meters long, do not only concern the electronics design. The choice of cables was one of the most important points. After carrying out a considerable amount of tests on different cables, the best cable was the nexans, one that a fulfilled all the requirements. These tests were made by the whole collaboration group.

6.4. Laboratory Series Tests

6.4.1. Series production

The series production consists on 120 VFE units. We assumed that 100 of them would be for the experiment, as it is explained at Chapter 4, the SPD contains 6000 channels, and the other 20 spare units and possible malfunctions.

The production involved several factories: LabCircuits, a Catalan factory in charge of the realization of the PCB card from our design; ROMPAL, another Catalan factory in charge of the mounting of the components; ERMEC, a distributor of ERNI, the farm in charge of mounting the high speed connectors (they were mounted in Germany).

On one hand, the fabrication of the cards was almost perfect, the number of bad cards, were minimum, around 2% and it lasted 5 weeks. On the other hand, when the series arrived from the mounting farm, more than 40% of the production had some kind of mistake (soldering), and it lasted 4 weeks. This implied a tedious task: inspect the soldering path per path, measuring all the signals with the oscilloscope…in order to achieve the number of the VFE Units that we needed for the experiment. More than 4 months were required to achieve this goal and then the series test started al laboratory. Finally the mounting of High Speed connectors by ERNI was an exit, a 100% of performance and it lasts only one week.

Several tests were needed to validate each card at lab: Noise and Offset Tests, Burn in Tests, Signal Tests and finally Stability Tests.

The paragraphs below explain each of these tests.

6.4.2. Noise and Offset Tests

Noise and Offset tests gave the information that the digital functions, signal paths were ok and obviously they gave a figure for the noise and the offset of the card. The Figure 91 shows the set up at laboratory. Again the DAb card was used to make the tests.

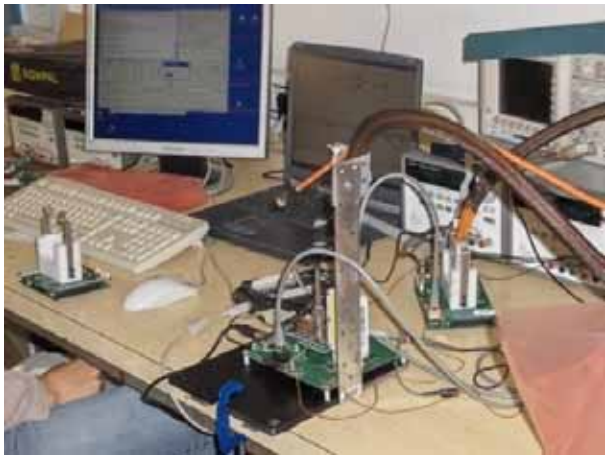

Figure 91. Laboratory Setup

Special software was required to make these tests in an automatic way. The figure below shows the main window:

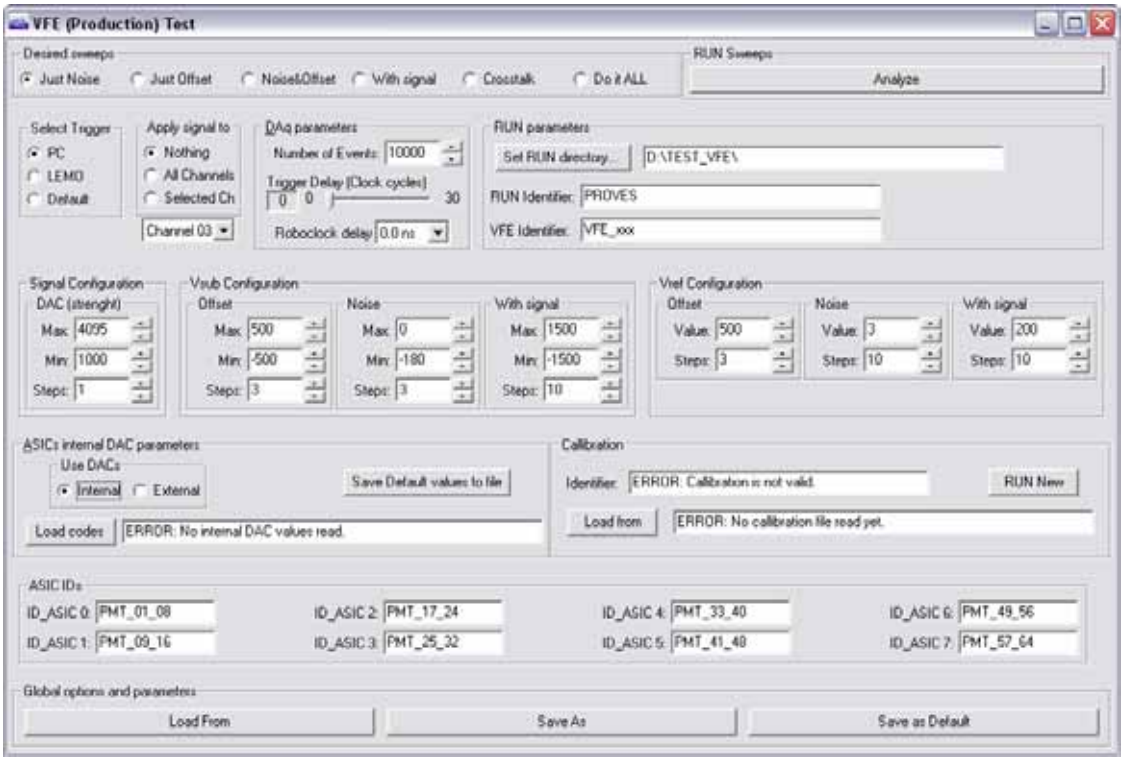

Figure 92. Program Test

The validation protocol (implemented in the program test) for this test was the following based in the validation protocol depicted at 6.3.2. The steps are the following:

1. The test had to be configured with the card identifier (each VFE Unit had an identifier)
2. Reset the FPGA of the VFE Unit: This informed that the communication path between the Test Card and the VFE Unit was correct.
3. Write/Read DACs: Testing the I2C path between the FPGA and DACs.
4. Write/Read ASICs: Testing the digital path between FPGA and ASICs.
5. Calibration of Vref and Vbias: They needed to be calibrated to make the best performance in the Noise and Offset Test.
6. Noise and Offset test (Threshold scan): A sweep for the whole values of the threshold is made for each subchannel of each ASIC. A noise figure for each subchannel was achieved, as well as a figure for the offset of each subchannel. This test also gave the information of the signal path, in normal conditions, each subchannel had to make a transition during the sweep, if this transition did not occurred implies that the path were broken at some point.

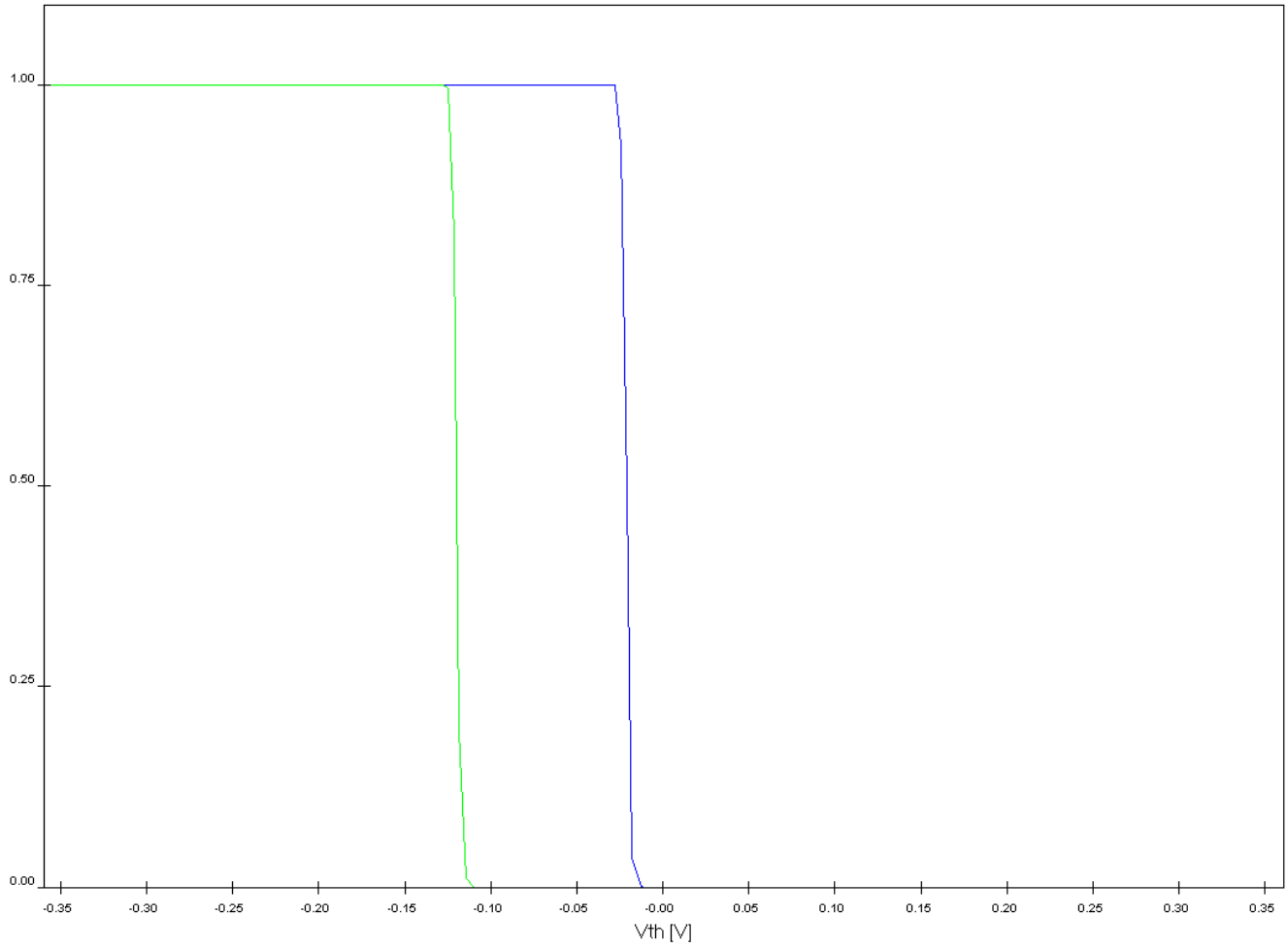

Figure 93. Threshold sweep on channel 25 of S005. First subchannel in blue, second in green.

As an example, the Figure 93 shows one of these correct transitions. The first subchannel is the blue one and the second subchannel is the green one. In principle, they should have the same shape and the same value, but this difference is due to the different offset and the difference noise in the subchannels.

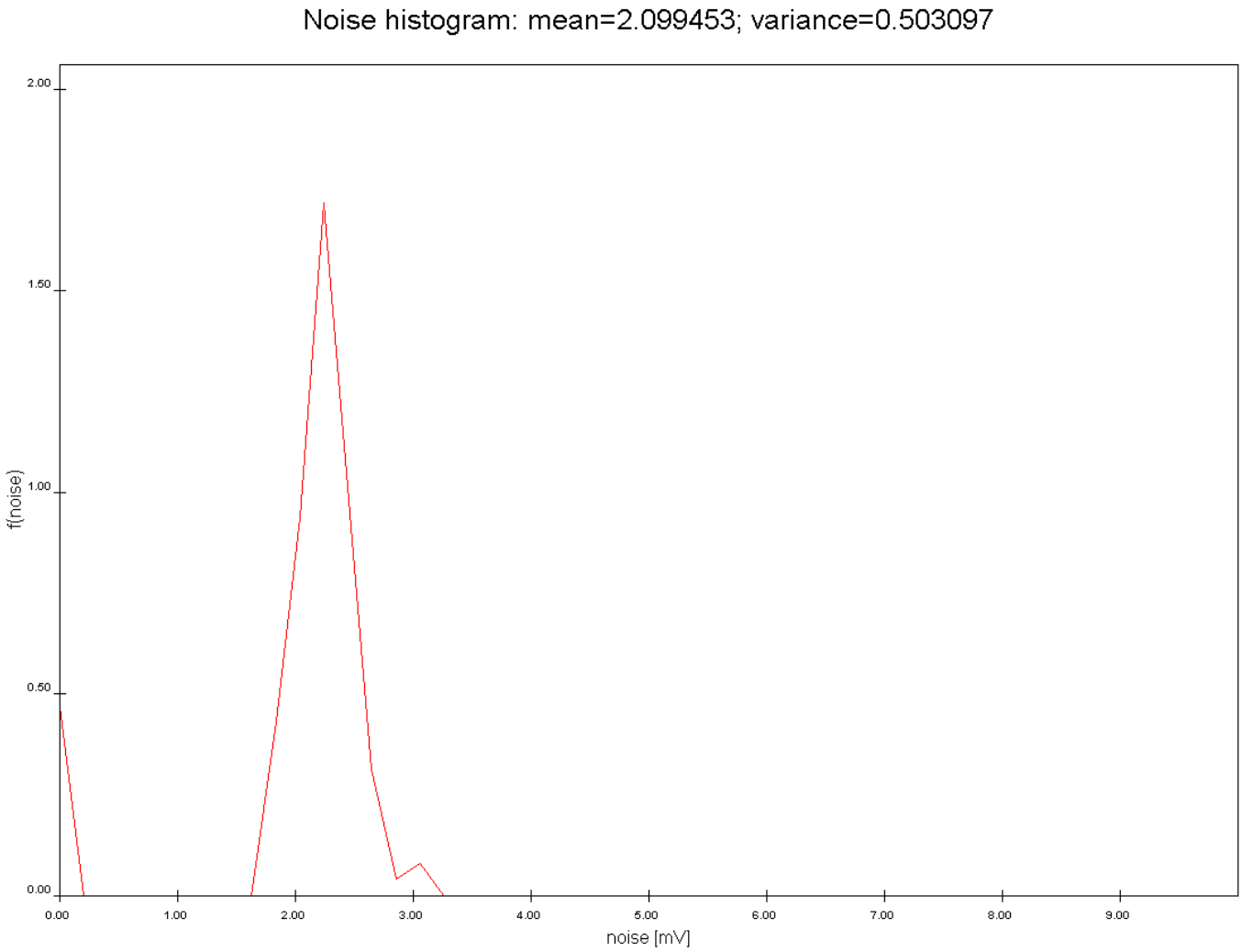

Figure 94. Average noise on S005.

The same software calculates a noise histogram and an offset histogram with the information taken by the sweep. This histogram was very useful to detect some problematic channels. The Figure 94 shows a noise histogram for the card numbered S005, and the Figure 95 the offset histogram for the same card. These tests are made for the internal theshold sweep and for the external theshold sweep as well.

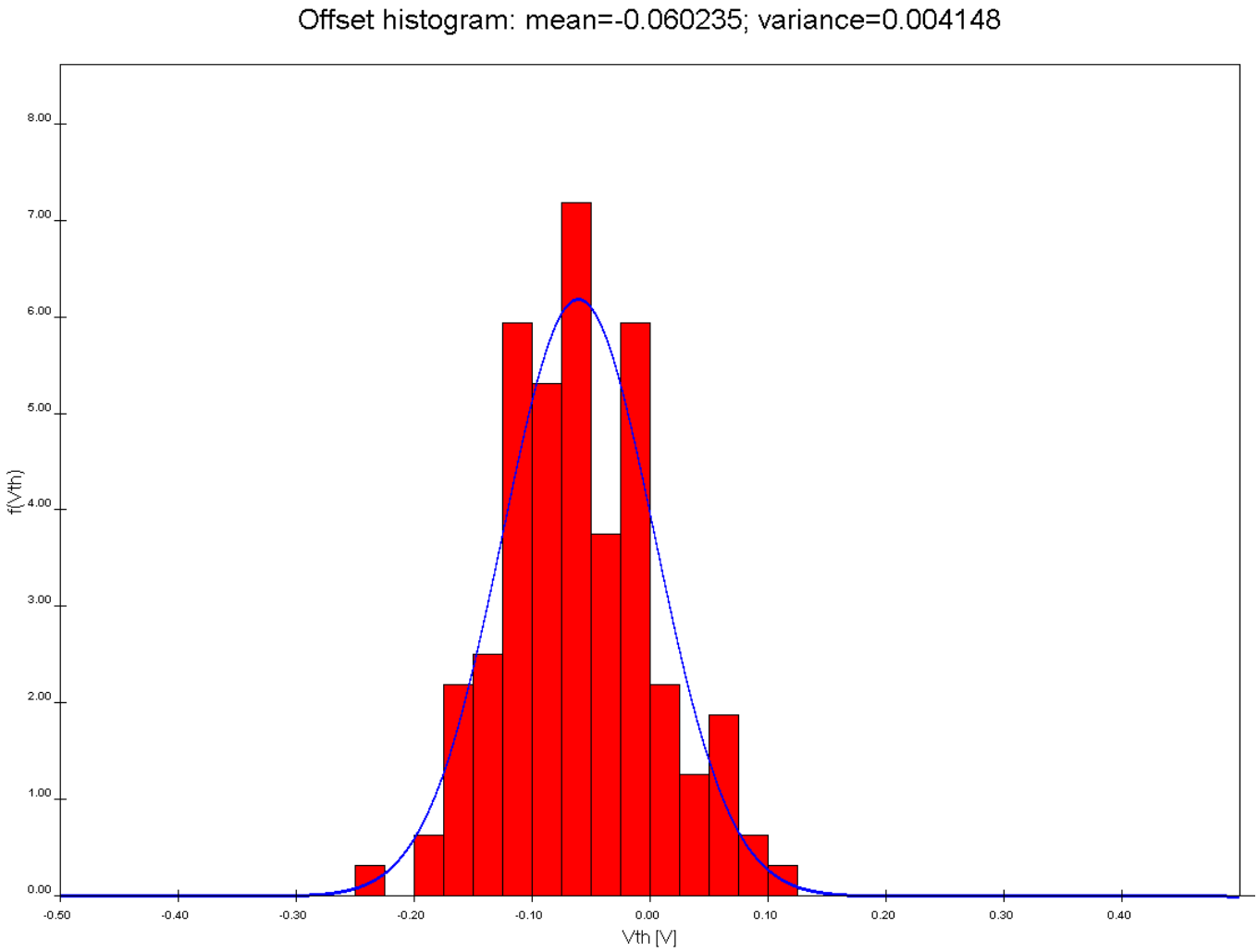

Figure 95. Average offset on S005.

The program also was prepared to calculate the comparison between the offset achieved for the internal sweeps and for the external sweeps. Next figure shows it.

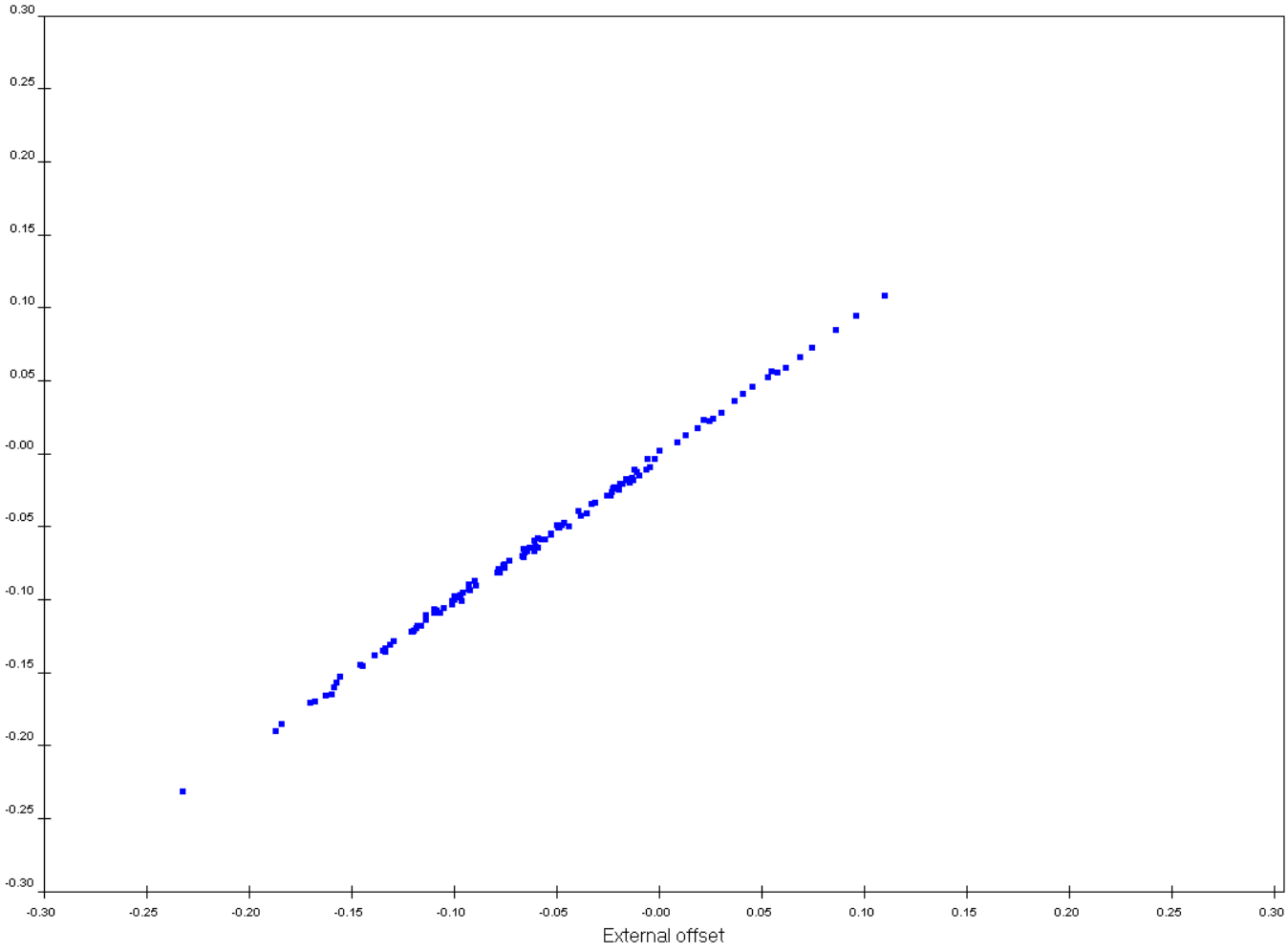

Figure 96. Internal Offset vs. External Offset

7. And finally, assembling the radiators and PMT Baseboard

The behavior of the cards with or without the assembling was different (The assembling was connected to the reference ground of the card). This assembling affects on the noise figure, and on the calibration of Vref and Vbias. For this reason, all the steps had to be retested again with the assembling.

6.4.3. Burn in Tests

This kind of tests is done for avoiding the 'mortal infancy' of the components. As it is mentioned in Chapter 2, the card belongs to a real experiment at CERN where the cards are placed at pit 100m below earth. For this reason, it is important to avoid

this ‘mortal infancy’ of components in order to change the minimum amount as possible.

It consists on a several cycles in a climatic chamber where the temperature and humidity are controlled and monitored. In the Figure 97 we can see the climatic chamber.

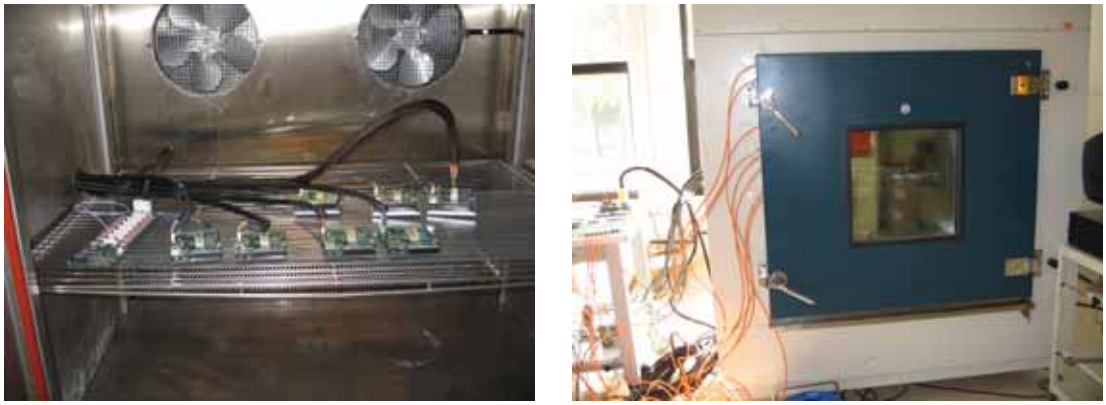

Figure 97. Burn in tests

In our specific case the cycles were:

8 cycles of 8h15 between 0 and 50 Celsius degrees with a 2h20 stop at 0 degrees, 40 degrees, and 70 degrees, with slopes of 2 degrees per minute in rising and 1 degree per minute in negative slope.

The maximum temperature of the cycle is marked for the most sensitive component, in our case the FPGA. The maximum temperature for the FPGA is 85ºC for a good operation. Assuming a security level and assuming that in this test there is not any cooling system, the 50ºC was decided.

This cycle tests the functionality at the maximum and minimum temperature and also at the temperature of current working. The Figure 98 shows the results for the pre-series.

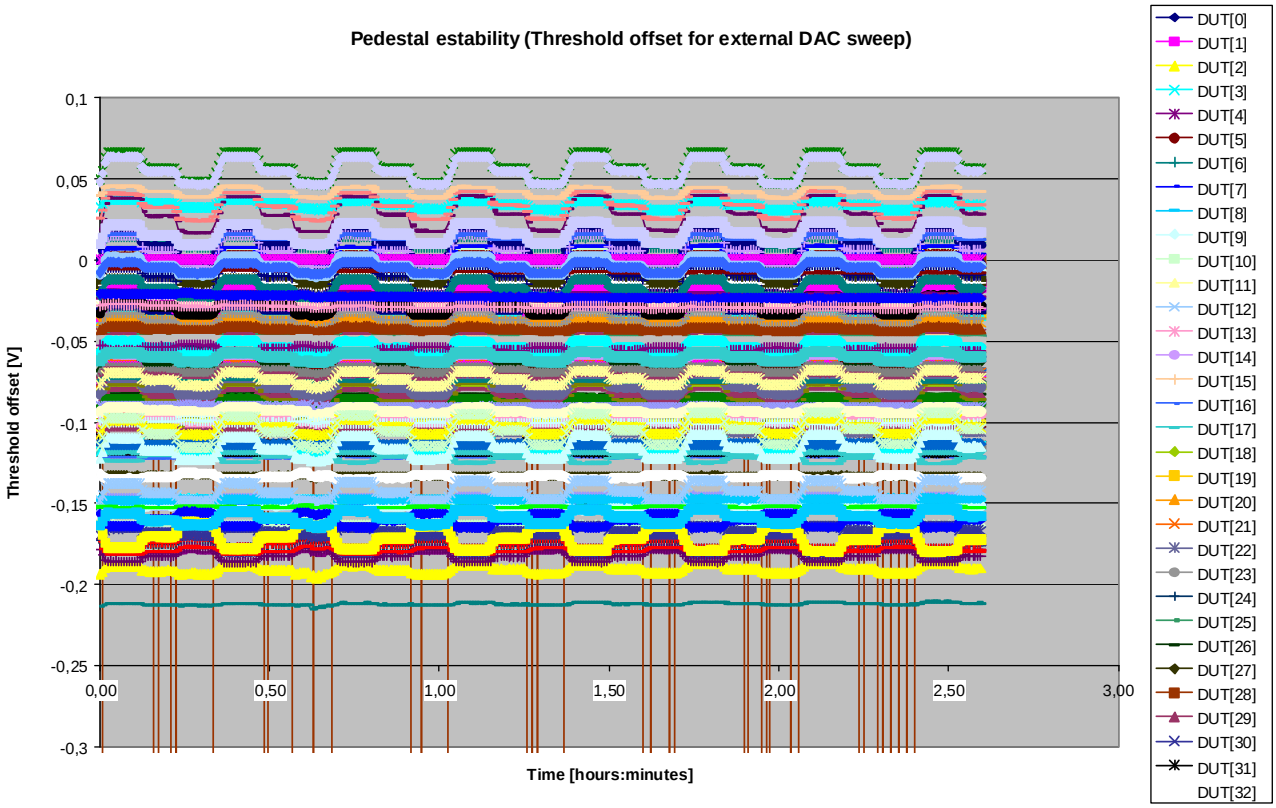

Figure 98. Burn in results

These tests were done by Applus+, a Certification Technological Center in Barcelona.

6.4.4. *Signal Tests*

A special setup where the VFE unit is closed inside a black box (in order to eliminate the light), and an optical fiber can be placed in front of the photomultiplier is needed. A mechanical structure with a pair of stepper motors has been constructed in order to move the optical fiber through the 64 channels of the multiplier (Figure 99). This optical fiber comes from another box which contains a little scintillator with a led pulser outside the black box.

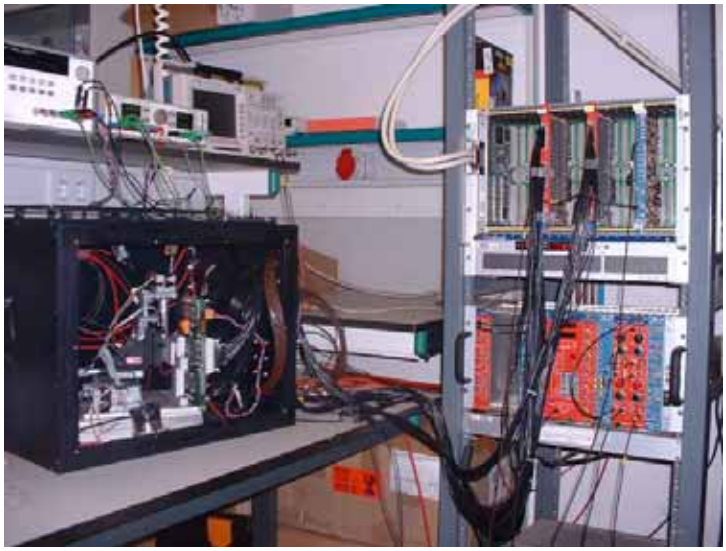

Figure 99. Black box setup

With this setup two kinds of tests can be performed: Signal Tests and PMT Tests. In both of them, the VFE Unit is completely assembled including the PMT.

On the first ones, the signal tests mentioned before, the 64 channels of the photomultiplier are completely illuminated by the led system giving the information about the signal in all channels, and on the last ones a unique fibber is put in front of each channel of the PMT and it is pulsed channel by channel in order to test the crosstalk.

The validation protocol for this test was the following:

1. The test had to be configured with the card identifier (each VFE Unit had an identifier)
2. Introduce the VFE Unit inside the black box and put in front of the PMT the 'dispersor' of light.
3. Make a sweep of Vbias illuminating the 64 channels together. Thus the pile up subtraction is tested for the whole card.
4. Check the results in order to check if tail compensation is working.

Next plots show different behaviors of the outputs as a result of making a different pile-up correction.

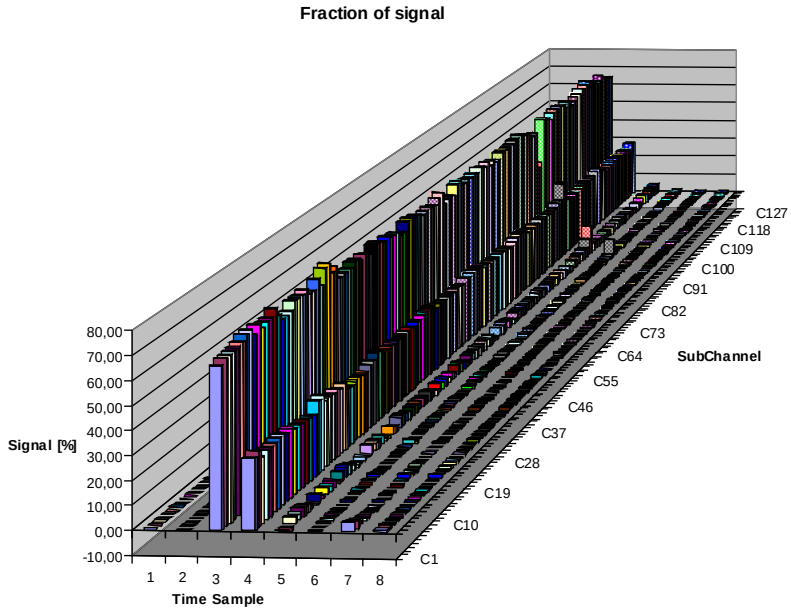

Figure 100. Signal fraction with Vsub=+100mV

In Figure 100 is shown a plot showing the pile up compensation. The event is in the time sample 3, and the tail is in 4, 5 and also 6. Figure 101 shows a decreasing of the tail as the compensation increases and finally in Figure 102 the tail is eliminated (or even negative).

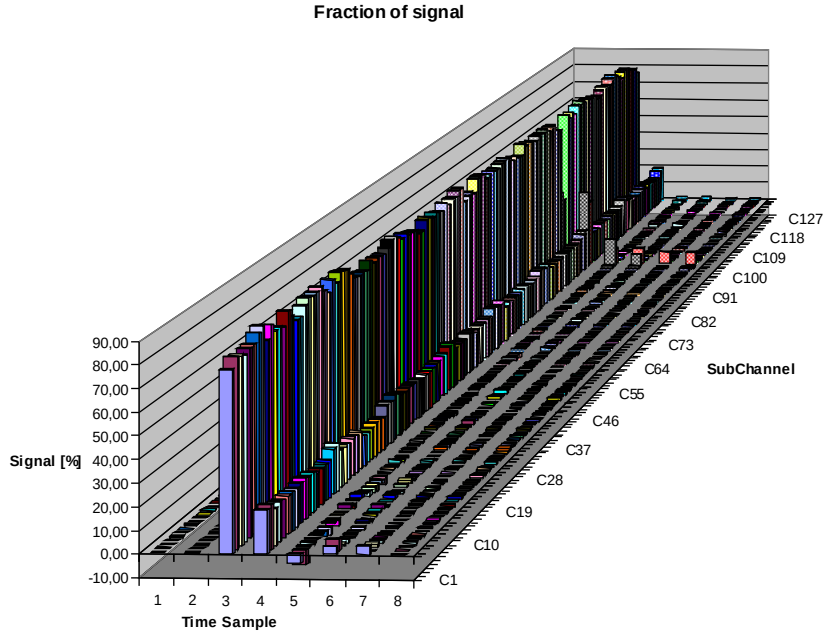

Figure 101. Signal fraction with Vsub= -50 mV

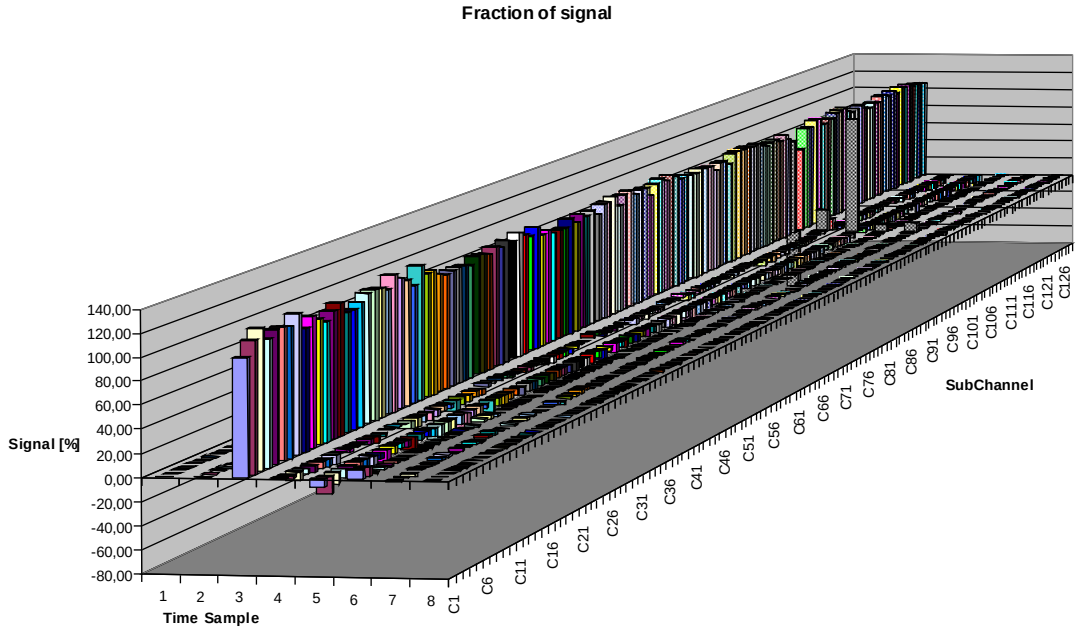

Figure 102. Signal fraction with Vsub= -250 mV

5. If the tail compensation is working, then the black box has to be opened and connect the unique fibber, and the little scintillator to the led pulser. This test checks the crosstalk between channels.
6. Make the channel sweep for the unique fibber.

The results show the crosstalk between channels (optic and electric crosstalk). Figure 103 depicts the crosstalk generated in the other channels when the signal is injected on each even channel (in the card numbered S009); the results are given in %. It can be checked that almost in all channels is below 5% (which belongs to optical crosstalk).

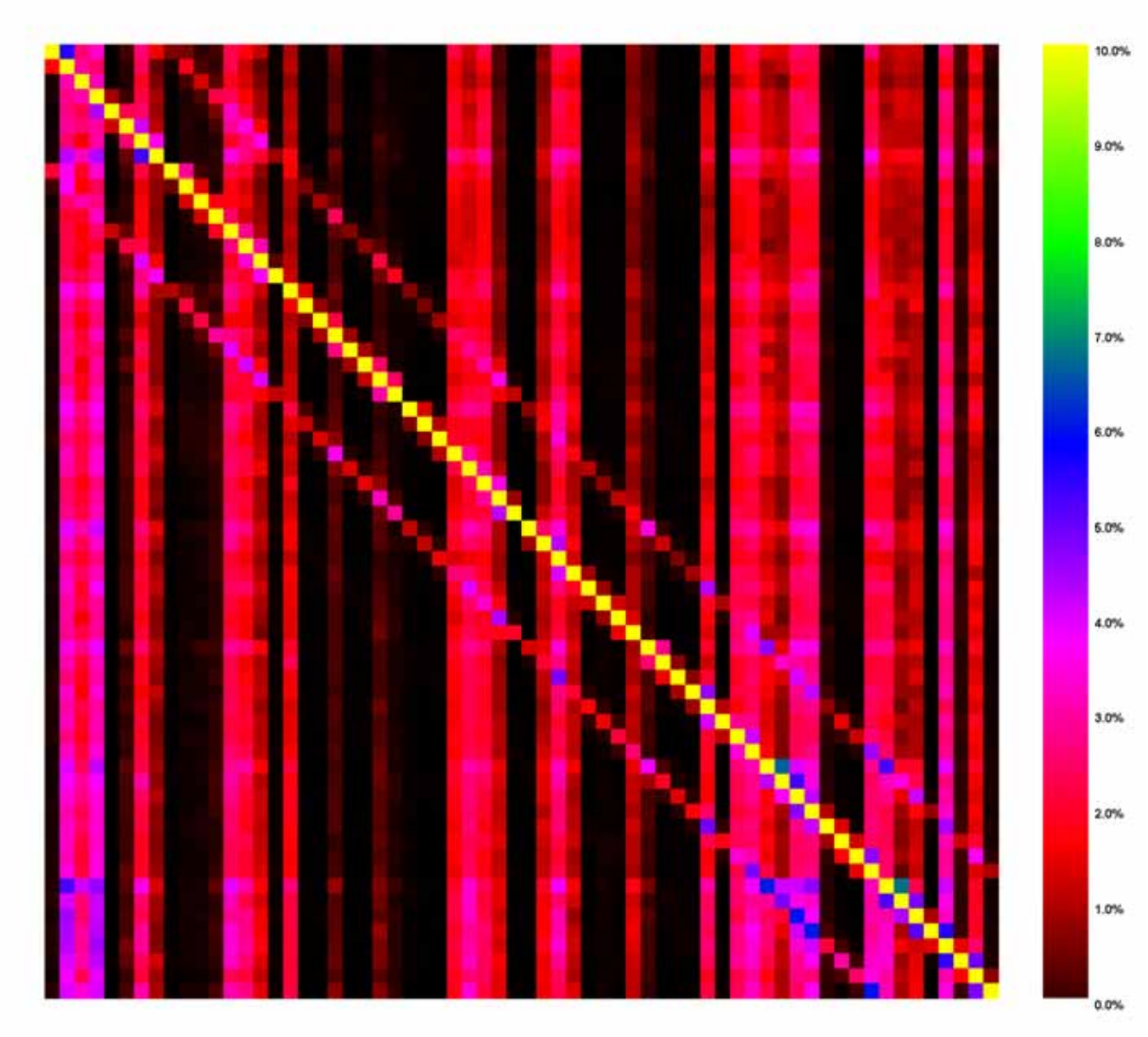

Figure 103. Crosstalk for even channels in S009 VFE Unit

6.4.5. Stability Tests

These tests are in charge of testing the VFE Units in a stress mode. The final goal of these units is to be mounted at the cavern in the SPD subdetector. Therefore, they must work for long periods without stopping. The stability tests were made in the closest conditions to the situation at cavern: the same metallic box, the cooling, and the place for the cards.

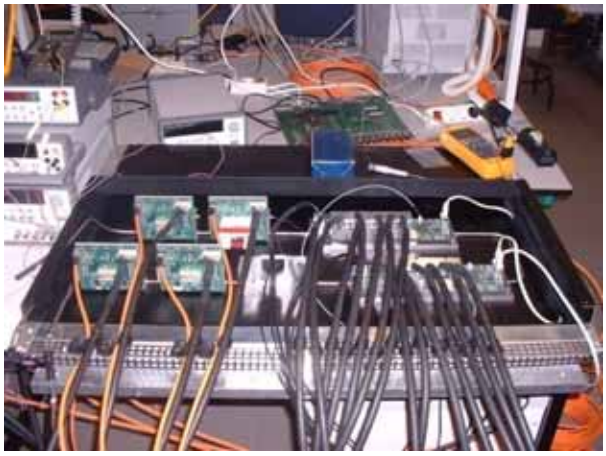

Figure 104. View of the box used at laboratory for stability and cooling tests

These tests consist on making the same tests as on the laboratory, but in this scenario proving that the environment does not affect enough on the card functionality.

Noise and Offset results are in the next figures. These figures were acquired after a stress mode: four hours connected in the metallic box continuously running.

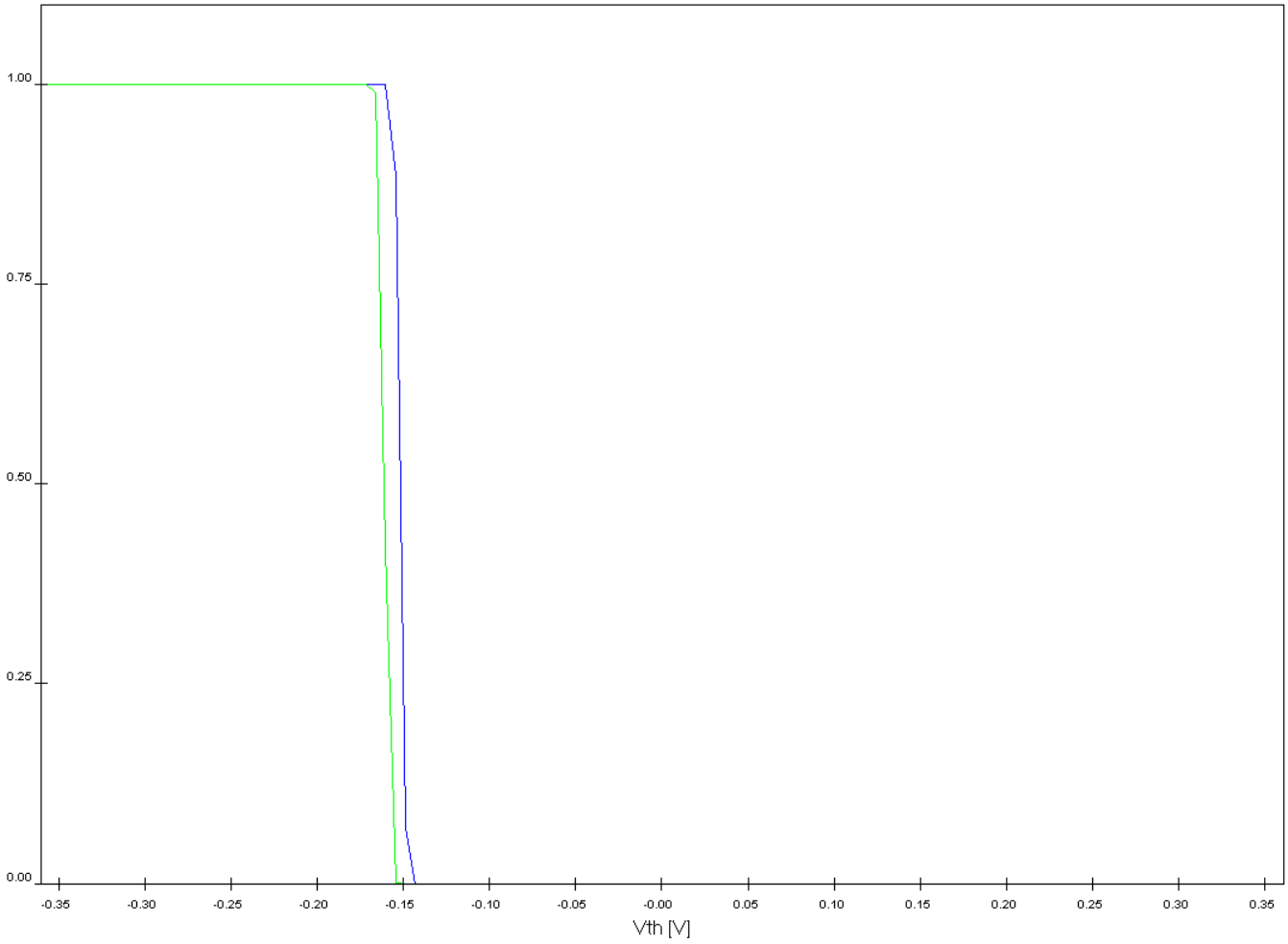

Figure 105. Threshold sweep for channel 36. First subchannel in blue, second in green.

Figure 105 shows the theshold sweep for S013. It can be checked that the offset between subchannels is very little (the difference shapes when are changing the level).

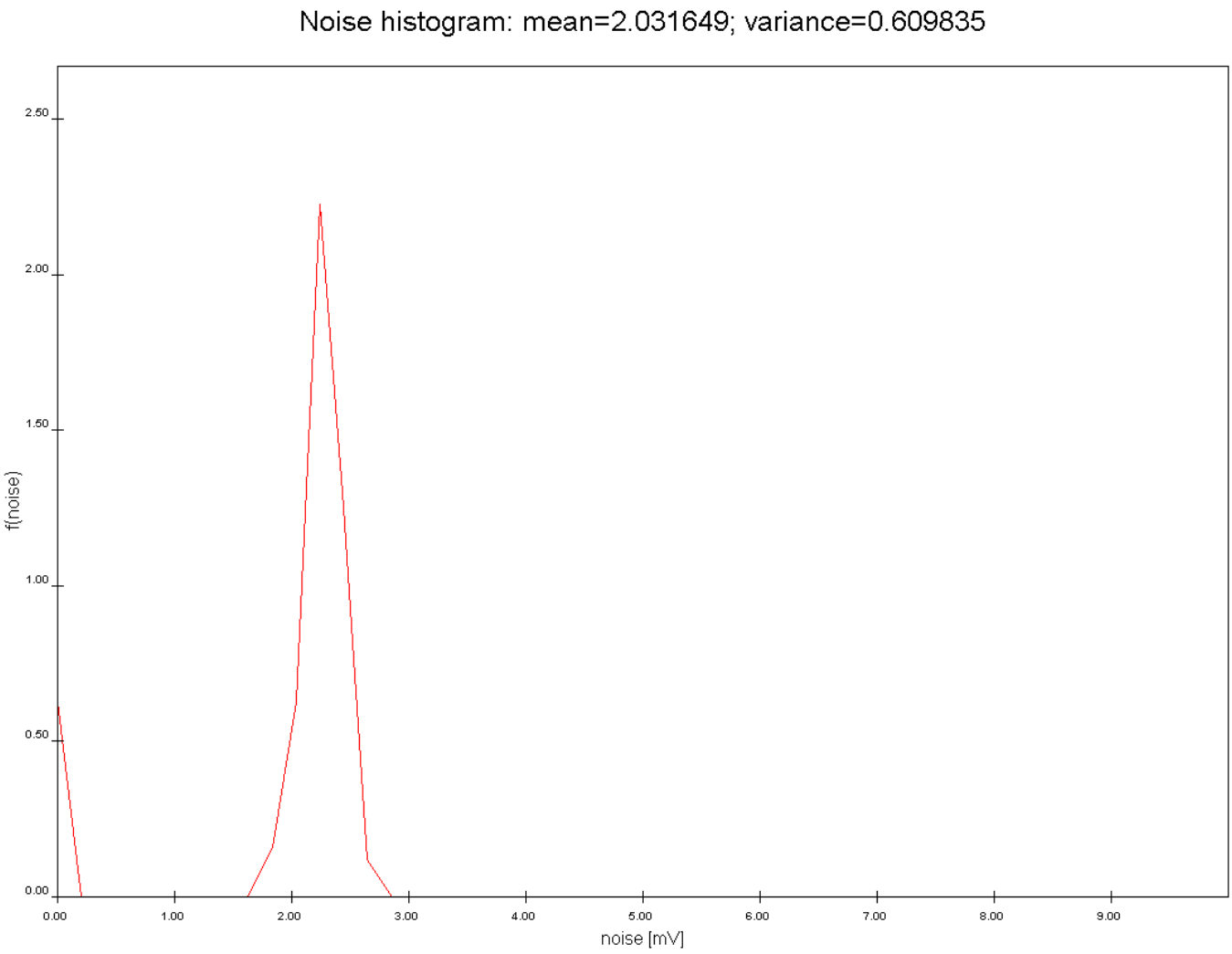

Figure 106. Average Noise measured on S013 VFE Unit.

Figure 106 shows the noise histogram for S013 as well. The value achieved is lower than the LSB required also in a stress mode.

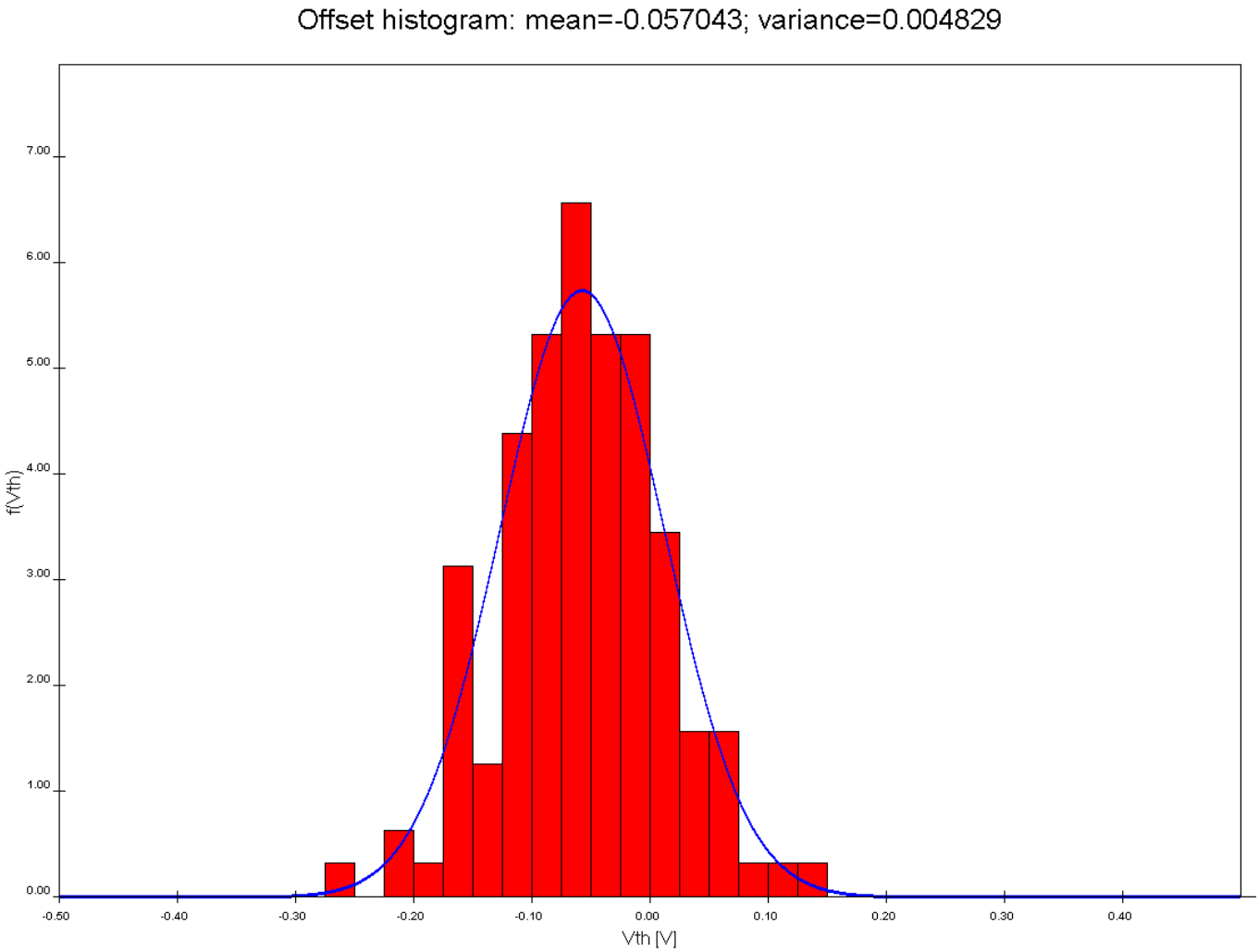

Figure 107. Average Offset measured on S013 VFE Unit.

In this case, the previous figure shows the average offset in the same card. Comparing to the results achieved without stress mode, there is a little difference.

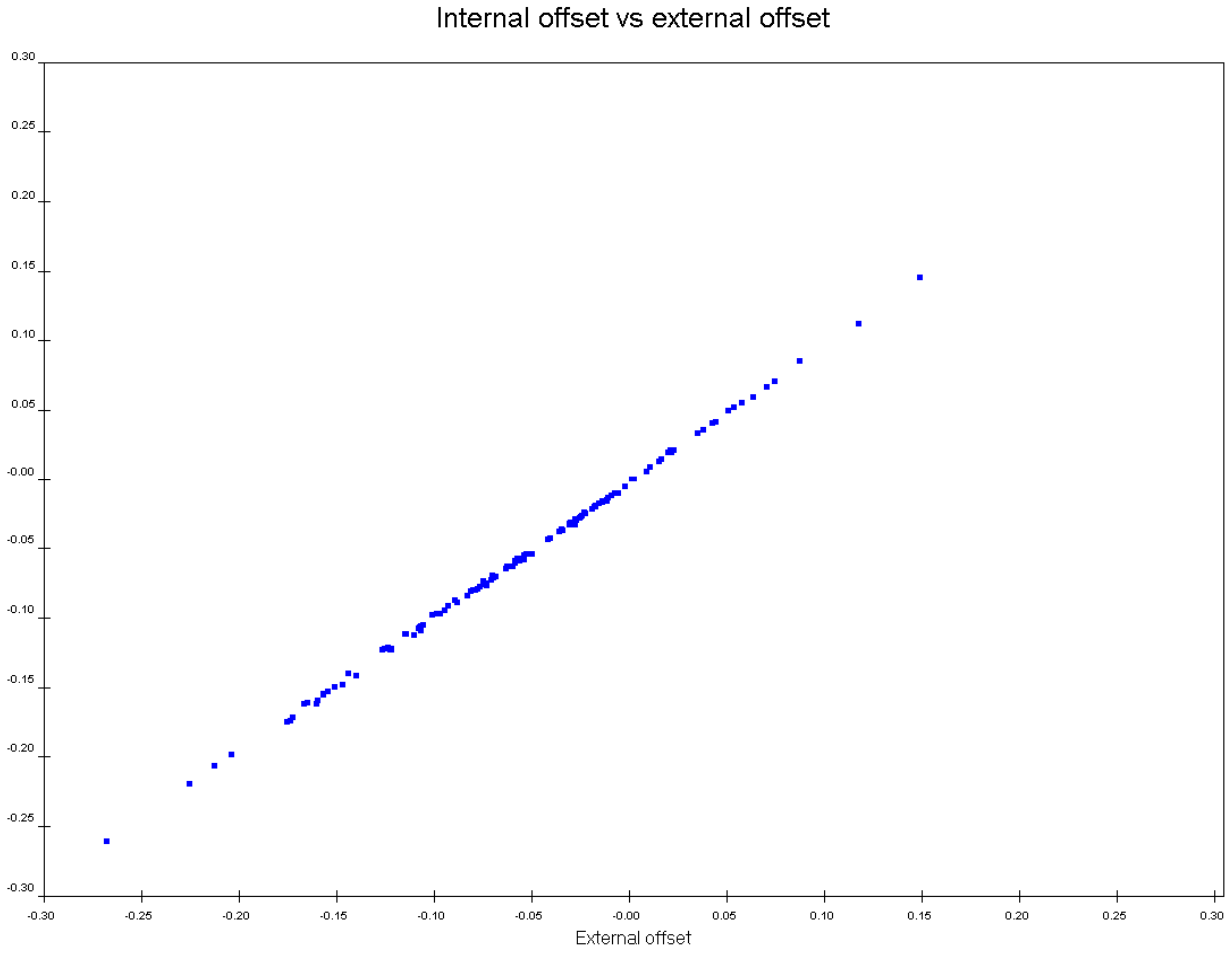

Figure 108. Internal Offset vs. External Offset

The figures shown the results obtained for S013, showing the correct operating.

6.5. Pit Series Tests

6.5.1. Mounting at Pit

Once the series tests at laboratory were finished, a hundred of these VFE Units had to be transported to CERN and also they had to be mounted at the cavern.

The transport to CERN was made by car during March 2007. The mounting was a very hard task as a result of the environment at the cavern (the SPD is divided in four groups, C-side top and Bottom and A-side top and bottom): The situation of the SPD in the detector not only left only about 50cm free in the z-axis, but also the height (y-axis) for the Bottom part is about 2.5m and for the Top part is about 12m, as it is mentioned in Chapter 2. Next figures show the difficulties.

Figure 109. Transport, left. Mounting on Bottom part, right

Figure 110. Scaffolding, left. View from Top part, right

Figure 111. Box of 11 VFE Units without cabling

The mounting was made between March and July.

6.5.2. *Noise and Offset Tests*

Once the cards were installed, the same Noise and Offset Tests done at laboratory had to be repeated to check the functionality of the cards. We had to be sure that the new environment didn't change the results.

Of course, the conditions were very different: at pit there was not any setup to check the cards; therefore a new portable setup was needed in order to test the cards. It was based in the same setup at laboratory; it is shown in the Figure 112:

Figure 112. Test setup at Pit

The validation protocol of the cards was the same as at laboratory. The most important points are:

1. Test had to be configured with the card identifier.
2. Reset the FPGA of the VFE Unit
3. Write/Read DACs.
4. Write/Read ASICs.
5. Calibration of Vref and Vbias.
6. Noise and Offset Test

The figure of mean noise achieved in the tests was around 2.3mVrms except for some noisy channels (more or less the same figure achieved at laboratory). These tests were done without High Voltage and High Voltage also (this is the voltage need for the PMT), see Figure 113. This figure fulfills the requirements of the Noise depicted at Chapter 4, one LSB.

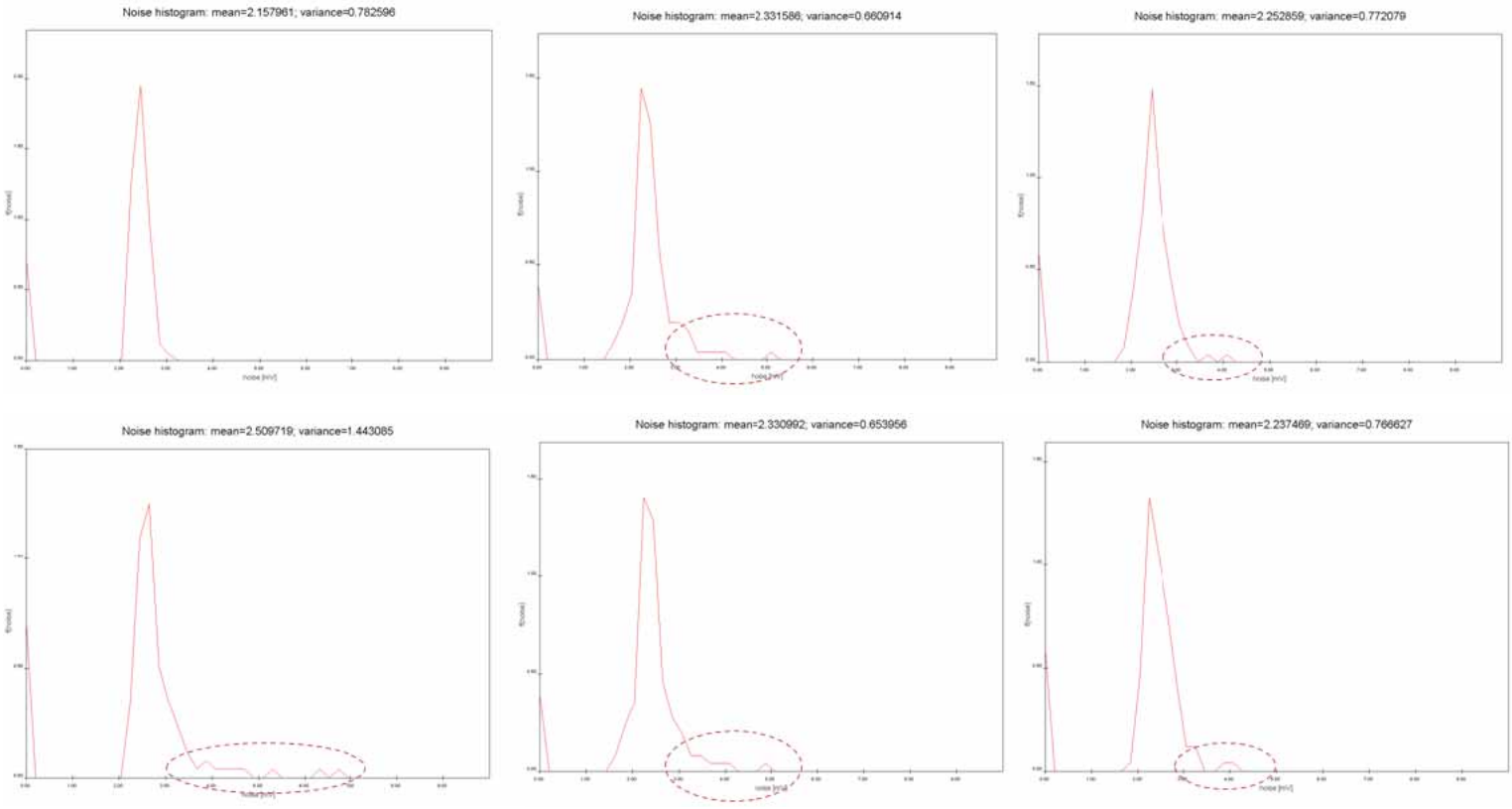

Figure 113. Figures of noise, noisy channels marked (HV=0V Top, HV=700V Bottom)

Despite the fact that the requirements were accomplish, the problem was investigated in Barcelona and it has been discovered that if the connection of the ground of the VFE card to radiator (box ground) is improved the noisy channels disappear.

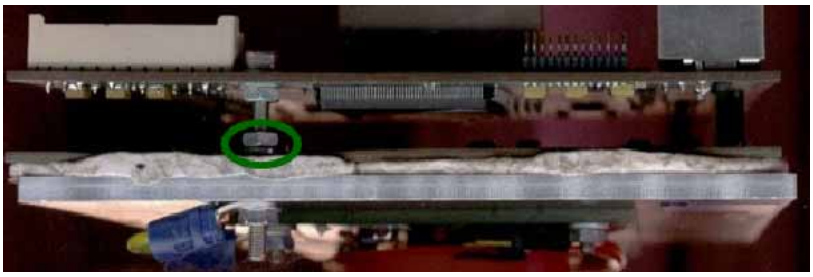

Figure 114. Nut added to improve ground connection

The improvement consists on adding a washer and nut to improve connection of ground screw to the radiator see Figure 114.

6.5.3. Signal Led Tests

The signal test made at laboratory had to be repeated as well, but in this case the difficulty increases. In order to make this test at laboratory, the setup needed was a black box with a little scintillator connected to a fibber that gave the signal to the photomultiplier.

At pit, in the experiment, this was impossible; in order to test the signal at photomultiplier, the group from Moscow made a setup with leds. These leds illuminate the photomultiplier giving the light needed to make the test. Of course, this led setup needed some indications (signals) to work such as the power supply and the trigger.

On one hand, the trigger given by our setup card, had to be delayed depending of the situation of the led card in the system, then a delay unit was used to make the test. Actually, some tries had to be done until the best delay was found.

On the other hand, the power supply of the led card was not fixed, it had a range. This range gave the swing of the light. Therefore, this power supply had to be calibrated in order not to saturate the photomultiplier and also in order to give it enough light.

Results achieved only shown that all the photomultipliers, and also the cards, had a good functionality, but the figures given were not so specific as a result of the functionality of led cards.

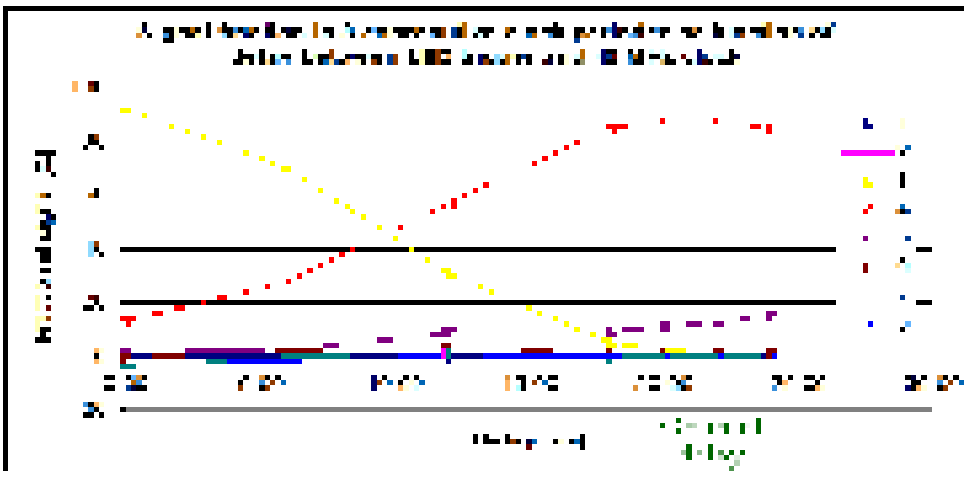

Figure 115. Signal fraction achieved changing the delay on trigger signal

In the setup for led tests was needed a delay unit. The delay of the trigger was not known and it had to be configured. The Figure 115 shows the optimal delay obtained for making the tests.

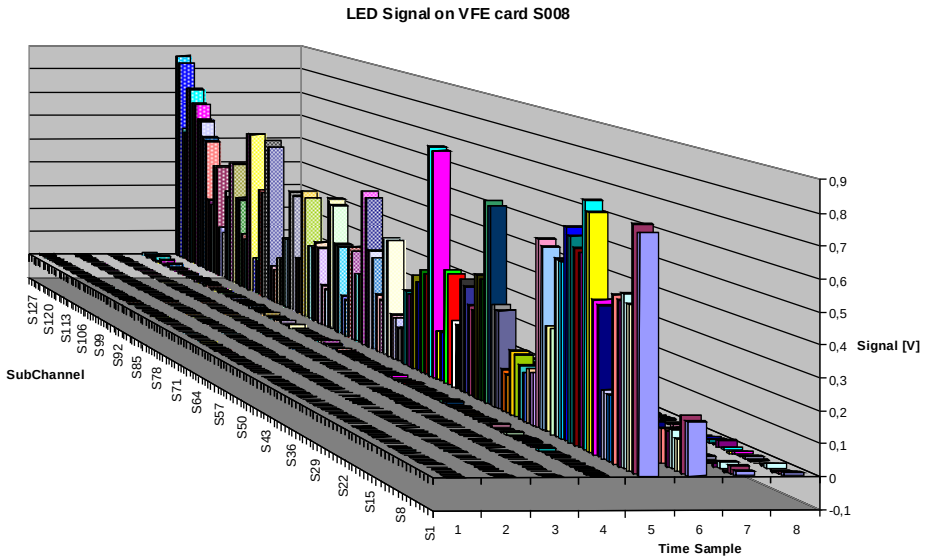

Figure 116. Signal test on S008 with led setup

Figure 116 shows the results achieved with the optimal delay in the card S008 with the led setup.

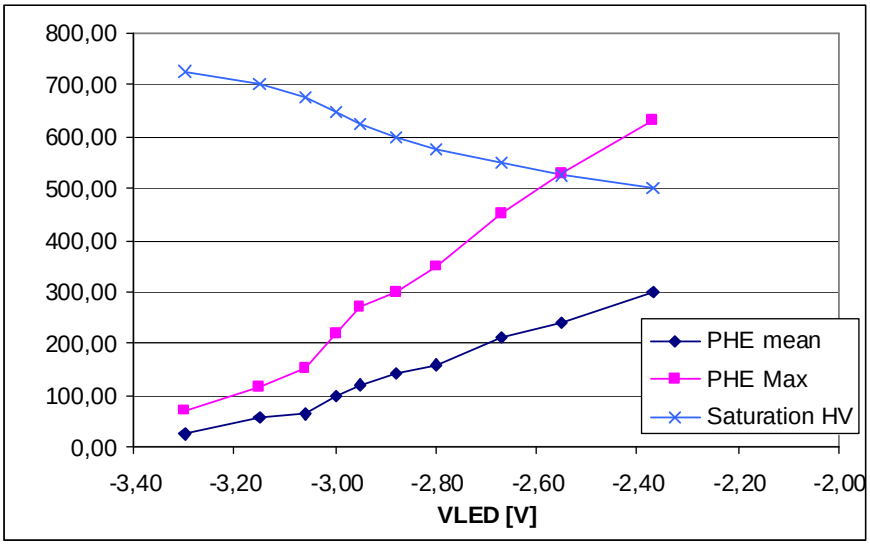

Figure 117. Number of photoelectrons vs. power supply of led card

The power supply of the led card must be configured as well. Figure 117 shows the number of photoelectrons achieved in function of the power supplied given for the led card.

6.5.4. Commissioning Tests

Nowadays the commissioning of SPD is being made by the Barcelona Group. The first commissioning tests done during last months are the following:

- Nphe/MIP of cells obtained from cosmic measurements.
- Pedestals (PS) or offset (SPD) and noise first values measured.
- Time alignment within PS/SPD boards studied.
- LED system used to check all channels.
- Cosmic measurements have been started. Data is under analysis for time alignment and to check the mapping.

The results show the performance of the whole system of the Calorimeter as well as the Online System, which processes the data, as an example, Figure 118 shows a cosmic event using the Calorimeter and reading the information with the Online System. [45]

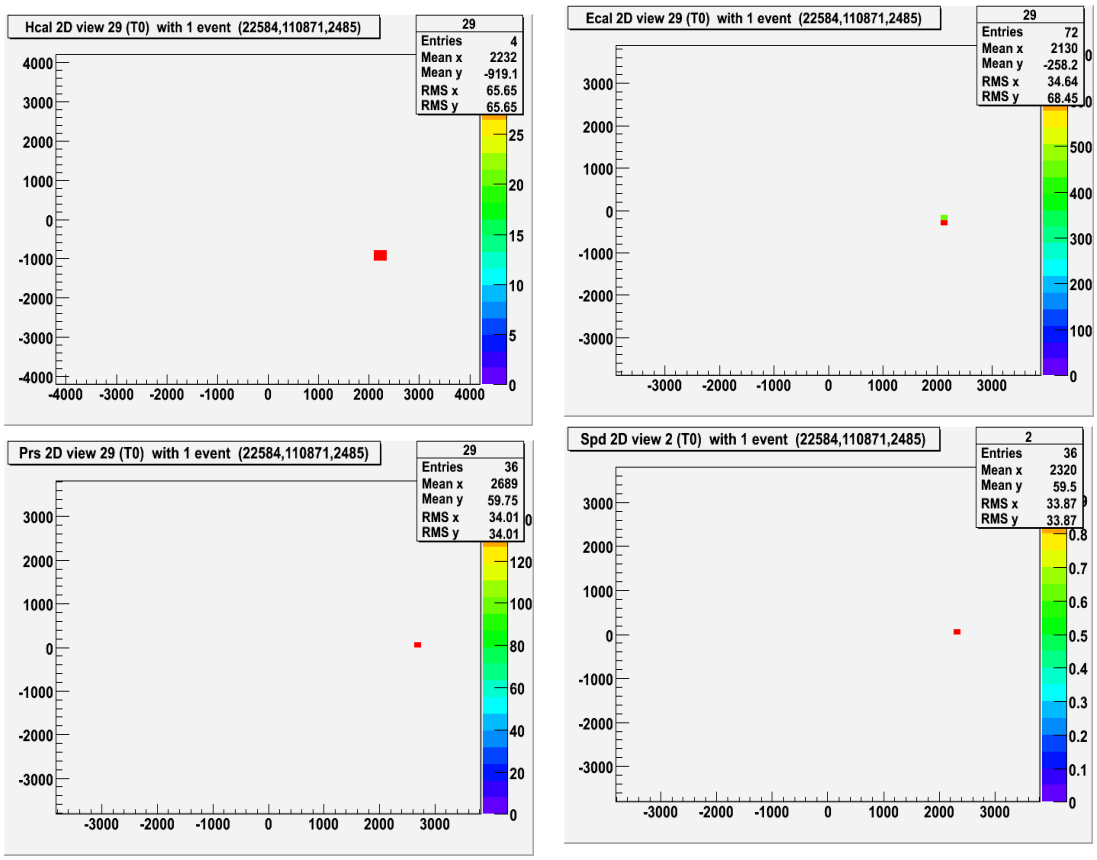

Figure 118. Cosmic event in the Calorimeter. HCAL at Top Left, ECAL at Top Right, PS Bottom Left and SPD Bottom Right.

Chapter 7: Conclusions

Chapter 7. Conclusions

High Energy Physics requires a specific instrumentation in order to implement the theories that they are searching and studying. This instrumentation is usually made by a full custom design as a result of being a unique solution.

Electronics is submitted to particularly hard conditions such as: Analog and little signal ranges implying in most cases the use of full custom designs (ASICs) in order to make the processing, as well as the use of field programmable gate arrays (FPGA) to make the design reprogrammable.

Not only the signal range has to be taken into account, but also the ionizing radiations, which may disturb data by changing memory contents (SEU) or even damage electronics by causing latch up's (SEL). At least Radiation Tolerant components must be used and memories have to be protected by redundancy methods and error correcting techniques. Each component must have a radiation qualification. Therefore if they have not the qualification, they must be irradiated in order to achieve it. Not all the components passed this irradiation that implied a change in the design, for example, the first LVDS multiplexer that we tried to use was the 5DS90CR464 of 64 input channels, but it hadn't pass the qualification and we have to put four DS90CR215 of 21 input channel that passed this irradiation for accomplishing the specifications.

Mechanical constraints given by the geometry of the detector related to the need to preserve faint signals.

For these reasons solutions to electronics rely on full custom designs, for boards, but also for buses and components.

Apart from Electronics, a real experiment related to high energy physics involves several constraints, the most important enumerated in the paragraphs above.

On the first term, the changes in specifications during years: This fact implies a considerable delay in the beginning of the final design; it could not start as soon as it was planned. The final specification was not closed until final of 2005 implying continuous changes in the design.

On second term, belonging to a real experiment at CERN was an important challenge; on one hand a lot of groups, involving different skills such as Electronics, Physics and Mechanics, working in the same experiment. Despite this fact, the coordination of the Calorimeter, the group where the SPD was involved, was so efficient. Of course a lot of meetings between the groups were needed to solve the problems that designs required; on the other hand, a real experiment implies a real mechanics. Some mechanical constraints were unknown when the design started, and then the VFE had to be changed during the development meanwhile the mechanics was designed.

On the last term, the number of tests required to fulfill the specification must be taken into account too. Belonging to the LHCb Calorimeter also implies accomplishing the requirements, not only for a prototype but also for a series. When a series of a design is produced, a type of validation protocol must be decided in order to test this series. It is not viable making the same tests for a prototype than a 120 cards. This fact implies a design of a setup test; customized hardware and software were required.

This thesis contribution is the solution for the VFE electronics of the Scintillator Pad Detector of LHCb, the foremost detector layer in the calorimeter, devised to discriminate electrons and photons at the level 0 trigger. The SPD is made of 6000 scintillator pads of 3 different sizes according to the distance to the beam pipe, which is read in groups of 64 by a Hamamatsu multi-anode photomultiplier through WLS fibers connected to clear fibers. Typical signals range from 12 to 25 photoelectrons. The experiment clock is set to 40 MHz, so that signal may pile of from one cycle to the next. Signal processing is taken care by an ASIC dealing with 8 channels

simultaneously divided into two subchannels with programmable thresholds. Its binary output at CMOS level must be sent in real time to the PreShower front end board by LVDS link: about 27 meters at 280MHz clock, implying the use of a full custom cable. The different elements used in the design imply the use of several power supplies.

In order to avoid further degradation of the light signal in the fibers, VFE electronics lays in boxes on the top and the bottom of the detector of size around 96cmx70cmx12cm forcing the maximum size of one board to be about 10cmx10cm. Since FE boards are installed in racks on top of the calorimeter platform, data shall have to be sent through cables from 20 to 30m by an LVDS link.

The VFE Unit involves 3 connected boards: One hosting the PMT active base, designed in Clermont; the second card was the analog one, it contains the MAPMT, the eight ASICs and the DACs and OPs needed to make the thresholds and pile-up compensation; the last one was the digital one, it shares digital and LVDS signals, containing the FPGA and the LVDS transceivers and serializers as well as the power adaptations.

Both cards are ten layer-cards with components in Top and Bottom layer, class-6 and made with FR-4. The number of layers obeys the number of power supplies and the mixed signals in both cases: the former shares analog and a few digital signals and the later shares digital and differential signals.

The design fulfills all the requirements for the VFE Unit: On one hand, noise figure achieved in the real experiment is around 2.3mV, the shape and jitter of the critical signals such as 40MHz and 20MHz clock are good; on the other hand, the design of the LVDS link achieved a correct eye diagram after about 25 meter distance. The production itself also accomplishes specifications, after laboratory tests, burn in tests, stability tests as well as the pit tests.

Technology used in this design is related to Calorimetry in high energy physics that not only could be used for particle physics but also for medical proposals.

Calorimetry in high energy physics, astronomy and other physics sciences share many common instrumentation, detector and electronics technology platforms with two nuclear medicine imaging modalities used in clinics and medical research.

Chapter 8: Publications

Chapter 8. Publications

8.1. Introduction

In this chapter, publications produced during the research are presented. The publications are divided into four groups: Conference contributions, Journal publications, Book publications and other publications not related to PhD.

However, a lot of work needs to be done prior to publishing. (This work has taken several years) as a result of being an open experiment, subject to lots of changes in specifications, and also because of the need to previously design a specific ASIC of the detector, which has been a slow process (the final design was achieved after four years of work).

8.2. Book contributions

This section presents an overview of the contributions made to books.

Title	LHCb RICH, Technical Design Report
Authors	LHCb Collaboration
Date	2000
Place	Geneva (Switzerland)
Editorial	CERN

Table 11 Book1:LHCb RICH, Technical Design Report

Title	LHCb Muon System, Technical Design Report
Authors	LHCb Collaboration
Date	2001
Place	Geneva (Switzerland)
Editorial	CERN

Table 12 Book2: LHCb Muon System, Technical Design Report

Title	LHCb Vertex Locator, Technical Design Report
Authors	LHCb Collaboration
Date	2001
Place	Geneva (Switzerland)
Editorial	CERN

Table 13 Book3: LHCb Vertex Locator, Technical Design Report

Title	LHCb Outer Tracker, Technical Design Report
Authors	LHCb Collaboration
Date	2001
Place	Geneva (Switzerland)
Editorial	CERN

Table 14 Book4: LHCb Outer Tracker, Technical Design Report

Title	LHCb Inner Tracker, Technical Design Report
Authors	LHCb Collaboration
Date	2002
Place	Geneva (Switzerland)
Editorial	CERN

Table 15 Book5: LHCb Inner Tracker, Technical Design Report

Title	LHCb Reoptimized Detector Design and performance, Technical Design Report
Authors	LHCb Collaboration
Date	2003
Place	Geneva (Switzerland)
Editorial	CERN

Table 16 Book6: LHCb Reoptimized Detector Design and performance, Technical Design Report

Title	LHCb Trigger System, Technical Design Report
Authors	LHCb Collaboration
Date	2003
Place	Geneva (Switzerland)
Editorial	CERN

Table 17 Book7: LHCb Trigger System, Technical Design Report

Title	Calorimetry in High Energy Physics
Authors	XII International Conference
Date	2006
Place	Chicago (USA)
Editorial	Argonne National Laboratory

Table 18 Book 8: Calorimetry in High Energy Physics

8.3. Contributions to Conferences

This section presents an overview of the contributions made to international conferences.

Conference	4th Conference on New Developments in Photodetection
Title	SPD Very Front End Electronics
Authors	S.Luengo, J. Riera, S. Tortella, X. Vilasis, A. Comerma, D. Gascon, L. Garrido
Date	June 2005
Place	Beaune (France)
Official Language	English
Organization	CNRS, IN2P3, DSM, CEA
Periodicity	Triannual

Table 19 Beaune Conference

Conference	11th Workshop on Electronics for LHC and future Experiments (LECC'05)
Title	Scintillator Pad Detector Very Front End Electronics
Authors	S.Luengo, J. Riera, S. Tortella, X. Vilasis, A. Comerma, D. Gascon, L. Garrido
Date	September 2005
Place	Heidelberg (Germany)
Official Language	English
Organization	CERN, Kirchhof Institute, Max-Plank Institute
Periodicity	Annual

Table 20 Heidelberg Conference

Conference	The 10th International Conference on Accelerator and Large Experimental Physics Control System (ICALEPCS'05)
Title	SPD Very Front End Electronics
Authors	S.Luengo, J. Riera, S. Tortella, X. Vilasis, A. Comerma, D. Gascon, L. Garrido
Date	October 2005
Place	Geneva (Switzerland)
Official Language	English
Organization	CERN, CRPP-EPFL, EPS-EPCS
Periodicity	Biannual

Table 21 Geneva Conference

Conference	XII INTERNATIONAL CONFERENCE on CALORIMETRY in HIGH ENERGY PHYSICS (CALOR'06)
Title	Scintillator Pad Detector: Very Front End Electronics
Authors	S.Luengo, J. Riera, S. Tortella, X. Vilasis, L. Garrido
Date	June 2006
Place	Chicago (USA)
Official Language	English
Organization	ARGONNE, University of Chicago
Periodicity	Biannual

Table 22 Chicago Conference

Conference	12th Workshop on Electronics for LHC and future Experiments (LECC'06)
Title	The Front End Electronics of the Scintillator Pad Detector of the LHCb Calorimeter
Authors	C. Abellan , S. Bota, A. Comerma, A. Dieguez, L. Garrido, D. Gascon, A. Gaspar, R. Graciani, E. Grauges , A. Herms , M. Llorens , S. Luengo , E. Picatoste , J. Riera, H. Ruiz , S. Tortella , X. Vilasis
Date	September 2006
Place	Valencia (Spain)
Official Language	English
Organization	University of Valencia
Periodicity	Annual

Table 23 Valencia Conference

8.4. Contribution to Journals

This section presents an overview of the contributions made to journals.

Title	LHCb Calorimeters, Technical Design Report
Authors	LHCb Collaboration
Date	2000
Journal	LHCC-2000-0036
Pages	

Table 24 Journal 1: LHCb Calorimeters, Technical Design Report

Title	SPD Very Front End Electronics
Authors	S.Luengo, J. Riera, S. Tortella, X. Vilasis, A. Comerma, D. Gascon, L. Garrido
Date	2005
Journal	Nuclear and Instrumentation Methods, A
Pages	310-314

Table 25 Journal 2: SPD Very Front End Electronics

8.5. Other

This section presents an overview of the contributions made to conferences, journals and patents that are not related to the PhD.

Journals

Title	Guiding a mobile robot with Cellular Neural Networks
Authors	X.Vilasís-Cardona, S.Luengo, J.Solsona, G.Apicella, A.Maraschini, M.Balsi
Date	2002
Journal	International Journal of Circuit Theory and Applications Volume 30
Pages	612-624

Table 26 Journal3: Guiding a mobile robot with Cellular Neural Networks

Title	Fabric Tactil Panel
Authors	M.Alsina, F.Escudero, J. Margalef, S. Luengo
Date	2007
Journal	Sensors, ISSN 1424-8220
Pages	In press

Table 27 Journal 4: Fabric Tactil Panel

Title	Determining position inside non-industrial buildings using ultrasound transducers
Authors	F.Escudero , J. Margalef, S. Luengo, M. Alsina, J. M. Ribes, J. Pérez
Date	2007
Journal	Sensors, ISSN 1424-8220
Pages	In press

Table 28 Journal 5: Determining position inside non-industrial buildings using ultrasound transducers

Conferences

Conference	6th International Work Conference on Artificial Neural Networks 2001
Title	Cellular Neural Networks for mobile robot vision
Authors	Marco Balsi, Alessandro Maraschini, Giada Apicella, Sonia Luengo, Jordi Solsona, Xavier Vilasís Cardona
Date	June 2001
Place	Granada (Spain)
Official Language	English
Periodicity	Biannual
Publication	Proceedings of IWANN 2001, J.Mira, A.Prieto (Eds.) Lecture Notes in Computer Science 2085, pp 484-491, Springer Verlag 2001.

Table 29 Granada Conference

Conference	Autonomous Minirobots for Research and Edutainment (AMiRE) 2001
Title	Cellular Neural Networks for mobile robot vision in a structured environment.
Authors	Marco Balsi, Alessandro Maraschini, Giada Apicella, Sonia Luengo, Jordi Solsona, Xavier Vilasís Cardona
Date	October 2001
Place	Padeborn (Germany)
Official Language	English
Periodicity	Biannual
Publication	Proceedings of AmiRE 2001, U.Rückert, J.Sitte, U.Witkowksy (Eds.) Heinz Nixdorf Institute 2001

Table 30 Padeborn Conference

Conference	4rt Congrés Català d'Intel·ligència Artificial
Title	Mobile Robot Guidance Using Cellular Neural Networks and Fuzzy Logic
Authors	Marco Balsi, Alessandro Maraschini, Giada Apicella, Sonia Luengo, Jordi Solsona, Xavier Vilasís Cardona
Date	October 2001
Place	Barcelona (Spain)
Official Language	English
Periodicity	Annual

Table 31 Barcelona Conference

Conference	Proceedings of International Conference on Computational Intelligence, Robotics and Autonomous Systems (CIRAS 2001)
Title	Robot Vision using Cellular Neural Networks
Authors	Xavier Vilasís-Cardona, Sonia Luengo, Jordi Solsona, Giada Apicella, Alessandro Maraschini, Marco Balsi
Date	November 2001
Place	Singapore
Official Language	English
Periodicity	Annual
Publication	Proceedings of International Conference on Computational Intelligence,Robotics and Autonomous Systems CIRAS 2001. K.K.Tan, S.Y.Lim (Editors) ISSN 0219-6131. pp 367-372.

Table 32 Singapore Conference

Patents

Patent number	P200403022
Title	Alfombra con Detector de Presencia
Authors	V. Cambra, J. Gisbert, F. Escudero, S. Luengo
Date	2007

Table 33 Patent 1: Alfombra con Detector de Presencia

Patent number	P20071599
Title	Sistema de localizacion
Authors	Francesc Escudero, Sonia Luengo i Maria Alsina
Date	2007

Table 34 Patent 2: Sistema de localizacion

Patent number	P20071598
Title	Rugosímetro
Authors	Francesc Escudero, Sonia Luengo, Maria Alsina, Jordi Margalef
Date	2007

Table 35 Patent 3: Rugosímetro

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Appendix 1: Mappings

The four different mappings that the VFE Unit can have are depicted below.

Bottom Mapping

MAPMT	PS FE	SPD detector
1	18	64
2	20	48
3	2	63
4	4	47
5	12	62
6	10	46
7	28	61
8	26	45
9	46	38
10	48	54
11	62	37
12	64	53
13	56	40
14	54	56
15	40	39
16	38	55
17	21	28
18	23	12
19	5	27
20	7	11
21	15	26
22	13	10
23	31	25
24	29	9
25	41	2
26	43	18
27	57	1
28	59	17
29	51	4
30	49	20
31	35	3
32	33	19
33	17	60
34	19	44
35	1	59
36	3	43
37	11	58
38	9	42
39	27	57
40	25	41

41	45	34
42	47	50
43	61	33
44	63	49
45	55	36
46	53	52
47	39	35
48	37	51
49	22	32
50	24	16
51	6	31
52	8	15
53	16	30
54	14	14
55	32	29
56	30	13
57	42	6
58	44	22
59	58	5
60	60	21
61	52	8
62	50	24
63	36	7
64	34	23

Bottom Half Mapping

MAPMT	PS FE	SPD detector
33	17	28
34	19	12
35	1	27
36	3	11
37	11	26
38	9	10
39	27	25
40	25	9
41	13	2
42	15	18
43	29	1
44	31	17
45	23	4
46	21	20
47	7	3
48	5	19
49	18	32
50	20	16
51	2	31
52	4	15

53	12	30
54	10	14
55	28	29
56	26	13
57	14	6
58	16	22
59	30	5
60	32	21
61	24	8
62	22	24
63	8	7
64	6	23

Top Mapping

MAPMT	PS FE	SPD detector
1	8	1
2	6	17
3	24	2
4	22	18
5	30	3
6	32	19
7	14	4
8	16	20
9	60	27
10	58	11
11	44	28
12	42	12
13	34	25
14	36	9
15	50	26
16	52	10
17	3	37
18	1	53
19	19	38
20	17	54
21	25	39
22	27	55
23	9	40
24	11	56
25	63	63
26	61	47
27	47	64
28	45	48
29	37	61
30	39	45

31	53	62
32	55	46
33	7	5
34	5	21
35	23	6
36	21	22
37	29	7
38	31	23
39	13	8
40	15	24
41	59	31
42	57	15
43	43	32
44	41	16
45	33	29
46	35	13
47	49	30
48	51	14
49	4	33
50	2	49
51	20	34
52	18	50
53	26	35
54	28	51
55	10	36
56	12	52
57	64	59
58	62	43
59	48	60
60	46	44
61	38	57
62	40	41
63	54	58
64	56	42

Top Half Mapping

MAPMT	PS FE	SPD detector
33	3	5
34	1	21
35	19	6
36	17	22
37	25	7
38	27	23
39	9	8

40	11	24
41	31	31
42	29	15
43	15	32
44	13	16
45	5	29
46	7	13
47	21	30
48	23	14
49	4	1
50	2	17
51	20	2
52	18	18
53	26	3
54	28	19
55	10	4
56	12	20
57	32	27
58	30	11
59	16	28
60	14	12
61	6	25
62	8	9
63	22	26
64	24	10

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